MECHANICAL COMPONENTS

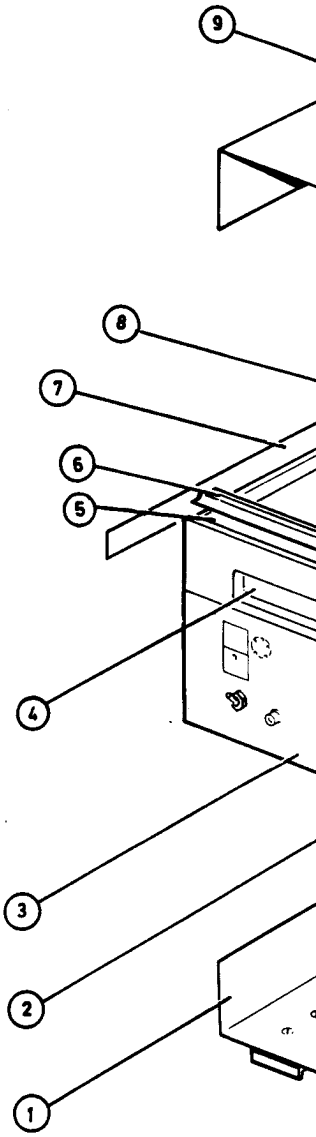
31. Order without prefix.

Fig. 1

Item	Description	Part no.
1	Bottom outer cover	35903-279B
2	Front panel switch caps, marked:-	
	STORE	37590-323X
	RECALL	37590-324M
	MOD OSC	37590-371U
	MOD ALC	37590-372Y
	INCREMENT	37590-373N
	CARRIER FREQ	37590-374L
	FM	37590-375J
	AM	37590-376F
	RF LEVEL	37590-377G
	7	37590-334H
	4	37590-331K
	1	37590-328K
	0	37590-325C
	8	37590-335E
	5	37590-332A
	2	37590-329A
	.	37590-326R
	9	37590-336U
	6	37590-333Z
	3	37590-330B
	-	37590-327B
	MHz/V	37590-390X
	kHz/mV	37590-391M
	Hz/µV	37590-392C
	%/dB	37590-393R
	INT/EXT	37590-394B
	TOTAL	37590-395K
	UP	37590-396A
	ON/OFF	37590-397Z
	RETURN	37590-398H
	DOWN	37590-399E
	SECOND FUNCT	37590-400B
3	Front panel assy.	35903-115A
4	Carrier frequency bezel	37590-408N
	Modulation and r.f. level bezel	37590-409L
5	Front trim panel	34900-477G
6	Front trim infill	35902-371Z
7	Left-hand side trim infill	35902-384V
8	Left-hand side frame assy.	35903-314M
9	Top outer cover	35903-278R
10	Back foot	37590-514L
	Stud	37590-223C

Fig. 1

Item	Description	Part no
11	Selector plate	35902-441Z
12	Rear trim	34900-470E
13	Rear panel assy.	35903-229F
14	End cap	37590-255C
	End cap	37590-256R
15	Liner	22315-584T
16	Cover moulding	37590-257B
17	Steel liner	22315-587M
18	Right-hand side trim infill	35902-386W
19	Side rail assy.	34900-723V
20	Right-hand side frame assy.	35903-315C
21	PVC extrusion	22315-590M
22	Bush	35900-785V
23	Rear lower foot	37590-224R
	Stud	37590-223C
24	Side trim infill (handle)	35902-368Z
25	Screw	21857-465C
26	Screw cup washer	21171-550W
27	Front foot	37590-253X
	Tilt stand	37590-254M



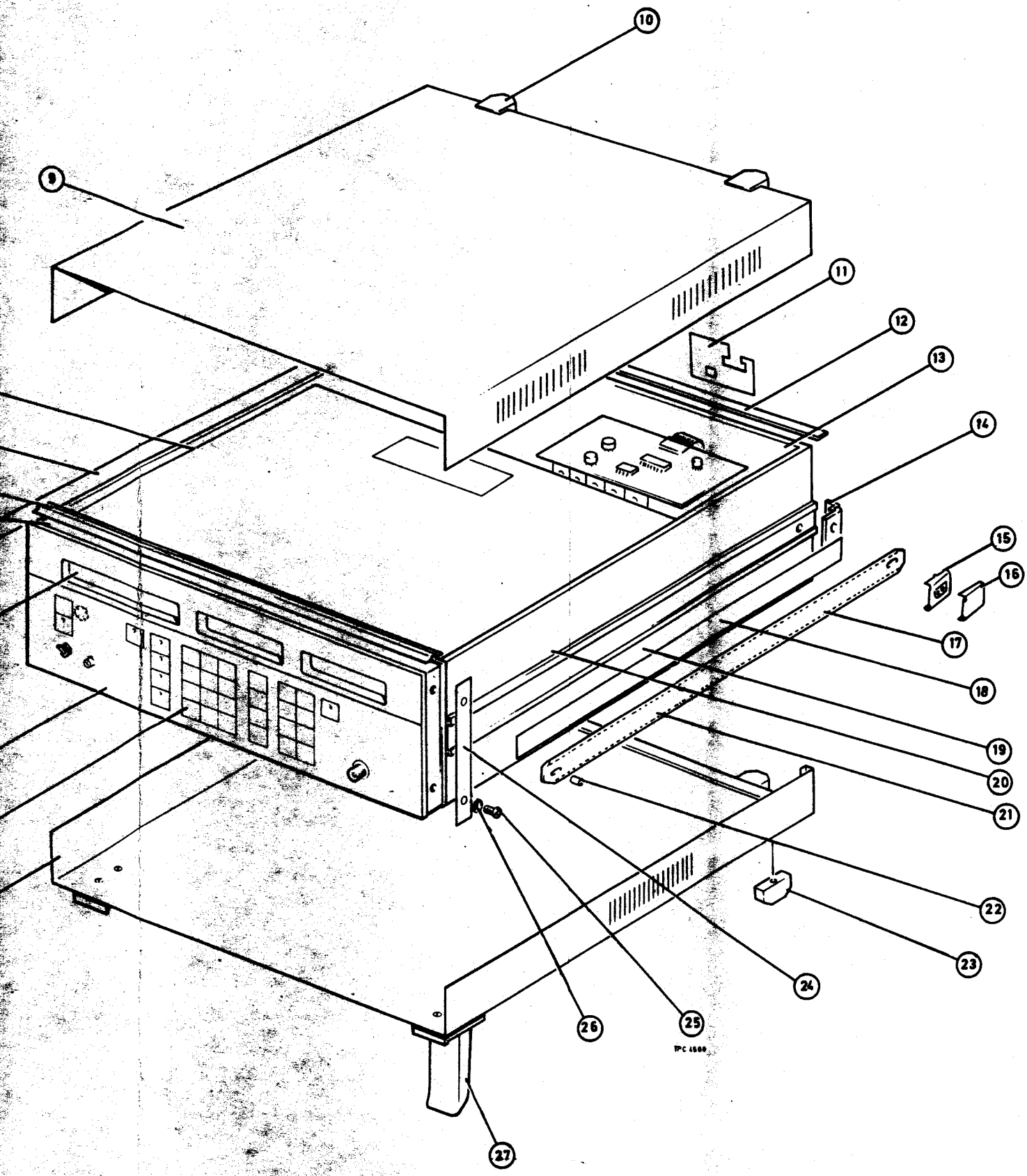


Fig. 1 ***Miscellaneous mechanical*** *parts*

Chapter 7

SERVICING DIAGRAMS

CONTENTS

CIRCUIT NOTES

1. Component values

Resistors : Code letter R = ohms, k = kilohms (10^3), M = megohms (10^6).

Capacitors : Code letter m = millifarads (10^{-3}), µ = microfarads (10^{-6}), n = nanofarads (10^{-9}), p = picofarads (10^{-12}).

Inductors : Code letter H = henrys, m = millihenrys (10^{-3}), µ = microhenrys (10^{-6}), n = nanohenrys (10^{-9}).

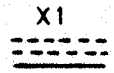
† SIC : value selected during test, nominal value shown.

2. Components are marked normally with two, three or four figures according to the accuracy limit ±10%, ±1% or ±0.1%. The code letter used indicates the multiplier and replaces the decimal point. Because a marking 4m7 could be interpreted as milliohms, millifarads or millihenrys all values are placed near to its related symbol.

3. Symbols

Symbols are based on the provisions of BS 3939 with the following additions :


edge connector



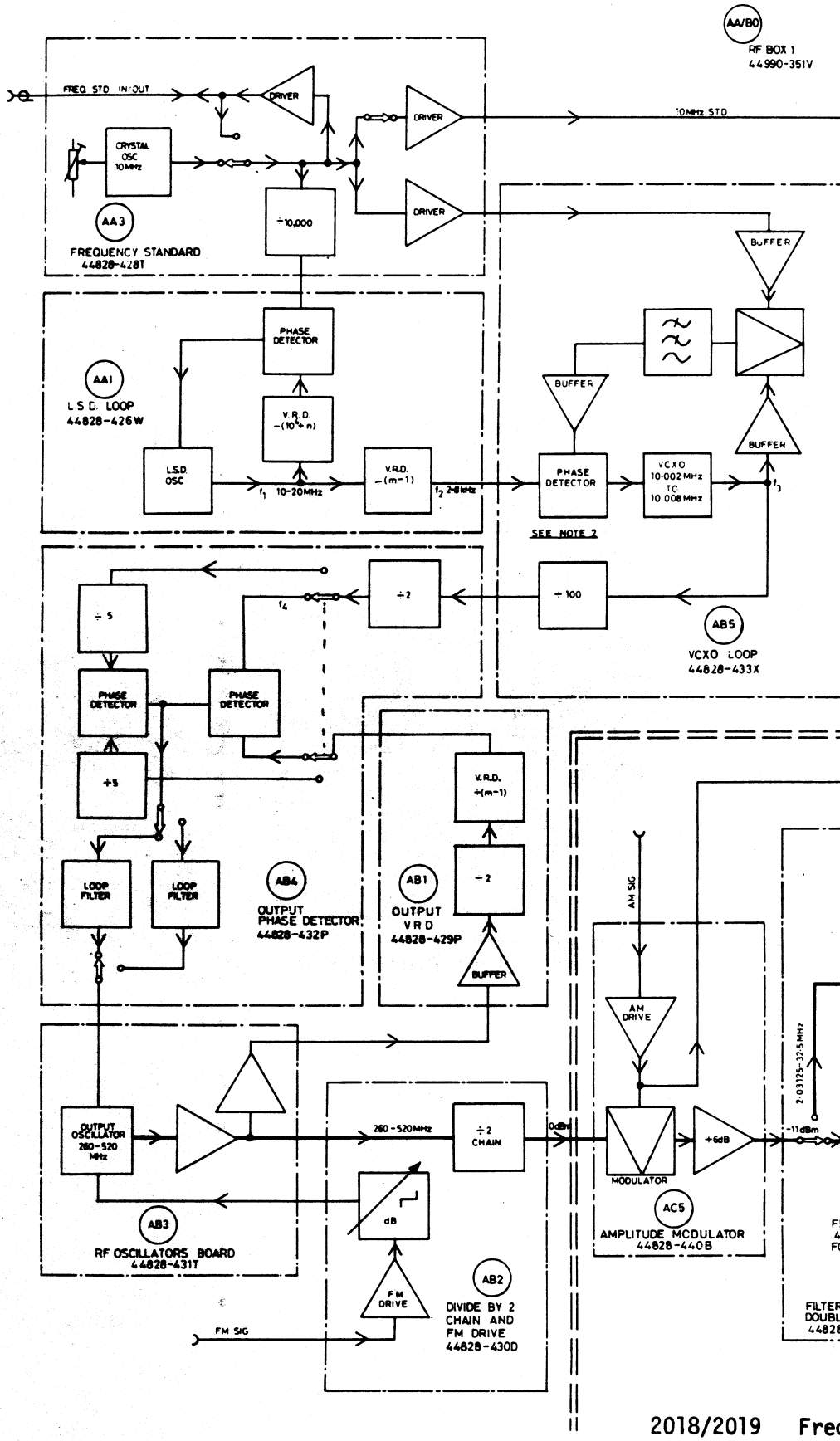
ferrite bead


warning, see page (iv), notes and cautions


Beryllia : health hazard, see page (iv), notes and cautions

unit identification number

P printed component



2018/2019 Freq

Fig. 1

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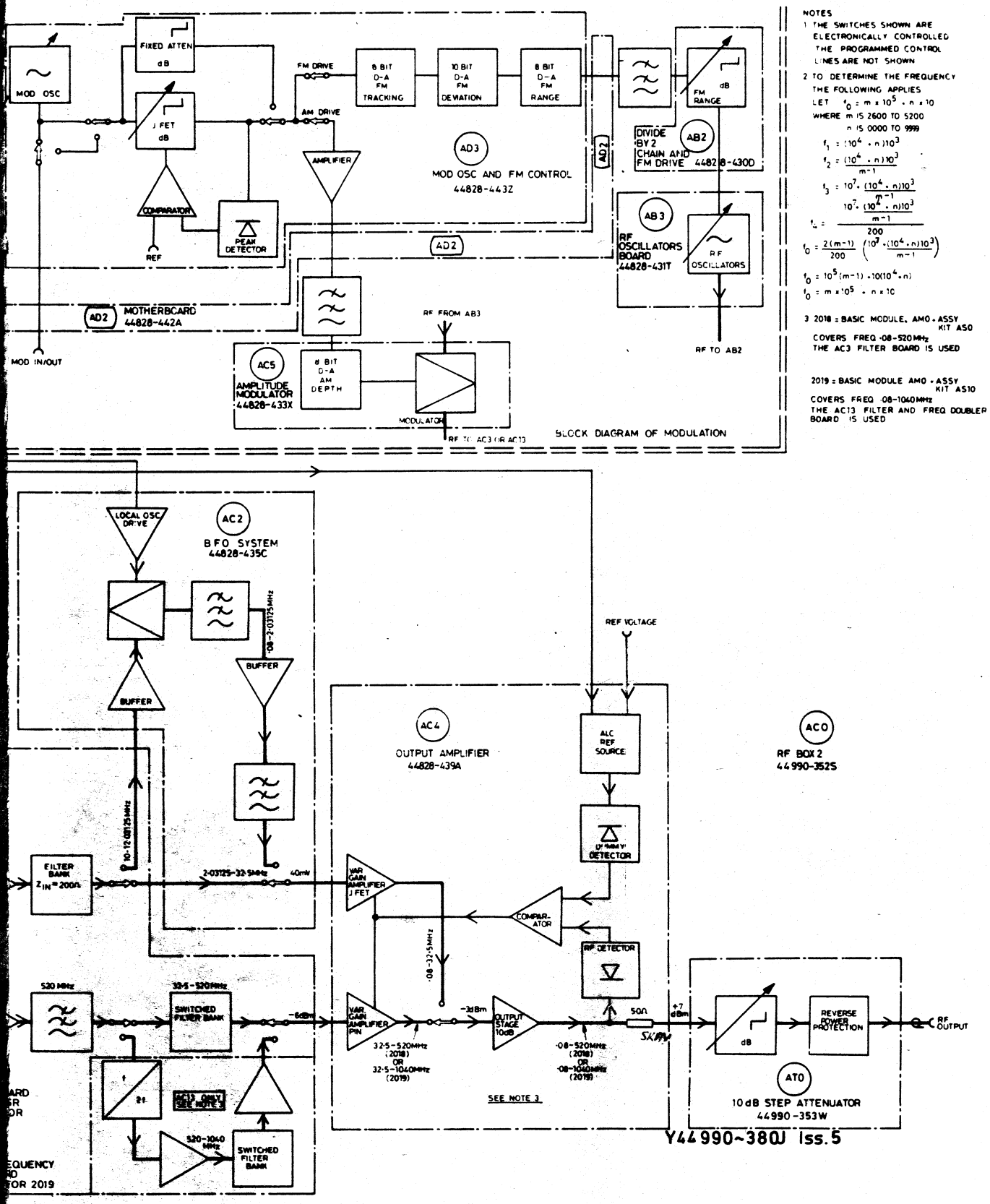
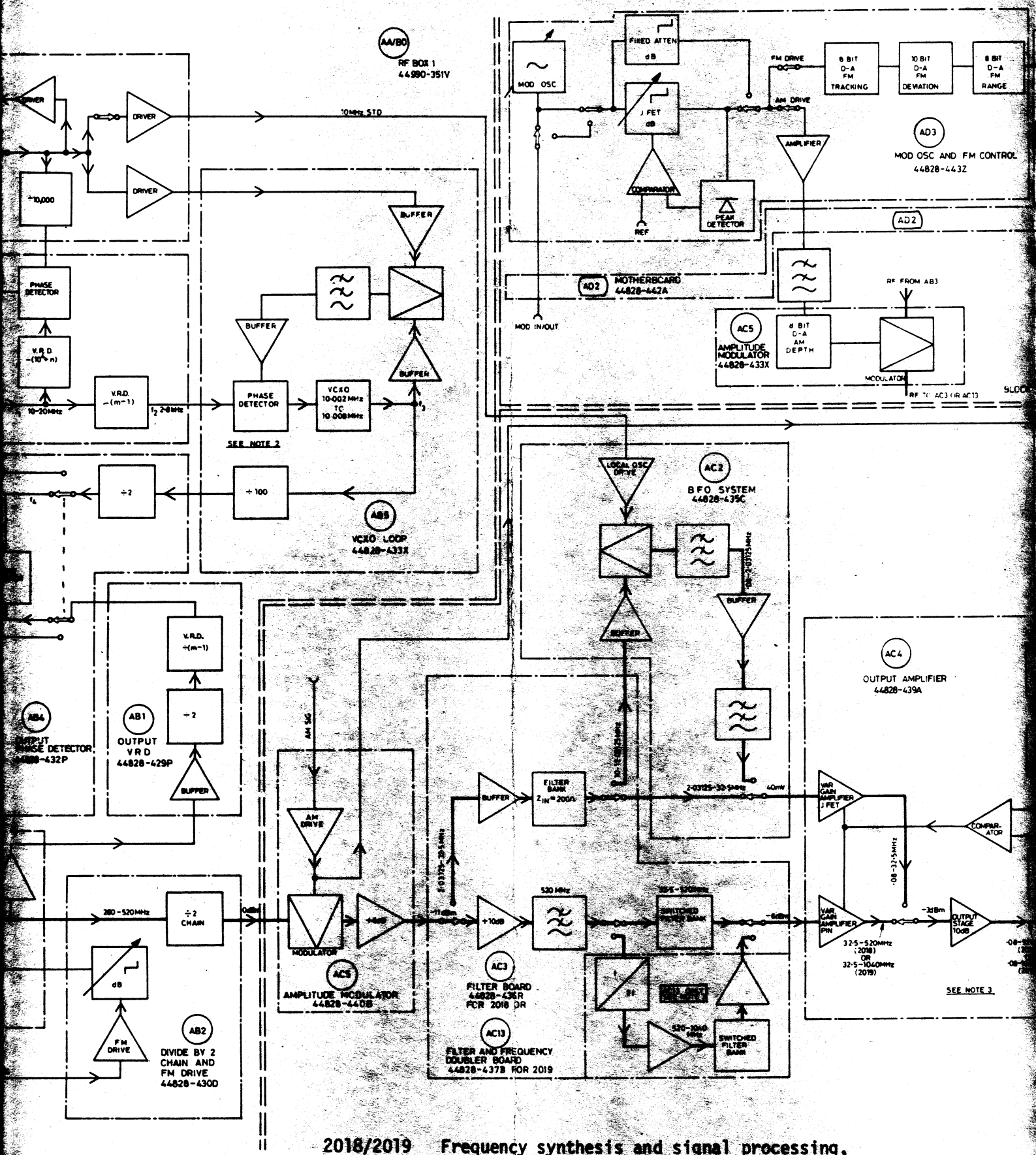
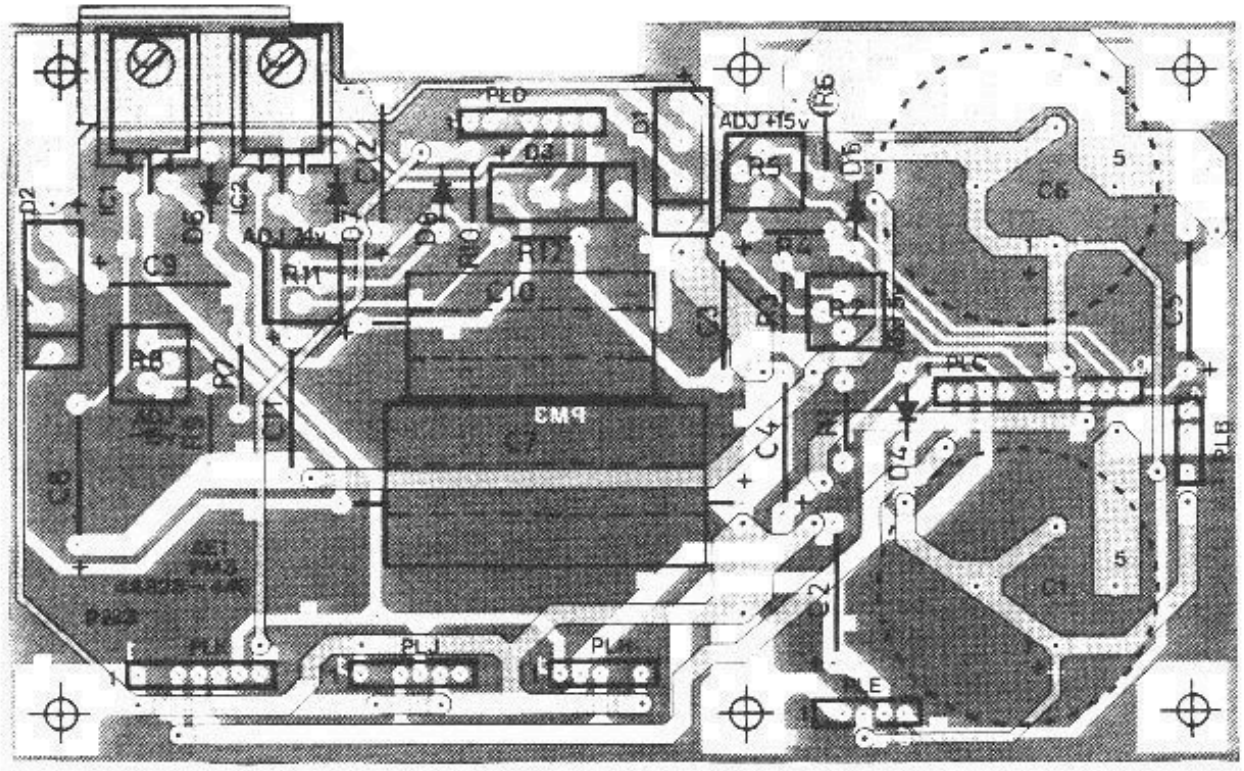


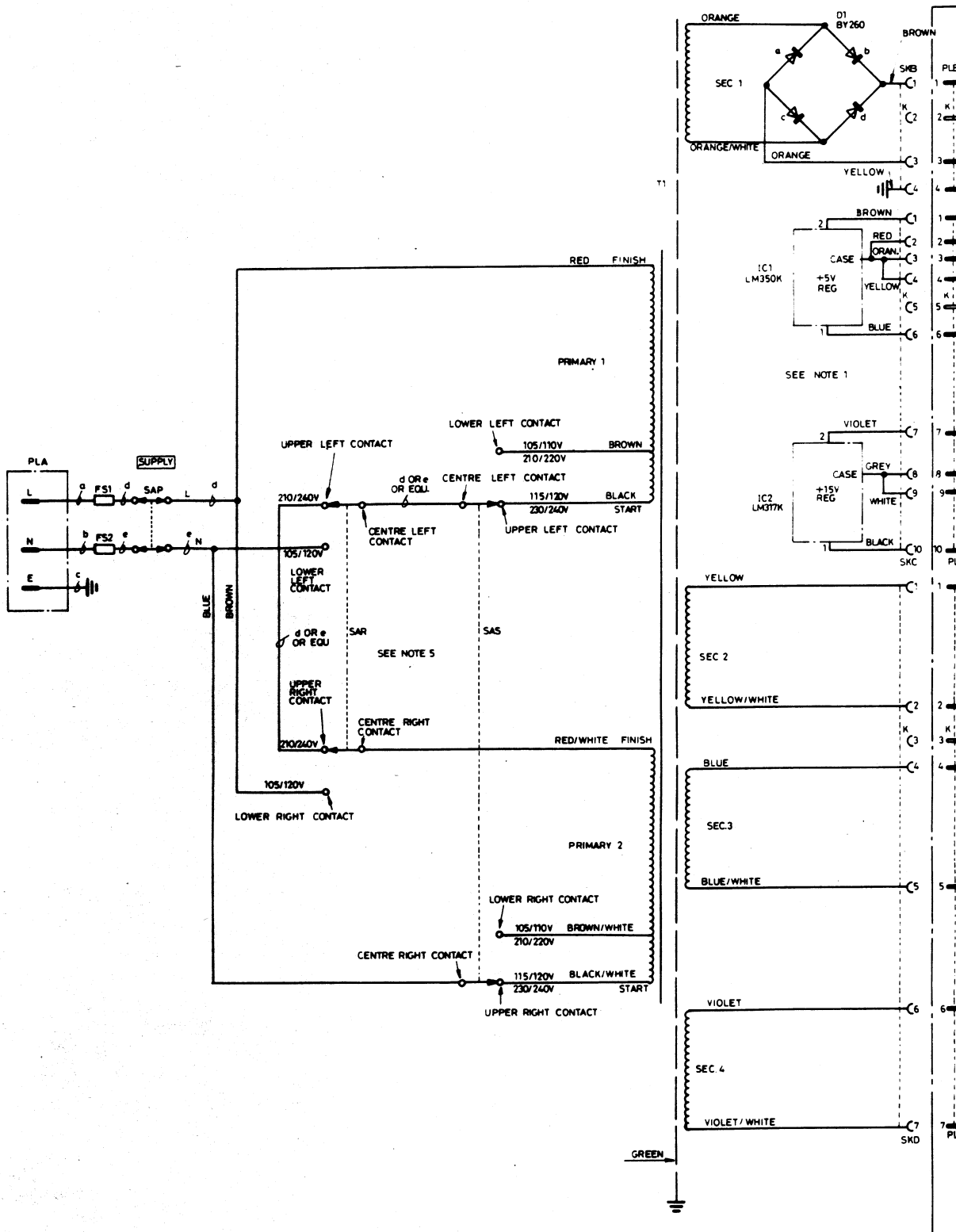
y synthesis and signal processing,
ified block diagram



2018/2019 Frequency synthesis and signal processing, simplified block diagram



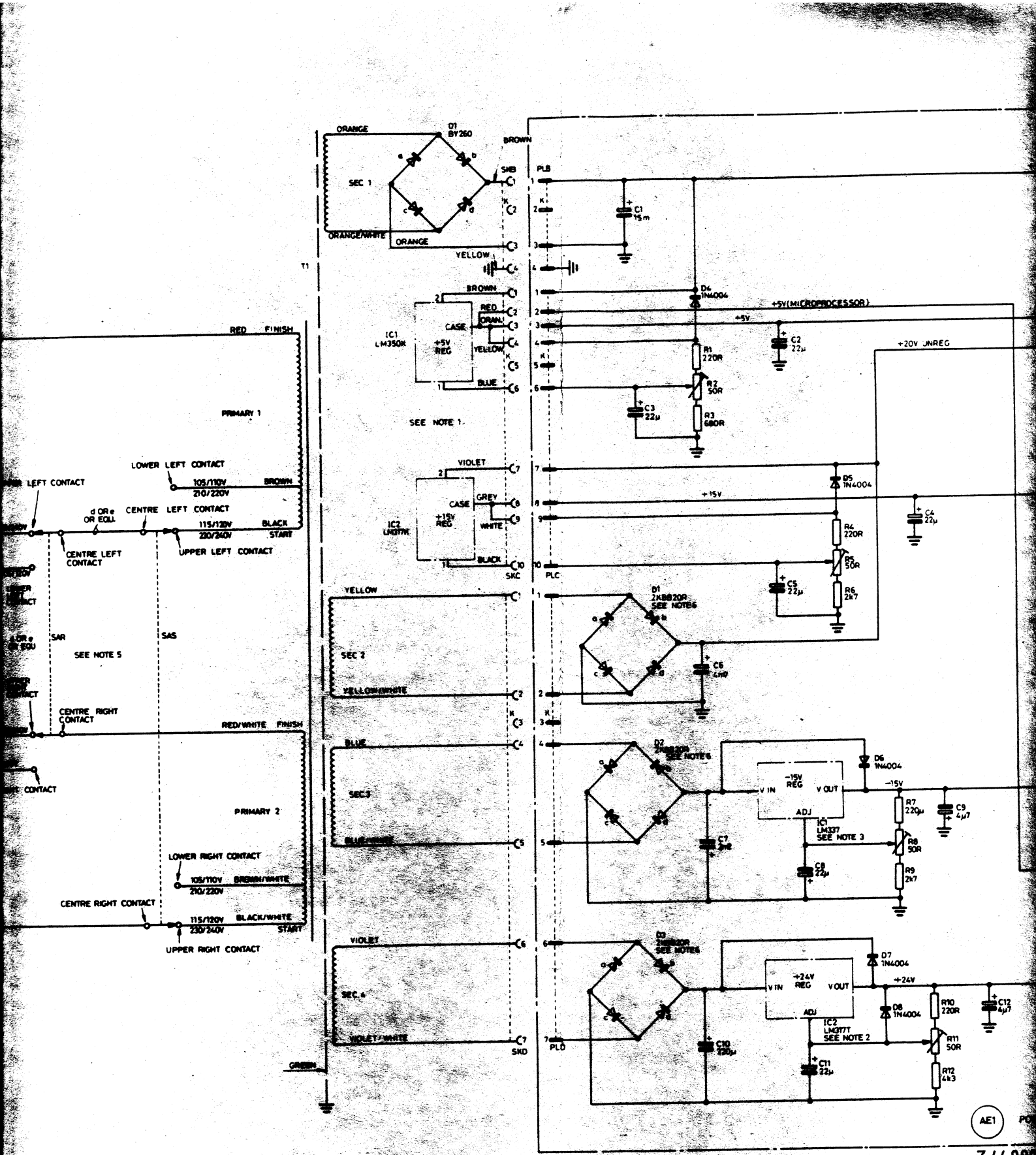
Component layout, AE1



Power suppl

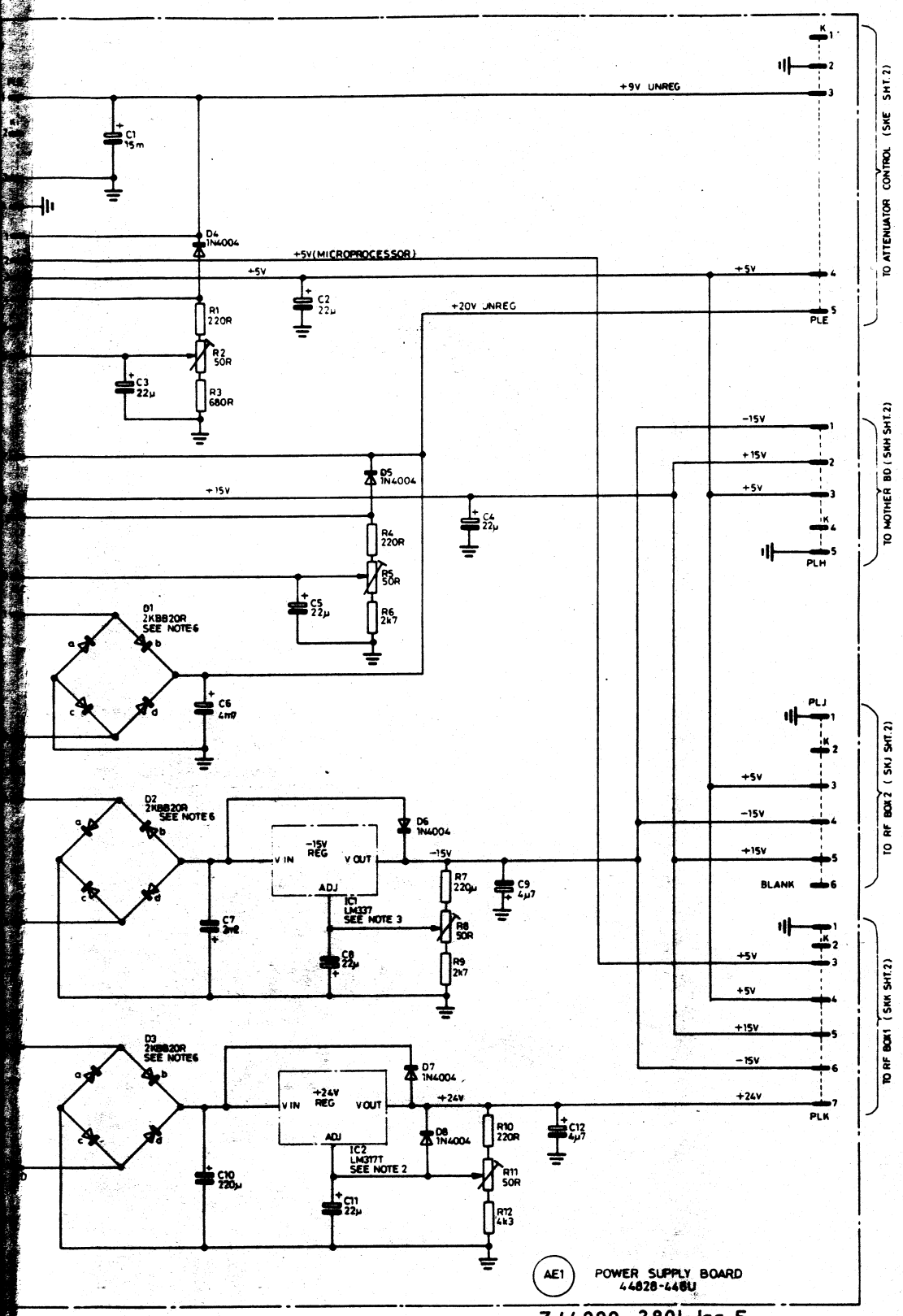
Fig. 2

Sep. 81



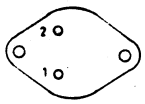
Z 4499

Power supplies, AM0 (includes board AE1)



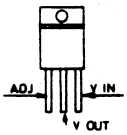
Z 44 990-380J Iss. 5

1



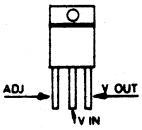
LM350K
LM317K
VIEW ON PIN SIDE

2



LM317T
VIEW FROM TOP

3



LM337T
VIEW FROM TOP

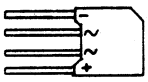
4. WIRES MARKED AS FOLLOWS

a ARE 15410-227T
b ARE 15410-222G
c ARE 15420-278U
d ARE 15410-187W
e ARE 15410-182J

UNMARKED WIRES ARE TO M15410-207 S.S.

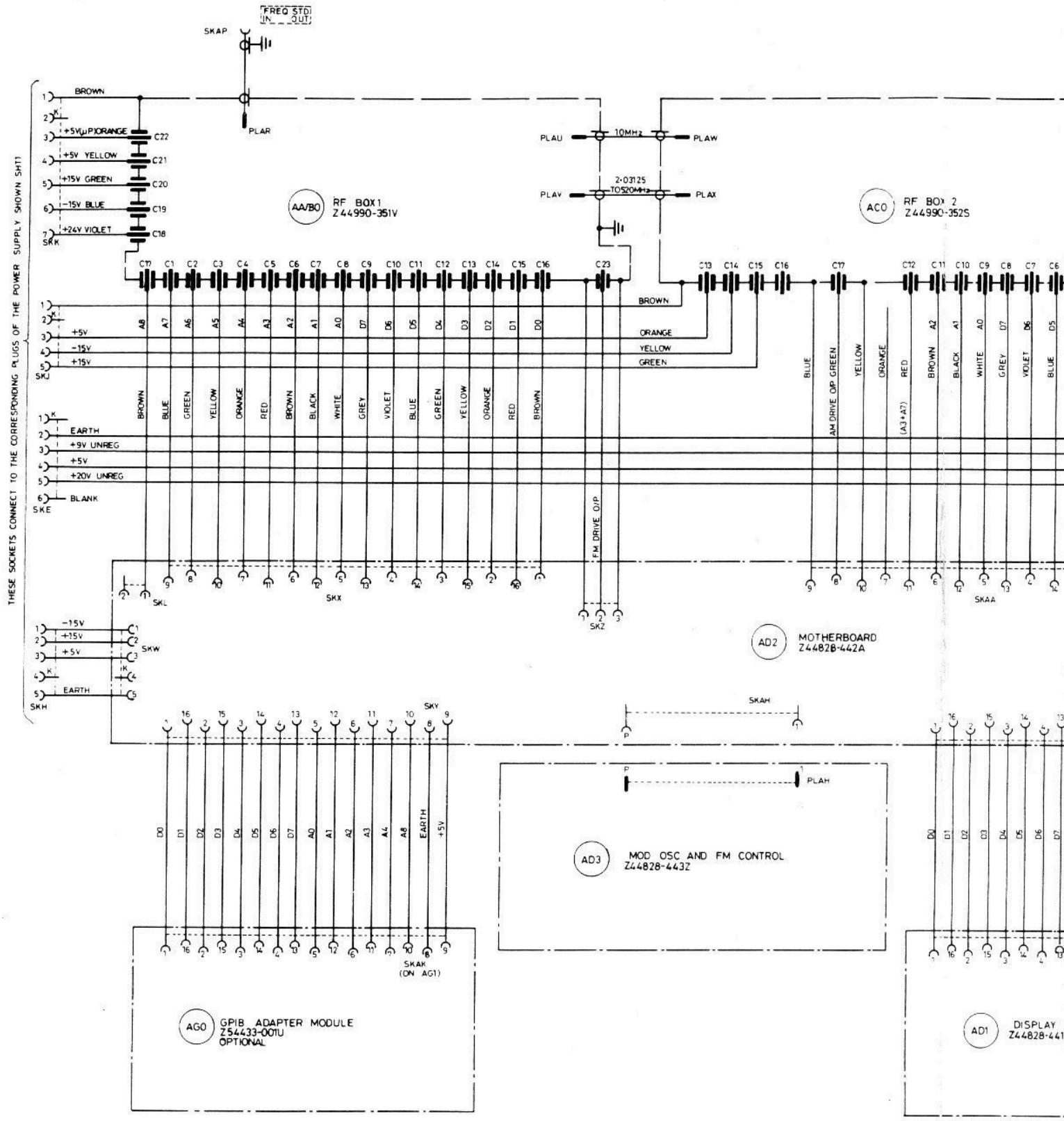
5 LOOKING FROM FRONT OF INST. SWITCH SAR IS TO THE RIGHT OF SAS NOTES OF LEFT AND RIGHT CONTACTS REFER TO THE VIEW FROM THE INST. FRONT

6.



2KBB20R

es, AMO (includes board AE1)



Basic module interconnections, A

Fig. 3

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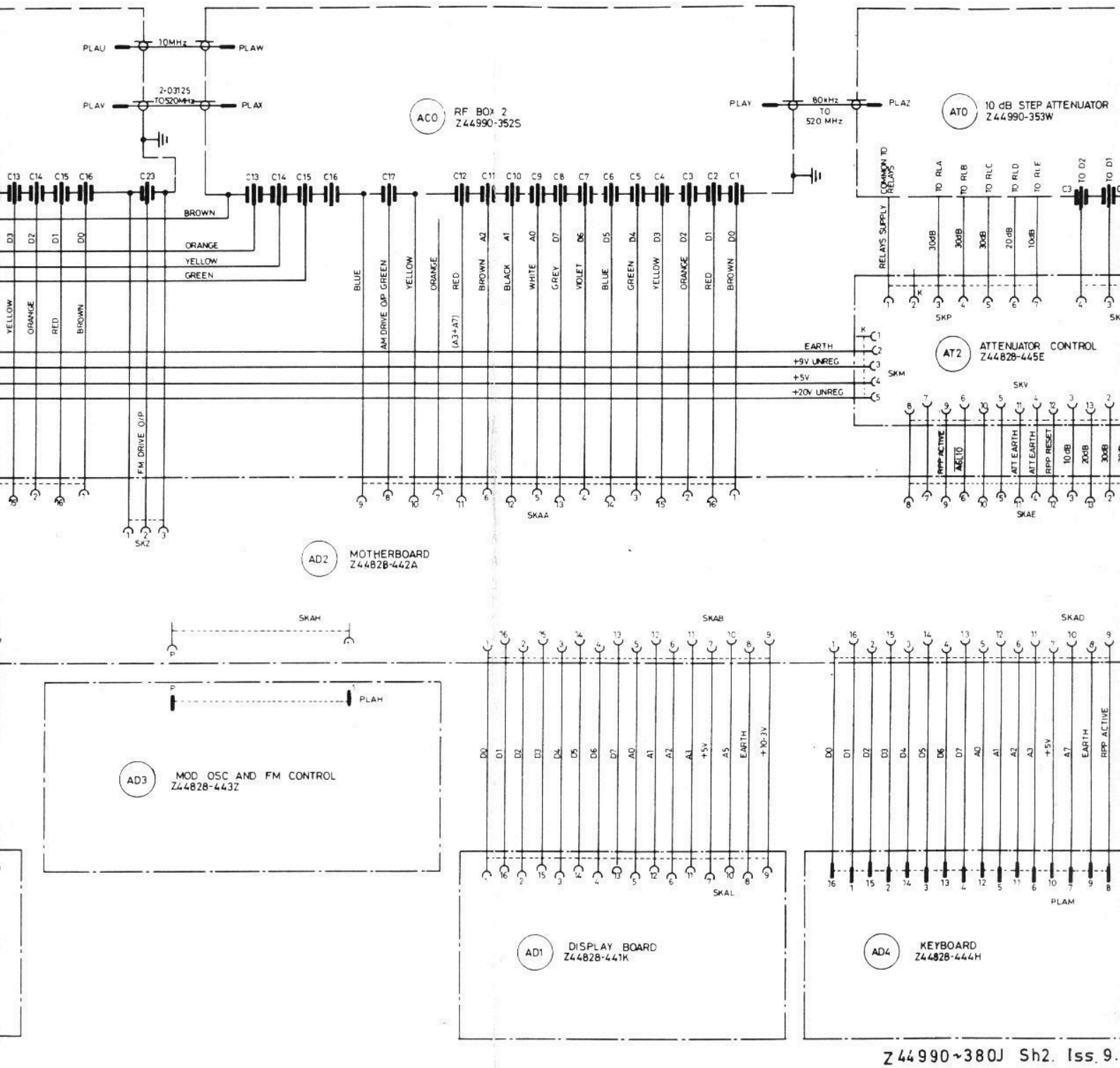
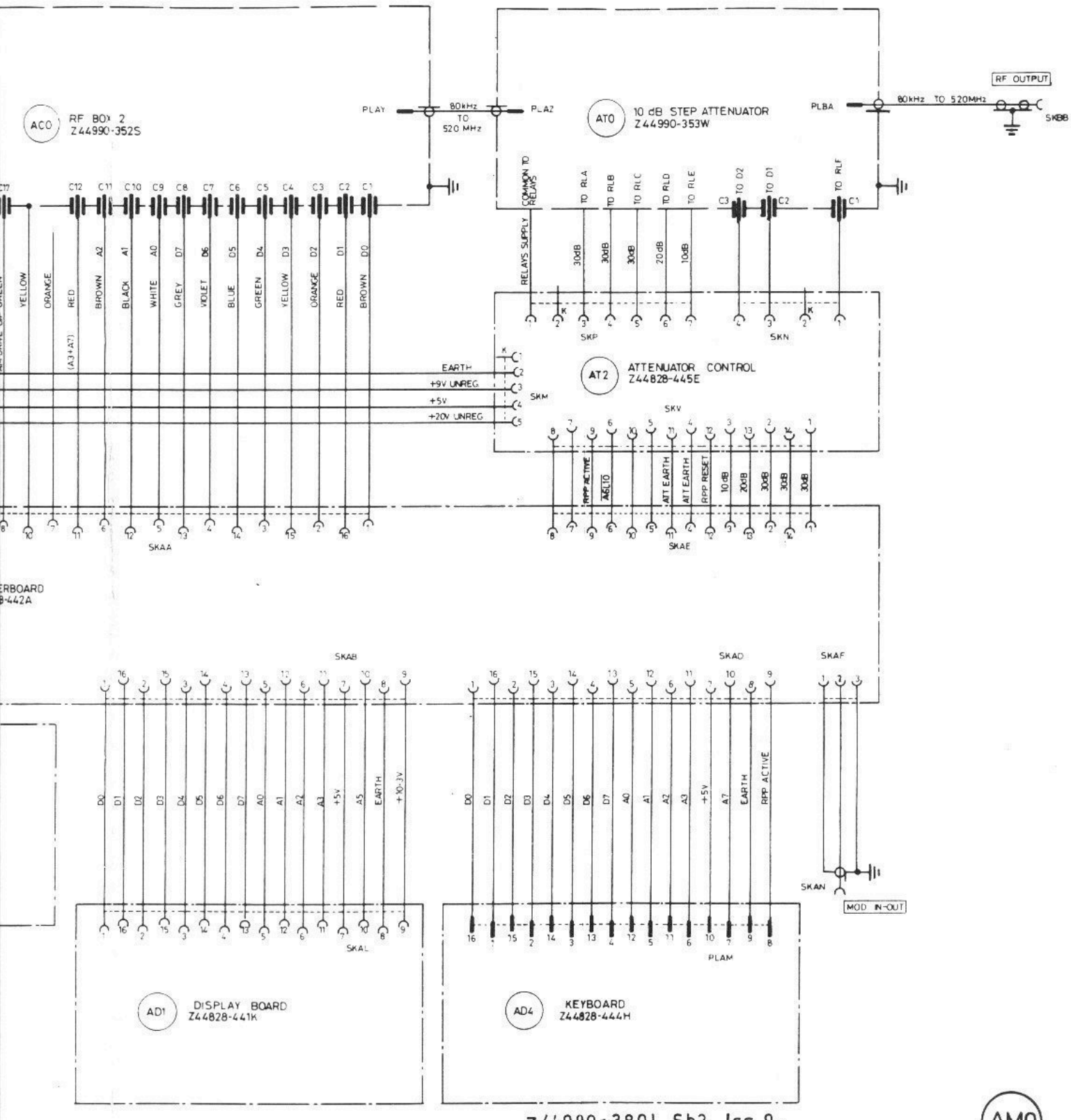


Z44990-380J Sh2. Iss.9.

Basic module interconnections, AM0

1 MATING PLUGS AND SOCKETS CARRY CORRESPONDING IDENTITY ie PLAR PLUGS INTO SKAR THEREFORE IN SOME CASES ONLY ONE OF THE PAIR MAY BE SHOWN
2 THE 1·04 GHz VERSION 52018-301K (A010) IS IDENTICAL EXCEPT FOR RF BOX 2



Z44990-380J Sh2. Iss.9.

dule interconnections, AM0

AM0

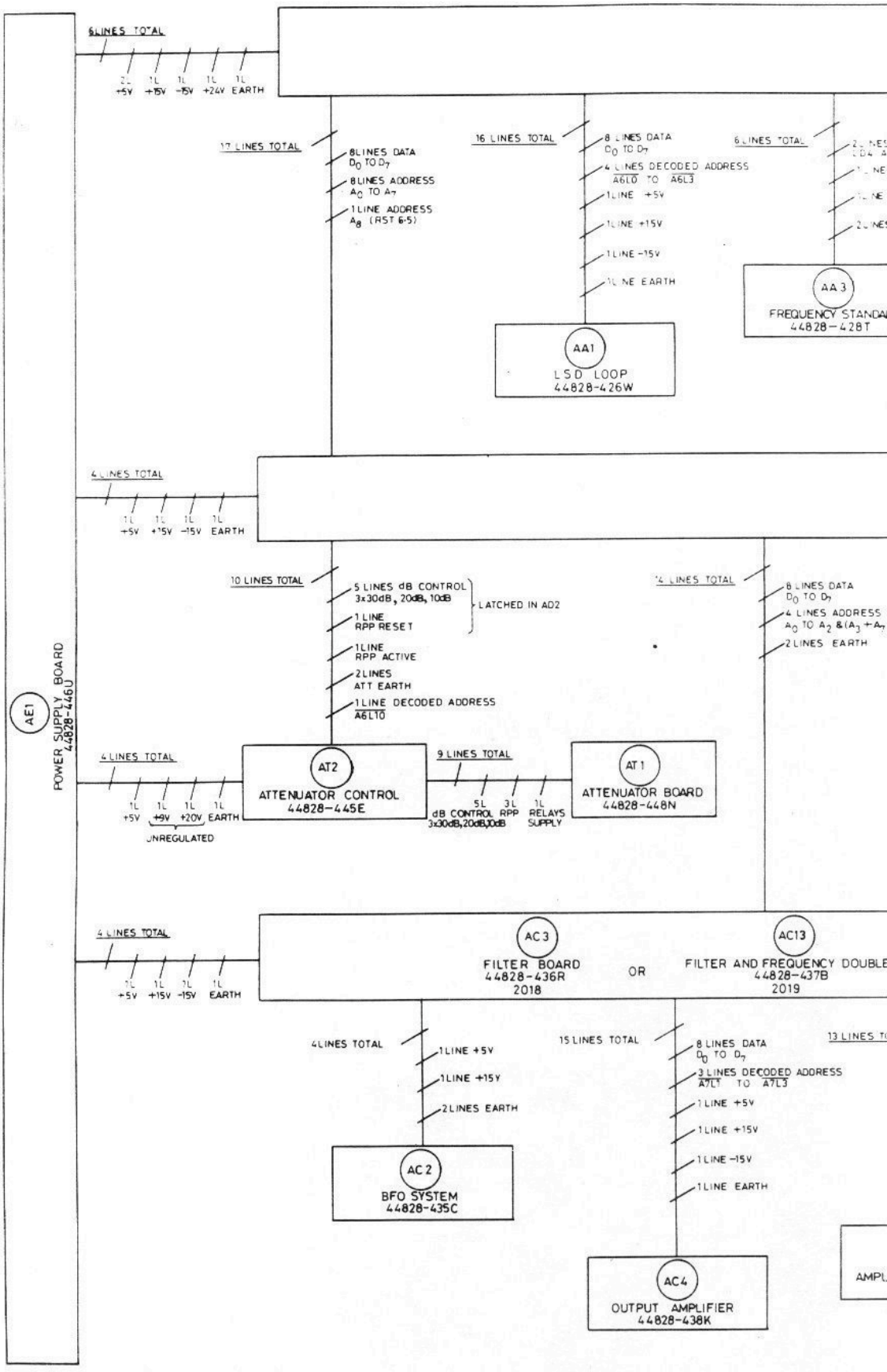

6 LINES TOTAL
2L +5V
1L +15V
1L -15V
1L +24V
1L EARTH
17 LINES TOTAL
8 LINES DATA D0 TO D7
8 LINES ADDRESS A0 TO A7
1 LINE ADDRESS A8 (RST 6·5)
16 LINES TOTAL
8 LINES DATA D0 TO D7
4 LINES DECODED ADDRESS A6L0 TO A6L3
1 LINE +5V
1 LINE +15V
1 LINE -15V
1 LINE EARTH
AA1
LSD LOOP
44828-426W
6 LINES TOTAL
AA3
FREQUENCY STANDA
44828-428T
4 LINES TOTAL
1L +5V
1L +15V
1L -15V
1L EARTH
10 LINES TOTAL
5 LINES dB CONTROL 3x30dB, 20dB, 10dB
LATCHED IN AD2
1 LINE RPP RESET
1 LINE RPP ACTIVE
2 LINES ATT EARTH
1 LINE DECODED ADDRESS A6L10
14 LINES TOTAL
8 LINES DATA D0 TO D7
4 LINES ADDRESS A0 TO A2 &(A3 +A7
2 LINES EARTH
AE1
POWER SUPPLY BOARD
44828-446U
4 LINES TOTAL
1L +5V
1L +9V
1L +20V
1L EARTH
UNREGULATED
AT2
ATTENUATOR CONTROL
44828-445E
9 LINES TOTAL
5L dB CONTROL 3x30dB,20dB,10dB
3L RPP
1L RELAYS SUPPLY
AT1
ATTENUATOR BOARD
44828-448N
4 LINES TOTAL
1L +5V
1L +15V
1L -15V
1L EARTH
AC3
FILTER BOARD
44828-436R
2018
OR
AC13
FILTER AND FREQUENCY DOUBLE
44828-437B
2019
4 LINES TOTAL
1 LINE +5V
1 LINE +15V
2 LINES EARTH
AC2
BFO SYSTEM
44828-435C
15 LINES TOTAL
8 LINES DATA D0 TO D7
3 LINES DECODED ADDRESS A7L1 TO A7L3
1 LINE +5V
1 LINE +15V
1 LINE -15V
1 LINE EARTH
AC4
OUTPUT AMPLIFIER
44828-438K

Fig. 4

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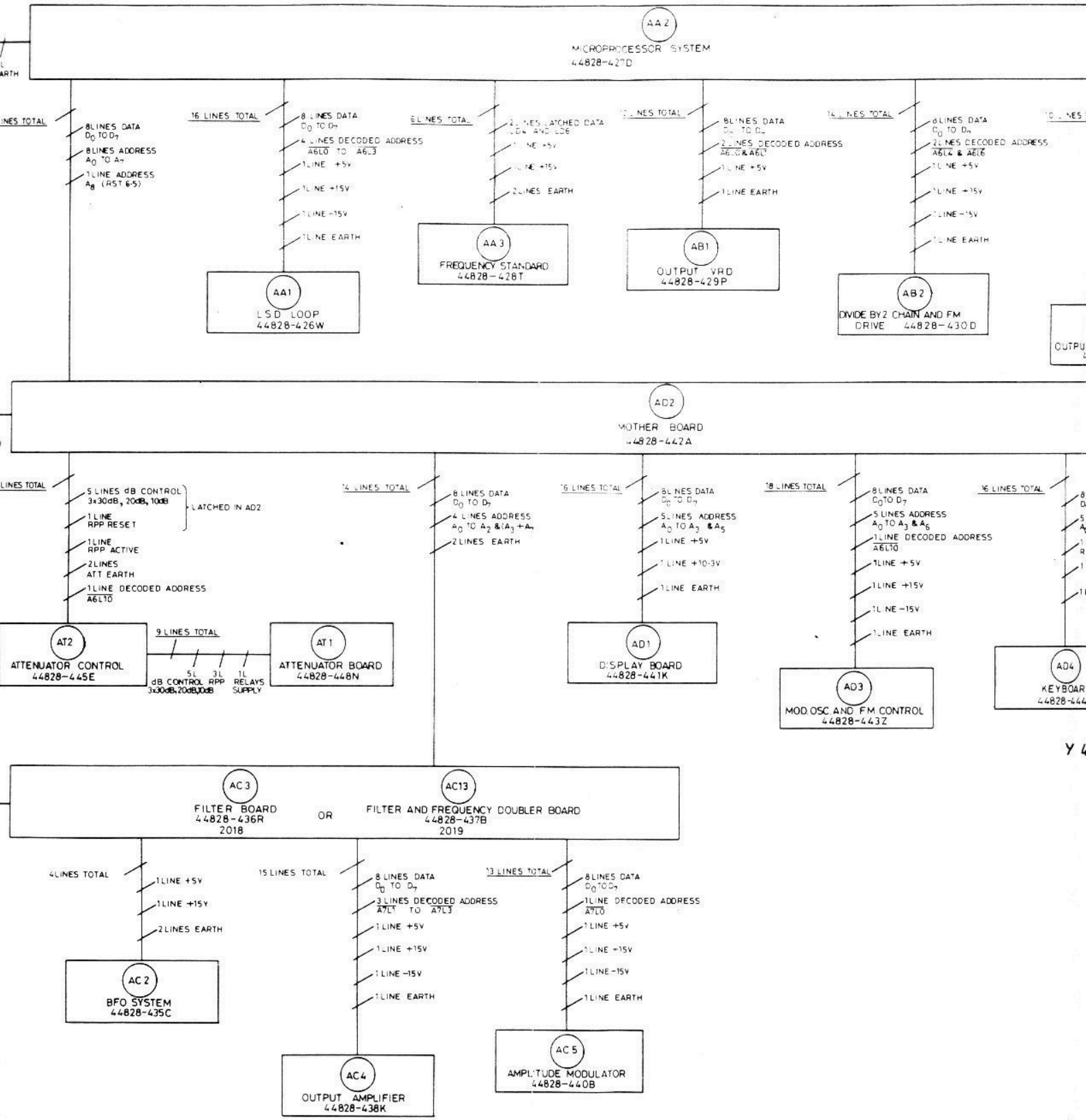
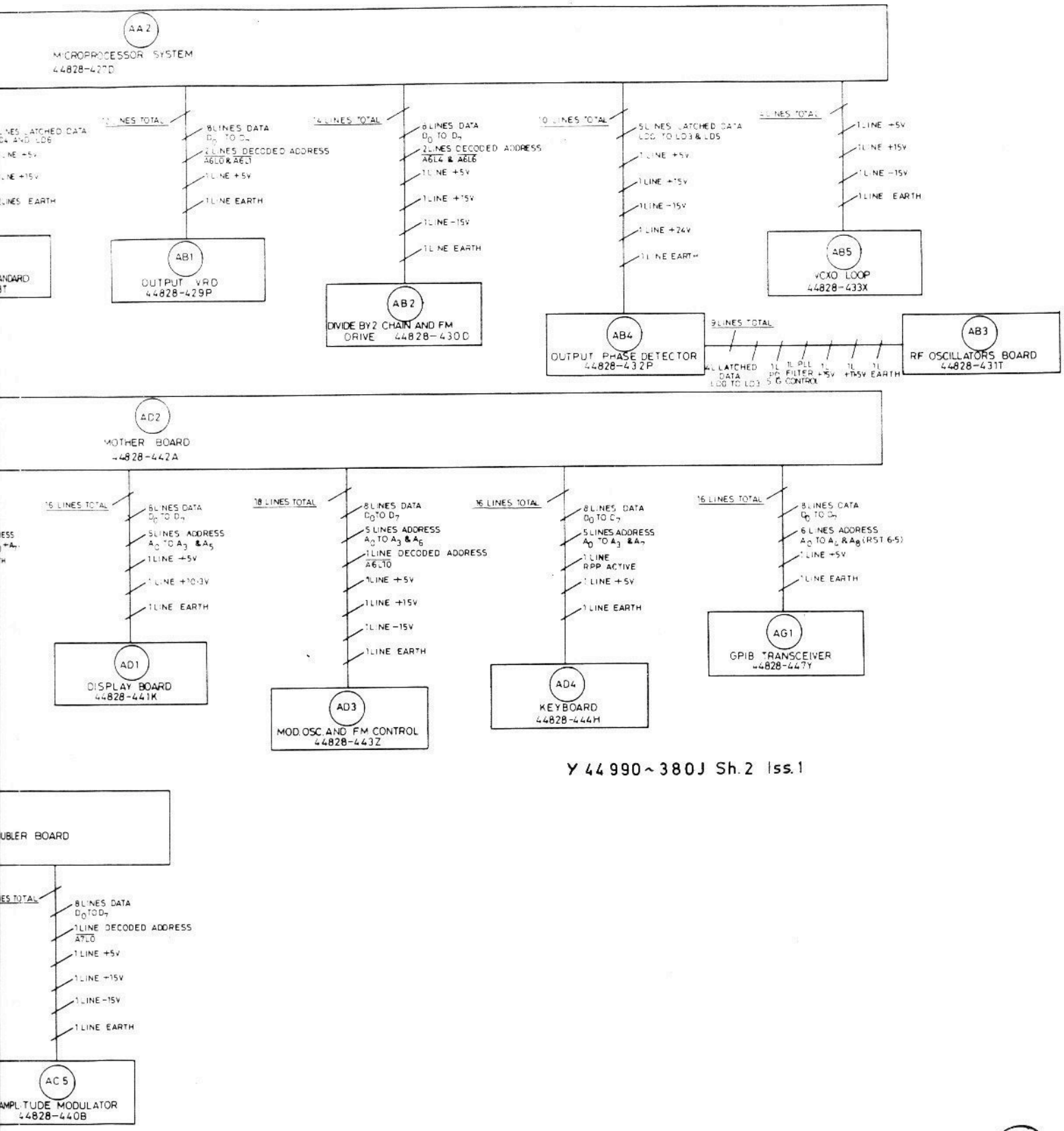
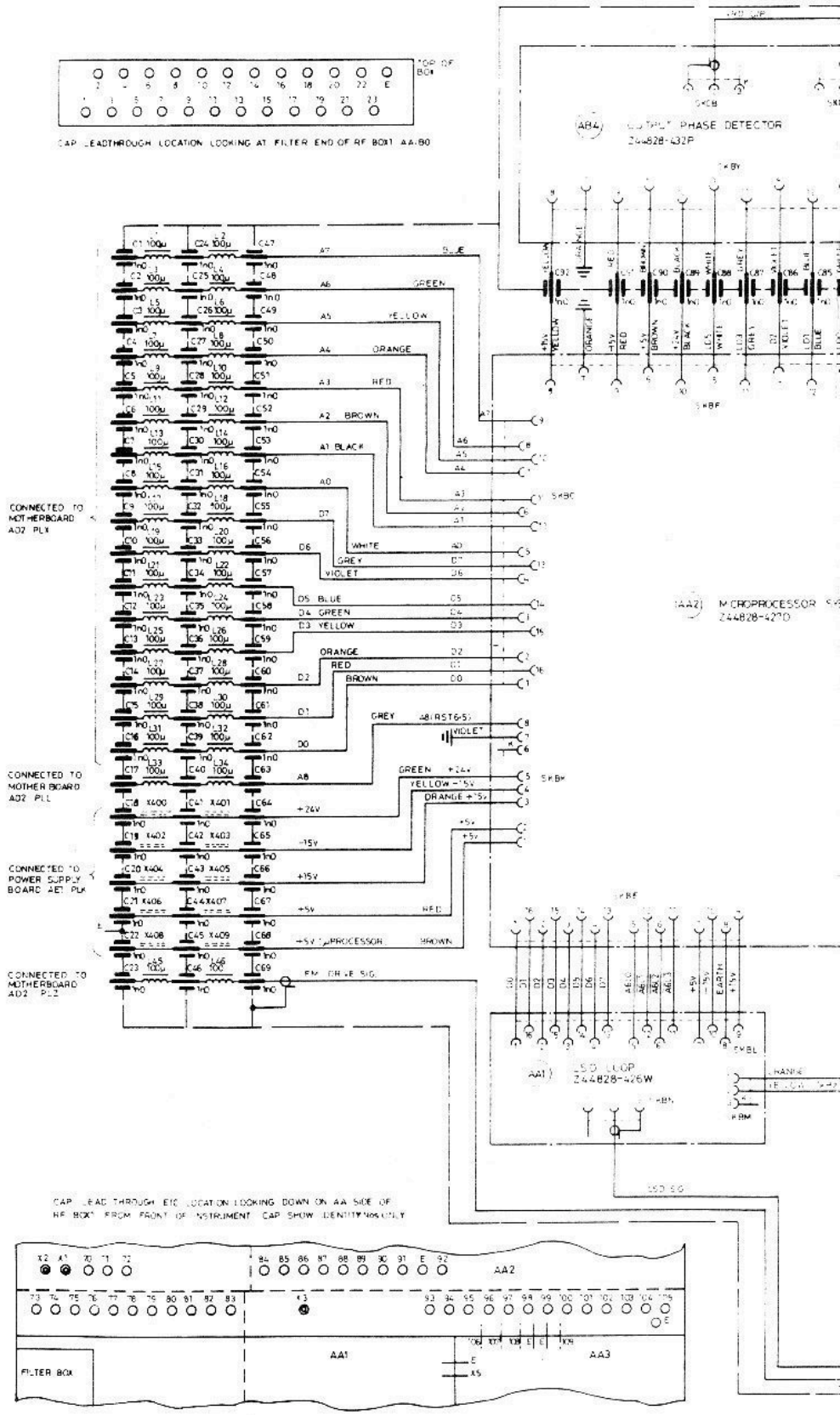


Control and power supply lines, AM0



Y 44990~380J Sh.2 Iss.1

Control and power supply lines, AMO



RF box

Fig. 5

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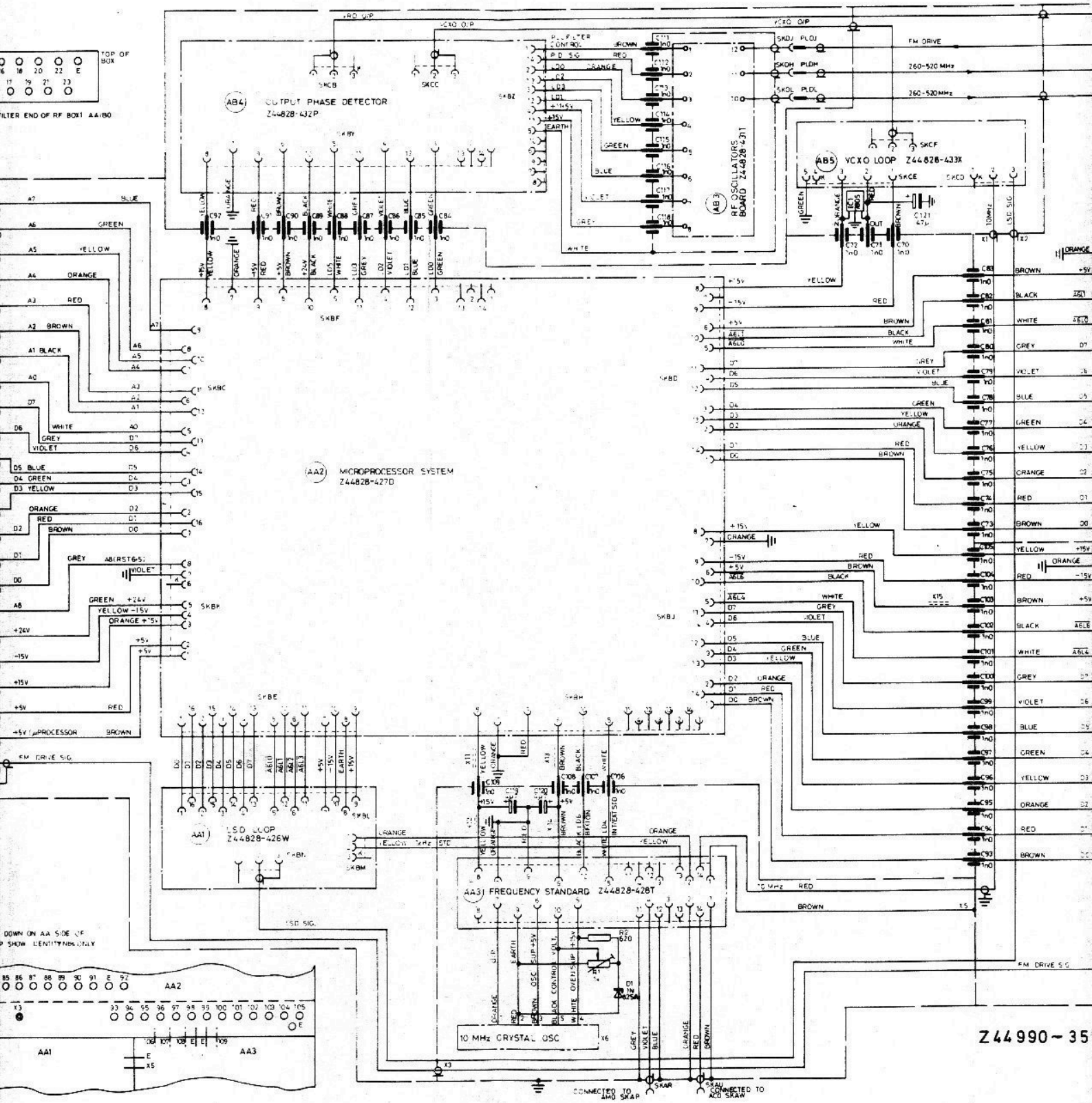
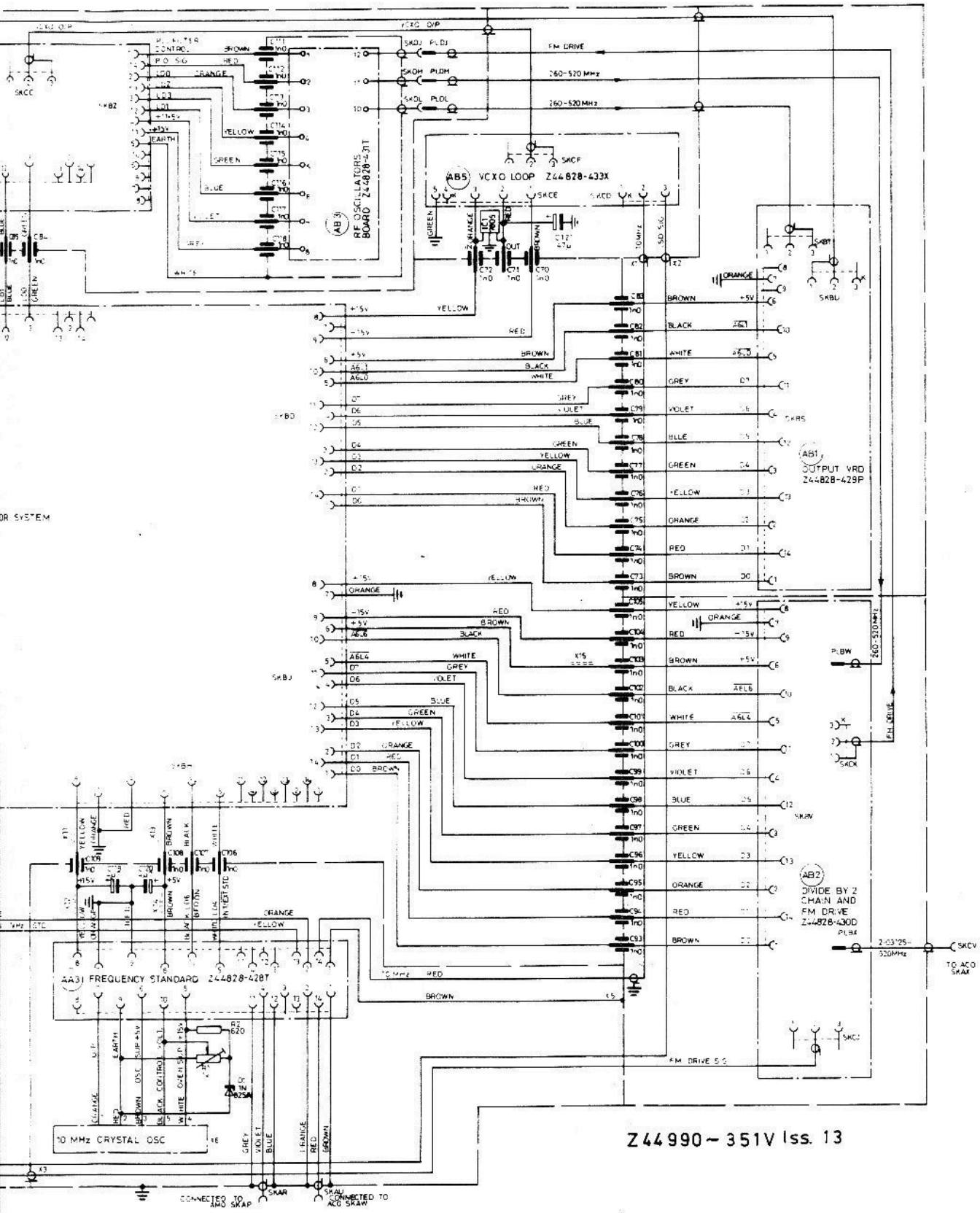
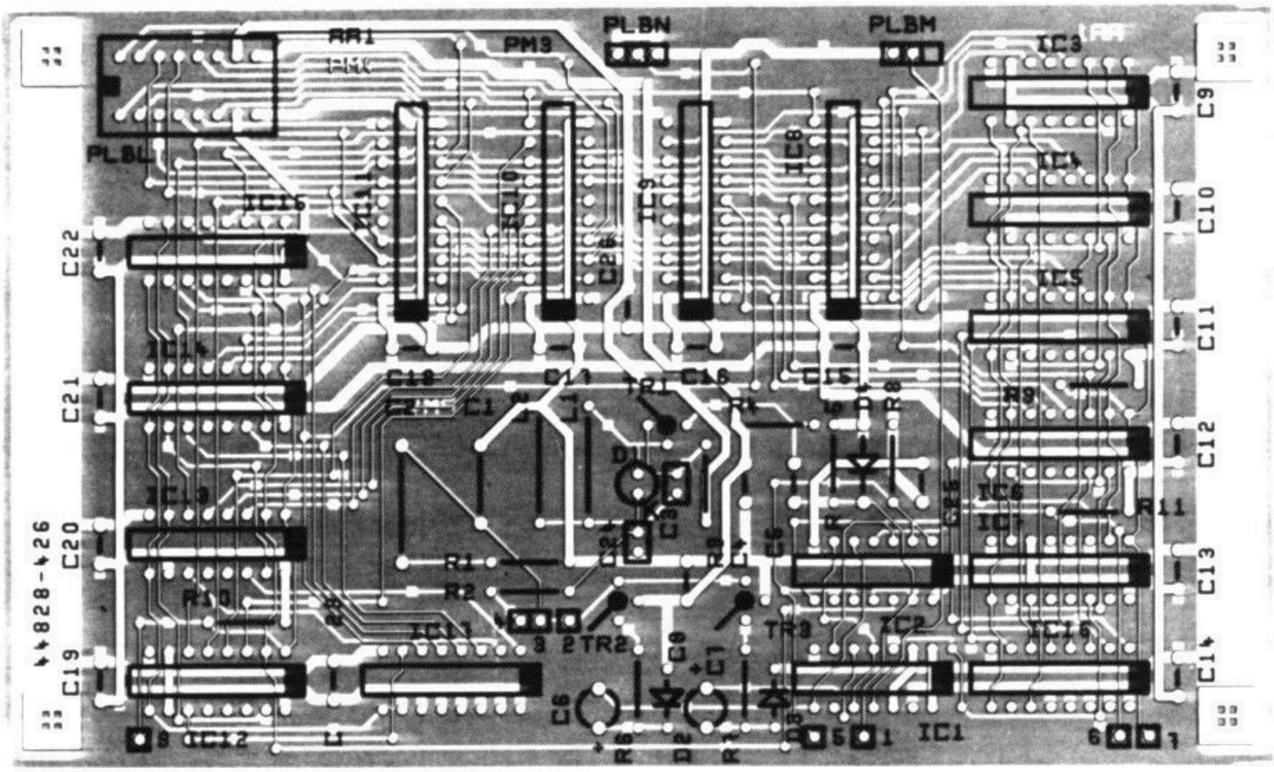


RF box 1 interconnections, AA/B0



box 1 interconnections, AA/BO

AA/BO



Component layout, AA1

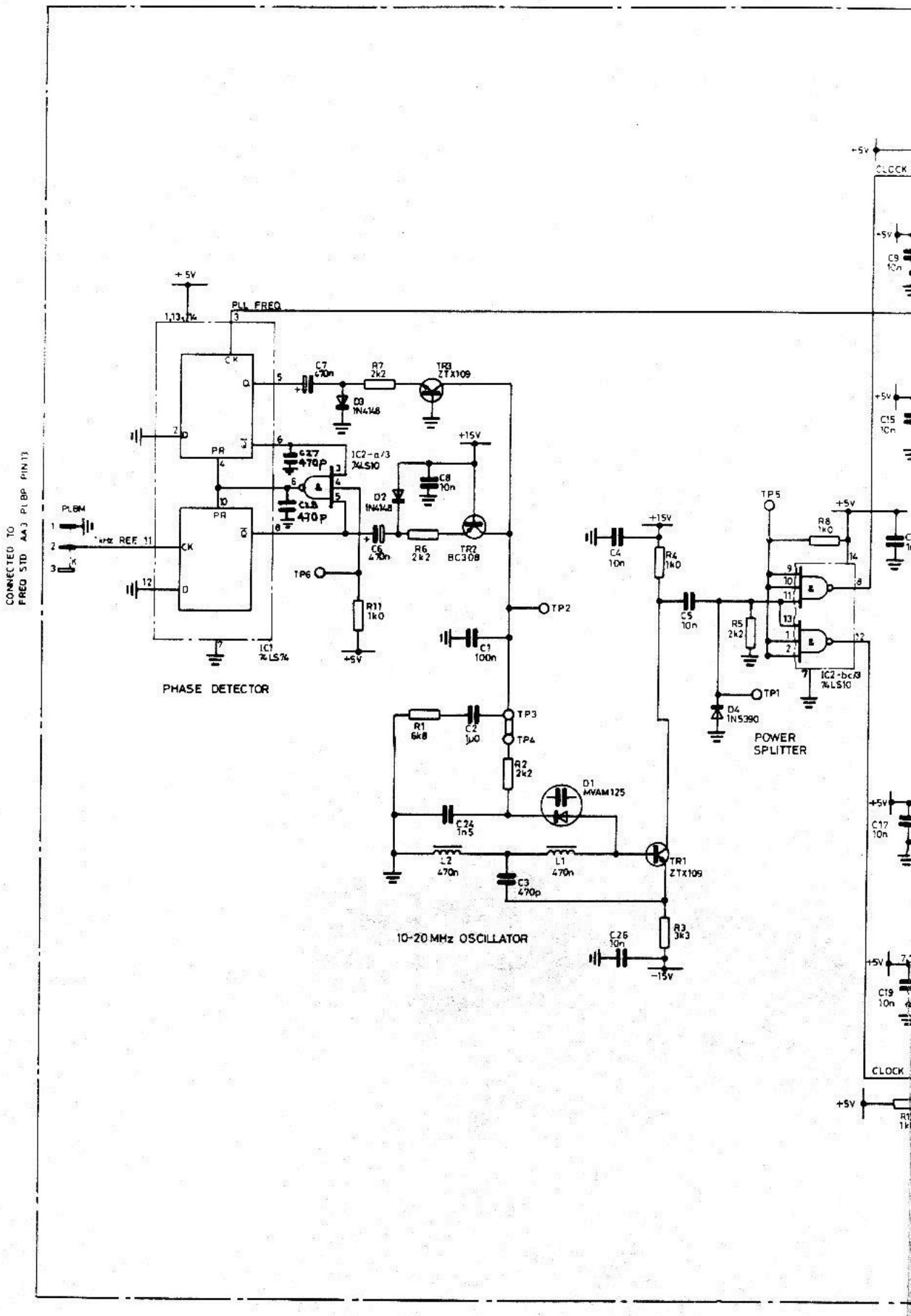

CONNECTED TO FREQ STD AA3 PLBP PIN 13
PLBM
1kHz REF 11
K
+5V
1,13,14
PLL FREQ
3
CK
Q
D
PR
5
6
2
4
10
12
7
C7 470n
R7 2k2
TR3 ZTX109
D3 1N4148
C27 470P
C28 470P
IC2-a/3 74LS10
C8 10n
D2 1N4148
+15V
C6 470n
R6 2k2
TR2 BC308
TP6
R11 1k0
IC1 74LS74
PHASE DETECTOR
TP2
C1 100n
R1 6k8
C2 1µ0
TP3
TP4
R2 2k2
D1 MVAM125
C24 1n5
L2 470n
L1 470n
C3 470p
TR1 ZTX109
10-20 MHz OSCILLATOR
C26 10n
R3 3k3
-15V
TP5
C4 10n
R4 1k0
C5 10n
R5 2k2
R8 1k0
IC2-b/3 74LS10
TP1
D4 1N5390
POWER SPLITTER
CLOCK
C15 10n
C17 10n
C19 10n

Fig. 6

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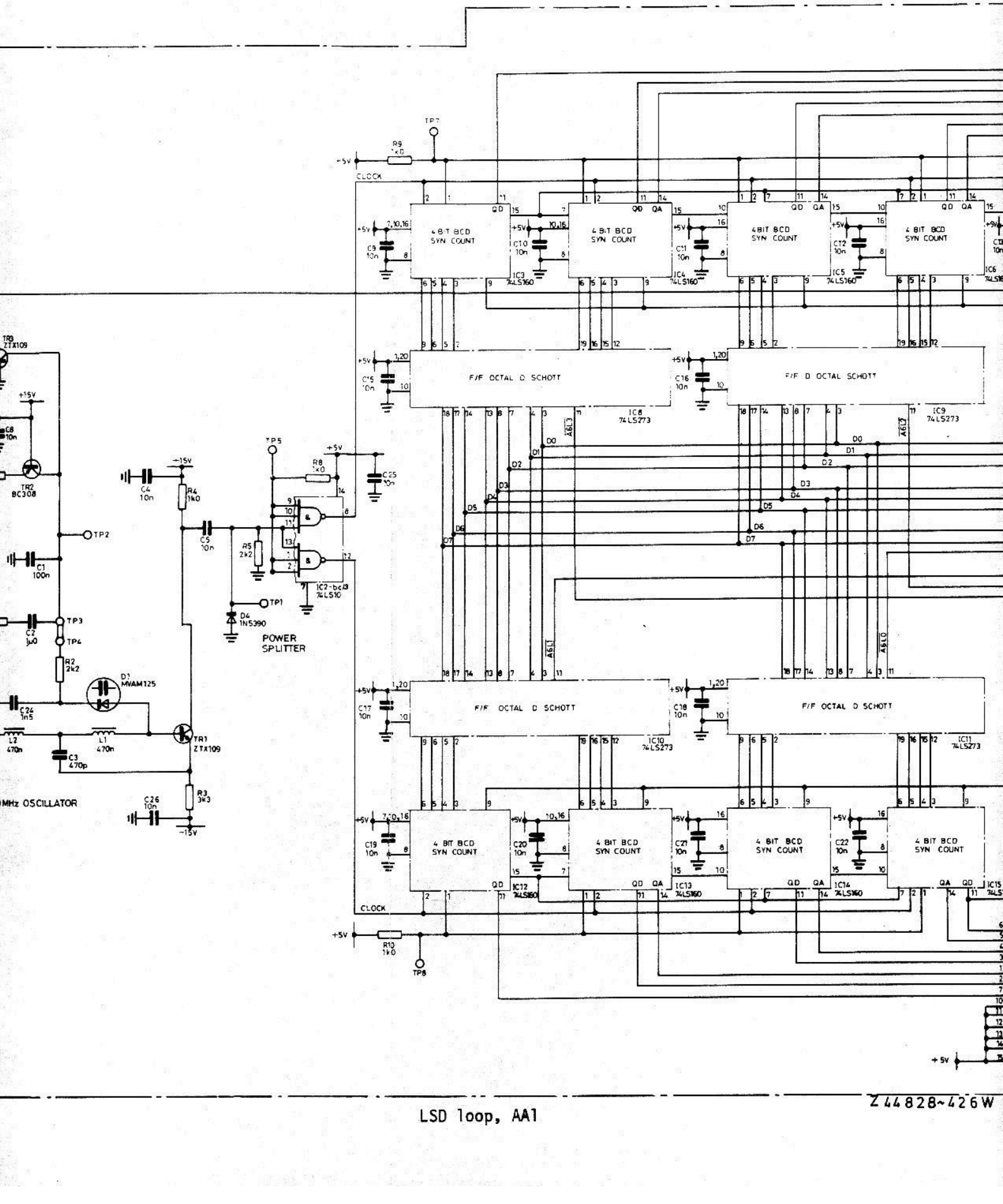
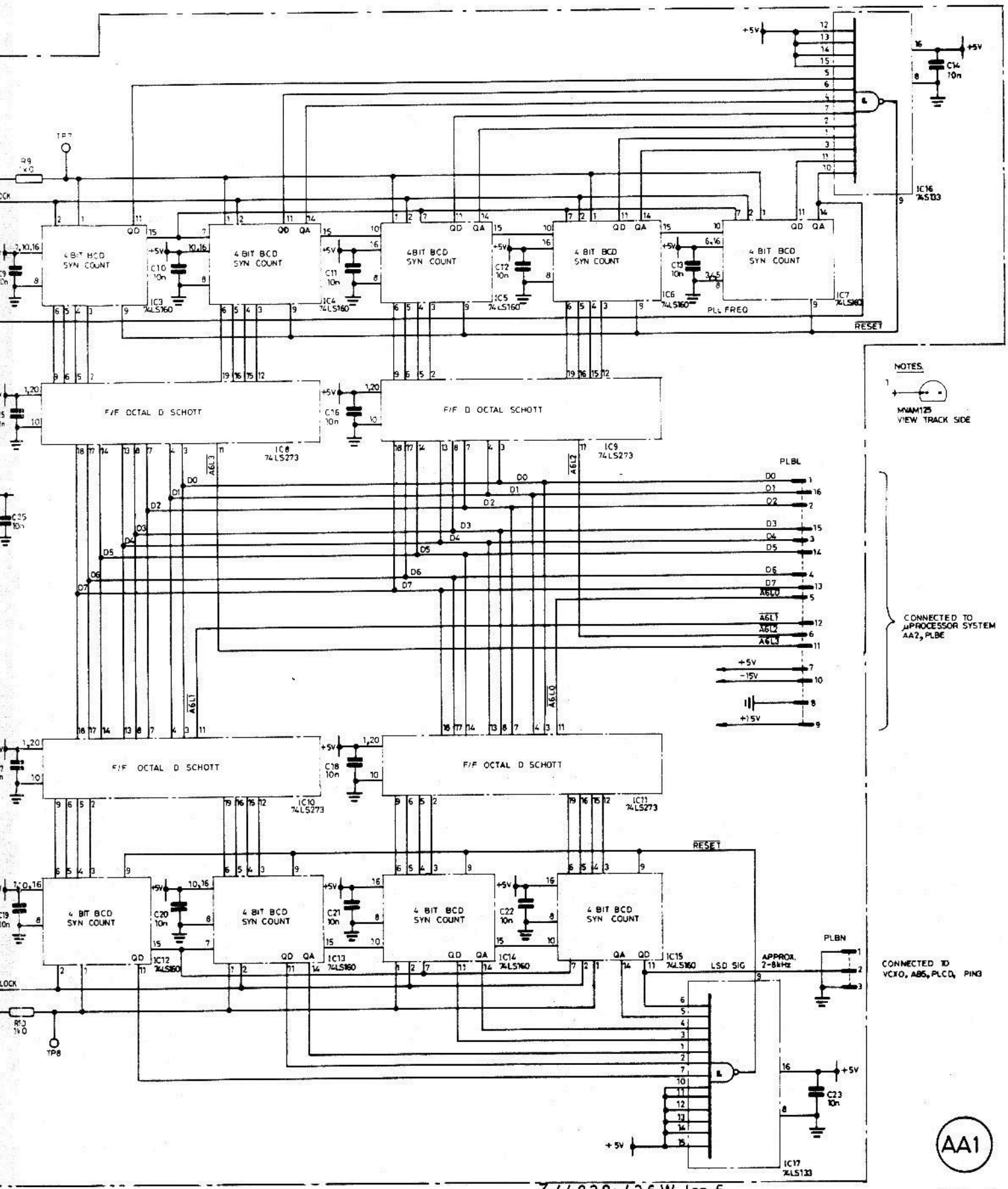


Z44828~426W

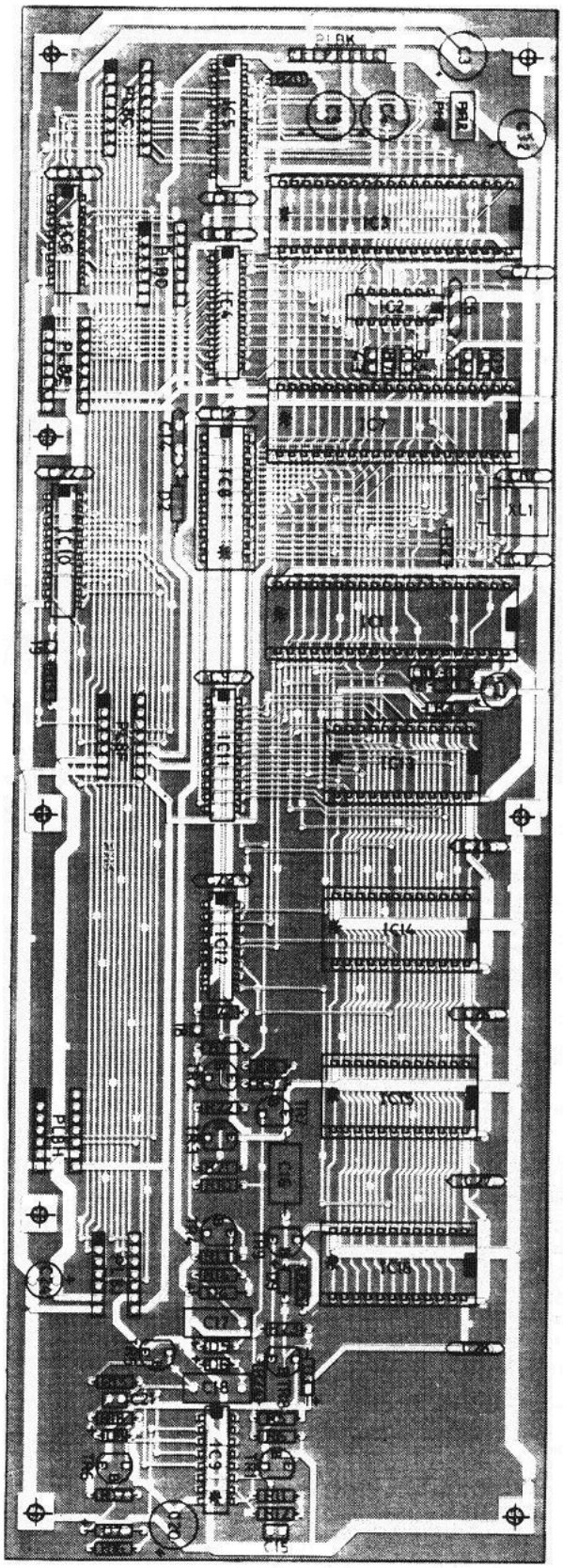
LSD loop, AA1



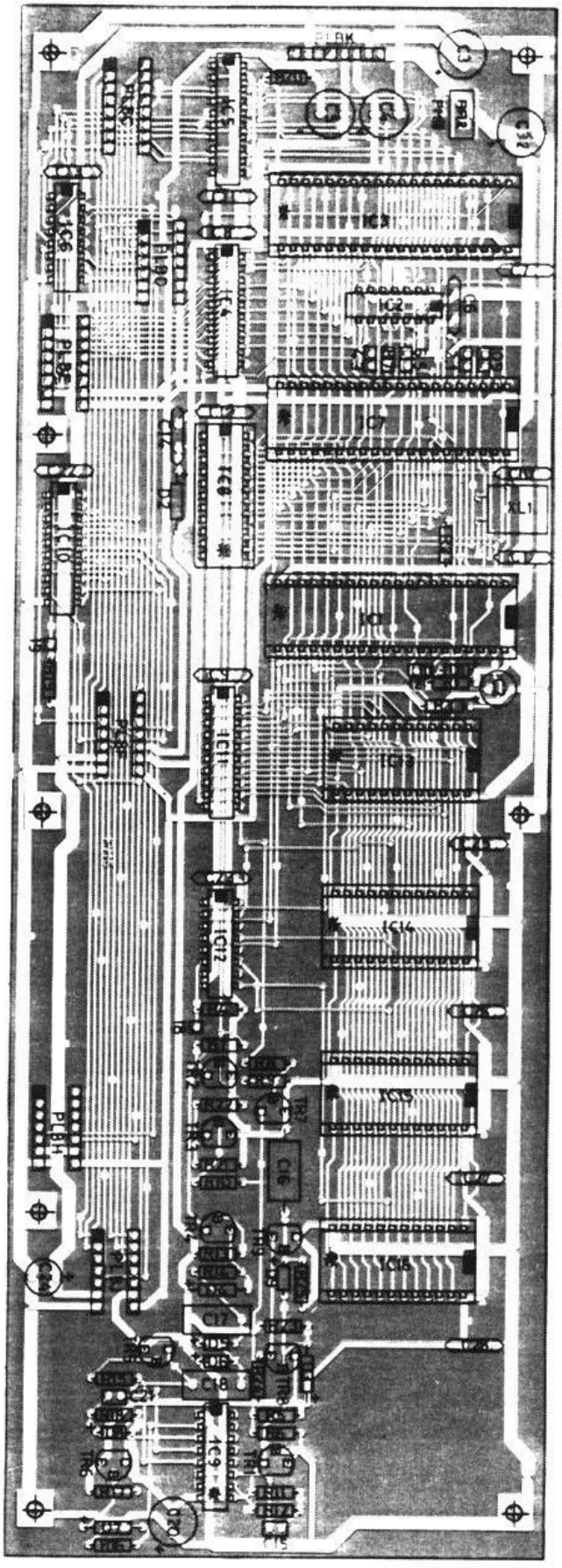
Z 44828-426W Iss. 6

LSD loop, AA1

AA1



Component layout, AA2



Component layout, AA2

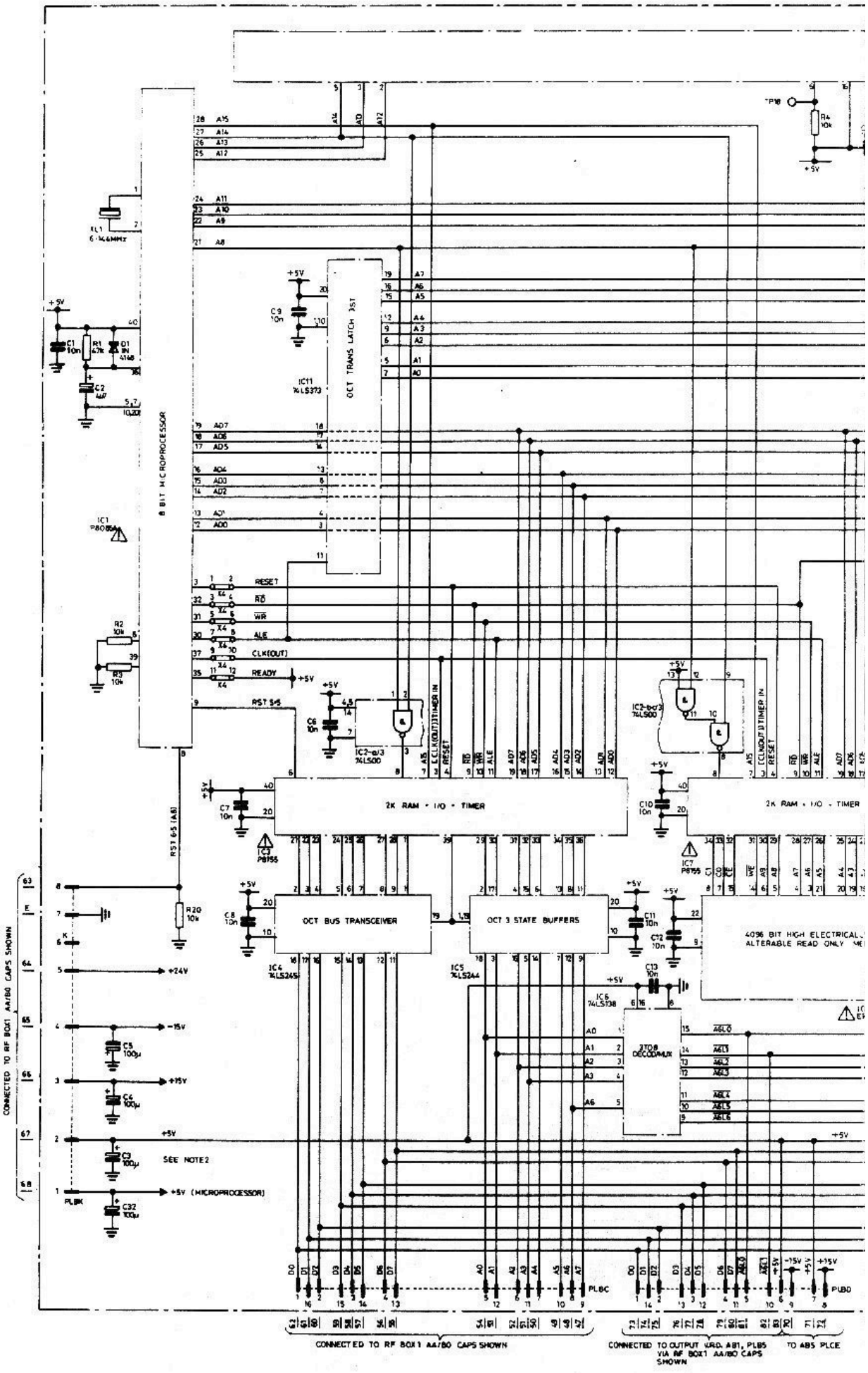

8 BIT MICROPROCESSOR
OCT TRANS LATCH 3ST
IC11 74LS373
IC1 P8085A
RESET
RD
WR
ALE
CLK(OUT)
READY
RST 5·5
RST 6·5 (A8)
2K RAM + I/O + TIMER
IC3 P8155
IC7 P8155
OCT BUS TRANSCEIVER
IC4 74LS245
OCT 3 STATE BUFFERS
IC5 74LS244
IC6 74LS138
3TO8 DECODE/MUX
4096 BIT HIGH ELECTRICAL
ALTERABLE READ ONLY
CONNECTED TO RF BOX1 AA/BO CAPS SHOWN
+24V
-15V
+15V
+5V
SEE NOTE2
+5V (MICROPROCESSOR)
PLBK
PLBC
PLBD
CONNECTED TO RF BOX1 AA/BO CAPS SHOWN
CONNECTED TO OUTPUT VERO. A81, PLB5 VIA RF BOX1 AA/BO CAPS SHOWN
TO AB5 PLCE

Fig. 7

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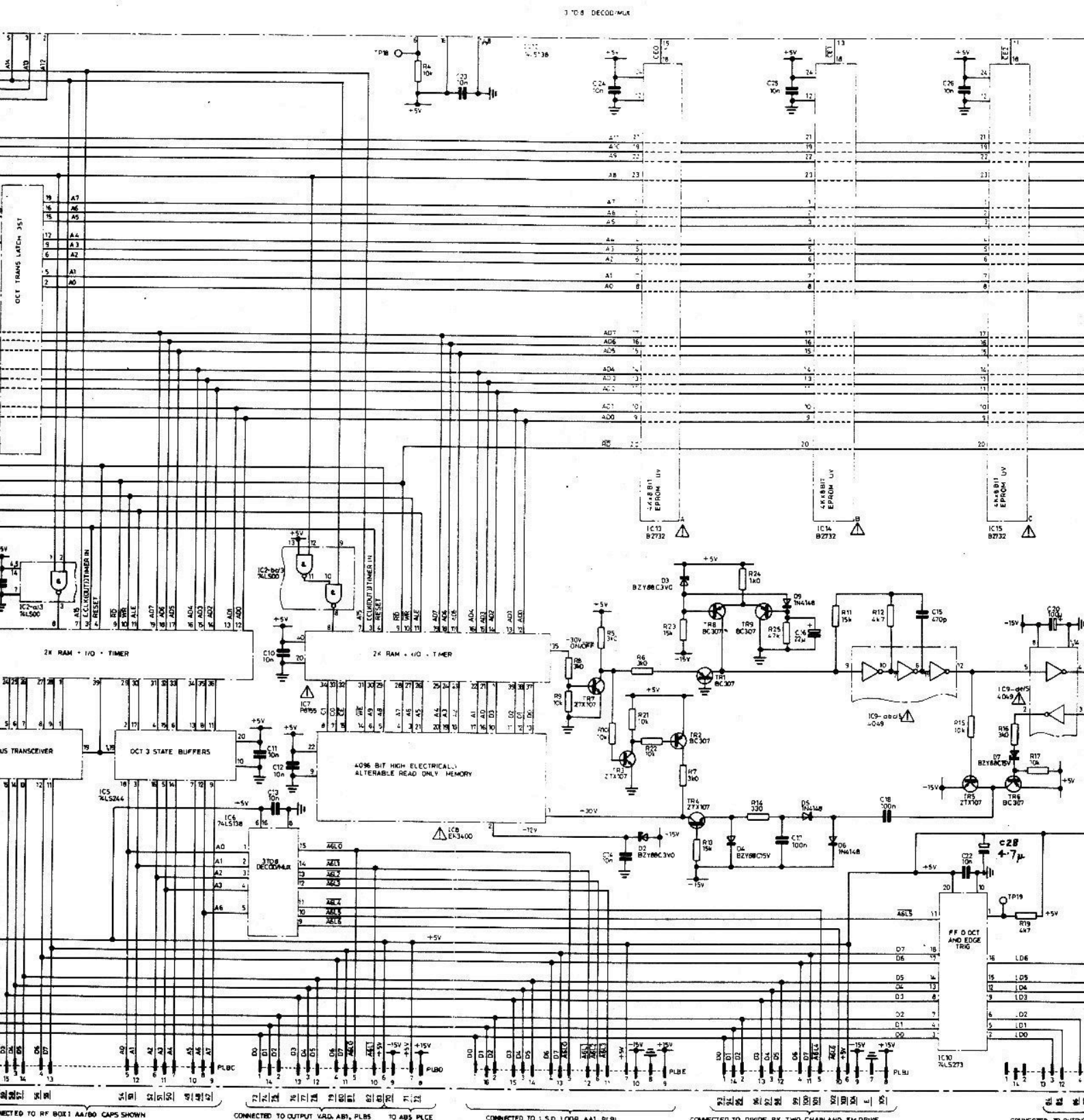
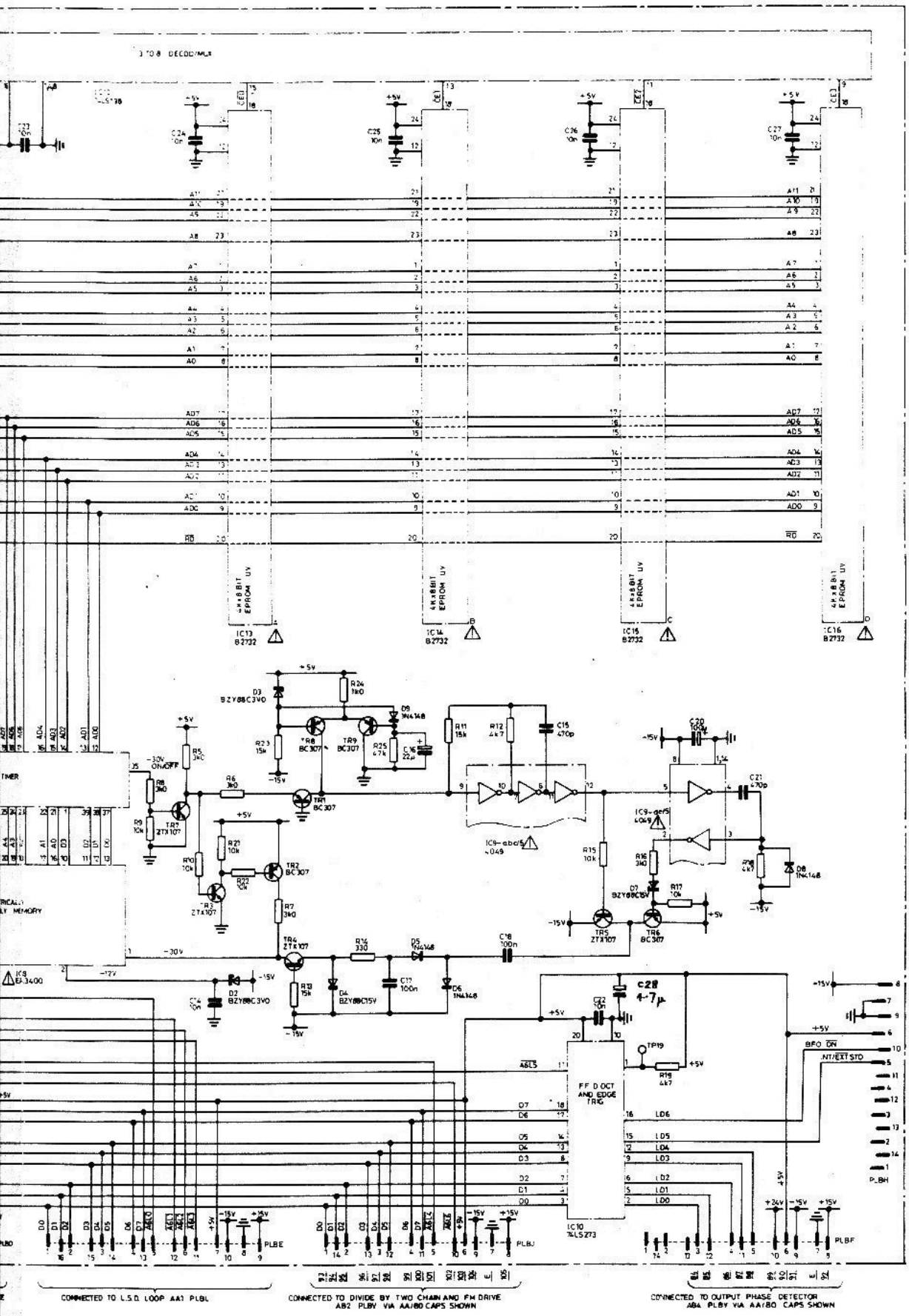


Microprocessor system, AA2

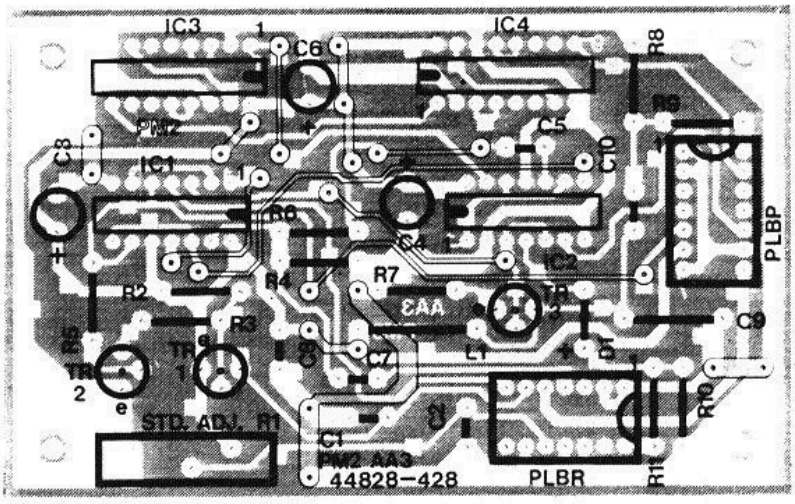
Z44828-427D



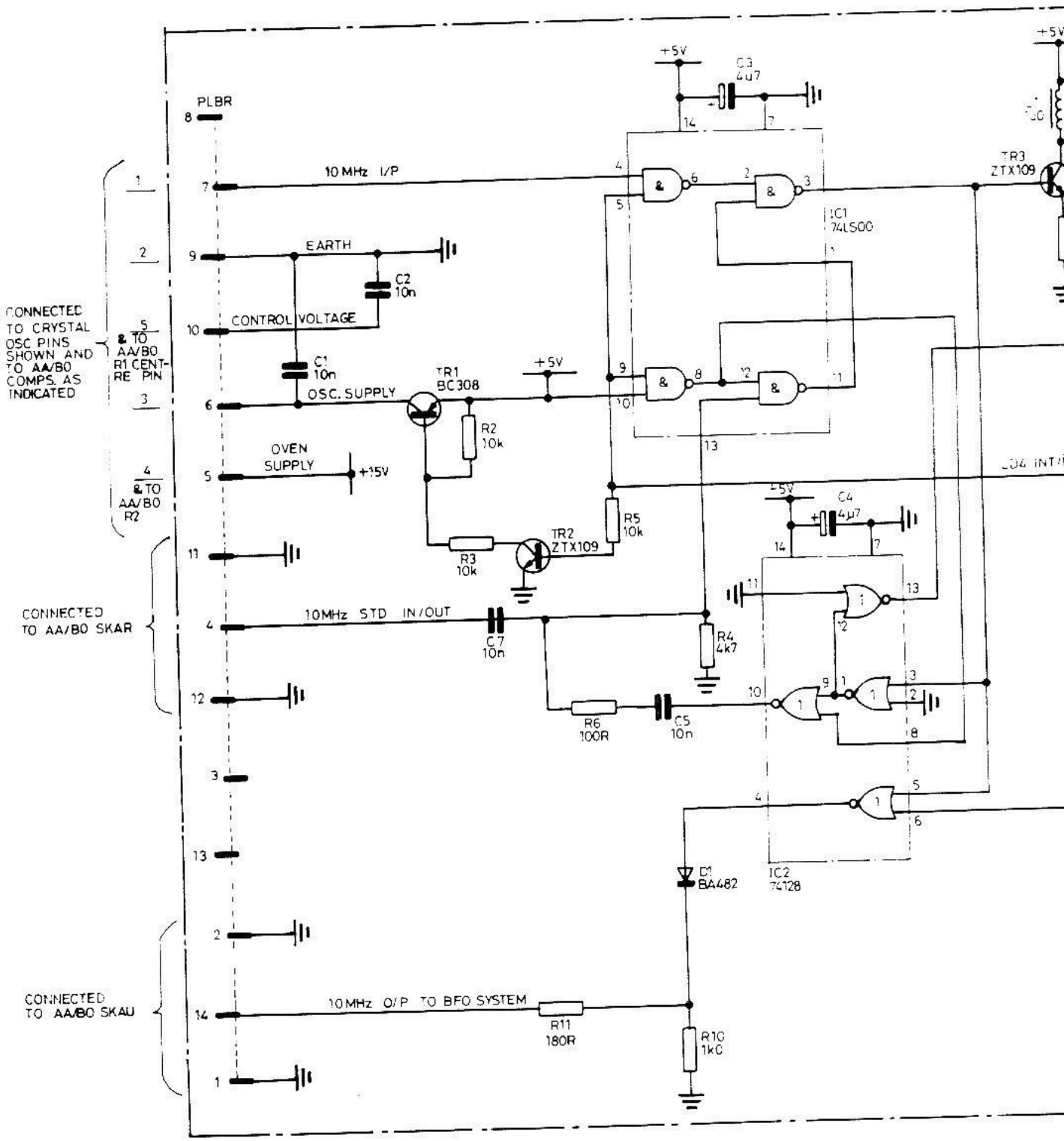
Microprocessor system, AA2

Z 44828-427D Iss.11

AA2



Component layout, AA3



Frequency stand

Fig. 8

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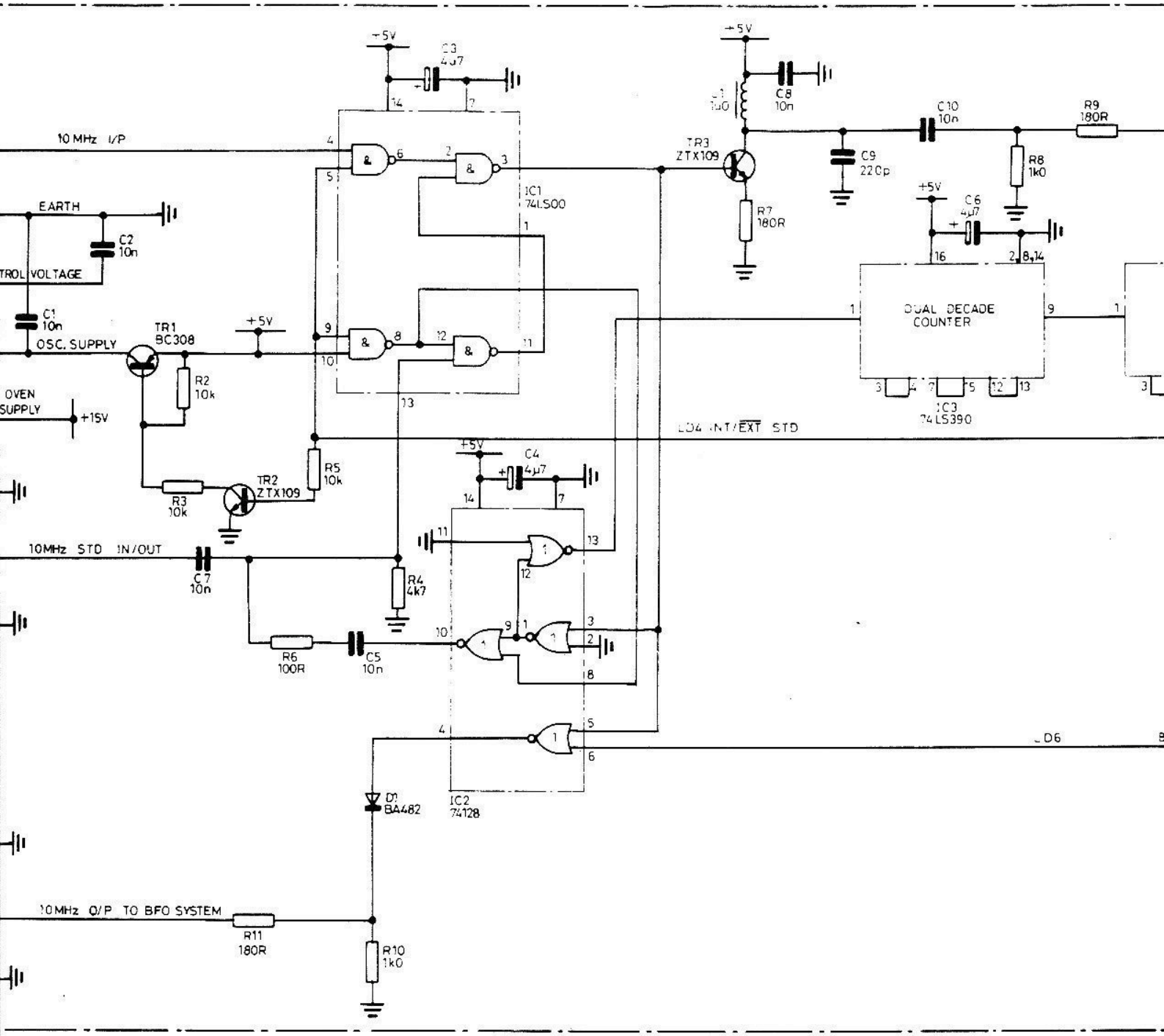
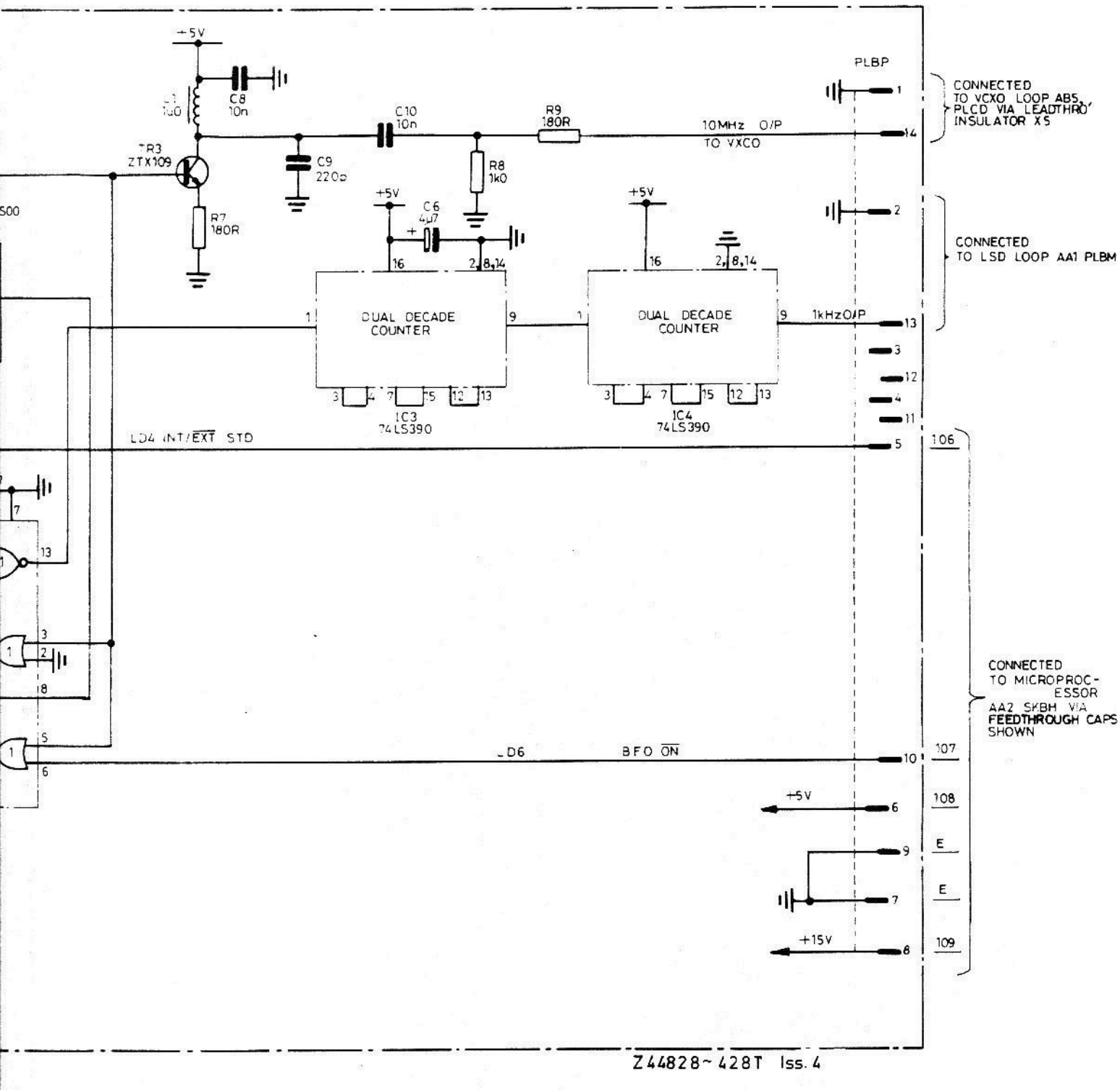


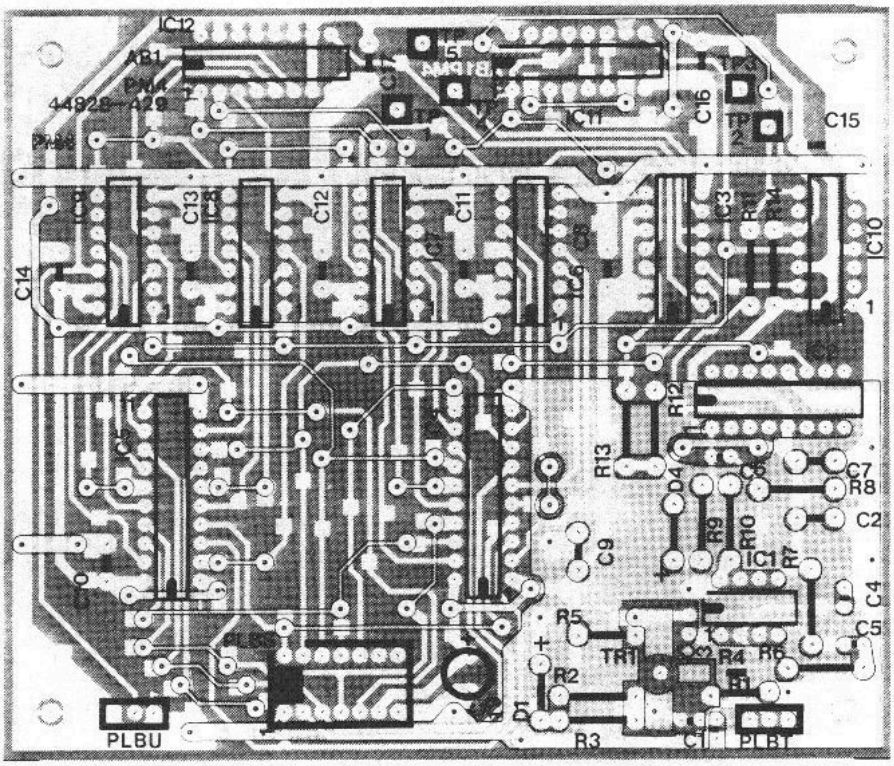
Frequency standard, AA3



Z44828~428T Iss.4

Frequency standard, AA3

AA3



Component layout, AB1

Fig. 9a
Chap. 7
Page 18

Fig. 9a

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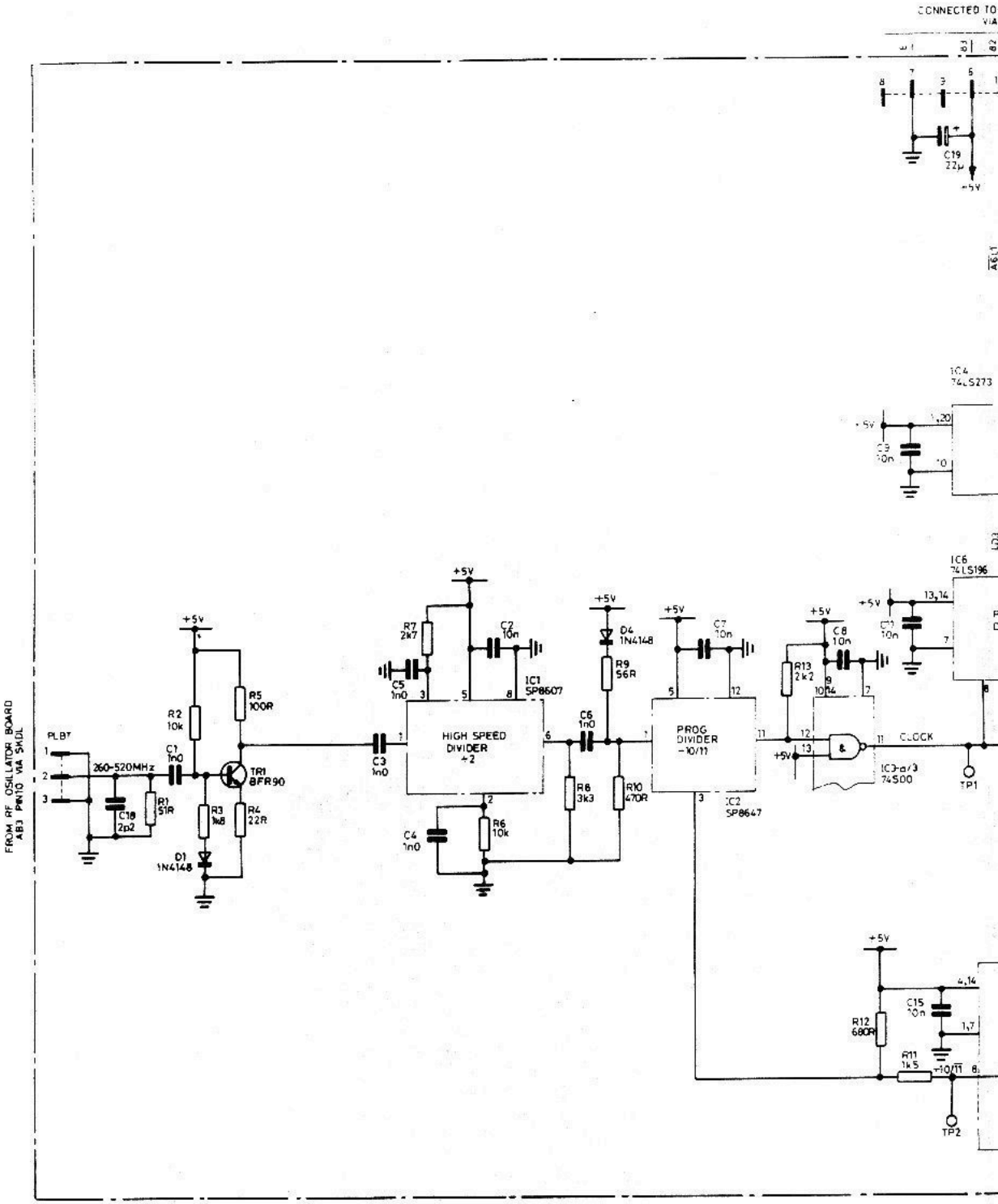
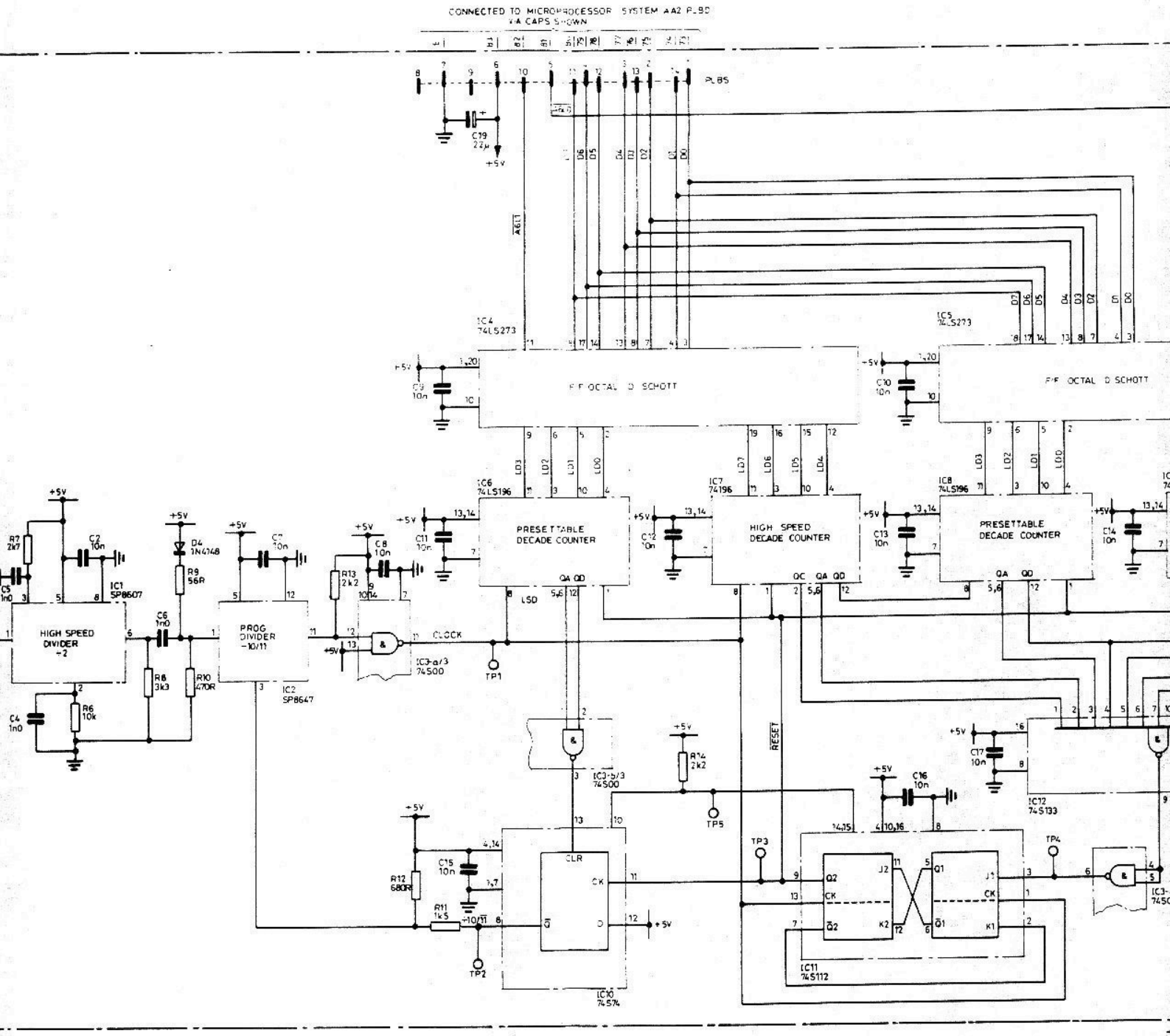
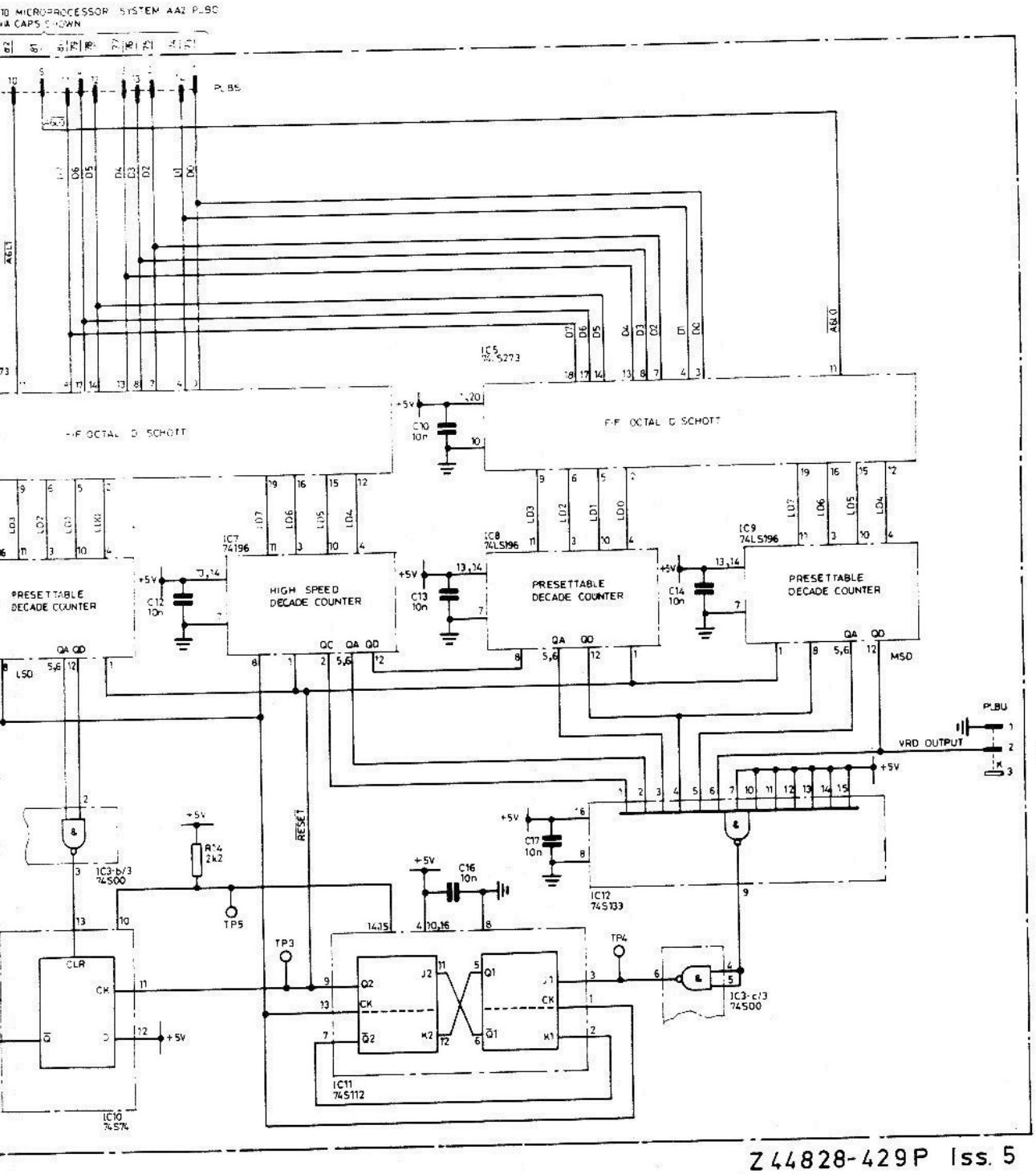

FROM RF OSILLATOR BOARD
ABJ PIN10 VIA SKDL
PLB1
260-520MHz
C18 2p2
R1 51R
C1 1n0
R2 10k
R5 100R
TR1 BFR90
R3 1k8
R4 22R
D1 1N4148
+5V
C3 1n0
R7 2k7
C2 10n
C5 1n0
IC1 SP8607
HIGH SPEED DIVIDER ÷2
C4 1n0
R6 10k
C6 1n0
R8 3k3
D4 1N4148
R9 56R
R10 470R
PROG DIVIDER ÷10/11
IC2 SP8647
C7 10n
R13 2k2
C8 10n
C11 10n
IC6 74LS196
IC3-a/3 74S00
CLOCK
TP1
C19 22µ
IC4 74LS273
C9 10n
R12 680R
C15 10n
R11 1k5
TP2

Fig. 9

Sep. 81



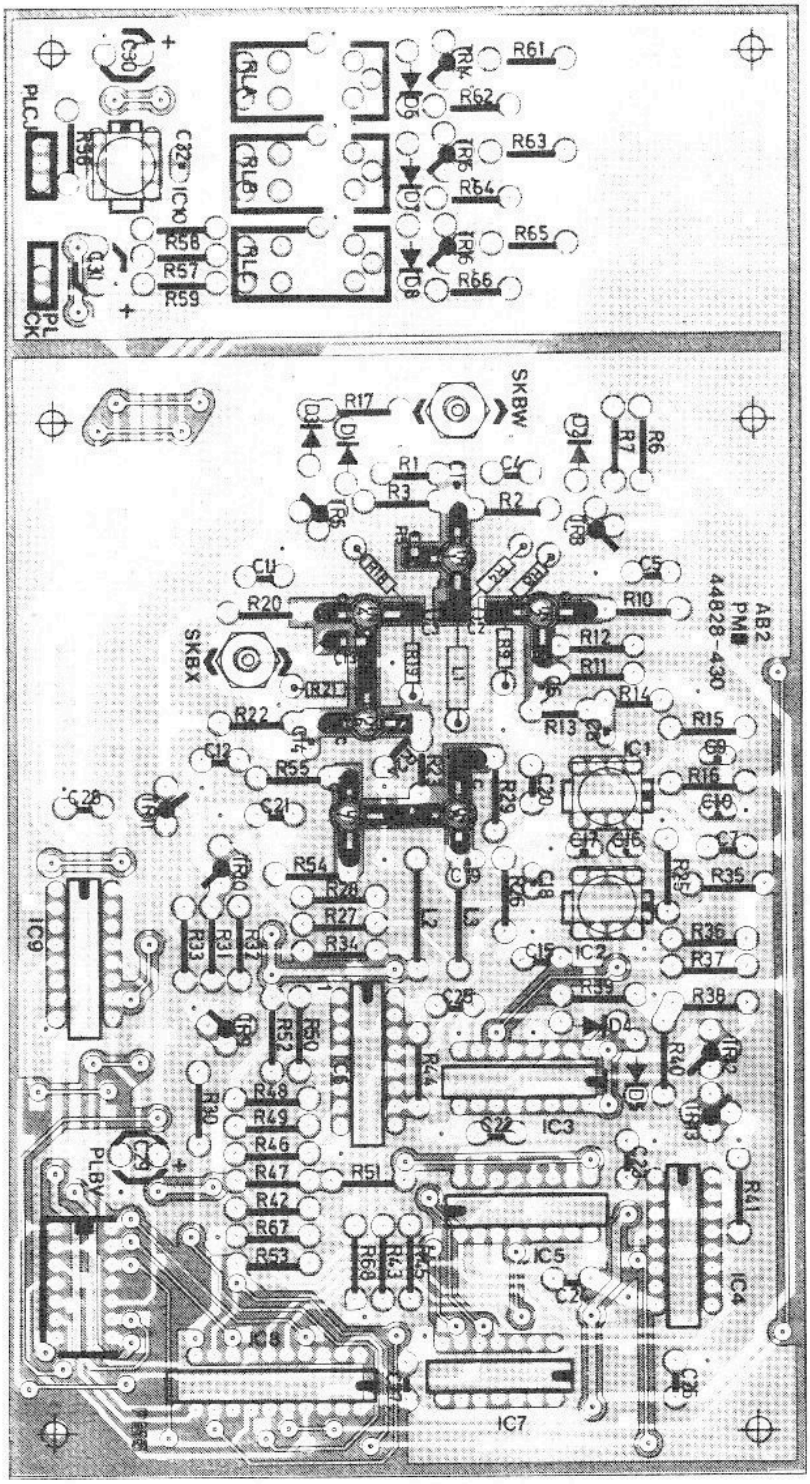
Output v.r.d., AB1



Z44828-429P Iss. 5

AB1

Output v.r.d., AB1



Component layout, AB2

Fig. 10a
Chap. 7
Page 20

Fig. 10a

Sep. 81

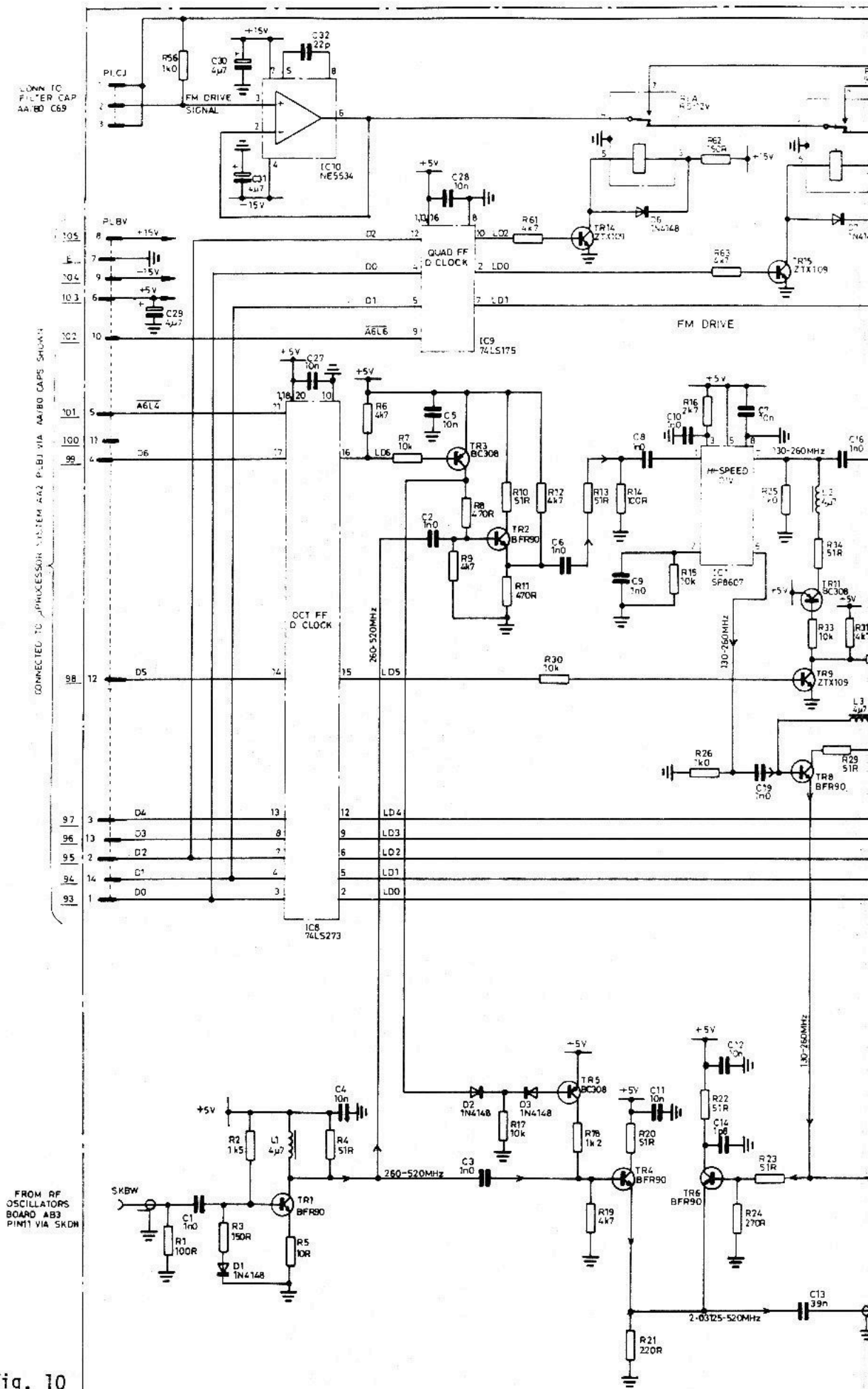
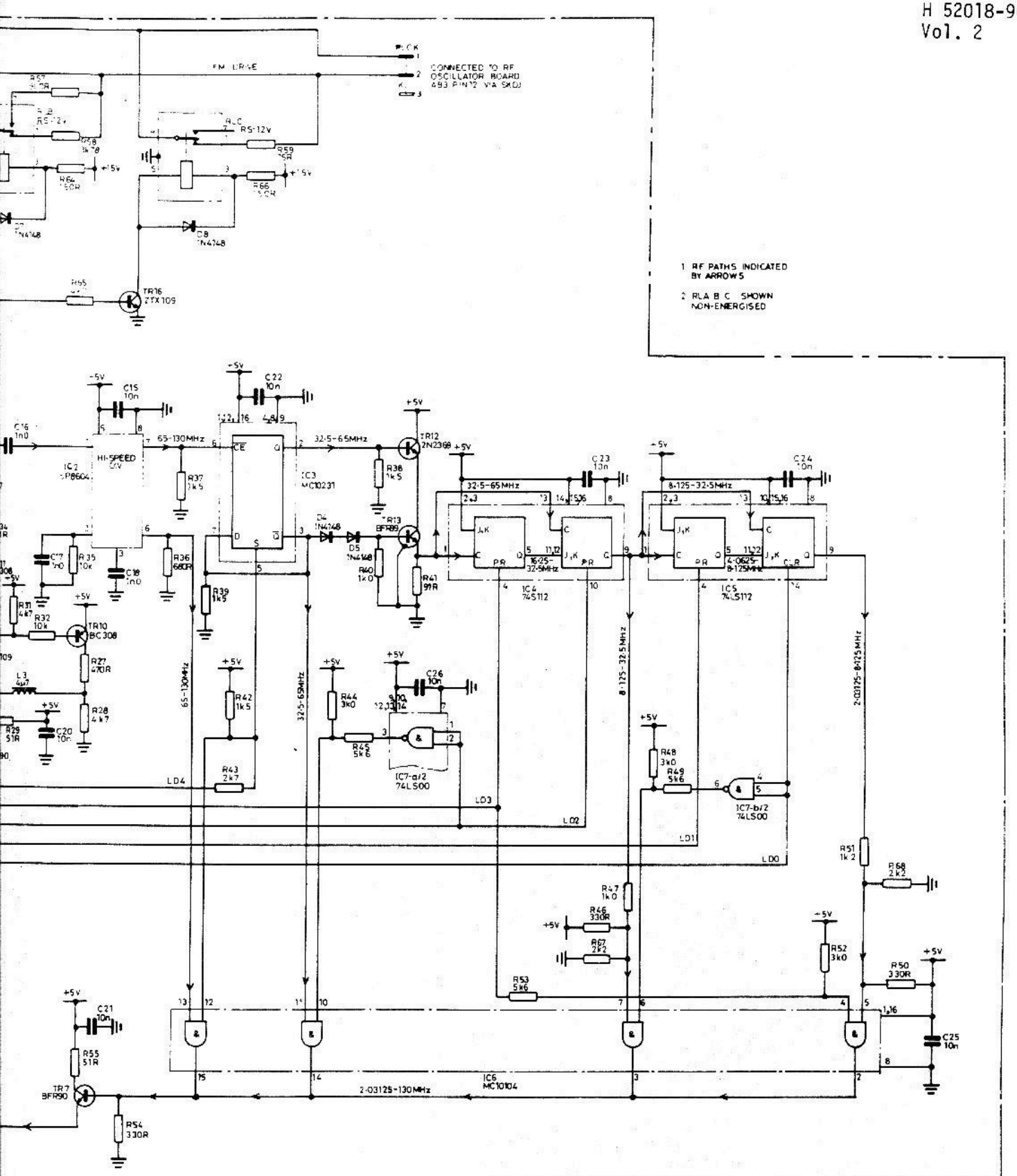

CONN TO FILTER CAP AA/BD C69
P1.CJ
FM DRIVE SIGNAL
IC10 NE5534
P1.BV
QUAD FF D CLOCK
IC9 74LS175
FM DRIVE
OCT FF D CLOCK
IC8 74LS273
CONNECTED TO μPROCESSOR SYSTEM AA2 P1.BJ VIA AA/BD CAPS SHOWN
260-520MHz
130-260MHz
HI-SPEED
IC7 SP8607
FROM RF OSCILLATORS BOARD AB3 PIN11 VIA SKDN
SKBW
2-03125-520MHz

Fig. 10

Sep. 81

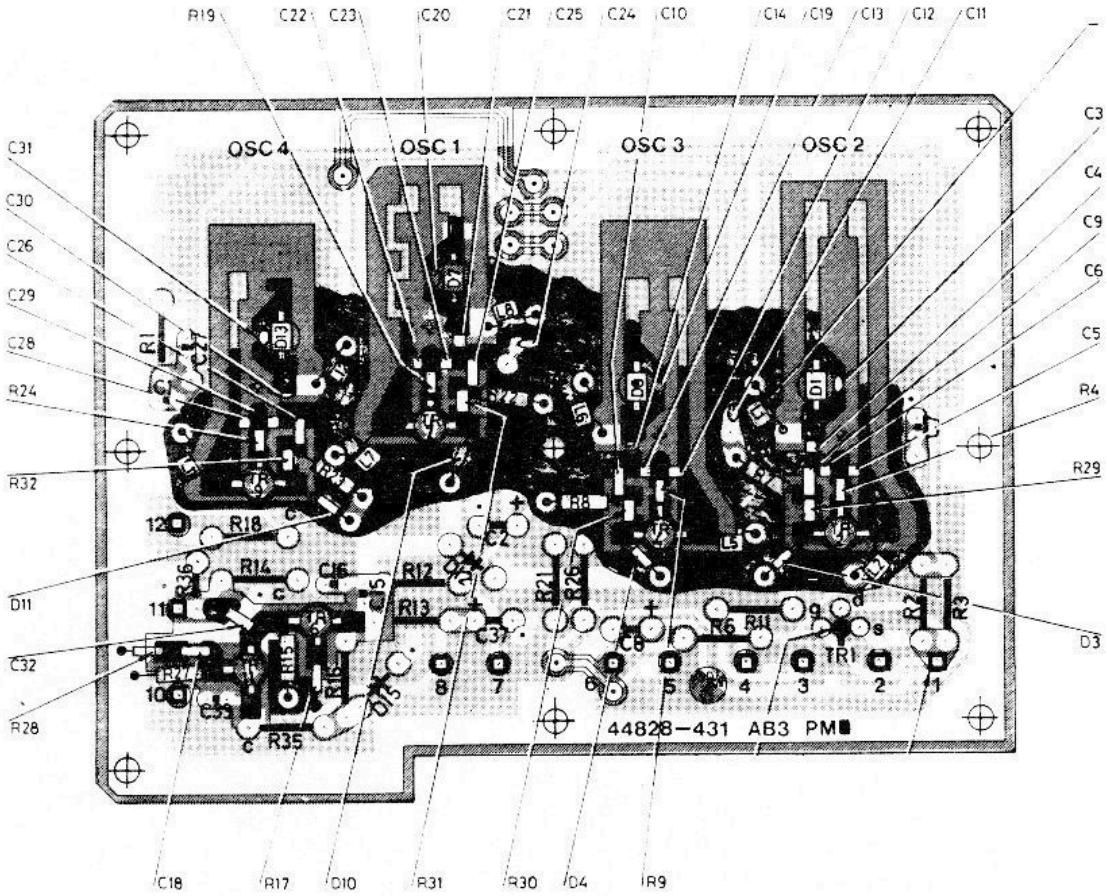


DIVIDE BY 2 CHAIN

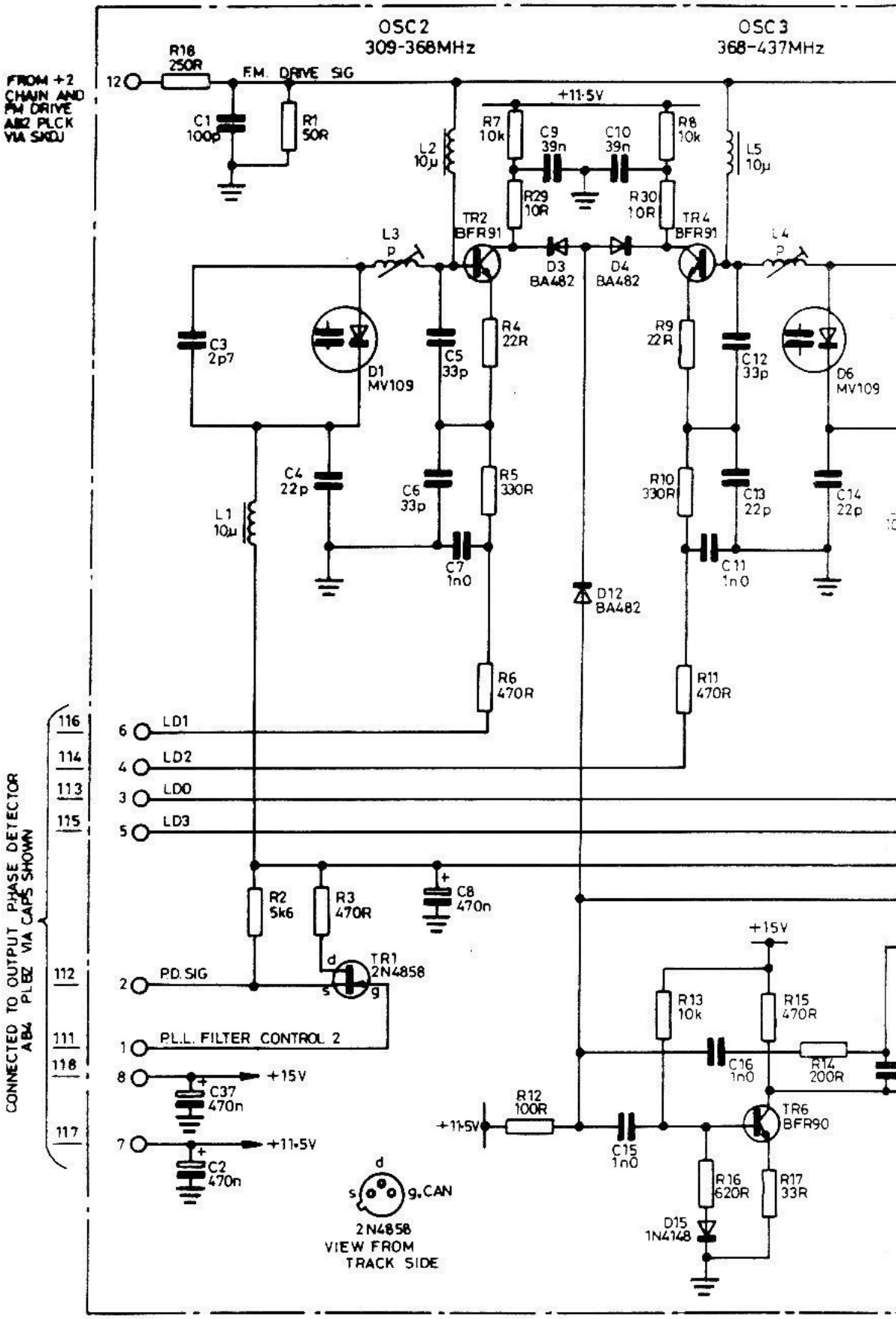
Z44828-430D Iss.7

Divide by 2 chain and f.m. drive, AB2

AB2



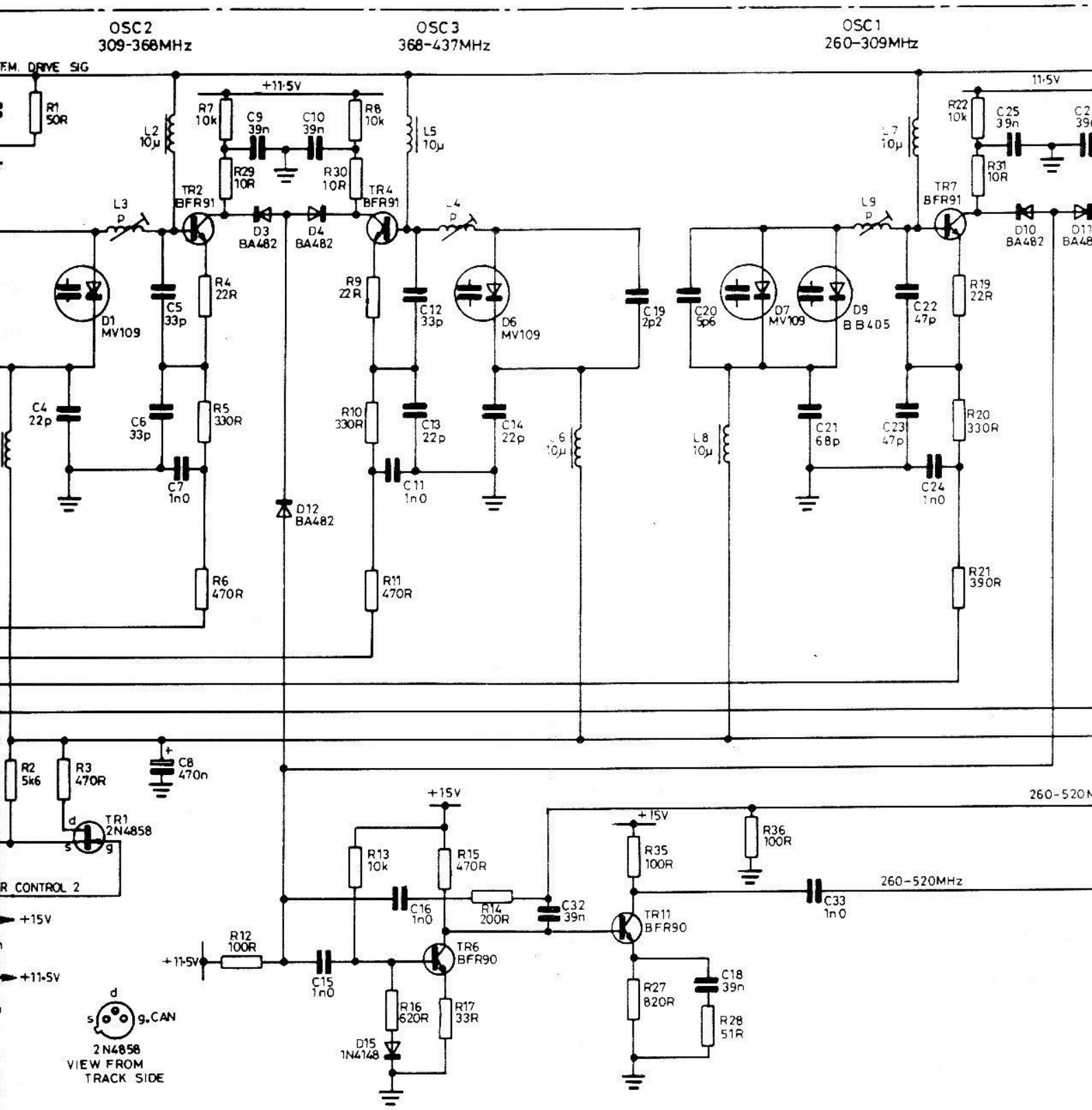
Component layout, AB3



RF

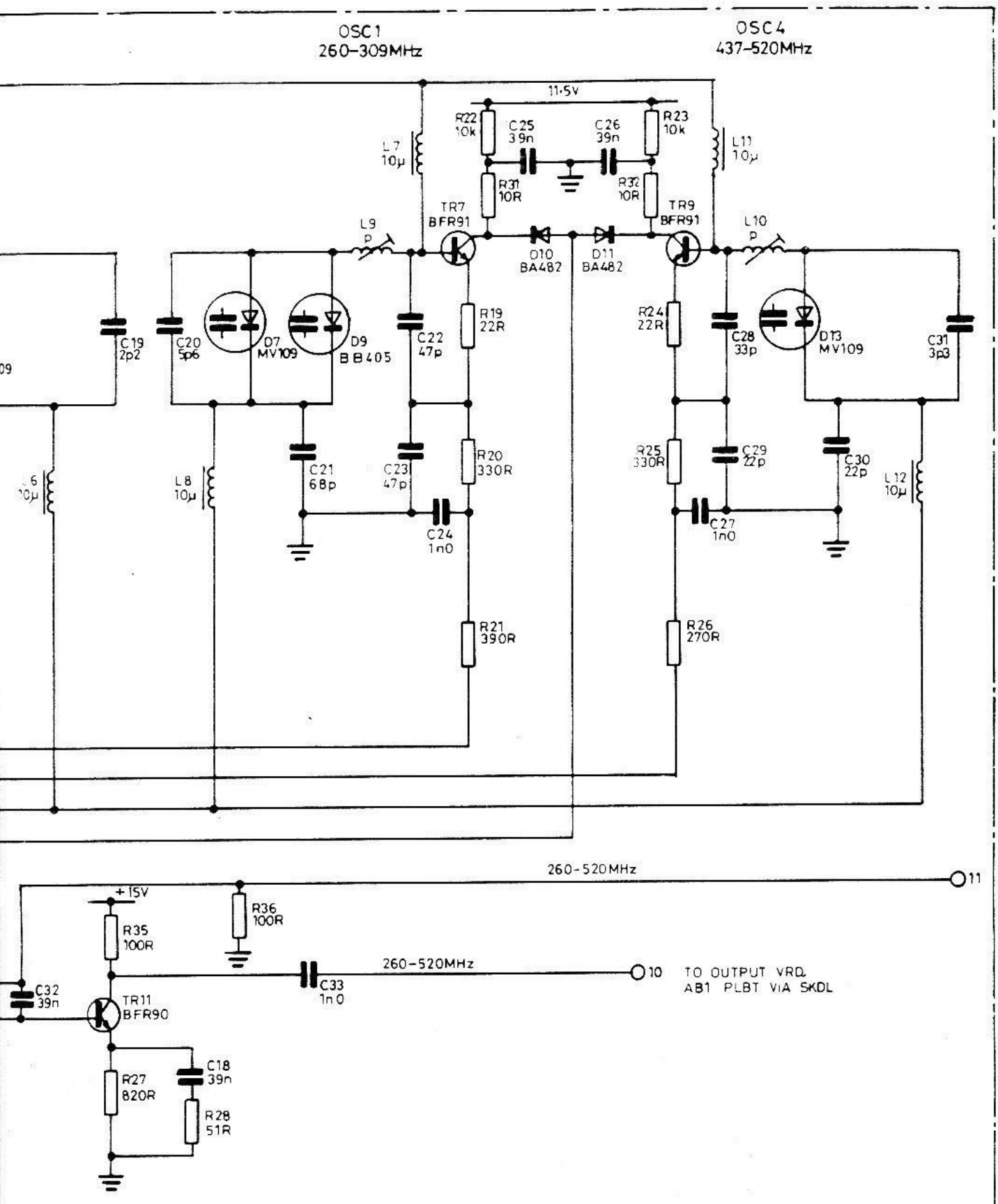
Fig. 11

Sep. 81



Z44828-4

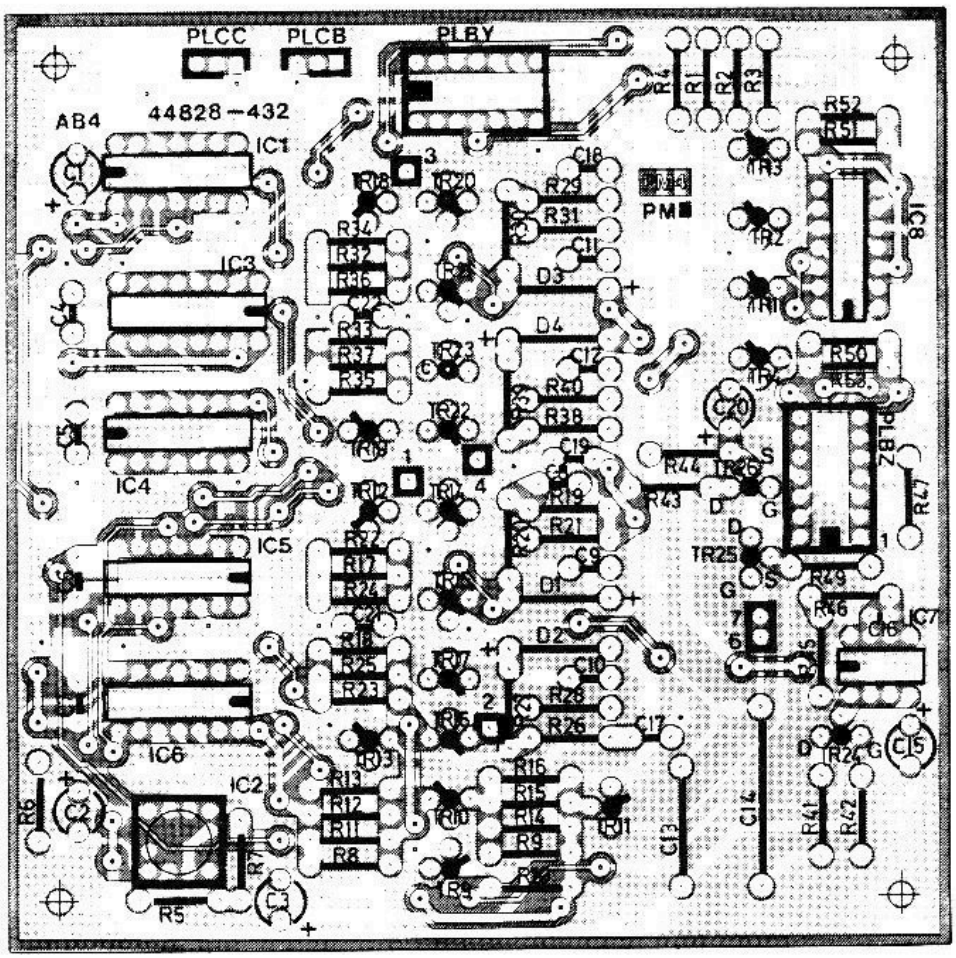
RF oscillators board, AB3



Z44828-431T Iss.12

AB3

RF oscillators board, AB3



Component layout, AB4

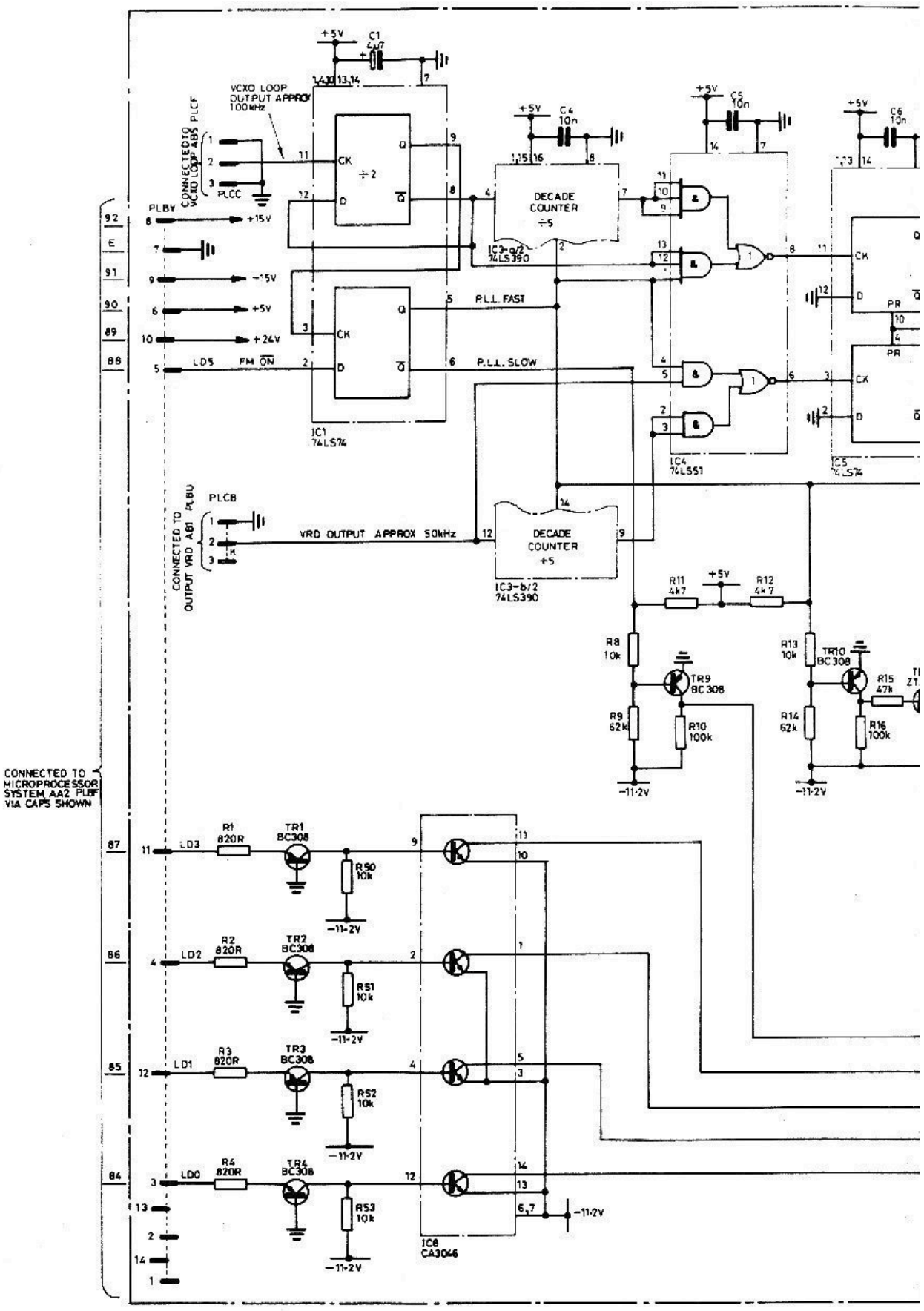
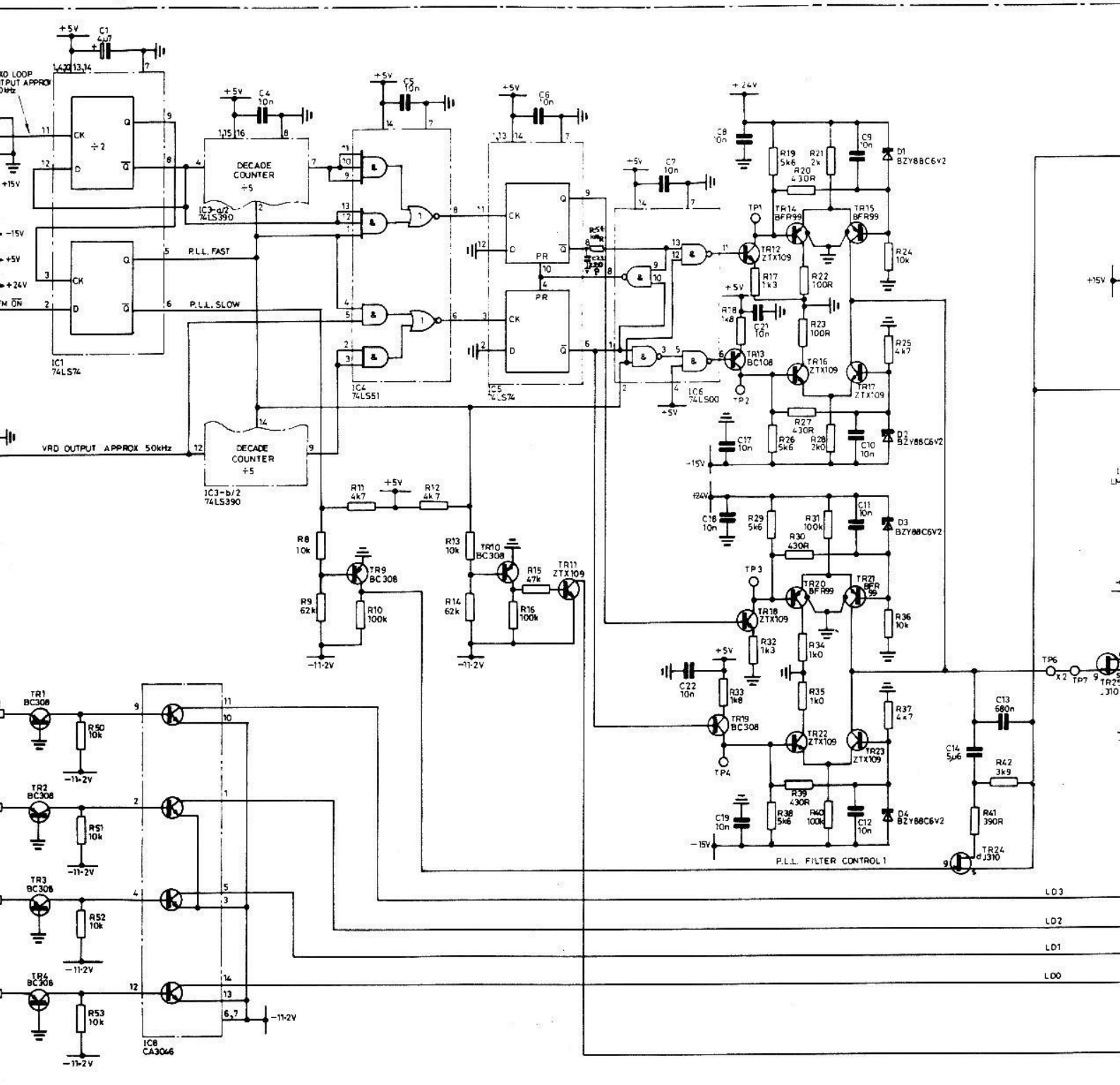
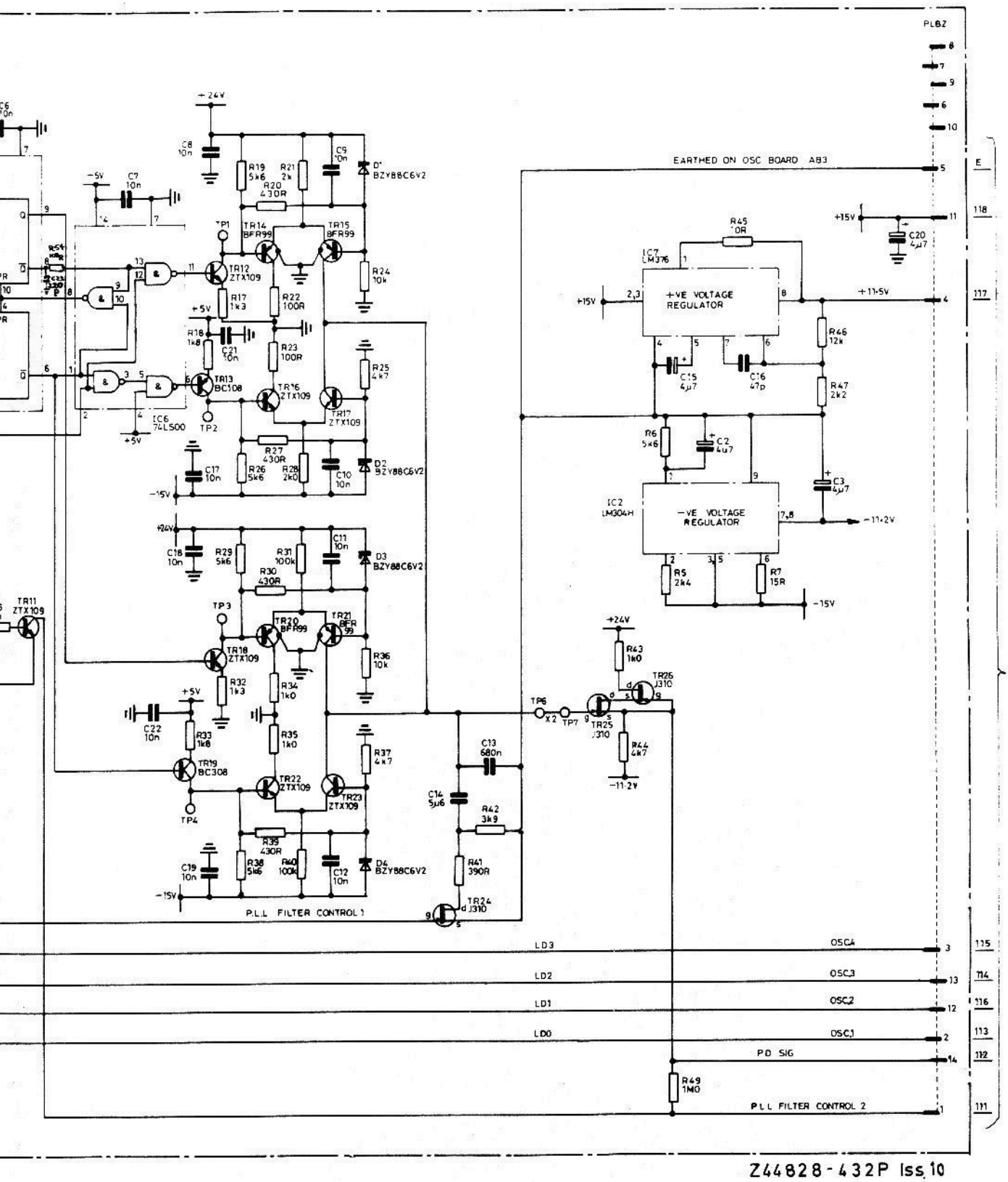

+5V
C1
4u7
VCXO LOOP OUTPUT APPROX 100kHz
CONNECTED TO VCXO LOOP ABS PLCF
PLCC
PLBY
+15V
-15V
+5V
+24V
LD5
FM ON
÷2
CK
D
Q
DECADE COUNTER ÷5
IC3-a/2 74LS390
P.L.L. FAST
P.L.L. SLOW
IC1 74LS74
IC4 74LS51
IC5 74LS74
PLCB
CONNECTED TO OUTPUT VRD ABI PLBU
VRD OUTPUT APPROX 50kHz
IC3-b/2 74LS390
R11 4k7
R12 4k7
R8 10k
R13 10k
TR9 BC308
TR10 BC308
R9 62k
R10 100k
R14 62k
R16 100k
R15 47k
-11·2V
CONNECTED TO MICROPROCESSOR SYSTEM AA2 PLBF VIA CAPS SHOWN
LD3
LD2
LD1
LD0
R1 820R
R2 820R
R3 820R
R4 820R
TR1 BC308
TR2 BC308
TR3 BC308
TR4 BC308
R50 10k
R51 10k
R52 10k
R53 10k
IC6 CA3046

Fig. 12

Sep. 81



Output phase detector, AB4

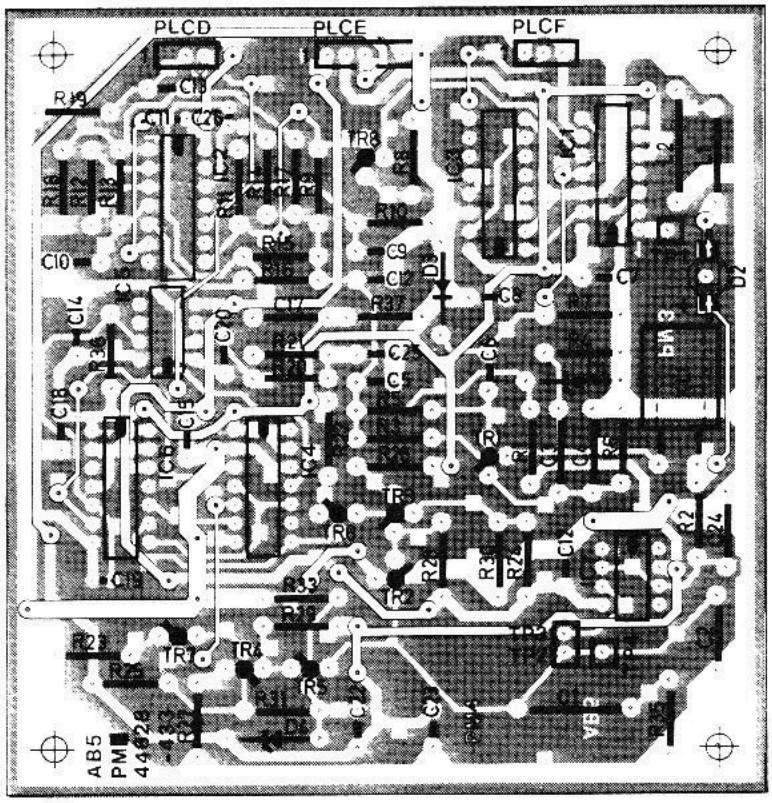


Z44828-432P Iss 10

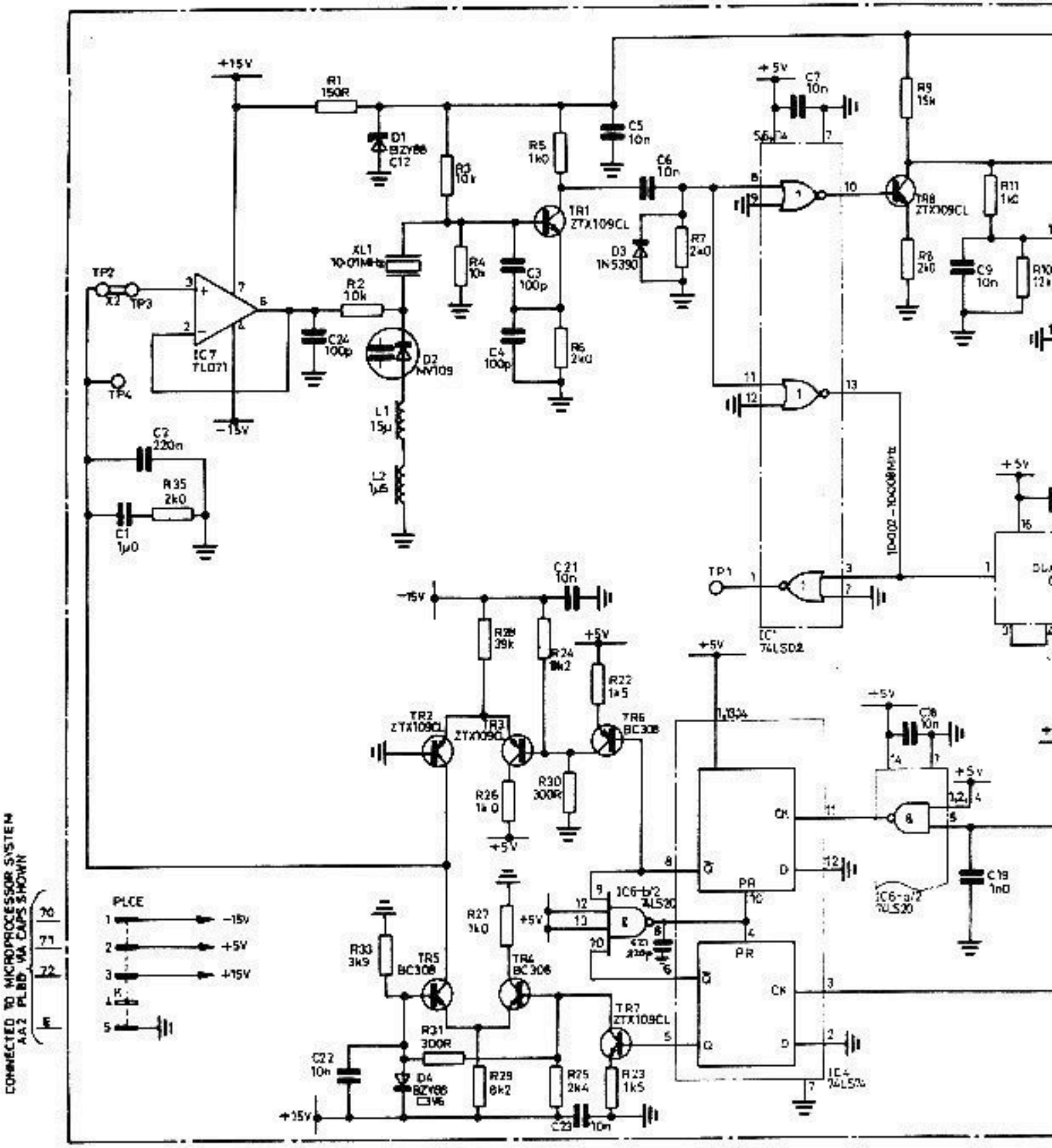
AB4

Output phase detector, AB4

Fig. 12
Chap. 7
Page 25



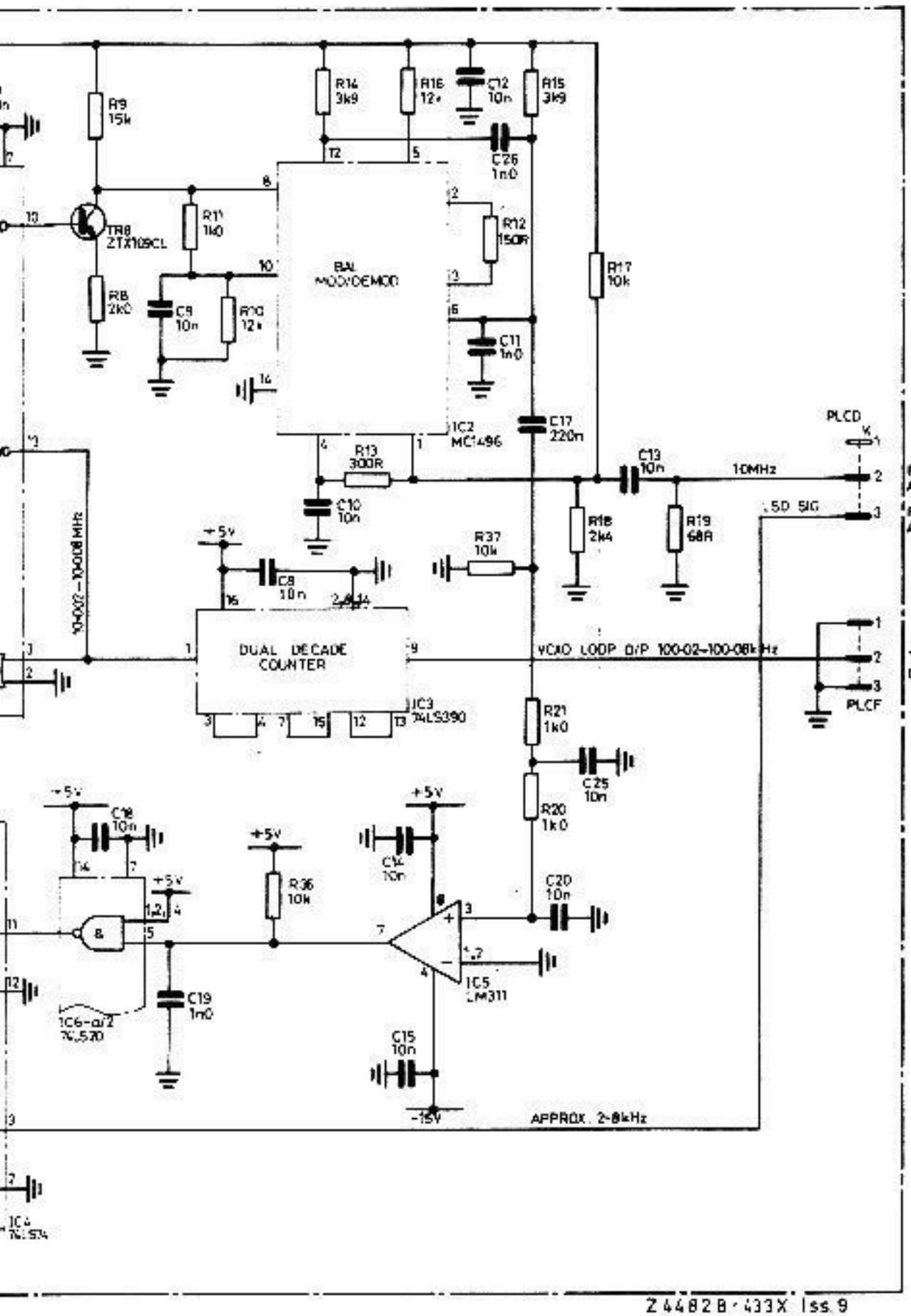
Component layout, AB5



Voltage controlled crystal oscillator loop

Fig. 13

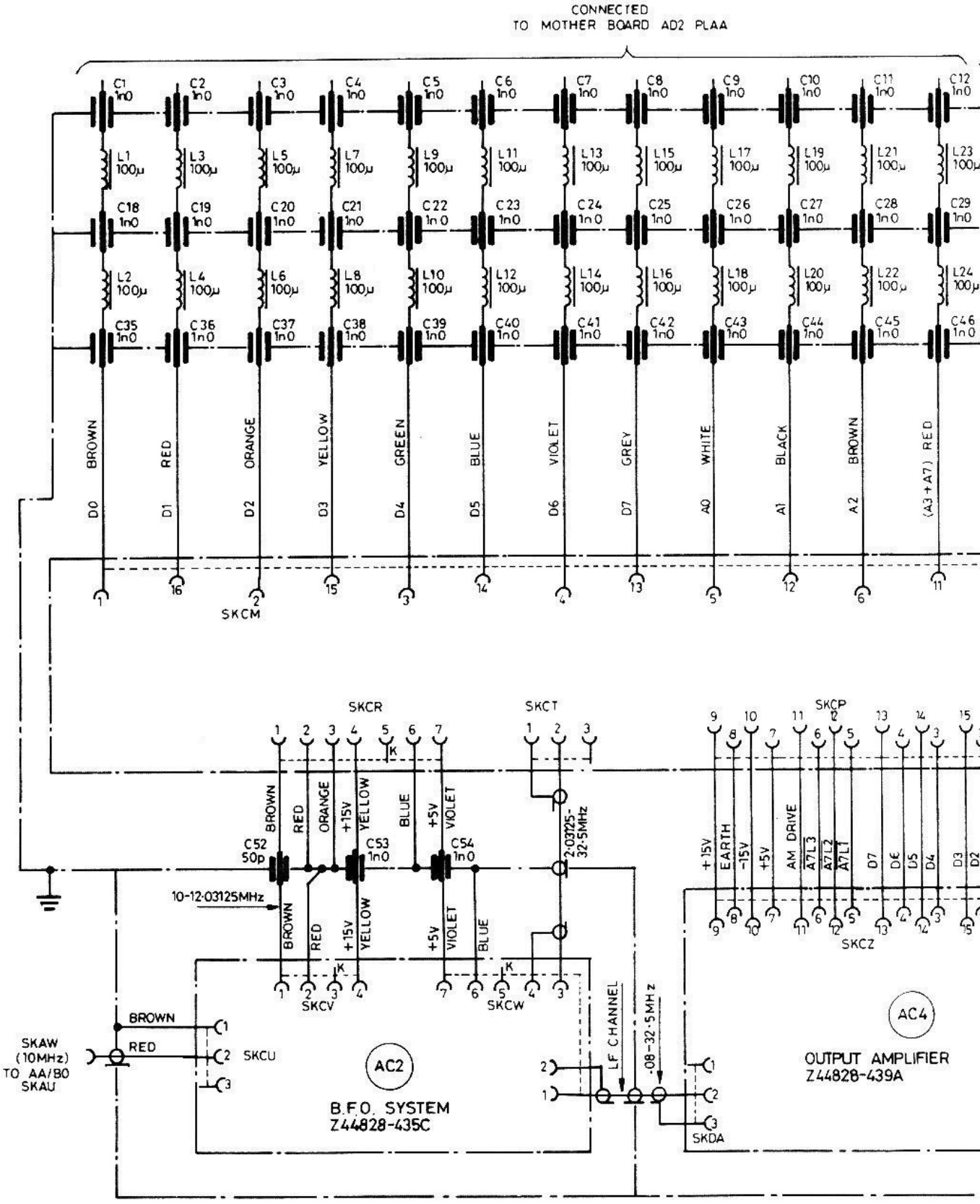
Sep. 81



Z 44828-433X Iss 9

AB5

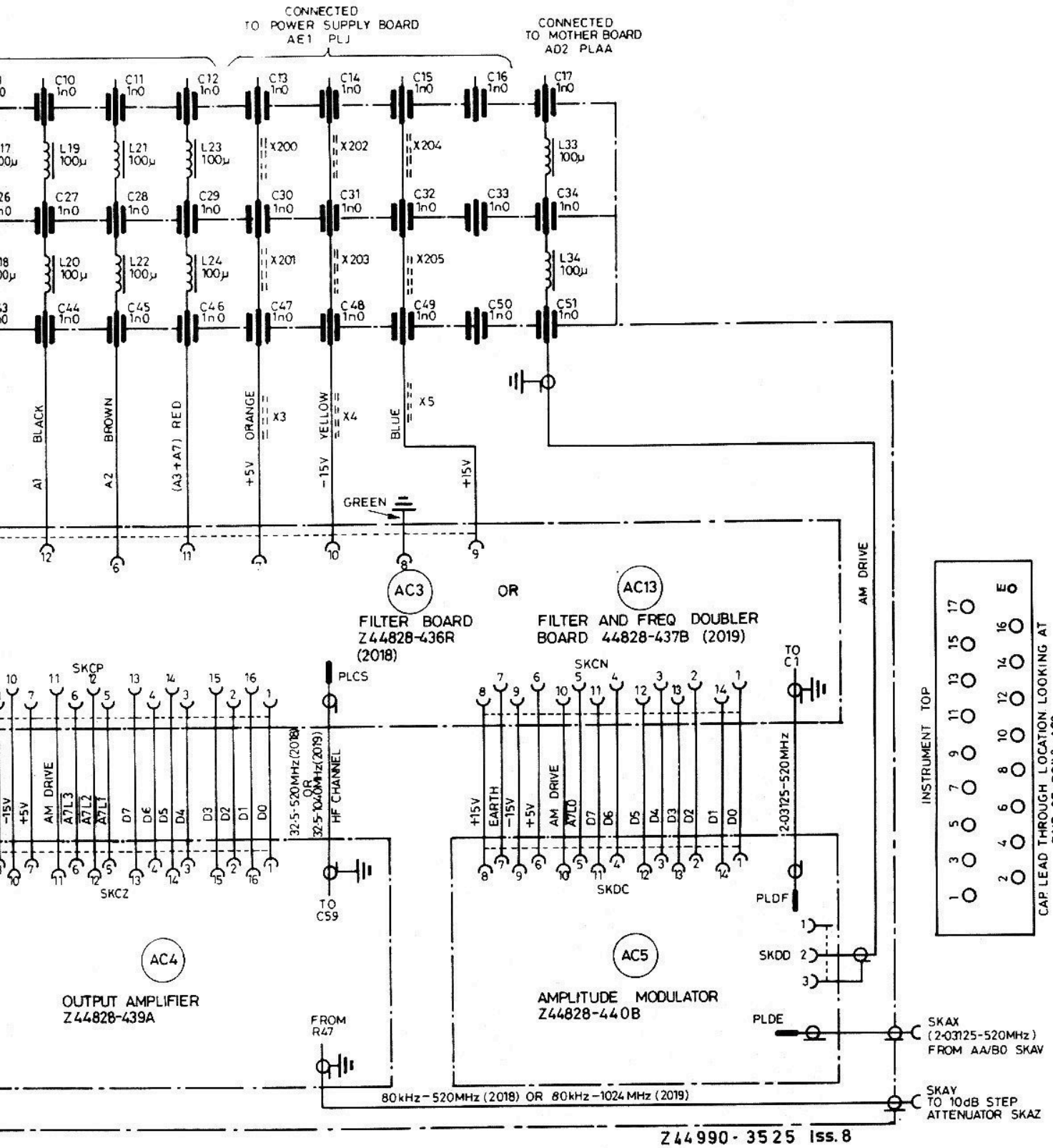
d crystal oscillator loop, AB5



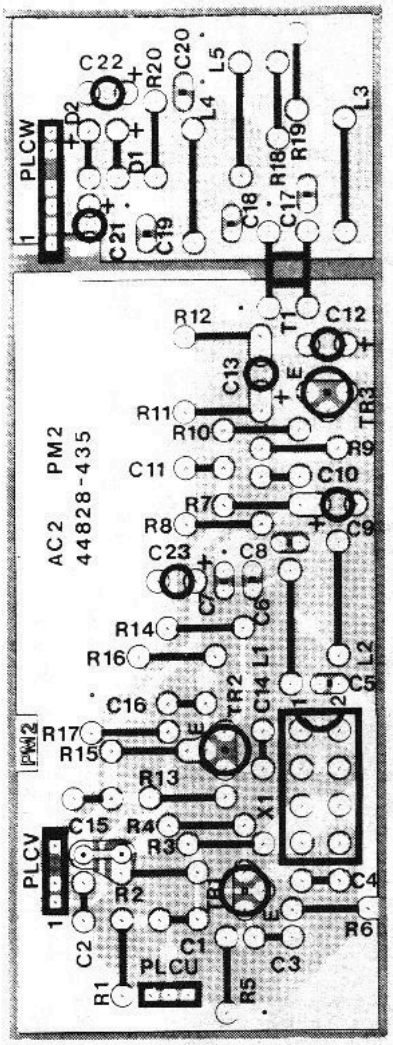
RF box 2 intercon

Fig. 14

Sep. 81

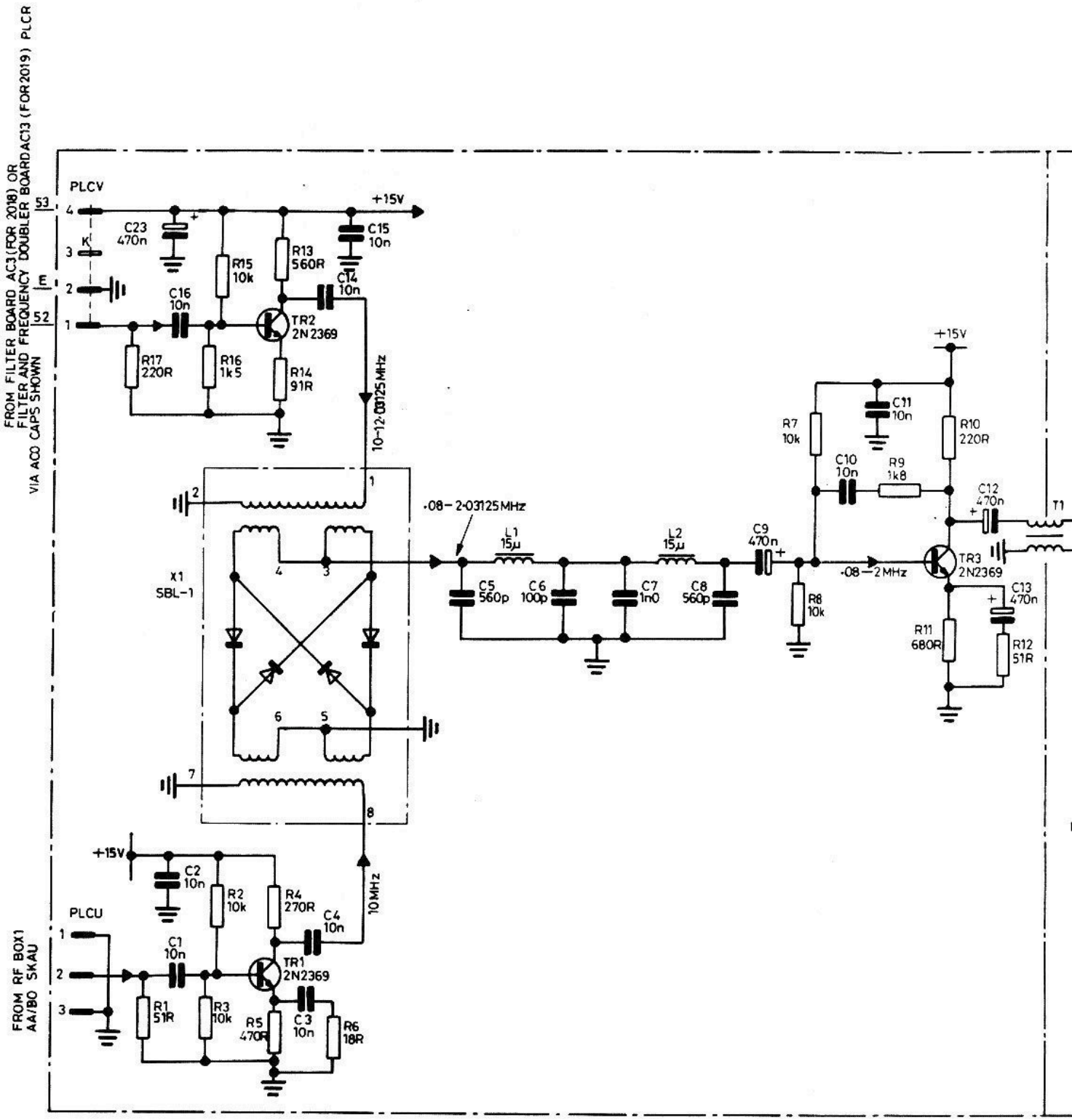


RF box 2 interconnections, AC0



Component layout, AC2

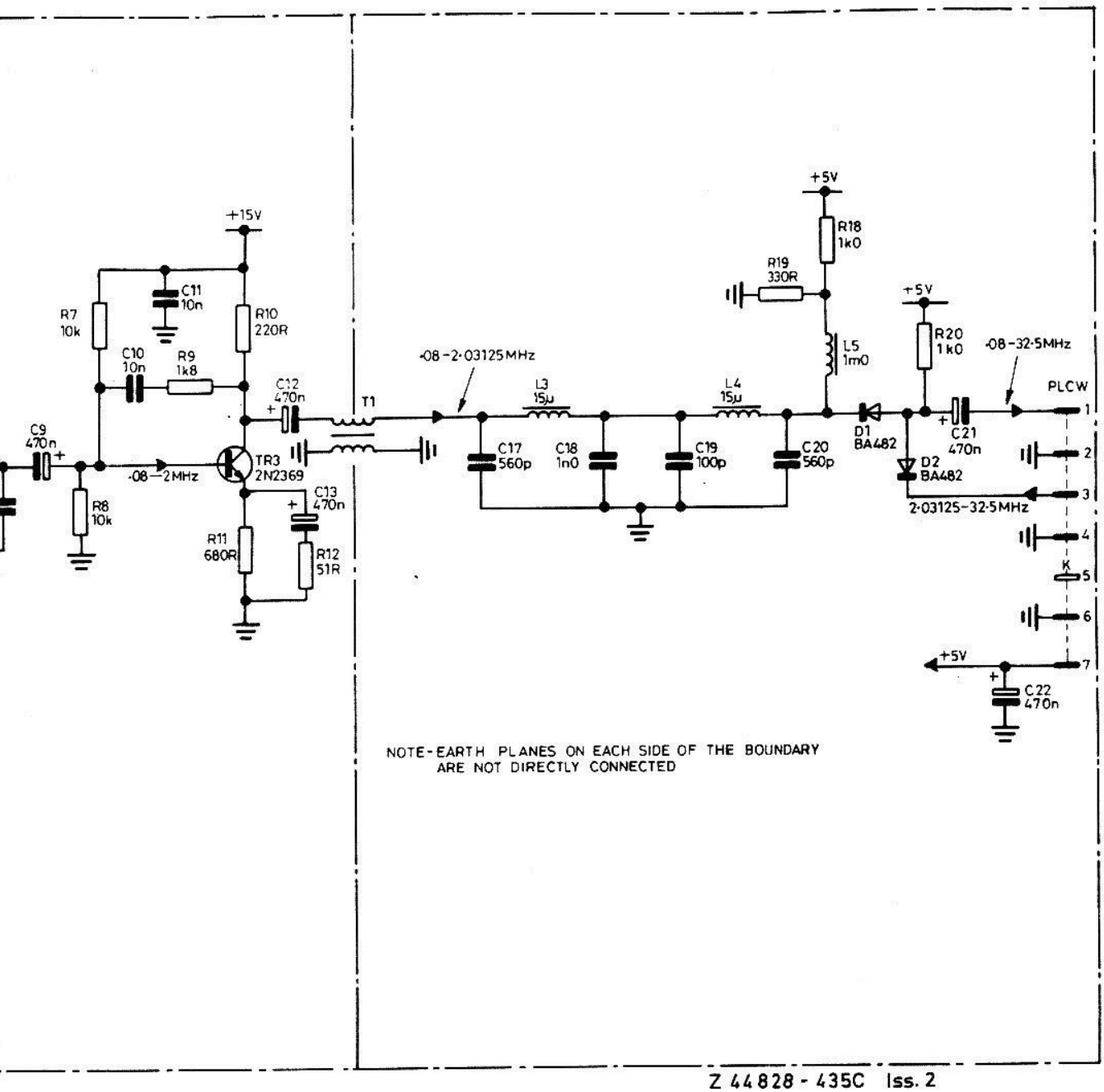
Fig. 15a



BFO system, AC2

Fig. 15

Sep. 81

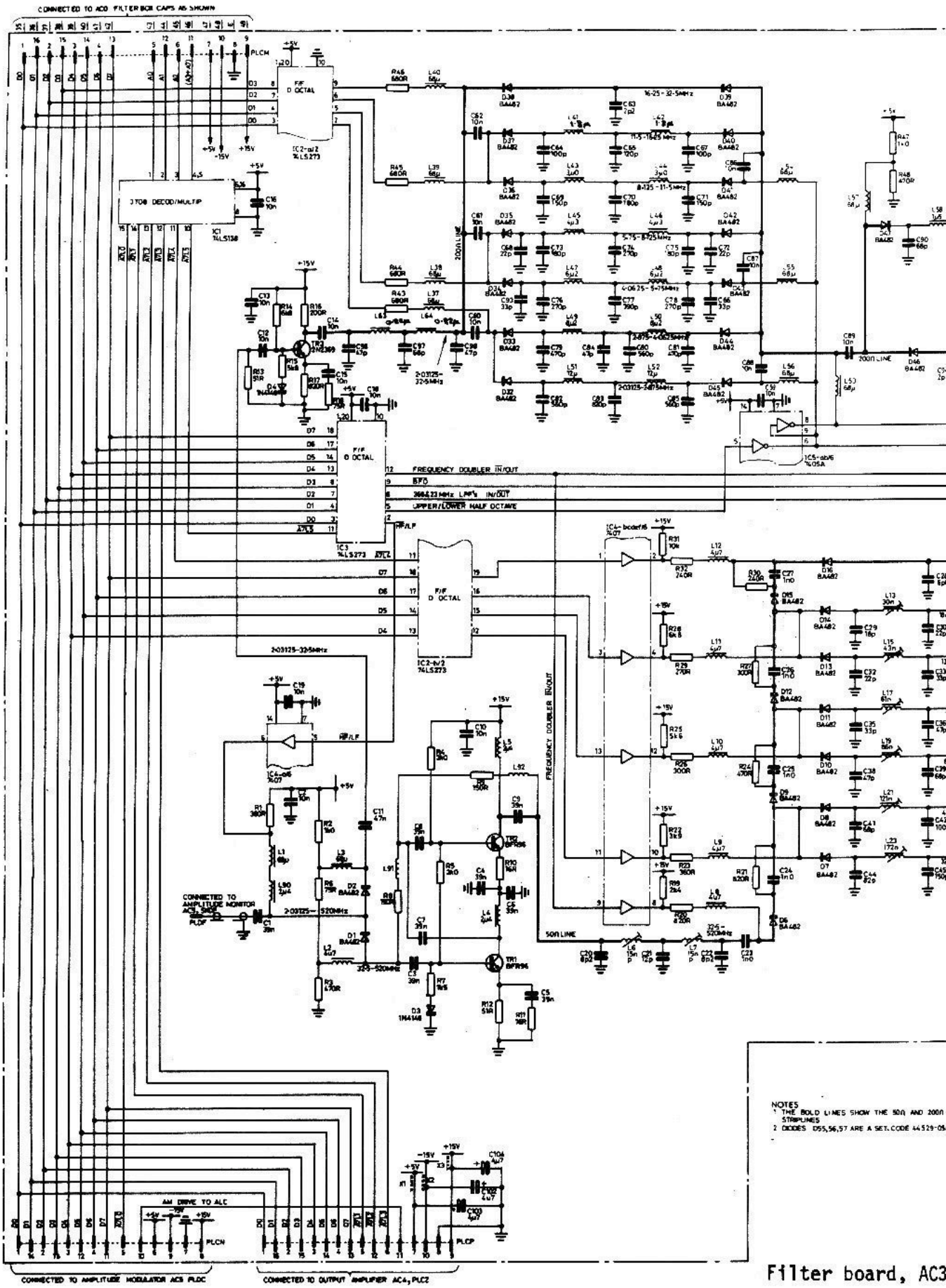


Z 44828 - 435C Iss. 2

AC2

BFO system, AC2

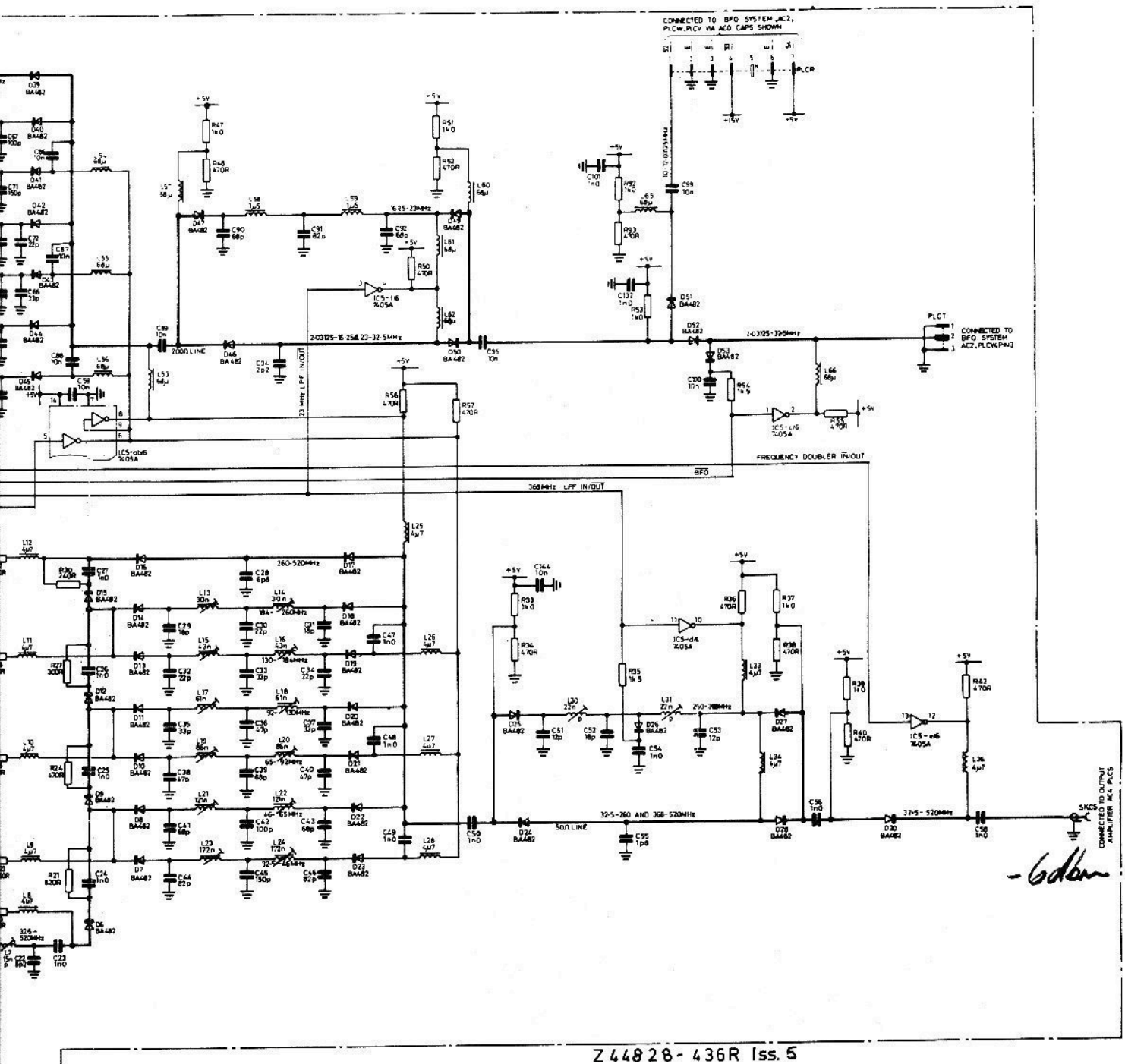
Fig. 15
Chap. 7
Page 31/32



Filter board, AC3

Fig. 16

Sep. 81

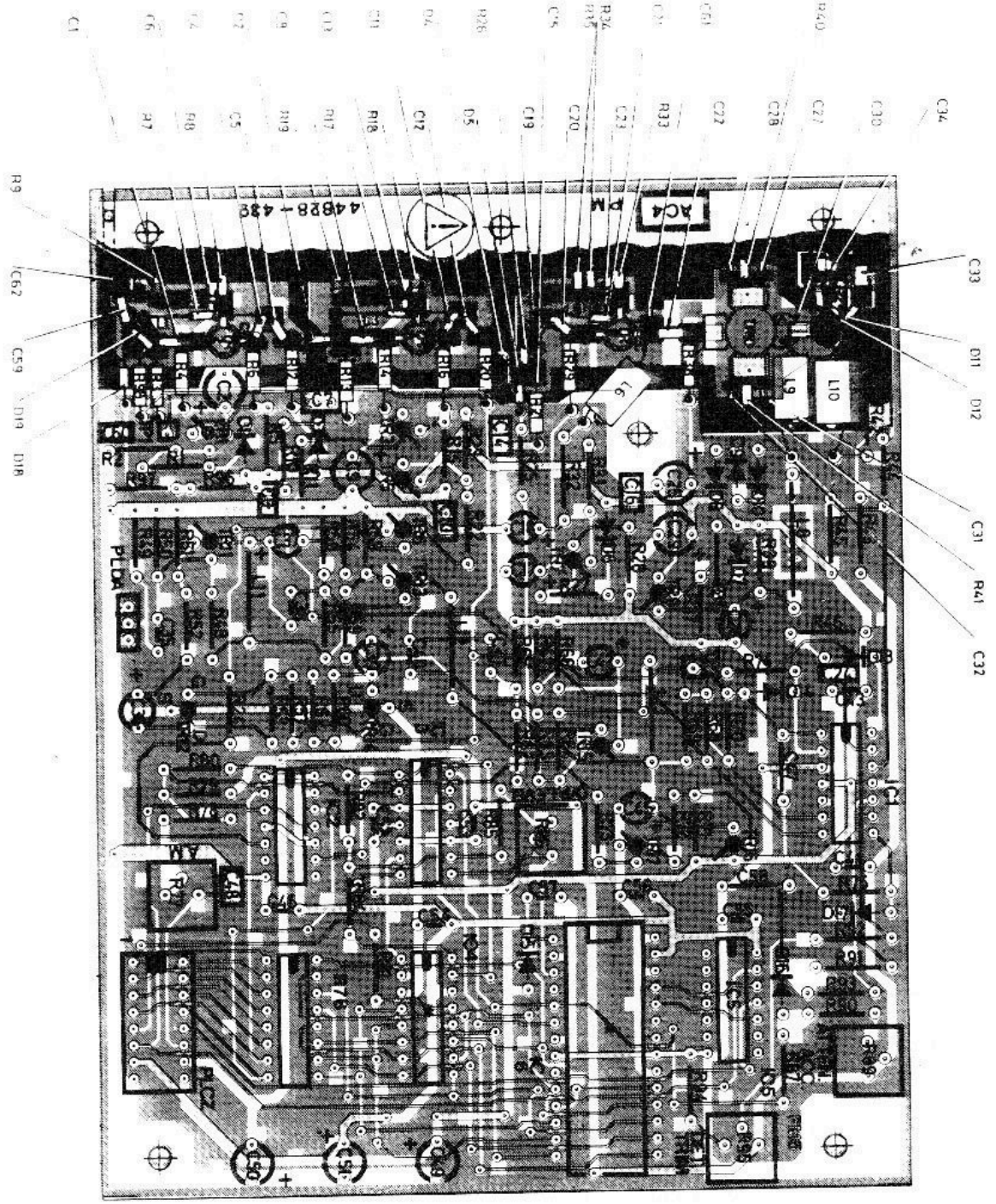


Z44828-436R Iss. 5

NOTES
1 THE BOLD LINES SHOW THE 50Ω AND 200Ω STRIPLINES
2 DIODES D55,56,57 ARE A SET. CODE 44529-058G

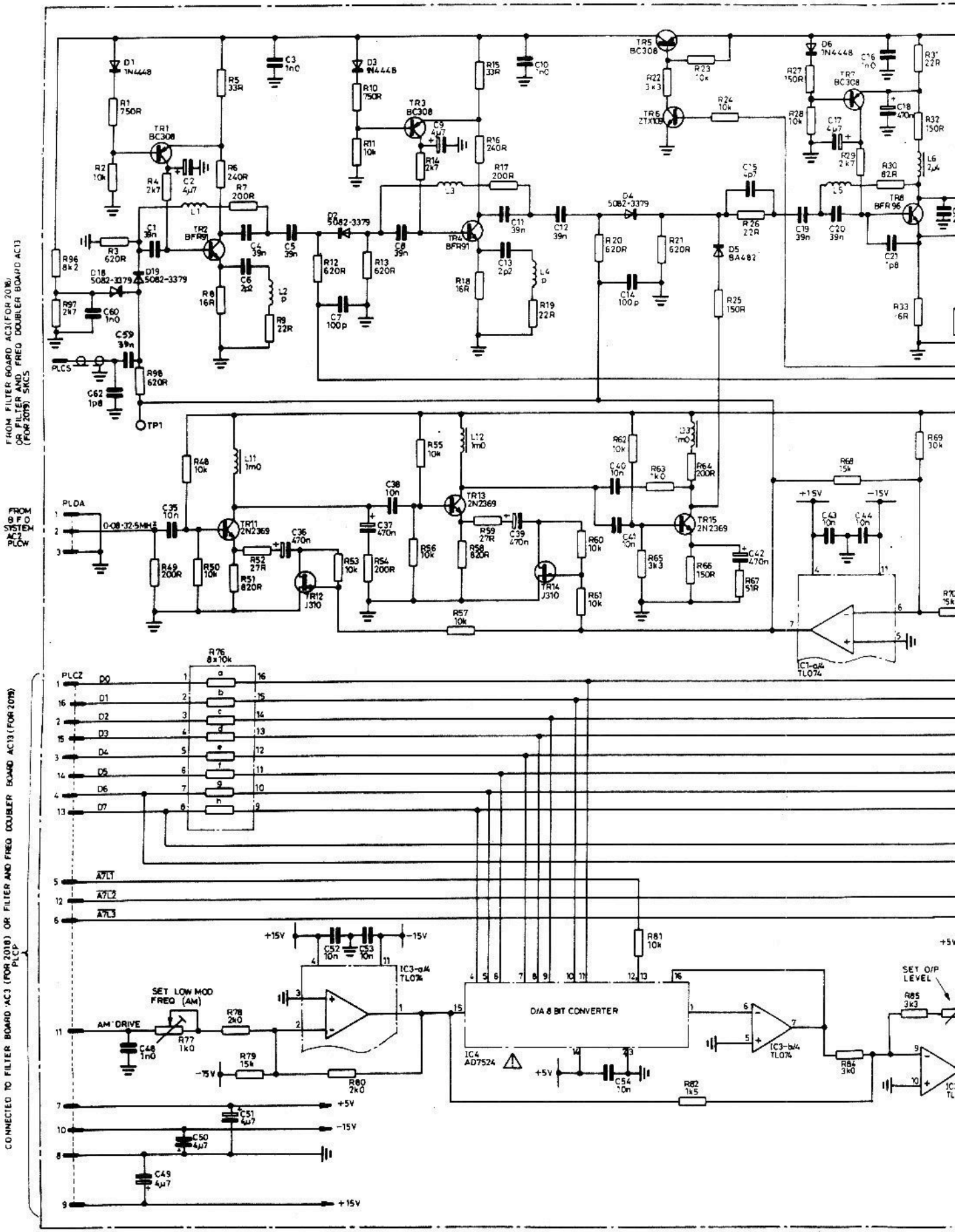
Filter board, AC3 (for component layout see Fig. 19a)

AC3



Component layout, AC4

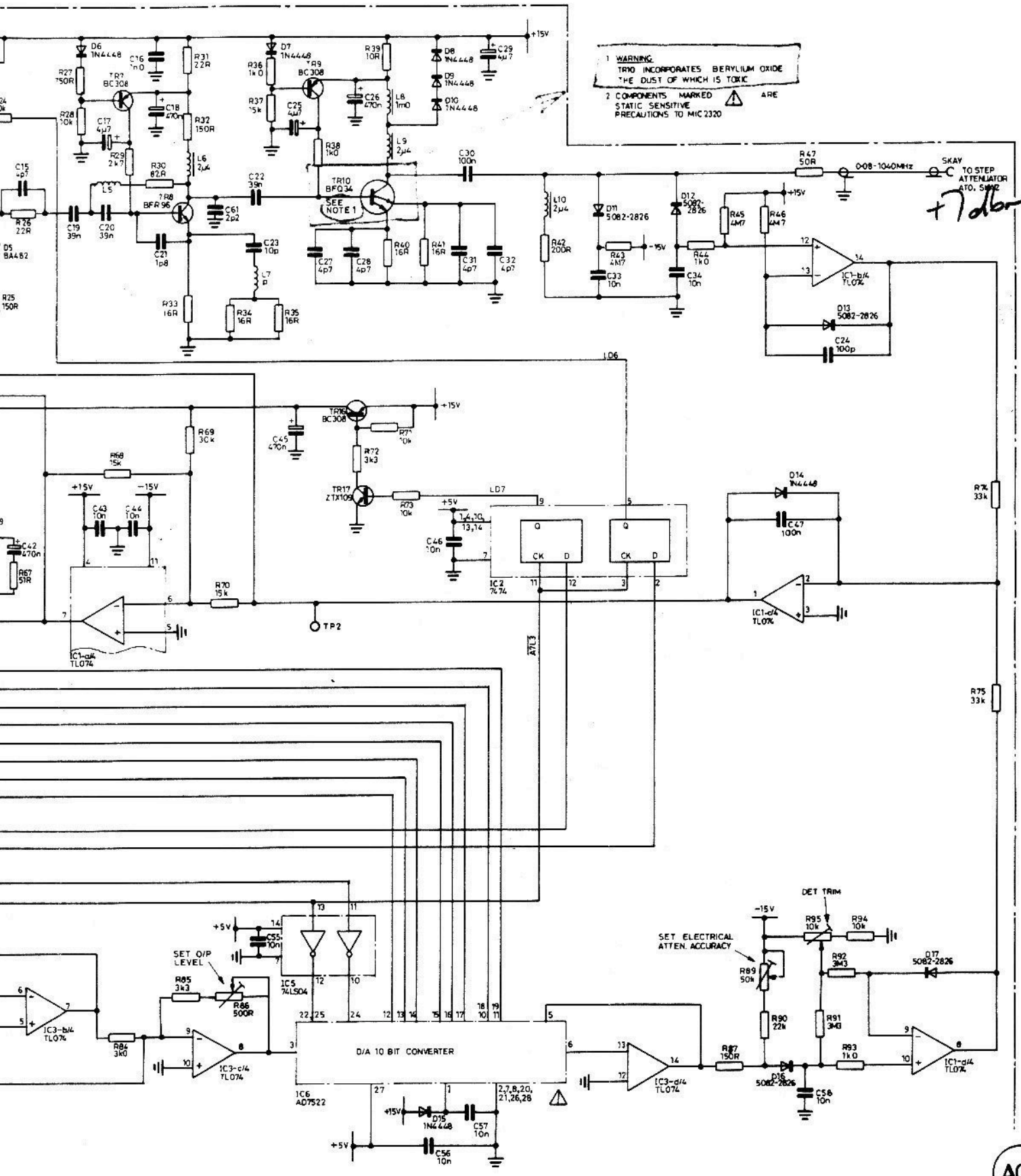
Fig. 17a



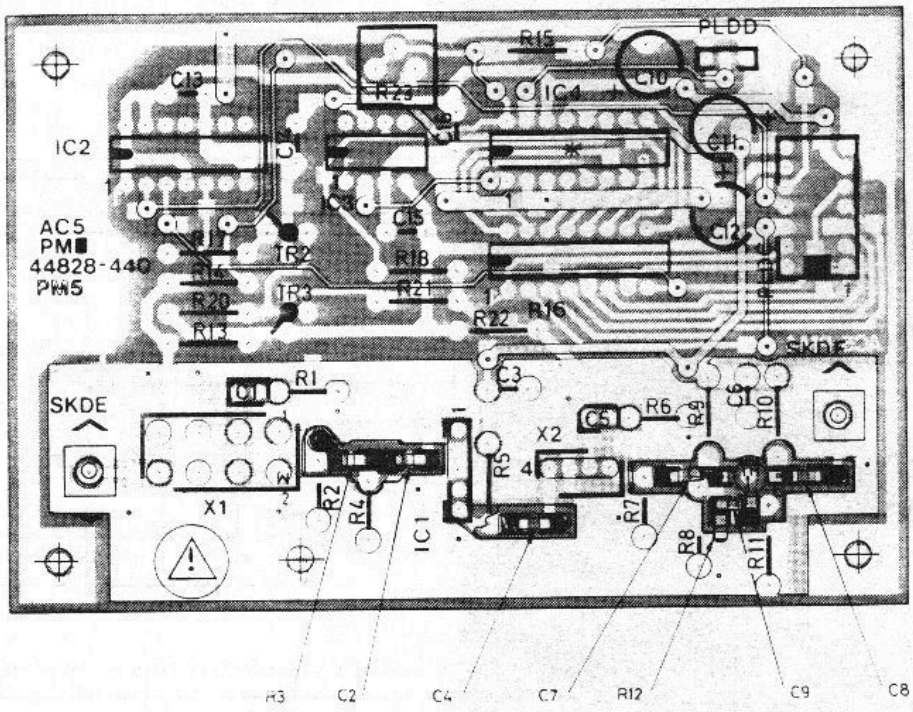
Output amplifier,

Fig. 17

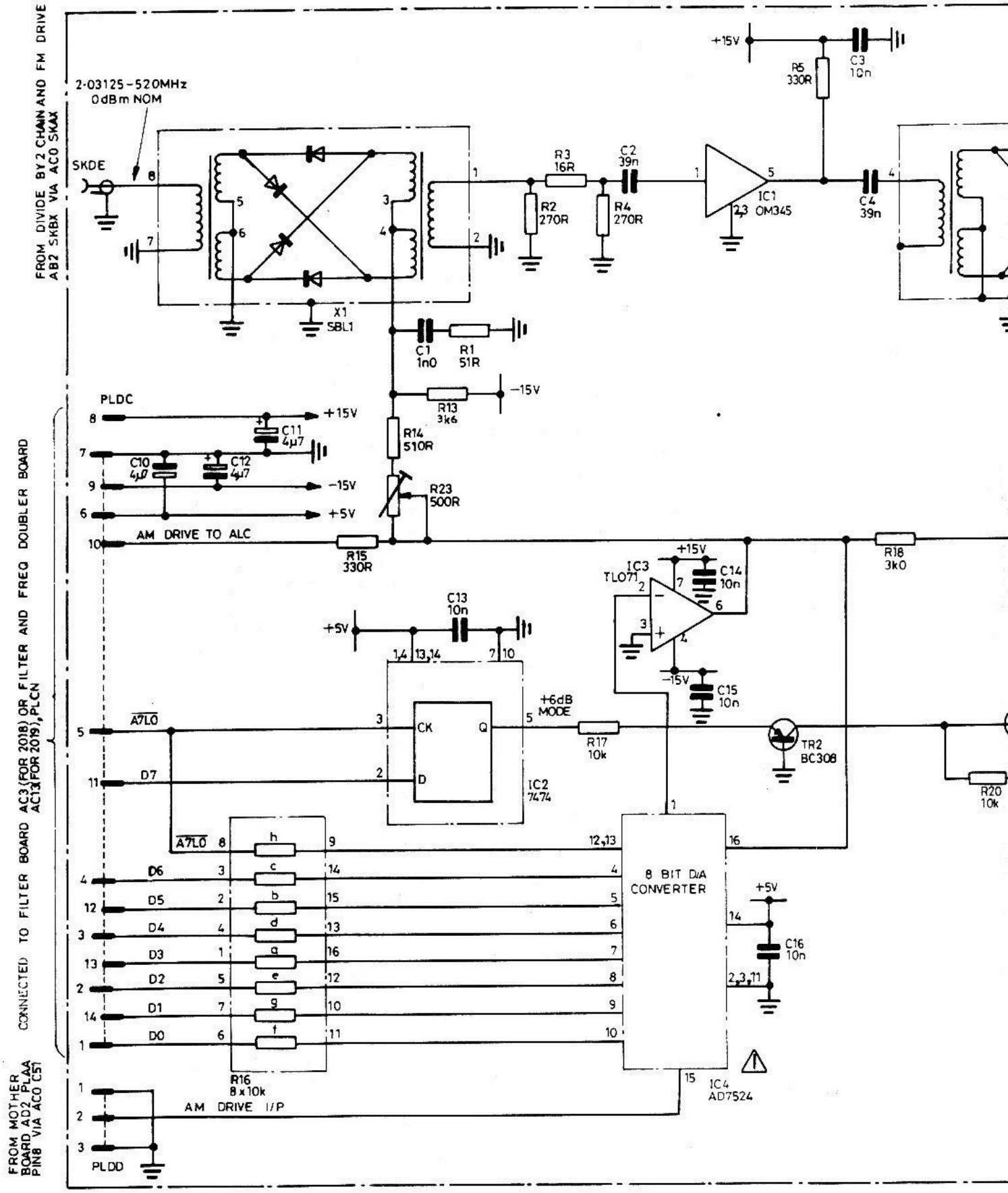
Sep. 81


1 WARNING
TR10 INCORPORATES BERYLIUM OXIDE
THE DUST OF WHICH IS TOXIC
2 COMPONENTS MARKED ⚠ ARE
STATIC SENSITIVE
PRECAUTIONS TO MIC2320
TR8 BFR96
TR9 BC308
TR10 BFQ34
SEE NOTE 1
TR16 BC308
TR17 ZTX109
IC1-a/d TL074
IC1-b/d TL074
IC1-c/d TL074
IC2 74LS74
IC3-a/d TL074
IC3-b/d TL074
IC3-c/d TL074
IC5 74LS04
IC6 AD7522
D/A 10 BIT CONVERTER
SET O/P LEVEL
SET ELECTRICAL ATTEN. ACCURACY
DET TRIM
TP2
0-08-1040MHz
TO STEP ATTENUATOR ATO. SMA
+15V
-15V
+5V

AC4



Component layout, AC5

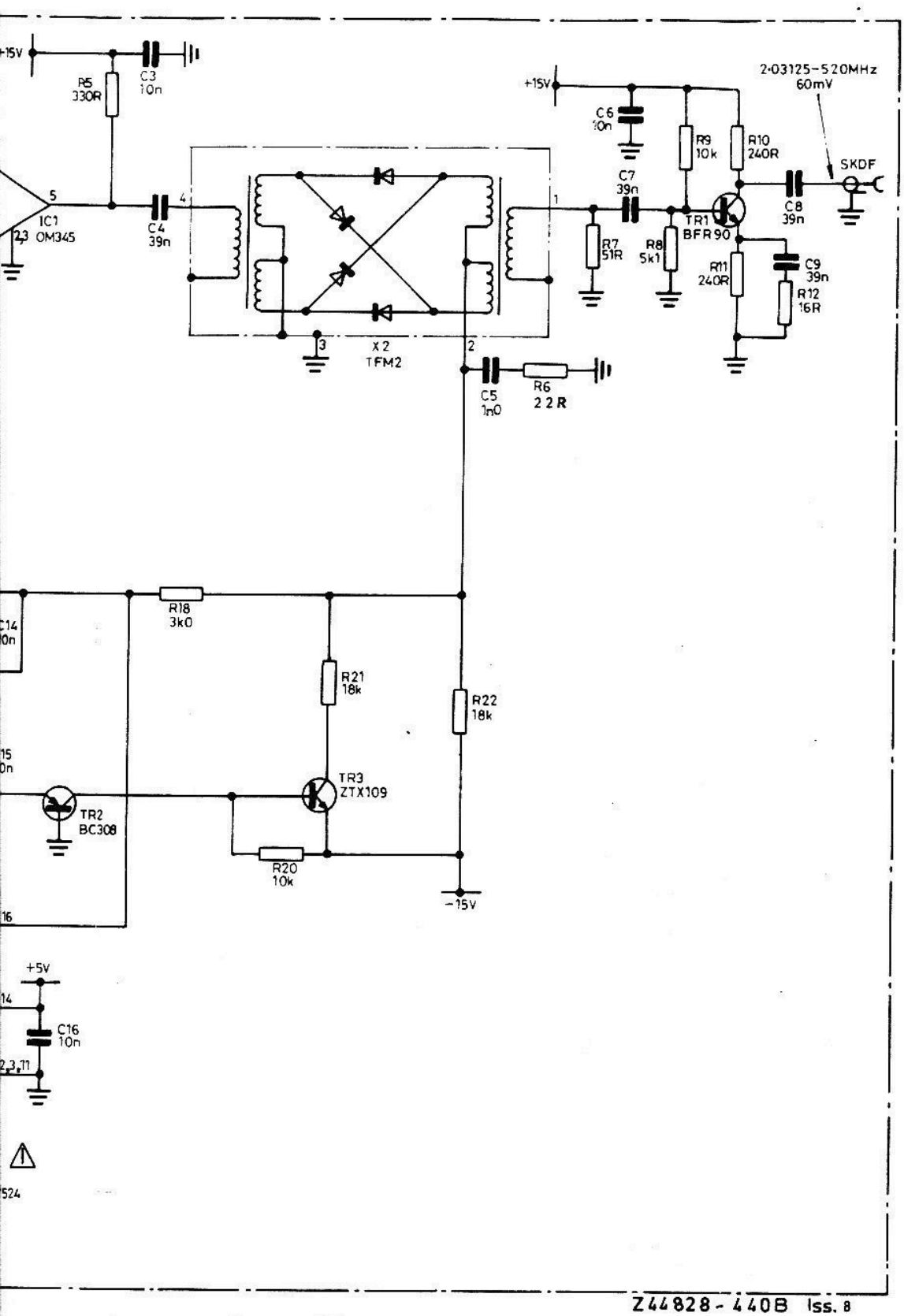


Amplitude modulator,

Fig. 18

Sep. 81

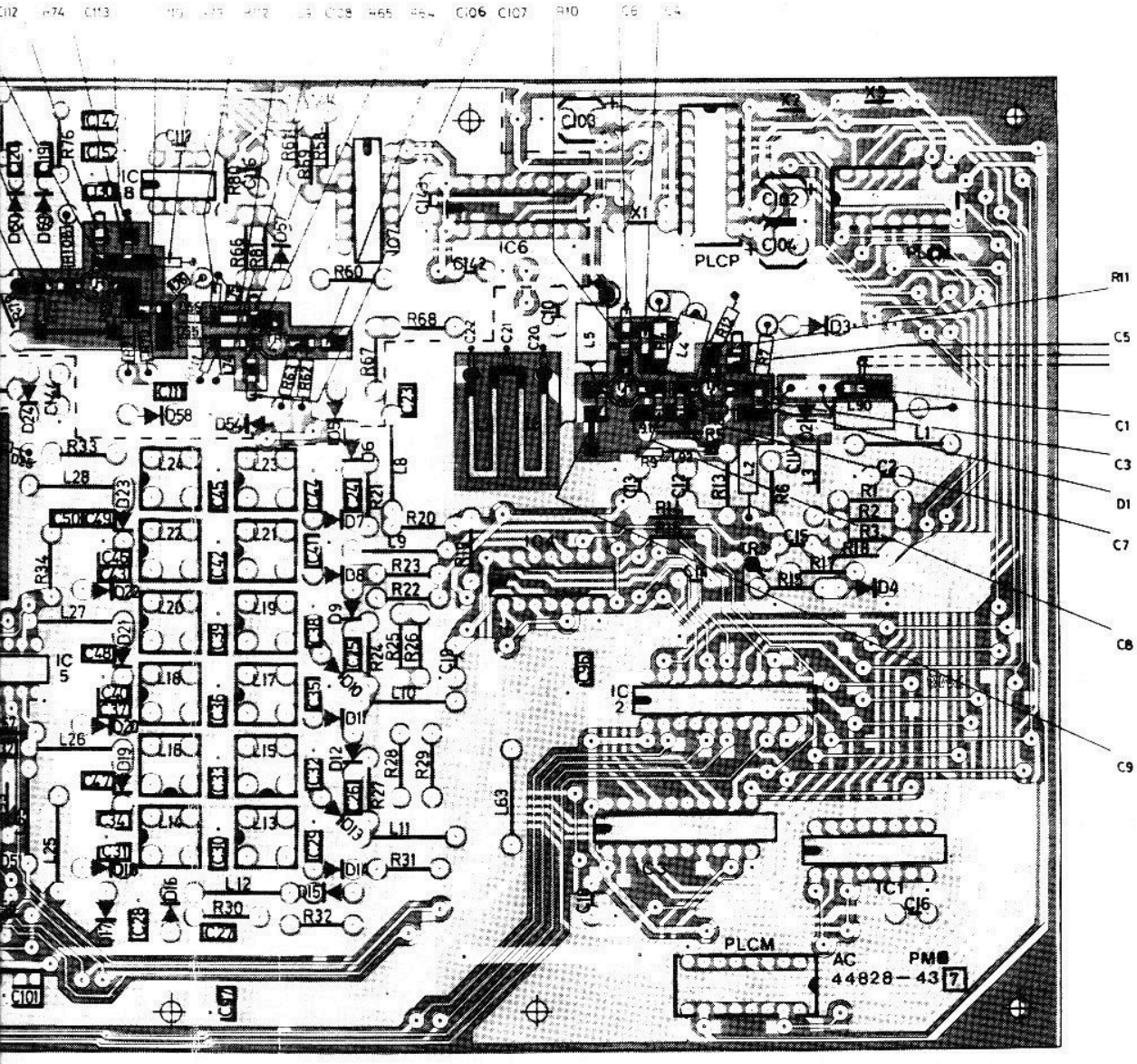
1. COMPONENT MARKED ⚠ IS STATIC SENSITIVE, PRECAUTIONS AS PER MIC 2320



Z44828-440B Iss. 8

Amplitude modulator, AC5

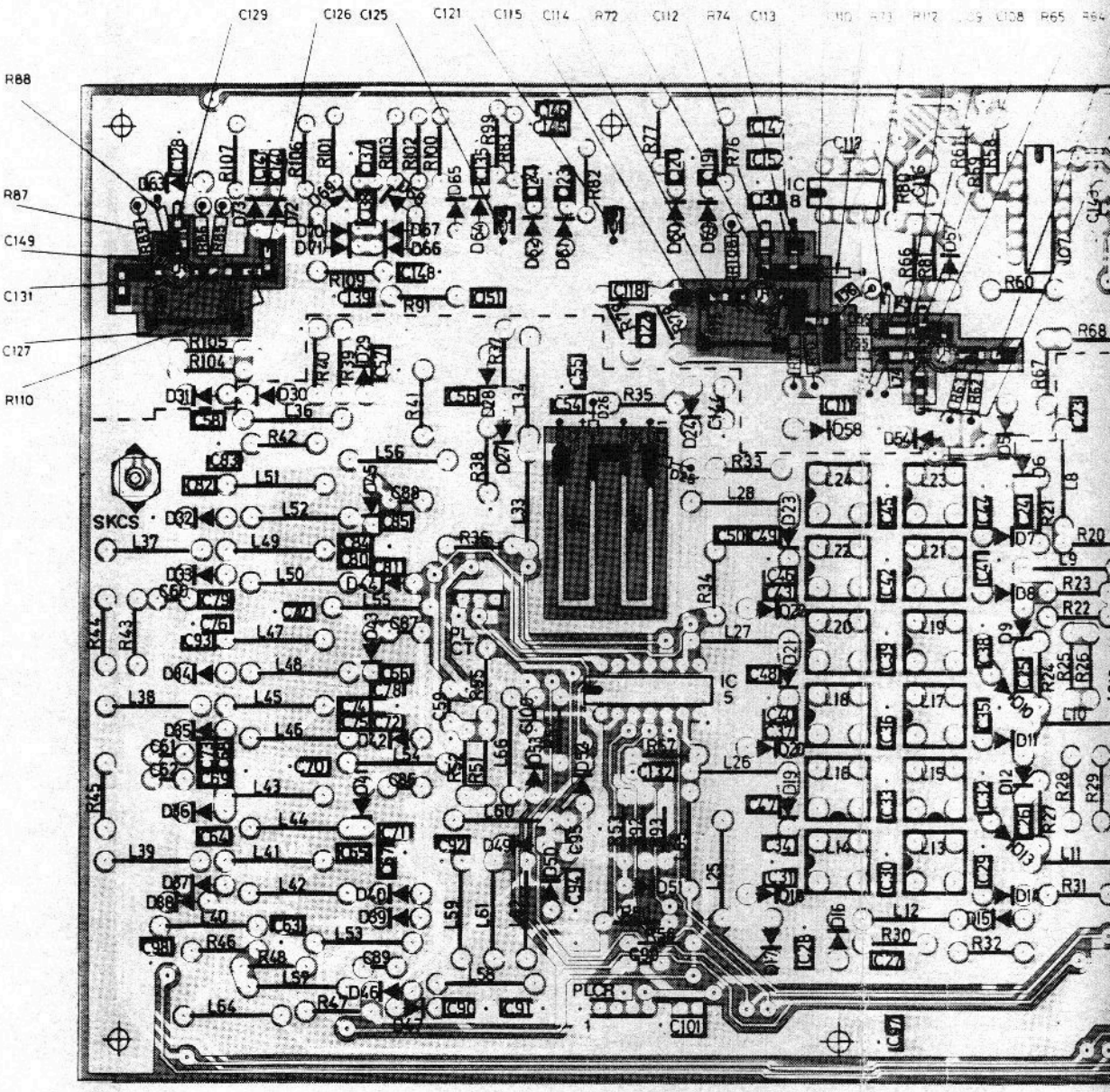
AC5



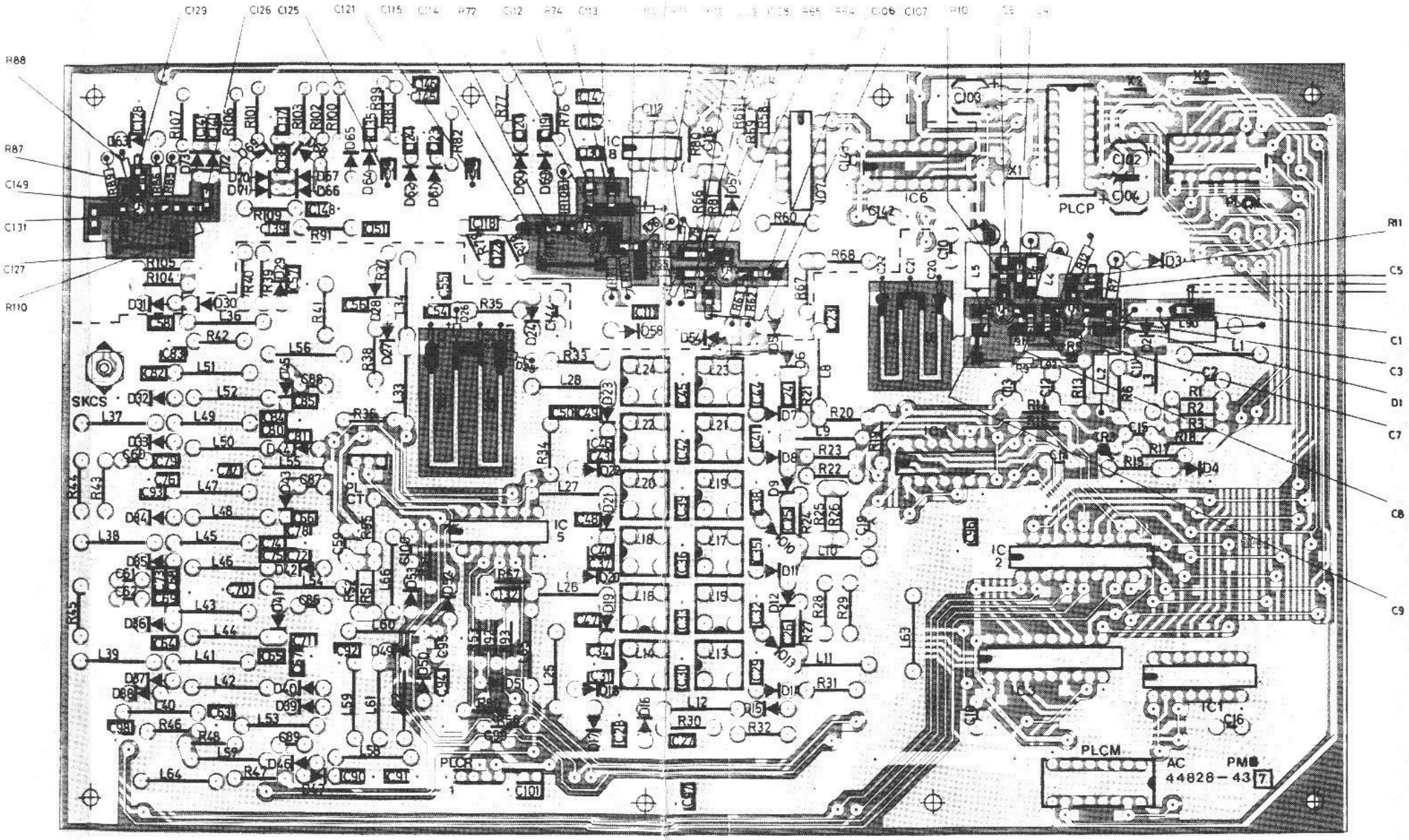
Component layout, AC3 & AC13

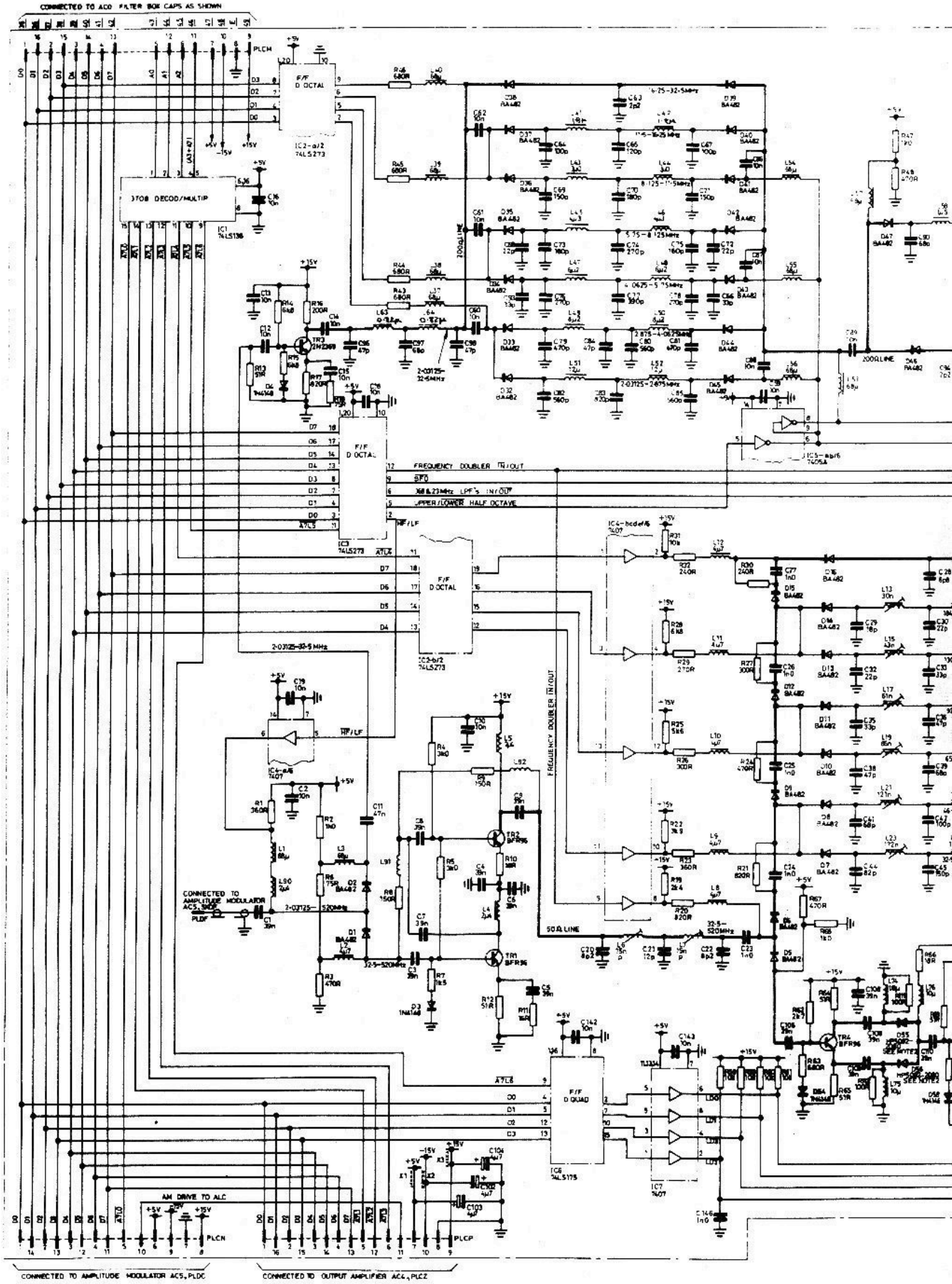
Fig. 19a

Sep. 81



Component layout. AC3 & AC13

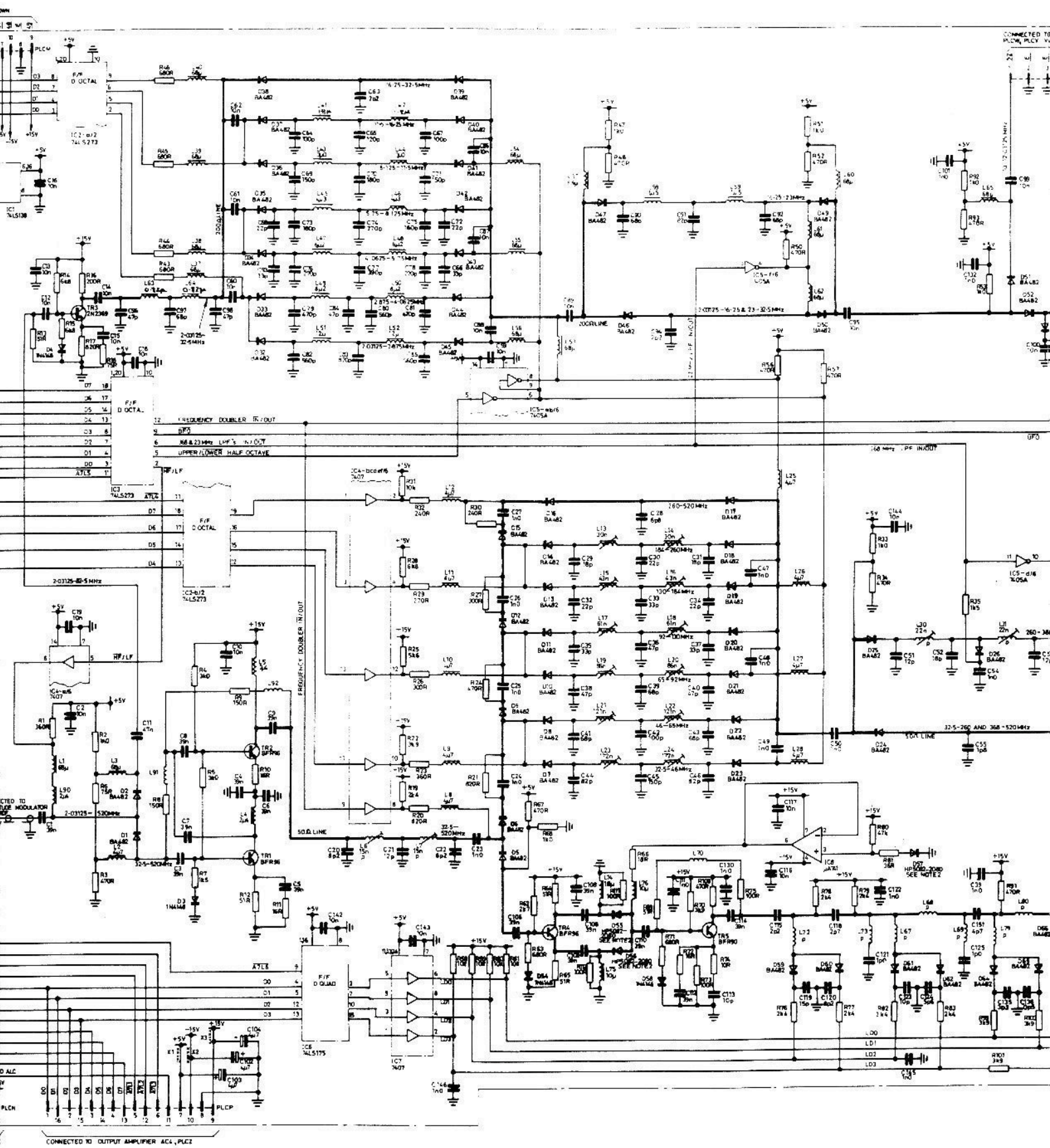

PLCP
PLCM
PLCR
SKCS
IC6
IC5
IC4
IC2
IC1
IC8
X1
AC
44828-43
PMB



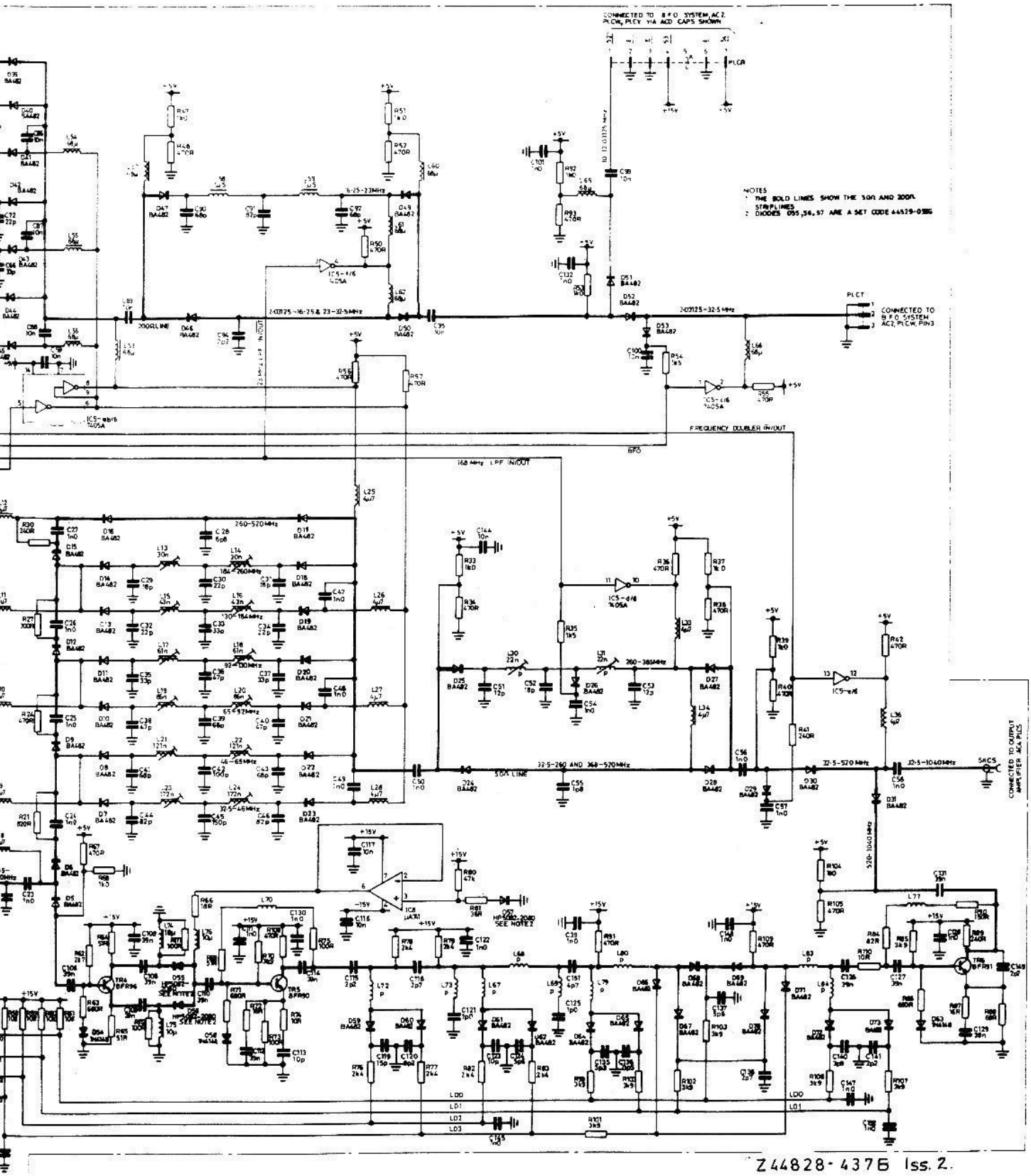
Filter and frequency doubler

Fig. 19

Sep. 81



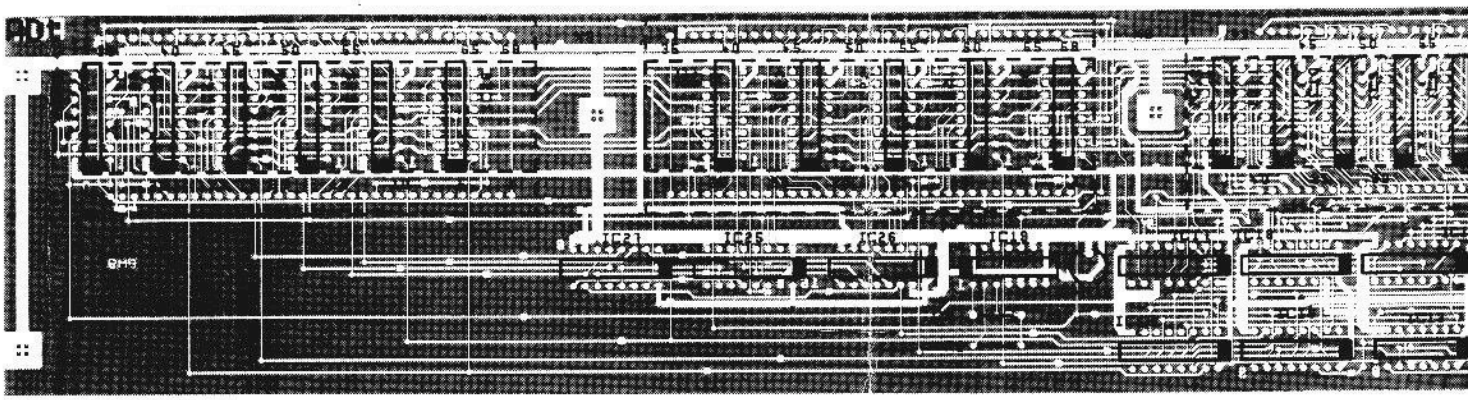
Filter and frequency doubler, AC13 (2019 only)



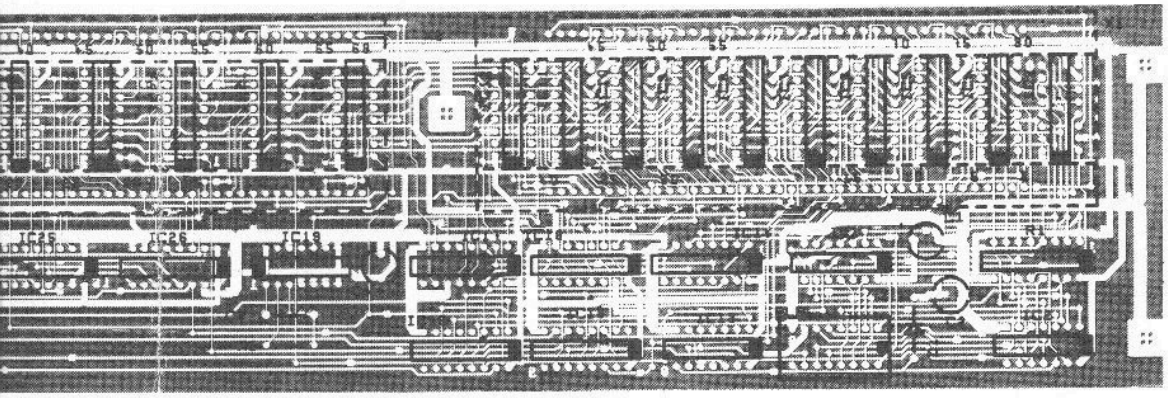
Z44828-4376 Iss. 2.

AC13

and frequency doubler, AC13 (2019 only)



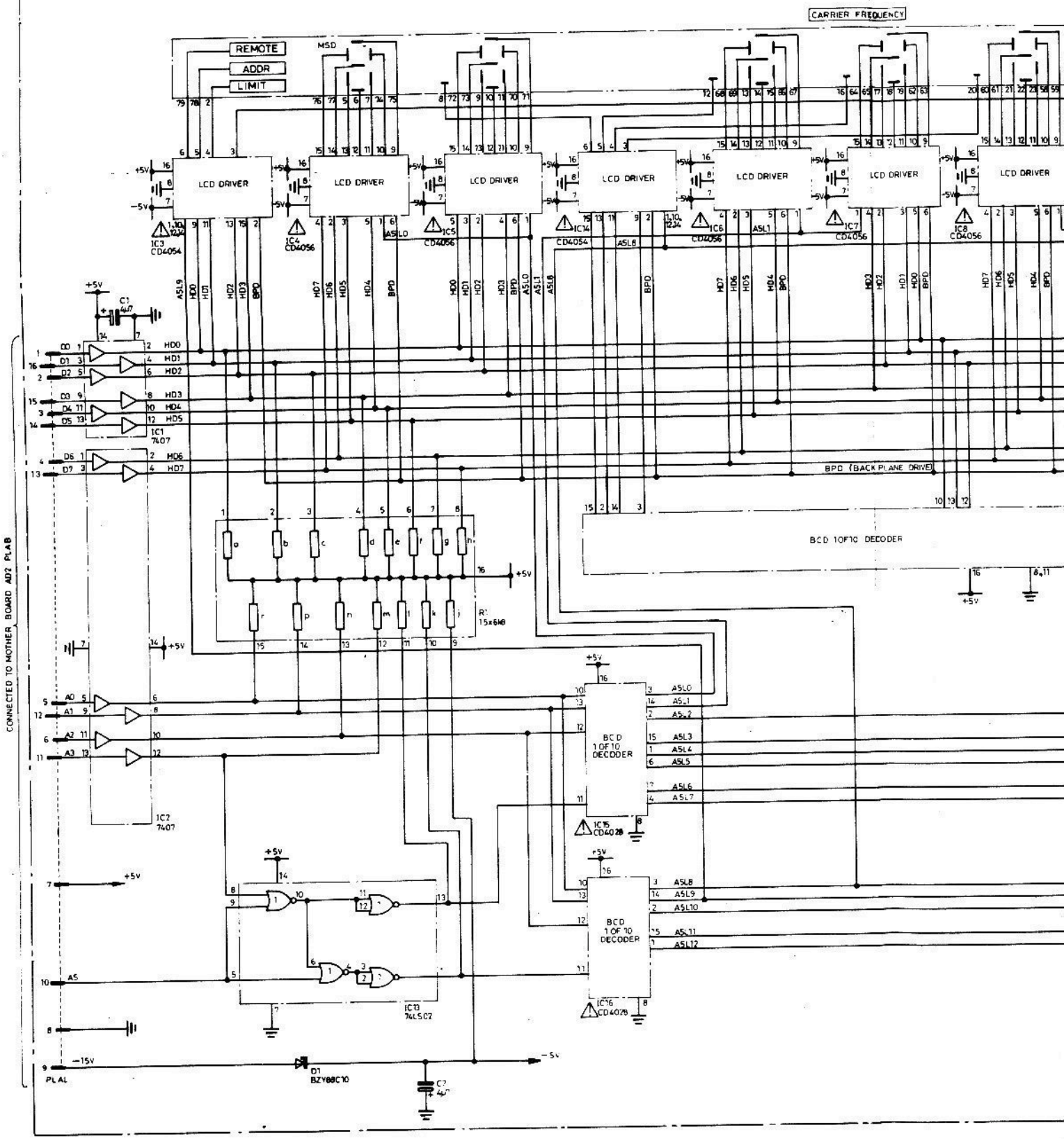
Component layout, AD1



Component layout, ADI

Fig. 20a

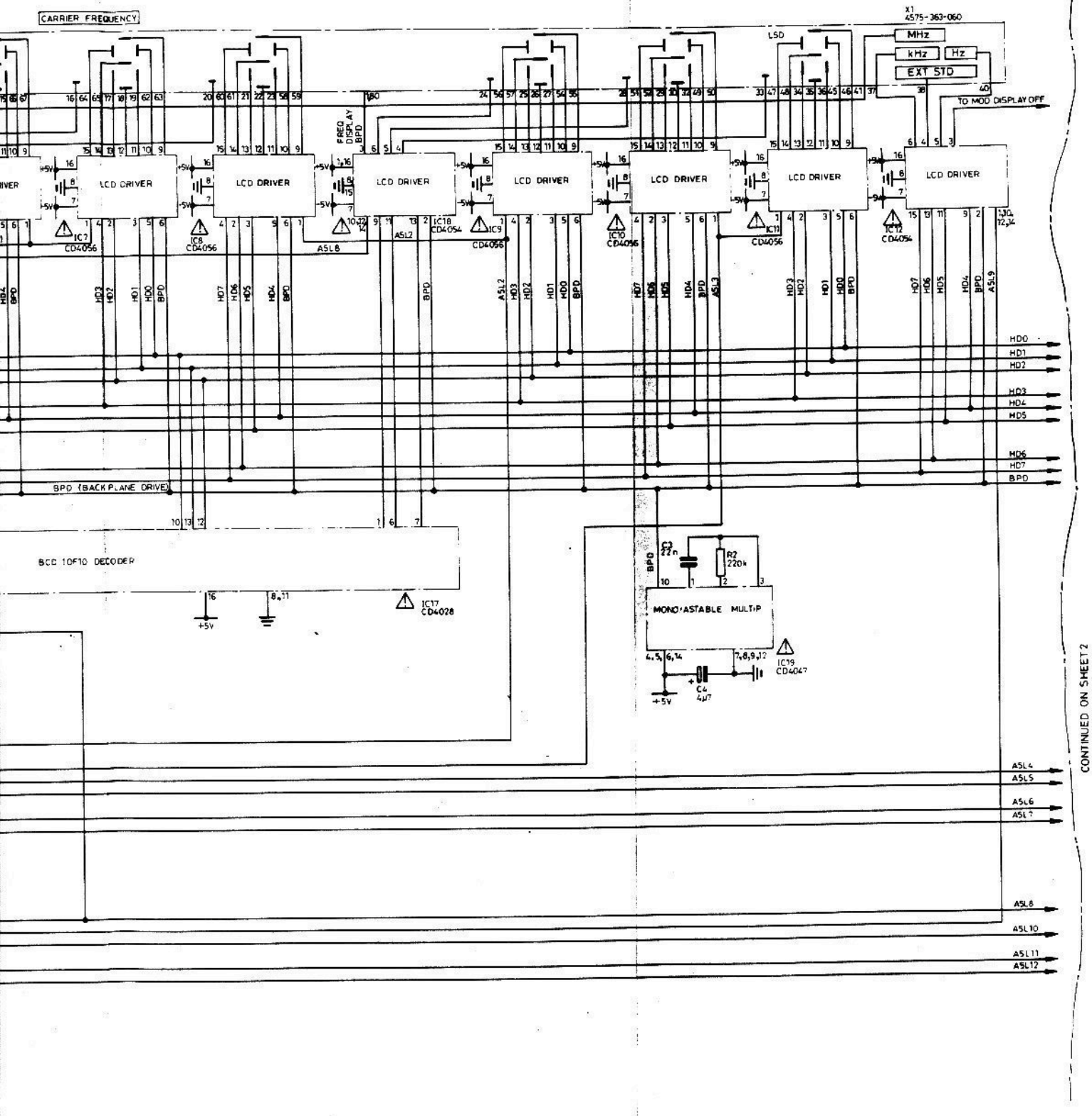
Sep. 81



Display board, AD1 (sheet

Fig. 20

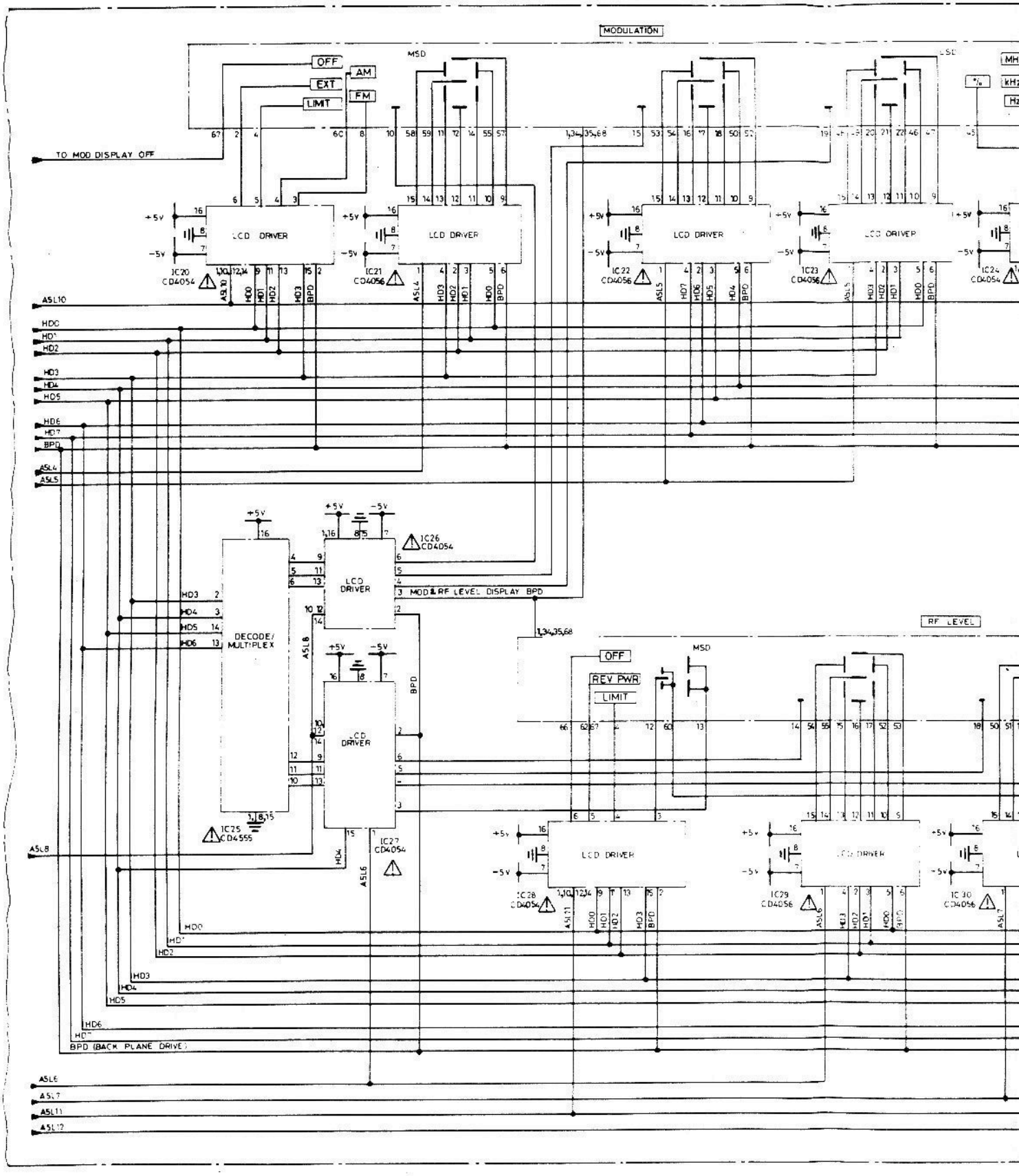
Sep. 81



Z44828-441K Iss 5

ADI

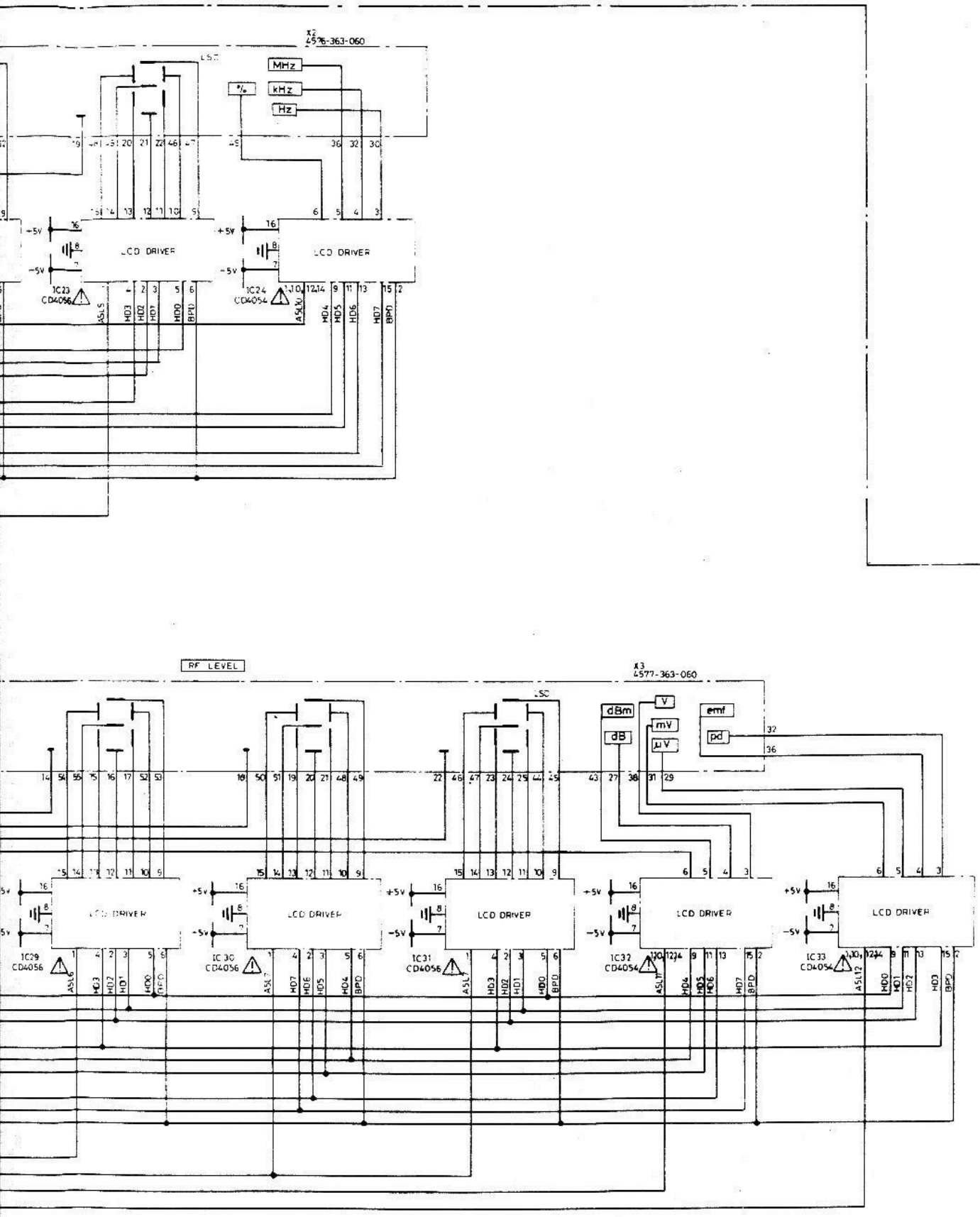
Display board, ADI (sheet 1)



Display board, AD1 (sheet 2)

Fig. 21

Sep. 81

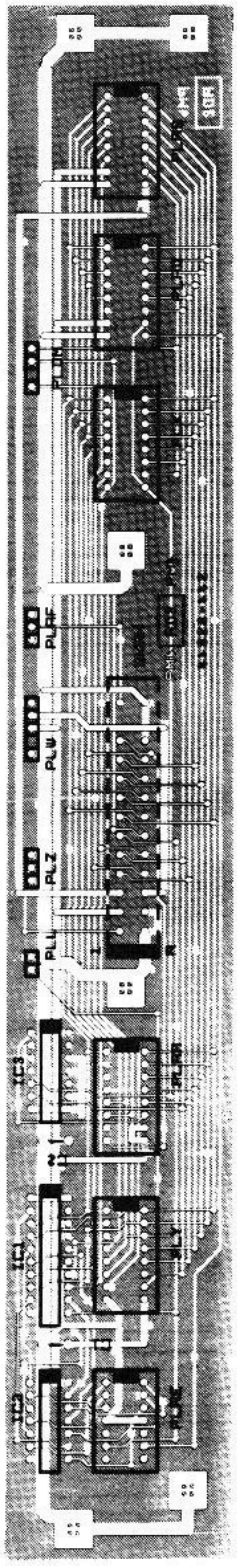


Z44828-441K Sh 2 of 2 Iss 4.

AD1

play board, AD1 (sheet 2)

Fig. 21
Chap. 7
Page 43



Component layout, AD2

Fig. 22a

Sep. 81

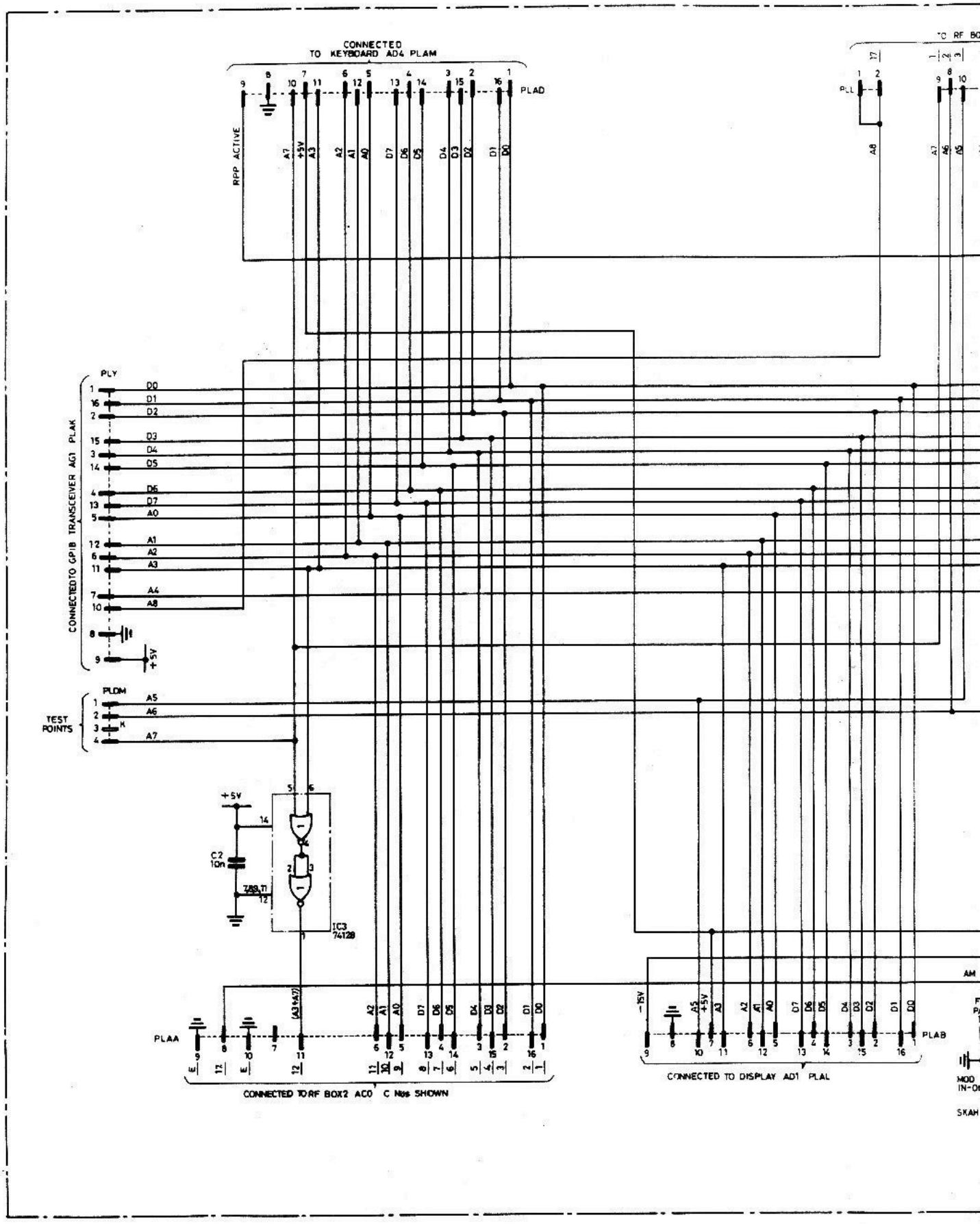
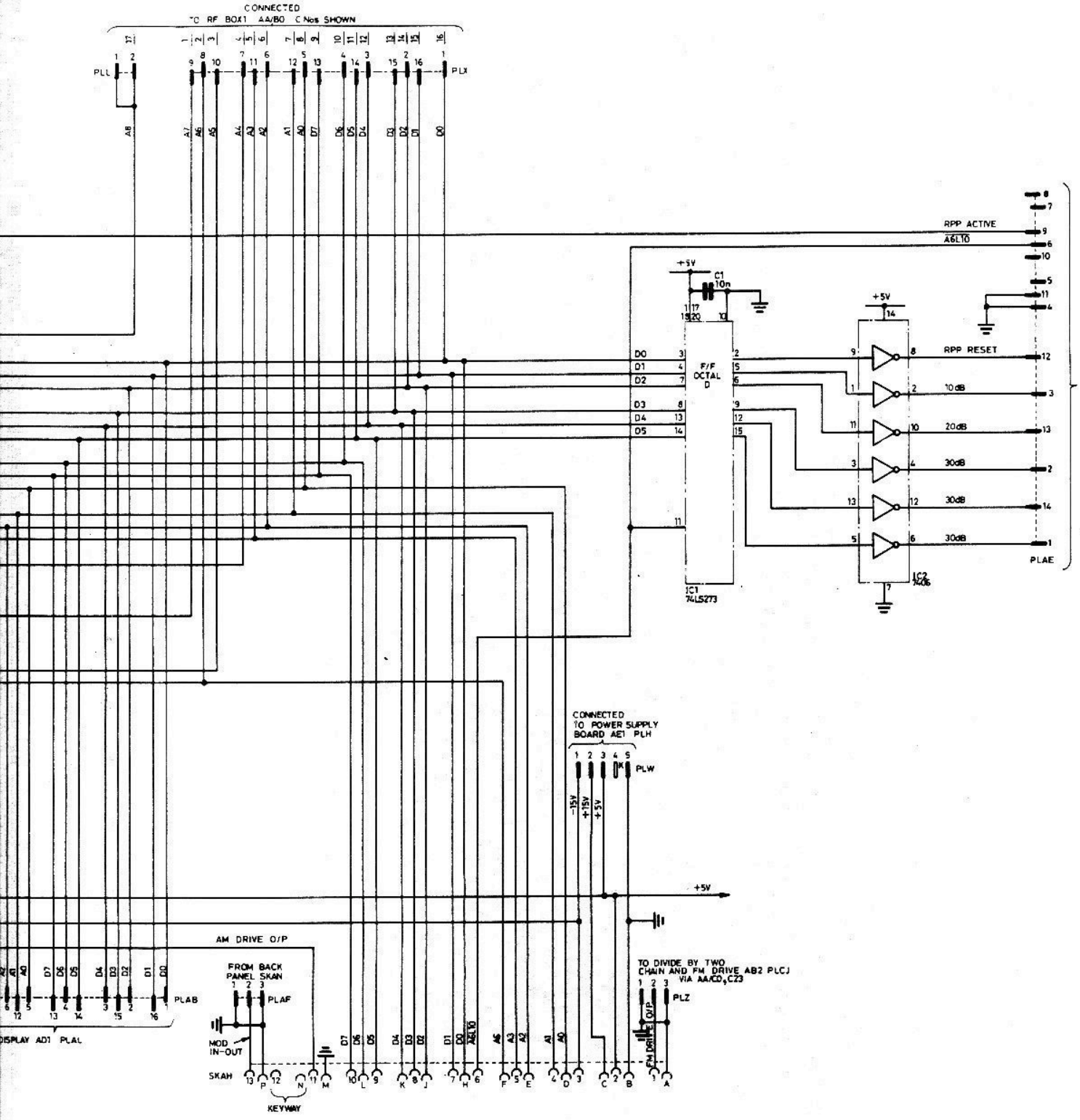


Fig. 22

Motherboar

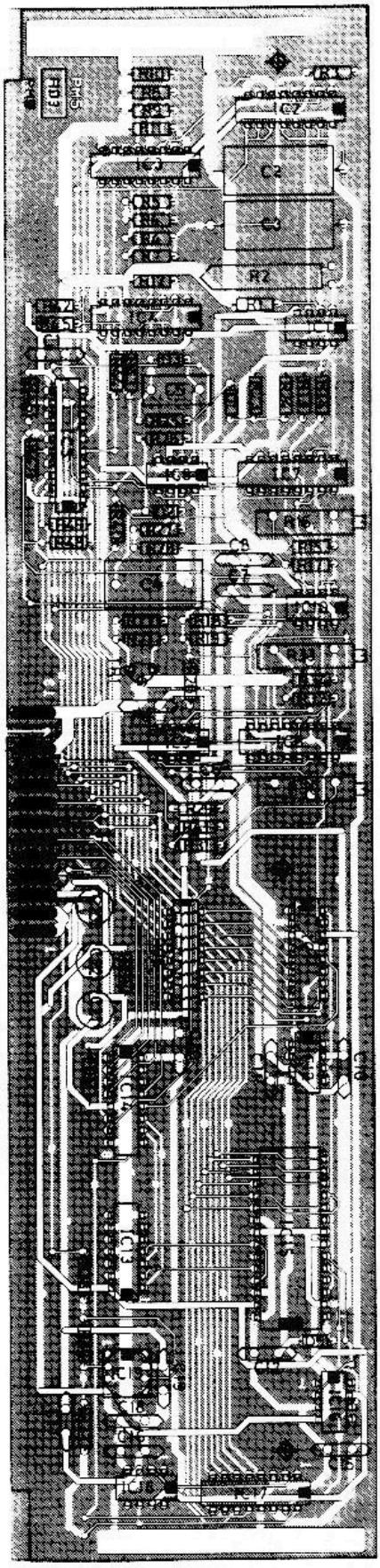
Sep. 81



AD2

Z 44828-442A Iss.6

Motherboard, AD2



Component layout, AD3

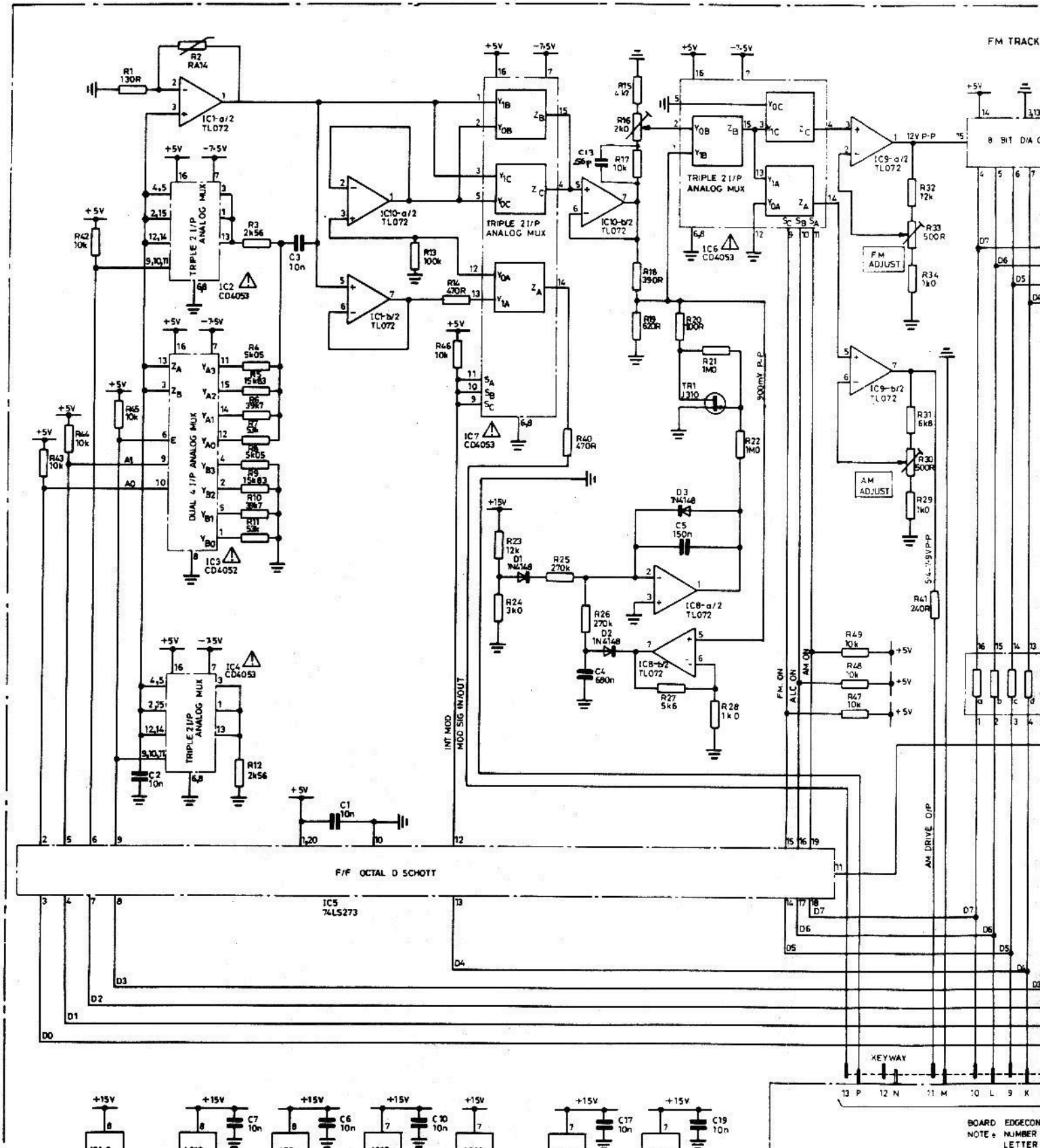
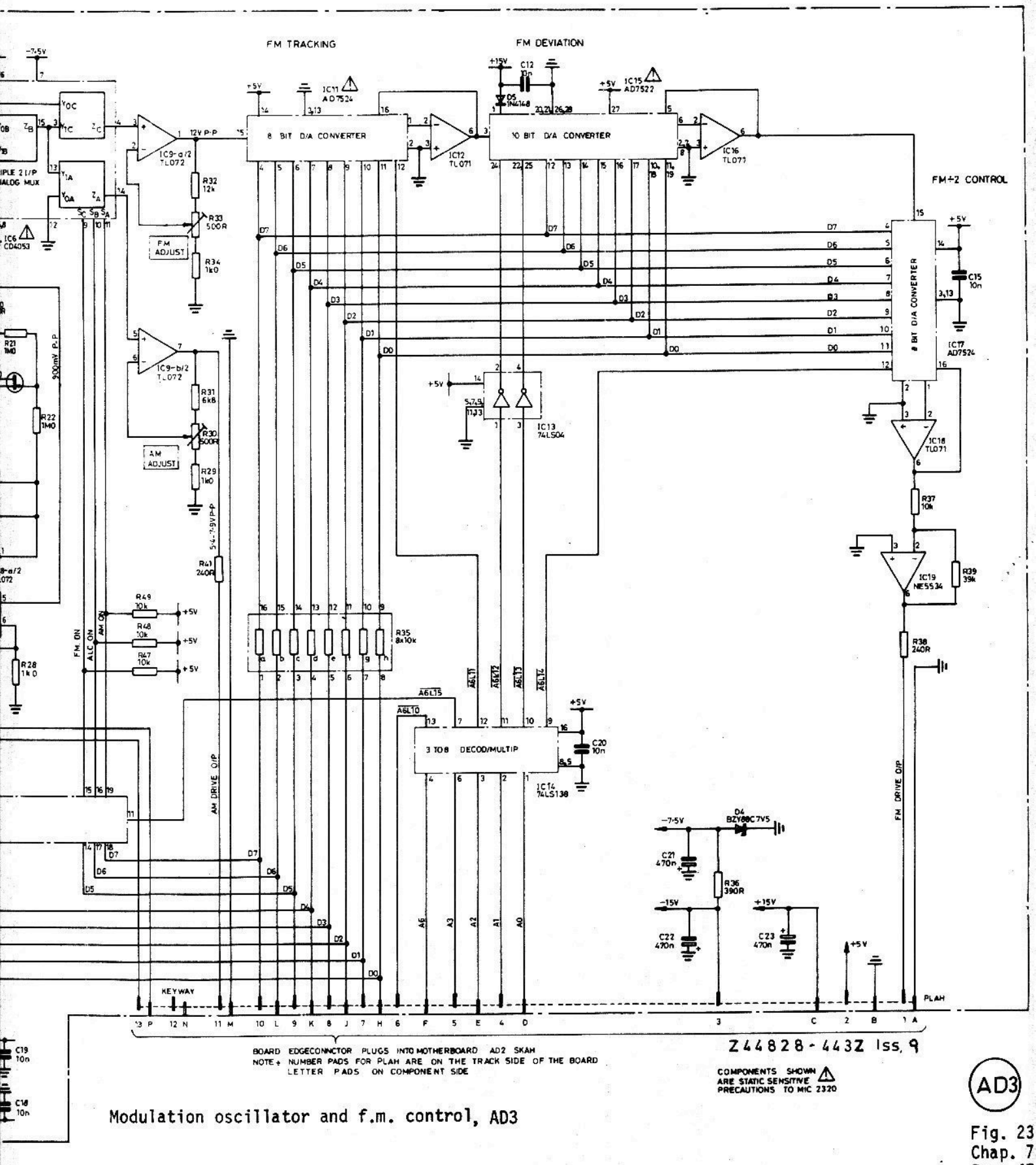
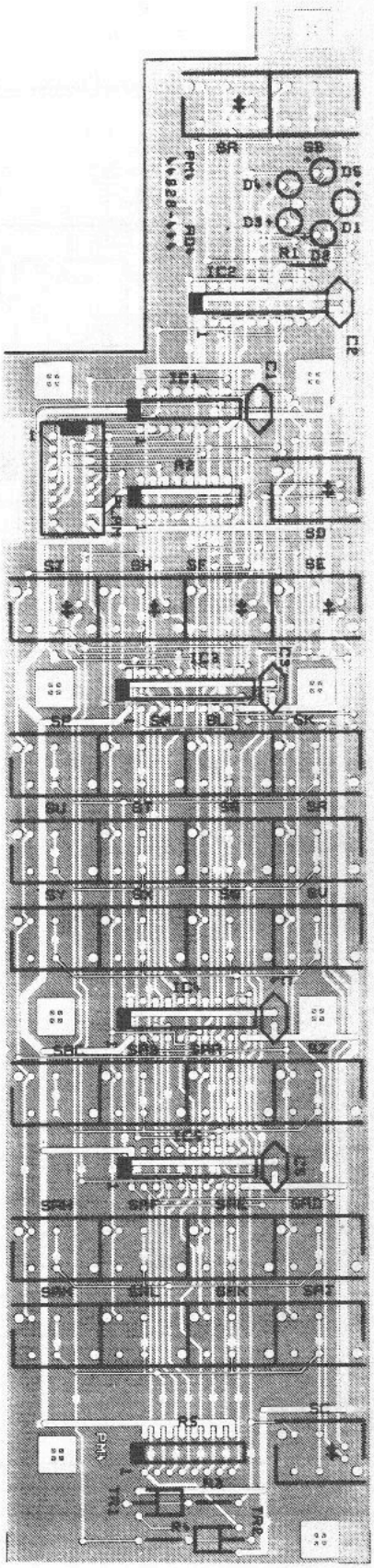

FM TRACK
R1 130R
R2 RA14
IC1-a/2 TL072
IC1-b/2 TL072
IC10-a/2 TL072
IC10-b/2 TL072
TRIPLE 2 I/P ANALOG MUX
IC2 CD4053
R3 2k56
C3 10n
R13 100k
R14 470R
R42 10k
R46 10k
IC7 CD4053
R40 470R
DUAL 4 I/P ANALOG MUX
IC3 CD4052
R4 5k05
R5 15k83
R6 3k87
R7 5k11
R8 5k05
R9 15k83
R10 3k87
R11 5k11
R43 10k
R44 10k
R45 10k
IC4 CD4053
C2 10n
R12 2k56
C1 10n
R15 4k7
R16 2k0
C13 56p
R17 10k
IC6 CD4053
R18 390R
R19 620R
R20 100R
R21 1M0
R22 1M0
TR1 J310
900mV P-P
D3 1N4148
C5 150n
R23 12k
D1 1N4148
R25 270k
R24 3k0
R26 270k
D2 1N4148
C4 680n
IC8-a/2 TL072
IC8-b/2 TL072
R27 5k6
R28 1k0
INT MOD
MOD SIG IN/OUT
IC9-a/2 TL072
IC9-b/2 TL072
12V P-P
R32 12k
R33 500R
FM ADJUST
R34 1k0
R31 6k8
R30 500R
AM ADJUST
R29 1k0
5.4-7.9V P-P
R41 240R
R49 10k
R48 10k
R47 10k
FM ON
AM ON
ALC ON
AM DRIVE O/P
8 BIT D/A C
F/F OCTAL D SCHOTT
IC5 74LS273
D0
D1
D2
D3
D4
D5
D6
D7
KEYWAY
13 P
12 N
11 M
10 L
9 K
BOARD EDGECON
NOTE : NUMBER
LETTER
IC1,8
IC10
IC9
IC12
IC16
IC18
IC19
C6 10n
C7 10n
C8 10n
C9 10n
C10 10n
C11 10n
C16 10n
C17 10n
C18 10n
C19 10n
+15V
-15V
Modulation oscillator a

Fig. 23

Sep. 81



Modulation oscillator and f.m. control, AD3



Component layout, AD4

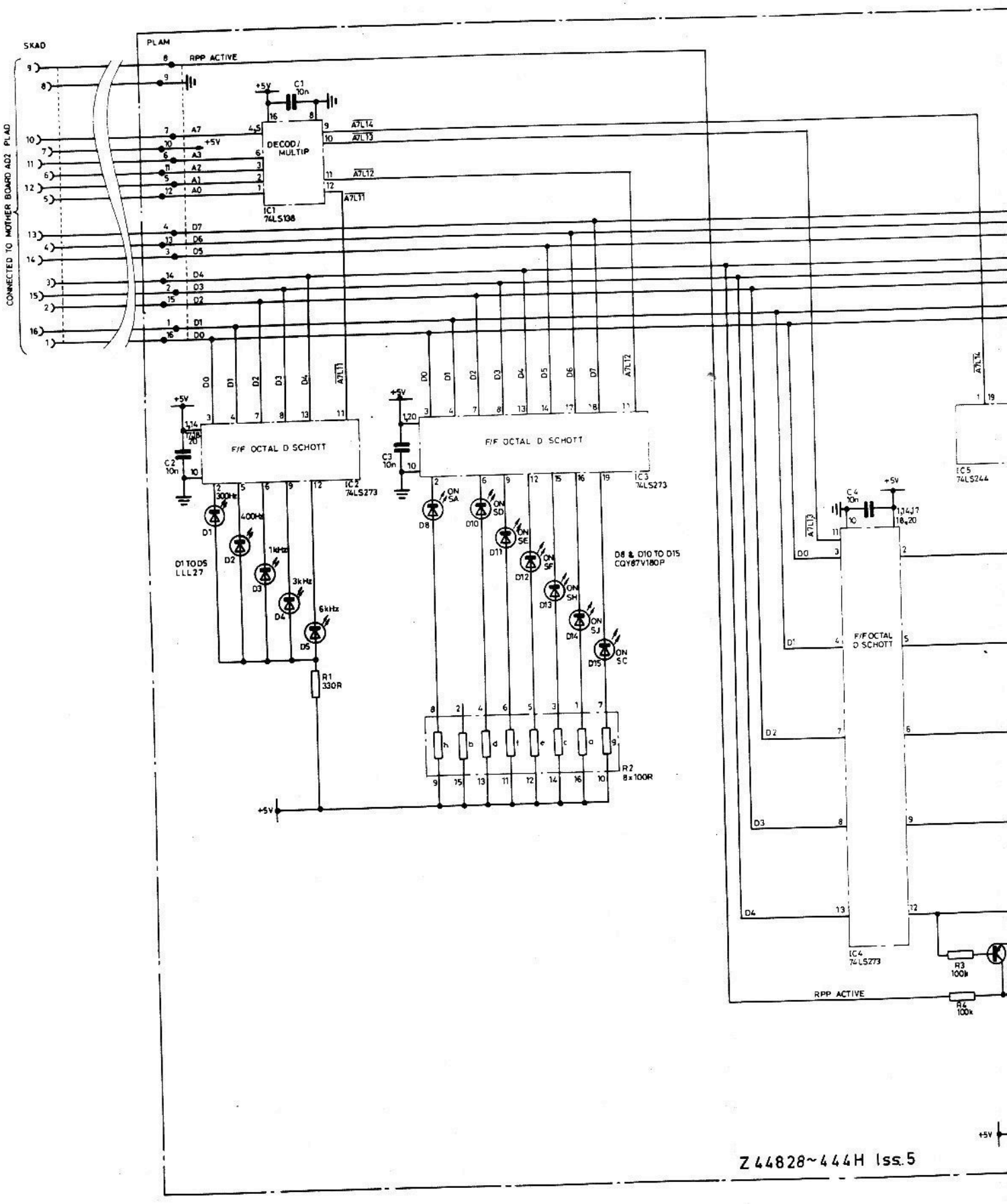
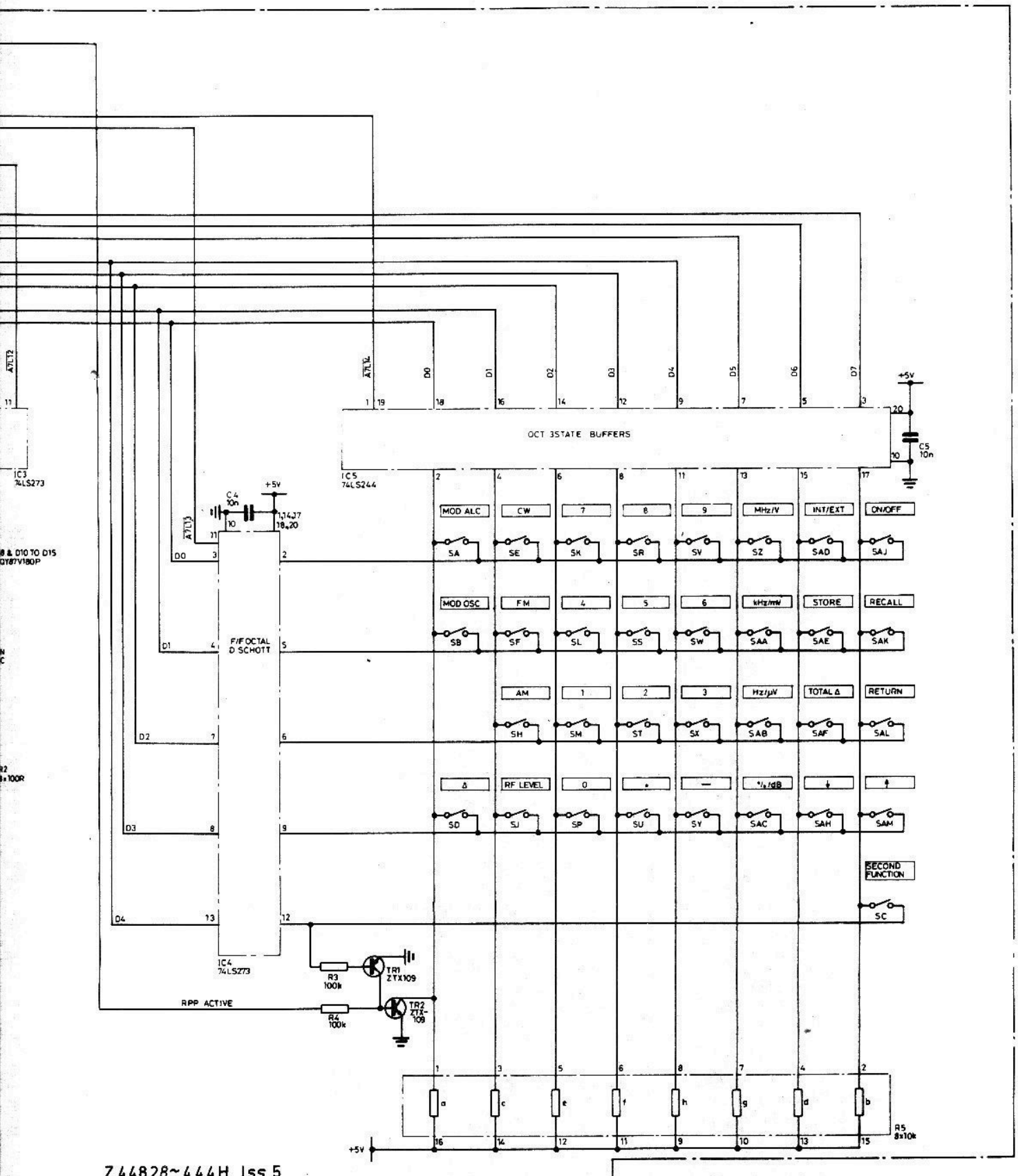

SKAD
CONNECTED TO MOTHER BOARD A02 PLAD
PLAM
RPP ACTIVE
+5V
C1 10n
DECOD/ MULTIP
IC1 74LS138
A7L14
A7L13
A7L12
A7L11
D7
D6
D5
D4
D3
D2
D1
D0
F/F OCTAL D SCHOTT
IC2 74LS273
IC3 74LS273
C2 10n
C3 10n
D1 TO D5 LLL27
300Hz
400Hz
1kHz
3kHz
6kHz
D8 & D10 TO D15 CQY87V180P
R1 330R
R2 8x100R
IC4 74LS273
IC5 74LS244
C4 10n
R3 100k
R4 100k
Z 44828~444H Iss.5

Fig. 24

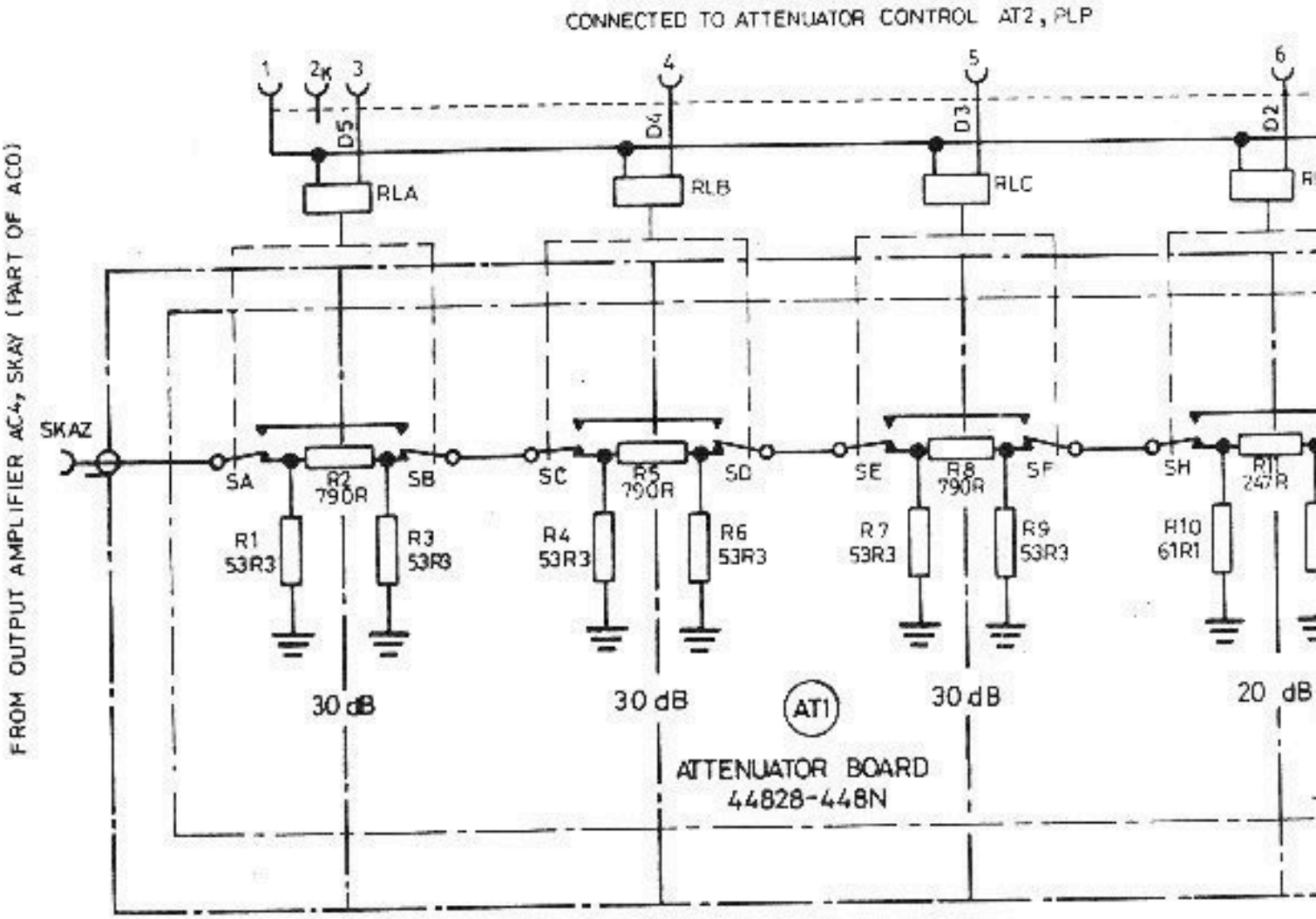
Sep. 81



Z44828~444H Iss.5

Keyboard, AD4

AD4

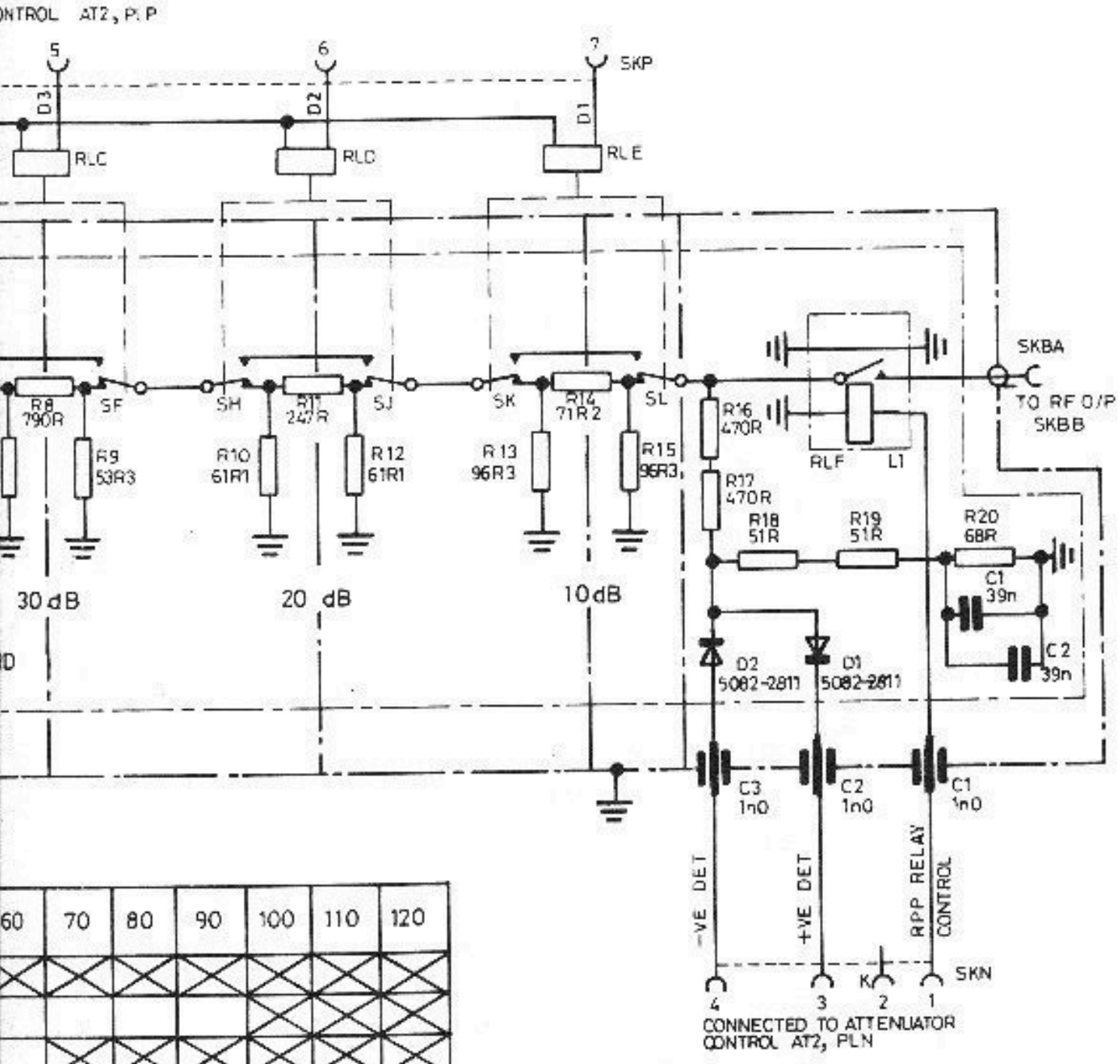


dB ATTENUATION			0	10	20	30	40	50	60	70	80	90	100	110
PADS IN CIRCUIT	A	30dB					X	X	X	X	X	X	X	X
	B	30dB											X	X
	C	30dB								X	X	X	X	X
	D	20dB			X	X		X	X		X	X		X
	E	10dB		X		X	X		X	X		X	X	

10 dB step attenuator, AT0

Fig. 25

Sep. 81

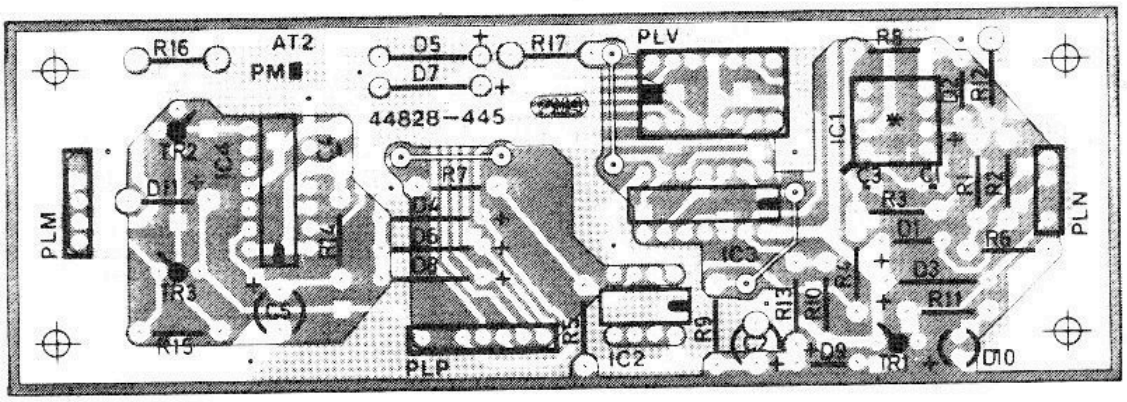


INCLUDES AT1

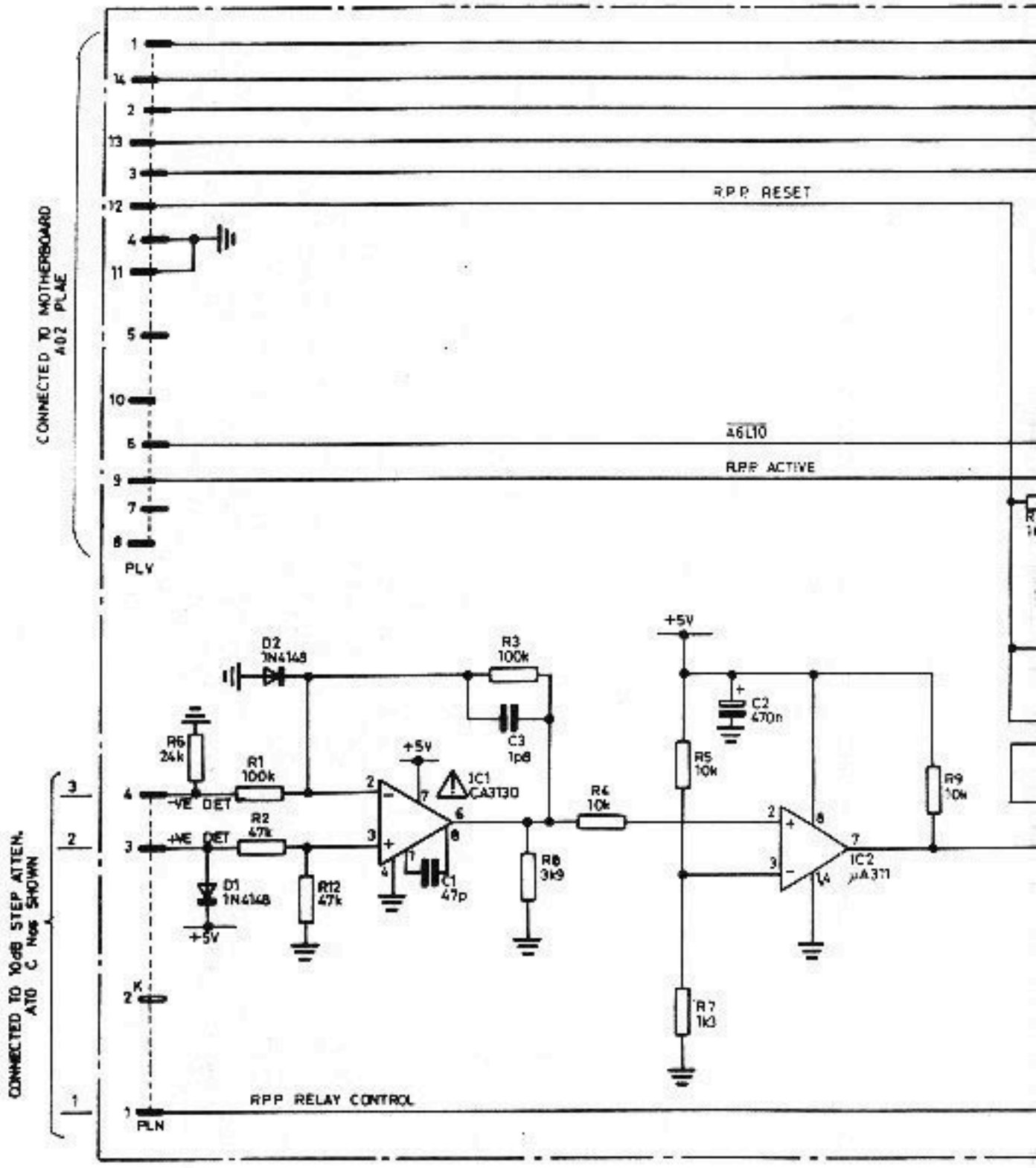
Z 44 990-353W Iss. 4

AT0

10 dB step attenuator, AT0



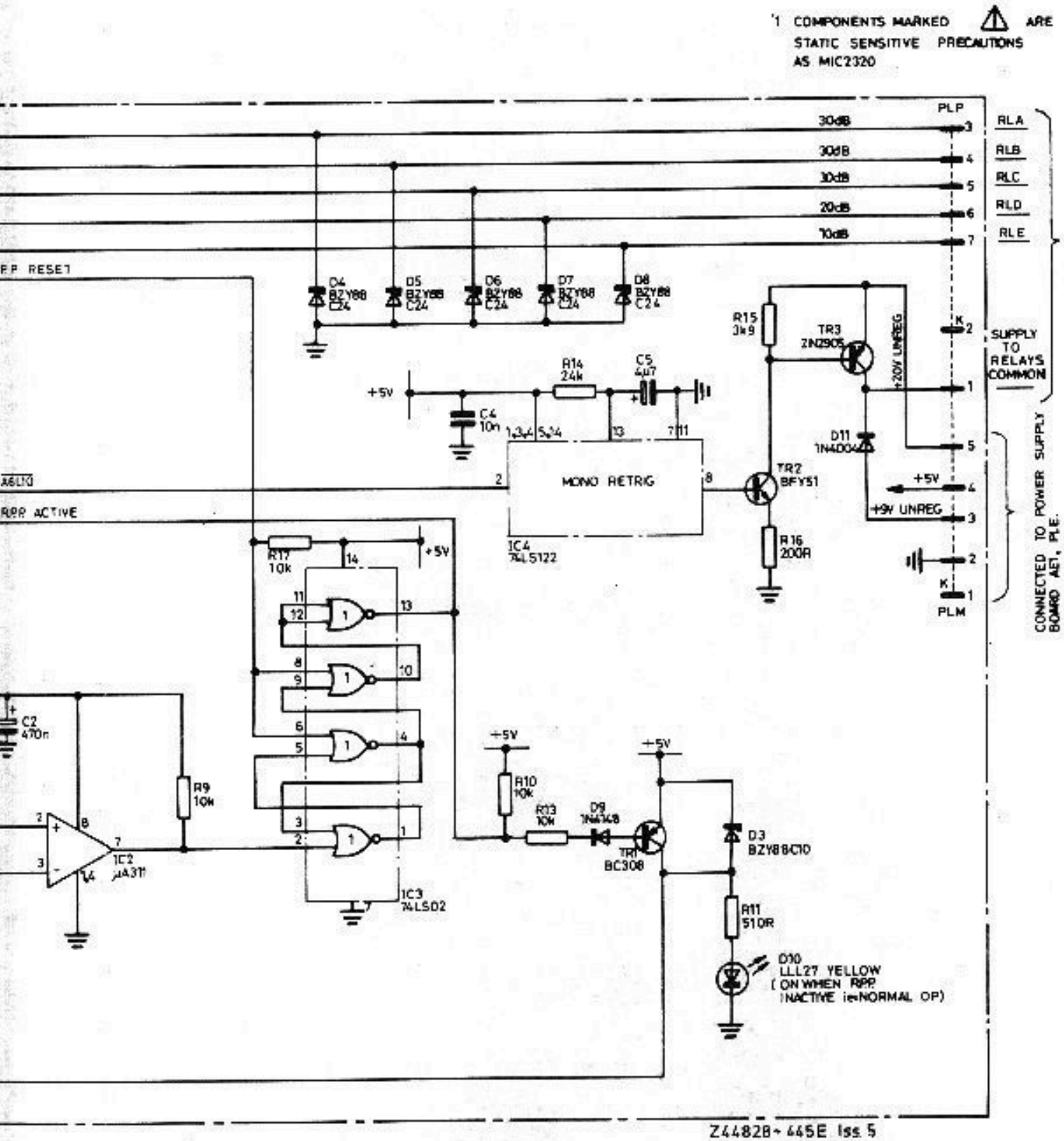
Component layout, AT2



Attenuator contro

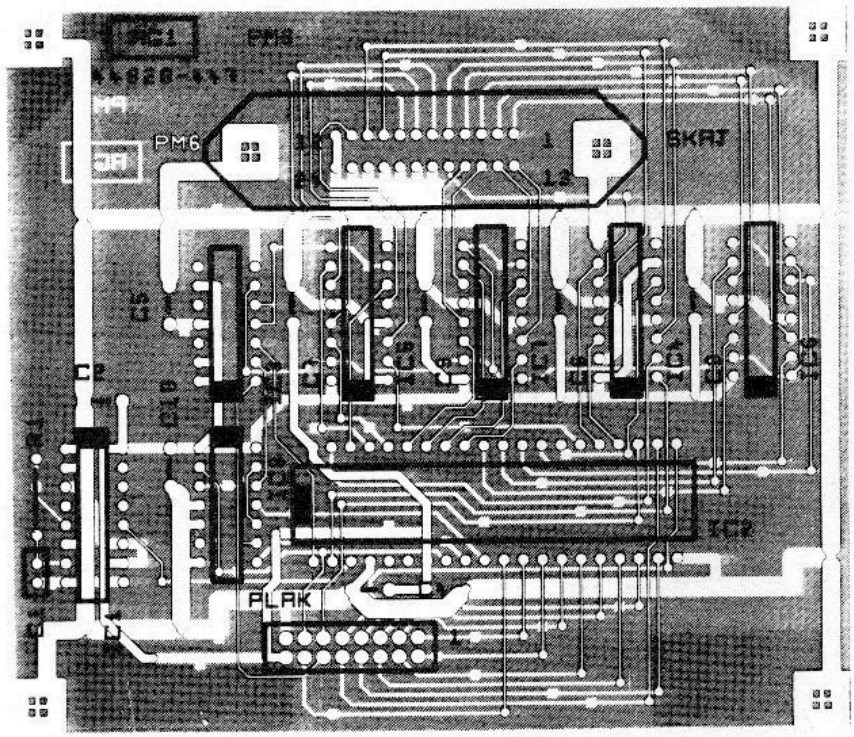
Fig. 26

Sep. 81



Attenuator control, AT2

AT2



Component layout, AGO

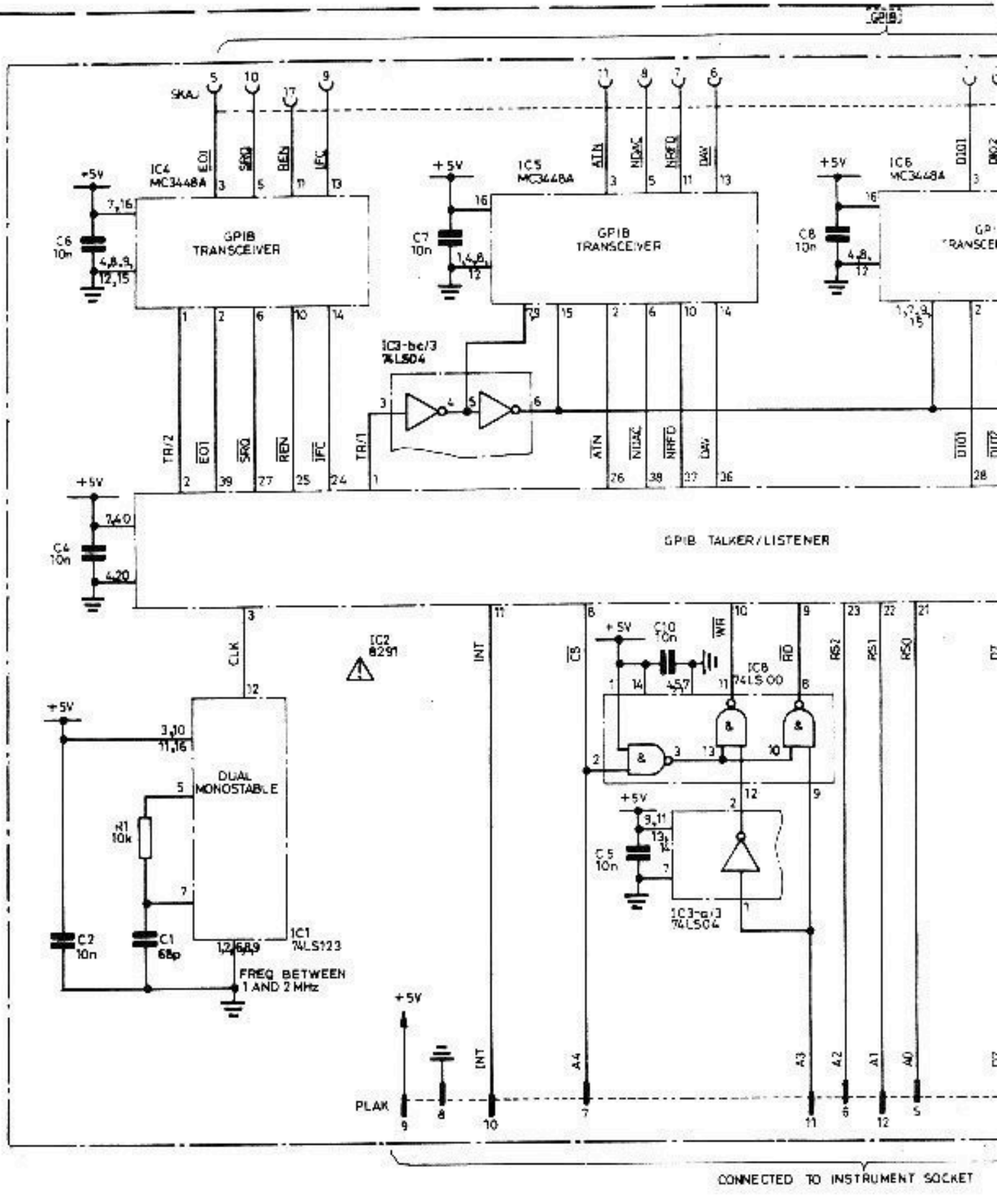
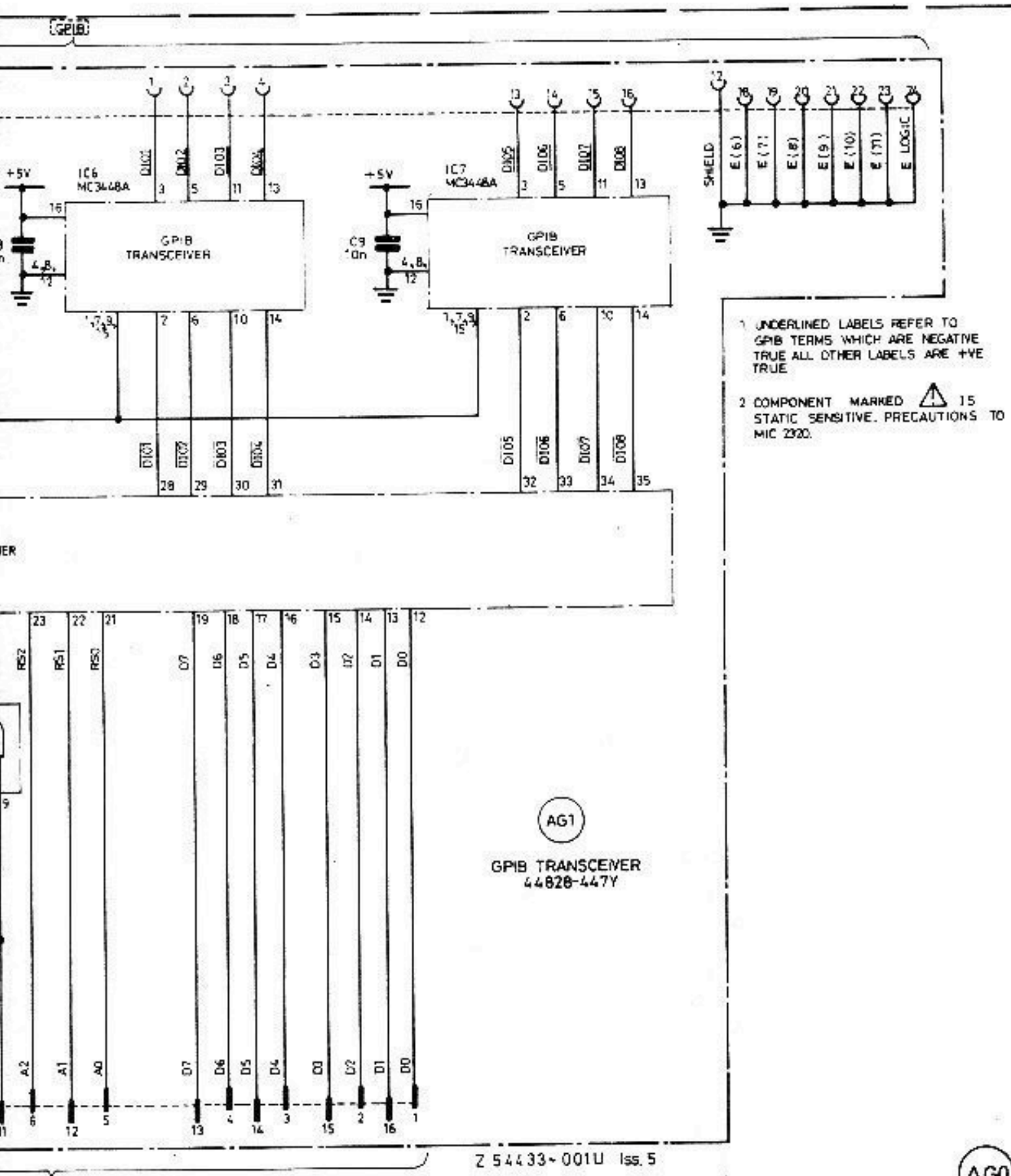


Fig. 27

GPIB adapter module, AG0

Sep. 81



apter module, AG0

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A GEC-Marconi Electronics Company

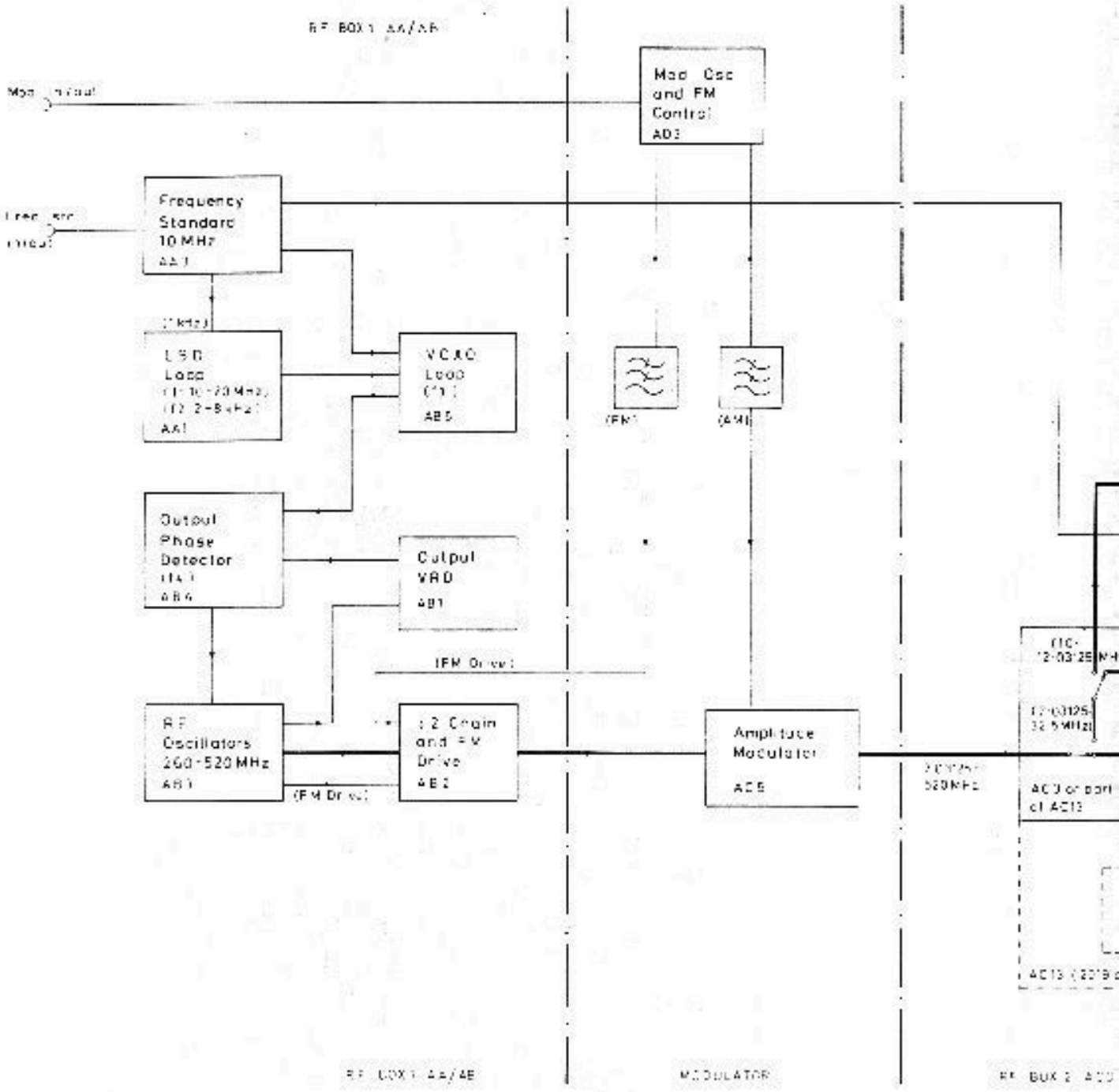


Fig. 1 Simplified block diagram of 2019/2019 frequency s
signal processing

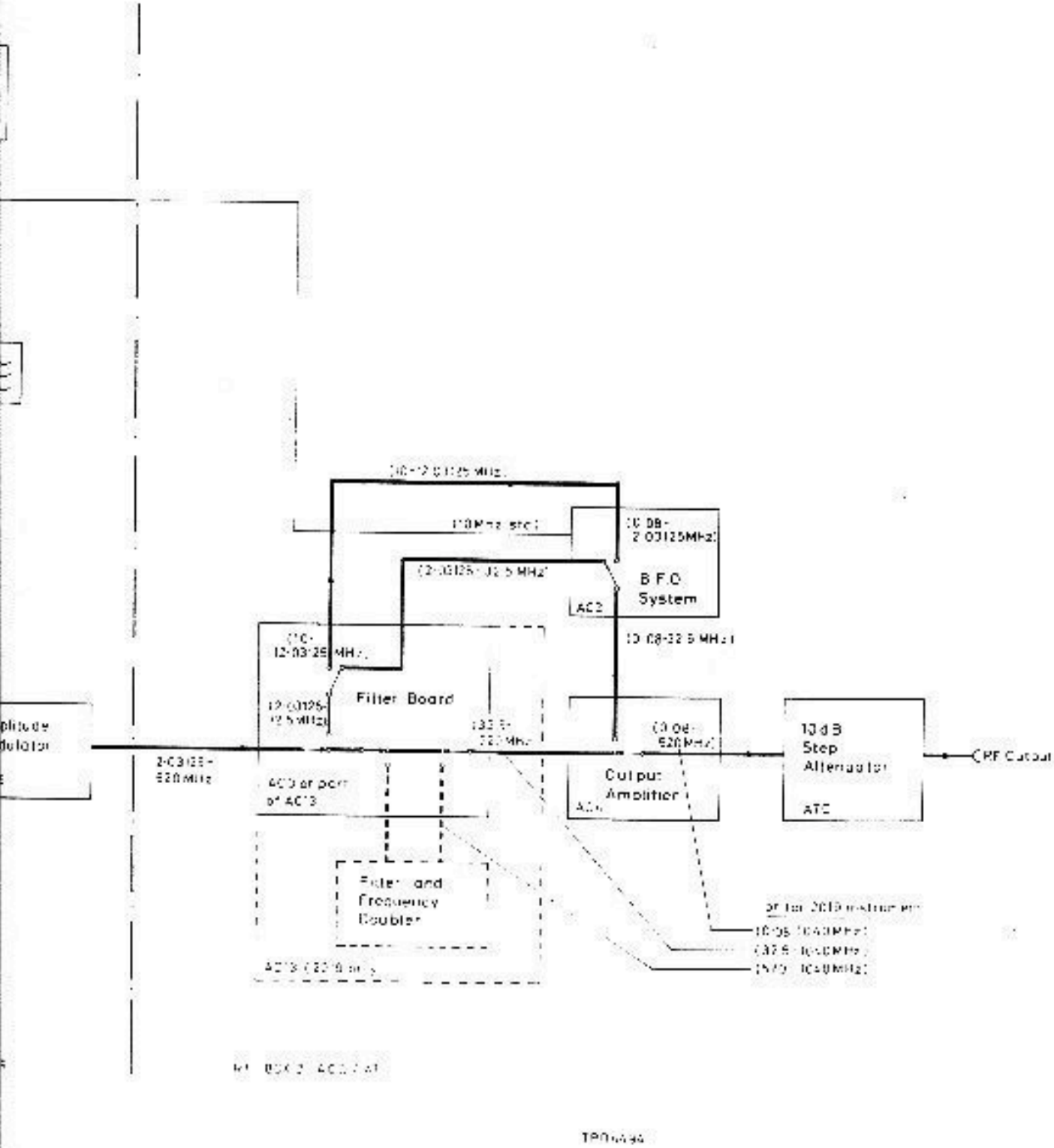


Diagram of 2013/2019 frequency synthesis and signal processing

Digital control system

Circuit diagram : Chap. 7, Fig. 3

9. The internal data bus consists of a total of 17 control lines. The first eight lines D0 to D7, are data lines. The data bus is bi-directional e.g. data may be input into the microprocessor via the front panel keyboard or control data can be sent to the data latches from the microprocessor.

10. The next four lines A0 to A3, are address lines. These are used to control the address of the latch to which the data is to be sent or from which data is being read.

11. The following four lines A4 to A7 are data valid lines. A0 to A3 lines are fed to address decoders and with it one of the data valid lines A4, A5, A6 or A7 is connected to each address decoder. Only when this line is activated '0' low is the decoder enabled, and its decoded output then activates the required data latch.

12. The last control line A8 is the GPIB interrupt line. This line calls for the microprocessor to service the GPIB module.

13. Bus interconnections are shown in Chap. 7, Fig. 5 Servicing diagrams. The microprocessor AA2 serves as the motherboard in the top r.f. box. Some of the data is latched on AA2 in order to minimize the number of interconnections. The addresses of the other latches are also decoded on AA2 to minimize interconnections. The entire 17 line data bus is connected to AD2 motherboard via an r.f. filter box. The filter box ensures that r.f. signals are not conducted down the data bus. From the motherboard the data bus is distributed to the boards outside the top r.f. box. A further connection is made to the lower r.f. box containing AC2, AC3, AC4 and AC5 via a second filter box.

Frequency sunthesizer and signal processing

Circuit diagram : Chap. 7, Fig. 1

14. The frequency synthesizer provides a scable frequency source at the output of AB3 RF oscillators board covering the frequency range 260 MHz to 520 MHz that is phase locked to the internal frequency standard, board AA3 with a resolution of 10 Hz. As an aid to deriving the frequency at any point in the synthesizer the output frequency from AB3 is considered to be of the form

$$fo = m \times 100000 + n \times 10$$

where m is between 2600 and 5200
n is between 0000 and 9999

If an output frequency of 512.34567 MHz is selected then m = 5123 and n = 4567. and the output

$$fo = \frac{2\ (m-1)}{200} \left[10^7 + \frac{(10^4 + n)\ 10^3}{m-1} \right]$$

Intermediate frequencies at significant points within the synthesizer are given as f1, f2, f3 and f4 and are shown on the simplified block diagram Chap. 7, Fig. 1. Each frequency can be determined by applying one of the following formulae :

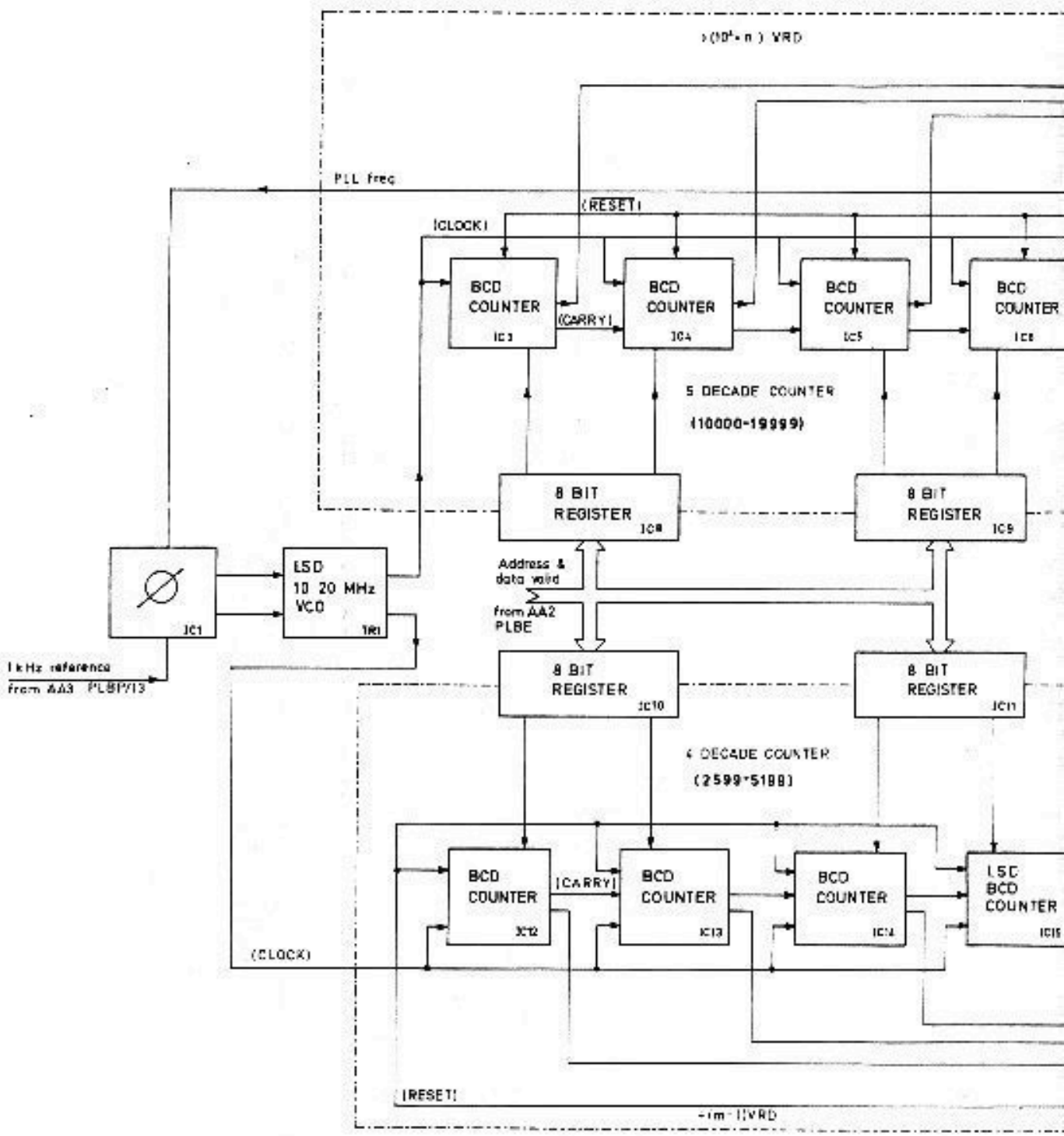
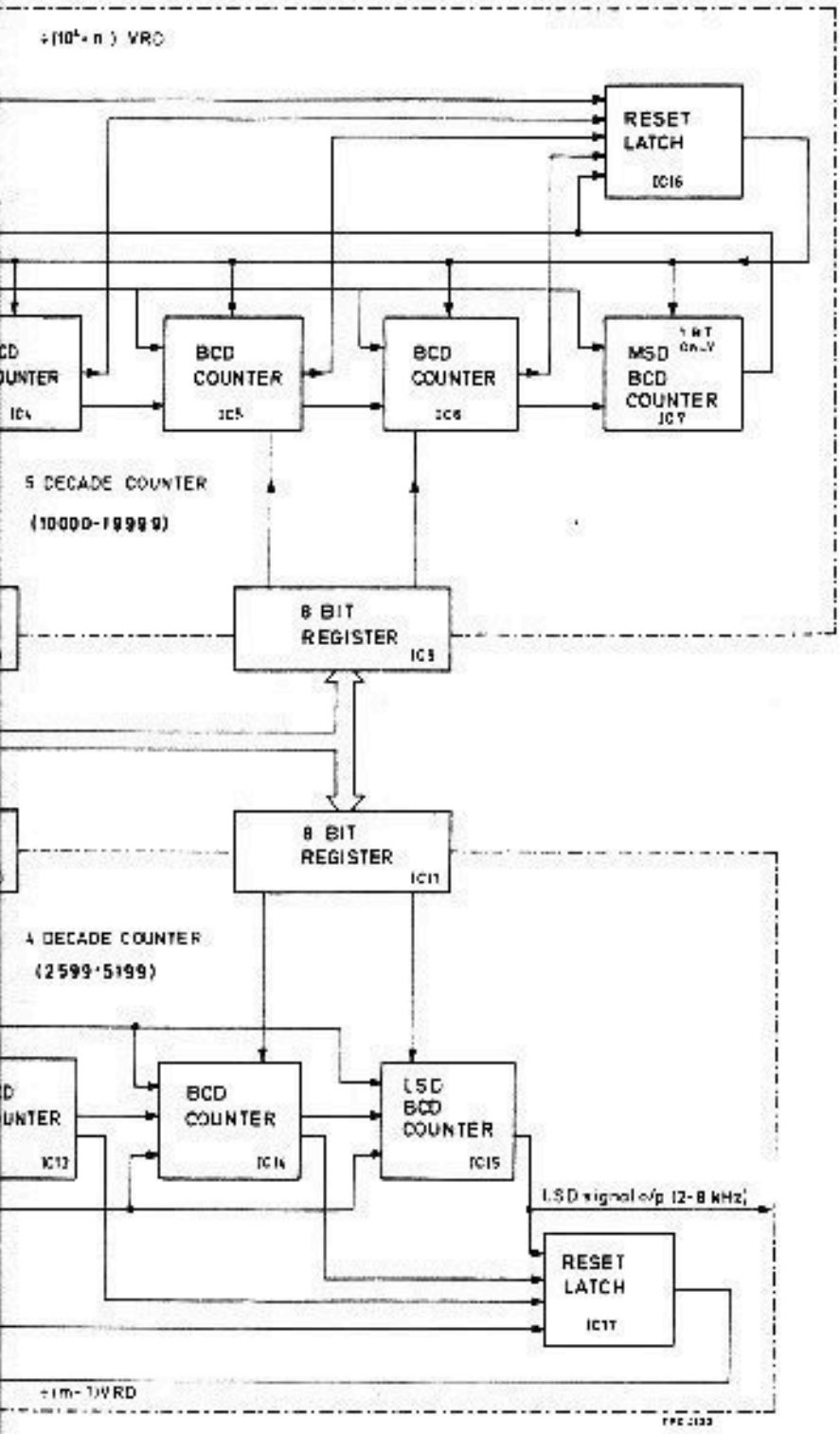


Fig. 2 LSD loop (AA1)



g. 2 LSD loop (AAI)

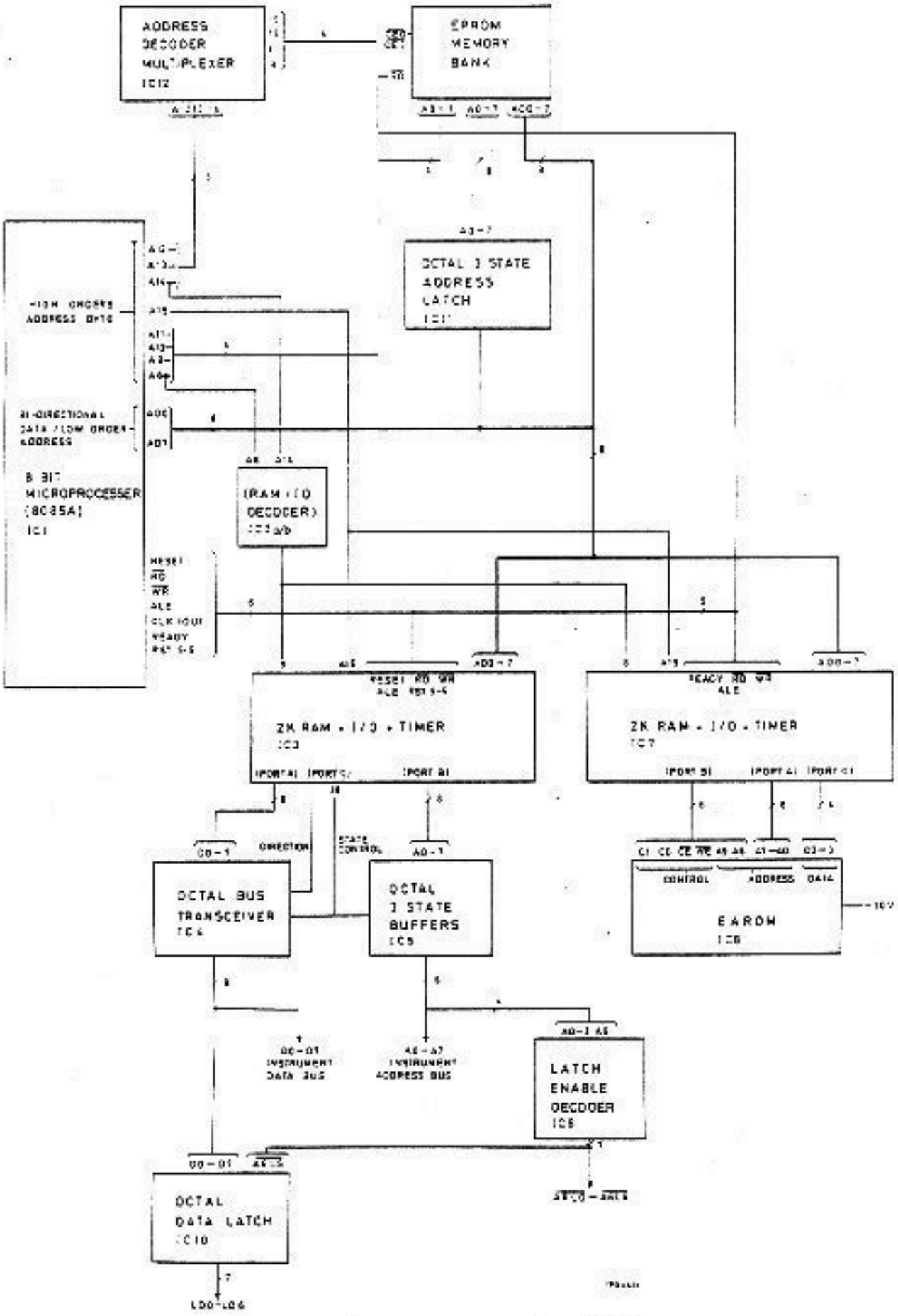


Fig. 3 Microprocessor system (AA2)

(AA3) - Frequency standard

Circuit diagram : Chap. 7, Fig. 8

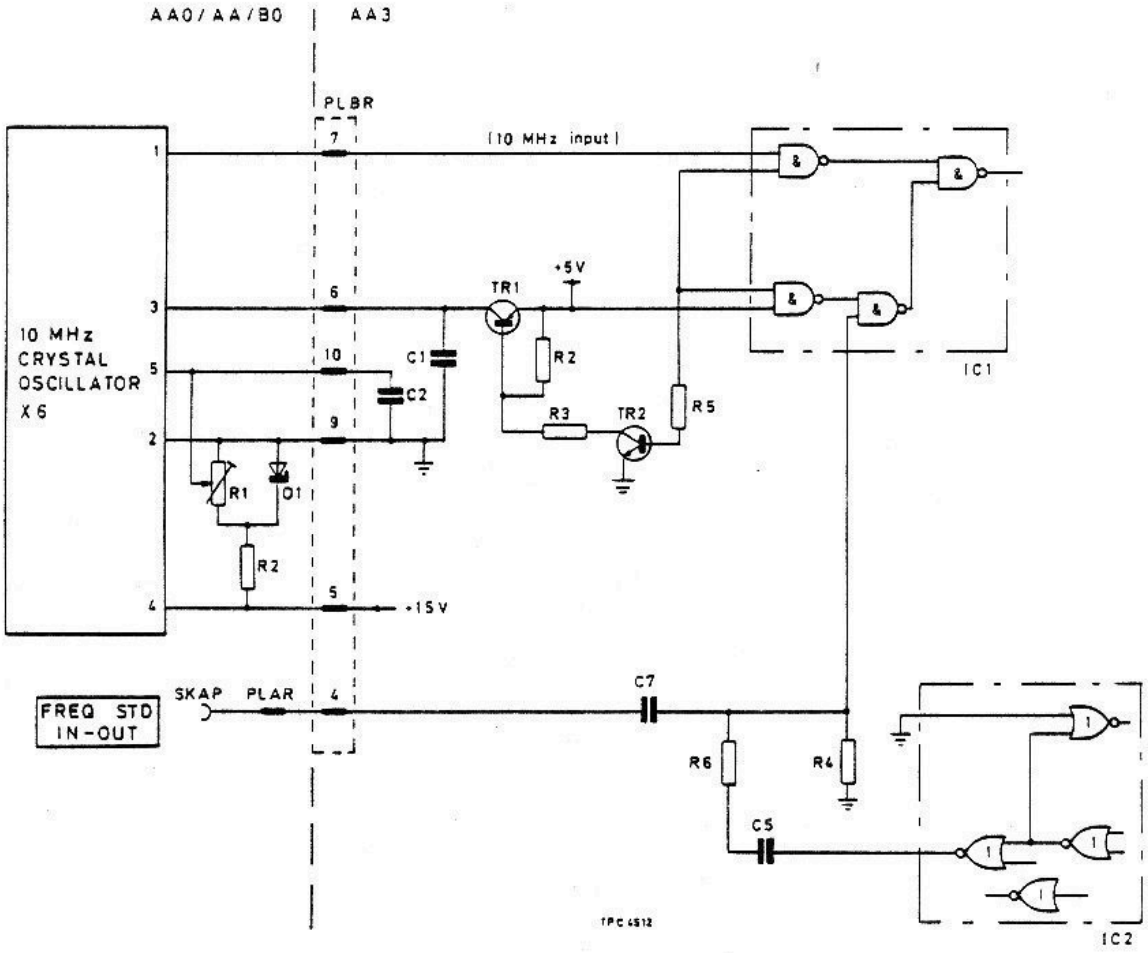


Fig. 4 Internal/external frequency standard (AA3)

43. The purpose of board AA3 is to select the required frequency standard and to distribute the necessary reference frequencies derived from the standard throughout the instrument. Control data is brought on two lines from a latch on the microprocessor AA2, via feedthrough capacitors and PLBP pins 5 and 10. If the INT/$\overline{\text{EXT}}$ STD line is high, the voltage supply to the temperature controlled crystal oscillator is turned on and its 10 MHz output frequency appears on PLBR pin 7.

44. The potentiometer AA0,R1 provides the means of trimming the crystal oscillator frequency. The oven supply is permanently on and is drawn from PLBR, pin 5. The logic gates are enabled so that the 10 MHz signal appears on IC1 pin 3. The output of IC1 is fed to the VCXO loop, AB5, via TR3, and also to the rear panel via PLBR, pin 4. The output to the VCXO loop is nominally a sine wave, the square wave drive being filtered by the tuned circuit L1 and C9. The 10 MHz standard is also divided down to 1 kHz by ÷100 dividers IC3, IC4 and then routed to the LSD loop via PLBP pin 13.

45. If the INT/$\overline{\text{EXT}}$ line is low the internal crystal oscillator is switched off and PLBR, pin 4 is used to input the external frequency standard from the rear panel socket.

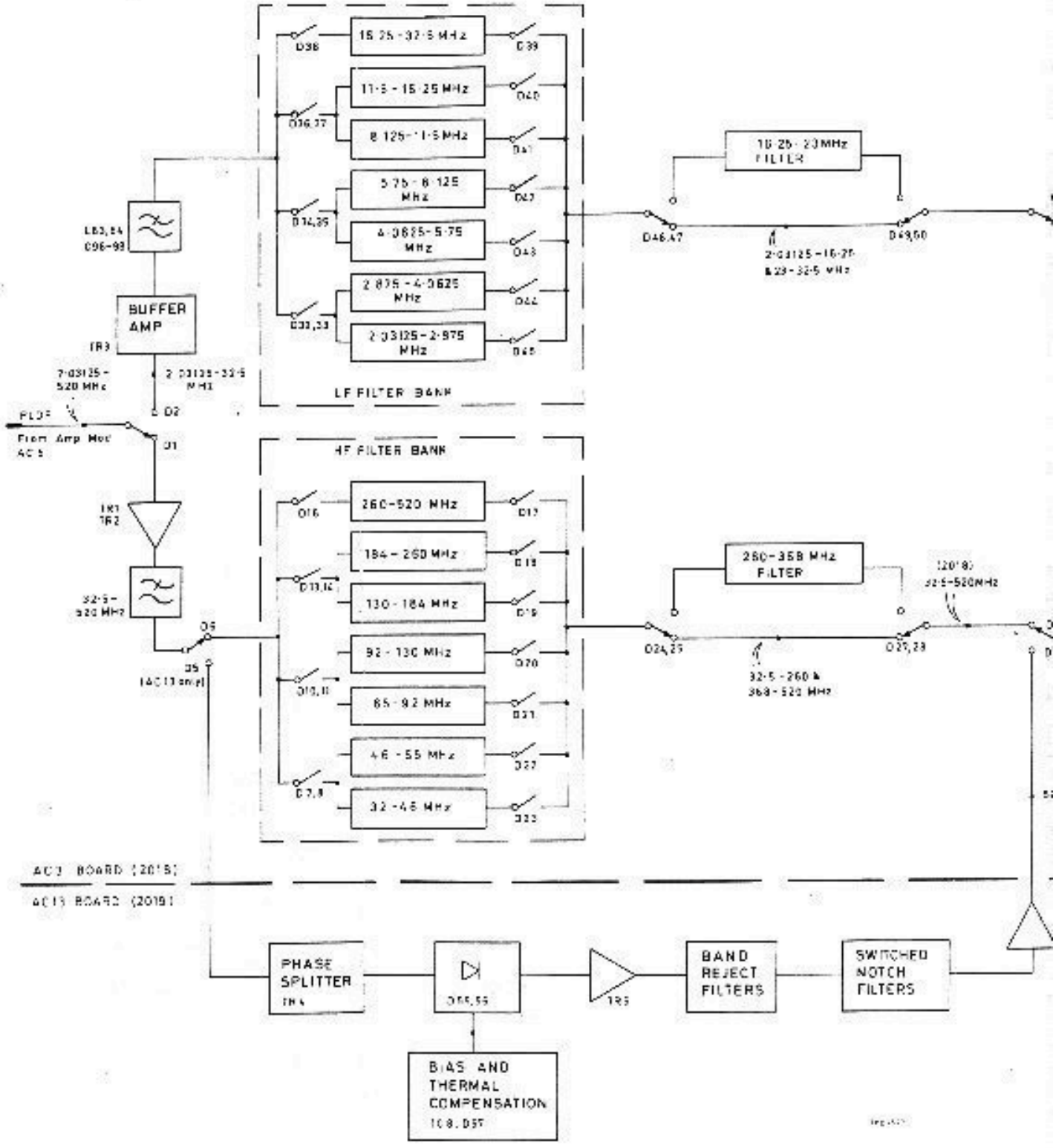
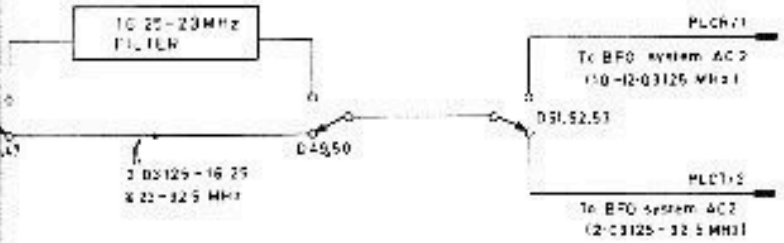
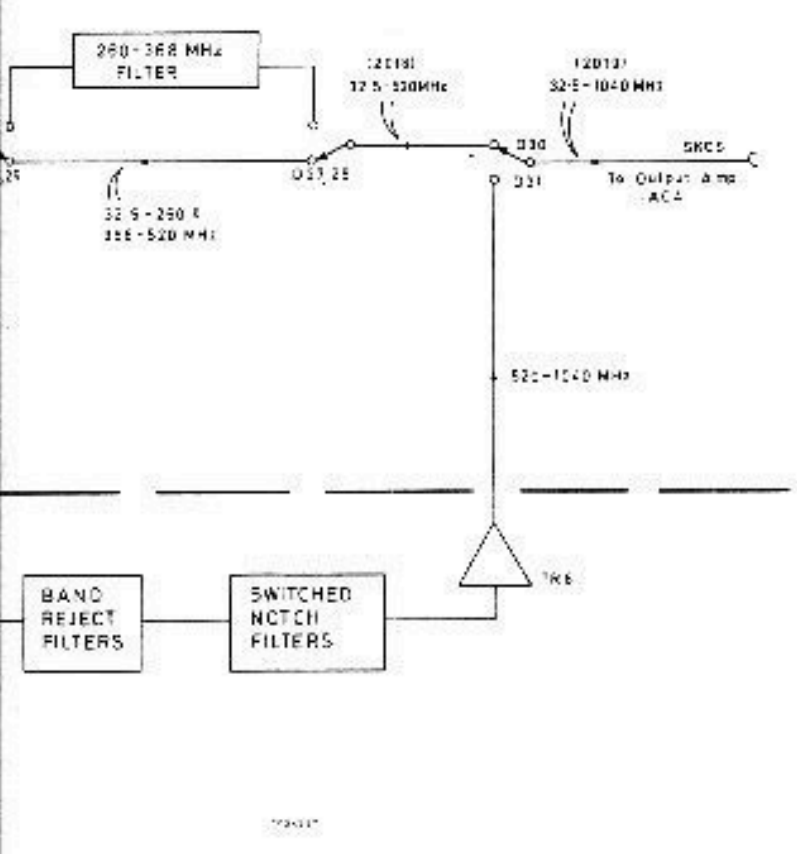


Fig. 11 Filter and frequency doubler board (AC3/AC13)





er board (AC3/AC13)

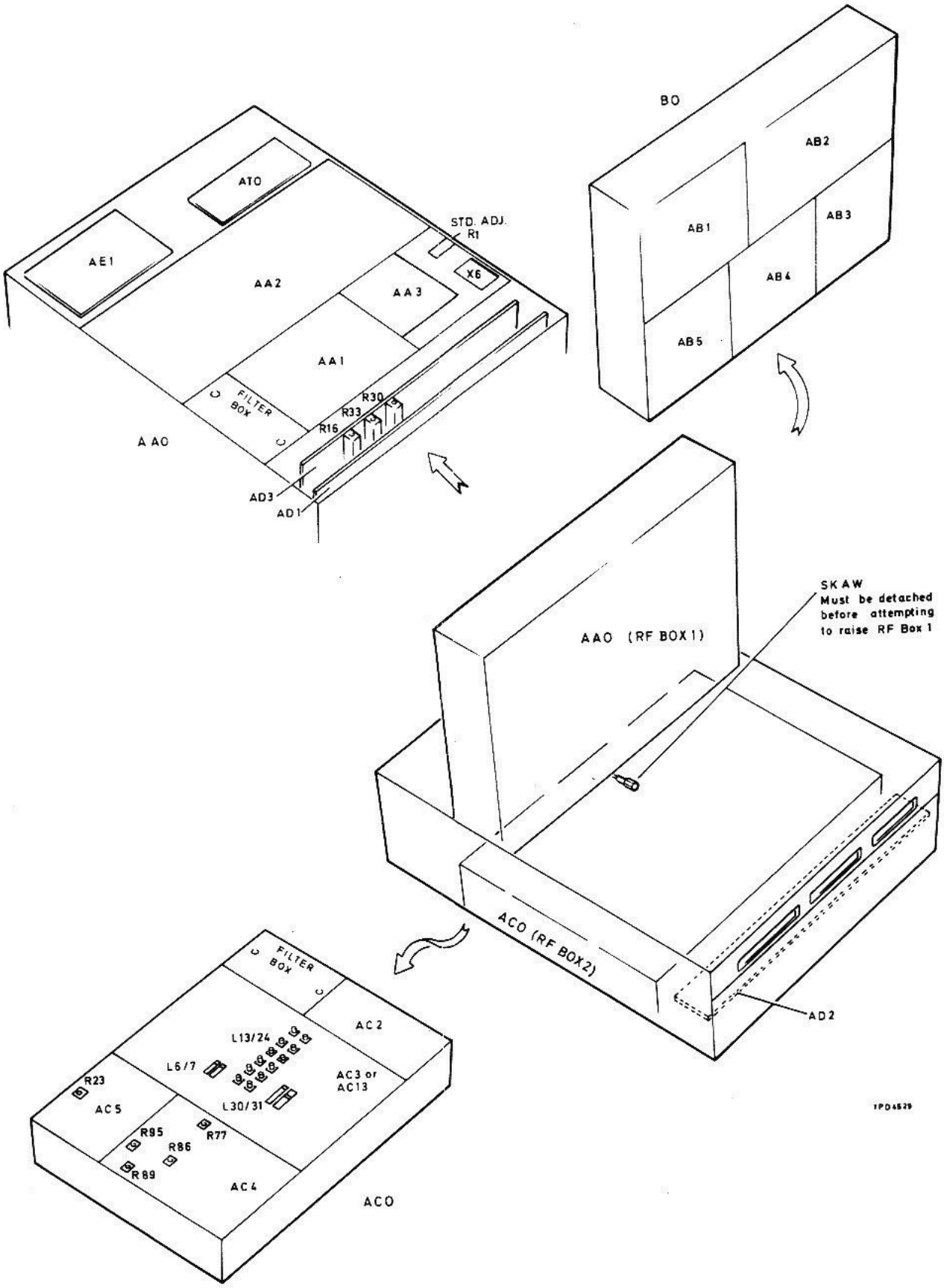


Fig. 1a Board location, access and pre-set adjustments

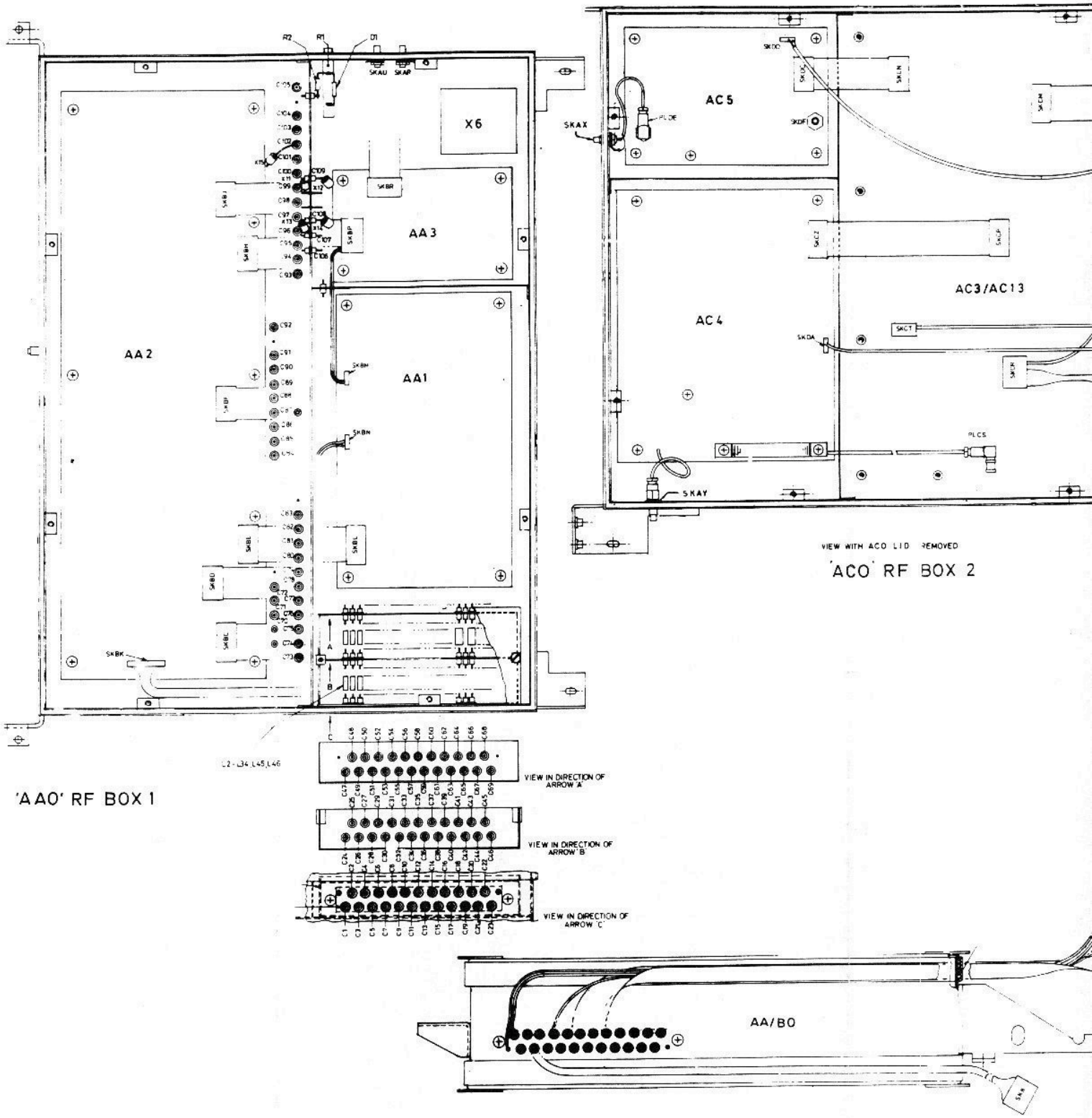
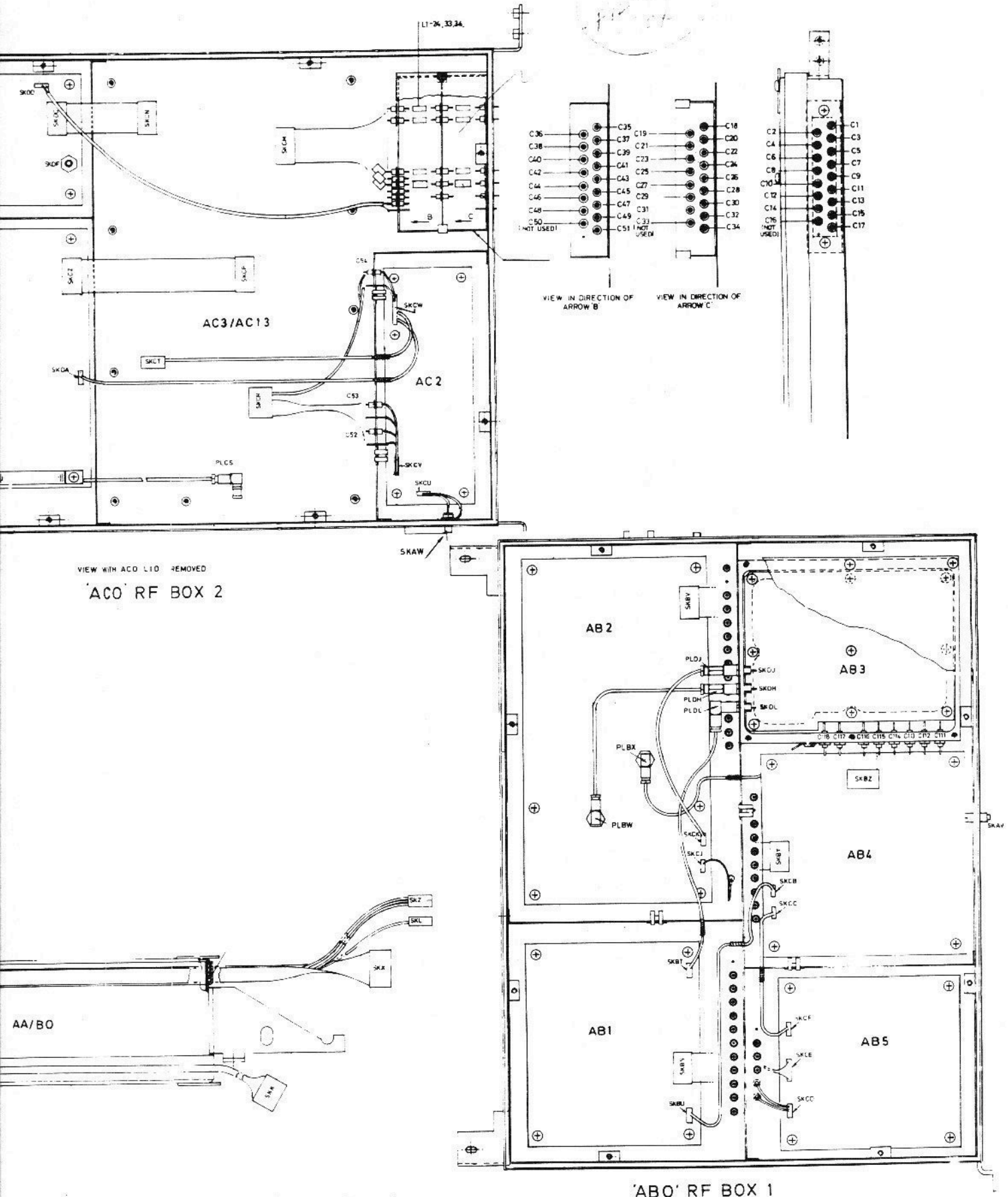
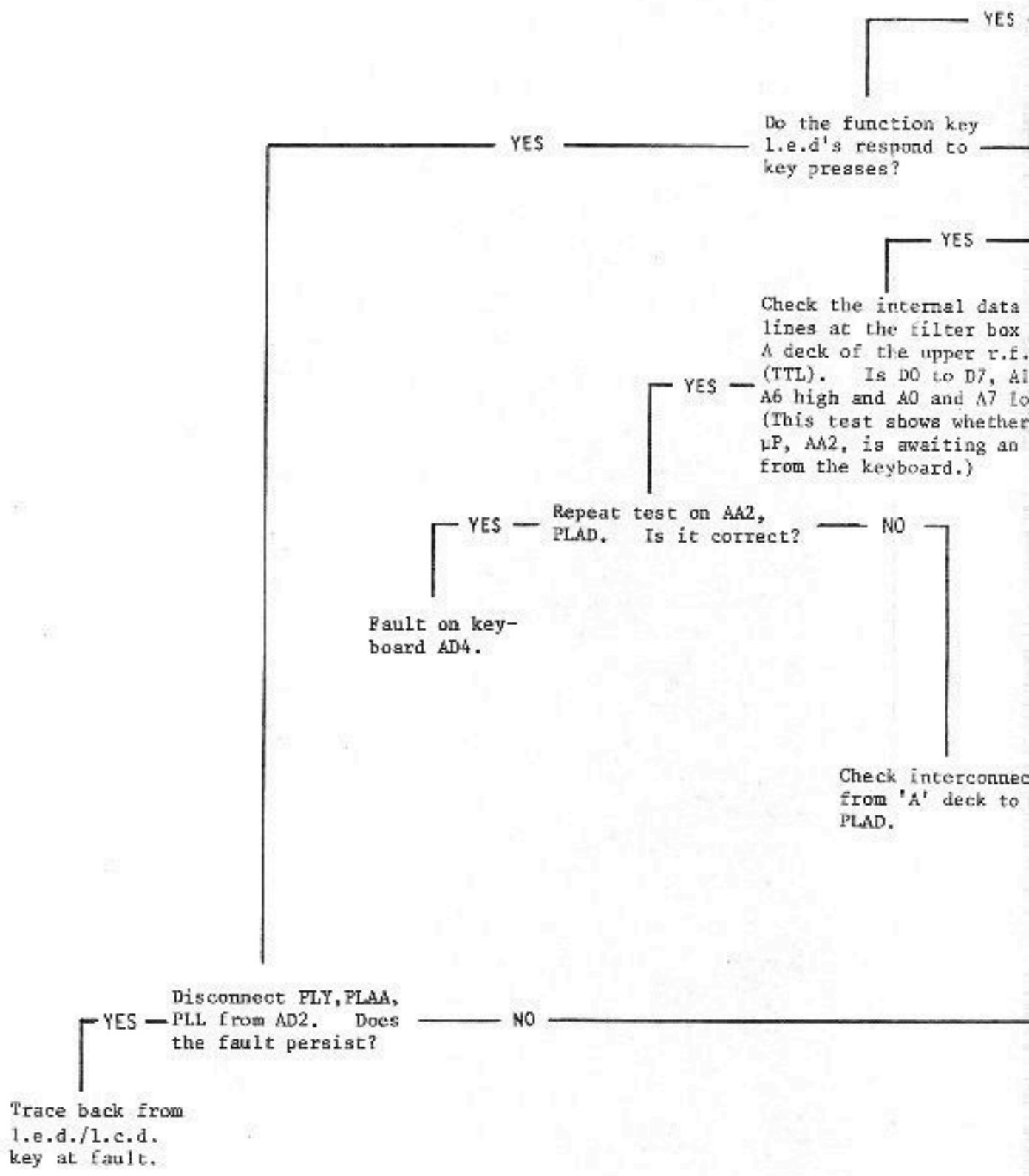


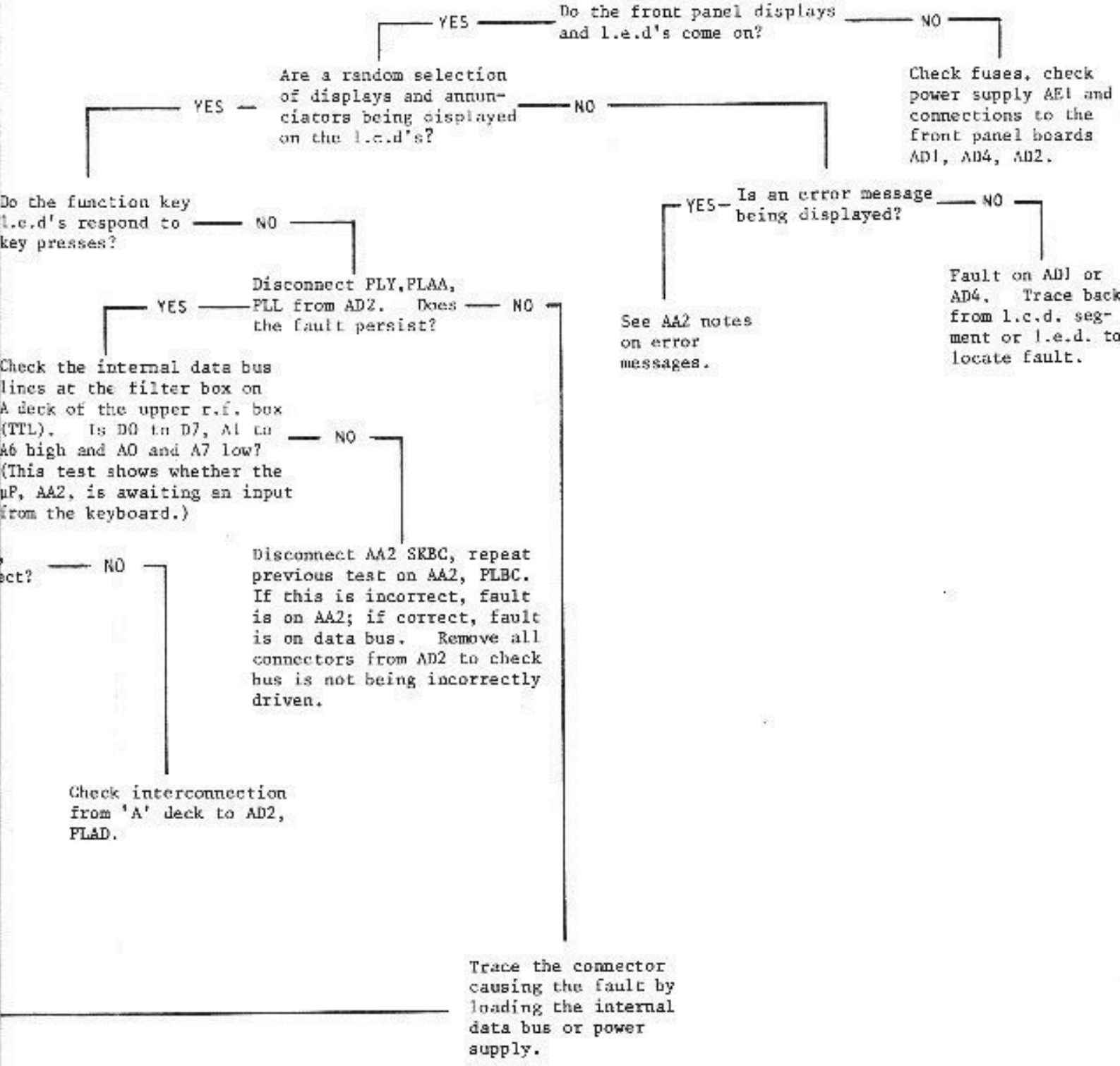
Fig. 1b Location of components, connectors, plugs and



of components, connectors, plugs and sockets


YES
Do the function key l.e.d's respond to key presses?
YES
YES
Check the internal data lines at the filter box A deck of the upper r.f. (TTL). Is D0 to D7, A1 A6 high and A0 and A7 lo (This test shows whether µP, AA2, is awaiting an from the keyboard.)
YES
Repeat test on AA2, PLAD. Is it correct?
NO
YES
Fault on key-board AD4.
Check interconnec from 'A' deck to PLAD.
Disconnect PLY,PLAA, PLL from AD2. Does the fault persist?
YES
NO
Trace back from l.e.d./l.c.d. key at fault.

FRONT PANEL FAILURE



FRONT PANEL FAILURE

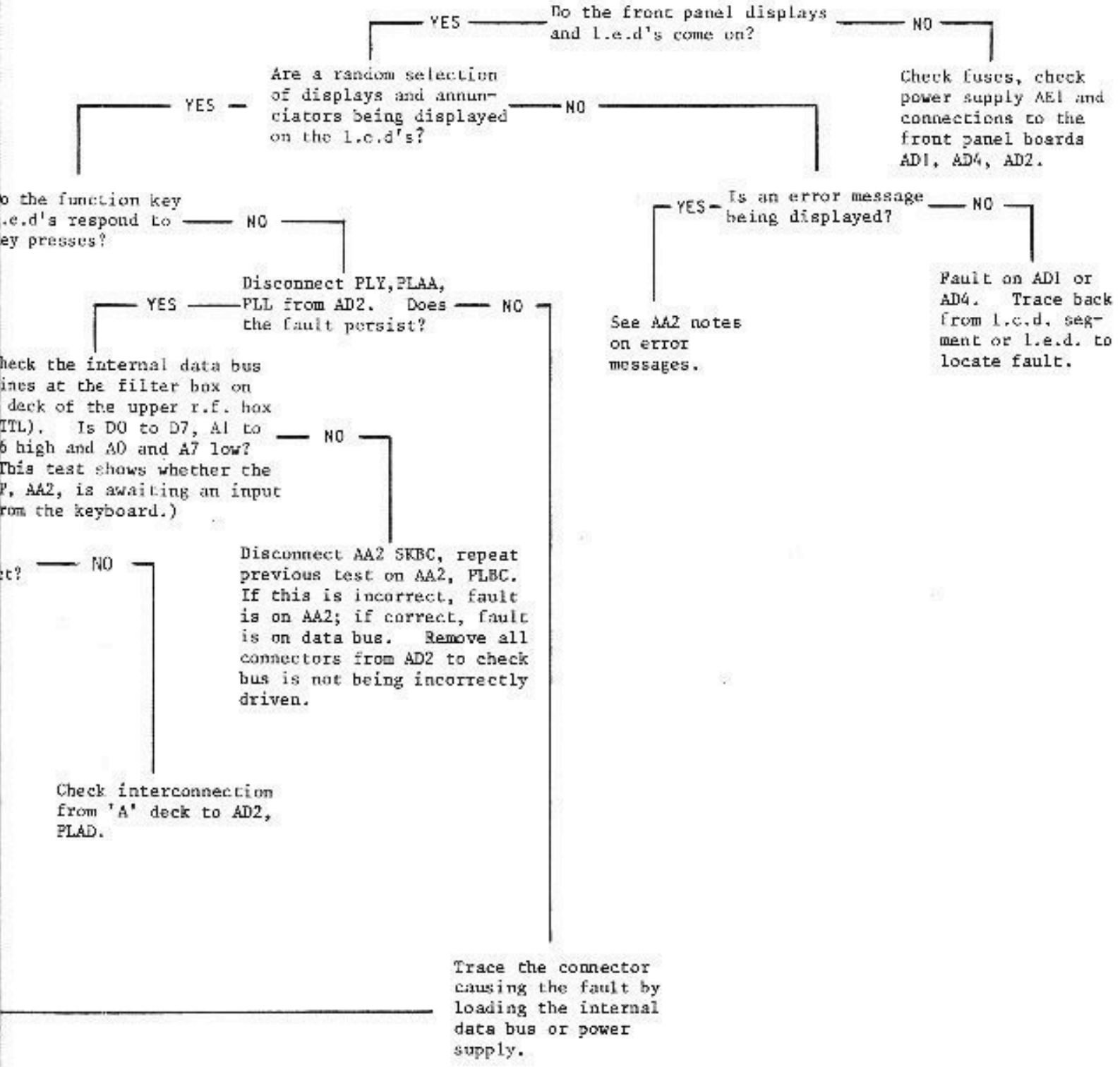


TABLE 7 RF LEVEL FAULT

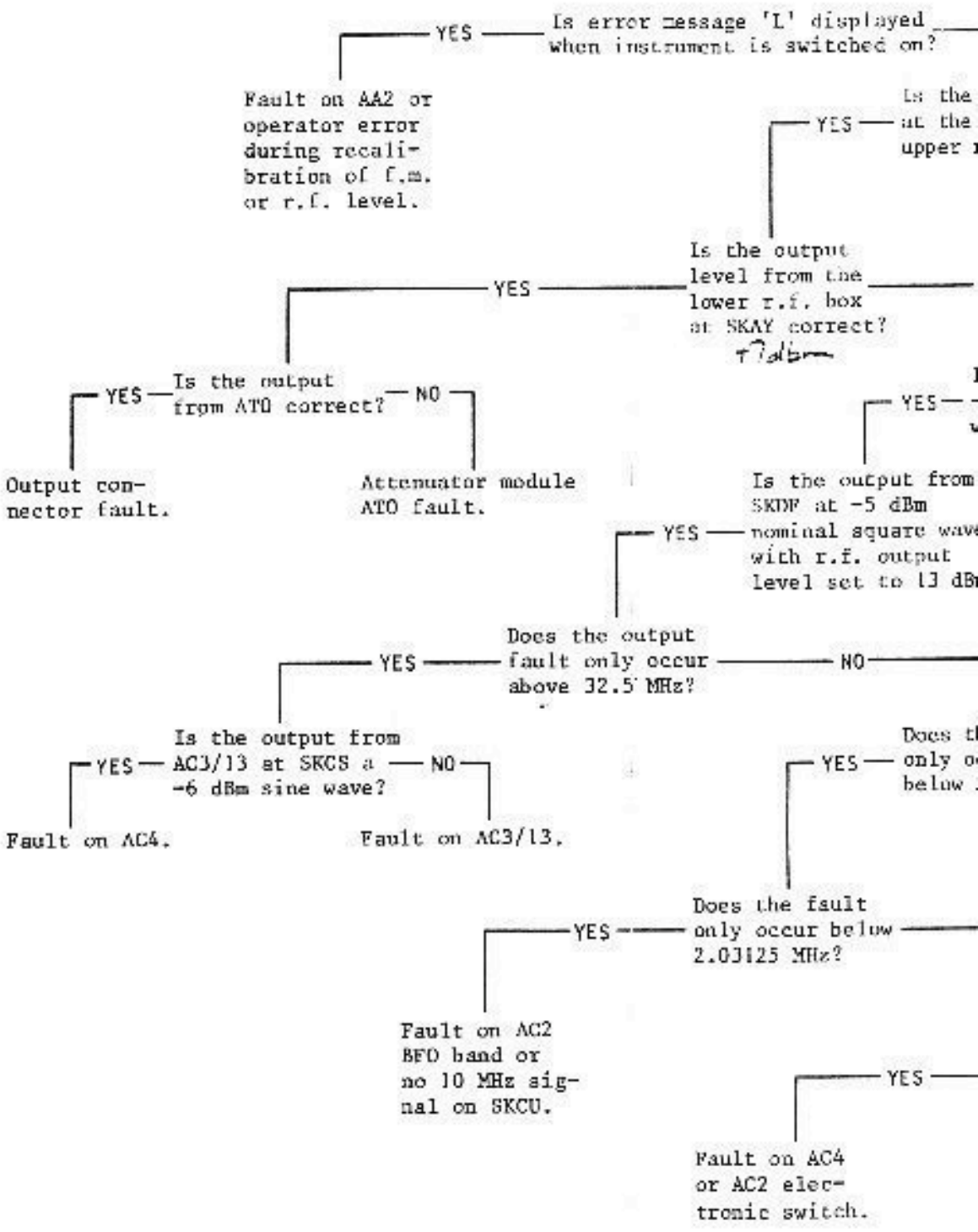
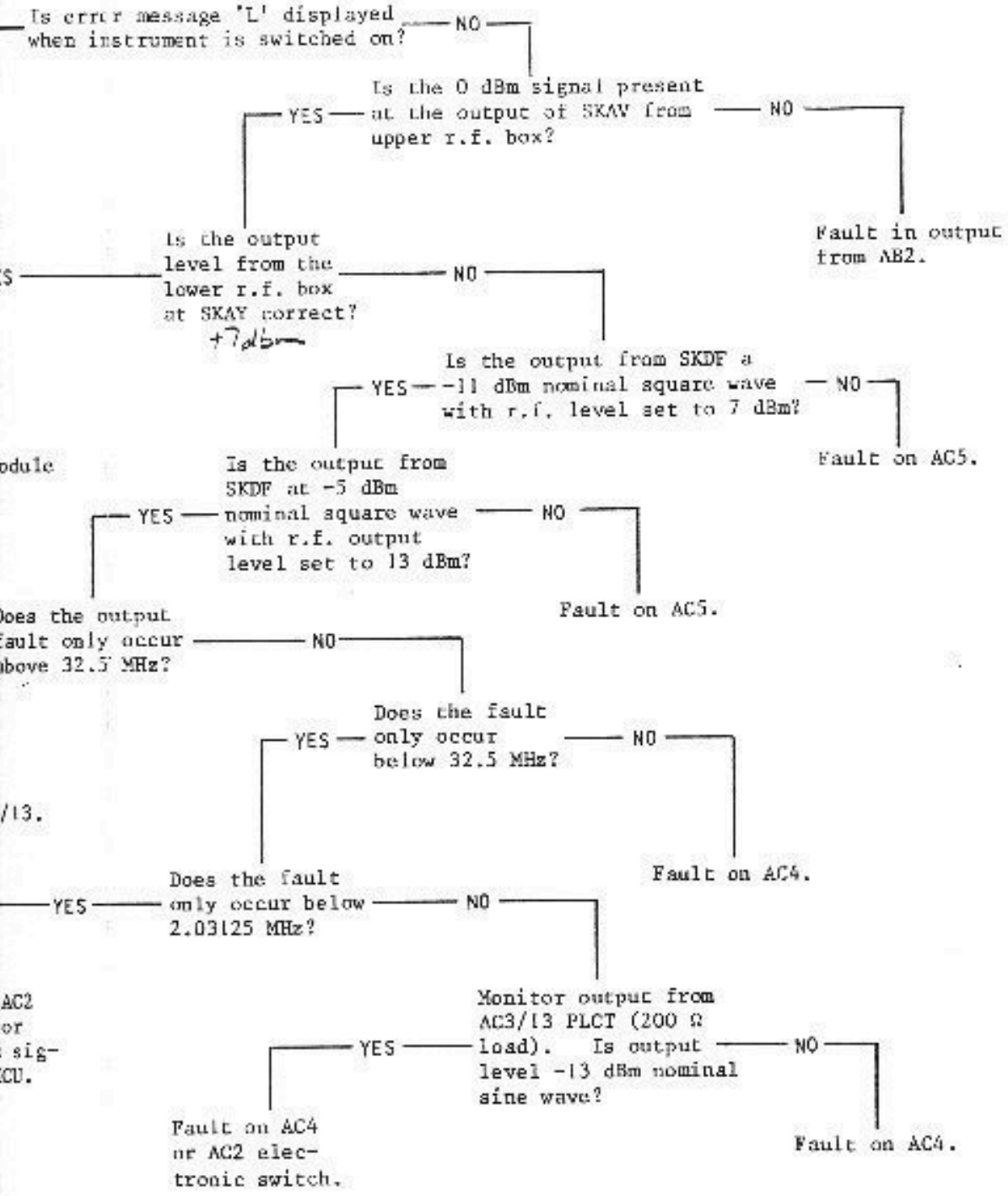


TABLE 7 RF LEVEL FAULT



AA2 : Microprocessor system

68. The board AA2 contains the microprocessor controller and an interconnection system for distributing control data. All the complex IC's on this board are plugged into IC sockets in order to aid fault finding. Without these sockets fault finding can be difficult because of the complex nature of the operations undertaken on this board. If the error message "R" is displayed at switch-on this indicates a RAM fault in either IC3 or IC7. If the error message "P" is displayed at switch-on this indicates a fault in the PROM set IC13,14,15 or 16. This set of IC's is normally replaced as a set. Faulty IC sockets, breaks or shorts in tracks may also lead to error messages being displayed if they result in the RAM/PROM being incorrectly read. If error message "L" is displayed the calibration data in the EAROM store has changed and does not agree with the check sum. This would indicate a faulty EAROM or that the -30 V supply is being incorrectly switched during switch-on or off.

69. Failure to display an error message does not eliminate RAM or PROM faults if the microprocessor is unable to run the system. If no obvious fault can be found (e.g. IC's running hot) first check that there is a clock signal on IC1 pin 7. If there is not check for loading effects by removing the mini-jump from TP7,8 and then try replacing IC1 and XL1. If no fault can be found try replacing each IC in turn until the cause can be found.

70. Faults confined to the EAROM store should be investigated by first checking that the -30 V supply to the EAROM, IC8, is operated during a store operation. Also check that at switch-on and switch-off the -30 V line is not turned on. If these tests are satisfactory replace IC8 and re-calibrate the instrument. The replacement EAROM will have to be initialized as described in the calibration section.

71. Test data AA2.

IC1, pin 37	Microprocessor clock 3.072 MHz.
IC7, pin 35	Normally low. When completing a store operation it should go intermittently high (and sometimes tri-state) in order to turn on the -30 V supply to IC8.
IC9, pin 12	Normally at -15 V. When completing a store operation it should oscillate between -15 V and ground.
IC9, pin 2	Normally at 0 V. On completing a store operation it should oscillate between 0 and -15 V.
TR5 collector	Normally at 0 V. When completing a store operation it should oscillate between +5 and -15 V.
TR4 emitter	Normally at -15 V. When completing a store operation it falls to -30 V.
IC8, pin 1	Normally at +5 V. On completing a store operation it falls to -30 V intermittently.

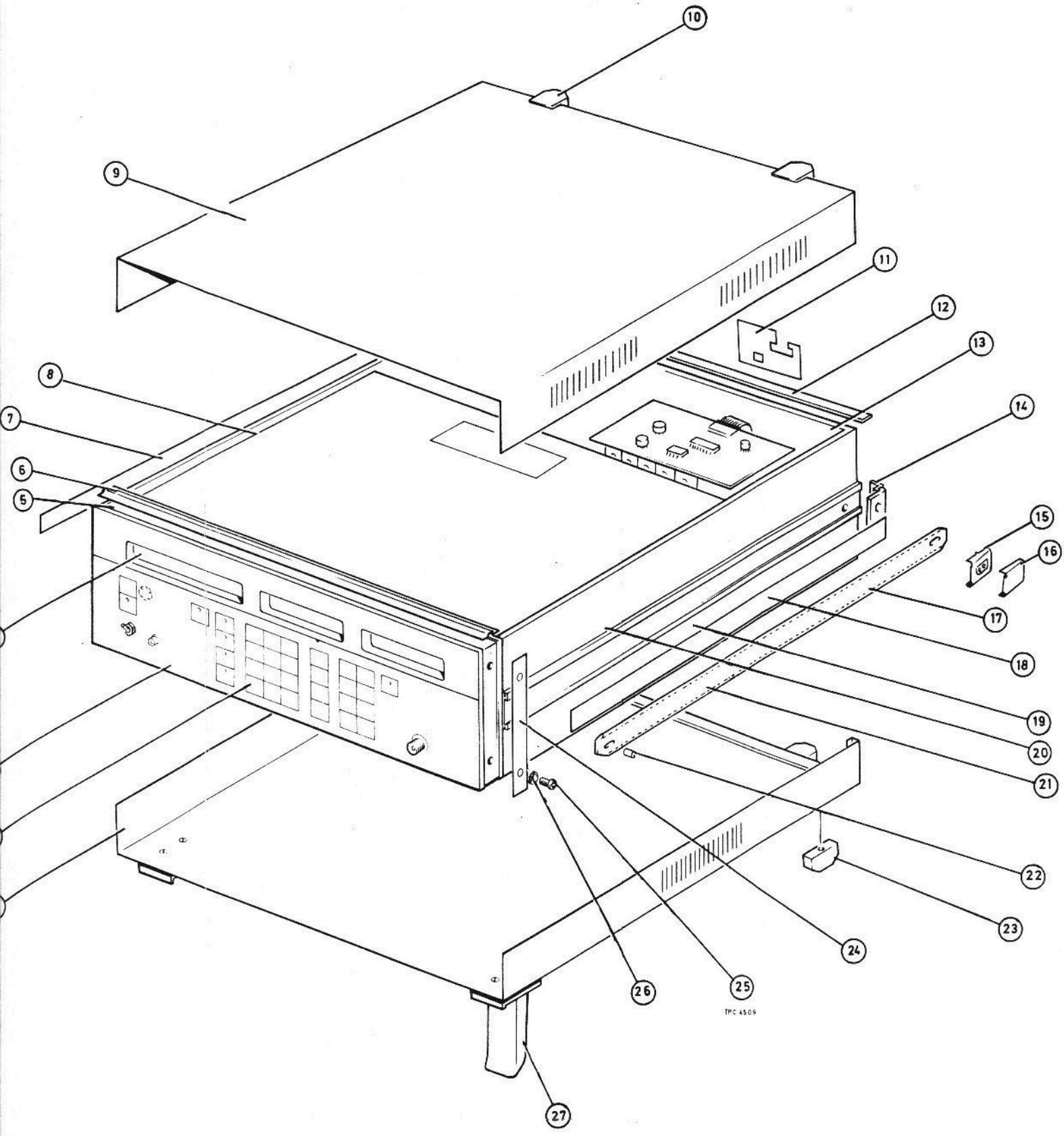


Fig. 1 Miscellaneous mechanical parts

Fig. 1

Item	Description	Part no
11	Selector plate	35902-441Z
12	Rear trim	34900-470E
13	Rear panel assy.	35903-229F
14	End cap	37590-255C
	End cap	37590-256R
15	Liner	22315-584T
16	Cover moulding	37590-257B
17	Steel liner	22315-587M
18	Right-hand side trim infill	35902-386W
19	Side rail assy.	34900-723V
20	Right-hand side frame assy.	35903-315C
21	PVC extrusion	22315-590M
22	Bush	35900-785V
23	Rear lower foot	37590-224R
	Stud	37590-223C
24	Side trim infill (handle)	35902-368Z
25	Screw	21857-465C
26	Screw cup washer	21171-550W
27	Front foot	37590-253X
	Tilt stand	37590-254M

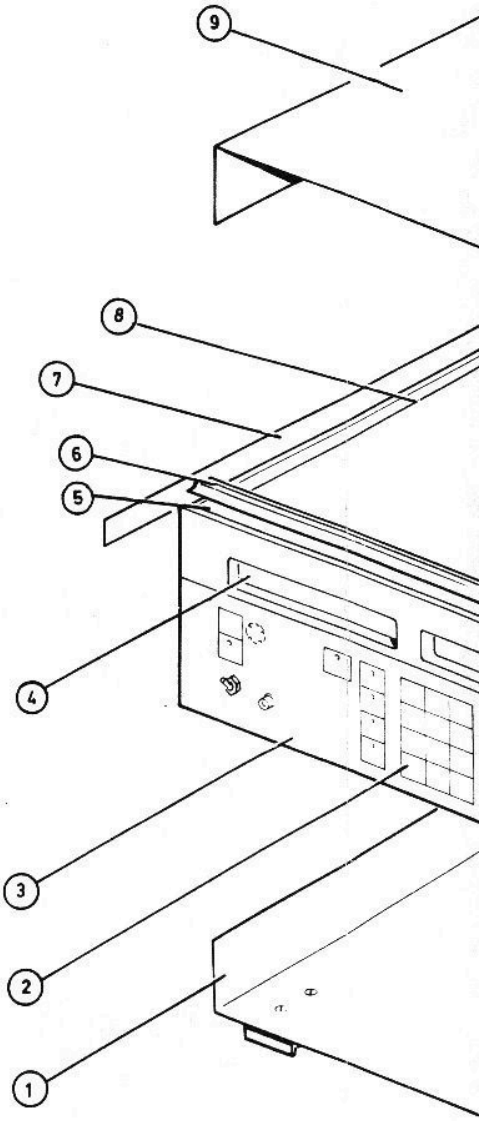
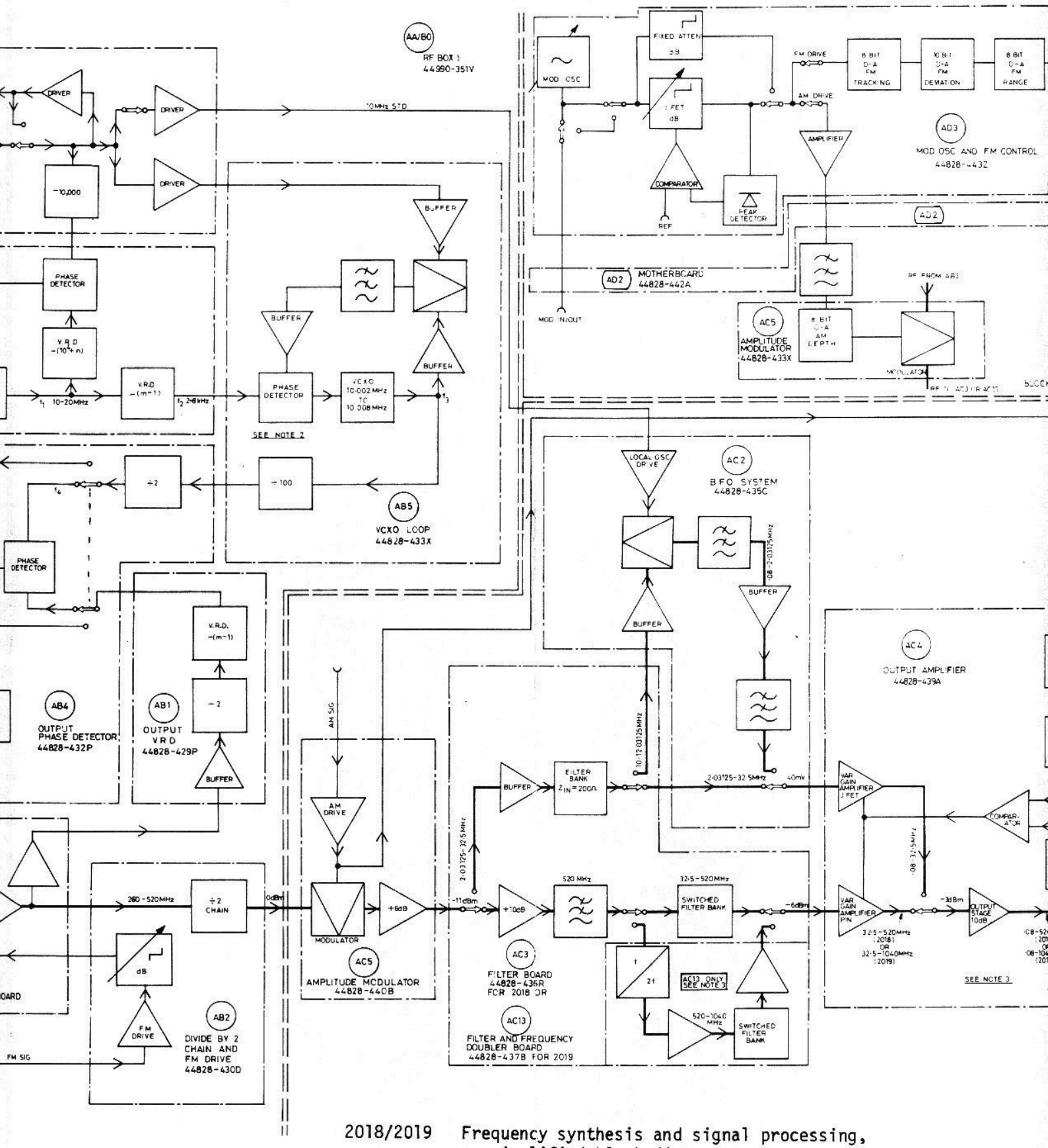
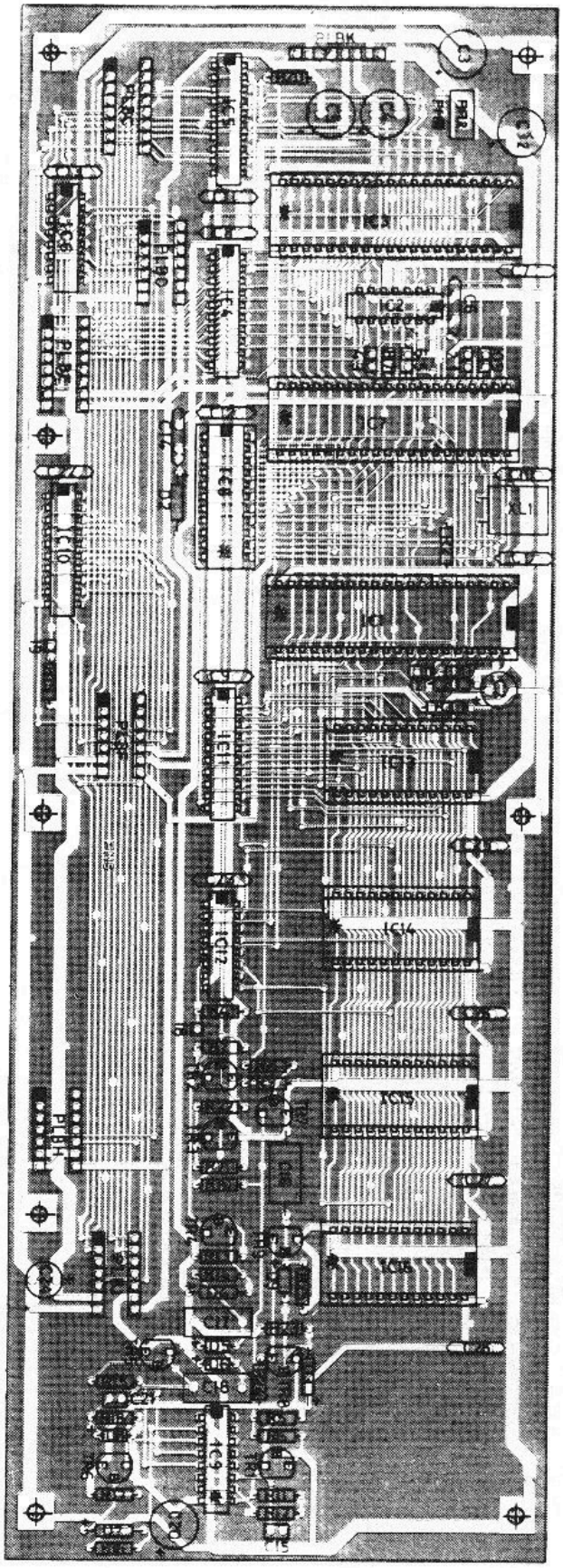


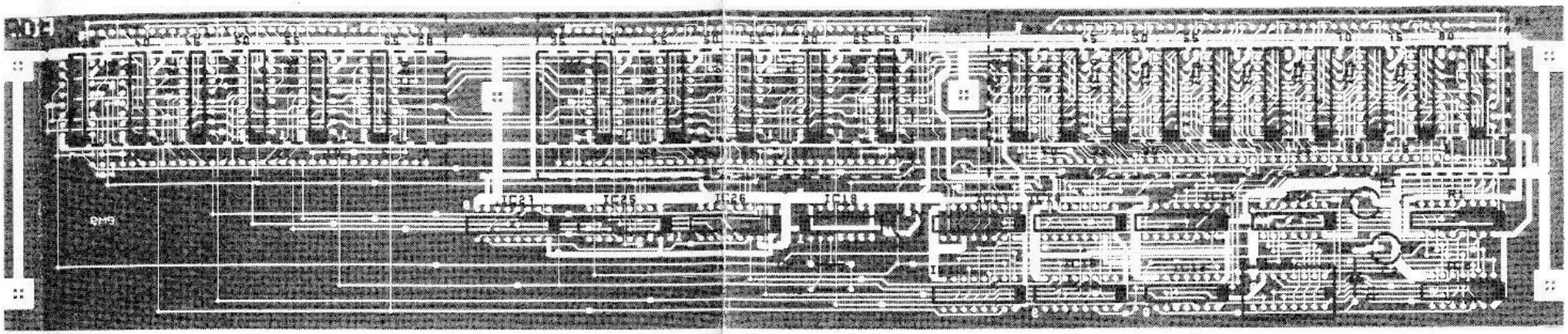
Fig. 1 Mis



2018/2019 Frequency synthesis and signal processing, simplified block diagram



Component layout, AA2



Component layout, AD1