Service Manual

H 52380-900E
Vol. 2

Spectrum Analyzer
Display Unit
2380

Code No. 52380-900E

AMENDMENT RECORD

The following amendments are incorporated in this manual.

Amendment No.	Date	Issued at Serial number prefix
-	June 86	152027

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CONTENTS

HAZARD WARNING SYMBOLS

The following symbols appear on the equipment:

Symbol	Type of hazard	Reference
⚠	Static sensitive device	Page (iv)
⚠	Dangerous voltages present	Page (iii)
⚠	Supply voltage	Page (iii)

Note ...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ▶ .... ◀ to show the extent of the change. When a chapter is reissued the triangles do not appear.

Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers ⚠

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be allowed to discharge through the bleed resistors fitted for the purpose; do not attempt to remove the safety covers from the power supply until the lamp under the top cover stops blinking. Should the unit be reconnected to the supply with the safety covers removed then disconnected, do not attempt to discharge the power supply unit's main reservoir capacitors using a shorting link as the equipment may be damaged. Discharge should always be allowed to occur gradually.

Note also that the 12 kV e.h.t. circuit for the cathode ray tube retains its charge for a considerable time after switch off. Therefore before any handling is carried out in the vicinity of the cathode ray tube or e.h.t. unit it is essential that the supply is disconnected from the instrument and the final anode lead is shorted to the chassis several times immediately after unplugging. The residual charge on the c.r.t. itself must also be removed by shorting the anode connection to ground.

AC supply plug ⚠

The supply plug shall only be inserted in a socket outlet provided with a protective ground contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Fuses - primary and secondary

Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided. A number of secondary fuses are fitted to boards in the upper and lower units. For details of both primary and secondary fuses, refer to Performance data in the Operating Manual.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol ⚠ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange disks, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disk or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with a grounded conductive surface.

Metallic tools grounded either permanently or by repeated discharges.

A low-voltage grounded soldering iron.

A grounded wrist strap and a conductive grounded seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

(4) If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

Cathode ray tube. When exposing or handling the tube take care to prevent implosion and possible scattering of glass fragments. Handling should only be carried out by experienced personnel and the use of a safety mask and gloves is recommended. A defective tube should be disposed of in a safe manner by an authorized waste contractor.

WARNING : TOXIC HAZARD

Many of the electronic components used in this instrument employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

RADIO FREQUENCY INTERFERENCE

This equipment conforms with the requirements of IEC Directive 76/889 as to limits of r.f. interference.

LOGIC MNEMONICS USED IN THE LOGIC SECTION

A OR A-B SEL	A OR A-B trace SEL
ADSR	A channel Display Shift Register
AVG	A Video Generator
B SEL	B trace SELect
BDC	B Data Comparator
BDML	B DeMultiplex Latch
BDSR	B channel Display Shift Register
BVG	B Video Generator
COL	Current Ordinate Latch
DACK1	Direct memory access ACKnowledge 1
DDM	Data Display Mask
DIV H	DIVIDE Higher bit
DIV L	DIVide Lower bit
DMA	Direct Memory Access
DMARL	Direct Memory Access Request Latch
DREQ 1	Direct memory access REQuest 1
DRQ	Direct memory access ReQuest
DRQ 1	Direct memory access ReQuest 1
DSR	Display Shift Registers
EOC	End Of Conversation
ERSD	Even Row Start Detector
ESPG	Extra line Sync Pulse Generator
ESTB	Extra Sync Trigger Bistable
GCHM	Gated Clock & Horizontal Mask generator
GDSR	Graticule Display Shift Register
HRTC	Horizontal ReTraCe
HRTCS	Horizontal RetraCe Sync
HSTB	Horizontal Sync Trigger Bistable
HSYNC	Horizontal SYNC
IOW	Input/Output Write
LCVM	Line Count & Vertical Mask generator
MPY	Multiply
SDA	Spectrum Display Area
VML	Vertical Mask Latch
VRTC	Vertical ReTraCe
VRTCS	Vertical ReTraCe Sync
VSYNC	Vertical SYNC
WD	Write Display
WE	Write Even
WO	Write Odd
WPG	Write Pulse Generator
XV1DEN	Y VIDeo ENable
YVIDEN	Y VIDeo ENable

Chapter 4-2

TECHNICAL DESCRIPTION

CONTENTS

INTRODUCTION

1. The following description should be read in conjunction with the appropriate diagrams in this chapter and with the circuit diagrams in Chap. 7. The circuits are summarized in paras. 3 to 8 and then described in detail in the paras. that follow.

2. The spectrum analyzer comprises one or more lower units containing the frequency synthesizer plus a common upper unit described in this volume containing the display and power supply. Communication is via a two-way serial 9600 baud 20 mA current loop for housekeeping data whilst a one-way high speed serial link is used for the display data. The upper unit's power supply will power up to two lower units with only one selected at any one time. The lower units are internally wired to be self-addressing, therefore any configuration of units may be controlled via the front panel or remotely via a single GPIB socket as if it were a single instrument.

CIRCUIT SUMMARY

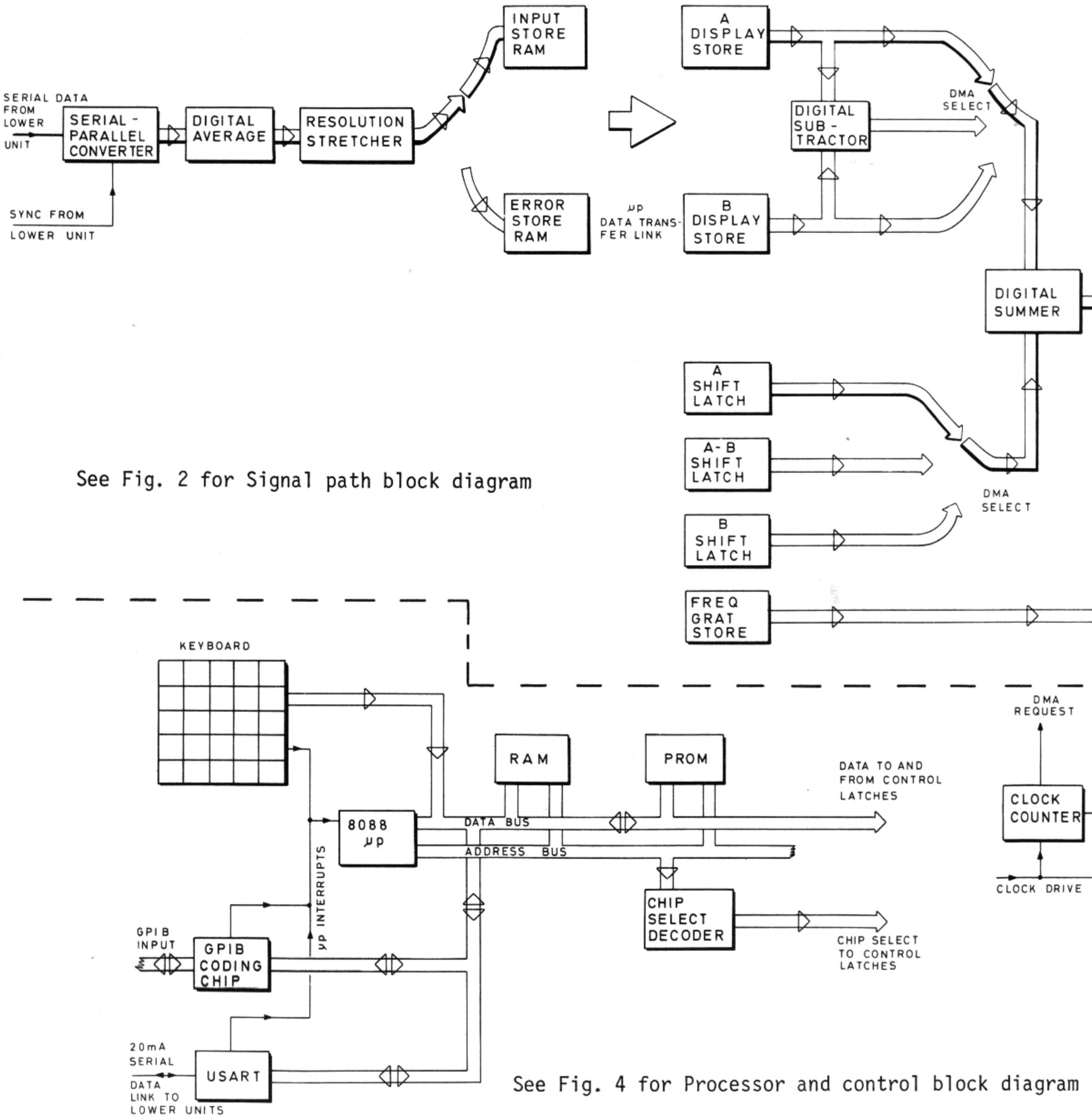
Signal path, display, pen plot & RGB video

3. The serial data input from the selected lower unit at the 2.5 MHz bit rate (see Fig. 1) is converted to 16-bit parallel data and is subjected to a running digital averaging process to simulate the customary video filter. A normal analogue RC network is inappropriate since, due to the inclusion of the high resolution switched gain logarithmic amplifier, no full range detected analogue signal exists anywhere in the system.

4. Since the final stored picture has a resolution of 500 slots across the displayed frequency span, it is necessary to ensure that any spectral responses less than one slot wide do not get missed or attenuated. The Resolution Stretcher is designed to do this whilst at the same time not exaggerating the noise level, as a simple peak hold circuit would do.

5. The processed data word is now transferred under Direct Memory Access (DMA) control to RAM space dedicated as Input Store or Error Store depending on whether the current sweep is a measurement scan or a calibration scan. The data in these two stores is now selectively subtracted (the data space in the Error Store permits correction over the range 100 Hz to 400 MHz) and loaded into the appropriate dedicated RAM spaces known as A Store and B Store under microprocessor control.

6. Each Display Store shift register contains 500 bytes representing the data for the currently displayed image. These data can be used to produce an infilled display or an outlined display depending on the option selected. On the completion of each horizontal scanning line (one complete recirculation of data in the shift register), the Clock Counter generates a DMA request. This results in a DMA transfer of a single display slot of data from the appropriate Display Store to the appropriate shift register. During this transfer the 16-bit word in the Display Store is added to the 16-bit word in the Shift Latch to arrive at the correct vertical display value and is then subject to the correct hardware multiplication to give the selected scaling factor before the 8 bits appropriate to the selected display range are loaded into the recirculating shift register. The output from the shift register is used to produce a solid (infilled) display or is subjected to further line draw processing to produce an outlined display. The resulting signal is then mixed with the graticule and character symbol data before being applied to the video amplifier and thence to the c.r.t.

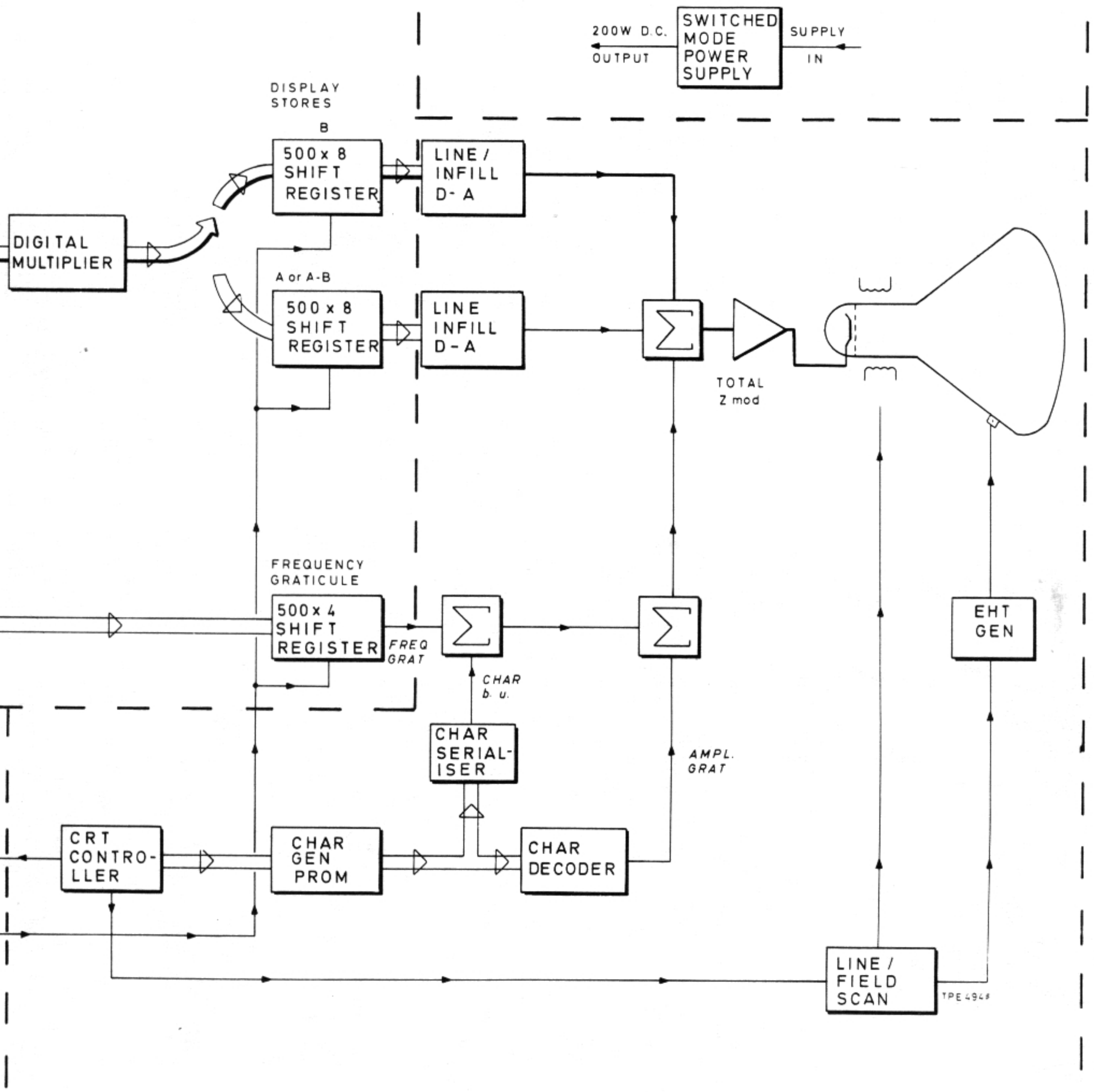


See Fig. 2 for Signal path block diagram

See Fig. 4 for Processor and control block diagram

Block schemati

See Fig. 8 for Power supply block diagram



See Fig. 3 for Display block diagram

7. The frequency graticule data and marker data are similarly refreshed, two bits being used for Graticule brightness information and two bits being used for Steady or Flashing Markers.

8. The c.r.t. controller chip organizes the display drive waveforms and also drives the character generator EPROM to annotate the graticule and display mode status information. The first character of each line is used as a control character and is suppressed, decoded and used to generate the amplitude graticule. Thus the graticule for both axes is under microprocessor control and may draw in any type of ruling to suit the needs of the display.

9. An optional board supplies the drives for the x and y axes of a pen recorder, as well as RGB outputs for use with a colour monitor and a composite video output for a monochrome monitor.

Processor and control

10. Front panel controls are serviced via microprocessor interrupt procedures. Additionally, the processor shares the data and address buses with a DMA controller to allow direct memory access to selected peripherals. All system switching, control and flag reads are done via a two-way buffer on the microprocessor bus. In this way, bus wiring is free from the continuous data train of pulses on the normal microprocessor bus thus reducing the possibility of interference to the analogue circuits. Housekeeping data between the processor and the r.f. units is conveyed by 20 mA current loop. The GPIB interface housed in the display unit allows the spectrum analyzer to form part of a system acting under the direction of a controller.

Power supply

11. Besides powering the display unit, the power supply supplies one r.f. unit on full power and a second on standby power. The switched mode power supply controller operates in synchronism with the associated r.f. unit's frequency standard. The controller shorts down to provide protection against overload, overvoltage or overheat conditions while rear panel l.e.d's illuminate to warn of overvoltage, undervoltage and overload as well as to indicate when no r.f. unit is connected.

SIGNAL PATH

12. The signal path block diagram is shown in Fig. 2. Serial data for display from the r.f. unit at a 2.5 MHz bit rate and accompanied by a synchronizing pulse is applied for processing by board AB2. Only the least significant 13 bits of the 23-bit word are used by the r.f. unit. The data is serial to parallel converted and simultaneously averaged in a shift register. Here, up to the full 23 bits may be used for addition during the averaging process used to simulate a video filter. Synchronizing pulses are counted on AB2 to indicate to the processor when data for the next ordinate (out of the 500 displayed) is to be written into the data store, as well as indicating end of sweep, according to display mode. Maximum and minimum data latches on AB2 implement the resolution stretcher used to ensure that spectral responses less than one slot wide do not get missed. The data is next transferred under direct memory access to either the input store or the error store in RAM depending upon whether the current sweep is for data or measurement purposes. After selective subtraction, the now calibrated data is loaded into the A or B display store in RAM.

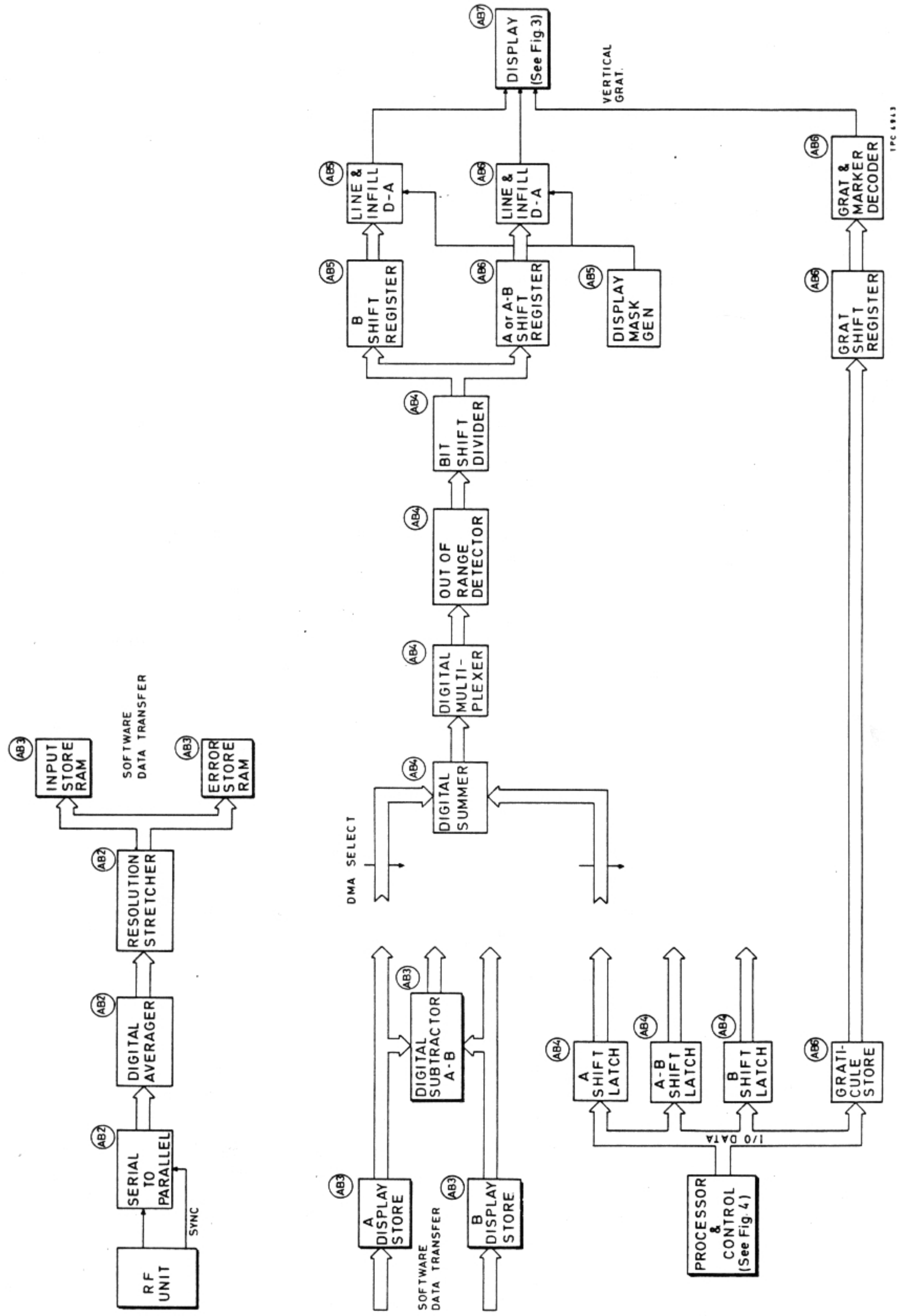


Fig. 2 Signal path block diagram showing main functions of boards

13. Data from the A store, the B store or the result of A-B is summed on AB4 with the A,B or A-B shift latch respectively to determine the vertical display position. A x1 or x5 multiplier on AB4 provides the required scaling factor. The following bit shift divider, responding to controls such as for reference level, operates in conjunction with out of range detectors. The B data is fed to AB5 while the A or A-B data together with the graticule data is fed to AB6.

14. 8-bit data for each of 502 ordinates is held in Display Shift Registers (DSR) on boards AB5 and AB6. The A store DSR on AB6 holds either A or A-B data, while the graticule DSR on the same board holds 4-bit data for the vertical graticule lines (horizontal line data is processed on AB7). All shift registers are recirculating to enable the data to be read non-destructively in byte serial form. Each circulation represents one horizontal display scan. At each ordinate position, the 8-bit display data is decoded to determine which picture elements are to be lit up to provide the selected infilled or outlined display. In the case of the graticule, the elements are lit up to form the vertical line when the scan reaches the appropriate position. The 4-bit graticule data in fact contains both graticule and marker information, 2 bits are decoded to define a major, minor, dashed or no graticule line, while the remaining 2 bits are used for steady or flashing marker selection.

15. Clock generators on AB5 control the operation of the shift registers on both AB5 and AB6, as well as providing the horizontal and vertical masks used for screen blanking to prevent spurious data from appearing outside the 502 x 250 element display area. Outputs for the different displays are taken to the video mixer on AB7.

Board AA1 - Mother board &
Board AA2 - Auxiliary connector

Circuit diagrams : Chap. 7, Figs. 4,5 & 14

16. Mother board AA1 connects together eight 60-way 2-side edge connectors and five smaller connectors. The eight hold the main logic boards, AB1 to AB8. The backplane behind them consists of two sets of bused signal lines and an area of daisy-chained lines. The bused signals are common to many of the boards, e.g. power rails, data bus, processor read and write signals and clock signals. The daisy chain area is used to connect 'private' signals between adjacent boards. Included in the bused signals are some which will allow expansion at a later date, mainly on the options board AB8. Examples of this are colour video output and the addition of a second interrupt controller.

17. The small connectors on AA1 are as follows : PLA is used to transfer signals from the backplane to the lower unit via the data connector on the rear panel. PLB connects the backplane to the INTENSITY controls and the SUPPLY ON l.e.d. on the front panel. PLC connects the main power rails from the power supply to the backplane. PLD connects some signals and the minor power rails from the power supply to the backplane. SKJ connects the TV unit to the backplane.

18. Auxiliary connector AA2 transfers some 'private' signals between AB5 and AB6, there being too many to fit in the daisy-chain area of the mother board alone.

Board AB2 - Input signal data processing

Circuit diagrams : Chap. 7, Figs. 8 & 9

19. The circuit of AB2 can be split into two major blocks, following roughly the same break line as the two sheets of the circuit diagrams. The first section deals with the gathering of the data from the lower unit, which is in serial form, and producing a parallel data word. In this section of the circuit the data is averaged. There is also a number of ICs employed in the synchronization of the serial to parallel conversion, and the calculation of the Ordinate Rate, which is the rate at which data is input to the data stores of the analyzer.

20. The second section of the circuit includes a maximum and a minimum detector which acts on the parallel data word produced by the averaging process in the first part of the circuit. An algorithm is used to determine which of the two detectors is used as the source of data which will be stored in the data stores.

Parallel to serial conversion and averaging

21. The data from the lower unit is sent in a serial format and is packaged as a 23-bit word every 10 ms at a 2.5 MHz bit rate. Only 13 of the bits are used by the lower, r.f. unit, and occupy the least significant 13 bits of the 23-bit word. The least significant bit is sent first. To enable the data to be synchronized as it arrives from the lower unit, an END OF CONVERSION pulse is provided by the r.f. unit. This negative-going pulse arrives on a separate line. The positive-going edge marks the beginning of the first data bit.

22. The circuit based on IC30 serves to provide clock pulses that have edges about half way through each data bit period. This part of the circuit (a divide by 5) has a 2:3 mark space ratio. The divider is held in the reset state during the END OF CONVERSION synchronizing pulse, and it is clocked at a clock rate 5 times faster than the required clock frequency. In this way, the divider produces on its output a clock frequency at 2.5 MHz which is used to clock the data into the shift registers. The active edge is 2/3 of the way through the data periods.

23. As with standard serial to parallel practice, the two clock frequencies (the one clocking the data out of the lower unit, and the one clocking the data into the upper unit) need not be exactly the same, so long as the difference in frequency does not cause the clocking edges to drift outside the data bit periods. In this case, since the clock pulses may start within 1/3 of the clock period from the edges of the data periods, and there are 23 such data periods, the accuracy of the clock should be better than 1 part in 69. It is for this reason, that the difference in the master clocks of the two units (about 1 part in 400) is of no consequence since both master clocks are crystal controlled and phase locked together.

24. The actual serial to parallel conversion takes place using three 8-bit shift registers, ICs 15 to 17. The data is input via a one bit full adder. The action of this adder is to add together the incoming data with the data which is being shifted through the shift registers. By selecting the correct tap on the shift registers (the 23rd tap, since the data words are 23-bits long), the recirculated data bits will have the same bit value as the bits to which they are to be added. After two data words have been added, the value in the shift register will be twice the value of the two individual data words

(assuming both data words had the same numerical value). Hence the correct value can be obtained from the shift register by performing a one bit shift in the correct direction (a one bit shift to the right is a divide by two). If the two data words were different, then the value obtained would be the average of the two words.

25. By taking four words at a time, adding them in the same manner as above, and then performing a two bit shift, the average of four words can be obtained. Averages over other numbers of data words can also be done, but to enable simple division by the application of bit shifts, these are restricted to simple binary numbers. Since the total of the additions must be stored in the shift register until the time when the final shift/division takes place, there is a maximum number of additions that can take place before the 23 bit capability of the shift register is exceeded.

26. The controlling of the shift register, the adder and the final shift/division is achieved by the Average Clock Counter, IC20. This counter is programmed with the total number of clock pulses to be applied to the shift register. To clock in one complete word, 23 clock pulses are required. To add two words together, 46 clock pulses would be required etc. These numbers are modified by two factors: the final shift/division, and the positions of the 13-bit parallel taps. Since the taps are on the first thirteen bits of the shift register, the number of clock pulses required for the first word to appear at the output taps is only 13. However it still takes 23 pulses before it reaches the end of the shift register and is ready to be added to the next data word should this be required.

27. To allow for the final shift/division, extra pulses must be applied to the shift register to move the data through by the correct number of bits. The final division ratio becomes 23 x N - 10 + 2LOG(N), where LOG is to the base 2. This formula is derived from; 23 bits x N, where N is the number of averages of 23-bit words; -10 for the offset due to the position of the taps; and LOG(N) for the number of bits of shift to perform the correct division.

28. After the correct number of clock pulses, the output of the Average Clock Counter causes the data appearing on the shift register taps to be latched into ICs 32 and 33. At the same time the shift register is reset ready for the next average, and the pulse is passed to the second block of the circuit on the ENABLE line to signal that data is available.

29. The one bit full adder, mentioned earlier is made from separate gates. The CARRY OUT is latched from one data bit period, and applied to the carry input during the next data bit period.

30. Some very slow sweep rates using narrow filters require that the averaging be done over a period of greater than 210 data input words. This is not possible, as stated earlier, because the shift register cannot contain the total of that number of data words. However, the data words produced by such a sweep are necessarily varying at a very slow rate due to the band limiting effect of the i.f. filters, and thus two or more consecutive words cannot differ by any significant amount. Under these circumstances a proportion of the input words is lost, without any fear of losing required data. The programmable Input Word Rate Divider and the latch IC18a provide a gating signal to the STROBED 2.5 MHz clock used to clock the shift register. In this way, a gating signal is provided to extend the data averaging period by up to 216 times greater than the basic 10 microsecond sampling rate.

Clock generation

31. The Ordinate Clock Generator and the Sweep Terminator Generator are two closely related parts of the circuit. During normal (swept linear frequency) scans, the incoming END OF CONVERSION pulses are counted, and a pulse is produced which signals to the processor that it is time for the next data ordinate to be written into the data stores. The END OF SWEEP pulse produced by the Sweep Terminator Generator is, on these 'normal' sweeps, a pulse produced by a division by 502 (by IC20) on the ORDINATES pulse. The division is by 502 because there are 50 ordinates in each of the 10 frequency segments across the display, and 2 more are on the last graticule line.

32. It should be noted that, although the averaging and the ordinate clocks are both derived from the same END OF CONVERSION pulses, they are not locked together; the averaging clock is a 1 2 4 8 16... division on the END OF CONVERSION pulses, and the ORDINATES clock is a 1 2 5 10 20... division on the END OF CONVERSION pulses.

33. For the Zero Span modes, the r.f. unit defines the ordinate rate and therefore the Ordinate Clock Generator division ratio must be set to one. Since this is an inadmissible division ratio for this programmable section, the divider has to be bypassed. This is done by programming its output to be high impedance, pulled to a logic 1 by the pull-up resistor, and using only monostable pulse generator IC34 to produce the 1:1 END OF CONVERSION to ORDINATES pulse ratio. The Sweep Terminator Generator still produces its pulses every 502 ordinates.

34. In the Log Scan mode, each decade is swept separately by the lower unit. Each decade sweep is used to fill 1/nth of the data stores, where n is the number of decades requested for the display. The total number of ordinates in n decades is not exactly 502 (or 500 for that matter) for all values of n, since there must be the same number of ordinates in each decade, and 500 is not divisible by 3, 6, 7 etc.

35. During these Log sweeps, the Sweep Terminator Generator is used in a different manner. It is used to create the log shaping to the frequency scale of each decade. The linear decade frequency scan produced by the lower unit is divided into ten segments. Each segment will have the same number of ordinates, but will represent a different amount of the frequency scan, the proportions being in a logarithmic ratio. The Sweep Terminator Generator is used to signal the end of each of these segments. It is programmed to interrupt the processor after the (fixed) number of ordinates in each segment. The Ordinate Clock Generator is programmed with a different number for each segment, and by using the facilities of the programmable counter, viz preselecting the next count ratio before the last count has been completed, the interrupt from the Sweep Terminator Generator need not be very high priority.

36. On Logarithmic sweeps, where the number of decades is low, the number of END OF CONVERSION pulses per ordinate is small. It is not possible to produce a good approximation to a logarithmic scan by using the same number of END OF CONVERSION pulses for each ordinate in any one segment. Since the overhead of programming the Ordinate Clock Counter differently for each ordinate is too great, a much faster clock is used so that the gradation from one segment to the next can be much finer and more exact. The clock chosen is a 2.5 MHz output from the CLOCK TICK generator prescaler IC31. It is

gated (in the programmable divider) by a signal from IC25a which starts with the first END OF CONVERSION pulse, and stops when the Sweep Terminator Generator produces its END OF SWEEP pulse.

37. Divider IC29 in this section of the circuit provides a glitch-free 6.25 MHz clock for the microprocessor and the UART; the clock produced by the 6.25 MHz phased clock generator may have glitches until the CRT generator is set up. Another divider, IC20 and IC31 produces the CLOCK TICK signal for the real time executive. The clock rate is 10 ms.

Maximum and minimum detectors

38. The maximum detector consists of the 16-bit comparator formed by ICs 9 to 12 which compares the incoming PARALLEL AVERAGED DATA with the data already stored in the Max Data Latches, IC23 and IC24. The presence of new data is signalled by the ENABLE pulse from the Averager Clock Counter. Should the new data be smaller, no action is taken, but should it be larger it is transferred to the Max Data Latches and becomes the new maximum data value. IC12 pin 5 'greater than' output is ANDed with ENABLE by IC13a and used to set max latch IC14a to show that a new maximum value has been found. If the data value did not rise above that stored in the Max Data Latches during an ordinate period, the max latch IC14a will not be set.

39. The minimum detector formed by ICs 5 to 8 works in a similar way to the maximum detector. The comparator finds the minimum values of the data, and stores them in the Min Data Latches ICs 21 and 22, setting min latch IC14b at the same time. If the data value did not fall during an ordinate period, the min latch IC14b will not be set.

Max/min select logic

40. At the end of each ordinate period, signalled by the ORDINATES pulse from the Ordinate Clock Generator, the Max/Min Latch Select Logic circuit (IC29a pin 1) and the DMA controller (DRQ Latch IC41 pin 13) are strobed. The Max/Min Select Logic operates using the algorithm described below.

41. Two of the several requirements of the spectrum analyzer display are that it should show the maximum value of any signals, and should at the same time show a reasonable representation of noise, and not just its peak and minimum values.

42. In a display where the IF filter bandwidth used is relatively wide compared with the scan width, the signal appears as a wide, rounded topped, display. Noise on the other hand would appear more ragged, and may well appear as 'grass', having a very fine amplitude v time display. During any one ordinate time period, when the analyzer is scanning through the signal part of the display, the max and min detectors, and their associated max and min latches would be detecting either a rise or a fall, but not both, since the signal amplitude is changing smoothly from one value to the next. When the scan is in the noise part of the display, it is likely that during any one ordinate period, new maximum and minimum values will be found, and both the max and the min latches will be set.

43. To form an acceptable display for this type of scan a very simple algorithm is used. When the signal amplitude is rising only, the peak detector is used. When the signal amplitude is falling only, the minimum detector is used. When the signal amplitude both rises and falls, then the state of the max and the min latches during the previous ordinate is checked. Should

this previous state be rise only, then the max latch is read for this ordinate; should the state be fall only, then the min latch is read for this ordinate; should the state be both rise and fall, then the opposite latch to that last read, is read for this ordinate. In this way, during periods of noise, the detector latches will be set during each of the ordinates, and the max and min data latches will be read alternately. However at a signal peak, the max latch will be read even though the signal both rises and falls, since the detector latches would have been showing 'rise only' during the previous ordinate.

44. To satisfy the algorithm, the outputs of max latch IC14a and min latch IC14b are ANDed by IC27a to produce a change-over signal to the following gates. These gates select either the state of the max latch if max.min= '0', or the J-K bistable IC29a if max.min = '1'. When the signal does not both rise and fall, i.e. max.min = '0', then the max or min data latches are read depending on the state of the max latch - when max.min = '1' then the J-K bistable performs the needed algorithm. It is clocked on the falling edge of the ordinates pulse, and therefore at the start of the next ordinate pulse the history of what happened at the last ordinate is available. Should the detector latches both be set, the J-K will toggle ready to select the opposite latch to that used on the current ordinate in the event of the next ordinate having max.min = '1'. If the detector latches have differing outputs (max.min = '0') then the outputs of the J-K will reflect the input state after the clocking pulse. Hence the output will select the same latch as the previous ordinate if max.min = '0'.

45. The data enters the max output latches IC37 and IC39 and the min output latches IC35 and IC36 as a 16-bit word under DMA transfer. Since the DMA process transfers 8 bits at a time, two transfers per word have to take place, with the least significant byte being sent first. The ORDINATES pulse from the Ordinate Clock Generator sets the cross-coupled NAND R-S bistable IC41a, IC41d, causing DRQ 0 to become active. The High/Low Byte Select Generator then selects which of the two data bytes must be sent first. This m.s.b./l.s.b. signal is further gated with the max/min latch select signal so that the correct byte from the correct data latch is selected. When the second byte is selected, the R-S bistable is reset which removes the DRQ 0 signal.

46. It is possible, since the ordinate rate and the rate at which averaged data words are produced are not synchronized, that new averaged data will arrive during the data transfer process, and a change in the detector latch outputs could occur. This would cause corruption of the data levels since half of the data word would be read from one latch and half from the other. To stop this happening, the output of the change-over gate, selecting either the max or min data, is latched so that it remains constant during the time that the data is read into the input store of the display.

47. The rules about resetting the max and the min data latches are quite simple. Each time data is output to the data stores, the min data latches and the min latch are reset. The min data latches are reset to the current value of the data from the averager. The resetting of the max data latches occurs whenever they are read, and also whenever the min data latches are read as a result of a min only signal (max.min = 0). It too is reset to the current value of the data from the averager. The max latch is reset each time data is read, at the same time as the min latch and the min data latches.

48. Bypass of the display detector, (for use during Sampled Zero Span displays), is provided via IC38 (CS1E). The detector circuit is enabled whenever IC38 pin 2 is at a logical ´1´ state. It will be seen that under these conditions the three most significant bits of the new data being compared in the max and in the min data identify logic comparators will be set, and will match exactly the three m.s. bits applied to the other inputs. The comparison will then ignore these identical bits, and compare the bits of lesser significance. When IC38 pin 2 is at a logical ´0´ state, the m.s. bit of the max comparator new data input is at a ´0´ and hence the new data input must always be judged ´less´ by this comparator, and hence the max latch will not be set, and no data will be transferred to the max data latches. The minimum detector has its inputs controlled in the same way, and will therefore set the min latch and transfer the data to the min data latches. The detector circuit is hence disabled since its output is always set to give the ´min´ signal (i.e. no max and min stitching), and the data transferred to the input data stores is always that applied to the min latch immediately before the data transfer.

Sweep flyback

49. When a new sweep is started, data from the previous sweep will still be held on the board and would, incorrectly, both be averaged with the new data and displayed as the first ordinate of the new sweep. The DISPLAY DETECTOR FORCE MAX, FORCE EOC and MISS FIRST ORDINATE signals from octal latch IC38 prevent this from occurring. The sequence is as follows: DISPLAY DETECTOR FORCE MAX is asserted low to IC12 pin 1 in preparation for the next data byte. Averager Clock Counter IC20 then generates a pulse during flyback which resets the Serial to Parallel Converter IC15,16,17 to zero and latches the zero into the paralled averaged data latch IC32,33 while also providing the ENABLE pulse to the next stage. With its most significant bit pin 1 set low, IC12 recognizes the applied zero data as a new maximum so that, at the end of the ENABLE pulse, the zero data is latched into max data latches IC23,24 and max latch IC14a is set. At this point the DMA controller on AB3 causes extra DMA cycles to be made to dump the unwanted data in the output latches to spare memory locations. FORCE EOC is next asserted high to IC42 pin 10. Then ZERO SPAN MODE is asserted low to IC19 pin 4 and when FORCE EOC is removed, the falling edge causes IC34 to generate an ORDINATES pulse to High/low Byte Select Gen IC43b and latches the zero data into max output latches IC37,39. But to prevent this data from being accepted into the data store, IC38 asserts MISS FIRST ORDINATE high to prevent a DMA request from being made. To do this, the signal is inverted to reset IC25b causing IC41b to gate off the ORDINATES pulse from DRQ latch IC41a,b so preventing DRQ being asserted high to the DMA controller on AB3. When the data for the new sweep arrives it is recognized as a new maximum (since the previous data was zero) and thus replaces the zero data in the max output latches.

Board AB4 - Mathematics operations

Circuit diagrams : Chap. 7, Figs. 12-14

DMA control and input data selection

50. Board AB4 receives two sets of data, A and B, and from these generates a third, A-B. Data enters the A latches IC38, IC40 and the B latches IC39, IC23 under DMA (Direct Memory Access) control. DMA request latch IC19 output pin 5 goes high at the trailing edge of the WD signal to pin 3. WD goes low when data is to be written to the display shift registers. Since the WD

pulses occur at the line refresh rate, AB4 has about 64 μs in which to process new data before it is required for display.

51. The A and B latch sets each accept 16-bit data (although only the lower 15 bits are actually used), which are presented in the byte sequence; B low, B high, A low, A high. The DMA controller, in fact, follows these with a byte of graticule data, but this is not used on AB4, being latched on AB6 instead. The input latches are controlled by the DMA byte counter IC35 and the associated B, A, graticule demultiplexer IC18. The DMA byte counter counts 5 DACK1 + IOWR clock pulses before resetting DMA request latch IC19 on pin 1.

52. The WD pulse when active low to pin 1 IC35, resets the DMA byte counter to point at the B low latch IC39, ready for the first byte in the sequence. When the DACK1 + IOWR signal becomes active it clocks DMA byte counter IC35 which causes demultiplexer IC18 Y1 output to go active low and the Y0 output to go inactive high. Thus the B low latch IC39 receives a positive-going clock edge on its pin 11 and the first byte enters that latch. As succeeding DACK1 + IOWR pulses arrive, so Y1, Y2, Y3 and Y4 each in turn supply a positive-going edge to their associated latches IC23, IC38, IC40 and that on AB6 respectively. When the fifth pulse arrives, IC35 pin 12 goes high and, via IC24d, IC37c and IC36a, resets DMA request latch IC19a. The whole sequence repeats when the next WD pulse arrives, with the exception of the period when FRAME is active low to IC36 pin 2; the signal prevents DMA channel 1 getting out of step with the display.

53. Once both bytes of B data have been latched, the data can be processed by the rest of AB4. That the B data is available is signalled by the B SEL pulse on IC18 Y2 output which clocks the A low byte latch IC38. Similarly, when both bytes of A data have been latched, the fact is signalled by the A OR A-B SEL pulse on the Y4 output which clocks the graticule byte latch on AB6. The trailing edge (positive-going) of B SEL is used to clock the processed data from AB4 into the latch on AB5, and A OR A-B SEL does the same on AB6.

54. A OR B SEL is gated with the outputs of the A/A-B select latch IC19 to give A SEL from IC37 pin 11 and A-B SEL from IC37 pin 3. These together with B SEL are used to decide which pair of tristate buffers, ICs 20 and 25, ICs 2 and 4 or ICs 1 and 3, will be enabled so as to send data forward for processing. The signals also control the outputs of the shift latches. The processor writes to the A/A-B select latch IC19b using CS36.

55. The A-B data is produced by adding the two's complement of the B data to the A data. This is done by ICs 21, 22 and 24 and ICs 14 to 17. The A-B data is then buffered by ICs 2 and 4 ready for selection if required.

Multiplier

56. In order that the displayed spectra can be moved up and down the screen, it is necessary to add a variable offset to the data. This is achieved by part of the circuit on sheet 2.

57. The 16-bit offset values for the three sets of data are loaded by the processor into the three pairs of shift latches ICs 41 and 44, ICs 42 and 45, and ICs 43 and 46. The processor addresses the latches individually via the local chip select decoder IC49. Maths function latch IC47 controls the multiply and divide circuits. This latch and the A/A-B select latch IC19b are addressed simultaneously using CS36; the latter accepts bit 0 of the byte

which the processor writes, while the former accepts bits 1 to 6. The multiply and divide circuits may need to operate differently for the B data and the A OR B-A data, so the maths function latch contains two sets of control bits at any time. The appropriate set is selected by the maths function multiplexer IC48 according to the states of the B SEL and the A OR A-B SEL signals.

58. When the outputs of the appropriate data buffers and shift latches are enabled the combined data appears at the outputs of the shift adder formed by ICs 26 to 29. Since the data is in two's complement form, the m.s.b. of the combined data on IC29 pin 13 represents the sign bit. And since no data is displayed whose value is less than zero this bit provides the UNDERRANGE signal used to limit the display to bottom of screen (i.e. any data which has a value less than zero is presented as zero on the display). The rest of the combined data is passed to the multiplier circuit formed by ICs 5 to 9, 30, 13a and 36b.

59. The multiplier can multiply by 5 or by 1, according to the state of the MPY signal from IC48 pins 5 and 16. To multiply by 5 (when MPY = 0), a copy of the data is moved 2 bits left (equivalent to multiplying by 4), and then added to the original. The original data is applied to the A inputs of the multiplicant adders, ICs 5,7,8 and 9. The x4 data is applied, via multiplier drive buffer IC6 and IC30, to the B inputs, with the exceptions that the two least significant B inputs and the least significant carry input, are all set to zero by the MPY signal. Thus the output of the multiplicand adders represents the input data x5. Because a 16-bit number is added to a 14-bit number, the m.s.b. of the multiplicand adders is output by IC36 pin 6.

60. To multiply by 1, the multiplier drive buffer (IC6 and IC30) outputs are disabled by MPY being high, and are pulled high by R3 and R4, so that the B inputs of the multiplicand adders and the input to inverter IC13 are all high. Thus the effect of the B inputs is negated; firstly by making all the B inputs logical '1', then adding 1 to the carry input pin 7 of IC5 so that an overflow occurs from IC9 pin 9, and finally by disabling IC36 so as to gate off the overflow.

Overrange detector and divider

61. The bit shift divider selects the appropriate set of 8 bits from the 17 available at the output of the multiplier circuit, but since the smallest division ratio is 2, the l.s.b. of the multiplier output is simply ignored. The bit shift divider formed by ICs 51, 31, 32 and 50 selects sets of 8 bits which give effective ratios of 2,4,8 or 16 under the control of the division select decoder, which is, in turn, controlled by the maths function latch.

62. Even after the data has been passed through the divider circuit, it is possible for its value to exceed that which can be represented on the display (maximum is 250). Therefore, the overrange detector formed by ICs 10,11,12 and 34a, and controlled by the logic on the DIV L and DIV H lines checks the data for illegal values before it is finally sent to the output. For example, when the division ratio is set to 8, bits 2 to 9 are sent via IC32 to the display, while bits 10 to 15 are checked. If any of the latter are on then the data is overrange. The higher the division ratio, the fewer are the bits checked by the overrange circuits. Table 1 shows which bits are checked for the various division ratios.

63. Normally, division select decoder IC33 will enable one of the bit shift divider buffers by taking one of its Y outputs low. However, if the overrange detector finds that the value of the input data is too large, it disables the decoder via IC12c thus preventing any of the Y outputs from going low. The tristated output of the divider buffer will be pulled to all ones by the action of pull-up resistors R5. Similarly, if the UNDERRANGE signal is active, decoder IC33 outputs are disabled via IC12d while the underrange clamp IC52 is enabled thus pulling the output data to all zeros. The resulting processed display data is passed out to AB5.

TABLE 1 OVERRANGE DETECTOR OPERATION - AB4

Division ratio	16	8	4	2
Control signals:-				
DIV L	L	H	L	H
DIV H	L	L	H	H
Bits checked:-				
8				✓
9			✓	✓
10		✓	✓	✓
11	✓	✓	✓	✓
12	✓	✓	✓	✓
13	✓	✓	✓	✓
14	✓	✓	✓	✓
15	✓	✓	✓	✓

Example: For ÷16 DIV L and DIV H are both low and bits 11 to 15 are checked for overrange.

Board AB5 - Timing & B display dynamic store

Circuit diagrams : Chap. 7, Figs. 15 & 16

Circuit Sheet 1

64. The method of displaying frequency spectra on the TV screen and the operation of the A channel, B channel, and Graticule Channel Display Shift Registers (ADSR, BDSR, GDSR) are very closely related. Note that the ADSR and GDSR circuits are on AB6, but all three DSR's are considered here, since they are governed by common timing circuits which appear on this board. The Spectrum Display Area (SDA) on the TV screen is essentially a histogram, nominally 500 ordinates along the X, or Frequency, axis, and 250 levels along

the Y, or Amplitude, axis. The histogram can be overlain by a graticule, and, depending on the contents of the GDSR, the SDA can be made to represent graphs which are lin/lin, lin/log, log/lin, or log/log. Since it is desirable, for linear graphs, that the graticule should encompass an even number of ordinates, the DSRs are actually designed to hold data representing 502 ordinates on the X axis. In the A and B DSR's, one byte (8 bits, using 250 of 256 possible levels) is used for each ordinate.

65. The GDSR is used to hold data which represents the frequency (vertical) graticule lines only: the display of amplitude (horizontal) graticule lines is due to circuits on AB7. Also, the graticule is displayed at half the resolution of the spectra, and thus the GDSR is only half the length of the A and B DSRs. The GDSR holds just two bits of data for each graticule line position since it is only necessary to define a major, minor, dashed or no graticule line. The remaining two bits of the GDSR are used to hold marker data, and are discussed in the description for AB6.

66. The DSRs are provided with data feedback paths, so that the data may be read non-destructively in byte-serial form. The method and rates of clocking the DSRs are such that the data makes one complete rotation in the time the TV scan takes to pass across the SDA. On a given SDA scan line, the spectrum data for each ordinate is compared with the scan line number, and the result passes to logic which decides whether or not to light up the pixel (picture element) corresponding to the ordinate on that line. The graticule data is used directly to light pixels as the scan reaches the appropriate positions.

67. In order that new data may be written into the DSRs from time to time, they have multiplexers at their inputs. These select either data fed back from the DSR outputs, or new data which has been processed by AB4. They are under the control of the even/odd Write Pulse Generator (WPG), which allows one new byte to be written into each DSR during each SDA scan line period.

68. Each 8-bit DSR is formed by running 4-bit banks in parallel; the LSB bank which holds bits 0 to 3, and the MSB bank for bits 4 to 7. Each bank is comprised of two physical SRs, EVEN and ODD. New data is written to the EVEN registers of each bank simultaneously; similarly, the ODD registers. The EVEN and ODD pairs are written alternately. The register output multiplexers select, in parallel, the outputs of the EVEN pair alternately with the ODD pair, and the overall effect is thus of an 8-bit DSR whose length and clocking rate are each twice that of the physical SRs.

69. Each shift register is formed from three ICs, and since all four registers are similar, a description of the operation of the EVEN register of the LSB BANK can serve for all. The heart of the register is IC13 which is a 4-bit by 256 word device. This m.o.s. IC is driven by a high level bi-phase non-overlapping clock derived from the 6.25 MHz SHIFT REGISTER GATED CLOCK. The signal, with a pulse width of 70 ns, is applied to pin 4 (Φ1) and pin 11(Φ2). IC13's clock-to-data-output delay is such that it cannot directly recirculate data and therefore an extra register stage, IC14a follows whose output delay is very much shorter. IC14a consists of 4 D-type bistables and is clocked by 6.25 MHz SHIFT REGISTER GATED CLOCK. IC13 outputs are open drain and are made t.t.l. compatible by pull-down resistors R7a to d. Output is to multiplexer IC30.

70. Output multiplexers IC25 and IC30 are driven by the 6.25 MHz SHIFT REGISTER CLOCK signal and thus produce two streams of 4-bit data in parallel at a rate of 12.5 MHz. Input multiplexers ICs 26, 27, 28 and 29 are normally set to select recirculated data from the extra register stages of IC9 and IC14.

However, once every alternate TV horizontal scan (see above), the input multiplexers for the EVEN register pair, ICs 27 and 29, are made to select new data under control of the WE output from the Write Pulse Generator (WPG) to pins 1. Similarly, the ODD pair, ICs 26 and 28, are written due to WO once every other scan. Since data is written into the registers at a much slower rate than it is read, the WPG must keep track of where next to write data: the way it does this is described in a succeeding paragraph.

71. The high-level bi-phase clock for the shift registers is derived from the 6.25 MHz SHIFT REGISTER CLOCK signal by ICs 41, 42, 43 and 45. IC41 acts as a phase splitter, producing Φ1 from pin 5 and Φ2 from pin 6. The positive-going leading edges of Φ1 trigger monostable IC42a which emits 70 ns positive-going pulses. These are a.c. coupled to clock drivers IC43 and IC45 which convert the pulses to high level (+5 V, -12 V) to supply Φ1a and Φ1b for the shift registers. Similarly, Φ2 triggers monostable IC42b, and the 70 ns pulses which this emits are converted to Φ2a and Φ2b. The width of the Φ1a,b pulses is set by R4, Φ2a, b by R3.

72. Because the data in the DSRs must complete just one rotation during each TV horizontal scan, it is necessary to stop the DSR clocks periodically. This is done by the Gated Clock and Horizontal Mask Generator (GCHM). Although the A and B DSRs each hold 502 bytes of data to be sent to the display, they are actually 514 stages long. Hence, after allowing the DSRs to receive 502 clocks, the GCHM sets a mask which prevents the display of further "data", while the DSRs are given another 12 clocks. The GCHM then stops the DSR clocks completely, and awaits the next horizontal scan before resetting the mask, and re-enabling the DSR clocks. It should be noted that the DSRs operate over the whole vertical scanning cycle; in particular, the DSR clocks are NOT gated by any vertical retrace signals. The SDA, however, is defined with reference to vertical retrace (see below).

73. In order to maintain alignment between displayed data and displayed characters, the GCHM synchronizes its activities to the leading edge of HRTC (L) to pin 13 of IC40. Before HRTC goes low, the counter formed by ICs 16, 31 and 48 is held in the load state by IC40 pin 8, and START from IC16 pin 12 therefore is low. When HRTC goes low (beginning of horizontal retrace), it resets IC40 whose Q(L) output goes high. The counter is released from the load state and begins to count PHASED 12.5 MHz CLOCKS. Since the data display appears within an annotated border on the screen (i.e. the SDA), the counter is preloaded with a value such that when IC16 pin 12 goes high to assert START, an interval corresponding to the horizontal retrace period plus the chosen width of the border has elapsed. The rising edge of START clocks IC15b taking CLOCK EN low, which, via IC47b and IC46b produces the 6.25 MHz SHIFT REGISTER GATED CLOCK signal. Thus the DSR clock is started and data contained in the registers begins to appear at the output of multiplexers IC25 and IC30.

74. The same edge of START also clocks IC15a whose Q output supplies the X-direction video enable signal, XVIDEN. This is combined with other signals (see below) to enable the display of data within the SDA and so prevent spurious data appearing outside the SDA. When the counter has counted 502 clocks after START, all of the data in the DSRs will have been presented in the SDA. This state is detected by AND-gate IC32, and used to reset IC15a restoring XVIDEN low.

75. At this stage however, data byte 1 has not yet returned to register position 1 which it occupied before clocking began. This is because the data occupies only 502 of the available 514 positions. Therefore, the counter continues counting up to 514 clocks after START. This stage is detected by IC47a and used to reset IC15b. CLOCK EN therefore, goes high which stops the 6.25 MHz SHIFT REGISTER GATED CLOCK to the DSRs. Consequently, the shift registers stop with data byte 1 in position 1 again. At the same time, the rising edge of CLOCK EN clocks IC40a whose Q(L) output goes low, forcing the counter into the load state. This completes the horizontal scan cycle, and the whole circuit waits for the next HRTC falling edge.

76. A new data byte on the MULTIPLEXED PROCESSED DISPLAY DATA bus which is destined for the BDSR is first placed in B demultiplexing latch IC44, under control of B SEL to pin 11. IC44 outputs present the data to the NEW data inputs of the DSR input multiplexers. These normally select their recirculating inputs. However, once during every other SDA scan line period, the EVEN input multiplexers select their NEW inputs, so that the new data enters the EVEN register pair. On the alternate scans, the ODD input multiplexers select their NEW inputs, and the new data enters the ODD register pair. The signals controlling the input multiplexers are called Write Even (WE) and Write Odd (WO) and they are generated by the WPG.

77. The heart of the WPG is a 10-bit counter formed by ICs 1,17 and 33. The counter is clocked by the 6.25 MHz SHIFT REGISTER GATED CLOCK and thus receives 257 clocking edges per horizontal scan. Bit 9 output from IC33 pin 13 to the inputs of bit 9 (IC33 pin 4) and bit 0 (IC1 pin 3) allows the counter to divide by 257 and 258 alternately. Hence, on every other scan, the counter's transition to a given state will move one clock pulse later, relative to the immediately previous scan. This is used as a pointer to successive locations in the register pairs. The counter is configured to derive WD(L) from IC34 pin 6 which determines where data should be written in a register pair, and the odd/even output from IC33 pin 13 which points alternately to the ODD and EVEN register pairs. Since there are only about 320 horizontal scans per TV field, it takes the WPG the best part of two fields to put new data into all 502 DSR locations. However, if the WPG writes to a DSR location on every scan in both fields, it will cause wrap-around. To prevent this, for every two fields the WPG is resynchronized to the trailing edge of FRAME(L) to IC2 pins 2 and 4, and after 502 bytes have been written into the DSR, DREQ1 is used, which remains high to pin 5 IC34, to prevent any further WD pulses reaching the DSR. WD(L) from IC34 pin 6 is inverted and combined with odd/even output from IC33 pin 13 to form WO or WE which control the DSR input multiplexers.

78. What happens between the end of one TV frame and the start of the next, is explained from a point near the end of a frame when WD goes low for the 502nd time. Just after WD's falling edge, the 501st data byte is written into the DSR. On AB4, WD's rising edge clocks the DMA Request Latch (DMARL) making DRQ1 go high. The DMA controller on AB3 sends some data bytes, and eventually resets the DMARL so that DRQ1 goes low again with byte 502 placed in B Demux Latch (BDML), IC44. The DMA controller has now reached the end of process on channel 1 and will not send further data until reset during the next FRAME period. As WD goes low for the 503rd time, data byte 503 enters the DSR, and DRQ1 goes high. It will remain so for the rest of the frame when the DMA controller becomes inactive. DRQ1 high to pin 5 of IC34 prevents any further WD pulses from reaching the DSR, and also means that data byte 502 is left undisturbed in BDML IC44.

79. When FRAME goes low, the DMARL on AB4 is reset and held so until the end of FRAME and so DRQ1 goes, and is held, low. This does not affect the DSR, however, because the WPG is also reset by FRAME to IC2 pins 2 and 4, and so no WD pulses are produced in this period. Sometime during FRAME, the DMA controller is re-initialized by part of the processor's frame interrupt routine. Eventually, FRAME goes high again and the WPG is able to begin its first count cycle during the first horizontal scan of the new TV frame. This first cycle is of 258 states, and obviously the WPG will stop in its terminal count state as it receives only 257 6.25 MHz SHIFT REGISTER GATED CLOCKS during the scan. Thus WD is asserted and remains low, and WE holds the EVEN bank input multiplexers open, until the first clock edge of the second scan. At this point, data byte 502 is deposited in the final position of the EVEN bank, and since the WPG's first cycle is complete, WD goes high, thus setting the DMARL on AB4. The DMA controller now sends data byte 1 (for this frame) to wait in the BDML. The WPG's next cycle has 257 states, but it has already used one of the clocks of this (second) scan to complete the previous cycle. Therefore, another elongated WD pulse occurs, which, this time, results in the transfer of data byte No. 1 to the last position in the ODD bank on the first clock edge of the third scan. Simultaneously, DRQ1 goes high and the DMA controller soon sends data byte 2 to the BDML. The WPG now has a 258 state cycle again, with only 256 clocks of the present (third) scan left. Hence, terminal count does NOT coincide with the last clock edge of the scan, and a Orshort WD pulse occurs between the first and second clock edges of the fourth scan. Data byte 2 is thus written into the first position of the EVEN bank. Similarly, data byte 3 is written into position 1 of the ODD bank. This process continues until data byte 502 which concludes the sequence.

Circuit Sheet 2

80. On sheet 2 are seen the B channel Video Generator (BVG), which consists principally of the line draw and infill bright up operator, and the Line Count and Vertical Mask generator (LCVM). The vertical display mask, YVIDEN from IC40 pin 5 defines the top and bottom of the SDA. The LCVM consists mainly of a 9-bit ripple down counter formed by ICs 36 to 38 which is clocked by HRTC. When VRTC is asserted low to IC37 pin 11, the counter is parallel-loaded with 273. After the trailing (rising) edge of VRTC, which coincides with the start of the TV picture, the counter first counts down to 250. This state is detected and LINE 250 goes low from IC39 pin 11 which sets Vertical Mask Latch (VML) IC40b. This causes YVIDEN to go high, and the top of the SDA is defined. The counter continues down to zero, at which point LINE 0 from IC38 pin 13 goes low resetting VML IC40, and so defining the bottom of the SDA, YVIDEN and XVIDEN are combined with Box by AND-gates IC3a and b to produce the Data Display Mask signal TOTAL DDM. The latter has two functions: to define the SDA Window within the TV picture, and to provide blank boxes around characters which appear within the SDA.

81. The current SDA scan line number (250...0) is extracted from the LCVM as the lower 8 output bits of the counter and passed to the B Data Comparator (BDC), ICs 7 and 8 on the HIGH SPEED B CHANNEL DATA lines. The rising edge of the 12.5 MHz PHASED CLOCK is taken to the clock inputs of ICs 23a and b forming the Current Ordinate Latches (COL), and used to latch in the greater than (>) and less than (<) decision signals from IC8 pins 5 and 7 respectively. Use of the clock ensures that the BDC has enough time to reach its decision, resynchronizes the less than and greater than decision signals and results in every data byte being displaced right by one ordinate position on the display. Compensation for this is made near the beginning of each horizontal scan across the SDA. While XVIDEN from IC15 pin 5 (see Sheet 1) is low and CLOCK EN from pin 8 is high, the DSR waits with display data byte 1

present at its output. Since the 12.5 MHz PHASED CLOCK does not stop, the BDSL is repeatedly loaded with data byte 1, and the COL receives the same decision from the BDC on every clock edge. Then, as soon as XVIDEN goes high, and CLOCK EN goes low, the BVG paints up data byte 1 in the first ordinate position. However, data byte 1 will now be clocked into the BDSL once in the normal way, and will, therefore, also appear in the second ordinate position (see above). After this, operation returns to normal, leaving data byte 1 as the only double ordinate.

82. The BVG uses the BDC decisions stored in the COL and Previous Ordinate Latches (POL), IC22, to create either line draw or infill type display video. However, line 250 (top line of the SDA) is a special case since this line must be lighted over those sections where data amplitude is greater than top of SDA. B display amplitude limiter IC21 ensures that this happens for line draw displays. The algorithms for the two types of display are shown in Table 2.

TABLE 2 DISPLAY ALGORITHMS - AB5

Algorithm	COL	POL	250(L)	video
INFILL	D<L	x	x	off
	D>L	x	x	on
	D=L	x	x	on
LINE DRAW	D<L	D<=L	x	off
	D>L	D>=L	1	off
	D>L	D>=L	0	on
	D<L	D>L	x	on
	D>L	D<L	x	on
	D=L	x	x	on

Where D is data, L is line number and X is don't care

Board AB6 - Graticule & A display dynamic store

Circuit diagrams : Chap. 7, Figs. 17 & 18

Shift registers and video generator

83. For a description of the A channel Display Shift Register (ADSR) on sheet 1, and the A channel Video Generator (AVG) on sheet 2, refer to the description of the identical circuits on AB5. Note that the shift register clocks, $\phi 1$ and $\phi 2$, have their pulse widths set locally (IC35a,b), so as to avoid sending these critical signals across motherboard AA1.

84. The Graticule Display Shift Register (GDSR), on sheet 1, is also very similar to the A and B DSR's, but is only half the length (257 locations instead of 514) and half the width (4-bit words instead of 8-bit) of the former. Its output data rate is half that of the larger DSR's too, which means that vertical graticule lines are always two ordinate positions wide on the TV screen. Graticule information destined for the GDSR is placed in the Grat Input Latch, IC37, under control of circuits on AB4, but the data itself comes directly from memory (by means of the DMA controller) without passing through AB4. Since the GDSR works at half the speed of the other two DSRs, it needs to have new data written in only half as frequently. For this

reason its input multiplexer, IC23, is controlled on pin 1 by Write Odd (WO) only.

Vertical graticule and marker generation

85. On sheet 2 the GDSR output is synchronized with that of the ADSR and BDSR by latching it in IC21, using the PHASED 12.5 MHz CLOCK as the latch control to pin 9. The latched 4-bit data is then split into marker and graticule information, and each is decoded to generate various effects on the TV screen. The 2-bit graticule data from pins 10 and 15 is decoded by IC20 so as to give one of four possible effects in any vertical graticule line position (see Table 3). Dashed major lines are produced by combining the inverted output of the decoder with a suitable line count bit. Dashed and normal major graticule lines are combined into MAJOR VERT GRAT by IC4a before being sent to AB7. The minor line output is inverted to form MINOR VERT GRAT to AB7. On AB7 these vertical graticule lines are combined with the horizontal graticule lines, and then sent to the video mixer.

TABLE 3 VERTICAL GRATICULE DECODING - AB6

Input IC20		IC20 output pins				Effect selected
Pin 13	Pin 3	4	5	6	7	
L	L	H	H	H	L	No graticule line (default)
L	H	H	H	L	H	Minor graticule line
H	L	H	L	H	H	Major graticule line
H	H	L	H	H	H	Dashed major graticule line

TABLE 4 IC7 MARKER DECODING - AB6

Input pins			Active output pins								Effect selected
13	3	1,15	9	10	11	12	7	6	5	4	
L	X	L	L		L						No marker
H	X	H						L		L	Steady marker, odd ordinate
L	X	H					L		L		Steady marker, even ordinate
H	H	L				L					Flashing marker, odd ordinate
H	L	L		L							Flashing marker, even ordinate

86. Three bit data is decoded by 3 to 8 line decoder IC7 which selects the required marker effect. A marker can appear in any ordinate position and sits at the data value for that ordinate. Markers however, are available on only one channel at a time. The five possible effects decoded by IC7 are shown in Table 4. To supply the flashing marker, IC8 is configured to divide the VRTC signal by 4 to produce a square wave of about 12 Hz from pin 9 to set

the FLASH RATE for the flashing marker signal. The odd/even flashing ordinate markers are produced by a combination of the logic on the ODD/EVEN FLASHING MARKERS line (low to select even coordinates) and the level on the GATED 6.25 MHz line (i.e. half the ordinate rate). By this means selected alternate markers are flashed at a 12 Hz rate. The MARKER signal from IC5 pin 8 is gated with A/B MKRS which selects the channel to which the markers refer, and with A= and B= which determine the vertical positioning of the markers on the TV screen. Marker data is then clocked out from D-latch IC40a synchronized to the PHASED 12.5 MHz CLOCK to provide the MKR VIDEO signal for the summer on AB7.

87. Display status latch IC36 controls the main features of the TV display within the Spectrum Display Area (SDA). The processor writes control bits into the latch using pin 11. The resulting B VIEW ON and B INFILL ON are sent to AB5 where they perform the equivalent to the A view and A infill signals for this board.

DISPLAY

88. The block diagram for the display is shown in Fig. 3. The spectrum display area has 250 TV lines divided by the horizontal graticule into 10 major divisions of 25 lines. Each major division is able to display 2 rows of annotation characters. Each of these 5 x 7 dot characters is displayed within a 7 x 12 dot cell. Including the out of display area, the total number of cells is 66 x 24. The character generator is on AB7 and is a PROM which outputs 2 bits initially used for horizontal graticule type selection, and 6 bits to define each line of the character to be displayed. At the start of each line, the first character line generated defines the horizontal graticule; whether the graticule is a major one or a minor one is determined by bits 1 and 2 whose states are then held for the duration of the line. When the second or subsequent character line generated forms part of an annotation, the data configures 5 dots for the character plus a 2 dot intercharacter separator which is always blank. At the same time one of the unused graticule bits is used to control the blanking of all other video information within a character cell so that the character appears in high contrast.

89. AB7 contains the video mixer which controls the contrast of the various images making up the display. The mixer accepts 9 channels of video data and produces a single channel of mixed video for display. One channel, read-in bright-up, has fixed contrast and is used for the slower sweeps to enable the progress of the left to right sweep to be distinguished. The relative contrast for the remaining 8 channels in 3 groups is set for the mixer by the front panel INTENSITY controls for the A display, B display and graticule (which includes markers and annotating characters).

90. The board also contains the clock generators used for all data timing as well as for the production of the vertical field, and the horizontal line, synchronizing pulses.

91. AD1/1 via AT2 supplies the drive voltages to the cathode ray tube in order to display the information supplied by the c.r.t. controller and video mixer on AB7. Synchronizing signals to IC2,IC3 and IC4 supply the required horizontal and vertical electromagnetic deflection. Horizontal scanning, from left to right, is at a line rate of 15.625 kHz. Vertical scanning, from top to bottom, is at a frame rate of 48 Hz. Video modulation signals are applied to the c.r.t. cathode, and dynamic focus to anode 3. For protection purposes, AT2 (which supports the c.r.t. base) has spark gaps punched into it.

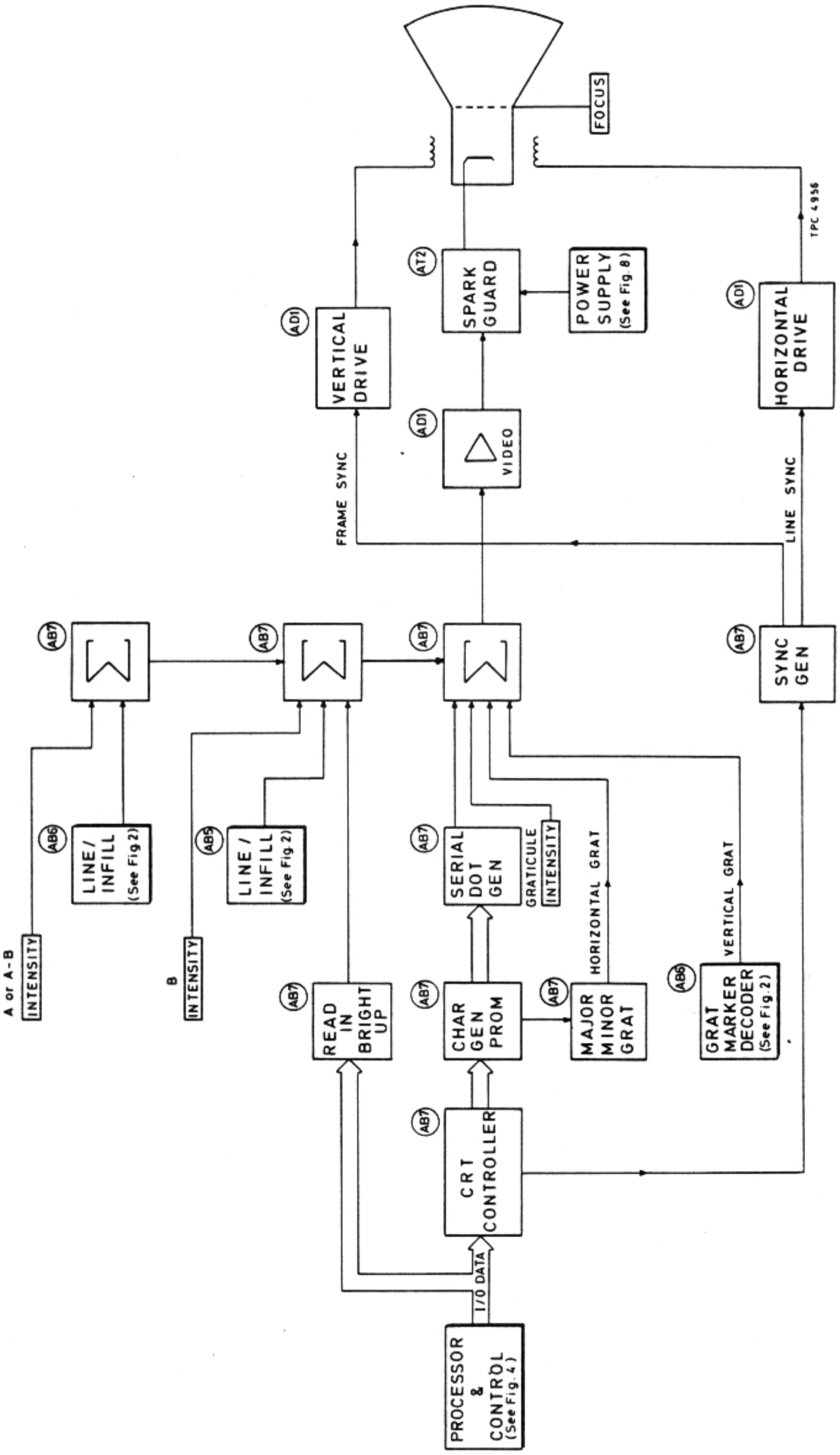


Fig. 3 Display block diagram showing main functions of boards

Board AB7 - CRT control, clock and video mixer

Circuit diagrams : Chap. 7, Figs. 19-21

Oscillator and p.l.l.

92. Sheet 1 shows the phase locked oscillator which generates the upper unit master clock using the lower unit master clock as reference. The oscillator is a modified Butler circuit built around TR13. Its output via TR16 is buffered and amplified to t.t.l. compatible levels by TR11 and TR12 and fed out as the 25 MHz CLOCK signal. This signal is also fed to the feedback loop via divider IC1 connected to divide by 5. The resulting 5 MHz is compared with the 5 MHz SYNC CLOCK for phase by EXclusive-OR gate IC2a whose output is connected to the inverting input of error amplifier and search oscillator IC42.

93. IC42 is a very low frequency Wien oscillator with feedback components R16, C78, R9 and C77. When out of lock, the square wave output from IC2a enables IC42 gain to be set by R11, R12 and R15 to just over 3 and so enable search oscillator operation. When the LC oscillator during its sweep attains lock, the IC42 inverting input becomes a virtual ground which sets the gain to 1 and halts search oscillator operation.

94. When during a fault condition or for servicing purposes the 5 MHz SYNC CLOCK is removed, integrator R7, C75 ceases operation causing TR15 to switch off and TR14 to switch on. This connects 5 V to the non-inverting input of IC42 causing the amplified output to varactor diodes D19 and D20 to hold the LC oscillator at its mid frequency and adjustment point. In this condition, the oscillator may be set to its 25 MHz operating frequency by means of C43.

Character generator

95. The character dot and clock generator on Sheet 2 determines the rate at which the dots forming the characters are sent to the screen. IC31a and b accept the 25 MHz master clock and divide it by 3 to produce the 8.3 MHz dot clock from IC31b pin 9. CHAR CLOCK, which is used as the timing reference by most of the circuits associated with the Cathode Ray Tube Controller (CRTC) IC15, is generated from the dot clock by counter IC30. IC30 also generates addresses for the dot multiplexer IC29. The data representing the dots for a given line within a particular character is latched in IC28 by CHAR CLOCK to pin 11, and emerges in serial form at the output of the multiplexer, IC29 pin 6. The CRTC uses the falling edge of CHAR CLOCK to pin 30 as its timing reference.

96. Following the falling edge of CHAR CLOCK, multiplexer IC29 inputs are addressed in the order 2,3,4,5,6,7,0,1. This, allied to the particular interconnections between latch and multiplexer, means that the dot data from the Character Gen (CG) PROM IC27 is sent to the screen in the following order: bit 2 (pin 11), bit 7 (pin 17), bit 6 (pin 16), bit 5 (pin 15), bit 4 (pin 14), bit 3 (pin 13), bit 2 (pin 11). Bit 2 is the inter-character separator which is always blank. Thus each character is 5 dots wide, and sits in a box 7 dots wide, so that there are two dot widths between adjacent characters. The two CG bits not used as dot data, bit 0 (pin 9) and bit 1 (pin 10), are used by the circuits which generate the amplitude graticule and character boxes.

Graticule generator

97. Amplitude (horizontal) graticule lines are controlled by special non-printing characters which are placed in the first position of each character row in the display area. Amplitude graticule generator operation for this purpose is examined at a time when IC33b pin 6 is high. Then, during the horizontal retrace period, the low HRTC output from IC15 pin 7 holds IC32a, IC32b and IC33a all in the reset state. Following the trailing edge of HRTC, CHAR CLOCK (inverted by IC10b) clocks IC32a to take its Q output high. This supplies a single clocking edge to IC32b and IC33a. IC32b latches the state of bit 1, and IC33a latches the state of bit 0 from character generator IC27. These states are thus held for the duration of a scan line, and are used by the video mixer to produce the horizontal graticule lines.

98. In any character position except the first within a given row, CG bit 1 from IC27 pin 10 controls the BOX signals from IC33b pins 5 and 6. These signals blank out all video information within a character cell except the character itself so that characters written in the spectrum display area are seen in high contrast. Bit 1 provides the data input for IC33b which is latched for every character. To subject the major and minor horizontal graticule lines to BOX, the Q(H) outputs of IC32b and IC33a are ANDed with the Q(L) output of IC33b. Before being sent off the board, BOX is gated with CHAR ON and EXTRA LINE by IC6b and IC20. This is done so that if the character video channel is disabled, blank boxes will not appear in the display area; similarly, during the extra line period, the display is not affected by BOX.

ERSD and ESPG

99. The Even Row Start Detector (ERSD) and the Extra line Sync Pulse Generator (ESPG) are present due to the following considerations: Firstly, the number of TV lines that the spectrum display occupies is chosen to be the largest within an 8-bit range, which is easily divisible by 2,5 and 10; so 250 is selected giving 10 major divisions of 25 lines each. Secondly, it is required to have two rows of annotation characters per major division. These requirements conflict, since the CRTC can (obviously) only display character rows which contain a whole number of TV lines. The solution used is to program the CRTC to use 12 TV lines per character row, and then to modify the operation using the ESRD/ESPG circuit. The circuit stops the CRTC for the duration of one line at the start of every other character row, and to insert an extra sync pulse so that the TV unit is unaffected.

100. During the vertical retrace period, the ERSD is held in a reset state by VRTC to IC11 pins 4 and 13; the Q(L) output of IC11a being low, that of IC11b being high. LC3 is inverted and goes high to the clock input pin 3 of IC11a at the start of each character row. After the end of VRTC, binary divider IC11a receives the clocking edge which sets its Q(L) output high. This, in turn, clocks IC11b whose Q(L) output goes low to assert EXTRA LINE. The signal stops CRTC IC15 by disabling its CHAR CLOCK input, while enabling ESPG IC23 by taking its resets low. After the end of the extra line period, the ESPG takes DETECT 76 low which resets IC11b, thus re-enabling the CRTC. The CRTC then proceeds to display two rows of characters (24 TV lines) in the normal manner. At the start of the odd-numbered character rows, IC11a also receives a clocking pulse, but this time it simply resets Q(L) output low

again. Note that the extra line does not affect the displayed characters in any way, since it is inserted between rows; similarly, the horizontal graticule lines are not affected, since they are generated within the character rows.

101. ESPG IC23, when enabled by ERSD, counts 67 character clock positive edges on its pin 1 (66 characters per row are displayed but the CRTC changes the line count one character clock before the beginning of a line, therefore an extra clock edge has to be counted), and then sets EXTRA SYNC (IC34 pin 12) active low for one character clock period. On the positive (trailing) edge of EXTRA SYNC (which, due to counting positive character clock edges, is half a character clock period later than a normal HRTC edge), the sync pulse generator (see below) emits an extra sync pulse. When the ESPG has counted on to 76 character clocks, i.e. counted out the HRTC period, it resets IC11b which re-enables the CRTC as discussed above.

DMA request disable

102. The CRTC's DMA requests are gated by IC8a with EXTRA LINE, because the CRTC simply holds the state of its outputs when the character clock is stopped. If this were not done, and DREQ from pin 5 happened to be asserted when the CHAR CLOCK stopped, the DMA controller would carry on transferring data, unable to know that the CRTC was ignoring it. IC8a prevents this by disabling the DMA request DREQ3 when the CRTC is not being clocked.

Phased clock generator

103. The Data Display Phased Clock Generator is used to obtain 12.5 MHz and 6.25 MHz clock signals whose phase is guaranteed at the start of every TV field. The phased signals are used by the Display Shift Registers on AB6 and AB5, which must have clocks of known phase in order that data is entered in the correct sequence.

104. IC5a produces a fast synchronized version of VRTC, the trailing edge of which from pin 5 is used to indicate the start of the field. IC3a divides the master clock input by two, supplying 12.5 MHz unphased to the rest of the instrument on its Q(L) output, and to the phasing circuit on its Q(H) output. At the start of a field, IC4b is clocked and latches the state (and thus the current phase) of the 12.5 MHz signal to its Q(L) output which is then used to control pass/invert gate IC2b. The latter is supplied with 12.5 MHz at its other input, and therefore its output from pin 3 is 12.5 MHz of fixed phase which is sent to AB5 and AB6. IC3b also receives the phased 12.5 MHz signal and divides it by two to supply 6.25 MHz to the phasing circuit formed by IC5b and IC2c. This operates in the same way as discussed above, producing 6.25 MHz of fixed phase at the output of IC2c.

Sync pulse generator

105. The main sync pulse generator on Sheet 3 produces HRTC, VRTC, HSYNC and VSYNC using VRTCS HRTCS and EXTRA SYNC. VSYNC from monostable IC21b is the vertical (field) sync for the TV unit, and has a pulse width of about 160 µs. HSYNC from monostable IC21a is the horizontal (line) sync and is about 4.7 µs wide.

106. At the start of every vertical retrace interval, the leading edge of VRTCS is differentiated by IC9c and C56 to produce a narrow negative-going pulse. This is used to reset, via IC22d, the Horizontal Sync Trigger Bistable (HSTB), IC19b, thereby avoiding a possible power-up lock in the loop formed by IC19b, IC7d and IC21a.

107. HSTB IC19b and Extra Sync Trigger Bistable (ESTB) IC19a are used to obtain the OR function of the positive-going edges of HRTCS and EXTRA SYNC at the output of IC7d. This is used to trigger HSYNC pulse generator IC21a, which would otherwise be difficult since HRTCS remains high during the whole extra line period. ESTB IC19a is reset by HRTCS when next it goes low after an extra sync pulse has been generated, while HSTB IC19b is reset by HRTC, the inverted version of HSYNC, from IC21a, and by VRTCS as noted above.

Read-in bright-up

108. Read-in Bright-up is used on the slower sweeps so that the user can more easily see how the sweep is progressing. The visible effect is of a slight brightening of an increasing portion of the spectrum display, starting from the left. The edge between the brighter and normal parts indicates the ordinate being read at the time. For the following description, it is assumed that bright-up is enabled, i.e. IC13a pin 1 is high.

109. The processor loads sweep position latch IC26 using CS18, when ready, with the ordinate number which represents the current read-in position. This is loaded into the bright-up down counter, IC24 and IC25, on every TV line using HRTC. Simultaneously, HRTC sets the Q output of IC12b high. When the TV line scan reaches the spectrum display area, DDM (Data Display Mask) goes high to pin 2 IC13a, which makes READ-IN BRIGHT-UP high, and the SR CLOCK starts to decrement bright-up down counter IC25. Thus, the spectrum display is brightened from the left side. When the down counter passes zero, it clocks IC12b which sets its Q output low, and takes READ-IN BRIGHT-UP low again. Outside the spectrum display area, the output of the down counter has no effect because of DDM. As the processor updates the sweep position latch, IC26, the brightened region is seen to expand from left to right across the spectrum display.

Video mixer

110. The video mixer accepts nine channels of t.t.l. level video data and produces a single channel of mixed video of 0.5 V p-p maximum. The READ-IN BRIGHT-UP channel has fixed contrast level, but the other eight channels have variable contrast, and are grouped as follows:-

CONTRA 1(A)	:	A INFILL, A LINEdraw
CONTRA 2(B)	:	B INFILL, B LINEdraw
CONTRA 3(G)	:	MAJOR graticule, MINOR graticule, MARKER, CHARacters

The contrast level of each group is controlled by an INTENSITY potentiometer on the front panel. The relative contrast level of the members of a group is fixed by the resistive divider which connects each channel to its contrast control.

111. The operation of the A INFILL channel, which is representative of all other channels (except READ-IN BRIGHT-UP), is discussed next and is assumed to be the only active channel. The contrast control voltage appearing on CONTRA A1, say V1, is converted to the required level, V2, by the divider R30, R31

and R32; hence the cathode of D1 is held at V2. D1 compensates for changes in TR1's Vbe with temperature, and C50 decouples the base voltage to prevent TV field-synchronous variations in displayed brightness due to the transistor switching. The voltage at the base of TR1 is about V2 + 0.6 V, so its emitter voltage is very nearly V2. Thus, when A INFILL is high, a known current will flow in R35 and R34. Consequently, TR1's collector voltage, V3, is established, and the 'Soft Clamp', D2 and R36, holds the output of the Video Summer at about V3 (cold end of R110).

112. The 'Soft Clamps' give the Video Summer a non-linear characteristic: however, two inputs of nominally the same level will not result in an output of twice that level. This limits the dynamic range of the video signal sent to the TV unit, and produces a more pleasing display than results if the levels of the various channels are simply added. The effect is rather like overlaying transparencies.

113. The mixed video passes to the Output Buffer, TR9, which reduces the amplitude of the signal to about 0.5 V p-p max. (so that the TV unit is not over-driven), and presents it at a suitably low impedance. The speed-up capacitor, C63, is present so that narrow horizontal and vertical lines may have the same apparent brightness.

114. The READ-IN BRIGHT-UP channel, TR10, has fixed contrast, its level having been chosen so that it is clearly seen when active, whatever the levels of the other channels. The remaining channels all operate in the same way as the A INFILL channel, described above.

Board AD1/1 - Display drive & Board AT2 - CRT base

Assembly AD0 - CRT

Circuit diagram : Chap. 7, Fig. 28

Summary

115. The display p.c.b. AD1/1 and associated p.c.b. AT2 provides the drive voltages to display the information generated by the c.r.t. controller and video mixer on AB7. Electromagnetic scanning is employed to generate a 325 horizontal line, non-interlaced raster, every 20.8 ms on a 19 cm c.r.t. with video modulation applied to the cathode. AD0 consists of the c.r.t. and deflection yoke assembly with associated wiring. AD1/1 contains six discrete sections:

Voltage regulator

116. IC1 regulates the +14.5 V supply input and provides +11.5V (±0.3 V) to AD1/1 when the display is enabled. Should the display be required to be disabled, then TR1 clamps the voltage adjust pin of IC1 to ground, reducing the supply to the board to +1.2 V. R18 bypasses IC1 to maintain the c.r.t. heaters at +7.5 V while AD1/1 is in standby; this reduces warm-up time when the display is re-enabled.

Video amplifier

117. The video signal from AB7 arrives on AD1/1 (TP17) at +3.5 V p-p positive-going with respect to ground. After attenuation by R4 and R5, the signal is a.c. coupled to the video buffer TR3 and amplified by the cascode amplifier

TR4 and TR5 to give 35V p-p negative cathode drive with respect to black level set by R17 to around +70 V (depending upon the c.r.t. gun characteristics). D2 conducts during the vertical retrace period, blanking the display to avoid vertical retrace lines appearing on the raster. TR2 clamps the input to ground during horizontal retrace, restoring the d.c. level at the input and preventing black level shifts due to display content variations.

Vertical drive

118. IC2 handles the whole of the vertical drive circuitry, taking the vertical retrace input at TP9 and producing a high output, distortion corrected, saw-tooth current and driving the vertical deflection coils directly. R45 adjusts the display height and R53 the top/bottom linearity balance. At TP10 the +11.7 V supply is allowed to rise to +23 V during vertical retrace supplying IC2 with the required high boost voltage for the output stage in the device; this signal is also used to blank the display during this time by raising the emitter of TR4. A small sawtooth voltage at TP13, generated across R55, is used to provide the vertical component of the dynamic focus correction after shaping by TR6.

Horizontal drive

119. The horizontal retrace pulse at TP11 is inverted and level shifted to trigger monostable IC3 on the rising edge of the pulse. IC3 retimes the retrace pulse and modifies the frequency of the astable oscillator IC4 causing it to lock to the frequency of the incoming pulses. R61 adjusts the phase relationship of the drive from IC4 to that of the retrace pulse by varying the pulse width generated by IC3, thereby giving control over the horizontal position of the display information at TP17 relative to the raster. The network following IC4 shapes the base drive to TR11 effecting a rapid turn-on and turn-off ensuring efficient switching of the horizontal output transformer T1 and deflection assembly. During flyback, the rate at which the voltage at the collector of TR11 is allowed to rise is taylored by the resonant circuit formed by C38 with the primary inductance of T1 and the horizontal deflection inductance. This controls the retrace period and sets the level of the supplementary supplies. TR11 collector voltage at TP12 also drives the black level clamp, TR2, during the 8.2 µs retrace period. The amplitude of the sawtooth deflection current passing through the horizontal deflection coils is modified by the series inductor L1 and the saturable inductor L2 linearizes the sweep. R73,R74,C42 and C43 are damping networks to reduce ringing after retrace.

Supplementary supply generator

120. T1 generates the supplementary supplies for the c.r.t., video amplifier and dynamic focus circuits. Autotransformer action produces a 25 V boost rail smoothed by C36 and during flyback, four further voltages are generated and rectified vis. +11 kV, +540 V, +90 V, -235 V. The Vg2 potential for the c.r.t. at TP8 is derived from the +540 V supply by potential divider R37 and R38.

Dynamic focus

121. The dynamic focus system maintains uniform spot focus as the c.r.t. beam is deflected from the centre of the screen towards the edges. This is effected by modulating the preset d.c. focus potential with an a.c. coupled parabolic waveform correction signal derived from the two deflection circuits. The vertical parabola is produced from the sawtooth generated across R55 by

amplifying and shaping circuit TR6, R22-28 and C8-10. This waveform is mixed with the horizontal parabolic waveform at TP14 into the cascode amplifier TR7 and TR8 to produce a 350V p-p modulated correction signal at TP15. This is coupled by C13 to the focus potential set by R39.

AT2

122. AT2 supports the c.r.t. base socket and has spark gaps punched into it to protect the semiconductors on AD1 in the event of a high voltage flashover inside the c.r.t. Resistors in series with the electrodes in conjunction with circuit capacitances on AD1 limit the voltage risetime of any transients generated during flashover to a safe value.

PROCESSOR AND CONTROL

123. When a front panel push-button is pressed, AB1 causes a processor interrupt (see Fig. 4). The processor responds by decoding the keyboard data from AF1 to determine the position of the button within an 8 x 8 matrix. The button position defines the function which is then acted upon by the processor. Data is routed out to the front panel by the processor to illuminate the annunciator l.e.d's. Direction of data is determined by a two-way buffer between the quiet data bus to the front panel and the I/O bus to the processor and memory. The purpose of the quiet data bus is to free the bus wiring in the keyboard area from the normally continuous trains of pulses from the processor area. Operation of the SET REF FREQ control on AZ1 similarly causes processor interrupts from AB1 and these indicate direction of movement to enable the frequency to be adjusted.

124. Parallel to serial conversion of the housekeeping data between the display unit and the r.f. unit is by means of the AB1 USART. This converts parallel data from the processor into serial data for transmission to the r.f. unit, and receives serial data from the r.f. unit for conversion to parallel data for the processor. The data is conveyed by a 20 mA current loop. Also on AB1 is the master interrupt controller and the GPIB interface. The interrupt controller manages 8 interrupt request lines and assembles the requests into priority order before communicating with the processor. The GPIB interface performs the talker and listener functions for the instrument to enable it to form part of a system acting under the direction of a controller. The instrument GPIB address is set on 5 slider switches on the rear panel. Connections to the GPIB and address switches are all made via AR1.

125. The central processor and the DMA controller on AB3 share the processor address and data buses. The DMA process allows the peripherals on the I/O bus to read or write directly from memory without involving the processor. Main memory is held in 896 K of EPROM while 16 K of RAM is used for scratchpad purposes which includes 4 K used for the A, B and A-B displays as well as for screen annotation. All data transfers between the processor and the memory and I/O data buses are via 2-way buffers. These prevent processor activity from appearing in the memory and peripheral areas. Address lines are decoded on both AB3 and AB1 to provide the chip select signals used to select the required functions. The slave interrupt controller on AB3 complements the master on AB1.

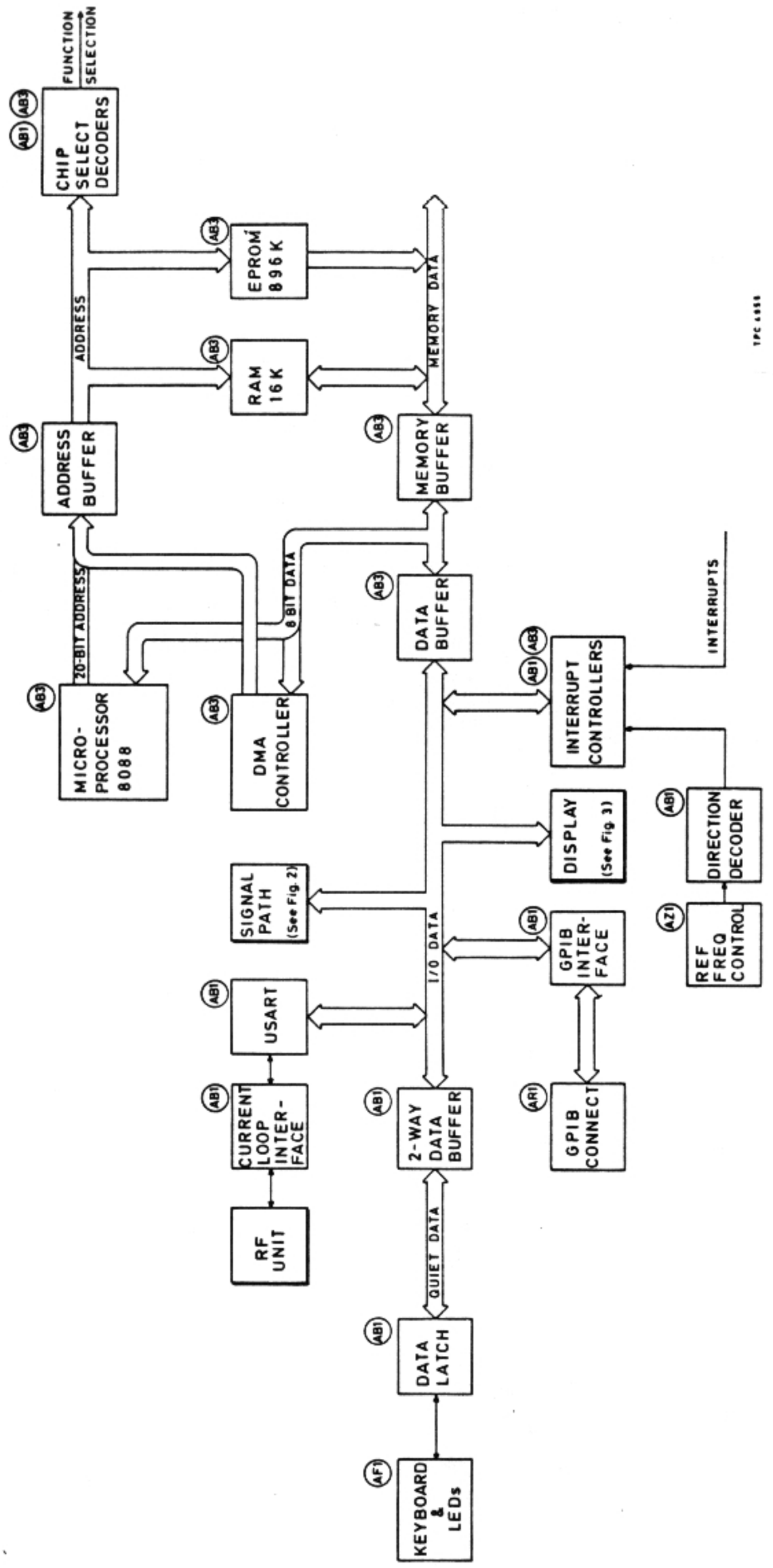


Fig. 4 Processor and control block diagram showing main functions of boards

Board AB1 - I/O & keyboard communication & Board AR1 - GPIB connector

Circuit diagrams : Chap. 7, Figs. 6 & 7

126. Board AB1 contains the keyboard interface, the USART for communication with the r.f. unit, the processor master interrupt controller and the GPIB interface.

Keyboard inputs

127. When a push-button on the front panel keyboard AF1 is pressed, the inputs to AB1 consist of a negative-going signal on the KEY PRESSED line and the push-button identity on the KD0 to 5 lines. The former signal is taken to the key debounce circuit while the latter is applied to latch IC24. The debounce circuit comprises dual multivibrator monostable IC16 and dual bistable IC1. These cater for the different settling times of the Schadow switches at make and break. When a button is pushed resulting in KEY PRESSED, the falling edge to pin 1 IC16a triggers the monostable which produces a negative-going pulse of 5 ms duration (the debounce time for make). At this time IC16b is unaffected by KEY PRESSED since its A input on pin 9 is held high by IC1a output pin 5. At the end of the pulse, IC1a is clocked taking its output pin 5 low. This has two affects. It sets IC1b Q output high, which signal is sent as KEY to the slave interrupt controller on AB3. And to IC16b pin 9 it enables the monostable to be triggered on pin 10 by the next positive edge to appear on the KEY PRESSED line; thus IC16b can detect when a button has been released. When so triggered IC16b produces a negative-going pulse of 20 ms duration (the debounce time for break). This sets IC1a output high and clocks IC1b whose Q output goes low i.e. KEY goes inactive again.

128. When KEY goes high from the debounce circuit it latches the 6-bit key code from AF1 into IC24. Two of the input bits are preset so that an 8-bit word is read from the latch by the processor when it takes CS20 low. Similarly, the bit pattern for l.e.d. illumination is latched into ICs 22 and 23 when CS1A or CS1C is taken low respectively. Latch outputs feed to the l.e.d's via the current limiting resistors R17 and R18. The direction of the data flow between the I/O data bus and the quiet data bus to the keyboard is controlled by the two-way buffer IC21. This is enabled only when one of the CS1A, CS1C or CS20 signals is asserted low. Data direction is determined by the IORD line; for a read operation this line is taken low.

Set ref. freq. control

129. The direction detector for the SET REF FREQ control receiver quadrature outputs from shaft encoder AZ1, and produces pulses on one of two output lines depending upon the direction in which the shaft is turning.

130. The output pulse trains from the encoder arrive at IC14c: let them be X to pin 9 and Y to pin 10. Y is used as the reference phase and is also connected to IC14b pins 4 and 5. When an edge occurs due to movement of the control, a delay is caused by R15, C25 so that pins 4 and 5 are momentarily logically opposite. The trailing edge of the resulting narrow pulse triggers monostable IC13a whose output on pin 13 enables IC15b and IC15c with a window pulse of about 2 µs duration. If X leads Y, then IC14c pin 8 will always be low during the window period, and negative-going pulses will appear at output pin 3 of IC15c. Conversely, if X lags Y, IC14c pin 8 will always be high

during the window period, and negative-going pulses will appear at output pin 6 of IC15b. The pulses from IC15b and IC15c will have the same duration as the window pulse but at twice the frequency of X and Y. The output from IC15b is used as SH UP (IR5) and that of IC15c as SH DOWN (IR4), when they are sent to interrupt controller IC6. An example of operation is shown in Fig. 5.

Display enable

131. When either CS10 or IOWR return high (i.e. when the data has settled), display enable latch IC20 is clocked to latch out c.r.t. control signals DISPLAY ENABLE and CHAR ON. The former signal to AD1 turns on the TV unit, while the latter enables the character data channel in the TV mixer on AB7.

Baud rate generator

132. An input from AB2 at the microprocessor clock rate of 6.25 MHz is divided by 10 by IC12a whose output takes two paths. One path is to IC12b for further division to supply the 125 kHz synchronizing pulses for AC1. The second path is to baud rate generator IC11 which divides the 625 kHz input by 4 to provide the 156.25 kHz transmit/receive clock for USART IC19.

Inter-unit bus USART

133. IC19 is a USART (universal synchronous/asynchronous receiver/transmitter) operating at 9600 baud and performing asynchronous data control between display and r.f. units. It accepts data from the processor in parallel format and converts it into a serial stream for transmission to the r.f. unit. Simultaneously, it can receive serial data from the r.f. unit and convert it into parallel format for the processor. It is interrupt driven and signals to the processor whenever it can accept a new character for transmission or whenever it has received a character from the processor. The processor can read the status of the USART at any time.

Operation

134. At initialization, the processor addresses IC19 by taking chip select line CS0B low then setting A0 to the C/D input high and the write (WR) line low to send a set of control words on the data bus. These define the operating format. Subsequently, a high RESET pulse can force the USART into an idle state to enable a new set of control words to be written in.

135. Serial housekeeping data is clocked in and out of IC19 at the 9600 baud rate derived from the 156.25 kHz input to pin 9. Serial input data is assembled in a receive buffer within the IC and, when the character is complete, RXRDY pin 14 takes the IR1 line high to interrupt controller IC6 to request a processor interrupt. If, however, the assembled character is a Break instruction, it is BD pin 16 instead which requests the interrupt via the slave interrupt controller on AB3/1. When ready to read the character, the processor addresses the USART using the CS0B line, then takes C/D and RD (read) low and accepts the data on the I/O data bus.

136. When able to accept a character for onward transmission to the r.f. unit, the USART takes TXRDY pin 15 high to request an interrupt on the IR0 line to IC6. When ready with a character, the processor places the data on the bus, addresses the USART on the CS08 line, then takes the C/D and WR lines low. The character is accepted by a transmit buffer within the IC and then serially clocked out on the TXD pin to the 20 mA current loop.

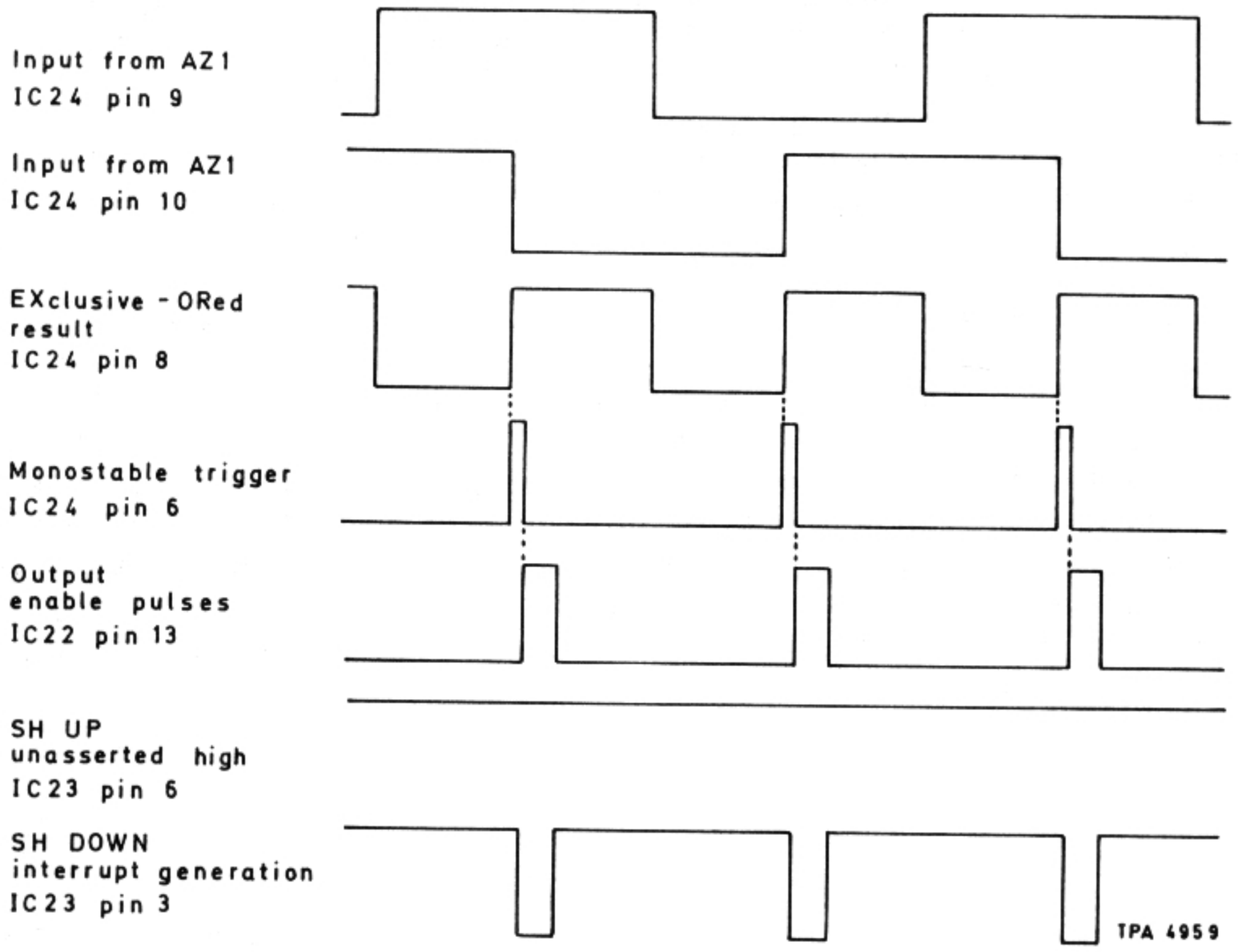


Fig. 5 SET REF LEVEL control direction detector operation. Example shows down movement - AB1

Chip select decoding

137. The 2 to 4 line decoders IC8a and IC8b decode address lines A1 to A3 to form the chip select signals for the GPIB transceiver and address reader as well as for the USART.

Status GPIB address reader

138. Tristate buffer IC5 which is enabled whenever CS0A and IORD are asserted low, performs a dual function. It provides 5 bits of the GPIB address used by GPIB transceiver IC4 for instrument address recognition, as well as providing two status bits. The instrument GPIB address is configured by the user on the 5 switches forming switch bank SA on GPIB connector board AR1. The two status bits are provided by HOT which conveys temperature sensing information from the power supply and EXT STD which is asserted low to indicate that an external frequency standard is connected to the r.f. unit in use.

Interrupt controller

139. Master interrupt controller IC6 manages 8 interrupt requests on lines IR0 to IR7 which are passed in priority order on the INT line to the processor. At initialization, IC6 is enabled by chip select line CS0E and, in conjunction with command select line A0, IOWR (write) is asserted low to allow an initialization command to be written in from the I/O data bus. Amongst its other functions the command configures the interrupt priority levels so that, for this instrument, IR0 has the highest and IR7 has the lowest priority. At a later stage, IORD (read) may be asserted low to read the status and then WR asserted to change the priority or to mask off an interrupt request line.

140. When an interrupt request occurs, IC6, unless engaged with a higher priority interrupt, passes on the request to the INTR input of the processor on AB3. On receipt, the processor completes its current instruction then acknowledges the interrupt by sending a low INTA pulse. This sets a buffer on AB3 for data input as well as being received by the interrupt controller on the INTA line. IC6 sends a call instruction back to the processor which responds by sending two further INTA pulses. These enable IC6 to release its preprogrammed address onto the bus in the order low byte, high byte. The address contains a pointer to the area in memory holding the routine to service the interrupt.

GPIB interface

Operation

141. The function of IC4 is to provide communication between the instrument and the General Purpose Interface Bus (GPIB). The IC is a talker/listener which, in conjunction with the transceivers, implements all the necessary GPIB functions for the instrument. It is processor controlled and has capabilities which include data transfer, handshake protocol, talker/listener address recognition, service request and serial poll.

142. The interface takes care of data transfer as well as decoding control messages. Control messages and addresses are passed on the the data bus by means of the handshaking process with ATN asserted to differentiate them from data. Control messages such as SPE, SPD used for serial poll are decoded and the function carried out. The IC also performs address recognition. The data on lines DIO 1 to 5 is compared for equivalence with data set on the 5 rear panel address switches (SA on board AR1). When a possible address is recognized and providing certain other conditions are satisfied, the data on DIO lines 6 and 7 is decoded to determine whether the instrument is being addressed as a talker or a listener. When designated a talker, the interface transfers data from the processor by means of a talk handshake to listeners via an internal register to the transceivers configured to send. When designated a listener, data is received via the transceivers by means of the listen handshake and stored in an internal data register.

143. IC4 contains 16 registers (8 read, 8 write), 2 for data transfer the rest for interface control, status, etc. Address lines A0, A1 and A2 are used to select the required internal read/write register in conjunction with IORD and IOWR lines. Reading or writing then takes place when the CS00 line is taken low.

144. Data outputs and inputs are via buffers IC2, 3, 17 and 18 with the direction of data transfer controlled by the T/R1 line being taken high for outputs and low for inputs. Additionally, this line is used for the

handshake process. For example, a low on the line, after inversion by IC9a, enables the listener handshake signals NRFD and NDAC to be asserted low on the bus while reinversion by IC9b ensures that the complementary DAV talker function is simultaneously disabled. The sole function of T/R2 is to set the bus management EOI line low for reception or high for transmission.

General purpose interface bus

145. The bus, which is entirely passive, uses 16 signal lines to connect all units of a system in parallel. These lines are functionally sub-divided into data, transfer and interface management buses (see Fig. 6).

Interface management bus : Manages the orderly flow of data across the interface and consists of 5 wires which carry the following signals:-

Interface clear (IFC) : Sent by the system controller to clear all interfaces so that they set to an initial condition.

Remote enable (REN) : Sent by the controller to enable instruments to be placed under remote control.

Attention (ATN) : Sent by the controller to indicate that an address or command is on the data lines.

End of identify (EOI) : An instrument or controller signal sent to indicate the end of a message.

Service request (SRQ) : Sent to a controller by an instrument to indicate that it needs service (e.g. has data to pass).

Transfer bus : Co-ordinates the flow of data and comprises 3 lines which are used for the handshaking process, by which a talker or controller synchronizes its readiness to send data with a listener's readiness to receive data. The handshake signals are:-

Not ready for data (NRFD) : Asserted (low) by a listener when it is active and not yet ready to receive data. Set high to signal its readiness to receive data.

Data valid (DAV) : Asserted by a talker to indicate that the data it has placed on the data bus has settled and may be accepted.

Not data accepted (NDAC) : Asserted by a listener when receiving data. Set high as confirmation of receipt of data.

Data bus : Comprises 8 data input/output lines DIO 1 to 8 and is used to transfer the data (commands, addresses and instructions) in bit parallel, byte serial form.

Bus operation

146. A sequence of messages may be commenced by the controller asserting IFC on the management bus to set the interface to its initial condition. The controller then asserts ATN and designates which instruments are to be listeners by sending their listen addresses on the data bus. Similarly, the controller designates the talker (only one instrument may talk at a time) by sending its talk address. Upon the controller removing ATN the talker is

free to send data to the listeners by means of the handshake process. The talker concludes the sequence by EOI and this tells the controller to resume control. The controller may now switch the talker and all listeners into the inactive state by sending UNT (untalk) and UNL (unlisten) on the data bus before selecting the next participants.

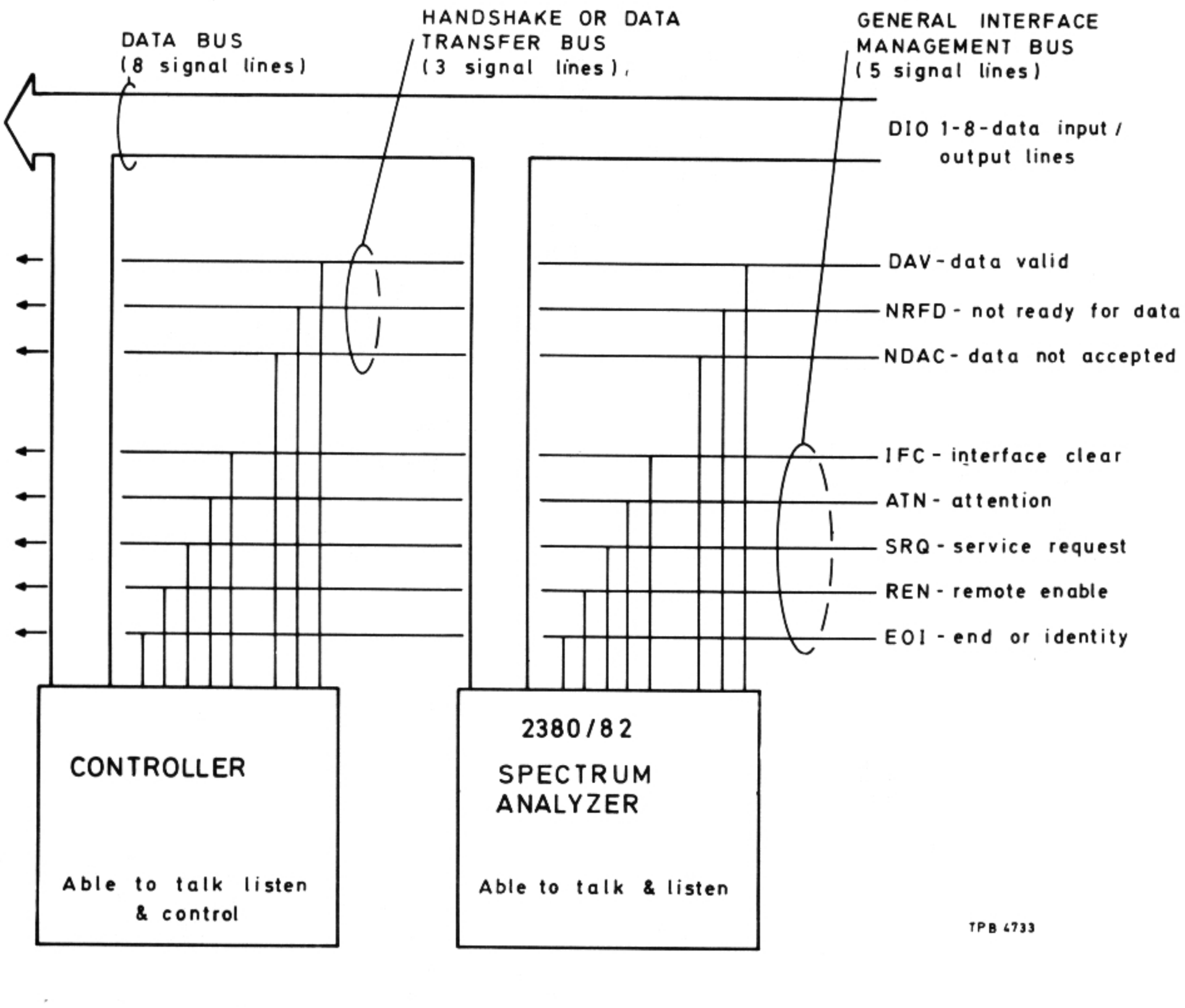


Fig. 6 General Purpose Interface Bus (GPIB) structure - AB1

Handshake

147. The handshake is used whenever data is transferred on the bus. When a signal is asserted the function indicated by the line is carried out, e.g. NRFD is asserted to signify the listener's unreadiness to receive data, and unasserted or removed when ready to receive data. Briefly, a typical handshake is as follows:-

(1) Talker (controller) places a byte on the data bus with DAV initially unasserted to show data is not yet valid.

(2) When all listeners are ready to receive data, NRFD is removed with NDAC at this time asserted.

(3) After a delay to allow data bus to settle, talker asserts DAV to show data is valid and may be accepted.

(4) Data byte is transferred, then listeners assert NRFD. When all listeners have accepted the byte, NDAC is removed to signify receipt.

(5) Talker removes DAV, listeners assert NDAC, and bus reverts to its initial condition ready for next data byte.

The handshake procedure is shown in Fig. 7.

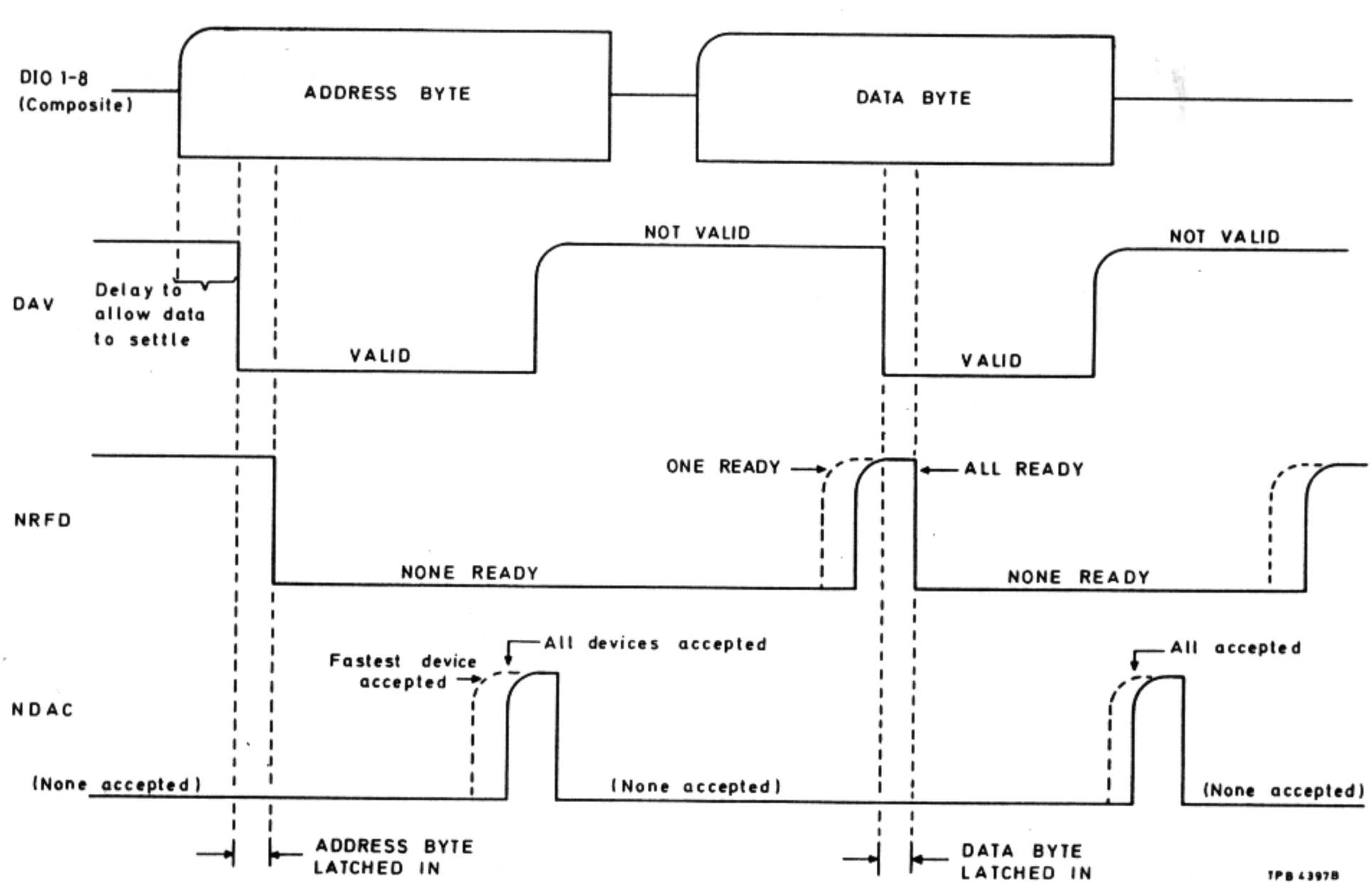


Fig. 7 Handshake procedure - AB1

Board AB3/1 - Processor, memory and chip select

Circuit diagrams : Chap. 7, Figs. 10 & 11

148. Board AB3 contains the microprocessor, the DMA controller and the RAM and EPROM memory banks.

Microprocessor

149. The central processor is an 8-bit Intel 8088 with 16-bit internal architecture. It uses a multiplexed data bus to accommodate the 20-bit address. This is split between the 8-bit high byte address bus, and the 8-bit data bus with the 4-bit upper address bus. Output lines A8 to A19 carry the high order memory address, with A8 to A15 valid for all bus clock cycles. Multiplexed input/output lines AD0 to AD7 carry the low order memory or input/output (I/O) address during the first bus clock cycle, and then carry data during the remaining clock cycles. ALE (address latch enable) is used to differentiate between data and address; when it is taken high the contents of the multiplexed data bus are treated as an address and latched by IC23. And since the upper address on lines A16 to A19 is only valid during the first clock cycle when ALE is active, this signal also latches IC4. IO/M is used to differentiate between an I/O and a memory address; when it is taken low the on-board memory is addressed. WR (write) and RD (read) asserted low enables the memory or I/O device selected by the address bus to be written into or read out from respectively. They also indicate that the data bus is available for a data transfer operation. For internal timing, IC1 supplies the CLK input with a signal at 1/3 of the frequency of the 12.5 MHz clock from AB2.

150. The 8088 has two interrupt inputs, INTR and NMI. Non-maskable interrupt NMI has the higher priority and is edge-triggered. This interrupt occurs at the conclusion of the FRAME pulse when enabled by data latch IC3b. Interrupts result in the transfer of control to a new program location. For NMI the processor automatically calls the required servicing routine. Interrupt request INTR is active high and is controlled in priority order by the interrupt controller on AB1. For INTR the processor responds with INTA (interrupt acknowledge), on receipt of which the interrupt controller sends the service routine address (vector) on the I/O data bus. To obtain this vector, INTA is also used to enable the I/O data bus buffer IC26.

Direct memory access (DMA) controller

Function

151. The primary function of DMA controller IC17 is to generate, upon a peripheral request, a sequential memory address which will allow a peripheral to read or write data directly from or to memory. DMA requests are serviced in priority order.

Internal registers

152. The DMA controller's internal registers are programmed by the processor when it selects the controller as an I/O device by taking CS4X low. The registers are then addressed on the A0 to A3 lines and data is written into them or read out from them when IOW or IOR is asserted respectively.

DMA operation

153. When the DMA controller receives a data transfer request from an enabled peripheral on one of the four DRQ lines, and it is in the idle state, i.e. not in control of the address and data buses, it asserts HRQ to request control from the processor. IC15 completes its current task then responds with HLDA to indicate that it has relinquished control. IC17 then addresses the appropriate area in memory. It outputs the most significant address byte on AD0 to AD7 which is strobed into latch IC24 by ADSTB and placed on the address bus by AEN. The least significant address byte is output on A0 to A7 to the address bus via buffer IC18. To enable the memory bank for a read or write operation, the controller takes the MRD or the MWR line respectively low. Finally, DACK is sent to the requesting peripheral as notification that it has direct access to the memory.

154. When enabled by DACK0 with IORD asserted low to IC21a, board AB2 reads 2 bytes from memory for its max and min output latches. AB4 is enabled to write 5 bytes to memory - 2 each for A and B displays and 1 for the graticule - when enabled by DACK1 with IORD asserted low to IC21d. When DACK3 is taken low, the c.r.t. controller on AB7 is enabled to read data in blocks for display.

Decoder

155. Quadruple 2 to 1 line selector IC16 decodes RD and WR into MEMR and MEMW respectively for memory read and write operations when its S input is taken low by the processor. When S is taken high, RD and WR are decoded to IOR and IOW respectively to enable the processor to read or program the DMA registers of IC17.

Buffers and latches

156. Both the processor and the direct memory access controller (DMAC) multiplex their data and address buses. When the processor has bus control, the upper and low byte parts of the address are latched out by IC4 and IC23 when strobed by the high ALE signal. The high and low bytes of the address feed directly to the address bus via buffers IC19 and IC18 respectively. And with the DMAC not in control, AEN is held low which enables buffer IC5 to complete the 20-bit address by outputting the 4-bit upper address. For a data transfer, ALE is taken low which disables the address latches.

157. When the DMAC has bus control, ADSTB is used as the strobe to latch out the high byte of the address from IC24. AEN is asserted high and this is inverted by IC20e to enable the latch as well as to select the preset upper address from buffer IC5. For a data transfer AEN is taken low to disable the address latch.

158. The data bus has two buffers in parallel, IC27 to the memory bus and IC26 to the I/O data bus. Each is enabled by a low on pin 19 only when its respective bus is read/written. For a write operation, pin 1 is taken high while for a read it is taken low.

159. The above simple scheme becomes slightly complicated under two circumstances. First, when the processor is programming the DMAC it sees the latter as being in the IO map, and since they are directly connected (i.e. on the same side of the I/O data bus buffer), the processor disables IC26 on pin 19 using the CS4X line to the DMAC in order to prevent possible bus contention. Secondly, when the processor wants to receive a vector from the

interrupt controller on AB1, which is on the I/O bus, it has to be able to 'force a path' through the buffers; for this reason, INTA from pin 24 of IC15 is combined with the other enabling/direction control signals for ICs 27 and 26.

Memory banks

160. The operating program is contained in 7 EPROMs (ultra-violet Erasable and electrically Programmable Read Only Memories) each of which contains 256 K bytes of memory. ICs 10 to 14 and 32 are directly controlled by IC7 which decodes the selection logic on address lines A15 to A18. IC33 is selected by the additional input of the A19 line to AND-gate IC22a. ICs 8 and 9 each contain 8 K bytes of RAM (Random Access Memory) used for scratchpad read/write operations. These are selected by IC6 which decodes A13 to A15 to select the required memory, and is itself enabled by A16 and A18. When the instrument is switched off the contents of these memories are lost.

Chip select decoding

161. ICs 30 and 29 perform chip select decoding for the IO map. IC29 is enabled during a processor I/O operation when AEN and IO/M are both low, and the binary address on the A4 to A6 lines is decoded to select 1 of 8 outputs. One of the outputs is used as an enable signal for IC30 and when IOEN also goes low for an I/O read/write the IC decodes the A1 to A3 address to select 1 of 8 outputs.

Interrupt controller

162. Slave interrupt controller IC28 can manage up to 8 interrupt requests on lines IR0 to IR7 and passes them in priority order on the SLAVE INT line to the master interrupt controller on AB1. The two interrupts managed are KEY to detect a keyboard button operation, and BREAK to detect a break message to the inter-unit USART. At initialization, IC28 is enabled by an output from chip select decoder IC29 and, in conjunction with command select line A0, IOWR is asserted low to allow an initialization command to be written in from the I/O data bus. The command may be used to configure the interrupt priority levels or to mask off an interrupt request line.

Board AF1 - Keyboard matrix and encoding

Circuit diagram : Chap. 7, Fig. 29

163. This board is mainly a static encoder for the 40 push-buttons which are arranged at the nodes of an 8 x 8 matrix. The code used to represent each button is derived from the node address; rows are numbered 0 to 7 and columns are numbered 8 to F hexadecimal. The code used to represent each button is derived from its node address, for example the dB button is coded A3H. Columns feed directly to decoder IC4 while rows feed to decoder IC1 via the 8 elements of ICs 2 and 3. With no buttons pressed, all the comparators' inverting inputs are held low by the elements of R2 connected to ground, while the non-inverting inputs are held slightly high by the potential divider formed by R4,R5. Consequently, the inputs to row decoder IC1 are held high as are all the inputs to column decoder IC4 due to the action of pull-up resistors R1. When a key is pressed, it shorts together a row and column of the matrix. This forms a potential divider from the respective elements of R1 and R2 causing the appropriate input lines to the decoders to be taken low. 8 to 3 line decoders IC1 and IC4 supply the l.s.b's and m.s.b's of the button

address respectively. Due to IC1 pin 5 being tied to ground, any input going low causes pin 14 also to go low and this feature is used to generate KEY PRESSED to AB1 for key debounce purposes.

164. The l.e.d's installed in some of the push-buttons have their anodes connected to the +5 V supply and their cathodes separately driven via selection logic from AB1.

Board AZ1 - Shaft encoder

Circuit diagram : Chap. 7, Fig. 30

165. This board forms part of the REF FREQ control. Its function is to indicate the direction of movement of the shaft of the control to board AB1. Power is supplied from AB1 on contacts 1 and 3 to two l.e.d's. These are optically coupled via a pierced disk mounted on the shaft to photo-detectors connected to contacts 4 and 5. By this means, as the shaft is rotated, quadrature pulses are generated for subsequent decoding in board AB1 to determine the direction and rate of movement of the control.

POWER SUPPLY

166. AC mains from the rear panel INPUT connector enters via a fuse in both the live and neutral leads and is connected by the front panel SUPPLY ON switch to the line filter on AC3 (see Fig. 8). A soft start circuit on AC1 follows which limits the maximum line current for 0.5 s after switch on. The LINE VOLTS SELECTOR on the rear panel changes the mains transformer primary tap for either 115 V or 230 V operation and reconfigures the AC1 full-wave rectifier in the 230 V position to a voltage doubler in the 115 V position. After smoothing, the h.t. supply of nominally ±170 V is fed through fuses FS1 and FS2 to the phase splitter and output switches operated by an SMPS controller. 12 V auxiliary power supplies the controller, provides the line trigger for the associated r.f. unit and, after regulation, supplies +5 V for the monitoring circuits.

167. The switched mode power supply controller on AC1/1 operates at 125 kHz in synchronism with the r.f. unit frequency standard. The current limit detector checks the supply current to the primary of the transformer used for d.c. to d.c. conversion in order to provide protection against an overload or a shorting of the secondaries. Protection is provided by the SMPS controller switch drive being inhibited. Additional protection is provided by the controller being reset, causing a soft start if possible, whenever AC2/1 detects an overload overvoltage or overheat condition, or when no r.f. unit is connected. A feedback line is used to control the switching duty cycle and hence the output power. A heatsink-mounted thermistor controls the speed of the cooling fan. If the instrument starts to overheat the processor causes a message to be displayed to that effect and, if the condition worsens a controller reset is generated. Rear panel l.e.d's illuminate on the occurrence of any of the above fault conditions.

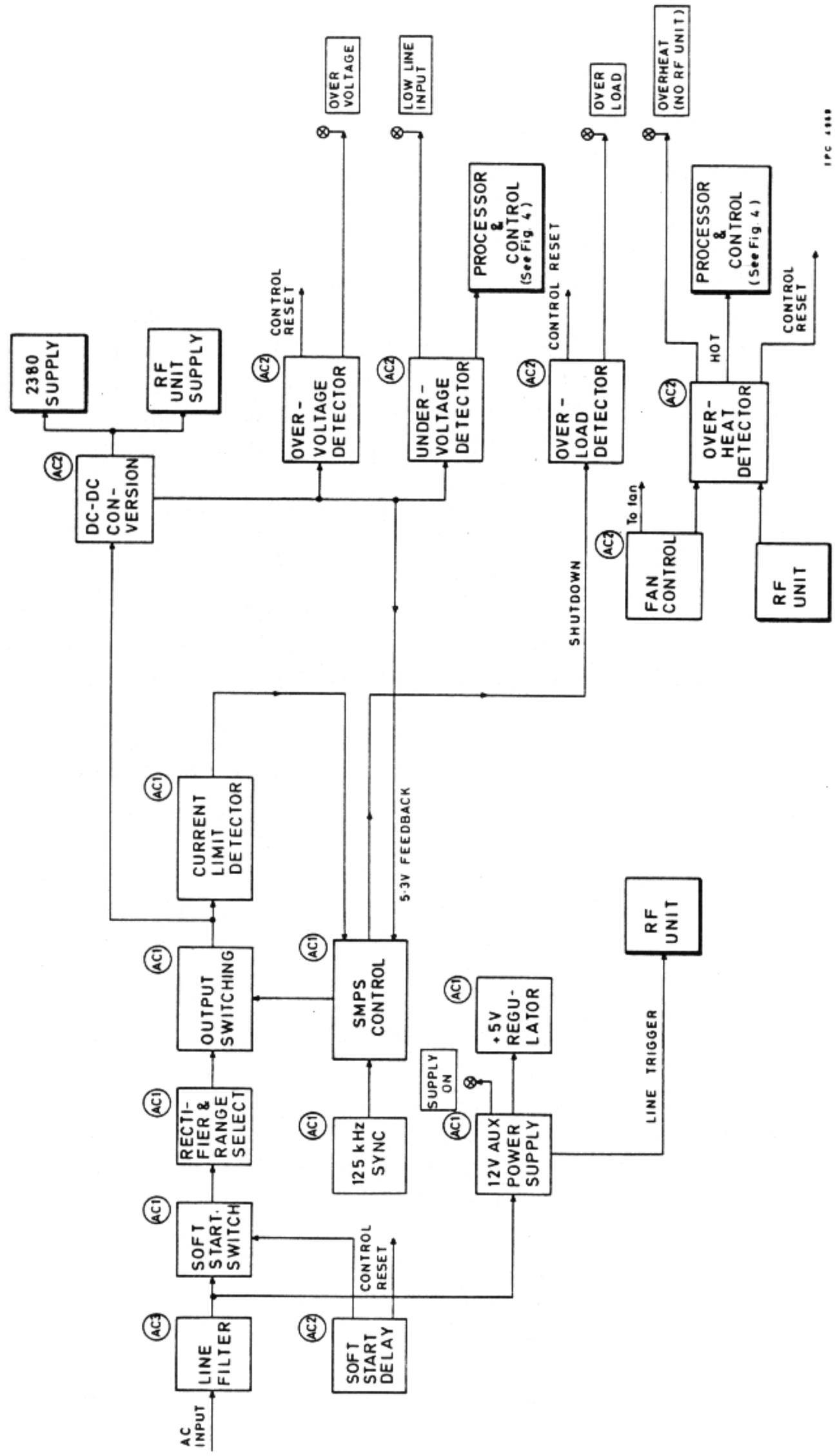


Fig. 8 Power supply block diagram showing main functions of boards

Board AC1/1 - Input control of SMPS & Board AC3/3 - Line filter

Circuit diagrams : Chap. 7, Figs. 25 & 27

General

168. AC1/1 consists of the high voltage switching circuits, the auxiliary supply and switching controller. Live and neutral from line filter AC3/1 is rectified to give a nominal +ve and -ve 170 V h.t. supply which is switched alternately by TR1 and TR2 into the h.f. power transformer on AC2/1 under control of IC2. The duty cycle on-time of both TR1 and TR2 is adjusted by IC2 to regulate the low voltage outputs of the supply against variations in line voltages and load currents by sampling one of the secondary outputs and comparing this to its own stable reference. Additional inputs to IC2 protect both the load and the supply from overload by sensing the output voltage and power transformer primary current. C1,C10,14 and 20 form part of the line filter, attenuating switching noise generated by the converter.

Soft-start

169. R1 and relay RLA form a soft-start circuit designed to limit the maximum line current taken at switch-on due to the capacitive load of the h.v. reservoir capacitors C2-5. A delay circuit on AC2/1 prevents RLA from being energized for approximately 0.5 s after switch-on. During this time C2-5 can only charge through R1. R1 limits the initial charging current to less than 3 A even under worst case conditions of maximum line input voltage and switch-on time (input waveforms at peak voltage).

170. After the soft-start delay, pin 8 on PLC is taken low and RLA energizes thereby shunting R1 which dissipates an insignificant amount of power during normal supply operation.

Rectifier and reservoirs

171. S1 selects either 115 V (105 V - 120 V) or 230 V (210 V - 240 V) line input voltage. It changes the primary tap on T1 and reconfigures D2 from a full-wave rectifier in the 230 V position, to a voltage doubler in the 115 V position maintaining an h.t. supply of nominally + and -170 V. R4 and R5 across capacitors C2-5 discharge the h.t. supply after switch-off while a relaxation oscillator C6, R6 and LP1 warns of the presence of voltages greater than 60 V across the h.t. rails; frequency, (between 1 & 5 Hz) is proportional to voltage. D3 and D4 protect the f.e.t's from high transient voltages by conducting in the event of either rail exceeding 220 V. FS1 and FS2 isolate TR1, TR2 and associated circuitry in the event of a fault which would draw heavy currents from the reservoir capacitors possibly damaging the p.c.b. L1 and L2 filter the h.t. lines of high frequency switching currents.

Auxiliary power supply

172. An auxiliary 12 V supply, T1, D7, C11, IC1 and C12 powers the control circuit and provides an isolated source of line frequency needed for the line trigger mode in the r.f. units. This 12 V line is further regulated to +5 V (+/- 2%) by IC2, TR3, R13, C13 and C15. TR3 buffers the 5 V reference from pin 18 of IC2, R13 supplies IC2's internal regulator while C13 and C15 provide decoupling of the supply lines. The stabilized +5 V is used on AC2/1 (via PLC pins 10 and 14) to supply the monitoring circuits.

Phase splitter and output switches

173. IC2 drives the two power f.e.t´s via T2 which functions both as an isolating element between the control electronics and line connected circuit and a phase splitter. During the first period of the switching cycle pin 13 is driven high (+12 V) while pin 16 is held at 0 V for time ´t´. During this period, TR1´s gate is driven 12 V positive while TR2´s gate is driven 12 V negative; consequently TR1 rapidly conducts as the gate potential rises above the f.e.t´s gate threshold of 2 V. The transition period is controlled by the time constant of R7 + R8 and the f.e.t. gate capacitance. While TR1 is on, current flows in the power transformer primary (T1 on AC2/1) via C9, a d.c. blocking capacitor, and T3 primary. Current is reversed when TR2 is on and TR1 is off in the second half of the switching cycle when IC2 pin 16 is at +12 V and pin 13 is held at 0 V for a second period ´t´. To ensure that simultaneous conduction of both TR1 and TR2 is prevented, diode D5 shunting R7, and D6 shunting R9 reduce the discharge time of the f.e.t. junction capacitance effecting rapid turn-off. Snubbers C7, R11 and C8, R12 damp any oscillation of the primary circuit during the time when neither TR1 nor TR2 are conducting.

SMPS controller

174. ´On´ period, ´t´, is dependant upon the feedback voltage from pin 15 of PLC. The variation of this as a result of line or load changes is attenuated by R19 and R20 and compared in IC2 with the +5 V reference. R19 gives a ± 300 mV adjustment around the nominal 5.35 V to accommodate tolerances in the +5 V reference and R20. The amplified and inverted difference voltage is compared again with a ramp generated by the internal oscillator in IC2 whose output controls the logic and output buffers such that, at the start of the switching cycle one output is enabled and remains active (+12 V) until the output level from the ramp generator is equal to the amplified error voltage whereupon the pulse is terminated. In this way, as the power supply output increases (leading to a reduction in the error voltage), ´t´ is reduced in duration which reduces the amount of power transferred to the secondaries. C19 and C21 with R21 and R30 in conjunction with the +5.35 V rail filter components on AC2/1 reduces the loop gain of the system above 150 Hz to maintain stability whilst giving an acceptable transient response.

175. Free running frequency of the oscillator is inversely proportional to the product of C18 and R14 and is approximately 120 kHz. When the supply is synchronized however, this is increased to 124.6875 kHz by means of the external SYNC input on pin 4 of PLC. The t.t.l. +ve going edge of sync. (at 125 kHz) is firstly a.c. coupled and differentiated by C22 and R27 and then clipped by D13 to clip negative transitions. TR4 is wire-ORed to the SYNC input of IC2 pin 12 and on driving this input low, discharges the timing capacitor, terminating the oscillator cycle prematurely and effectively synchronizing the controller by restarting the charging sequence. To stop spurious sync. inputs from upsetting the controller during power-up, a SYNC INHIBIT pulse, active for 930 ms after the supply is turned on drives TR5 into saturation and ground, any signals arriving at the base of TR4. By linking pins 2 and 3 on PLE, the external sync. may be disabled manually during the testing of the 2380 logic boards when the sync. integrity might be affected resulting in supply malfunction and shutdown.

176. Three methods are available to inhibit the controller, IC2 whilst in operation namely:- SHUTDOWN, RESET and CURRENT SENSE input.

177. The SHUTDOWN port, pin 8 of IC2, terminates the output drive when low and is wire-ORed with the output of the current sense amplifier output. It is used to drive the input of the overload sampler on AC2/1 in order to monitor overloads on the the p.s.u. and to shut it down if necessary.

178. The RESET input to pin 5 IC2 is driven from AC2/1 and when active (low) resets the controller. After 520 ms from switch-on, the soft start interval, the reset input is released and the controller itself executes a soft start whereby, under control of the soft start timing capacitor C17, the output duty cycle increases from zero until the error amplifier assumes control and regulation is maintained. This method of starting prevents supply output voltage overshoot which would occur at switch-on because of the delay inherent in the regulator feedback loop. This reset input is released as relay RLA is energized. R23 ensures that should the supply be switched on while PLC is disconnected, the controller remains reset until PLC is reconnected whereupon the supply soft starts safely.

Current limit detector

179. The Current Limit Detector, T3, R15-17, D11 and D12 protects the power f.e.t´s from damage from excessive primary current brought about by the shorting of any of the secondaries on AC2/1 or a general overload exceeding 250 W. T3 is a current to voltage transformer giving 2 V across R15 for each Ampere flowing in the primary. D11 and D12 rectify the signal while divider R16 and R17 give an input to IC2 pin 7 of 100 mV (the current sense amplifier threshold) at a primary current of 3 A. Under normal full load the primary current should not exceed 2.5 A peak.

Board AC2/1 - Output & monitors of SMPS

Circuit diagram : Chap. 7, Fig. 26

180. AC2/1 contains the power transformer, all l.t. rectifiers and smoothing components, output voltage monitoring, cooling control, and power-up sequencing.

Input and rectifiers

181. Seven l.t. supplies are produced directly from T1, and a further two, -5 V from the -8.5 V line and -12 V from the -14.5 V line. All outputs follow the same principle whereby a centre-tapped secondary is full-wave rectified by either two fast recovery diodes, for a single +ve or -ve output, or four diodes for a balanced +ve and -ve output.

182. The series R/C connection across each secondary forms a snubber to critically damp oscillations produced during switching by the junction capacitance of the diodes with the leakage inductance of the transformer secondaries. The square-wave output from the rectifiers is smoothed by a series choke and capacitors to ground with bleed resistors lightly loading the outputs to prevent them rising to an unacceptably high level should the supply be unloaded. The bleed resistors also ensure that any charge on the smoothing capacitors (especially in the case of the +80 V line) is quickly dissipated at switch-off.

183. D1 is a dual, centre-tapped Schottky rectifier mounted on a heat-sink, the temperature of which is monitored by a thermistor, R15, used to control the fan speed. R14 across the +5.35 V output loads this rail which is used as the feedback supply to the controller on AC1/1. Without sufficient load here, with the supply operating open-circuit, peak-detection at C1 will produce a sufficiently high feedback voltage to cause the controller to reduce the duty cycle to zero until the feedback decreases below +5.35 V. D2 prevents any high voltage transients on the output, by conducting at approx. 7 V, and acting as a fast over-voltage suppressor under possible fault conditions until the controller is shut down by the active over-voltage detection circuitry IC2b.

184. The auxiliary supply at +5 V from AC1/1 is decoupled by C29 and used to power the monitoring circuit on AC2/1. R1 and R2 with C30 provide a +2.5 V reference for use by comparators IC2.

Fan control

185. Fan speed is controlled indirectly by the temperature of D1 and associated heatsink. R15 is a negative temperature coefficient thermistor and in series with R16, which is normally connected to the -14.5 V line, produces a voltage at TP12 which is proportional to the temperature of the heaksink. This voltage is buffered by TR1 and drives the fan while D15 protects TR1 against reverse base emitter breakdown and D17 ensures that the fan has at least 13.8 V or 19 V applied to it (depending upon the setting of PLF) even under cold switch-on conditions when R15's resistance is high. C21 decouples the fan from the supply by providing the high current pulses required during commutation.

186. The voltage at TP12 is divided by R17 and R18 and is monitored by two comparators in IC2. IC2c's output goes low when the voltage at pin 10 rises above that at pin 11 (+1.5 V) set by potential divider R19, 22 and 23 corresponding to a voltage at TP12 of 4.8 V and a heatsink temp. of 80^{0}C. This output is taken via PLD to the processor and is used to warn the operator of an excessive rise in temperature in the instrument by means of a message on the display. Allowing the heatsink temperature to rise further, will result in the second threshold of +2 V to be exceeded and detected by IC2a. As IC2a's output drops, IC4b, an R-S latch, will be set and the supply controller will be shut down via the reset line, by IC5c. LED D25 indicates this on the back panel. A secondary function of the temperature monitoring circuit is to detect the absence of an r.f. unit power lead at switch-on and warn the user by resetting the supply and illuminating D25. Pin 28 SKA is normally looped through the power cable to -14.5 V in the r.f. unit to enable the temperature sensing circuit to function. Should this pin become open-circuit, then R51 pulls R16 up to the +14.5 V supply which activates the overheat comparator.

Voltage detection

187. The +5.35 V output is monitored by IC2b and IC2d. If the output exceeds 5.8 V then IC2b sets latch IC4c which resets the controller. D23 shows this. A secondary sense for over-voltage, D22 and R57, wire-ORed with the output of IC2b, detects a voltage on the -14.5 V line of less than -18 V again tripping the over-voltage latch. (This is in case the +5.35 V feedback line is affected i.e. D1 failing). To warn of possible instrument malfunctioning should the supply line be interrupted or fall outside the line input requirements (<95 V or <220 V), IC2d sets IC4a illuminating D24: LOW LINE INPUT. During power-up, IC2d buffered by IC5f, holds the reset inputs to the

instrument processor low until the +5.35 V line has stabilized and is wire-ORed to the reset circuits on the processor boards.

188. Line frequency input from AC1/1 is squared by IC6b and buffered by IC5e to be used by the r.f. units for triggering the sweep in line trigger mode. Also, the output from IC6b is used as the sampling period for the Overload Sampler IC7 whereby C37 and R29 differentiate the line frequency square-wave and after inversion by IC6e produce a 100 µs positive pulse to reset IC7 at line frequency. The Overload Sampler totalizes the transitions on the SHUT-DOWN line from AC1/1 and sets the overload latch, IC4d, if more than 127 pulses are received in 1 sampling period (2.2 - 22 ms depending upon line frequency). D26 gives a visual indication why the supply has reset. This arrangement protects the supply and loads against overloads (short circuits) without being susceptable to transient disturbances (during synchronization to the external sync. input for example).

Start-up sequencing

189. Two monostable circuits IC3a and IC3b provide start-up sequencing when the supply is first switched on. When the +5 V auxiliary supply is active, C22 charges through R26 and triggers the monostable outputs in IC3 to a high state. IC3a via IC6c and IC5b hold the supply controller RESET line low for approx. 520 ms during the soft start period and also resets the Overload and Overvoltage latches. After this delay, the soft start circuit on AC1/1 is bypassed and the converter begins operation. While the supply stabilizes, IC3b, via IC6a, holds the LOW LINE and OVERHEAT OR RF UNIT latches reset and inhibits the external sync. for a further 410 ms following the soft start delay.

PENPLOT AND RGB VIDEO (OPTIONAL)

190. D-A converters on board AB8 supply the drives for the X and Y axes of a pen recorder, with an additional signal provided to control the penlift operation (see Fig. 9). The RGB circuit outputs provide a red graticule, a green A display, a blue B display and a white display which is used for both markers and annotating characters. The horizontal and vertical synchronizing signals are combined for output on a single line. Provision is made for a composite video output for a monochrome monitor.

Board AB8 - Penplot & RGB video

Circuit diagrams : Chap. 7, Figs. 22 & 23

Latch selector and installed options indicator

191. During an IO read or write operation, latch selector IC13 decodes the A0 to A2 inputs to take one of its eight outputs low when enabled by CS5X going low and A3 going high. When output Y7 goes low in this way, the processor is able to read installed options indicator IC20. At the time that an option is installed, a link is inserted between the IC's input and ground so that when the processor reads a low data bit it can determine which option is fitted. When output Y2 goes low it clocks latch IC19 which controls the bleep tone generator. At the conclusion of the read or write operation, AND-gate IC7b output goes high causing all of the IC13 decoded outputs to go high. The resulting rising edge on a selected Y0, Y1 or Y3 output line is used to clock data latches IC4 or IC5 for the pen recorder or IC14 for the colour video generator.

Pen recorder drive

192. When CS58 or CS59 is taken high, data byte latch IC4 or control byte latch IC5 latches out its data to D-A converter IC3 or IC2 respectively. The data latched from IC4 supplies the pen recorder X axis, that latched from IC5 supplies the Y axis as well as operating RLA controlling the penlift operation.

193. Digital-to-analogue converter IC3 has an output resolution of 1024 steps and supplies the RECORDER X CHANNEL drive. The required 10 bits are supplied in parallel-bit, byte-serial form from IC4. Firstly, 8 bits on lines D0 to D7 are strobed into IC3 on the rising edge of LBS (Low Byte Strobe). Then a further 2 bits on lines D0 and D1 are strobed in on the rising edge of HBS (High Byte Strobe). The minimum output step size is determined by the reference output from IC6 level-shifted by Ref Volt Generator IC1a. When LDAC is taken high, D-A conversion takes place. The resulting IOUT current via IC7a varies the conduction of output buffer TR6 which supplies the feedback current to the converter's RFB input. This current produces the pen recorder X-axis voltage across R41.

194. To produce the RECORDER Y CHANNEL output, IC1a sets the minimum step size, while IC2 operates similarly to IC3 but is a 9-bit D-A converter whose output thus has a resolution of 512 steps.

Bleep tone generator

195. When CS5A goes low, it clocks latch IC19 whose outputs control the operation of the bleep tone generator which provides an audible warning signal. The generator consists of monostable IC18a, astable IC18b and piezo electric sounder XL1. The frequency and oscillation of IC18b is set to approximately 3 kHz by timing components R56, R57, C52 - and there are two pitch settings which are determined by the logic levels on the PITCH line. For interrupted sound operation, a falling edge on the BLEEP TRIG line takes IC18a output high for the period set by R52, C51 to enable oscillator operation after which the output ventures low to reset the oscillator. For uninterrupted operation, the CONTINUOUS line is held high to IC18b pin 10 to prevent a reset occurring.

Colour video generator

196. The logic level of data line D0 to D-type bistable IC14 determines whether the picture hue selected is a loud, foreground one or a quiet background one. When D0 is low and IC14 is clocked by CS5B, buffer IC15 is enabled to pass the video inputs from AB7 out to three colour combiners. The MINOR and MAJOR graticule inputs provide the RED VIDEO output, the A display INFIL and LINE inputs provide the GREEN VIDEO output and the B display INFIL and LINE inputs provide the BLUE VIDEO output. Each one of the inputs forming a pair is passed through a different value resistor. Thus the MINOR, A INFIL and B INFIL inputs are respectively fed through R9, R17 and R25 whose values are chosen so that they produce a dimmer display than the MAJOR, A LINE and B LINE inputs which are respectively fed through R10, R18 and R26. To produce a white display for the MARKER input as well as for a white character, these inputs are gated by the NOR-gates forming IC9 so that red, green and blue are selected simultaneously. When line D0 is high, the low clocked out to buffer IC16 enables quiet tone buffer IC16 to output colour of a different hue.

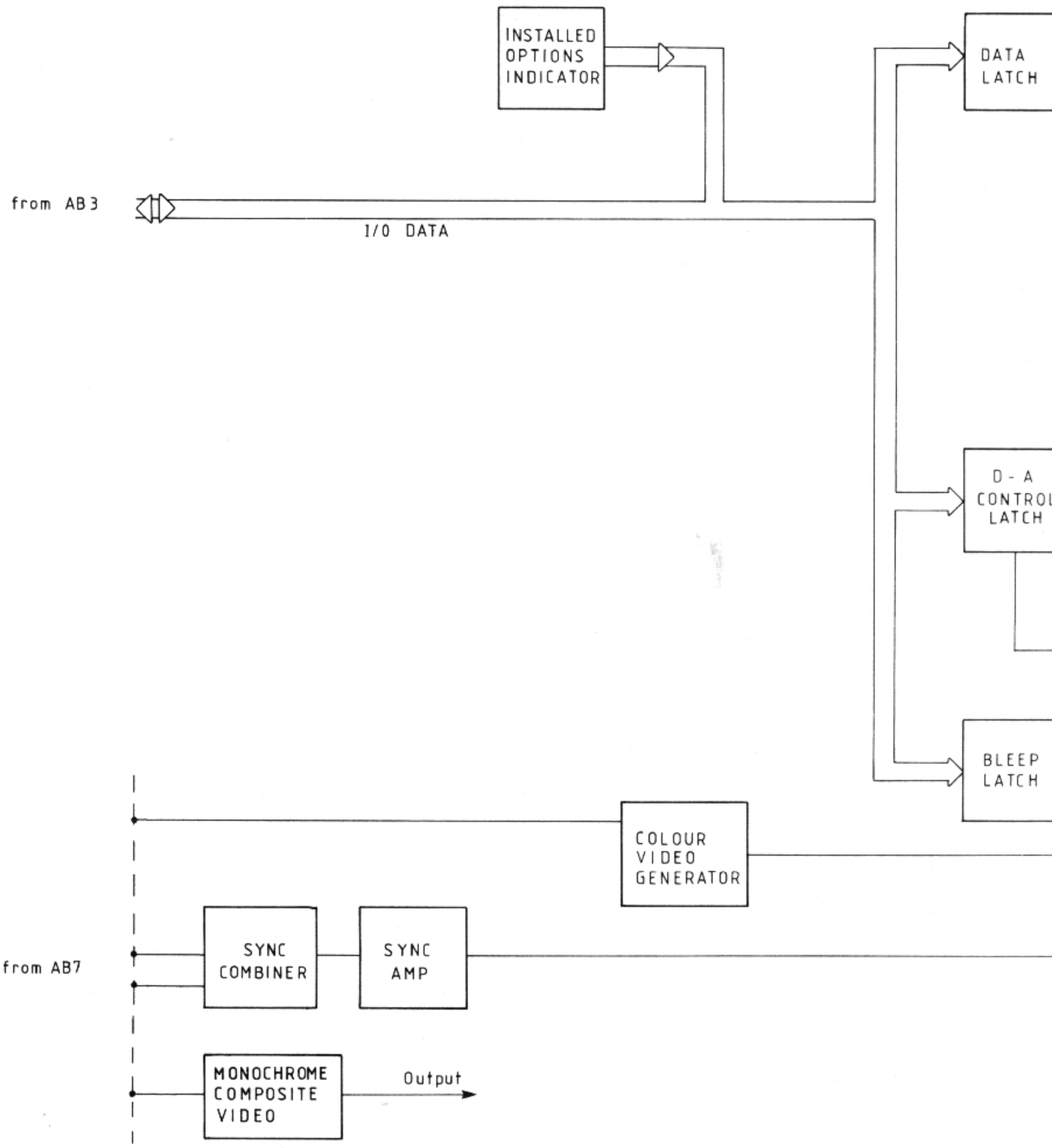
197. Character colour select decoder IC12 decodes the selection data on the GPA0S and GPA1S lines to set 1 of 4 outputs low. When enabled by CHAR to the NAND-gates forming IC10, Y0 to Y3 respectively select the required red, green, blue or white character colour in accordance with the display colour.

198. The horizontal and vertical synchronizing signals HSYNC (narrow pulse) and VSYNC (wide pulse) are combined by EXclusive-OR gate IC11d. This provides the single COMPOSITE SYNCS output from which the individual syncs may subsequently be recovered by the colour monitor.

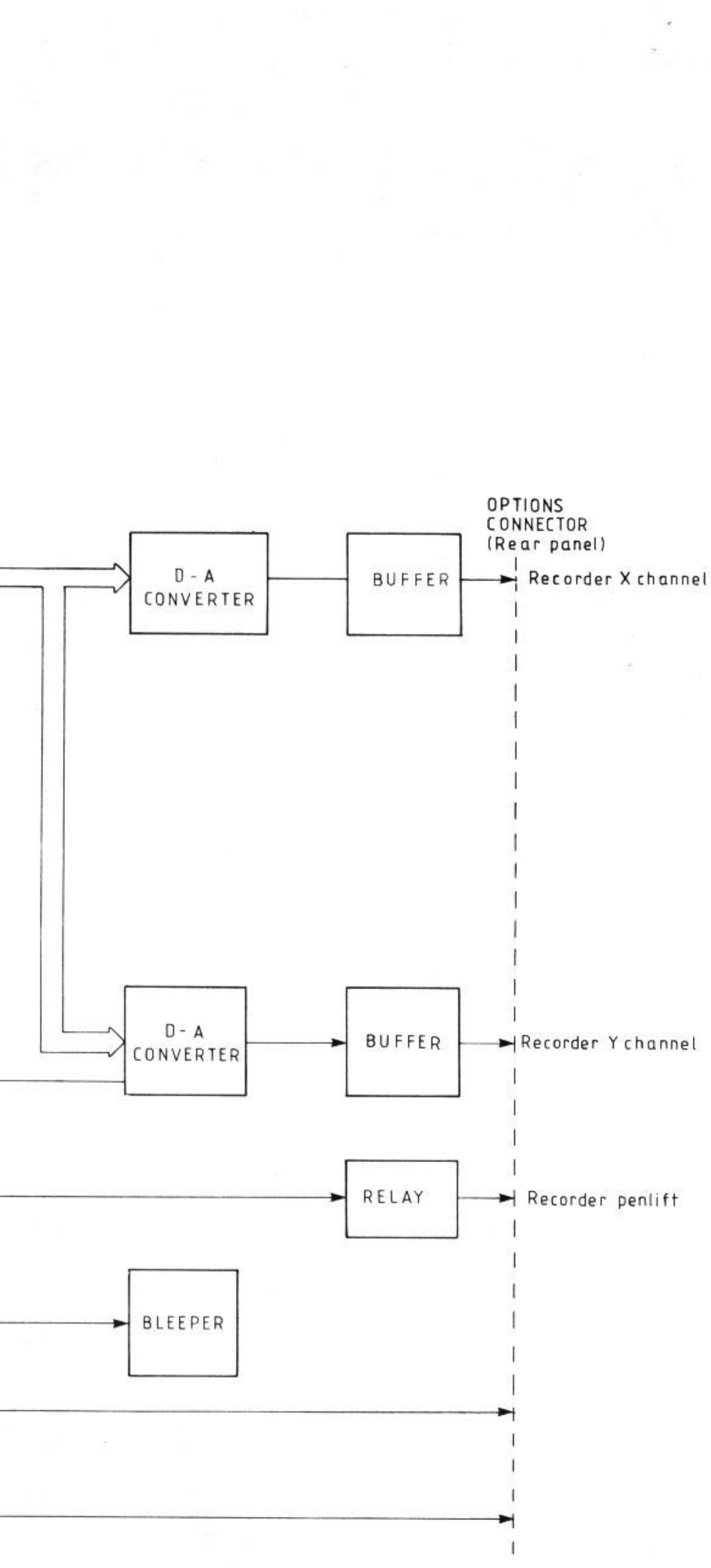
199. Outputs from the combiners operate switches TR1 to TR4 which produce a.c. coupled 1 V p-p signals to the rear panel OPTIONS connector.

Monochrome output

200. H SYNC and V SYNC via IC11d, and VIDEO from the video mixer to switch TR5, combine to operate switch TR6 which provide the COMPOSITE VIDEO OUTPUT signal for use by a monochrome monitor.



Pen plot and RGB video b



TPC 5240

ock diagram