20 GHz MICROWAVE COUNTER
2440

Code nos. 52440-301C
-302R
-304K
-305A

Amendment No.	*Date*	*Applies to Ser. Nos. commencing*
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MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND.

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CONTENTS

PRELIMINARIES

CHAPTERS

HAZARD WARNING SYMBOLS

The following symbols appear on the equipment.

Symbol	*Type of hazard*	*Reference in manual*
⚠	Precision connector	Page (iv)
⚠	Static sensitive device	Page (iv) and Chaps. 5, 6 and 7
⚠	Maximum input - Channel A/B	See Operating Manual
⚠	Maximum input - Channel C	

Note...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ◄ ..... ► to show the extent of the change. When a chapter is reissued the triangles do not appear.

Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2, etc.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be discharged; to discharge mains filter capacitors, if fitted, short together the L (live) and N (neutral) pins of the mains plug.

Mains plug

The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Fuses

Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol ⚠ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by yellow discs, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disc or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.
Metallic tools earthed either permanently or by repeated discharges.
A low-voltage earthed soldering iron.
An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

(4) If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

CAUTION : PRECISION CONNECTOR (on versions 52440-301C, -302R)

The precision type N connector (Channel C input) fitted to this instrument may be damaged by mating with general purpose type N connectors.

CAUTION : LCD HANDLING

When operating or servicing this equipment take care not to depress the front or rear faces of the display module as this may damage the liquid crystal display elements.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

WARNING : TOXIC HAZARD

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

Chapter 4-2

TECHNICAL DESCRIPTION

CONTENTS

CONTENTS (continued)

INTRODUCTION

1. Fig. 1 shows 2440 in block diagram form and identifies the main components and their functions.

2. Channel A and channel B have direct counting functions utilizing a low frequency counter and a high frequency counter respectively. Channel C has separate input and frequency control circuits and employs the 1.f. and h.f. counters to make final measurements. Channel selection, gating, measurement and displays are carried out under microprocessor control which enables local entries via the keyboard or remote control via the GPIB interface unit.

3. The detailed circuit descriptions which follow are basically separated for each channel with further sections for the microprocessor, keyboard, display, GPIB and converter units. They are intended to be read with reference to the circuit diagrams contained in Chap. 7 or in the case of Channel C microwave unit with reference to the circuit diagrams at the end of this chapter.

LOW FREQUENCY COUNTER : UNIT A7

Circuit diagram : Chap. 7, Fig. 19

4. The low frequency counter board contains the input, low-pass filter, gating and decade counter circuits that enable direct counting of the channel A input frequency. The gating and counter sections are also used during channel C operation to provide data for computing the channel C input frequency.

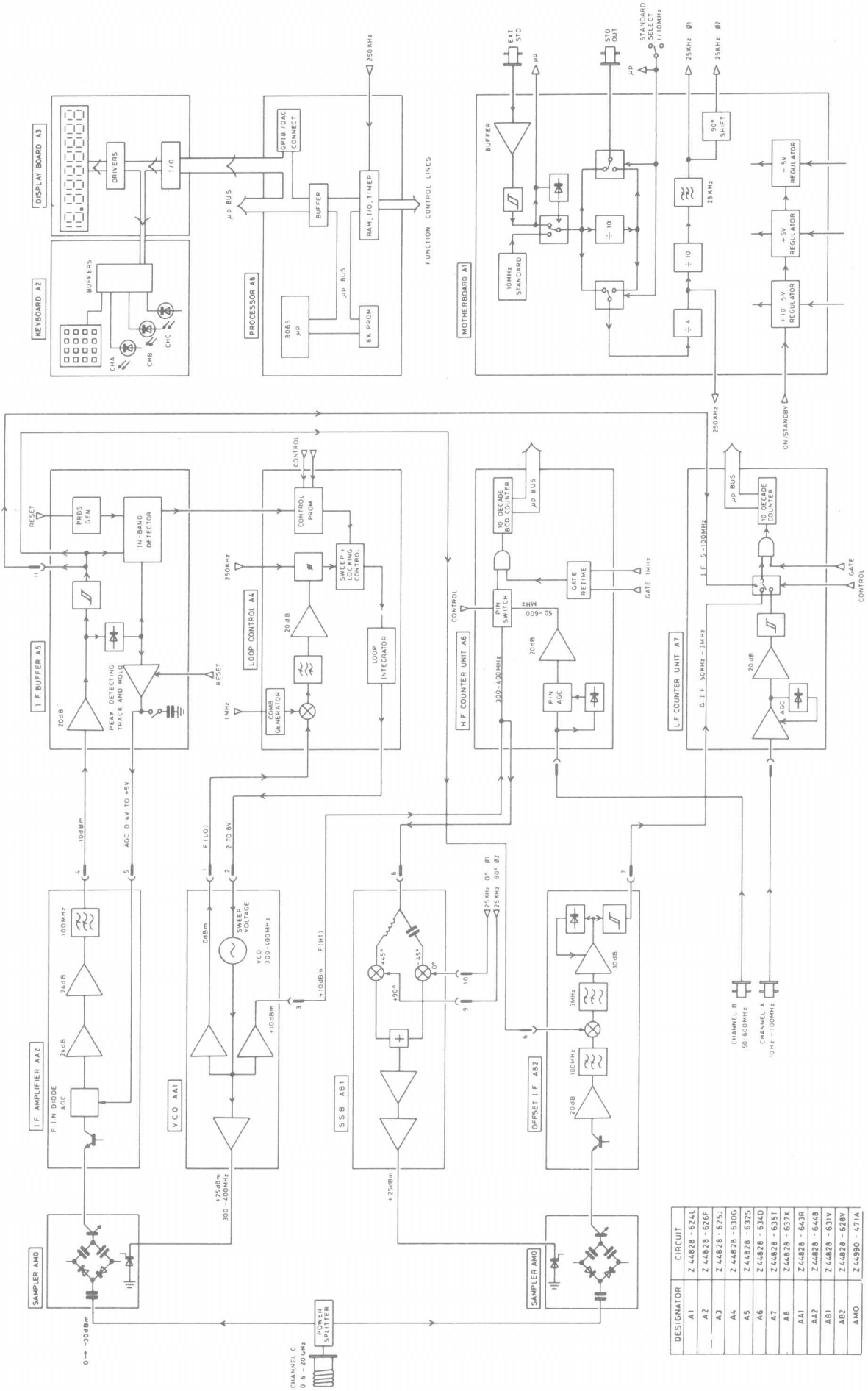
5. Control signals for insertion of the low-pass filter, counter input selection and channel operation are provided by the microprocessor board unit A8. A gating signal is also provided by the processor via a retiming circuit on the motherboard unit A1. Counter output is fed on to the data bus when addressed to do so by the processor.

Input, a.g.c. and amplifier circuits

6. Input to the low frequency counter board, unit A7 is direct from the front panel channel A input socket, SKA. A low-pass filter circuit at the board input is toggled in or out of circuit by operation of relay RLA. When LPF is selected the input line at pin 8b (PA5) from the processor is held low which switches on relay driver TR5. This energizes relay RLA and connects in to circuit the filter capacitor C2.

7. Diodes D1 and D2 and Zener diodes D3 and D4 are connected to provide voltage protection for the input amplifier TR1. If the voltage applied to channel A input is above the maximum allowed then diodes D3 and D4 conduct to ground.

8. TR1, TR2 and IC4 form an automatic gain control circuit. TR1 is a dual gate VHF amplifier/mixer, resistor coupled to TR2 which is emitter coupled to the counter amplifier IC1. A further output from TR2 is detected by diodes D6/D7 and capacitors C20/C21 and the resultant d.c. voltage applied to the non-inverting input of IC4. IC4 is an operational amplifier with its inverting input level set by variable resistor R31 (SET AGC) from the -5 V supply. Output from IC4 is fed to the second gate of TR1 which varies the gain to provide a stable input level to IC1a.



DESIGNATOR	CIRCUIT
A1	Z 44828 - 624L
A2	Z 44828 - 626F
A3	Z 44828 - 625J
A4	Z 44828 - 630G
A5	Z 44828 - 632S
A6	Z 44828 - 634D
A7	Z 44828 - 635T
A8	Z 44828 - 637A
AA1	Z 44828 - 643R
AA2	Z 44828 - 644B
AB1	Z 44828 - 631V
AB2	Z 44828 - 628Y
AM0	Z 44990 - 471A

Fig. 1 2440 block diagram

9. IC1a and IC1b are emitter coupled high speed differential amplifiers with the reference voltage provided by variable R10 (SET DC). C7, C8 and C9 ensure that this voltage is noise free. Output from IC1b is taken directly to the input select gate IC2c.

Channel A input operation

10. For channel A operation the channel A select line (PA4) from the processor is held low, which enables NOR gate IC2(c) and allows through the r.f. input signal to the counter gate IC2d.

Channel C input operation

11. During channel C operation, under processor control two further inputs are individually selected for counting. These are the i.f. signal and the Δi.f. signal.

12. The i.f. signal from the i.f. buffer A5 is fed to NOR gate IC2a pin 5 and gated by the i.f. select line PA2 held low. IC2a output goes low and is fed to the counter gate IC2d.

13. Similarly the Δi.f. signal from the offset board AB2 is fed to NOR gate IC2b pin 6. This signal is gated by the Δi.f. select line PA3 held low by the processor and passed to the counter gate IC2d.

Counter gate

14. The counter gate IC2d is a dual input NOR gate controlled by the ECL timing signal from the motherboard A1. This signal is derived from the 1 kHz timer (IC2) output on the microprocessor board and is retimed with the processor SOD output. When this gate line goes low the gate is oepened and the input signal transitions from low to high clock the first stage decade counter IC3.

First decade counter

15. IC3 is a 4 bit ECL decade counter connected for b.c.d. output on pins 14, 13, 4 and 2. Pin 14 carries the least significant bit and all 4 outputs, after conversion by the ECL to TTL converter IC5, are fed to the data selectors in the main counter chip IC6. Pin 2 and pin 3 of IC3 are complementary outputs connected to TR4 and TR3 respectively. Each time IC3 reaches end of count 9, a negative-going pulse from TR3 is produced which clocks the TTL decade counter IC7. 4 line output in b.c.d. format from this second decade counter is coupled directly to the main decade counters.

Main decade counters

16. The main decade counters are contained in a custom designed 10 decade counter chip IC6 which allows direct address and data interface to the microprocessor bus. The 2 most significant of the 10 decades are parallel loaded by the external counters IC3 and IC7. Data is accessed when the two select lines RD and CS6 are held low. Data output is in b.c.d. format with the least significant address.

17. IC7 also contains an overflow latch and a further address allows the overflow flag to be tested. At the end of the counting period a final address clears all decades to zero and outputs a pulse on the CLR L line to TR6. This turns off TR6 and the rise in collector volts resets the external counters IC7 and IC3.

HIGH FREQUENCY COUNTER : UNIT A6

Circuit diagram : Chap. 7, Fig. 17

18. The high frequency counter board contains the input, amplifier, gating and decade counter circuits that enable direct counting of the channel B input frequency. The gating and counter sections are also used during channel C operation to provide data for computing the channel C input frequency.

19. Control signals for counter input selection and channel operation are provided by the microprocessor board unit A8. A gating signal is also provided by the processor via a retiming circuit on the motherboard unit A1. Counter output is fed on to the data bus when addressed to do so by the processor.

Input, level control and amplifier circuits

20. Input to the high frequency counter for channel B operation is direct from the front panel socket SKB. Counter input is capacitor coupled to the voltage protection circuit centred on D2 and then level controlled by the action of PIN diode D3. C5 couples the detected signal pulses to the wideband differential amplifier IC1.

Channel B input operation

21. When channel B is selected the channel B select line (PA1) from the microprocessor (A8) is held low, forward biassing the Zener diode D1 and turning on TR1. Current flow through TR1 switches on the PIN diode D4 and amplifier output is fed to the first decade counter IC2.

Channel C input operation

22. During channel C operation, under microprocessor control an alternative input to the decade counter is selected. This is the voltage controlled oscillator frequency from the VCO board (AA1) which is fed to the PIN diode D6. The VCO select line (PA0) from the microprocessor is held low, forward biassing Zener diode D5 and turning on TR2. Current flow through TR2 switches on D6, allowing through the high level VCO input to the decade counter IC2.

First decade counter

23. IC2 is a high speed divide by 10 ECL counter with a gated clock input. Positive-going transitions on the clock input will clock the counter when the clock inhibit input is held low.

24. Output from the counter is in b.c.d. format (t.t.l. compatible) on 4 lines, to the main decade counters in IC7. ECL carry output is buffered and inverted by IC3 and clocks the second decade counter IC4.

First decade inhibit control

25. The inhibit control is used to gate the decade counter. Is is provided by the ECL D type bistable IC8a. Clock input to IC8a is a 1 MHz timing pulse derived from the frequency standard on the motherboard A1. D input is the TTL gating signal also from the motherboard. It is derived from the 1 kHz timer IC2 on the microprocessor board A8 and is retimed with the processor SOD output. The 1 MHz timing pulse clocks IC8a on positive transitions when the D input and the set input S are low.

26. Set input at IC8a pin 5 is used to ensure that the inhibit to the first decade counter is only removed when a valid input signal is present. This prevents random counts that might occur if channel B is selected without a signal being present.

27. Signal input at C12 from channel B amplifier is detected by D7/D8 and fed to voltage follower IC7a. Output is passed to IC7b inverting input where it is compared with the positive input set by variable R28. R28 is the SET LOCKOUT control and is adjusted to set the signal/no signal threshold level.

28. IC7b output is level shifted by resistors R33/R34 fed from the -5 V supply. Input to the network via D9 causes a voltage drop across R34 resulting in an ECL high state being applied to IC3b. This is an ECL inverter whose low output to the set input of IC8a pin 5, allows it to operate for normal counting.

29. With no signal input at C12 there is no output from the comparator IC7b. Level shift circuit R33/R34 now presents an ECL low level to inverter IC3b. The high output state from IC3b to IC8a sets the device with Q output held high. This inhibits the first decade counter IC2 and results in a zero display.

Second decade counter

30. IC4 is a 4 bit ECL decade counter which is triggered on the positive-going edge of the clock input pulses. It is connected for b.c.d. output with complementary outputs for the first and fourth bits. Pin 14 carries the least significant bit. Logic conversion from ECL to TTL is carried out by voltage comparator IC6 which feeds the 4 line b.c.d. output to the data selectors in the main decade counter chip IC7.

31. The fourth bit from IC4 is also fed to IC8b which is an ECL D type bistable. At the end of each count 9 pulse from IC4, the positive-going edge clocks IC8b which changes over its output state so performing a divide by 2 function. Transistors TR3 and TR4 are emitter coupled and fed from the equal and opposite outputs of IC8b. As the output states change over, TR3 and TR4 alternately switch on and off providing at TR3 collector a train of TTL logic pulses, which is fed to the main decade counters. Diode D7 maintains the pulse line polarity.

Main decade counters

32. The main decade counters are contained in a cusom designed 10 decade counter chip IC7, which allows direct address and data interface to the microprocessor bus. The 2 most significant of the 10 decades are parallel loaded by the external counters IC2 and IC4. The internal counters, divide by 5 and divide by 10, are loaded at pin 23 (IN) from TR3 collector. Data is accessed when the two select lines RD and CS5 are held low. Data output is in b.c.d. format with the least significant decade accessed in the least significant address.

33. Overflow information is provided by an internal latch which when addressed makes available an overflow flag. At the end of the counting period a further address clears all the internal counters to zero and outputs a reset high pulse on the R line. This resets the external counters IC2, IC4 and IC5.

MICROWAVE COUNTER CIRCUITS : CHANNEL C

Brief overall description (see block diagram Fig. 1)

34. Channel C employs the harmonic heterodyne conversion technique with a small offset on the oscillator frequency to enable computation of the harmonic number.

35. The input is split into two signal paths, both of which immediately down-convert the microwave signal to produce two i.f's in the 20 to 100 MHz range using identical sampling type mixers.

36. The primary mixer is driven by a local oscillator in the 300 to 400 MHz range and harmonics are generated within the mixer to beat with the input signal and produce a primary i.f. (IF_1). Under control of the microprocessor the local oscillator is swept over its full frequency range which allows the primary i.f. system to 'look at' the complete r.f. input spectrum.

37. A peak detecting a.g.c. system sets the i.f. gain such that only the largest amplitude input signal will be recognized. A dedicated counter detects an i.f. in the centre of the i.f. pass band and stops the local oscillator sweep. Control is then passed to a complex phase-locked loop which locks the local oscillator to the system time base and determines whether the upper or lower sideband has been acquired (+ or - sign).

38. The locked local oscillator frequency is shifted by a small amount and fed to the offset mixer. This results in a slightly different i.f. frequency which is mixed with the primary i.f. to produce a third i.f. (ΔIF). This frequency is a measure of the harmonic number (N).

39. By measuring this third i.f. and the primary i.f. (IF_1) in the LF counter and the local oscillator frequency (f) in the HF counter, the unknown input frequency (Fx) can be calculated by the microprocessor from the relation

$$Fx = Nf \pm IF_1$$

Summary of sequence of events

40. The following sequence of events lists the routines carried during channel C operation i.e.

Starting status
Acquisition of signal
Measurements
Calculations

It gives an overall view of the whole operation which can then be studied in detail by reference to the individual circuit descriptions that follow.

40.1 Starting status

(1) Channel C selected.
The c.p.u.:- resets a.g.c. peak detector,
resets pseudo-random generator,
selects mode in EPROM to continuously sweep voltage controlled oscillator (VCO) from 400 MHz to 300 MHz.

40.2 Acquisition

(1) VCO harmonics sweep in and out of zero beat with input signal frequency.

(2) Series of i.f. signals sweep through i.f. amplifier to peak detector.

(3) Peak detector samples and holds largest i.f. and sets a.g.c. for i.f. attenuator.

(4) When i.f. signal comes into mid-band range (48 MHz to 64 MHz) mid-band detector allows signal through to in-band counter.

(5) Binary output of in-band counter feeds EPROM via latch.

(6) TRACK signal sent to alert CPU that valid i.f. signal has been acquired.

(7) SEARCH signal is sent to disable the mid-band detector and allow through to in-band counter the whole i.f. bandwidth.

(8) EPROM functions as a sequence generator actioning data output sequences from incoming information which is supplied every time the in-band counter is gated.

(9) EPROM program operates VCO sweep control switches to track i.f. signal. Firstly to determine sideband polarity and secondly to pull VCO frequency such that i.f. signal comes into centre of mid-band i.e. ≅50 MHz.

(10) EPROM program finally pulls i.f. very close to 50 MHz and then sends PHASE LOCK signal to operate phase lock switch.

(11) EPROM program changes to the drift condition and the acquired i.f. signal very slowly drifts up or down within phase lock loop capture range (500 kHz).

(12) A 250 kHz signal derived from the VCO frequency and referenced from the internal standard frequency source locks the VCO sweep control circuit. This fixes the i.f. signal and VCO frequency.

(13) The i.f. frequency is mixed with an offset i.f. to produce Δi.f.

40.3 Measurements (under procesor control)

(1) ΔIF fed to LF counter, gated for 4 ms and result divided by 100 produces preliminary harmonic number N.

(2) VCO frequency preliminary count made by HF counter.

(3) N checked - must be whole number.

(4) VCO frequency checked - must end in .250 MHz or .750 MHz (indicates locked condition).

(5) IF (primary) frequency is counted by LF counter.

(6) VCO frequency is again counted by HF counter.

(7) ΔIF is again counted by LF counter and derived N is checked against earlier result.

(8) Counter measurements, harmonic number and sideband polarity saved in RAM.

40.4 Calculation

(1) Processor uses information saved in RAM to calculate the unknown input signal frequency from the relation:-

$$Fx = Nf \pm IF_1$$

where Fx = Unknown input frequency

N = Harmonic number

f = VCO frequency (local oscillator)

± = Sideband polarity

IF_1 = Primary i.f.

(2) This data is placed in the result store for subsequent display.

(3) If there is no change in input signal frequency the VCO remains locked and measurements and calculations are repeated for 4 to 5 seconds.

(4) At the end of this period, or if the input frequency changes before the end, the a.g.c., pseudo random generator, SEARCH and TRACK signals are reset ready to restart the signal acquisition procedure.

Circuit descriptions

41. The following circuit descriptions are for those boards dedicated only to channel C operation. These are:-

Sampler (AM0), VCO (AA1), IF amplifier (AA2), IF buffer (A5), Loop control (A4), Offset driver (AB1) and Offset i.f. (AB2).

42. Descriptions for the other boards involved in the operation are contained in sections under their own heading i.e. LF counter, HF counter, microprocessor etc.

Note...

The microwave unit which comprises the power splitter, samplers, VCO, IF amplifier, Offset driver and offset i.f. boards is a sealed unit. Descriptions and circuit diagrams for these components are given in this chapter only to assist in the technical comprehension of the instrument's functions. The unit must not be opened or the instrument warranty will be invalid.

Power splitter

Interconnection diagram : Chap. 7, Fig. 3

43. This is a sealed unit which splits the input signal into two paths with a 3 dB loss at each output port. One output is passed to the primary converter AA0 and the other is passed to the offset converter AB0.

Primary converter : unit AA0

Interconnection diagram : Fig. 6

44. The primary converter comprises a sampler AM0, a voltage controlled oscillator (VCO) AA1 and an i.f. amplifier AA2.

45. Output from the splitter is fed to the sampler which is driven by the VCO output. The resultant i.f. is amplified and passed to the i.f. buffer A5.

46. The i.f. buffer also provides an automatic gain control voltage which is applied to the i.f. amplifier input stages. Control of the VCO sweep voltage is provided by the loop control board A4.

Sampler : Unit AM0

Circuit diagram : Fig. 7

47. The sampler function is to mix the input frequency with harmonics of the VCO local oscillator frequency and produce an intermediate frequency - the primary i.f.

48. Signal input from the power splitter is fed to diodes D1 and D2 which form one half of a bridge network. VCO input drives step recovery diode D3 which feeds a train of pulses down a slotted line. This generates two

opposite polarity pulses which are capacitively coupled by the component substrate to drive the mixer diodes D1 and D2. Primary i.f. output produced is buffered by TR1 and fed to the i.f. amplifier AA2.

Voltage controlled oscillator (VCO) : Unit AA1

Circuit diagram : Fig. 8

49. The function of this board is to provide an oscillatory voltage that can range in frequency from 400 MHz to 300 MHz and output this at three different power levels. These provide - the drive to the sampler mixer AM0, an input to the HF counter A6 and an input to the loop control circuit A4.

50. The +10 V supply rail is further regulated and reduced to +8 V by IC1. This provides a very low noise supply for the oscillator TR1/TR2, the power amplifier TR3 and the low level amplifier TR4.

51. Varicap diodes D1 and D2 in the oscillatory circuit are fed with a descending ramp control voltage of 8 V to 2 V. This is supplied under EPROM program control from the loop control board A4 during the continuous sweep operation. This changing voltage across the varicap diodes causes the oscillator frequency to sweep from 400 MHz to 300 MHz. Oscillator output is power amplified by TR3 and drives the sampler mixer AM0. Variable capacitors C8,C9 and C13 are set to obtain the optimum overall frequency response.

52. On entering the signal acquisition mode the EPROM instructions change and the sweep voltage becomes a tracking voltage. This causes the oscillator frequency to change up or down until the signal acquisition loop locks. In this state the control voltage remains steady and the oscillator frequency is fixed.

53. A second output from the power amplifier is buffered by TR5 and provides a high level output to the HF counter unti A6. This is the VCO frequency signal which under processor control, will be counted and the result used in calculating the instrument input frequency.

54. A third output is made available by extracting a voltage direct from the oscillator circuit. This is buffered by TR4 and fed out as a low level input to the sweep locking circuit on the loop control board A4.

IF amplifier : Unit AA2

Circuit diagram : Fig. 9

55. The i.f. amplifier amplifies the primary i.f. signal from the sampler and utilizes an automatic gain control signal to maintain a fixed level output to the i.f. buffer A5.

56. Primary i.f. input is fed to TR1 and TR2 which amplify the signal by 12 dB. PIN diodes D1 and D2 attenuate this signal. The level of attenuation is varied by the a.g.c. voltage from the i.f. buffer circuit A5. This variable control voltage produces an attenuation range of 0 to 40 dB and maintains the final board output voltage at a nominal 200 mV p-p.

57. The level controlled i.f. signal from D2 is further amplified by IC1 (24 dB) and IC3 (24 dB) and passed via a 100 MHz low-pass filter network to the i.f. peak detector on A5 board.

IF buffer : Unit A5

Circuit diagram : Chap. 7, Fig. 15

58. The i.f. buffer board carries out the following main functions:

(1) Amplifies the primary i.f.

(2) Detects the largest peak for use as an a.g.c. control to the i.f. amplifier AA2.

(3) Detects the mid-band i.f. frequency range.

(4) Counts the detected i.f. signal using a dedicated step counter and feeds result to an EPROM latch on the loop control board A4.

(5) Provides the transfer signal to latch step counter data to EPROM.

(6) With the mid-band detector disabled the main i.f. signal is counted by the step counter. The output data via latch to EPROM finely controls the VCO frequency.

(7) Primary i.f. is connected to the LF counter A7 for final frequency measurement and to the offset mixer board AB2 to produce Δi.f.

20 dB amplifier and peak detector

59. With a signal connected to channel C input, the voltage controlled oscillator is initially set to continuously sweep the input frequency. As the VCO harmonics beat with the input frequency a series of i.f. signals pass through the i.f. amplifier AA2 to the 20 dB amplifier.

60. Output of the 20 dB amplifier IC1 is connected to a d.c. level detector centred on D1 and D2. Back to back connection of these diodes provides temperature compensation. The d.c. output level is integrated by IC2a and drives the track and hold peak detector IC2b and IC2c, Threshold level of the integrator is set by R11 (SET AGC).

61. Successive i.f. signal levels are sampled and the highest held to charge C10. Buffer TR2 passes this d.c. output, via a compensating circuit, to the p.i.n. diode attenuator on the i.f. amplifier board AA2. Compensation is provided by D10, D11 and R57, R58 which overcome the non-linearity of the p.i.n. diode action. Thus the amplifier gain is controlled and held at a level determined by the largest i.f. signal detected ensuring that lesser signals are ignored.

62. When the subsequent signal acquisition and measurements etc. are completed the peak detector circuit is reset ready to restart on a new train of i.f. signals. TR1, TR3 and TR4 form the peak detector reset circuit which is activated by the a.g.c. reset line from the processor on board A8.

63. When the reset line goes high, TR3 is turned on which turns on TR4 and TR1. With TR4 conducting to +10.5 V, C10 is effectively short circuit and discharges. TR1 conducting resets C8 in the a.g.c. integrator circuit to the no signal condition and also charges C9. This results in the a.g.c. control voltage falling to approx. 0.4 V and reduces the i.f. amplifier gain to minimum.

Schmitt trigger

64. Amplified primary i.f. signals from the 20 dB amplifier are fed to the Schmitt trigger circuit TR5 and TR6. They are shaped and squared and passed via emitter follower TR7 to the counter input NOR gate IC3c. DC level symmetry of the square waves is set by R30 (SET DC).

Mid-band detector

65. The 20 dB amplifier i.f. output is also passed to the mid band-pass filter L4, C36. When the i.f. signal is swept into the mid-band frequency range of 48 MHz to 64 MHz it is d.c. level detected by D8 and D9 and fed to amplifier IC2d. Output from IC2d is passed to the NOR gate IC3a where it is gated with the search signal line from the loop control board A4.

66. At this time the search line is held low and so the output of IC3a is held low for the period of the mid-band detector response. This output opens the counter input gate IC3c to allow through only the mid-band i.f. signal and 'lock out' the remainder. DC level of lockout control is set by R25 (SET IF LOCKOUT).

67. Later during the final signal acquirisiton stage the search line is set high and this in conjunction with the detector output causes IC3a output to be fixed low. This keeps open the counter input gate IC3c and allows through the whole i.f. spectrum from the Schmitt trigger TR7.

68. Output from IC3c, in addition to providing the counter input through IC3b, provides via IC3d two e.c.l. outputs. One to the LF counter unit A7 for subsequent measurement of the primary i.f. frequency and a second inverted output from pin 15 to the offset i.f. unit AB2 to mix with the offset i.f. and produce the difference frequency Δi.f.

In band counter

69. The in-band counter comprises a chain of divide by 2 bistables IC4, IC5a and IC11 which feed a 4 bit binary counter IC6. TR8 and TR9 form an e.c.l. to t.t.l. logic level shift and amplifier circuit. Diode D7 maintains the positive polarity of the input signal to IC7d. The counter output from IC6d to the EPROM latch on A4 board is in 3 bit binary format representing steps of 16, 32, 64 MHz. Thus a count of 20 MHz is represented by 001 and 55 MHz by 011.

70. The counter is initially cleared and reset by a 0.2 μs pulse from monostable IC9 which is triggered by the pseudo-random binary sequence (p.r.b.s.) generator IC7 and IC8. This generator is reset from the microprocessor on A8 and clocked by the 250 kHz standard frequency signal from the motherboard A1. A p.r.b.s. generator is chosen as the reset and gating source to prevent any coherence between the VCO frequency and the i.f. frequency when the input signal to be measured contains frequency modulation. If this were to happen false readings would occur.

71. The p.r.b.s. generator also triggers the monostable IC9b which provides a negative 7 µs pulse to NOR gate IC10a. This allows through the 250 kHz reference signal to edge trigger the bistable IC5b. IC5b produces an accurate negative 4 µs pulse which is applied to the exclusive OR gate IC7d. This gate functions as the counter gate by allowing through the output of counter bistable IC5a to complete the divide by 2 chain operation for a period of 4 µs.

72. The 7 µs pulse from IC9b is also fed to the loop control board A4 for use as the in-band counter output data latching signal.

Loop control : Unit A4

Circuit diagram : Chap. 7, Fig. 13

73. The loop control board performs the following functions:-

(1) Provides a ramp sweep voltage to drive the voltage controlled oscillator AA1.

(2) Reads into EPROM, data from the in band step counter on the i.f. buffer A5.

(3) Provides status signals from EPROM to the c.p.u. (track and sideband polarity) and to the i.f. buffer (search).

(4) Samples the VCO input and provides a 250 kHz reference signal to phase lock the VCO sweep voltage during the signal acquisition mode.

VCO sweep voltage

74. When channel C is selected, mode command 0 is sent by the processor to initialize EPROM IC2. The mode 0 program is implemented and data is output on lines D0, D1 and D2 to control the switches IC3a, b, c and IC4a.

75. The position of these switches and their associated resistors fed from +5 V or -5 V supplies, determine the current drive to the ramp sweep control voltage integrator IC5. IC3c and IC3a provide a choice of 4 current drives and hence 4 VCO ramp speeds selected by IC4a. These are sweep, track, drift and flyback. IC3b determines polarity i.e. ramp up or ramp down.

76. Output from IC5 is buffered by TR1 and produces a ramp voltage rising from 2 V to 8 V. This is fed as the sweep control voltage to the VCO on board AA1.

77. IC5 output is also fed to IC10a which operates as a Schmitt trigger to provide the ramp flyback voltage. Circuit conditions are set so that when TR1 ramp output voltage reaches 8 V IC10a triggers and via level shifter IC10b addresses the EPROM at A8. EPROM responds and outputs data on lines D1 and D2 which changes over the switches such that the ramp voltage drops to 2 V. This resets the trigger circuit and new data output from the EPROM changes the switches back again to restart the sweep.

78. Supplies to the sweep and acquisition control circuits and to the VCO sweep circuits are further regulated and smoothed by TR7, TR8 and TR9 circuits. These provide relatively noise free supplies of +9 V and -4.5 V which prevent frequency modulation being produced when the VCO swept frequency beats with the input frequency.

Search and acquisition control

79. The in-band counter binary output is presented as data input to latch IC1. On the low to high transitions of the i.f. latch signal IC1 output addresses the EPROM IC2 on lines A0, A1 and A2. The EPROM acts on the addressed locations and sends a STATUS signal to IC1. IC1 is clocked after every counter gate period and feeds successive counter outputs and status signals to IC2.

80. IC2 acts on this information and informs the processor on A8 board that a valid i.f. signal is present by sending the TRACK signal. At the same time the SEARCH signal is sent to disable the mid-band detector on i.f. buffer board A5 which allows through the whole i.f. spectrum.

81. Program in EPROM now outputs data on switch lines A, B and C to track the VCO frequency up and then down to determine the sideband polarity, see Fig. 2. As the VCO frequency is shifted up and down, the detected i.f. signal moves up and down within the sideband frequency response. The in-band counter readings to the EPROM change in relation to the VCO frequency shift. The EPROM reads the direction of this shift and determines whether the upper or lower sideband has been selected i.e. if VCO frequency is decreased and counter output frequency increases then upper sideband has been selected.

82. EPROM program shifts VCO frequency up and down to make more than one reading and so confirm the result. Sideband polarity is then sent to the processor. High for positive upper sideband and low for negative lower sideband.

83. The program now starts to pull the i.f. signal towards the centre (50 MHz) of the sideband by controlling small changes in VCO frequency. When the EPROM reads from the incoming counter data that the i.f. signal has reached the centre, switches IC3 and IC4 are changed over from the track to the drift positions. The PHASE LOCK line to IC4b is set high which connects in the phase locking circuits while the i.f. signal very slowly drifts within the phase lock loop capture range of 500 kHz.

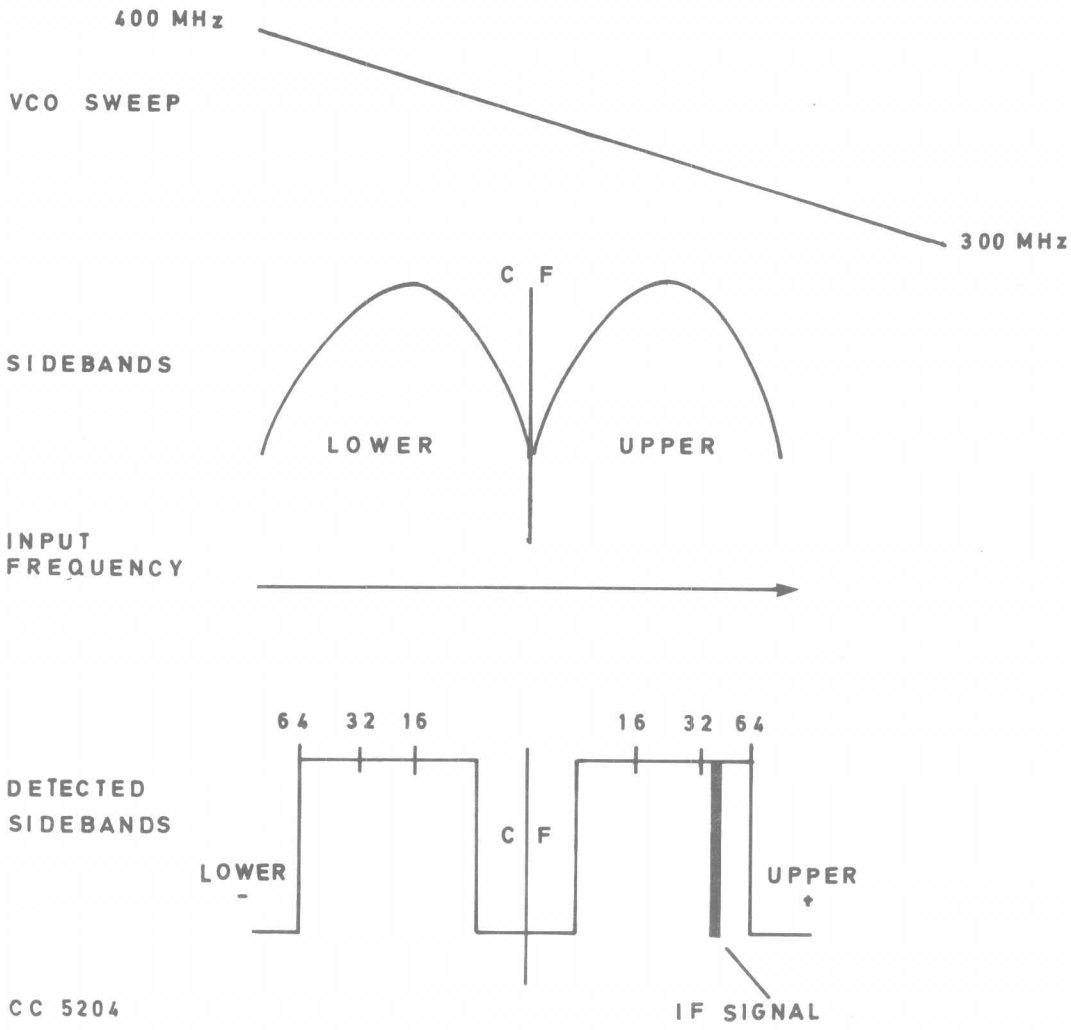


Fig. 2 Sideband polarity

Phase locking

84. The VCO low level output from AA1 board is fed to the sampler gate D3/D4, R31/R32. The standard 1 MHz reference frequency from the motherboard A1 is fed via AND gate IC7a, amplified by TR4/TR5 and coupled by transformer T1 to drive the sampler. This beats with harmonics of the VCO frequency and produces 250 kHz i.f. signals above or below the 1 MHz multiple i.e. .250 kHz or .750 kHz.

85. TR6 amplifies this signal which is then passed through the low-pass filter L1/C32, C34, L2 and further amplified by IC8 and IC9. These provide two equal and opposite outputs to switch IC4c which is operated by the 250 kHz reference frequency from the motherboard via IC7b AND gate.

86. Switch output is fed to IC6 which functions as a 250 kHz phase detector, filter and rectifier. IC6 output is a d.c. voltage proportional to the difference in phase between the 250 kHz reference frequency and the 250 kHz i.f. signals.

87. The d.c. voltage is passed to switch IC4b which is held in the low impedance IC5 input position by the PHASE LOCK control signal. Integrator IC5 operates on this d.c. voltage to control the VCO frequency which in turn determines the d.c. voltage and so the loop is closed and locks.

Offset converter : Unit AB0

Block diagram : Fig. 10

88. The offset converter comprises a sampler AM0, an offset VCO frequency driver AB1 and an offset i.f. amplifier and mixer.

89. Output from the power splitter is fed to the sampler which is driven by a frequency shifted VCO voltage. This produces a second intermediate frequency (offset i.f.) which is slightly different to the primary i.f.

90. The offset i.f. is mixed with the primary i.f. and the difference result (Δi.f.), which is a measure of the harmonic number, is amplified and passed to the LF counter A7.

Sampler : Unit AM0

Circuit diagram : Fig. 7

91. The sampler function is to mix the input frequency with harmonics of the offset VCO frequency and produce an intermediate frequency - the offset i.f.

92. This sampler is identical to that used in the primary converter but operates with different input and output signals.

93. Signal input from the power splitter is fed to diodes D1 and D2 which form one half of a bridge network. Offset VCO input drives step recovery diode D3 which feeds a train of pulses down a slotted line. This generates two opposite polarity pulses which are capacitively coupled by the component substrate to drive the mixer diodes D1 and D2. Offset i.f. output produced is buffered by TR1 and fed to the offset i.f. driver AB2.

Offset driver : Unit AB1

Circuit diagram : Fig. 11

94. The function of the offset driver is to change the VCO frequency by a small amount and amplify this for use as the drive to the offset sampler.

95. The high level output from the VCO is fed to the single sideband modulator IC1 and IC2 with L1 and C1 providing 90° phase difference between the inputs. Drive to the other side of the modulator is provided by two 25 kHz signals with a 90° phase difference. These signals are referenced to the internal frequency standard and are produced on the motherboard A1.

96. C1 in the VCO carrier input circuit and R4 (SET BAL) in the drive input circuit are adjusted for maximum rejection of the carrier and the unwanted sidebands. Output from the modulator is the upper sideband. This is the offset carrier which is 25 kHz above the VCO frequency.

97. TR1, TR2 and TR3 amplify the carrier signal and TR4 provides the power to drive the offset sampler. Variable capacitors C14, C15 and C16 are adjusted for optimum overall response of the sampler drive.

Offset i.f. amplifier : Unit AB2

Circuit diagram : Fig. 12

98. The offset i.f. amplifier board mixes the primary i.f. and the offset i.f. to produce the difference frequency Δi.f.

99. The offset i.f. signal from the offset sampler is amplified by TR1 and TR2 (12 dB) and then by IC1 (20 dB). It is passed through a 100 MHz low-pass filter and fed to the mixer circuit IC2. Second input to the mixer is the primary i.f. signal from the i.f. buffer board A5.

100. Output of the mixer, which is the difference frequency between the primary i.f. and the offset i.f., is taken through a 3 MHz low-pass filter to amplifier IC3. Gain of IC3 is controlled by an a.g.c. circuit centred on IC4 whose output is amplified by TR3. R38 (SET AGC) sets the level of a.g.c. control.

101. The amplitude controlled difference frequency Δi.f. is reshaped by Schmitt trigger circuit TR4, TR5 and TR6. R25 (SET DC) is adjusted for an equal mark/space ratio. ΔIF output from TR6 is passed to the 1.f. counter unit A7 where, under processor control, a frequency measurement is made and the result used to calculate the harmonic number N.

MICROPROCESSOR BOARD : UNIT A8

Circuit diagram : Chap. 7, Fig. 21

Microprocessor system

102. The microprocessor board contains the central processor unit (c.p.u.), address and data line buffers, address decoders, EPROM RAM, timer and I/O ports. Components and their functions are briefly described below. Full descriptions of the 8085A c.p.u. and the 8155 RAM, I/O, timer can be found in the "MCS 85 User's Manual" published by the Intel Corporation.

103. The c.p.u. controls the operation of the instrument by the program stored in the EPROM and implements this by means of the data/address bus and the I/O ports.

Processor functions

104. Processor functions can be summarized very briefly as follows. On power up tests are performed to check and set up the hardware. These are:-

ROM and RAM checks,
Check for and load GPIB interface,
Initialize 8155 timer/IO chip,
Check for real time clock,
Set up default status,
Set to make a measurement.

105. The processor then enters the measurement loop which is modified by the setting/resetting of flags actioned by the interrupt service routines. These are initiated by the restart inputs which are:-

Top priority	TRAP	Not used
	RST 7.5	Real time clock
	RST 6.5	GPIB commands
	RST 5.5	Keyboard commands
Low priority	INT	Not used

106. Responding to the interrupt the processor jumps to the appropriate routine in ROM and outputs the required information on to the data bus for display or for transmission over the GPIB bus.

System operation

Central processor unit

107. The c.p.u. IC1 is an 8 bit n.m.o.s. microprocessor with on chip clock generation, 3 vectored interrupts and a multiplexed address/data bus. A 6.144 MHz crystal is used with the clock generator which provides a basic clock of 3 MHz.

108. The data bus is multiplexed with the 8 low order address lines AD0 to AD7. Address lines A8 to A15 are output only lines carrying the high order address byte.

109. The RESET pin on IC1 is used for power up initialization. Resistor R5 pulls the line high and capacitor C1 to earth provides an automatic power on pulse. When power is first applied, the discharged capacitor is at low logic level and the processor internal circuits are cleared with the program counter reset to 0000 and interrupts disabled. Current through the pull up resistor causes the capacitor to charge up to the threshold of the reset input and the processor begins executing the program starting at 0000.

Address and data buffering

110. IC4 address buffer is an octal transparent latch which demultiplexes the eight lower address and data lines by means of the ALE (address latch enable) signal. The trailing edge of ALE (high to low transition) latches address information on AD0 to AD7 on to IC4 outputs. The address is then removed from the address/data bus to allow data transfer to take place.

111. IC6 data buffer is a bus transceiver comprising 8 parallel non-inverting bi-directional buffers and is enabled by the CE pin set low. Direction of data flow is controlled by the c.p.u. RD(L) output. RD set low enables data to be read in by the c.p.u. RD set high enables data to be written out by the c.p.u. This device only buffers data onto or off the board and is not used for on board data operations.

RAM, I/O and timer

112. IC2 contains 3 general purpose programmable I/O ports, a 256 bytes RAM and a programmable 14 bit counter/timer. At power on the device is initialized by the RESET OUT pulse from the processor. Input high on this line sets the 3 I/O ports to the input mode and stops the counter.

113. AD0 to AD7 3 state address/data lines interface with the c.p.u. lower 8 bit multiplexed address data bus. The 8 bit address is latched on the falling edge of ALE when the chip enable pin is low. The address can be for either the memory section (IO/$\overline{M}$ pin low) or the I/O section which includes the timer/counter (I/O $\overline{M}$ pin high), as selected by address line A11. 8 bit data is written in by WR low or read out by RD low.

114. Timer input is provided from the 250 kHz signal derived from the 10 MHz crystal oscillator on the motherboard A1. The programmed timer output (1 kHz) drives the RST 7.5 interrupt line to provide the real time 1 kHz clock for the microprocessor system. Timer output is also fed to the motherboard where it is retimed with processor SOD output and fed as a gating signal to the l.f. and h.f. counter units.

Chip selection

115. IC3 is a 3 to 8 line decoder which is enabled by IO/$\overline{M}$ low and A15. It decodes the address lines A12, A13 and A14 to provide chip select signals CS1 to CS7. CS1, CS2 and CS7 are NANDed in IC7a to enable the data buffer IC6. CS1 and CS2 are NANDed in IC7b and through IC7c to provide the enable signal (CS0) for the EPROM IC5.

CS L		ENABLES
1, 2	CS0	EPROM
3		GPIB or D to A Converter if fitted
4		KEYBOARD/DISPLAY
5		LF COUNTER
6		HF COUNTER
7		RAM, I/O, TIMER

EPROM

116. IC5 is an 8k x 8 bits EPROM which holds the operating program and test/diagnostic routines. It is enabled by CS0 held low and data is read when the output enable pin OE(L) is taken low by RD(L).

FREQUENCY STANDARD : UNIT A1

Circuit diagram : Chap. 7, Fig. 5

Internal 10 MHz

117. The internal standard frequency is provided by a high stability 10 MHz crystal oscillator whose supply voltage is regulated by IC2. R25 (SET 10 MHz) fed from the +10 V supply enables fine adjustment of the frequency to compensate for ageing.

118. With no external standard applied the INT/EXT select control line from IC10a is held high. This gates the 10 MHz oscillator output through the NAND Schmitt trigger IC12b to IC3a. IC3a is one half of a dual 4 line to 1 line data selector with select inputs (pins 14 and 2) common to both sections (IC3a and IC3b).

119. IC3a input select pin 14 is fed from IC12a whose output is held low by the pull up resistor at the input (10 MHz switch in open position). This enables IC3a to select the 10 MHz input (pin 4) from IC12b and pass it to the bi-quinary counter IC4a.

120. The 10 MHz oscillator frequency is made available at the STANDARD OUT socket via NOR gates IC11b and IC11d. 10 MHz (L) select signal from IC12a gates the 10 MHz oscillator signal from IC3a through IC11b to IC11d. Here it is gated through by IC11c output held low, to the output socket SKD.

121. IC4a 1 MHz output is fed to the second data selector IC3b. With input select pin 2 set high (INT H) the counter 1 MHz input is selected and passed to IC5a and then IC5b. These are edge triggered bistables connected for a divide by 4 function and provide a 250 kHz signal to the processor board timer (A8), the loop control board (A4) and tothe i.f. buffer (A5).

122. This 250 kHz signal is further divided by 10 in the bi-quinary counter IC4b and fed to the 25 kHz low-pass filter IC6a. The filtered signal is then subjected to a 90° phase shift by IC6b. An output is taken from each circuit and these signals 01 and 02 are fed to the offset driver AB1 for use during channel C operation.

Internal 1 MHz

123. With the 10 MHz/1 MHz switch set to 1 MHz position the circuits operate in the same manner as previously described for the 10 MHz internal standard with the following exceptions.

124. Input to IC12a is held low (1 MHz position to earth) and so the output to select pin 14 of IC3a is set high. The 10 MHz input at pin 3 is selected, passed to decade divider IC4a and the 1 MHz output fed to IC3b. With select pin 2 still held high (INT), IC3b selects the 1 MHz input at pin 13 and passes it to bistable IC5a for action as previously described.

125. The 1 MHz output from IC3b is gated through IC11c by the low input from the 1 MHz switch position. The 1 MHz select line is set high and this disables IC11b setting low the input to gate IC11d. 1 MHz frequency is now passed through IC11d to the STANDARD OUT socket SKD.

External 10 MHz

126. The 10 MHz external standard input is amplified by IC1 and fed to the data selector IC3a. Diodes D1 and D2 provide input voltage protection by conducting to ground if an input greater than 3 V is applied.

127. The amplified signal is also fed to the d.c. triggered multivibrator IC10a. The active high input produces a negative pulse which is used to close the internal standard gate IC12b and provide the select signal for data selector IC3b. It is also passed as the select signal (EXT L) to board A8 where it is read by the processor which causes the EXT annunciator to be displayed.

128. With select signals at pins 14 and 2 set low (10 MHz L, EXT L) IC3a selects at pin 6 the external standard input from IC1. This is passed to the decade divider IC4a and the 1 MHz output is selected at pin 10 by the second data selector IC3b. It is passed to IC5 and IC4b for division as described for the internal standard operation.

129. The 10 MHz external standard is alsomade available at the STANDARD OUT socket via NOR gates IC11b and IC11d in the same manner as the internal 10 MHz standard. That is 10 MHz L to IC11b gates through the external 10 MHz standard to IC11d. Have the low input from IC11c gates the 10 MHz through to the output socket SKD.

External 1 MHz

130. The external 1 MHz standard input is amplified and detected and the EXT annunciator is activated in the same way as that described for the 10 MHz external input operation.

131. The EXT L input from the detector IC10a closes the internal standard gate IC12b and provides the select input signal to IC3b pin 2.

132. 1 MHz switch position sets input to IC12a low which sets the output high. This provides the input select signal to IC3a which selects the 1 MHz input at pin 5. The 1 MHz signal is now fed directly to the second data selector IC3b pin 11 and passed to IC5 and IC4b for division as described previously.

133. NOR gate IC11a has both inputs set low. These are EXT L from the detector IC10a and 0 V via the 1 MHz switch position. IC11a output is therefore set high and this clears the bypassed decade divider IC4a.

134. The 1 MHz external standard is also made available at the STANDARD OUT socket via NOR gates IC11c and IC11d in the same way as the internal 1 MHz standard. That is, 0 V from the 1 MHz switch position gates the 1 MHz output of IC3b through IC11c to IC11d. Here the low input from IC11b gates the 1 MHz through to the output socket SKD.

KEYBOARD : UNIT A2

Circuit diagram : Chap. 7, Fig. 9

135. The keyboard comprises all the front panel key switches, a keyboard latch and three l.e.d's with a latch for channel indication. Use of the keyboard is controlled by the microprocessor on unit A8 in conjunction with display board A3.

Keyboard operation

136. Key switches are organized in a 4 x 4 array. Keyboard latch IC1 normally has all outputs set low. Diodes D4 to D7 in these output lines prevent the output levels being connected in parallel if more than one key in a row is pressed at the same time.

137. When a key is pressed the low state from IC1 is transferred through the closed switch to the interrupt gate on the display board A3. An interrupt is raised requesting keyboard service and on responding the processor initiates a scanning program to determine which key is pressed.

138. The program sends data patterns to the keyboard latch IC1 which is enabled by setting high the enable line on pins 13 and 4. The results are read by the keyboard read buffer (IC1) on the display board.

139. The scanning program sets high all but the right-hand column (col. 3). If the key pressed is in this column then the row line of that key is forced low. If not the row lines will remain high. The next column is then set low with the others held high and the process repeated until all the columns have been scanned. In this way the column and row information uniquely identifies the key pressed. This is converted into a key image which the processor interprets and then actions the appropriate function. The scanning program allows for contact bounce and resets the latch when a valid key code has been found.

140. When set to REMOTE by the GPIB only the column containing the local switch is low with the other outputs held high to disable all other keys. When in REMOTE/LOCAL LOCKOUT all the outputs are latched high to prevent the keys from raising an interrupt to the microprocessor.

Channel indicators

141. Channel indication is by 3 l.e.d's D1, D2, D3 which are driven from latch IC2 which is in turn driven from the microprocessor bus. Switch SD indicates to the processor that the channel A/B switch has been pressed and switch SC indicates that channel C has been pressed. Subsequent action is then determined by the processor.

142. The l.e.d's are turned on by taking low the relevant output of latch IC2. The latch is addressed by setting high the enable pins 13 and 4 from the decoder IC5 (4003 WR(L)) on display board A3. The required data code is then written to the latch on data linesa D1, D2, D3 from the processor.

DISPLAY BOARD : UNIT A3

Circuit diagram : Chap. 7, Fig. 11

143. The display board contains the liquid crystal display, display drivers and the control logic circuitry required to interface the keyboard and the display drivers to the address/data bus.

Interrupt RST 5.5

144. IC2a is a 4 input NAND gate that monitors the 4 row lines from the keyboard. With no keys pressed, lines from the keyboard are open and all inputs to the gate are held high by the pull up resistors R1 to R4. Gate output is in the low state - no interrupt. When a key is pressed that input line to the gate is pulled low and gate output goes high raising an interrupt request RST 5.5 to the processor for keyboard service.

Decoding

145. The processor, when responding to the interrupt, enables and addresses the decoder IC5. IC5 then enables the keyboard latch and the keyboard read buffer as required to run the keyboard scanning program.

146. Chip select line CS4 L enables the dual decoder IC5 and RD L or WR signals select one of the two internal decoders. Address lines A0 and A1 are decoded to produce active low outputs on pins 4, 5, 6 and 7. These are inverted by IC3 and used to enable IC1 and IC2 the l.e.d. and keyboard latches on the keyboard and IC4a and IC4b the display driver latches. A fifth output from IC5 asserted low enables the keyboard read buffer IC1.

Display operation

147. Control signals and data are fed via latches IC4a and IC4b to the display drivers which then drive the display.

148. The displays on the liquid crystal display unit are driven using three CMOS LSI circuits IC6, IC7 and IC8 connected in cascade. These integrated circuits each contain a shift register, latches, segment drivers and an oscillator. Fig. 3 shows the display driver in block diagram form.

149. Display data on D0 line is fed to latch IC4a which is enabled by the low level from IC3d. Data is in the form of 96 bits serial input with IC6 input shift register overflowing into IC7 and then into IC8 shift register via the data out/in connections. CLOCK and LOAD control signals for the display drivers on D1 and D0 lines are latched by IC4b.

150. Data information latched by IC4a is loaded into IC6 shift register with every clock pulse. The contents are shifted along with each data input until the register is full. The LOAD line is then asserted high which causes a parallel load of the data in the registers into the latches that control the segment drivers. Driver output is an a.c. voltage generated by the on chip oscillator.

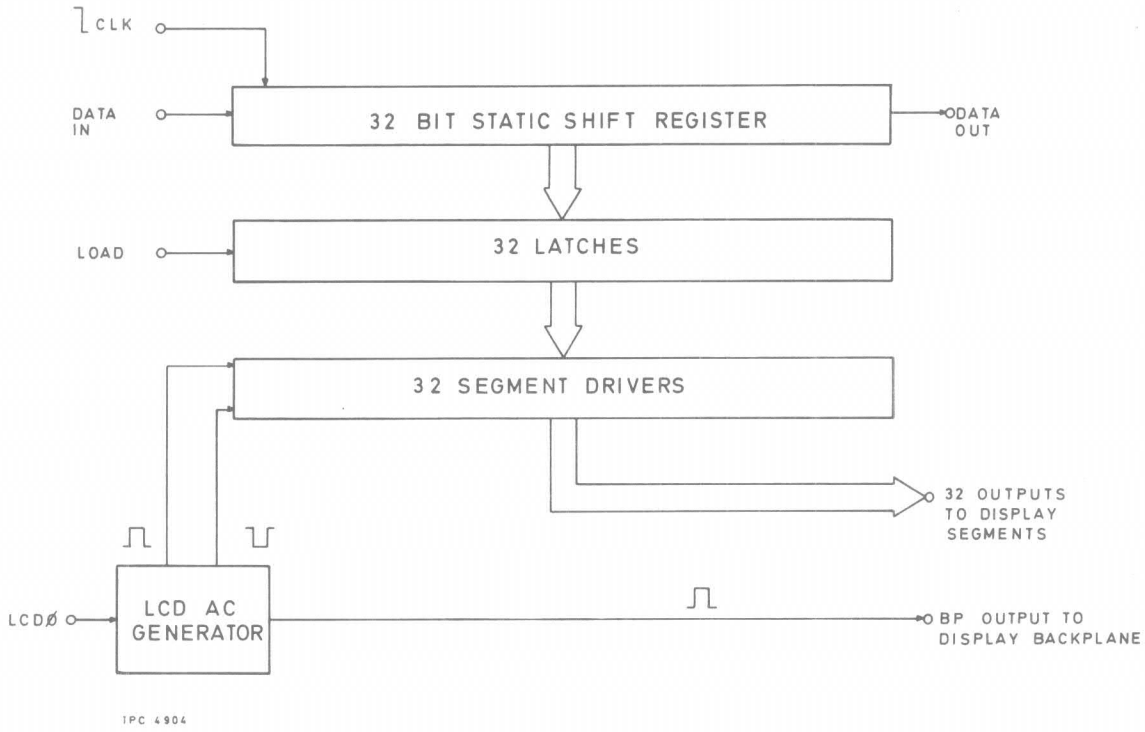


Fig. 3 Display driver : block diagram

151. The oscillator in IC6 generates a 50 Hz square wave voltage (frequency determined by C7) which is applied via the drivers to the individual display segments. The 50 Hz square wave voltage from IC6 is coupled to IC7 and then IC8 input pin 31 and used as the source for IC7 and IC8 drive to the display segments. This same square wave voltage is fed from IC8 pin 30 to the liquid crystal display unit backplane which forms the common electrode connection to the crystal displays.

152. With no data in to IC6, IC7 and IC8 the square wave drive to the display segments is in phase with that applied to the display backplane. As there is no potential difference across them, the crystals are not excited and the segments remain non-visible.

153. When the DATA IN line is asserted high and clocked and loaded, the driver latch output changes to an out of phase square wave voltage to the display segment electrode. The crystals for the selected segment are excited (scattered) and the segment becomes visible.

GPIB INTERFACE UNIT

Circuit diagram : Chap. 7, Fig. 23

154. The function of this unit is to provide communication between the 2440 and the General Purpose Interface Bus (GPIB).

155. The GPIB controller directs the flow of data on the GPIB which uses 16 lines to connect all units of the system in parallel. These lines are coupled directly to the GPIB interface board where a talker/listener integrated circuit and bi-directional buffers implement the interface functions.

Circuit description

156. IC3 is a talker/listener device which in conjunction with transceiver ICs 4, 5, 6 and 7 and address reader IC2, implements all the necessary GPIB functions for the instrument. It is processor controlled and has capabilities which include data transfer, handshake protocol, talker/listener address recognition, service request and serial poll.

157. Switch bank SW1 is the GPIB address switch which enables the GPIB address to be programmed. Five of the rocker switches set the address in binary format 1, 2, 4, 8, 16 for talk and listen modes. The sixth switch is set for talk only mode. The switches configure the address in negative logic : when a switch is open one of the pull-up resistors R1 to R6 holds the input high at logical '0', when a switch is closed the input is connected to earth for logical '1'. IC2 is a tristate-gated driver which, when enabled by CS and A3 both being taken low, places the switch settings on the D0 to D5 lines to IC3 for address recognition purposes.

158. Talker/listener IC3 takes care of data transfer as well as decoding control messages. Control messages and addresses are passed on the data bus by means of the handshaking process with ATN asserted by the controller to differentiate them from data. Control messages such as SPE, SPD used for serial poll are decoded and the function carried out. The IC also performs address recognition. During this phase, the data on lines D101 to D105 is compared for equivalence with data on the AD0 to AD4 lines from address reader IC2. When a possible address is recognized and providing certain other conditions are satisfied, the data on lines D106 and 7 is decoded to determine whether the instrument is being addressed as a talker or a listener. When designated a talker by the controller, the interface transfers data from the processor by means of a talk handshake to the listeners. It is sent via an internal register to the transceivers which are configured to send. When designated a listener by the controller - and providing Talk Only is not set on SW1 - data is received via the transceivers, which are configured to receive by means of the listen handshake and stored in an internal data register.

159. IC3 contains 16 read/write registers (8 read, 8 write), 2 for direct data transfer the rest for interface control, status etc. Address lines A0, A1 and A2 from motherboard AB1 are used to select the required internal read/write register in conjunction with the WR and RD lines. When the A3 line is taken high and the CS3 line is asserted low, decoders IC1a and IC1b take the CS input low which enables reading to or writing from the selected register. The interrupt request output INT is connected to the RST 6.5 input of the processor and is asserted high for request.

160. Data flow to and from peripherals and controller is via transceivers IC4 to IC7 with the direction of data transfer controlled by the T1/R1 line being taken high for outputs and low for inputs. Additionally, this line is used for the handshake process. For example, a low on the line, after inversion by IC1c, enables the listener signals NRFD and NDAC to be asserted low on the bus while reinversion by IC1d ensures that the complementary DAV talker function is simultaneously disabled. The sole function of T2/R2 is to set the bus management EOI line low for reception or high for transmission.

161. Fig. 4 shows the General Purpose Interface Bus structure with the 16 lines sub-divided into data, interface management and transfer. Bus and line functions are described below.

General purpose interface bus structure

Data bus

162. Comprises 8 data input/output lines DIO 1 to 8 and is used to transfer the data (commands, addresses and instructions) in bit parallel, byte serial form.

Interface management bus

163. Manages the orderly flow of data across the interface and consists of 5 wires carrying the following signals:

Interface clear (IFC); sent by the station controller to clear all device interfaces so that they set to an initial condition.

Remote enable (REN); sent by the controller to enable instruments to be placed under remote control.

Attention (ATN); sent by the controller to indicate that an address or command is on the data lines.

End or identify (EOI); an instrument or controller signal sent to indicate the end of a message.

Service request (SRQ); sent to the controller by an instrument to indicate that it needs service.

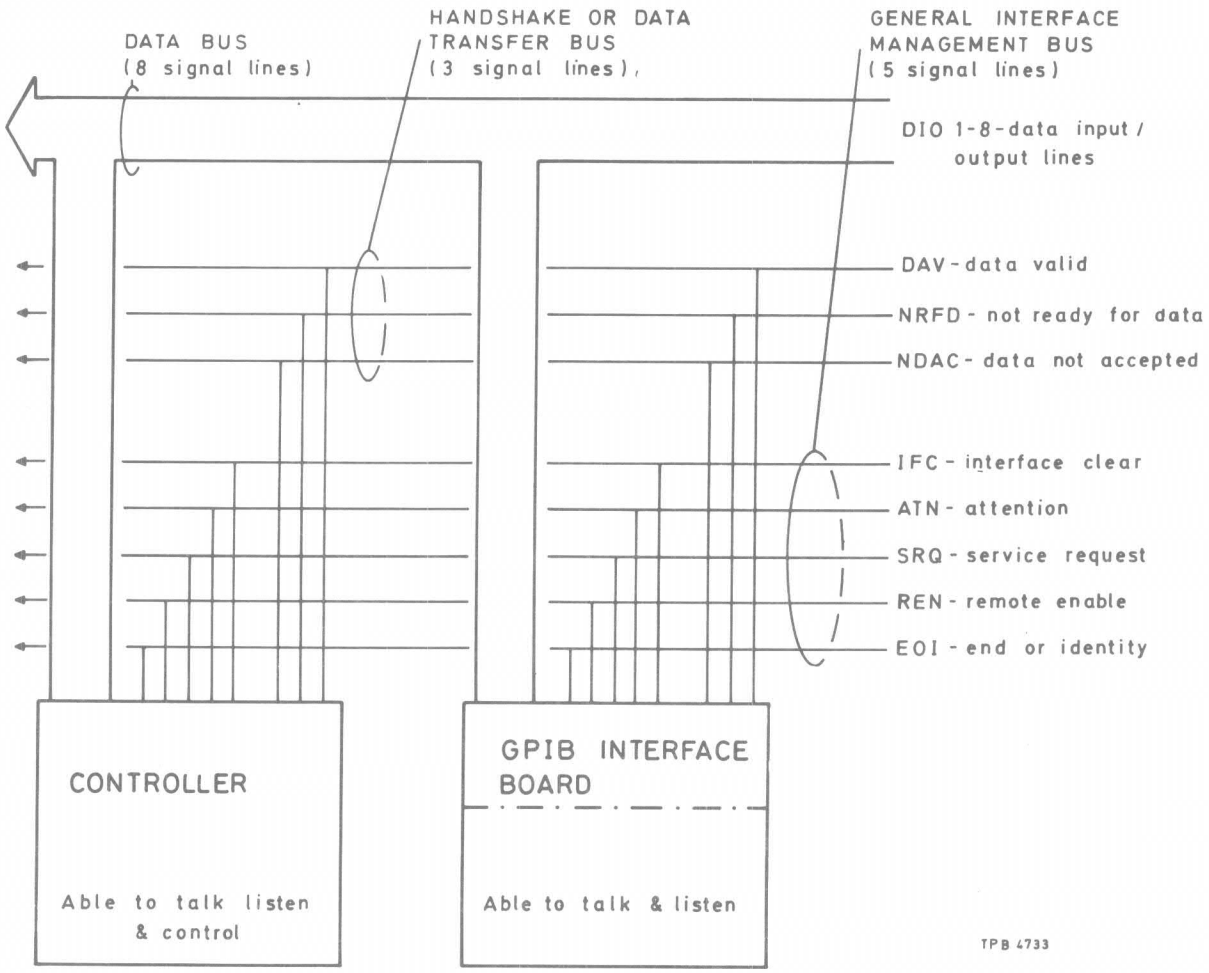


Fig. 4 General Purpose Interface Bus structure

Handshake or data transfer bus

164. Co-ordinates the flow of data and comprises 3 lines which are used for the handshaking process, by which a talker or controller synchronizes its readiness to send data with a listener's readiness to receive data. The handshake signals are:

Not ready for data (NRFD); asserted (low) by a listener when it is active and not yet ready to receive data. Set high to signal its readiness to receive data, DAV can then be signalled if further data is to be processed.

Data valid (DAV); asserted by a talker to indicate that the data it has placed on the data bus has settled and may be accepted.

Not data accepted (NDAC); asserted by a listener when receiving information from the data lines. Release of the NDAC line tells the data source that new data can be submitted.

Bus operation

165. (i) A sequence of messages may be commenced by the controller asserting IFC on the management bus to set the interface to its initial condition.

(ii) The controller then sets up which instruments are to be listeners by asserting ATN and handshaking the personalized listen address of these instruments over the bus. Similarly the controller designates the talker (only one instrument may talk at a time) by sending its talk address, again with ATN asserted.

(iii) On release of the ATN command (ATN low) the talker is then able to place data on the data lines DIO 1 to 8, the transfer of this is controlled by the handshake process and is received by all addressed listeners. The talker typically concludes the sequence by asserting EOI and the controller then resumes control.

(iv) Both the talker and the listeners may be switched by the controller into an inactive state by asserting IFC and UNL (unlisten) on the data bus.

Handshake procedure

166. The handshake is used whenever data is transferred on the bus. When a signal is asserted the function indicated by the line is carried out, e.g. NRFD is asserted to signify the listener's unreadiness to receive data, and unasserted or removed when ready to receive data. A typical handshake is as follows:

(i) Talker (controller) places a byte on the data bus with DAV initially unasserted to show data is not yet valid.

(ii) When all listeners are ready to receive data NRFD is removed with NDAC at this time asserted.

(iii) After a delay to allow the data bus to settle, talker asserts DAV to show data is valid and may be accepted.

(iv) Data byte is transferred, then listeners assert NRFD. When all the listeners have accepted the byte NDAC is removed to signify receipt.

(v) Talker removes DAV, listeners assert NDAC, and the bus reverts to its initial condition ready for the next data byte, a typical cycle is shown below in Fig. 5.

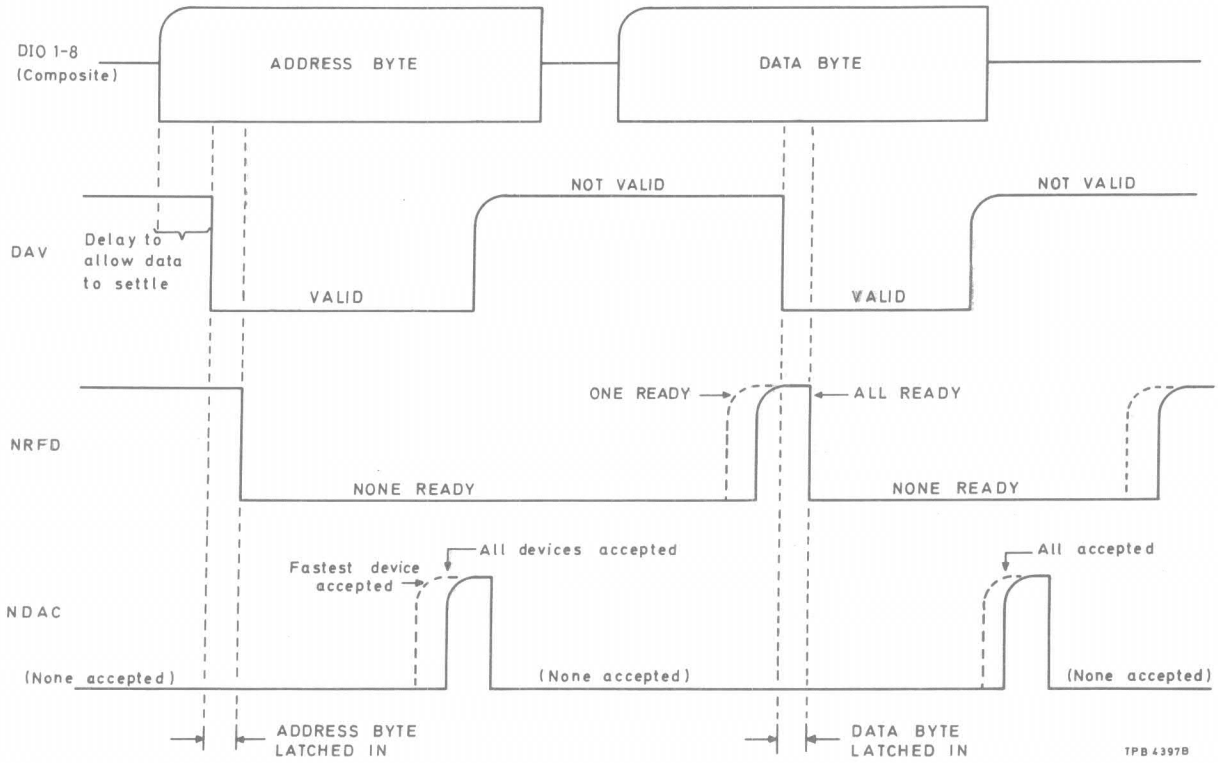


Fig. 5 Handshake procedure

DIGITAL TO ANALOGUE CONVERTER UNIT

Circuit diagram : Chap. 7, Fig. 25

167. This unit is an optional item and provides, under processor control, a voltage output proportional to three selected decades of frequency data. The unit is fitted in place of the supplied GPIB unit. The selected decades are converted to an analogue voltage in the range -1 V to +1 V which is made available at the rear panel connector.

Circuit description

168. On power up the three most significant decades are selected and may be changed later by keyboard selection. The selected data is sent by the processor to the data inputs of IC1.

169. IC1 is a 12 bit c.m.o.s. multiplying digital to analogue converter circuit and interfaces directly to the microprocessor board A8. It comprises three 4 bit data registers, a 12 bit d.a.c. register, address decoder and a 12 bit multiplying digital to analogue converter.

170. Data input is in the form of three 4 bit words. With the CS line (CS3) held low and addressed on lines A0, A1 data is latched into the three registers by the low to high transition of the WR(L) command. The most significant address together with WR(L) transfers the data into the 12 bit d.a.c. register which drives the converter.

171. The processor always sets the most significant data bit D11 to 0. The next data bit D10 is used as a sign bit (1 = +ve, 0 = -ve) and remaining data is entered on D0 to D9.

172. Current output from IC1 (IO1) is buffered by precision op-amp. IC2 where it provides an output between 0 and -2 V which is also fed back to the converter.

173. V ref. for the converter (4.096 V) is provided by D1 which is a temperature compensated band gap diode giving a stable output of 2.45 V. This is then scaled up by precision op-amp. IC3 set by variable R5. This circuit also provides the bipolar offset voltage to IC4 set by variable R10.

174. The outputs from IC2 (d.a.c. output voltage) and IC3 (bipolar offset) are summed, inverted and buffered by precision op-amp. IC4 to give an output of -1 V to +1 V. Low-pass filtering of the output is provided by R13, C13 and C15.

175. The scaled range of the output is determined by varying R5 (SET REF) and the +/- offset by varying R10 (SET BIPOLAR). New data fed to IC1 by the processor will overwrite the existing data in the registers to produce a new analogue output voltage.

POWER SUPPLY

Circuit diagram : Chap. 7, Figs. 2 and 5

176. The power supply input circuit comprises an a.c. mains input filter, two time lag fuses and mains transformer with two tapped primary windings linked in series or parallel by two switches. These switches, SD and SC, provide a choice of two input voltage ranges allowing operation from any voltage between 105 V a.c. to 120 V a.c. and 210 V a.c. to 240 V a.c.

177. Three transformer secondary windings feed three bridge rectifiers which supply the positive and negative unregulated a.c. voltages to the regulator circuits on the motherboard A1. These regulators provide d.c. supplies of +10.5 V, +5 V and -5 V.

178. The +10.5 V d.c. supply operates the front panel l.e.d. D4 to indicate that a mains supply is connected and that the standard 10 MHz crystal oscillator is running, even in the STANDBY condition. With the ON/STANDBY front panel switch in the STANDBY position, the +5 V and -5 V regulators are held in the off state by the interruption of the control voltage which is derived from the +10.5 V supply. Switching from STANDBY to ON activates the ventilating fan which is supplied from the +5 V rail.

+10.5 V supply : Unit A1

Circuit diagram : Chap. 7, Fig. 5

179. The +10.5 V supply voltage is regulated by TR4 and IC7. IC7 contains a complete voltage regulator with current sensing and limiting and a series regulating element whose output drives the larger current capacity series element TR4.

180. Setting of the +10.5 V supply voltage is achieved by adjustment of variable R21 which forms part of a potential divider connected between the supply line and earth. This sets the inverting input level to IC7 which provides the steady state controlling voltage to TR4.

181. If current consumption increases, the voltage across the potential divider and consequently input to IC7 falls. IC7 responds by amplifying the difference voltage and driving TR4 harder which reduces the voltage drop across it. This causes the +10.5 V line voltage to rise to the previously set value. Should the current consumption decrease then the regulating circuit will operate in the reverse manner to restore the line voltage.

+5 V supply : Unit A1

Circuit diagram : Chap. 7, Fig. 5

182. The +5 V regulated supply is a conventional series regulator circuit with TR5 as the series element. This is controlled by driver TR6 and operational amplifier IC8a.

183. The negative (inverting) input of IC5 is connected to the +5 V regulated line and the positive input is connected to the variable resistor R26. The voltage across R26, which is derived from the +10.5 V supply via the ON/STANDBY switch and R24, is stabilized by Zener diode D6 and provides the reference voltage to IC8a.

184. Increasing the reference voltage to IC8a produces a greater input to TR6 which provides more drive to TR5. This effectively decreases the resistance across TR5 due to the extra current drawn, and results in the supply line voltage rising. When the reference voltage is decreased the circuit operates in the reverse manner. Thus R26 is used to accurately set the +5 V supply voltage.

185. Because input voltage levels are not established instantaneously at switch on, IC8a output could possibly swing negative. This would result in excessive voltage across TR6 base/emitter junction. D7 connected across this junction ensures that any transient voltages of this nature are conducted away from TR6.

186. With the reference input voltage fixed by R26, IC8a gain is controlled by the inverting input and provides voltage regulation under normal operating conditions in the following way.

187. If the +5 V line voltage decreases (due to increased current consumption) then IC8a responds by amplifying the difference voltage. This causes TR6 to drive TR5 harder and as the voltage across the series element falls, the +5 V line voltage rises to the previously set value. If the +5 V line voltage increases above the set value, then the control circuit will operate in the reverse way to restore the line voltage.

-5 V supply : Unit A1

Circuit diagram : Chap. 7, Fig. 5

188. The -5 V regulated supply is a conventional series regulator circuit with TR8 as the series element. This is controlled by driver TR7 and operational amplifier IC8b.

189. The positive input of IC8b is connected to earth and the negative (inverting) input is connected via potential divider R29/R30 to the variable resistor R26. Setting of the -5 V line voltage and operation of the regulating circuit is the same as that described for the +5 V supply.

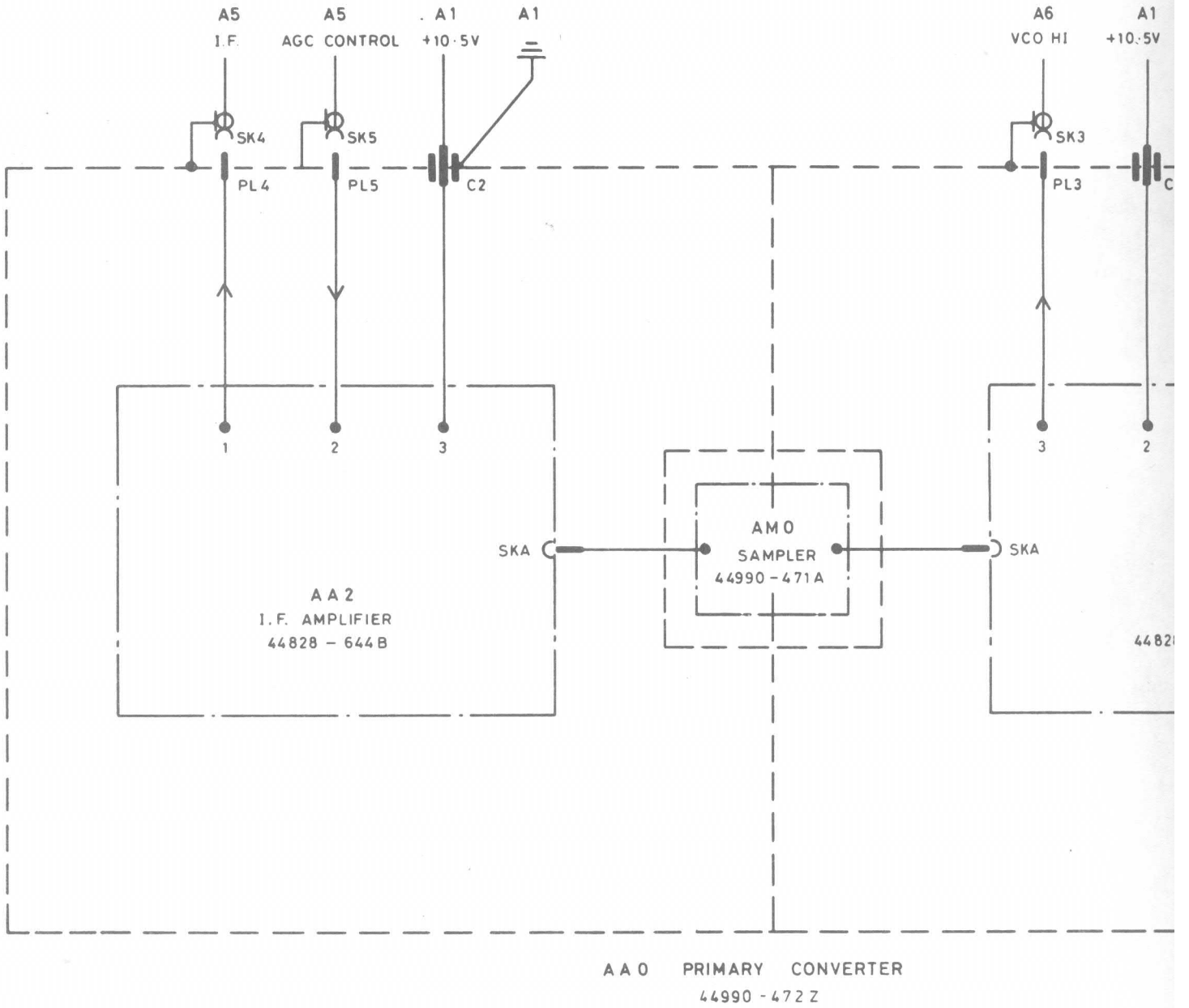
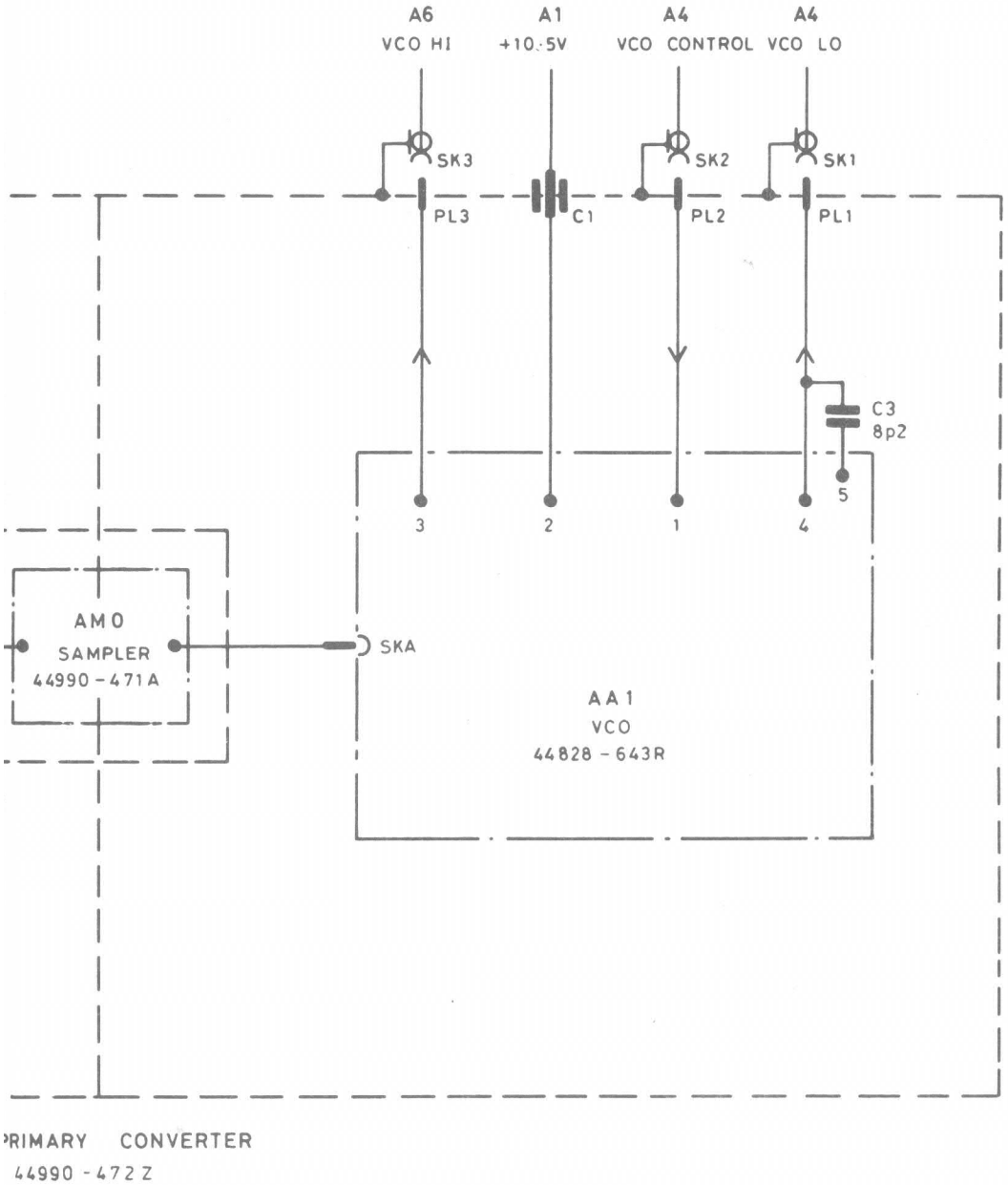


Fig. 6 AA0 Primary converter, interconnection diagram



PRIMARY CONVERTER
44990-472Z

werter, interconnection diagram

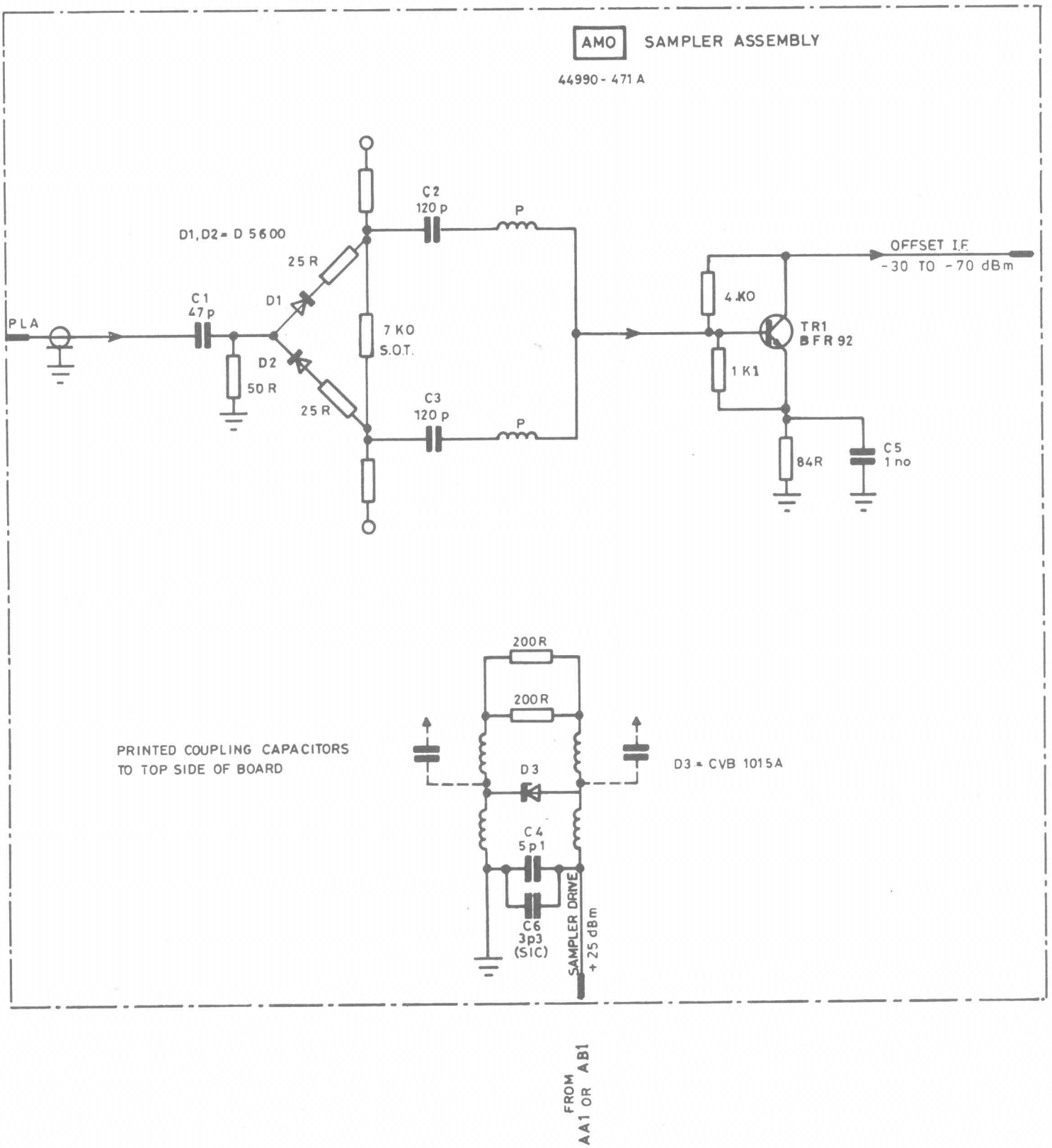
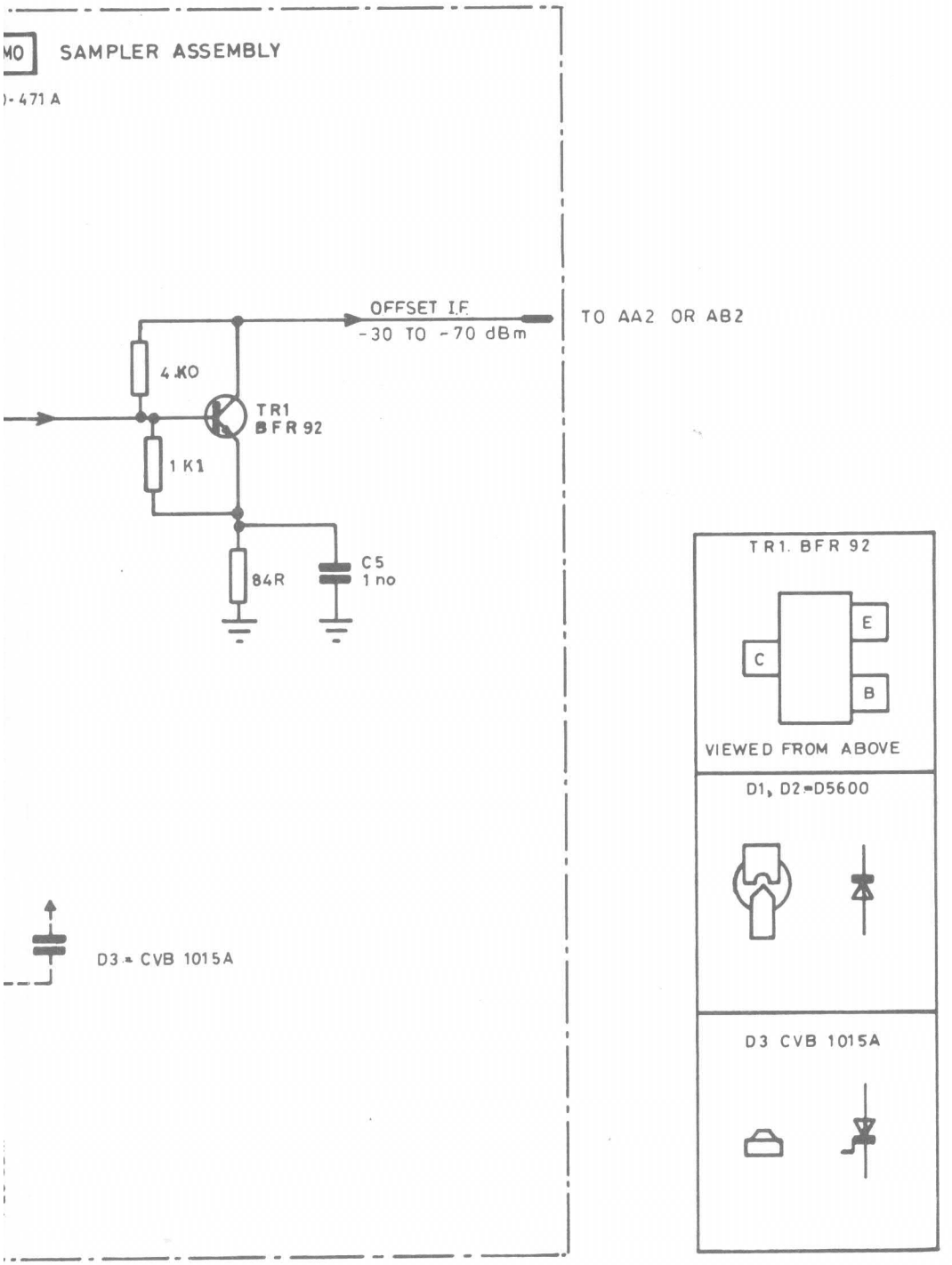
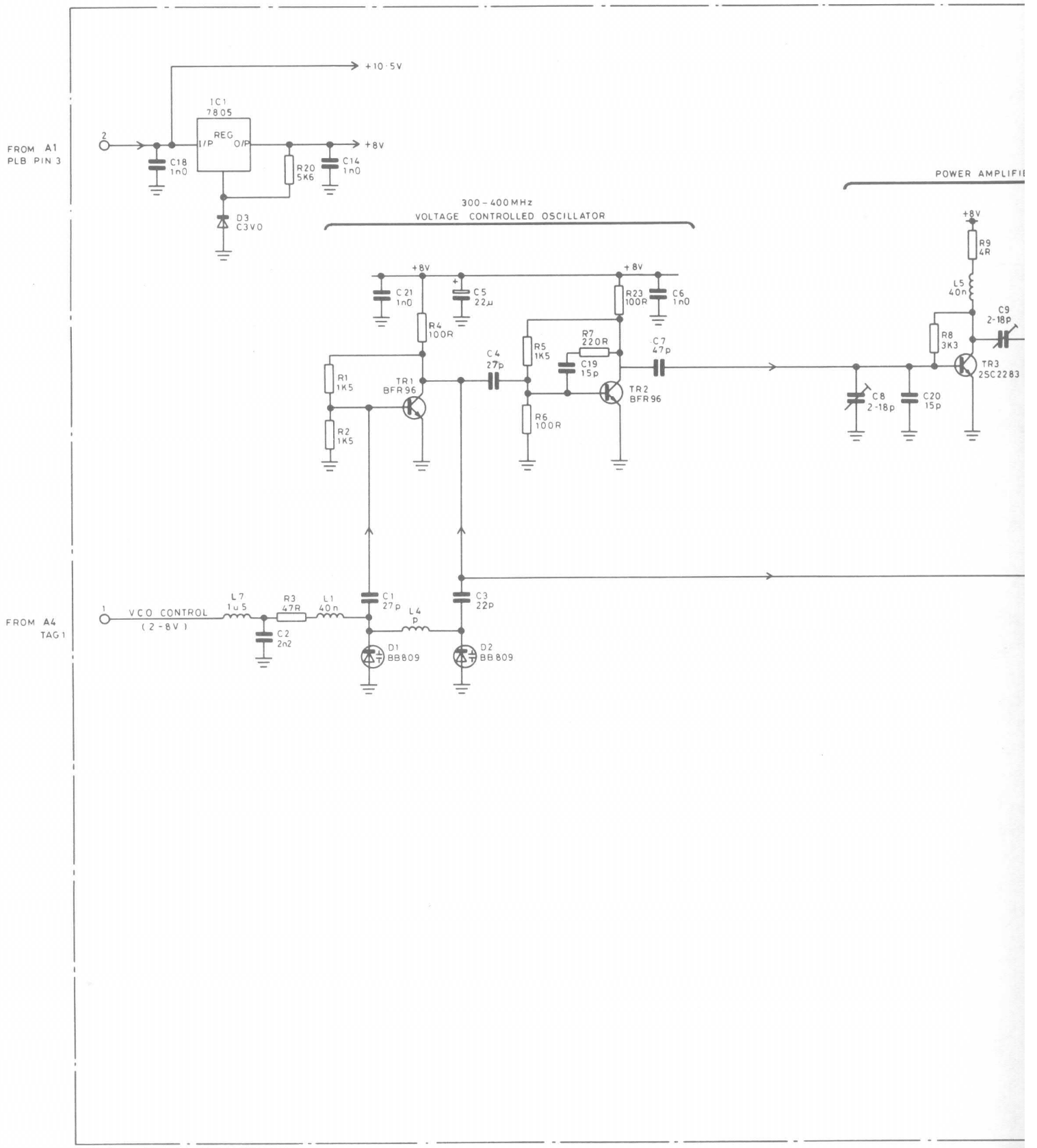


Fig. 7 AMO Sampler unit

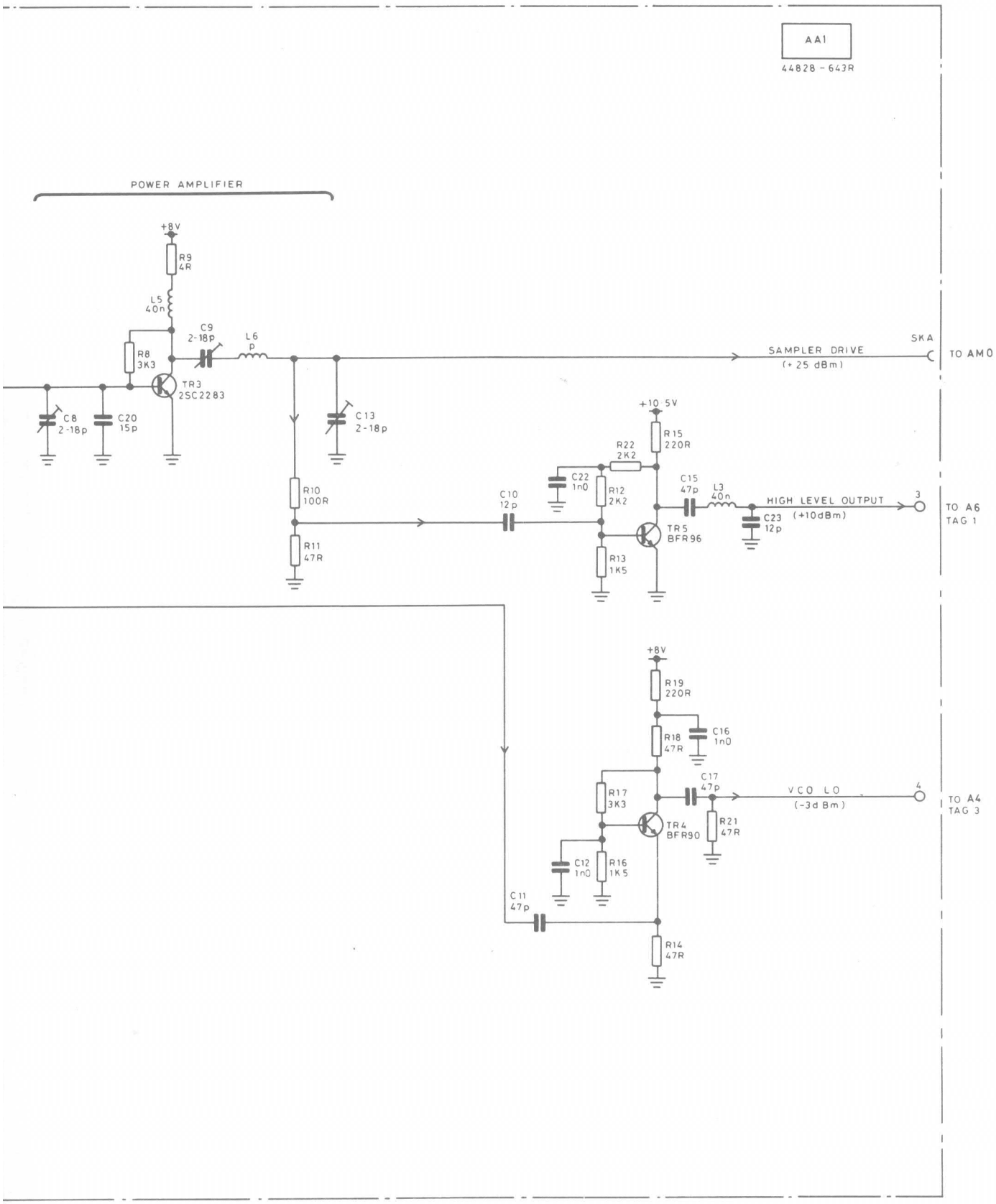


) Sampler unit



Z44828-643R Iss. 4

Fig. 8 AA1 Voltage controlled oscillator



ntrolled oscillator board, circuit diagram

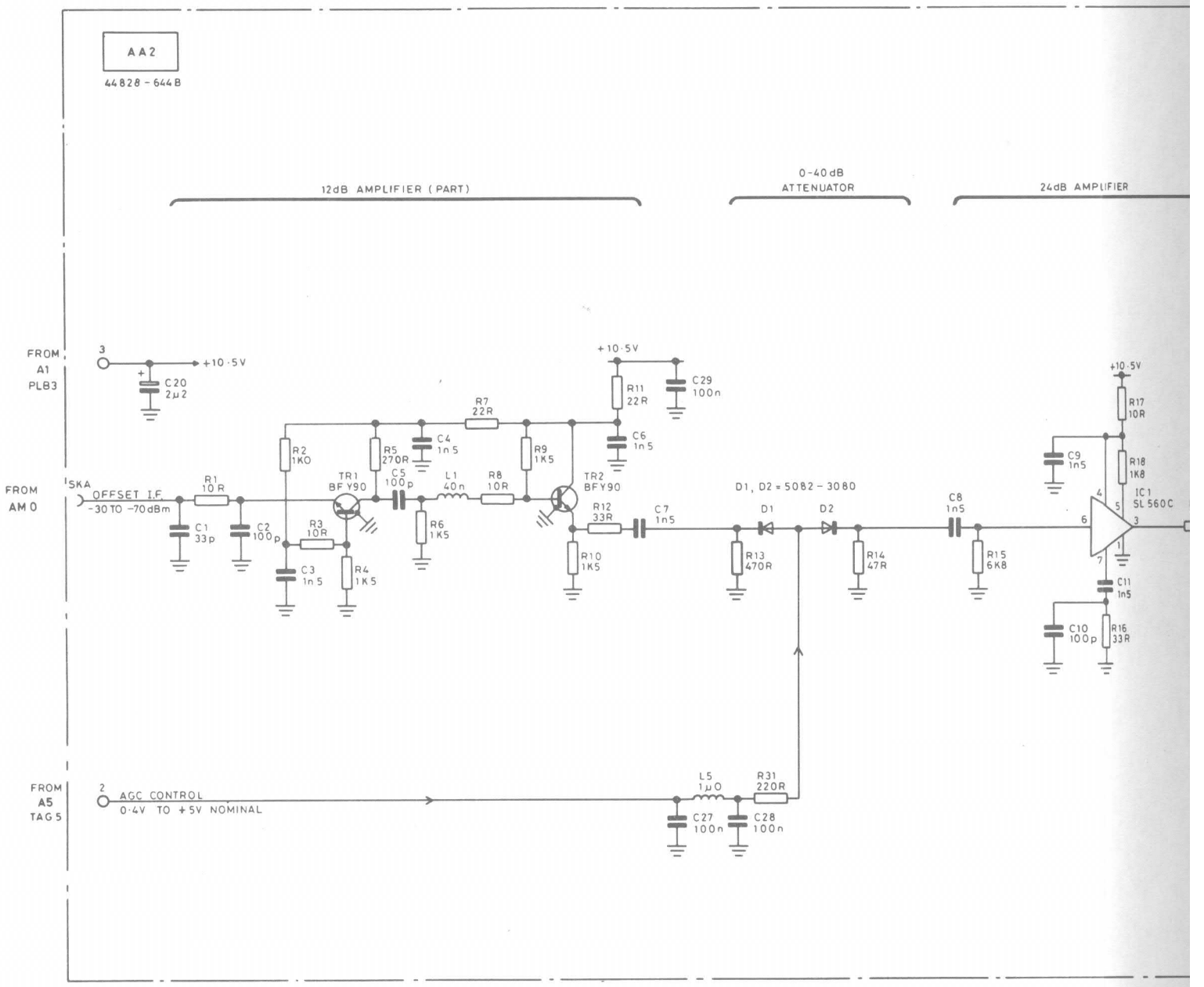


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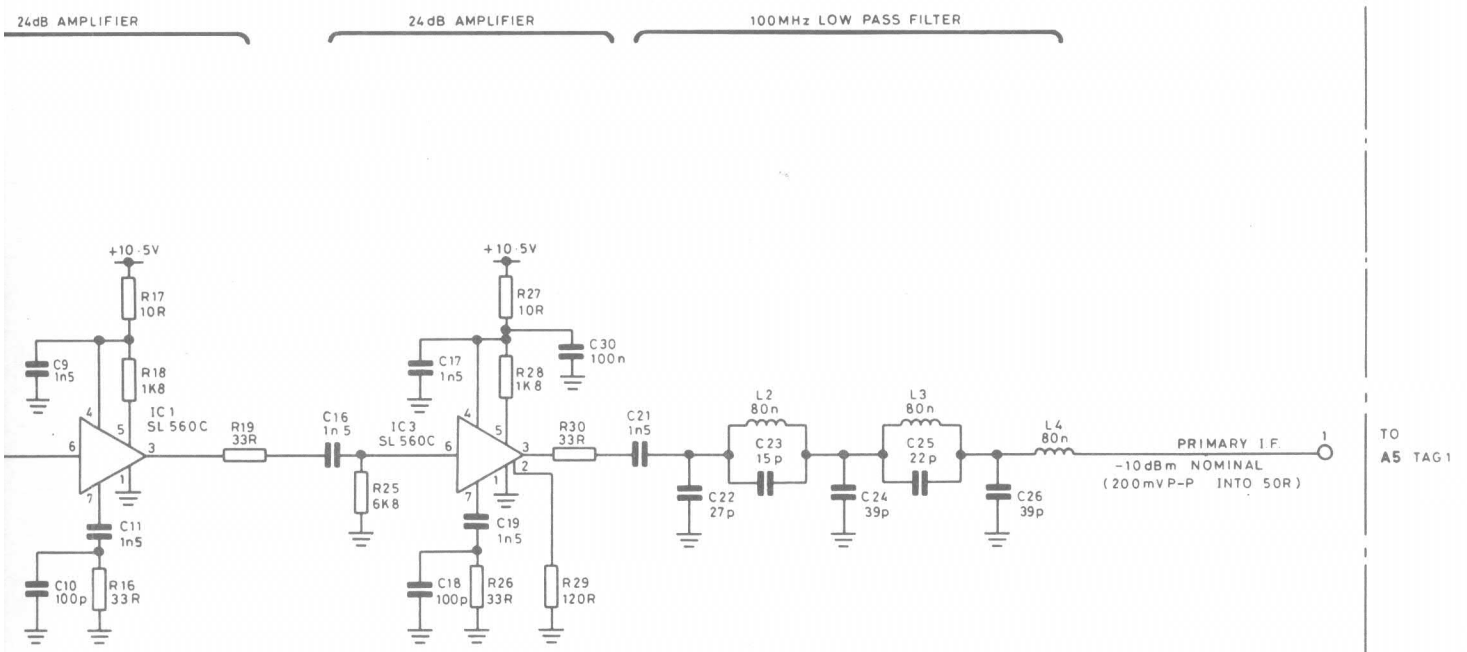
Fig. 9 AA2 IF amplifier board,



plifier board, circuit diagram

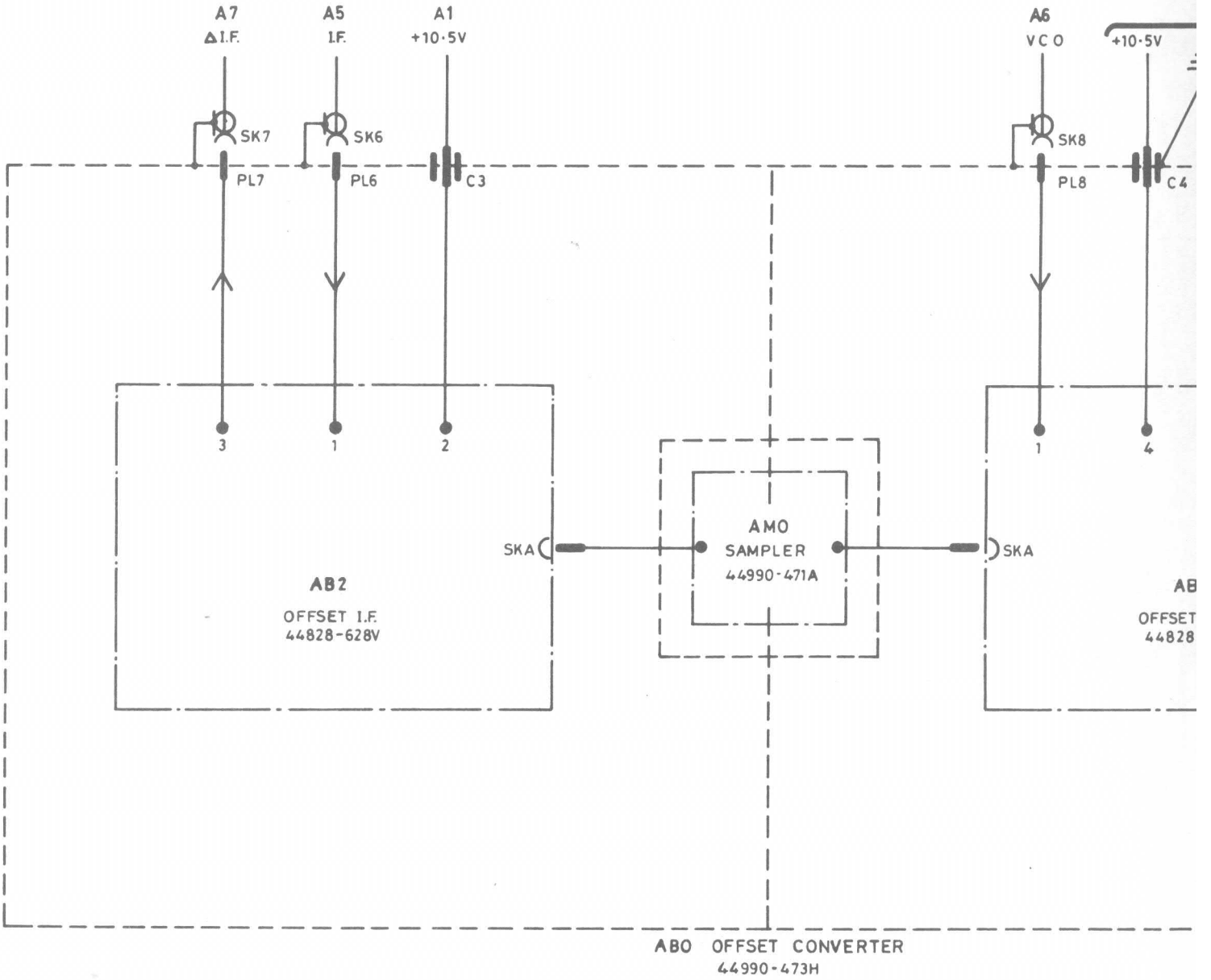
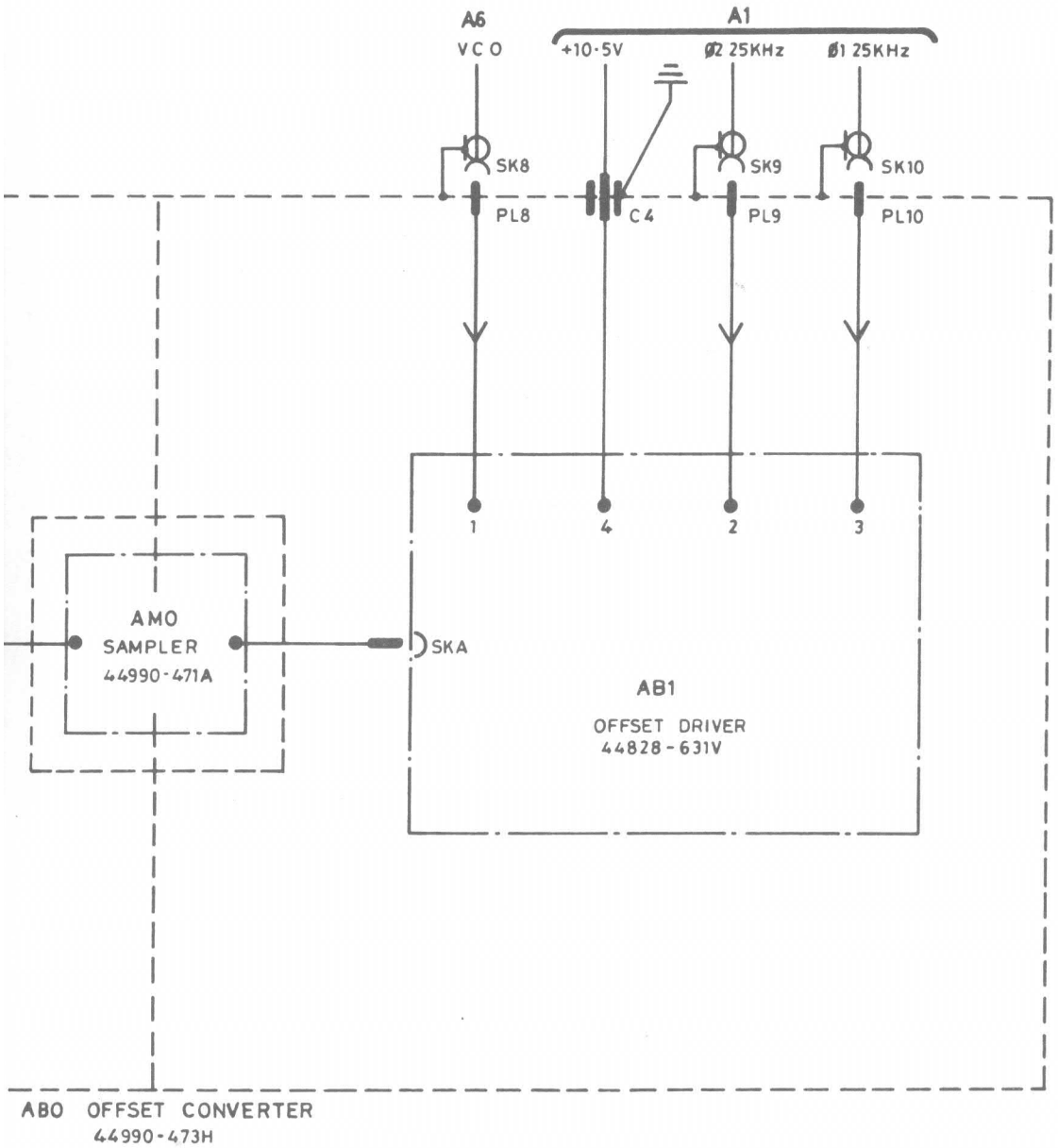


Fig. 10 AB0 Offset converter, interconnection diagram



converter, interconnection diagram

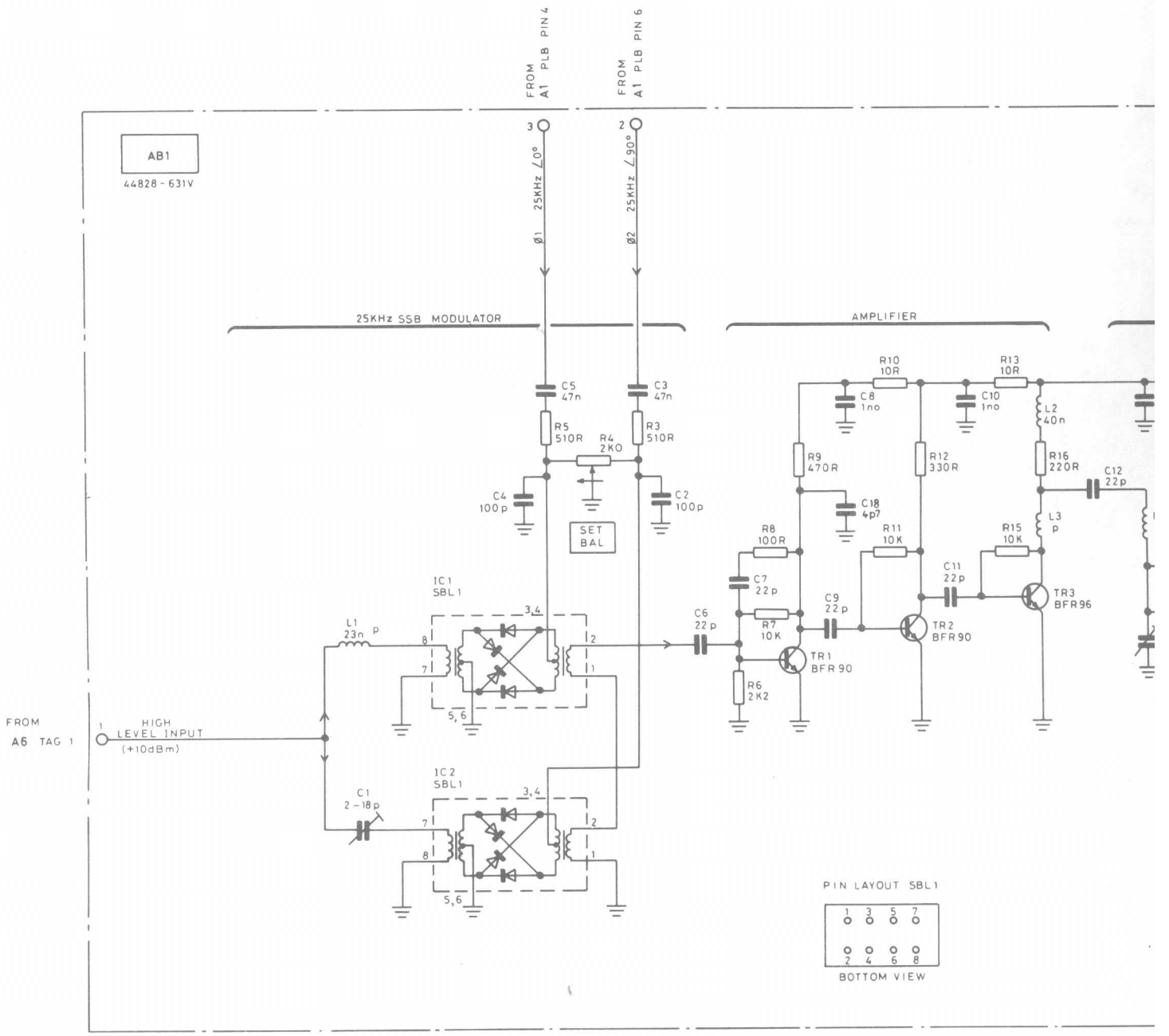
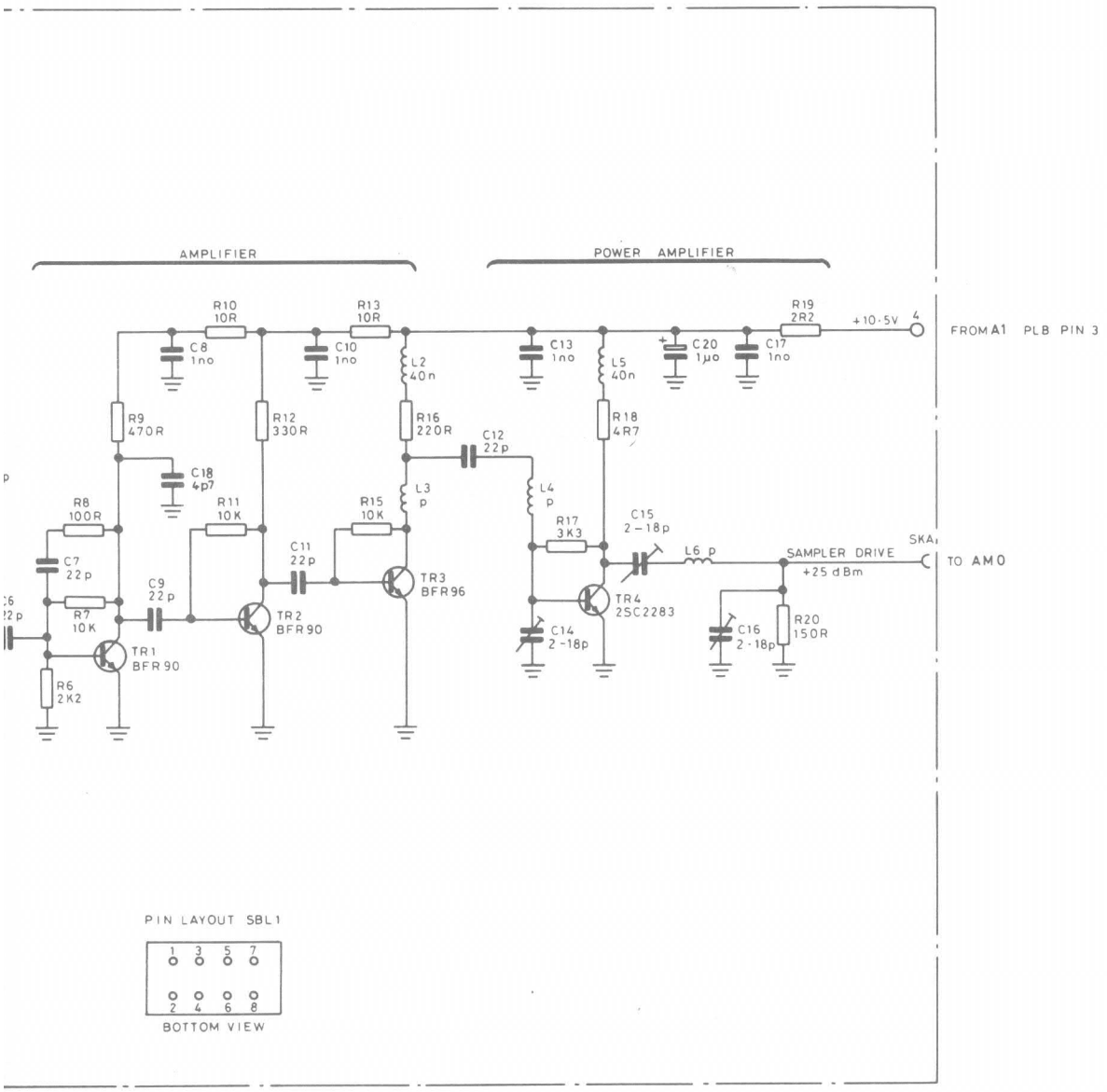
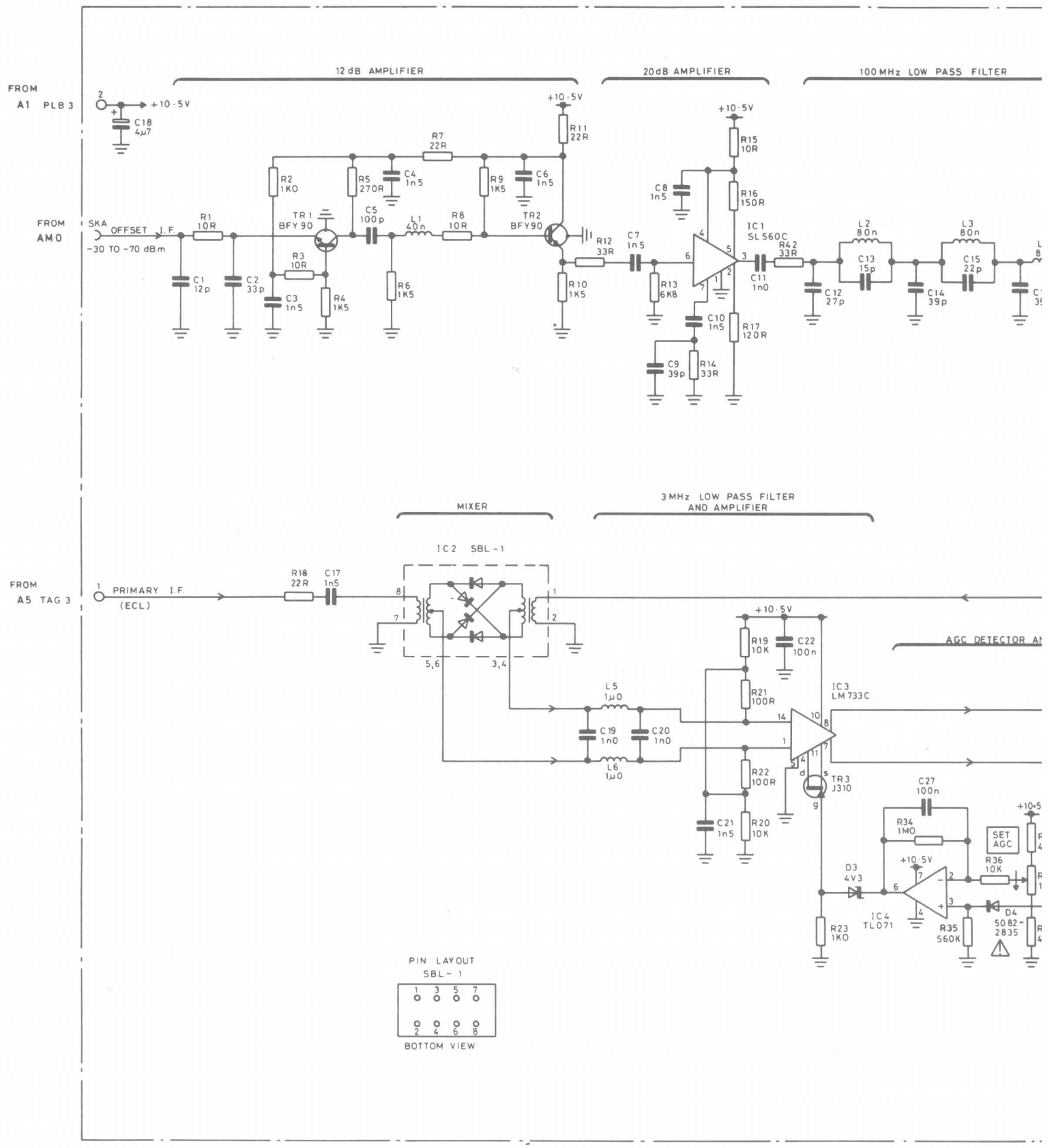


Fig. 11 AB1 Offset driver board, circuit diagram

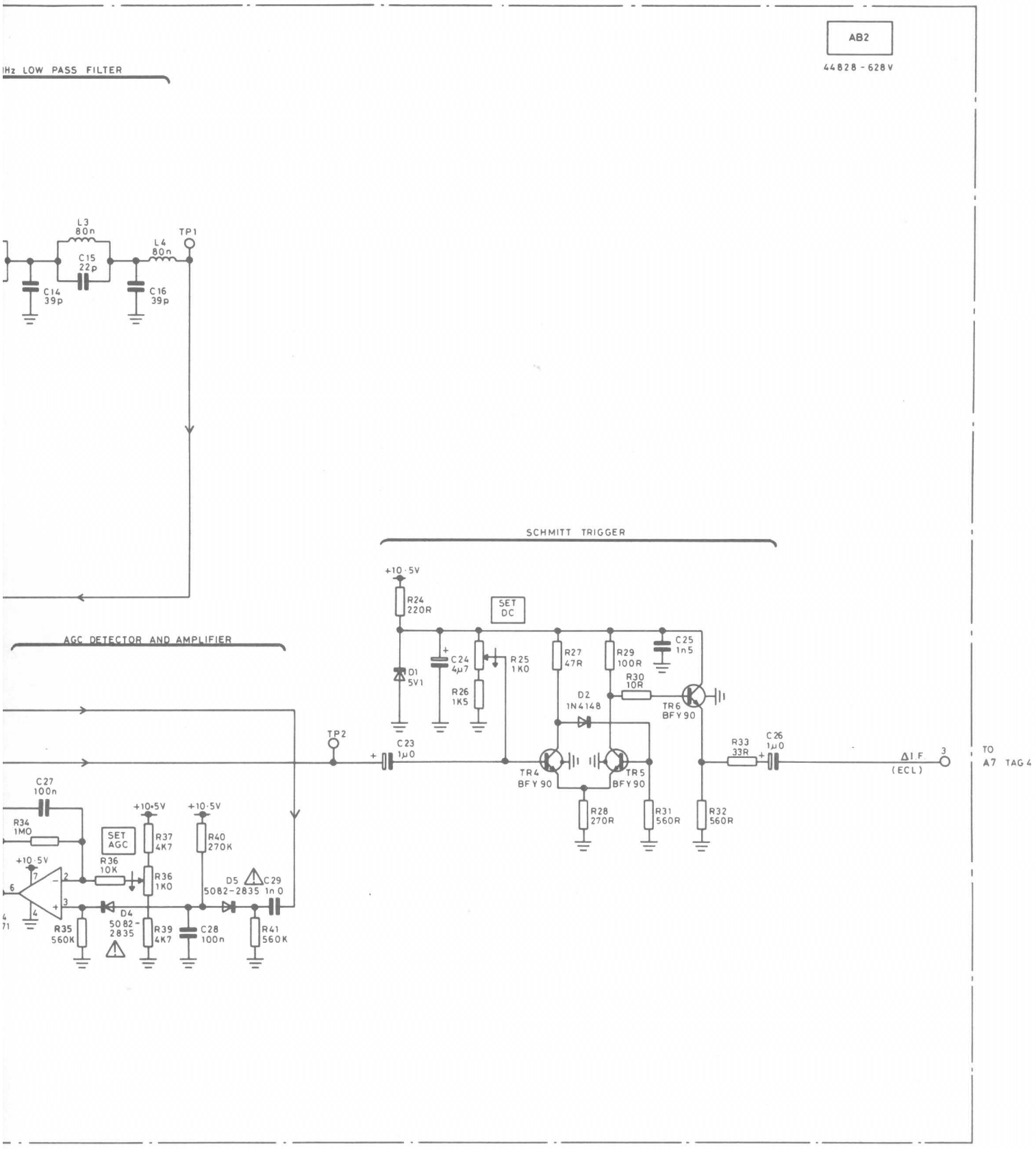


)ffset driver board, circuit diagram



Z44828-628V Iss. 5

Fig. 12 AB2 Offset i.f. boar



ffset i.f. board, circuit diagram

Chapter 5

MAINTENANCE

CONTENTS

INTRODUCTION

1. This chapter contains information for maintaining the equipment in good working order, checking its overall performance and details adjustment procedures that may be necessary after replacement of components. Before attempting any maintenance, the information given should be read with reference to the preceding Technical Description chapter.

2. Integrated circuits and semiconductor devices are used throughout this instrument, and although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reversed polarity and excessive heat or radiation. Avoid hazards such as prolonged soldering, strong r.f. fields or other forms of radiation, the use of insulation testers or accidentally applied short circuits.

3. Static sensitive components ⚠ . The c.m.o.s. integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges (see preliminary pages, Notes and Cautions).

ACCESS AND LAYOUT

Fuses

4. The counter is protected by fuses in both the live and neutral conductors of the mains supply. Access is by means of screw caps on the rear panel.

Removing external covers

5. The top and bottom covers are retained by the rear frame which is held in position by two screws through the rear feet. To remove the covers, withdraw these screws approximately 12 mm and pull the rear frame back away from the cover edges. Lift up the revealed cover edge and then lift the cover away from the chassis. Tighten the feet securing screws to maintain protection for the rear panel and frame.

6. If the rear feet and frame are removed from the chassis ensure that the feet spigots are correctly aligned when re-assembling.

Internal layout

7. Fig. 1 shows the positions of the major components of 2440. Boards A4 to A8 are conventional plug-in printed circuit boards. The following descriptions detail the procedures required to enable access to the components either by removal or part separation.

Removing the power supply unit

8. (1) Disconnect the a.c. mains supply connector at the rear panel.

(2) Unscrew and remove the four crossheaded screws which are arrowed on the top plate diagram. Unscrew and remove the two screws attaching the unit to the adjacent side frame.

(3) Lift up the front edge of the unit and pull slightly forward until the rear end of the plate has cleared the rear panel trim.

(4) Disconnect the d.c. supply cable from the motherboard and remove the unit.

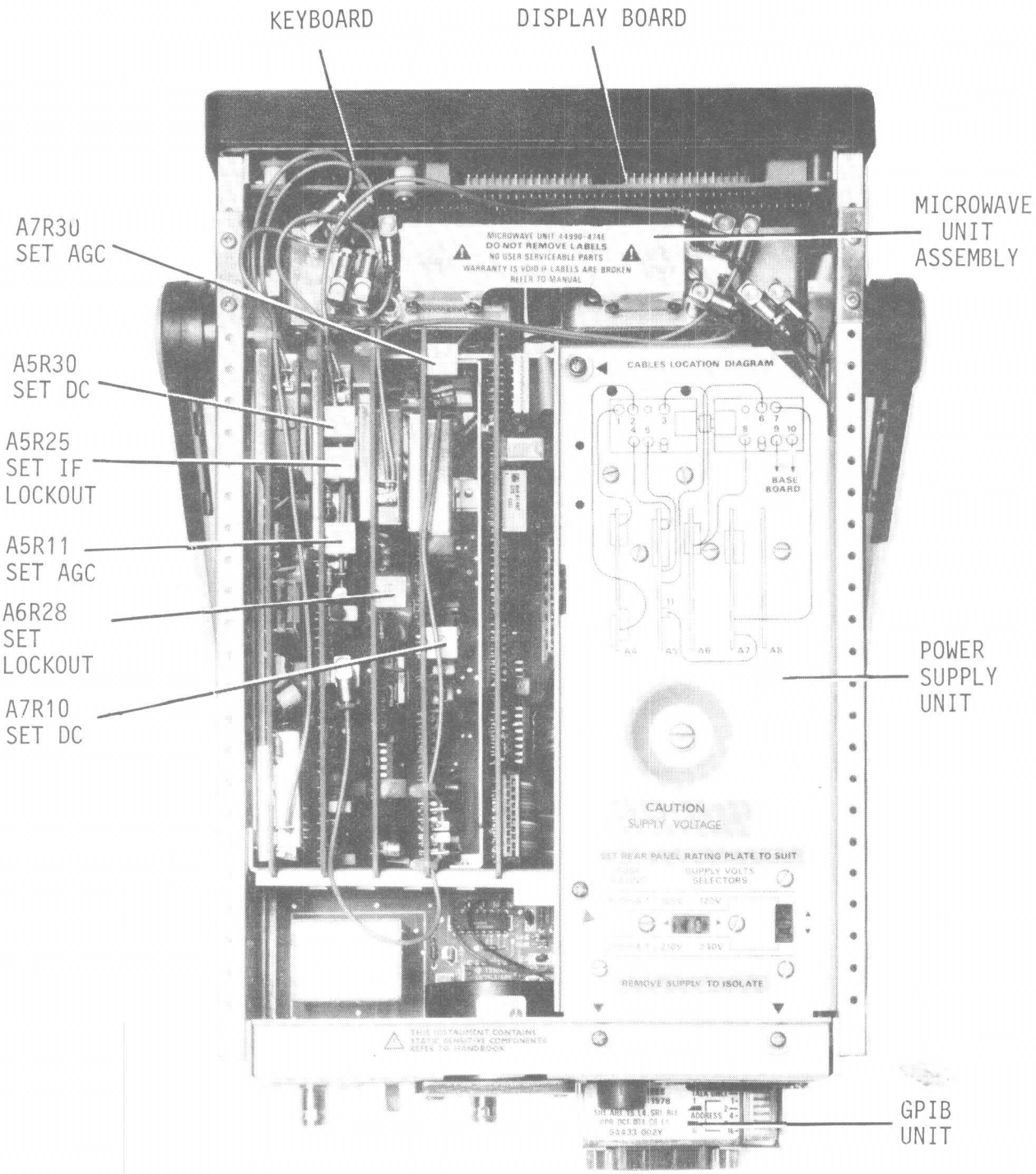


Fig. 1 2440 Internal layout

Removing the microwave unit assembly

CAUTION.

If an internal fault is diagnosed no attempt should be made to open the unit to effect repair. If the seals are broken the instrument warranty is invalid. The unit must be returned and replaced by a factory tested unit as detailed in the ordering section of Chap. 6.

9. (1) Remove the power supply unit as described in the previous para. and disconnect the cable assembly to the microwave unit from the motherboard.

(2) At the top of the unit disconnect the coaxial connectors except for positions 9 and 10 which are part of the cable assembly from the motherboard.

(3) Unscrew and remove the microwave tray steady screws which are fitted, one at each side, through the lower part of the side rails.

(4) Unscrew and remove the tray top securing screws which are fitted, two each side, into the side rails.

(5) Disconnect the channel C input connector cable (underside) from the power splitter. Use recommended tool 34901-087S which is part of optional accessory 46883-726Y. Ease the unit away to avoid undue flexing of semi-rigid cable whilst disconnecting.

(6) Lift the tray and microwave unit assembly up and out of the instrument, taking care not to foul other components and cables.

Note...

The microwave unit assembly code no. 44990-474E comprises the unit and the attached cables and connectors. When a replacement is required the whole assembly should be returned.

Access to rear panel components

10. (1) Remove the power supply unit as described in para. 8.

(2) Remove the GPIB unit or D to A converter if fitted, by unscrewing the two retaining screws at the rear panel and disconnecting the free socket from the processor board A8. Withdraw the unit through the rear panel cut-out.

(3) Unscrew and remove the two rear panel securing screws fitted at each side through the side rails. Retract the rear panel assembly.

Access to front panel components

11. (1) Unscrew and remove the microwave tray steady screws which are fitted, one at each side, through the lower part of the side rails. Also unscrew and remove the tray top securing screws which are fitted, two each side, into the side rails.

This frees the unit ready to facilitate the disconnection of channel C semi-rigid cable.

(2) Disconnect channel C input connector cable (underside) from the power splitter. Use recommended tool 34901-087S which is part of optional accessory 46883-726Y. Ease the microwave unit away to avoid undue flexing of semi-rigid cable whilst disconnecting.

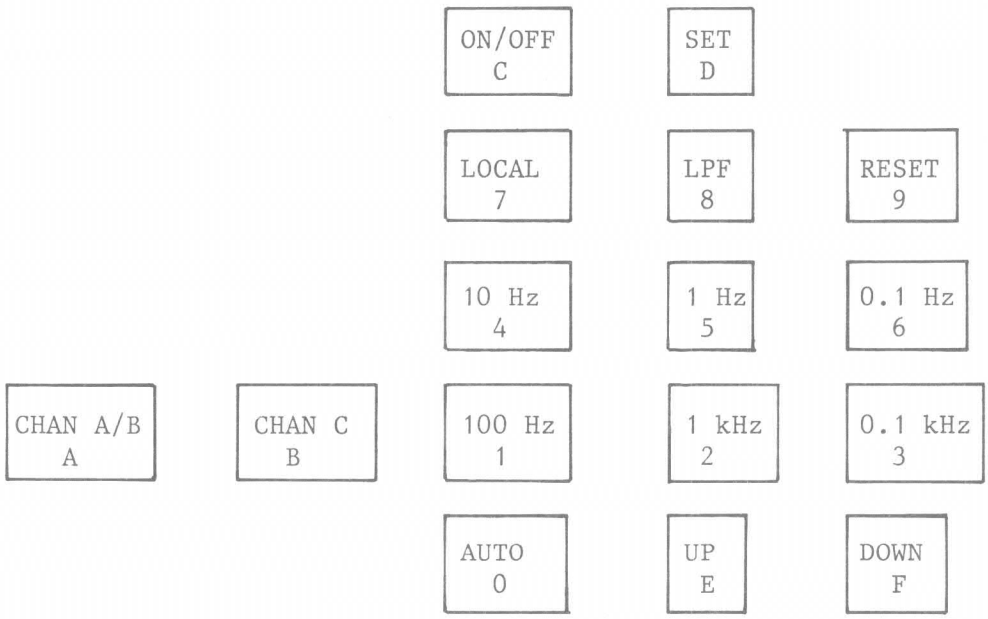
(3) Unscrew and remove the two front panel assembly screws fitted at each side through the side rails.

(4) Unclip the ribbon cable clamps mounted on the track side of the motherboard and retract the front panel assembly. Disconnect channel A and B connectors if necessary.

TEST MODES

12. Operation of [RESET] key followed by a number or function key enables the user to introduce various test and diagnostic routines to aid in fault finding.

13. The keypad layout is shown below with the associated values 0 to 9 and A to F assigned to them by the software look-up table.



14. Press [RESET] , then while "reset" is displayed select the appropriate test number or function key. This will be echoed on the display.

15. Test mode numbers and descriptions of routines are listed below.

Test mode

0 Restarts the processor from zero and is equivalent to turning the supply off and on.

1 Displays value of N during channel C operation. Must select resolution of 10 Hz. Decimal point and units have no significance.

2 Displays value of VCO during channel C operation.

Test mode

3 Displays value of i.f. during channel C operation.

4 Routes Δi.f. times 4 to l.f. counter unit and displays current value of N. If the VCO is unlocked then the counter will provide meaningless data on the real display.

5 Routes current VCO frequency to h.f. counter unit and display. The VCO frequency should end in .250 or .750 MHz. If not then the VCO is not locked correctly.

6 Routes current value of i.f. to the l.f. counter unit and display. An unstable i.f. will result in the last digits of the real display changing.

Note...

When modes 1, 2, 3 are selected the normal channel C signal and data checks are still performed.

When in modes 4, 5, 6 the relevant signals are linked directly to the two counters and NO data/signal checks are performed.

To exit modes 1 to 6 press any other key.

7 Turns on all the display l.c.d. segments (including all annunciators and decimal points) and l.e.d's. Exit by pressing either channel selector key.

8 Displays the current software issue number and date in the format xx_dd.mm.yy where xx is the issue number. Press either channel selector key to exit.

9 Resets the channel C a.g.c. system.

A (CHAN A/B) Not used.

B (CHAN C) External trigger mode toggle on and off.

C (ON/OFF) Checks the frequency of the real time clock. If faulty displays the FAIL message, if correct resumes normal operation.

D (SET) Sends mode command to loop control depending on number key pressed after prompt "h_".

0 Normal phase lock mode.

1 Locks VCO. When looking at the VCO frequency it should lock up whatever the value of the i.f. If it doesn't then the phase locking system is faulty.

2 Stops VCO with ramp at top for quiet operation.

Test mode

3 Track disabled. Ramps VCO continuously. Checks correct working of loop control and Schmitt trigger. IF 'birdies' may now be examined on an oscilloscope.

When in this mode pressing UP or DOWN will shift the VCO frequency up or down until the key is released which then locks the VCO (h1 mode).

E (UP) Enables contents of memory to be displayed. After prompt "P_" enter four digits corresponding to memory location (use 0 through to F as shown in keypad layout). Display will echo numbers and after the fourth key display the contents in hex. Pressing "UP" or "DOWN" increments or decrements the current address and displays the data contained in it.

Care should be taken when using this function as the two counter boards can be reset by reading them.

Exit by pressing any other key.

F (DOWN) Undefined.

2440 MEMORY MAP

Address decoding

The top address bus lines are decoded by a 74LS138 into 8 4k byte chunks,giving chip selects 0-7.This occupies the entire lower 32k of the 8085´s addressing space.Additionally,chip selects 0 and 1 are OR-ed together so that a 2764 8k Prom can be used.

	chip select	location	hardware
	0	0000-0FFF	2764 prom lower
	1	1000-1FFF	2764 prom upper
*	2	2000-2FFF	* not used at present *
*	3	3000-3FFF	GPIB or DAC board if fitted
*	4	4000-4FFF	keyboard and display
*	5	5000-5FFF	High Frequency Counter Unit
*	6	6000-6FFF	Low Frequency Counter Unit
	7	7000-7FFF	RAM and I/O Ports

Locations 8000-FFFF are unaddressed and available for expansion starred (*) locations are off-processor board and communicate via the 74LS245 bidirectional buffer on the processor card.

Detail decoding

```
CS 0            both
CS 1    decoded by the 2764
CS 2    * not used *
CS 3    GPIB
        3000    address switch
                (duplicated to 3007)
        3008    8291A data in/out
        3009    8291A int. status 1 /enable
        300A    8291A int. status 2 /enable
        300B    8291A serial poll status/mode
        300C    8291A address status/mode
        300D    8291A command pass/aux mode
        300E    8291A address 0
        300F    8291A address 1/EOS reg
        duplicated to 3FFF
CS4     Keyboard/Display
        4000    Key pattern wr/ key data rd
        4001    Display data latch (1 bit)
        4002    Display control latch (2 bits)
                        bit 1 = clock
                        bit 2 = load
        4003    Display leds latch (4 bits)
                note: data inverted for leds
        duplicated to 4FFF
CS5     HFCU
        5000    MA844 ls decade (ext)   4 bit BCD (top 4 bits invalid)
        5001    MA844 next decade (ext) 4 bit BCD (top 4 bits invalid)
        5002    MA844 next decade (int) 4 bit BCD (top 4 bits invalid)
        5003    MA844 next decade (int) 4 bit BCD (top 4 bits invalid)
        5004    MA844 next decade (int) 4 bit BCD (top 4 bits invalid)
```

CS5	5005	MA844 next decade (int) 4 bit BCD (top 4 bits invalid)
(contd)	5006	MA844 next decade (int) 4 bit BCD (top 4 bits invalid)
	5007	MA844 next decade (int) 4 bit BCD (top 4 bits invalid)
	5008	MA844 next decade (int) 4 bit BCD (top 4 bits invalid)
	5009	MA844 next decade (int) 4 bit BCD (top 4 bits invalid)
	500A	MA844 overflow bit (other 7 bits invalid)
	500B	MA844 test mode MEDL only
	500C	MA844 test mode MEDL only
	500D	MA844 test mode MEDL only
	500E	MA844 test mode MEDL only
	500F	MA844 Clear counters
	duplicated to 5FFF	
CS6	LFCU	
	as for HFCU	
	duplicated to 6FFF	
CS7	RAM/IO 8155	

RAM is loaded from 7000 to 70FF and duplicated to 77FF

location	name	description
7000	DSBUF	display buffer-holds 7-segment data
		lcd ANNUNCIATOR data
		bit 7 OVERFLOW
		bit 6 OFFSET
		bit 5 WIDE
		bit 4 EXT
		bit 3 REM
7001		lcd DIGIT data b1
		b2 | ‾ | b0
		b3 -
		b6 | | b4
		b5 - . b7
7009		
700A		lcd UNITS data
		bit 0 Hz
		bit 1 kHz
		bit 2 MHz
		bit 3 GHz
700B	~~~	lcd GATE
700C	ANUN	holds current LCD annunciator data
700D	UNIT	holds current LCD units data
700E	REMFLG	remote control status flag 1=remote
700F	KEYIM	holds keydata in KEYIN routine
7010	COUNT	holds current counter address
7011	~~	
7012	GATA	gate flag A-used in GATE routine
7013	STOREN	store for N,local to GATE routineand altered by it
7014	SETUP	status flag for KEYIN routine
7015	OFFLG	offset flag 1=offset function active
7016	EOSDAT	end of sequence data for GPIB =crlf
7017	N	holds current value of N in binary

location	name	description
7018	GLEN	current gate length in ms
7019	~~	
701A	DLEN	current dead time(multiples of 200ms)
701B	KEYPAT	key pattern store for use with GPIB
701C	KEVAL	key data store used in KEYIN
701D	AUTFLG	auto-resolution flag 1=active
701E	BUSUP	GPIB status byte
701F	SSHOT	single-shot mode flag for GPIB 1=active
7020	TEMP	temporary data store
7021	GSEL	current gate length selected 1-6
7022	DPADR	address offset of decimal point in data store
7023	NBCD	value of N in packed bcd
7024	NARO	narrow mode aquisition flag
7025	NVALD	N valid flag 1=valid
7026	SBMEM	sideband flag 1=lower sideband
7027	SRQINH	inhibit GPIB SRQ if 1
7028	CHANC	channel C flag 1=active
7029	TRY1	try counter 1
702A	TRY2	try counter 2
702B	TRY3	try counter 3..used as temporary store
702C	GTEM	temporary store for gate length
702D	~~	
702E	DIVID	divisor for maths routine
702F	SIGN	sign of result for maths routine 1=negative
7030	DTEM1	data store 1
~~	~~~	
7035	~~~	
7036	RESULT	result store,ie; current display
~~	~~~	
703C	~~~	
703D	TONLY	talk only flag for GPIB operation 1=active
703E	MODE	stores current mode data for loop control
703F	DATAHO	data holdoff flag for GPIB 1=active
7040	DTEM3	data store 3
~~	~~~	
7045	~~~	
7046	DTEM4	data store 4
~~	~~~	
704B	~~~	
704C	CTEM4	extra temporary store for division routine
~~	~~~	
704F	~~~	

location	name	description
7050	DTEM2	data store 3,also acts as keyboard buffer
~~	~~~	
705F	~~~	
7060	STORET	store for current gate length,altered by GATE routine
7061	~~~	
7062		
7063		
7064		
7065	DSHIFT	data shift required for change in gate
7066		
7067		
7068		
7069		
706A		
706B		
706C		
706D		
706E		
706F		
7070	OFDATA	offset data store
~~	~~~	
707C	~~~	
707D	OSE	zero store for subtraction routine
707E	OFSIGN	offset sign flag 1=add offset,0=subtract
707F	NOTEOI	flag for GPIB routine
7080	BODAT	GPIB output buffer
~~	~~~~~	
709F	~~~~~	
70A0	BIDAT	GPIB input buffer
~~	~~~~	
70BF	~~~~	
70C0	RESERVED FOR PROCESSOR STACK	
~~	~ ~	
70FF	~ ~	

Locations 7000 to 70FF duplicated to 77FF

IO ports

```
7800    8155 control/status register
7801    8155 port A - signal routeing control
        bit 0   chan B   - HFCU          ┐
        bit 1   VCO      - HFCU          │
        bit 2   if       - LFCU          │ these commands
        bit 3   delta if - LFCU          │ use inverted data
        bit 4   chan A   - LFCU          │
        bit 5   lowpass filter on/off    ┘
        bit 6   * not used *
        bit 7   * not used *
7802    8155 port B - loop control read status
        bit 0   track bit (1=valid)
        bit 1   sideband bit (1=high sideband)
        bit 2   in-band detector data
        bit 3           ~       ~
        bit 4           ~       ~
        bit 5   timebase switch (0=10 MHz)
        bit 6   timebase detector (0=external std)
        bit 7   * not available on edge connector *
7803    8155 port C - loop control write
        bit 0   ┐
        bit 1   │ loop control mode commands
        bit 2   ┘
        bit 3   loop control manual reset
        bit 4   * not available on edge connector *
        bit 5   * not available on edge connector *
7804    8155 timer counter low
7805    8155 timer counter high/control
duplicated to 7FFF
```

IO decoding

IO ports are not used,and are left undecoded and available for future expansion.

SOD line is used to signal "GATE" to the counters LFCU and HFCU.

SID is not used.

Interrupts

```
TRAP            not used
RST 7.5         real time clock (1kHz)
RST 6.5         GPIB
RST 5.5         Keyboard (will only work if key pattern includes
                          one or more zeros)
INT             not used (note INTA is not available either)

HOLD            not used (note HLDA is not available)
READY           not used or available
```

FAULT LOCATION

17. Fault finding charts, Tables 1 and 2 are provided to assist in the location of faults. It is advisable to study the descriptions of the instrument given in Chap. 4-2. A useful method of confirming if board or module is faulty, is to substitute the unit with a unit that is known to be good (e.g. from a spare working instrument).

18. Fig. 2 shows 2440 in a typical servicing position with the power unit removed but still connected and a p.c.b. fitted to an extender card.

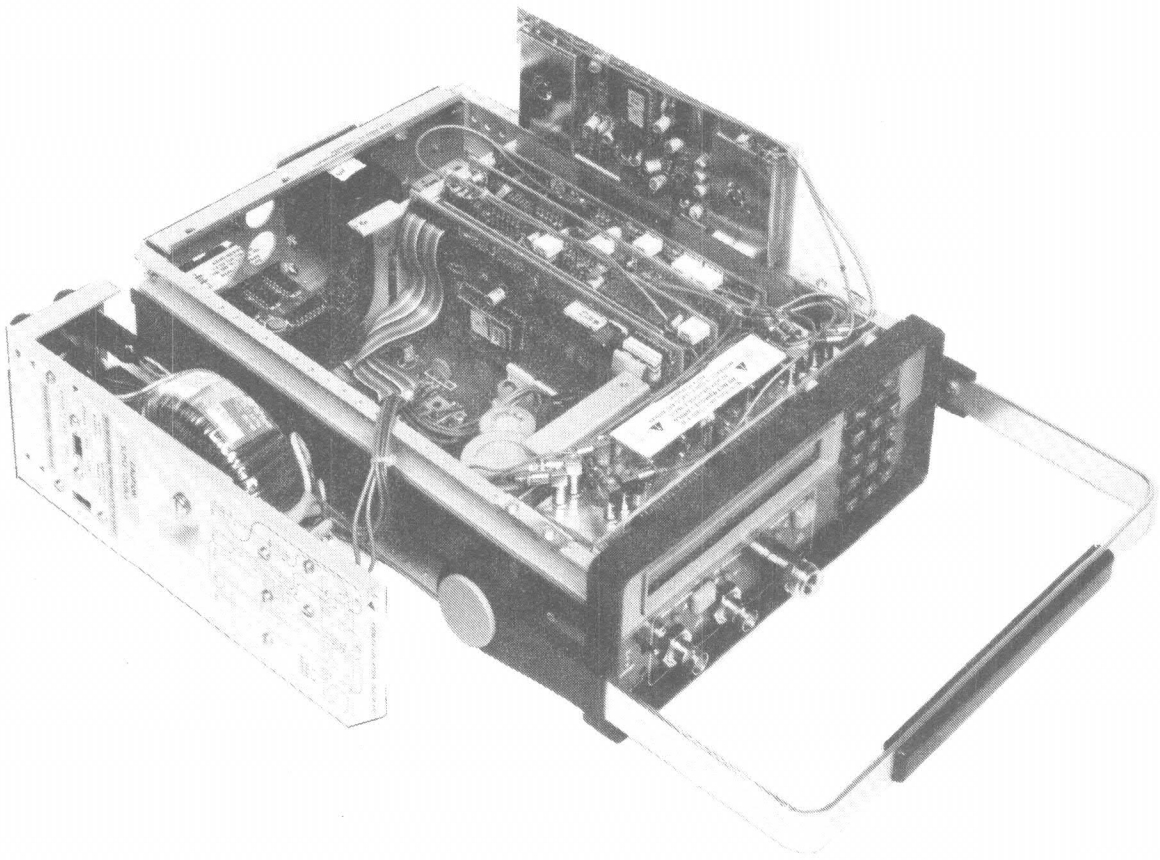


Fig. 2 2440 Internal view - servicing position

TABLE 1 2440 FAULT FINDING

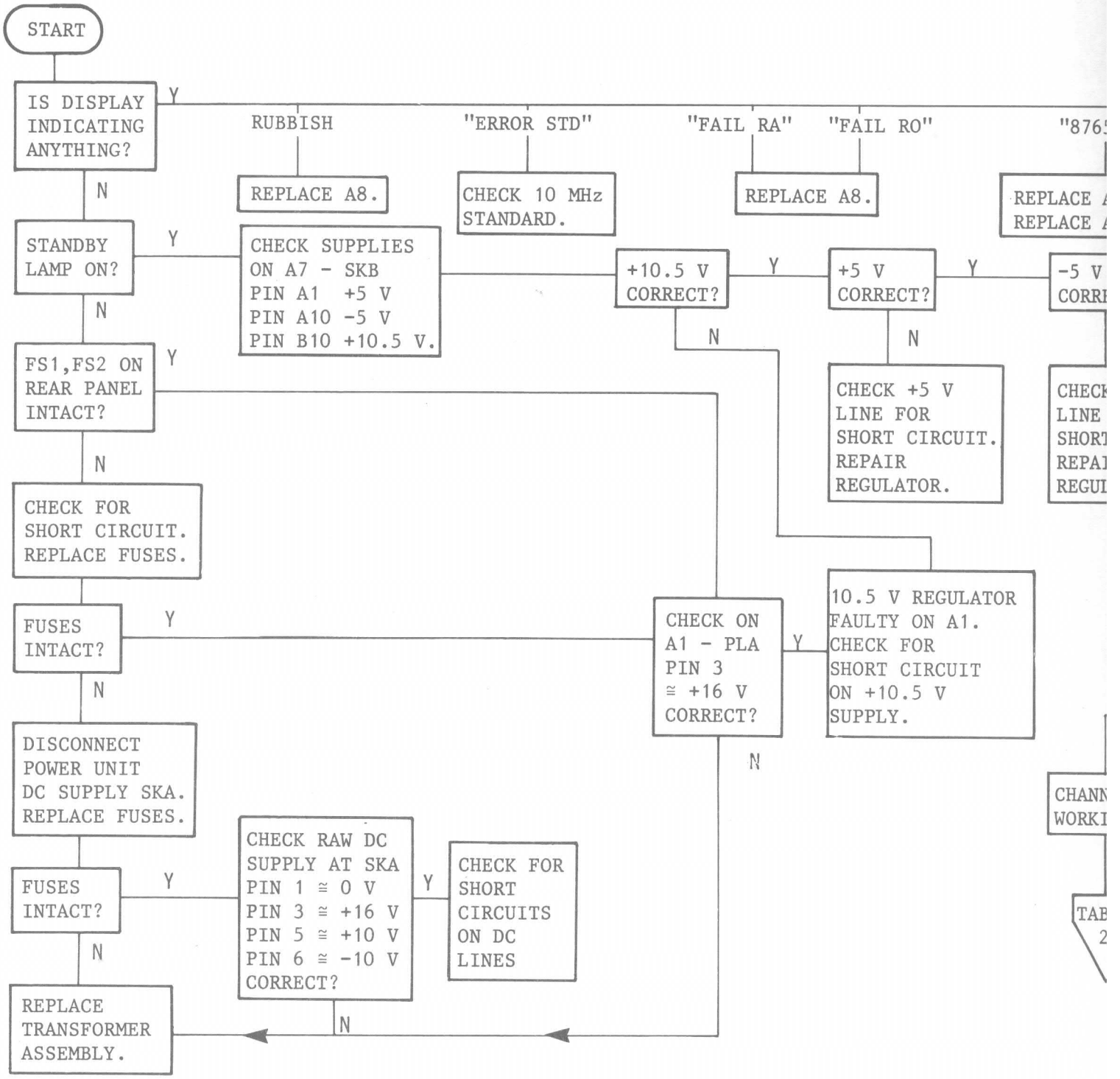


TABLE 1 2440 FAULT FINDING CHART

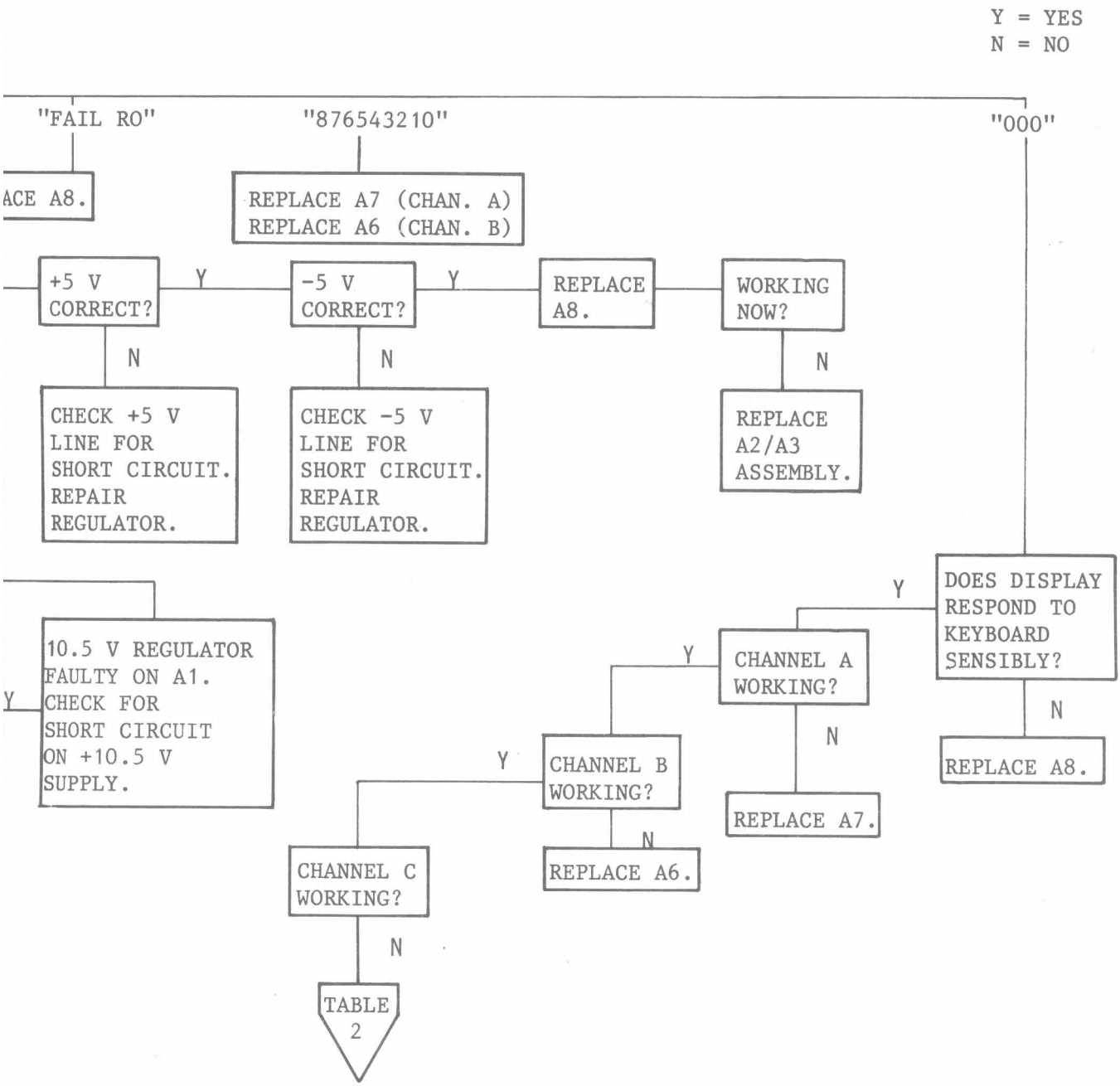


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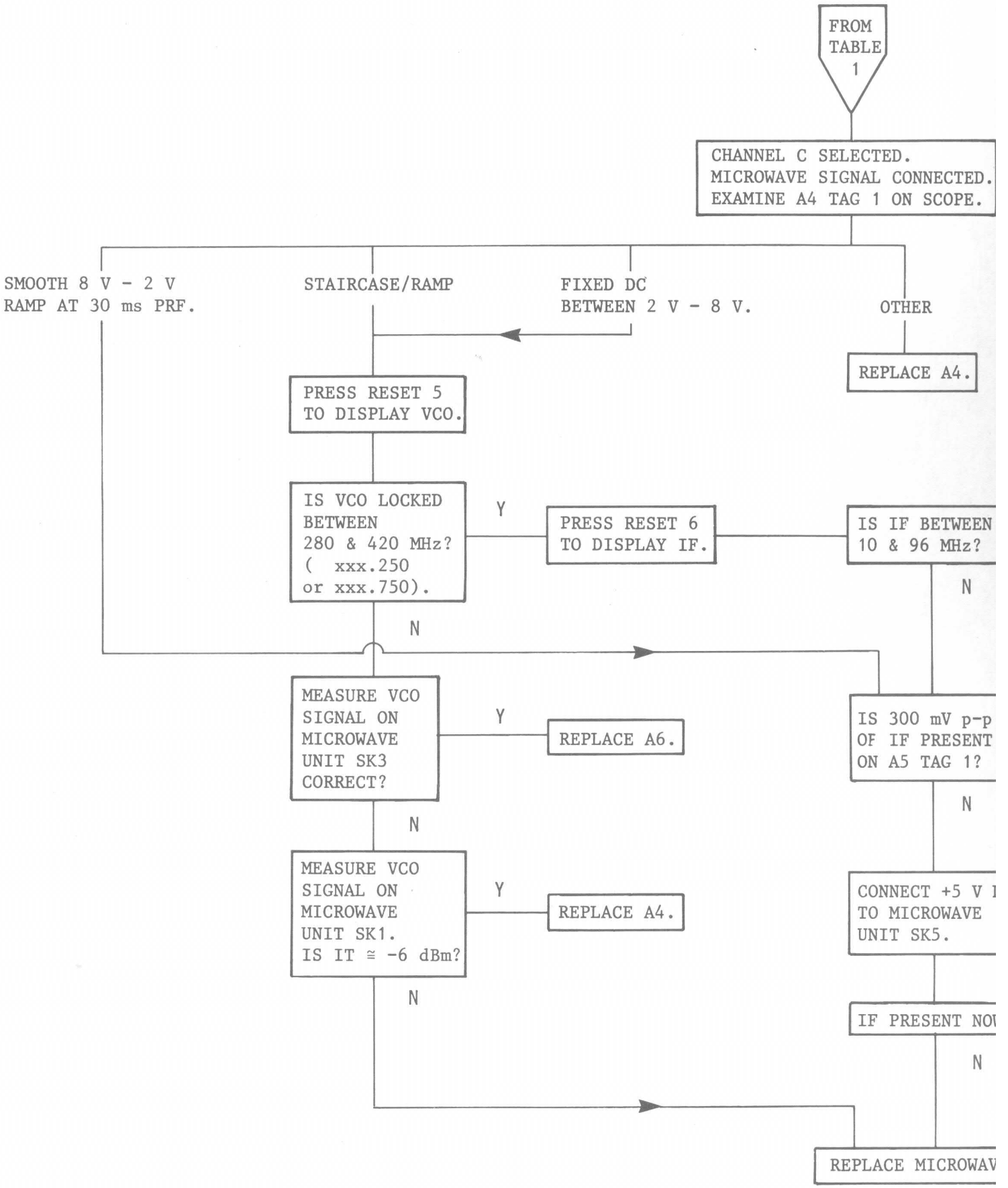
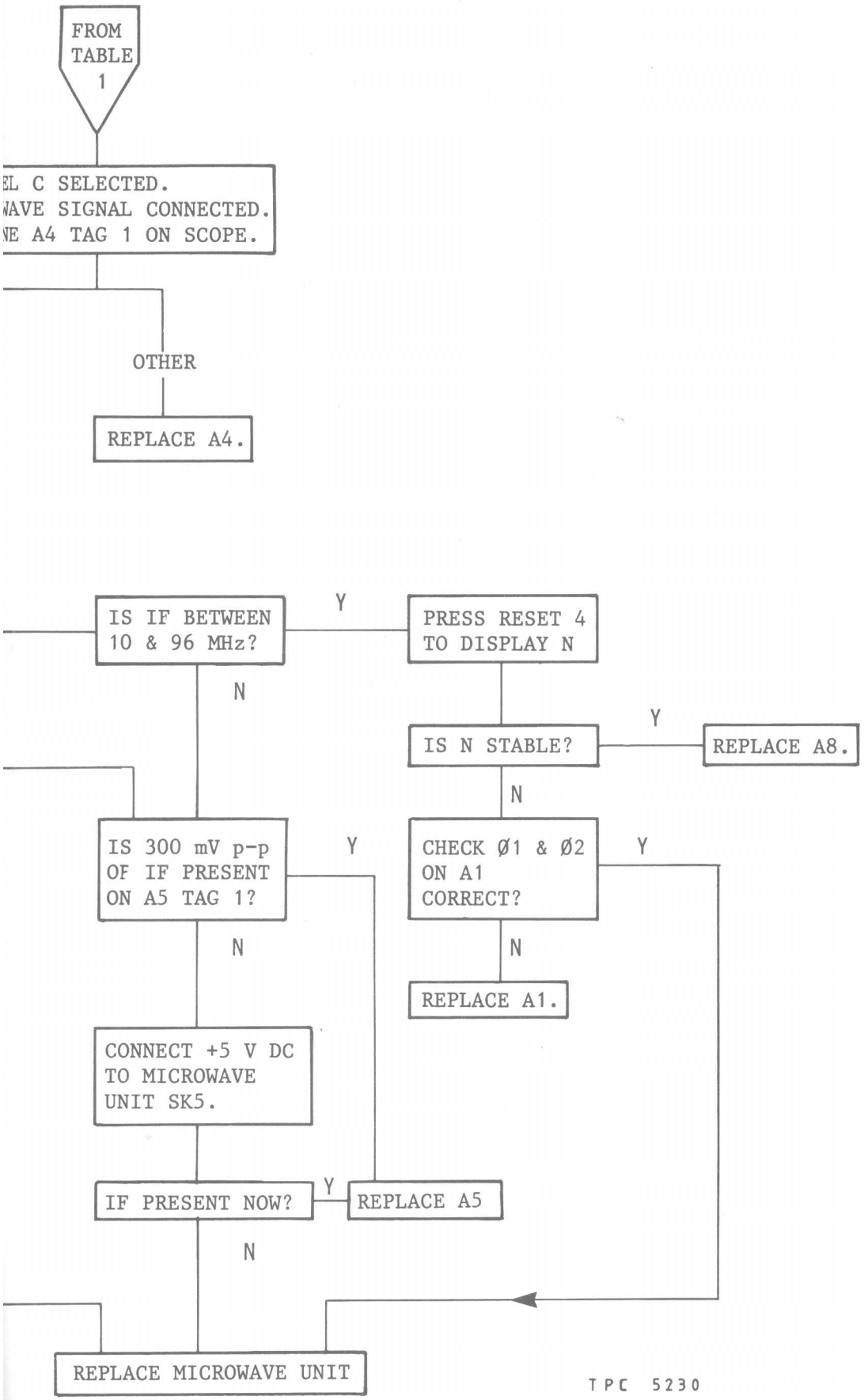
TABLE 2 FAULT FINDING CHART - CHANN



FINDING CHART - CHANNEL C



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Chapter 6

REPLACEABLE PARTS

CONTENTS

INTRODUCTION

1. Each sub-assembly or printed circuit board in this equipment has been allocated a reference designator code, e.g. A0, A1, A2 etc.

2. The complete component reference includes its reference designator as a prefix e.g. A2C1 (capacitor C1 on sub-assembly A2) but for convenience in the text and diagrams the prefix is omitted unless it is needed to avoid confusion. However when ordering replacements or in correspondence the complete component reference must be quoted.

ABBREVIATIONS

3. Electrical components are listed in alpha-numerical order of their complete circuit reference and the following standard abbreviations are used in the 'Description' column:

ADC	analogue-digital converter
ADDR	addressable
AMP	amplifier
AX	axial
BUS INRT	bus interrupt logic
CC	carbon composition
CDE CNV	code converter
CER	ceramic
CERM	cermet
CF	carbon film
CHAN	channel
CI	constant current
CIRC	circular
CKEN	clock enable
CLR	clear
COAX	coaxial
COMP	comparator/complementary
C/PIN	connector pin
CTLR	controller
CTR	counter
CUR REG	current regulator
DAC	digital-analogue converter
D/E	double-ended
DEC	decimal
DEC/DMX	decoder/demultiplexer
DEC U/D	BCD up-down counter
DECOD	decoder
DET	detector
DG	dual gate
DIF X1	differential amplifier, unity gain
DIV	divider
DRIV	driver
DUA	dual
EA	electrically alterable
ELECT/COND	electrically conductive
ENCOD	encoder
ETFE	ethylene-tetrafluoroethylene
EXPL GA	expandable gate
FF D	D type flip-flop
FF JK	JK type flip-flop
FIFO	first in, first out
F/MAG	ferro-magnetic
GPIB	general purpose interface bus
H/CARR	hot carrier
HEX RS	hex, set-reset latch

H SLW	high slew rate
HYB	hybrid
I/F	interface
INT	interrupt
INV	inverter
IR	infra-red
L BIAS	low bias current
L DFT	low drift
LN	low noise
L NSE	low noise
L/T	lead through
MBC	miniature bayonet cap
MC	metal clad
MF	metal film
MG	metal glaze
MIN	miniature
M/L	multi-layer
MN/RG/CTL	mains regulator control
MO	metal oxide
MOD	module/modular
MOD/DEMOD	modulator/demodulator
MOM	momentary
MONO	monostable
MP	microprocessor
MP SUP	microprocessor support
MULT	multiple
MUX	multiplexer
M/W	multi-way
NET	network
NGE	NPN germanium
NI	non-inductive
NJF	n-JFET
NMF	n-MOSFET
NSI	NPN silicon
OCT	octal
OCXO	oven controlled crystal oscillator
PC	polycarbonate
PE	polythene (polyethylene)
PETP	polyester (polyethylene terephthalate)
PGE	PNP germanium
PHOTO	photo-transistor
PIPO	parallel input, parallel output
PISO	parallel input, serial output
PJF	p-JFET
PLAS	plastic
PLL	phase-locked loop
PMF	p-MOSFET
PR	pair
PR/DR	processor driver
PRE	presettable
PRESC	prescaler
PROG	programmable

PROM	programmable read-only memory
PRTY TS	priority encoder, tristate
PS	polystyrene
PSI	PNP silicon
PTFE	polytetrafluoroethylene
PVC	polyvinyl chloride
PWR	power
RAD	radial
RAM	random-access memory
RECT	rectangular
ROM	read-only memory
RX	receiver
S/C ACC	semiconductor accessory
SCH	Schottky
SCHM	Schmitt
SCR	screened
S/E	single-ended
SH REG	shift register
SIPO	serial input, parallel output
SKT	socket
SOL	solenoid
SP	special
S/STATE	solid state
S/TAG	solder tag
STR	strobe
SUPP	suppressor
SW	switch
TANT	tantalum
TC	triac
TCXO	temperature compensated crystal oscillator
TEL	telephone
TP	totem pole
TR	trigger
TRIG	trigger
TX	transmitter
TXRX	transmitter-receiver
UART	universal asynchronous TXRX
UJT	unijunction transistor
UV	ultra-violet (alterable)
V/CAP	varicap (diode)
VCO	voltage controlled oscillator
V FOL	voltage follower
VREG	voltage regulator
WW	wirewound
XNOR	exclusive NOR gate
XOR	exclusive OR gate
XTAL	crystal
ZEN	Zener
!	static sensitive component

COMPONENT VALUES

4. One or more of the components fitted in the equipment may differ from those listed in this chapter for any of the following reasons:

(a) Components indicated by an asterisk (*) have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the equipment is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detailed improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the equipment.

ORDERING

6. When ordering replacements, address the order to our Service Division (address at rear of manual) or nearest agent and specify the following for each component required:-

(1) Type[#] and serial number of equipment.

(2) Complete circuit reference.

(3) Description.

(4) Part number.

[#]As given on the serial number label at the rear of the equipment; if this is superseded by a model number label, quote the model number instead of the type number.

Circuit Ref	Description	Part Number
Unit A0	- 2440 OVERALL ASSEMBLY	
7. When ordering, prefix circuit reference with A0		
	Complete unit	52440-900N
D1	DI BRIDGE BY260 200V 12A	28359-190S
D2	DI BRIDGE BY260 200V 12A	28359-190S
D3	DI BRIDGE BY260 200V 12A	28359-190S
D4	LAMP LED TIL211 4V GREEN	28624-108X
FS1	FUSE T/LAG 0.40A 20X5MM	23411-053D
	H/W FUSE HOLDER PANEL 20X5MM	23416-192R
	H/W COVER FOR FUSEHOLDER	23416-198E
FS2	FUSE T/LAG 0.40A 20X5MM	23411-053D
	H/W FUSEHOLDER PANEL 20X5MM	23416-192R
	H/W COVER FOR FUSEHOLDER	23416-198E
SA	SW SLIDE 2CO PANEL MTG	23467-157S
SB	SW TOG 1CO MIN ON-ON	23462-252Z
SC	SW SLIDE 2CO PANEL - VOLTS ADJUST	23467-170C
SD	SW SLIDE 2CO PANEL - VOLTS ADJUST	23467-170C
	COVER (VOLTS ADJUST SW)	37590-211G
SE	THERMOSTAT 10A 250VAC	23488-555D
SKC	CON RF BNC FEM 50 BKHD	23443-442B
SKD	CON RF BNC FEM 50 BKHD	23443-442B
SKE	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
SKF	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
	CABLE COAX 14CM SMB-FM/BNC-FEM	43129-986J
	CABLE COAX 14CM SMB-FM/BNC-FEM	43129-986J
	CABLE ASSY (PU)	43130-045A
	CON PWR MALE 3 FXD RF FILTER	23423-150L
	CON PART PWR COVER INS PVC BLK	23423-999Y
	CON JUMP FEM 2 1 ROW	23435-990X
	CONN N-SMA-SEMI RIGID	43129-992V
	FAN AX 5V DC 48MM	23535-127B
	TRANSFMR 2X120V/13.8/7.5/7.5V	23622-010J
	E PROM 2716 (A4)	44533-101K
	E PROM 2764 (A8)	44533-102A
	PLUG	37590-293K
	DISPLAY LCD 9-DIGIT 2440	44990-481L

Circuit Ref	Description	Part Number
Unit A01	- MICROWAVE UNIT ASSEMBLY	
8. When ordering, prefix circuit reference with A01		
	Complete unit	44990-474E
	This is a complete factory tested and set up unit, which includes cable assembly 43219-993S and is a direct replacement.	
Unit A1	- MOTHER BOARD	
9. When ordering, prefix circuit reference with A1		
	Complete unit	44828-624L
C1	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C2	CAP PS 100P 63V 2% RAD	26538-557S
C3	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C6	CAP CER 47N 25V 20% DISC	26383-017U
C7	CAP CER 10N 25V 20% DISC	26383-006C
C9	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C10	CAP CER 10N 25V 20% DISC	26383-006C
C11	CAP CER 10N 25V 20% DISC	26383-006C
C12	CAP CER 10N 25V 20% DISC	26383-006C
C13	CAP CER 1N0 63V 10% PLATE	26383-585M
C14	CAP CER 1N0 63V 10% PLATE	26383-585M
C15	CAP CER 1N0 63V 10% PLATE	26383-585M
C16	CAP CER 100N 30V 20% DISC	26383-031S
C17	CAP PS 1N00 63V 2% RAD	26538-690J
C18	CAP CER 47P 63V 5% PLATE	26343-473L
C19	CAP CER 10N 25V 20% DISC	26383-006C
C20	CAP CER 10N 25V 20% DISC	26383-006C
C21	CAP ELEC 10000U 25V 10%+ PCB	26422-330C
C22	CAP CER 10N 25V 20% DISC	26383-006C
C23	CAP CER 10N 25V 20% DISC	26383-006C
C24	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C25	CAP CER 10N 25V 20% DISC	26383-006C
C26	CAP ELEC 10000U 16V 10%+ PCB	26422-324P
C27	CAP ELEC 4700U 16V 10%+ PCB	26422-329B

Circuit Ref	Description	Part Number
Unit A1	- MOTHER BOARD (Contd.)	
C28	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C29	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C30	CAP CER 10N 25V 20% DISC	26383-006C
C31	CAP CER 47N 25V 20% DISC	26383-017U
C32	CAP CER 47N 25V 20% DISC	26383-017U
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI ZEN 1N829 6.2V 5% LOW TC *	28371-530K
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICD RX 75107A DUAL LINE TP	28469-198Y
IC2	ICA VREG+ 78L05AC 5V 0A1 TO92	28461-734Y
IC3	ICD MUX 74LS153 DUAL 4INP	28469-711K
IC4	ICD CTR 74LS390 DUAL 4BIT DEC	28464-127R
IC5	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC6	ICA AMP TL072CP DUAL FET I/P	28461-348Z
IC7	ICA VREG UA723C PROG DIL14	28461-706F
IC8	ICA AMP TL072CP DUAL FET I/P	28461-348Z
IC9	ICD FF D 74F74 DUAL +EDG TR !	28462-113S
IC10	ICD MONO 74LS123 DUAL RETR	28468-309B
IC11	ICD DRIV 74128 QUAD 2NOR 50OHM	28466-224S
IC12	ICD NAND 74LS132 QUAD 2INP SCH	28469-205N
PLA	CON PART MIN WAFER 8P 3008	23435-912F
PLB	TERM C/PIN 0.64SQX6 S/E REEL	23435-188V
PLD	TERM C/PIN 0.64SQX6 S/E REEL	23435-188V
R1	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R2	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R3	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R4	RES MF 220K 1/4W 2% 100PPM	24773-329T
R5	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R6	RES MF 82K 1/4W 2% 100PPM	24773-319J
R7	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R8	RES MF 47R 1/4W 2% 100PPM	24773-241A
R11	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R12	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R13	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R14	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R15	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R16	RES MF 6K2 1/4W 2% 100PPM	24773-292W

Circuit Ref	Description	Part Number
Unit A1	- MOTHER BOARD (Contd.)	
R17	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R18	RES MF 68R 1/4W 2% 100PPM	24773-245U
R19	RES WW 0R33 1.5W 10%	25133-033R
R20	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R21	RV CERM 2K0 LIN .5W 10% HORZ	25711-639V
R22	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R23	RES MF 560R 1/4W 2% 100PPM	24773-267R
R24	RES MF 390R 1/4W 2% 100PPM	24773-263P
R25	RV CERM 10K LIN .3W 10% FLAT	25748-507X
R26	RV CERM 2K0 LIN .5W 10% HORZ	25711-639V
R27	RES MF 56R 1/4W 2% 100PPM	24773-243H
R28	RES MF 100R 1/4W 2% 100PPM	24773-249J
R29	RES MF 24K0 1/4W 0.5% 50PPM	24753-345A
R30	RES MF 24K0 1/4W 0.5% 50PPM	24753-345A
R31	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R32	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R33	RES MF 4K7 1/4W 2% 100PPM	24773-289W
SKA	CON EDGE FEM 24 FXD .1" 2S K7	23435-813S
SKB	CON EDGE FEM 12 FXD .1" 2S K7	23435-811G
SKC	CON EDGE FEM 12 FXD .1" 2S K7	23435-811G
SKD	CON EDGE FEM 12 FXD .1" 2S K7	23435-811G
SKE	CON EDGE FEM 12 FXD .1" 2S K7	23435-811G
TR4	TR PSI BD676 45V 60K - 40W DAR	28435-239V
TR5	TR PSI 2N4918 40V 3M - 30W	28434-896Y
TR6	TR NSI BC209C 20V 150M - GEN	28452-771P
TR7	TR PSI BC308B 20V 130M - GEN	28433-455R
TR8	TR NSI BD135 45V 50M - 8W	28455-438J

Circuit Ref	Description	Part Number
Unit A2	- KEYBOARD	
10. When ordering, prefix circuit reference with A2		
	Complete unit	44828-626F
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP ELEC 22U 25V 20%+ AX	26486-583L
D1	LAMP LED OPL273 2.4V YEL	28624-121Z
D2	LAMP LED OPL273 2.4V YEL	28624-121Z
D3	LAMP LED OPL273 2.4V YEL	28624-121Z
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICD LATCH 74LS75 QUAD	28462-408U
IC2	ICD LATCH 74LS75 QUAD	28462-408U
R1	RES MF 270R 1/4W 2% 100PPM	24773-259T
R2	RES MF 270R 1/4W 2% 100PPM	24773-259T
R3	RES MF 270R 1/4W 2% 100PPM	24773-259T
SA	SW PUSH 1P1W MOM LIPA D6	23465-301P
SB	SW PUSH 1P1W MOM LIPA D6	23465-301P
SC	SW PUSH 1P1W MOM LIPA D6	23465-301P
SD	SW PUSH 1P1W MOM LIPA D6	23465-301P
SE	SW PUSH 1P1W MOM LIPA D6	23465-301P
SF	SW PUSH 1P1W MOM LIPA D6	23465-301P
SG	SW PUSH 1P1W MOM LIPA D6	23465-301P
SH	SW PUSH 1P1W MOM LIPA D6	23465-301P
SI	SW PUSH 1P1W MOM LIPA D6	23465-301P
SJ	SW PUSH 1P1W MOM LIPA D6	23465-301P
SK	SW PUSH 1P1W MOM LIPA D6	23465-301P
SL	SW PUSH 1P1W MOM LIPA D6	23465-301P
SM	SW PUSH 1P1W MOM LIPA D6	23465-301P
SN	SW PUSH 1P1W MOM LIPA D6	23465-301P
SO	SW PUSH 1P1W MOM LIPA D6	23465-301P
SP	SW PUSH 1P1W MOM LIPA D6	23465-301P

Circuit Ref	Description	Part Number
Unit A2	- KEYBOARD	(Contd.)
	SW CAP RECT BN "AUTO/0"	37590-786J
	SW CAP RECT BN "10KHz/1"	37590-787F
	SW CAP RECT BN "1KHz/2"	37590-788G
	SW CAP RECT BN "100Hz/3"	37590-789V
	SW CAP RECT BN "10Hz/4"	37590-790F
	SW CAP RECT BN "1Hz/5"	37590-791G
	SW CAP RECT BN "0.1Hz/6"	37590-792V
	SW CAP RECT BN "LOCAL/7"	37590-793S
	SW CAP RECT BN "LPF/8"	37590-794W
	SW CAP RECT BN "RESET /9"	37590-795D
	SW CAP RECT BN "^/."	37590-796T
	SW CAP RECT BN "v/+-"	37590-797P
	SW CAP RECT BN "ON/OFF"	37590-798X
	SW CAP RECT BN "SET"	37590-799M
	SW CAP RECT GY BLANK	37590-691S
	SW CAP RECT GY BLANK	37590-691S
Unit A3	- DISPLAY BOARD	
11. When ordering, prefix circuit reference with A3		
	Complete unit	44828-625J
C1	CAP CER 2N2 63V 10% PLATE	26383-587R
C2	CAP CER 2N2 63V 10% PLATE	26383-587R
C3	CAP CER 2N2 63V 10% PLATE	26383-587R
C4	CAP CER 2N2 63V 10% PLATE	26383-587R
C5	CAP CER 2N2 63V 10% PLATE	26383-587R
C6	CAP CER 2N2 63V 10% PLATE	26383-587R
C7	CAP CER 47P 63V 5% PLATE	26343-473L
C8	CAP ELEC 2U2 50V 20% L/LEAK	26421-009E
C9	CAP ELEC 2U2 50V 20% L/LEAK	26421-009E
IC1	ICD BUFF 74LS125A QUAD 3ST	28469-184X
IC2	ICD NAND 74LS20 DUAL 4INP	28466-347U
IC3	ICD INV 74LS04 HEX	28469-171L
IC4	ICD LATCH 74LS75 QUAD	28462-408U
IC5	ICD DEC/DMX 74LS155 DUAL 2-4	28465-026J

Circuit Ref	Description		Part Number
Unit A3	- DISPLAY BOARD (Contd.)		
IC6	ICD DRIV HLCD-0438 LCD SER IN	!	28467-016B
IC7	ICD DRIV HLCD-0438 LCD SER IN	!	28467-016B
IC8	ICD DRIV HLCD-0438 LCD SER IN	!	28467-016B
R1	RES MF 10K 1/4W 2% 100PPM		24773-297M
R2	RES MF 10K 1/4W 2% 100PPM		24773-297M
R3	RES MF 10K 1/4W 2% 100PPM		24773-297M
R4	RES MF 10K 1/4W 2% 100PPM		24773-297M
SKB	S/C ACC SKT SIL20 W/WRAP SNAP		28488-171K
SKC	S/C ACC SKT SIL20 W/WRAP SNAP		28488-171K
	CABLE ASSY 14 RIB		43130-002T
	CON JUMP MALE 12 FREE 1"LG		23436-106F
Unit A4	- LOOP CONTROL		
12. When ordering, prefix circuit reference with A4			
	Complete unit		44828-630G
C1	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C2	CAP CER 4N7 63V 10% PLATE		26383-591B
C3	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C4	CAP CER 4N7 63V 10% PLATE		26383-591B
C5	CAP CER 4N7 63V 10% PLATE		26383-591B
C6	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C7	CAP CER 4N7 63V 10% PLATE		26383-591B
C8	CAP CER 4N7 63V 10% PLATE		26383-591B
C9	CAP CER 4N7 63V 10% PLATE		26383-591B
C10	CAP CER 1N5 63V 10% PLATE		26383-593A
C12	CAP CER 1N5 63V 10% PLATE		26383-593A
C13	CAP CER 4N7 63V 10% PLATE		26383-591B
C14	CAP PETP 47N 63V 10% RAD MIN		26582-428J
C15	CAP PETP 470N 63V 10% RAD		26582-410P
C16	CAP TANT 4U7 10V 20% AX		26486-554G
C17	CAP TANT 4U7 10V 20% AX		26486-554G
C18	CAP TANT 1U0 35V 20% AX		26486-513U
C19	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C20	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C21	CAP CER 4N7 63V 10% PLATE		26383-591B
C22	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L

Circuit Ref	Description		Part Number
Unit A4	- LOOP CONTROL (Contd.)		
C23	CAP CER 22N 18V 20% DISC		26383-007R
C24	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C25	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C26	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
C27	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C28	CAP CER 22P 63V 5% PLATE		26343-469N
C29	CAP CER 3P3 63V .5PF PLATE		26343-459K
C30	CAP CER 3P3 63V .5PF PLATE		26343-459K
C31	CAP CER 1N0 63V 10% PLATE		26383-585M
C32	CAP CER 100P 63V 2% PLATE		26343-477V
C34	CAP CER 820P 63V 10% PLATE		26383-584X
C35	CAP CER 390P 63V 10% PLATE		26383-598Y
C36	CAP CER 10P 63V .5PF PLATE		26343-465H
C37	CAP CER 3N3 63V 10% PLATE		26383-589K
C38	CAP CER 3N3 63V 10% PLATE		26383-589K
C39	CAP CER 10P 63V .5PF PLATE		26343-465H
C40	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C41	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C42	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C43	CAP CER 3N3 63V 10% PLATE		26383-589K
C44	CAP CER 3N3 63V 10% PLATE		26383-589K
D2	DI ZEN BZX79C5V1 5.1V 5%		28371-401U
D3	DI H/CARR BAT29 5V		28349-014L
D4	DI H/CARR BAT29 5V		28349-014L
D5	DI ZEN BZX79C3V0 3.0V 5%		28371-209P
IC1	ICD FF D 74LS374 OCT +E TR 3ST		28462-618L
IC3	ICA MUX 4053 TRIP 2INP	!	28469-714H
IC4	ICA MUX 4053 TRIP 2INP	!	28469-714H
IC5	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC6	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC7	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC8	ICA AMP NE531N H SLW DIL8		28461-317H
IC9	ICA AMP NE531N H SLW DIL8		28461-317H
IC10	ICA COMP LM339N QUAD		28461-693H
L1	IND CHOKE 470UH 10% LAQ		23642-565X
L2	IND CHOKE 330UH 10% LAQ		23642-564P
L3	IND CHOKE 108uH ASSY		44290-876X
L4	IND CHOKE 108uH ASSY		44290-876X
L5	IND CHOKE 108uH ASSY		44290-876X

Circuit Ref	Description	Part Number
Unit A4	- LOOP CONTROL (Contd.)	
R1	RES MF 47K 1/4W 2% 100PPM	24773-313H
R2	RES MF 100K 1/4W 2% 100PPM	24773-321L
R3	RES MG 3M3 1/4W 5%	24321-879G
R4	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R5	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R6	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R7	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R8	RES MF 56K 1/4W 2% 100PPM	24773-315U
R9	RES MF 220R 1/4W 2% 100PPM	24773-257W
R10	RES MF 7K5 1/4W 2% 100PPM	24773-294T
R11	RES MF 680R 1/4W 2% 100PPM	24773-269K
R12	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R13	RES MF 22R 1/4W 2% 100PPM	24773-233M
R14	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R15	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R16	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R17	RES MF 68K 1/4W 2% 100PPM	24773-317N
R18	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R19	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R20	RES MF 10K 1/4W 2% 100PPM	24773-297M
R21	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R22	RES MF 180R 1/4W 2% 100PPM	24773-255V
R23	RES CC 820R 1/8W 5%	24331-993X
R24	RES CC 680R 1/8W 5%	24331-984V
R25	RES CC 22R 1/8W 5%	24331-988T
R26	RES CC 150R 1/8W 5%	24331-990D
R27	RES CC 680R 1/8W 5%	24331-984V
R28	RES CC 47R 1/8W 5%	24331-975Y
R29	RES CC 33R 1/8W 5%	24331-978J
R30	RES CC 33R 1/8W 5%	24331-978J
R31	RES CC 22K0 1/8W 5%	24331-960P
R32	RES CC 22K0 1/8W 5%	24331-960P
R33	RES CC 1K5 1/8W 5%	24331-959M
R34	RES CC 22K0 1/8W 5%	24331-960P
R35	RES CC 1K0 1/8W 5%	24331-967A
R36	RES CC 10K 1/8W 5%	24331-972H
R37	RES CC 10K 1/8W 5%	24331-972H
R38	RES CC 10K 1/8W 5%	24331-972H
R39	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R40	RES MF 1K0 1/4W 2% 100PPM	24773-273A
SKA	S/C ACC SKT DIL24 LOW PROFILE	28488-044N

Circuit Ref	Description	Part Number
Unit A4	- LOOP CONTROL (Contd.)	
TR1	TR PSI BC307A 45V 130M - GEN	28435-227H
TR4	TR NSI BFY90 15V 1G - AMP	28452-157R
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
TR6	TR NJF BF245B 30V 6MA	28459-048X
TR7	TR NSI BC208B 20V 150M - GEN	28452-781A
TR8	TR PSI BC307A 45V 130M - GEN	28435-227H
TR9	TR NSI BC208B 20V 150M - GEN	28452-781A
T1	MIN BALUN	43590-141Y
	BOARD SCREEN TOP	35904-207E
	BOARD SCREEN BASE	35904-208U
	CABLE ASSY RF SMB	43130-036X
	CABLE ASSY RF SMB	43130-037M
Unit A5	- I.F. BUFFER	
13. When ordering, prefix circuit reference with A5		
	Complete unit	44828-632S
C1	CAP CER 1N5 63V 10% PLATE	26383-593A
C2	CAP CER 1N5 63V 10% PLATE	26383-593A
C3	CAP CER 39P 63V 5% PLATE	26343-472N
C4	CAP CER 1N5 63V 10% PLATE	26383-593A
C5	CAP CER 10N 25V 20% DISC	26383-006C
C6	CAP CER 1N0 63V 10% PLATE	26383-585M
C7	CAP CER 100P 63V 2% PLATE	26343-477V
C8	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C9	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C10	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C11	CAP CER 10N 25V 20% DISC	26383-006C
C12	CAP CER 1N5 63V 10% PLATE	26383-593A
C13	CAP CER 10N 25V 20% DISC	26383-006C
C14	CAP CER 10N 25V 20% DISC	26383-006C
C15	CAP CER 220P 63V 2% PLATE	26343-481S
C16	CAP CER 220P 63V 2% PLATE	26343-481S
C17	CAP CER 220P 63V 2% PLATE	26343-481S
C18	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C19	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C20	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C21	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C22	CAP ELEC 33U 25V 20% SUBMIN	26421-115U

Circuit Ref	Description	Part Number
Unit A5	- I.F. BUFFER (Contd.)	
C23	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C24	CAP CER 10N 25V 20% DISC	26383-006C
C25	CAP CER 10N 25V 20% DISC	26383-006C
C26	CAP CER 10N 25V 20% DISC	26383-006C
C27	CAP CER 10N 25V 20% DISC	26383-006C
C28	CAP CER 10N 25V 20% DISC	26383-006C
C29	CAP CER 10N 25V 20% DISC	26383-006C
C30	CAP CER 10N 25V 20% DISC	26383-006C
C31	CAP CER 10N 25V 20% DISC	26383-006C
C32	CAP CER 10N 25V 20% DISC	26383-006C
C33	CAP PS 47P 63V 1PF RAD	26538-529P
C34	CAP PS 330P 63V 2% RAD	26538-603X
C35	CAP CER 1N0 63V 10% PLATE	26383-585M
C36	CAP CER 100P 63V 2% PLATE	26343-477V
C37	CAP CER 1N0 63V 10% PLATE	26383-585M
C38	CAP CER 100P 63V 2% PLATE	26343-477V
D1	DI H/CARR BAT29 5V	28349-014L
D2	DI H/CARR BAT29 5V	28349-014L
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL BA482 35V JUNC	28335-675R
D5	DI SIL BA482 35V JUNC	28335-675R
D6	DI SIL BAY72 100V JUNC	28337-126P
D7	DI H/CARR BAT29 5V	28349-014L
D8	DI H/CARR BAT29 5V	28349-014L
D9	DI H/CARR BAT29 5V	28349-014L
D10	DI ZEN BZX79C5V6 5.6V 5%	28371-417X
D11	DI ZEN BZX79C6V8 6.8V 5%	28371-550W
IC1	ICA AMP SL560CDP RF W/BND DIL8	28461-365S
IC2	ICA AMP TL074CN QUAD FET I/P	28461-349H
IC3	ICD NOR 10102 QUAD 2INP	28466-219G
IC4	ICD FF D 10231 M/SLAVE	28462-610K
IC5	ICD FF D 74F74 DUAL +EDG TR	28462-113S
IC6	ICD CTR 74LS93 4BIT BIN 2,8,16	28464-117W
IC7	ICD XOR 74LS86 QUAD 2INP	28466-406C
IC8	ICD SH REG 74LS164 8BIT SIPO	28467-515G
IC9	ICD MONO 74LS221 DUAL	28468-404D
IC10	ICD NOR 74LS02 QUAD 2INP	28466-214Y
IC11	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
L1	IND CHOKE 108uH ASSY	44290-876X
L2	IND CHOKE 108uH ASSY	44290-876X
L3	IND CHOKE 108uH ASSY	44290-876X
L4	COIL R.F. 0.08uH	34901-046N

Circuit Ref	Description	Part Number
Unit A5	- I.F. BUFFER (Contd.)	
	BOARD SCREEN TOP	35904-207E
	BOARD SCREEN BASE	35904-208U
PLA	CON RF SMB MALE 50 PCB ELBOW	23444-359Z
R1	RES CC 68R 1/8W 5%	24331-979F
R2	RES CC 6K8 1/8W 5%	24331-951G
R3	RES CC 33R 1/8W 5%	24331-978J
R4	RES CC 10R 1/8W 5%	24331-974U
R5	RES CC 150R 1/8W 5%	24331-990D
R6	RES CC 220R 1/8W 5%	24331-976N
R7	RES CC 33R 1/8W 5%	24331-978J
R8	RES MF 10K 1/4W 2% 100PPM	24773-297M
R9	RES MF 560K 1/4W 2% 100PPM	24773-340R
R10	RES MF 270K 1/4W 2% 100PPM	24773-331D
R11	RV CERM 1K0 LIN .5W 10% VERT	25711-602N
R12	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R13	RES MF 10K 1/4W 2% 100PPM	24773-297M
R14	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R15	RES MF 10K 1/4W 2% 100PPM	24773-297M
R16	RES MF 10K 1/4W 2% 100PPM	24773-297M
R17	RES MF 10K 1/4W 2% 100PPM	24773-297M
R18	RES MF 10K 1/4W 2% 100PPM	24773-297M
R19	RES MF 100K 1/4W 2% 100PPM	24773-321L
R20	RES MF 10K 1/4W 2% 100PPM	24773-297M
R21	RES MF 10K 1/4W 2% 100PPM	24773-297M
R22	RES MF 10K 1/4W 2% 100PPM	24773-297M
R23	RES MF 10K 1/4W 2% 100PPM	24773-297M
R24	RES MF 10K 1/4W 2% 100PPM	24773-297M
R25	RV CERM 1K0 LIN .5W 10% VERT	25711-602N
R26	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R27	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R28	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R29	RES MF 15K 1/4W 2% 100PPM	24773-301P
R30	RV CERM 1K0 LIN .5W 10% VERT	25711-602N
R31	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R32	RES CC 1K0 1/8W 5%	24331-967A
R33	RES CC 47R 1/8W 5%	24331-975Y
R34	RES CC 270R 1/8W 5%	24331-992P
R35	RES CC 100R 1/8W 5%	24331-997B
R36	RES CC 560R 1/8W 5%	24331-965B
R37	RES CC 560R 1/8W 5%	24331-965B

Circuit Ref	Description	Part Number
Unit A5	- I.F. BUFFER (Contd.)	
R38	RES NET 680R 5% SIP	24681-624Z
R39	RES MF 10K 1/4W 2% 100PPM	24773-297M
R40	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R41	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R42	RES MF 150R 1/4W 2% 100PPM	24773-253F
R43	RES MF 330R 1/4W 2% 100PPM	24773-261D
R44	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R45	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R46	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R47	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R48	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R49	RES MF 30K 1/4W 2% 100PPM	24773-308A
R50	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R51	RES CC 100R 1/8W 5%	24331-997B
R52	RES MF 10K 1/4W 2% 100PPM	24773-297M
R53	RES MF 560K 1/4W 2% 100PPM	24773-340R
R54	RES MF 270K 1/4W 2% 100PPM	24773-331D
R55	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R56	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R57	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R58	RES MF 150K 1/4W 2% 100PPM	24773-325V
TR1	TR PSI BC308B 20V 130M - GEN	28433-455R
TR2	TR NSI BC209C 20V 150M - GEN	28452-771P
TR3	TR NSI BC209C 20V 150M - GEN	28452-771P
TR4	TR PSI BC308B 20V 130M - GEN	28433-455R
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
TR6	TR NSI BFY90 15V 1G - AMP	28452-157R
TR7	TR NSI BFY90 15V 1G - AMP	28452-157R
TR8	TR NSI BFY90 15V 1G - AMP	28452-157R
TR9	TR NSI BFY90 15V 1G - AMP	28452-157R
	CABLE COAX 12CM SMB-FEM/-	43130-039R
	CABLE COAX 16CM SMB-FEM/-	43130-040M
	CABLE COAX 25CM SMB-FEM/-	43130-041C

Circuit Ref	Description	Part Number
Unit A6	- HIGH FREQUENCY COUNTER UNIT	
14. When ordering, prefix circuit reference with A6		
	Complete unit	44828-634D
C1	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C2	CAP CER 1N0 63V 10% PLATE	26383-585M
C3	CAP CER 1N0 63V 10% PLATE	26383-585M
C4	CAP CER 1N0 63V 10% PLATE	26383-585M
C5	CAP CER 1N0 63V 10% PLATE	26383-585M
C6	CAP CER 1N0 63V 10% PLATE	26383-585M
C7	CAP CER 1N0 63V 10% PLATE	26383-585M
C8	CAP CER 1N0 63V 10% PLATE	26383-585M
C9	CAP CER 1N0 63V 10% PLATE	26383-585M
C10	CAP CER 22N 18V 20% DISC	26383-007R
C11	CAP CER 1N0 63V 10% PLATE	26383-585M
C12	CAP CER 1N0 63V 10% PLATE	26383-585M
C13	CAP CER 100P 63V 2% PLATE	26343-477V
C14	CAP CER 150P 63V 2% PLATE	26343-479W
C15	CAP CER 1N0 63V 10% PLATE	26383-585M
C16	CAP CER 22N 18V 20% DISC	26383-007R
C17	CAP CER 1N0 63V 10% PLATE	26383-585M
C18	CAP CER 1N0 63V 10% PLATE	26383-585M
C19	CAP CER 1N0 63V 10% PLATE	26383-585M
C20	CAP CER 1N0 63V 10% PLATE	26383-585M
C21	CAP CER 22N 18V 20% DISC	26383-007R
C22	CAP CER 10P 63V .5PF PLATE	26343-465H
C23	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C24	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C25	CAP CER 22N 18V 20% DISC	26383-007R
C26	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C27	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C28	CAP CER 22N 18V 20% DISC	26383-007R
C29	CAP CER 22N 18V 20% DISC	26383-007R
C30	CAP CER 22N 18V 20% DISC	26383-007R
C31	CAP CER 3P3 63V .5PF PLATE	26343-459K
C32	CAP CER 1N0 63V 10% PLATE	26383-585M
D1	DI ZEN BZX79C3V3 3.3V 5%	28371-210D
D2	DI H/CARR BAT29 5V	28349-014L
D3	DI PIN 5082-3379 50V	28383-997T
D4	DI PIN 5082-3379 50V	28383-997T
D5	DI ZEN BZX79C3V3 3.3V 5%	28371-210D

Circuit Ref	Description	Part Number
Unit A6	- HIGH FREQUENCY COUNTER UNIT (Contd.)	
D6	DI PIN 5082-3379 50V	28383-997T
D7	DI H/CARR BAT29 5V	28349-014L
D8	DI H/CARR BAT29 5V	28349-014L
D9	DI H/CARR BAT29 5V	28349-014L
D10	DI H/CARR BAT29 5V	28349-014L
D11	DI ZEN BZX79C5V6 5.6V 5%	28371-417X
IC1	ICA AMP SL952 1GHZ LIMITING	28461-364V
IC2	ICD DIV SP8635B 4BIT DEC ECL	28464-012G
IC3	ICD RX 10116 TRIP LINE	28469-183P
IC4	ICD CTR 10138 4BIT DEC	28464-019X
IC5	ICA COMP LM339N QUAD	28461-693H
IC6	ICD CTR 844 10 DECADE CUSTOM !	28464-021P
IC7	ICA AMP TL072CP DUAL FET I/P	28461-348Z
IC8	ICD FF D MC10131L	28462-605R
L1	IND CHOKE .47UH 10% LAQ	23642-547Y
L2	IND CHOKE .47UH 10% LAQ	23642-547Y
L3	IND CHOKE .47UH 10% LAQ	23642-547Y
L4	R.F.COIL	34901-009U
L5	IND CHOKE 108uH ASSY	44290-876X
L6	IND CHOKE 108uH ASSY	44290-876X
	BOARD SCREEN TOP	35904-207E
	BOARD SCREEN BASE	35904-208U
PLA	CON RF SMB MALE 50 PCB ELBOW	23444-359Z
R1	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R2	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R3	RES CC 56R 1/8W 5%	24331-944N
R4	RES CC 47R 1/8W 5%	24331-975Y
R5	RES CC 220R 1/8W 5%	24331-976N
R6	RES CC 220R 1/8W 5%	24331-976N
R7	RES CC 47R 1/8W 5%	24331-975Y
R8	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R9	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R10	RES CC 47R 1/8W 5%	24331-975Y
R11	RES CC 47R 1/8W 5%	24331-975Y
R12	RES CC 220R 1/8W 5%	24331-976N
R13	RES MF 10K 1/4W 2% 100PPM	24773-297M
R14	RES MF 270K 1/4W 2% 100PPM	24773-331D
R15	RES MF 560K 1/4W 2% 100PPM	24773-340R

Circuit Ref	Description	Part Number
Unit A6	- HIGH FREQUENCY COUNTER UNIT (Contd.)	
R16	RES CC 150R 1/8W 5%	24331-990D
R17	RES CC 150R 1/8W 5%	24331-990D
R18	RES CC 68K 1/8W 5%	24331-981J
R19	RES MF 10K 1/4W 2% 100PPM	24773-297M
R20	RES MF 10K 1/4W 2% 100PPM	24773-297M
R21	RES MF 10K 1/4W 2% 100PPM	24773-297M
R22	RES MF 10K 1/4W 2% 100PPM	24773-297M
R23	RES MF 47R 1/4W 2% 100PPM	24773-241A
R24	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R25	RES NET 680R 5% SIP	24681-624Z
R26	RES NET 10K 5% 8DIL	24681-511P
R27	RES MF 11K 1/4W 2% 100PPM	24773-298C
R28	RV CERM 2K0R LIN .5W 10% VERT	25711-609W
R29	RES MF 10K 1/4W 2% 100PPM	24773-297M
R30	RES MF 10K 1/4W 2% 100PPM	24773-297M
R31	RES MG 10M 1/4W 5%	24321-885W
R32	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R33	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R34	RES MF 22K 1/4W 2% 100PPM	24773-305R
R35	RES MF 560R 1/4W 2% 100PPM	24773-267R
R36	RES MF 560R 1/4W 2% 100PPM	24773-267R
R37	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R38	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R39	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R40	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R41	RES MF 560R 1/4W 2% 100PPM	24773-267R
R42	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R43	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R44	RES MF 1K0 1/4W 2% 100PPM	24773-273A
TR1	TR PSI BC308B 20V 130M - GEN	28433-455R
TR2	TR PSI BC308B 20V 130M - GEN	28433-455R
TR3	TR NSI 2N2369 15V 500M - SW	28452-197H
TR4	TR NSI 2N2369 15V 500M - SW	28452-197H
	CABLE ASSY RF	43130-038C
	CABLE ASSY RF	43130-043B

Circuit Ref	Description		Part Number
Unit A7	- LOW FREQUENCY COUNTER UNIT		
15. When ordering, prefix circuit reference with A7			
	Complete unit		44828-635T
C1	CAP CER 33P 500V 20% DISC		26343-146M
C2	CAP CER 33P 500V 20% DISC		26343-146M
C3	CAP PETP 100N 250V 20%		26582-799N
C5	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C6	CAP CER 2N2 63V 10% PLATE		26383-587R
C7	CAP CER 22N 18V 20% DISC		26383-007R
C8	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C9	CAP CER 22N 18V 20% DISC		26383-007R
C10	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C11	CAP CER 22N 18V 20% DISC		26383-007R
C12	CAP CER 22N 18V 20% DISC		26383-007R
C13	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C14	CAP CER 12P 63V 5% PLATE		26343-466E
C15	CAP CER 1N0 63V 10% PLATE		26383-585M
C16	CAP CER 1N0 63V 10% PLATE		26383-585M
C17	CAP CER 1N0 63V 10% PLATE		26383-585M
C18	CAP CER 22N 18V 20% DISC		26383-007R
C19	CAP CER 22N 18V 20% DISC		26383-007R
C20	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C21	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C22	CAP CER 22N 18V 20% DISC		26383-007R
C24	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C25	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C26	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C27	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
D1	DI SIL 1N4148 75V JUNC		28336-676J
D2	DI SIL 1N4148 75V JUNC		28336-676J
D3	DI ZEN BZY88C3V0 3V 5%		28371-203G
D4	DI ZEN BZY88C3V0 3V 5%		28371-203G
D5	DI SIL 1N4148 75V JUNC		28336-676J
D6	DI H/CARR HP5082-2835	!	28349-006H
D7	DI H/CARR HP5082-2835	!	28349-006H
D8	DI H/CARR HP5082-2835	!	28349-006H
IC1	ICD RX MC10216 TRIP LINE		28469-169J
IC2	ICD NOR 10102 QUAD 2INP		28466-219G
IC3	ICD CTR 10138 4BIT DEC		28464-019X
IC4	ICA AMP UA741CN GP DIL8		28461-304T
IC5	ICA COMP LM339N QUAD		28461-693H

Circuit Ref	Description	Part Number
Unit A7	- LOW FREQUENCY COUNTER UNIT (Contd.)	
IC6	ICD CTR 844 10 DECADE CUSTOM !	28464-021P
IC7	ICD CTR 74LS90 4BIT DEC 2,5,10	28464-014S
L1	IND CHOKE 108uH ASSY	44290-876X
L2	IND CHOKE 108uH ASSY	44290-876X
	BOARD SCREEN TOP	35904-207E
	BOARD SCREEN BASE	35904-208U
PLA	CON RF SMB MALE 50 PCB ELBOW	23444-359Z
R1	RES MF 470K 1/4W 2% 100PPM	24773-337R
R2	RES MF 470K 1/4W 2% 100PPM	24773-337R
R3	RES MG 10M 1/4W 5%	24321-885W
R4	RES MF 10R 1/4W 2% 100PPM	24773-225W
R5	RES MF 220K 1/4W 2% 100PPM	24773-329T
R6	RES MF 47R 1/4W 2% 100PPM	24773-241A
R7	RES MF 470R 1/4W 2% 100PPM	24773-265M
R8	RES MF 10R 1/4W 2% 100PPM	24773-225W
R9	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R10	RV CERM 10K LIN .5W 10% VERT	25711-603L
R11	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R12	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R13	RES MF 510R 1/4W 2% 100PPM	24773-266C
R14	RES MF 510R 1/4W 2% 100PPM	24773-266C
R15	RES MF 15K 1/4W 2% 100PPM	24773-301P
R16	RES MF 510R 1/4W 2% 100PPM	24773-266C
R17	RES MF 330R 1/4W 2% 100PPM	24773-261D
R18	RES MF 510R 1/4W 2% 100PPM	24773-266C
R19	RES MF 510R 1/4W 2% 100PPM	24773-266C
R20	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R21	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R22	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R23	RES MF 10K 1/4W 2% 100PPM	24773-297M
R24	RES MF 10K 1/4W 2% 100PPM	24773-297M
R25	RES MF 10K 1/4W 2% 100PPM	24773-297M
R26	RES NET 680R 5% SIP	24681-624Z
R27	RES MF 10K 1/4W 2% 100PPM	24773-297M
R28	RES MF 470K 1/4W 2% 100PPM	24773-337R
R29	RES MF 100K 1/4W 2% 100PPM	24773-321L
R30	RES MF 47K 1/4W 2% 100PPM	24773-313H
R31	RV CERM 10K LIN .5W 10% VERT	25711-603L
R32	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R33	RES MF 560K 1/4W 2% 100PPM	24773-340R
R34	RES MF 560K 1/4W 2% 100PPM	24773-340R
R35	RES MF 100R 1/4W 2% 100PPM	24773-249J

Circuit Ref	Description		Part Number
Unit A7	- LOW FREQUENCY COUNTER UNIT (Contd.)		
R36	RES MF 10K 1/4W 2% 100PPM		24773-297M
R37	RES NET 10K 5% 8DIL		24681-511P
R38	RES MF 3K9 1/4W 2% 100PPM		24773-287V
R39	RES MF 1K2 1/4W 2% 100PPM		24773-275H
R40	RES MF 12K 1/4W 2% 100PPM		24773-299R
R41	RES MF 560R 1/4W 2% 100PPM		24773-267R
R42	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R43	RES MF 5K6 1/4W 2% 100PPM		24773-291S
R44	RES MF 3K9 1/4W 2% 100PPM		24773-287V
R45	RES MF 560R 1/4W 2% 100PPM		24773-267R
R46	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R47	RES MF 15K 1/4W 2% 100PPM		24773-301P
RL1	RELAY REED 1NO 5V 230R COAX		23486-513G
SKB	S/C ACC SKT DIL24 LOW PROFILE		28488-044N
TR1	TR NMF 40673 20V 400M DG	!	28459-010V
TR2	TR NSI 2N2369 15V 500M - SW		28452-197H
TR3	TR NSI 2N2369 15V 500M - SW		28452-197H
TR4	TR NSI 2N2369 15V 500M - SW		28452-197H
TR5	TR NSI BC208B 20V 150M - GEN		28452-781A
TR6	TR NSI 2N2369 15V 500M - SW		28452-197H
	CABLE COAX 29CM SMB-FEM/-		43130-042R
	CABLE COAX 15CM SMB-FEM/-		43130-044K

Circuit Ref	Description		Part Number
Unit A8	- PROCESSOR		
16. When ordering, prefix circuit reference with A8			
	Complete unit		44828-637X
C1	CAP TANT 4U7 35V 20% BEAD		26486-219P
C2	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C3	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C4	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C5	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C8	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C9	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C12	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C13	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C14	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
C15	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
IC1	ICD MP P8085A 8BIT NMOS	!	28469-396K
IC2	ICD MP SUP 8155 2KRAM+I/O+TIM	!	28469-304E
IC3	ICD DEC/DMX 74LS138 3-8		28465-027F
IC4	ICD LATCH 74LS373 OCT 3ST		28462-410E
IC6	ICD BUFF 74LS245 OCT TXRX		28469-188B
IC7	ICD NAND 74LS10 TRIP 3INP		28466-351Y
PLA	CON PCB HDR 20WAY FXD RT ANGLE		23435-950S
PLB	TERM C/PIN 0.64SQX6 S/E REEL		23435-188V
PLC	TERM C/PIN 0.64SQX6 S/E REEL		23435-188V
PLD	TERM C/PIN 0.64SQX6 S/E REEL		23435-188V
PLE	TERM C/PIN 0.64SQX6 S/E REEL		23435-188V
PLG	TERM C/PIN 0.64SQX6 S/E REEL		23435-188V
R1	RES NET 4K7 2% 7SIP		24681-608D
R2	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R3	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R4	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R5	RES MF 47K 1/4W 2% 100PPM		24773-313H
SKA	S/C ACC SKT DIL14 LOW PROFILE		28488-040H
SKB	S/C ACC SKT DIL28 LOW PROFILE		28488-045L
X1	XTAL 6.144M P30P 75R		28312-054J

Circuit Ref		Description	Part Number
Unit AC00		- GPIB UNIT	
17. When ordering, prefix circuit reference with AC00			
		Complete unit	54433-002Y
SKB		CON 57 FEM 24 FXD PCB EDG - GPIB	23435-133X
Unit AC01		-GPIB INTERFACE BOARD	
18.		Complete board	44828-639C
C1		CAP TANT 4.7UF 35V 20% BEAD	26486-219P
C2		CAP CER 0.047UF 25V 20% DISC	26383-017U
IC1		ICD NAND 74KS00 QUAD 2INP	28466-345H
IC2		ICD BUFF 74LS365	28469-194Z
IC3	!	ICD MP SUP 8291A GPIB TALK/LIST	28467-014C
IC4		ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC5		ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC6		ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC7		ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
R1		RES MF 47K 1/4W 2% 100PPM	24773-313H
R2		RES MF 47K 1/4W 2% 100PPM	24773-313H
R3		RES MF 47K 1/4W 2% 100PPM	24773-313H
R4		RES MF 47K 1/4W 2% 100PPM	24773-313H
R5		RES MF 47K 1/4W 2% 100PPM	24773-313H
R6		RES MF 47K 1/4W 2% 100PPM	24773-313H
SW		SW DIL 6SW - GPIB ADDRESS	23465-897N
		CABLE ASSY	43129-825W

Circuit Ref	Description	Part Number
Unit AC3	- D TO A CONVERTER UNIT (Optional accessory)	
19.	Complete unit	54414-001S
	FITTING INSTRUCTIONS .	46881-577H
SKA	CON RF BNC FEM 50 BKHD	23443-442B
Unit AC31	- D TO A CONVERTER BOARD	
20. When ordering, prefix circuit reference with AC31		
	Complete unit	44828-640X
C1	CAP ELEC 47U 10V 20%+ AX	26415-809E
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 4N7 63V 10% PLATE	26383-591B
C4	CAP CER 2N2 63V 10% PLATE	26383-587R
C5	CAP ELEC 47U 10V 20%+ AX	26415-809E
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 4N7 63V 10% PLATE	26383-591B
C9	CAP CER 4N7 63V 10% PLATE	26383-591B
C10	CAP PETP 47N 63V 10% RAD MIN	26582-428J
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C14	CAP CER 4N7 63V 10% PLATE	26383-591B
C15	CAP PETP 220N 63V 10% RAD MIN	26582-430L
IC1	ICA DAC 7542 12BIT MULT MP-COM	28469-435A
IC2	ICA AMP OP-07C 150UV OFFSET	28461-374M
IC3	ICA AMP OP-07C 150UV OFFSET	28461-374M
IC4	ICA AMP OP-07C 150UV OFFSET	28461-374M
IC5	ICA VREG ZN458A 2.45V PREC REF	28461-740J
R2	RES MF 10K 1/4W 2% 100PPM	24773-297M
R3	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R4	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R5	RV CERM 1K LIN .3W 10% FLAT	25748-504D
R6	RES MF 10K 1/4W 0.5% 50PPM	24753-628N
R9	RES MF 39K 1/4W 2% 100PPM	24773-311A
R10	RV CERM 10K LIN .3W 10% FLAT	25748-507X
R12	RES MF 10K 1/4W 2% 100PPM	24773-297M
R13	RES MF 47R 1/4W 2% 100PPM	24773-241A
R14	RES MF 6K81 1/4W 0.5% 50PPM	24753-619A
	CABLE ASSY	43129-825W

Circuit Ref	Description	Part Number
Unit 05	- 10 MHZ OSCILLATOR (MS)TCXO	
21. Fitted in versions 52440-301C and 304K.		
	Complete unit	44990-273N
Unit 06	- 10 MHZ OSCILLATOR (HS)OCXO	
22. Fitted in versions 52440-302R and 305A.		
	Complete unit	44990-419S
	- REAR INPUT KIT(SMA)	
23. Fitted in versions 52440-304K and 305A.		
	Complete unit	46883-709X
	FITTING INSTRUCTIONS	46881-518L
	CABLE REAR INPUT	43130-123Y

Circuit Ref	Description	Part Number
24.	- SUPPLIED ACCESSORIES	
	CABLE ASSY MAINS ELB CEE22 LBL	43129-003W
	COVER POLYTHENE	37490-435X
	OPERATING MANUAL H52440-900N	46881-486G
	GPIB INSTRUCTION CARD	46881-551Y
25.	- OPTIONAL ACCESSORIES	
	CABLE GPIB 1M IEEE	43129-189U
	CON ADAPT GPIB IEEE/IEC	46883-408K
	ADAPTER N-SMA	54311-094M
	CABLE ASSY FLEX 18GHZ N-MALE .5M	54351-022X
	CABLE ASSY FLEX 18GHZ SMA MALE .5	54351-023M
	RF CABLE ASSY BNC-SMC 1M	54351-024C
	ATTENUATOR 10DB, 5W, TYPE 6534/3	
	ATTENUATOR 20DB, 5W, TYPE 6534/4	
	EXTENDER CARD	46883-645R
	EXTENDER CARD (PROCESSOR)	46883-644C
	ACCESSORY BOX	46883-666S
	SPANNER TUBULAR (SERVICE AID)	46883-726Y
	RACK MOUNTING KIT (DOUBLE UNIT)	46883-536P
	RACK MOUNTING KIT (SINGLE UNIT)	46883-638P
	BLANK FRAME UNIT	46883-537X
	FRONT PANEL COVER (STOWAGE)	54124-022L
	GPIB MANUAL H 54811-010P	46881-365R
	SERVICE MANUAL H 52440-900N, Vol. 2	46881-487V

Item	Description	Part Number
	MISCELLANEOUS MECHANICAL PARTS	
	26. Item numbers refer to Fig. 1. Order without prefix.	
1	PANEL,FRONT (MARKED)	35904-117S
	PANEL,SUPPORT	35904-118W
2	TOP COVER	35903-667U
3	SIDE RAIL	34900-747N
4	FLANGE	37590-221X
5	SPRING WASHER	31119-045W
6	ARM	37590-222M
7	REAR FOOT	37590-505Z
8	CAP	37590-219M
9	BOSS	37590-220P
10	HANDLE ASSEMBLY	41700-239W
11	REAR FRAME	35890-072W
12	REAR PANEL	35904-120S
13	BOTTOM COVER	35903-668Y
14	FRONT FRAME	35890-083B
15	STUD	37590-223C
16	BOTTOM FOOT	37590-224R

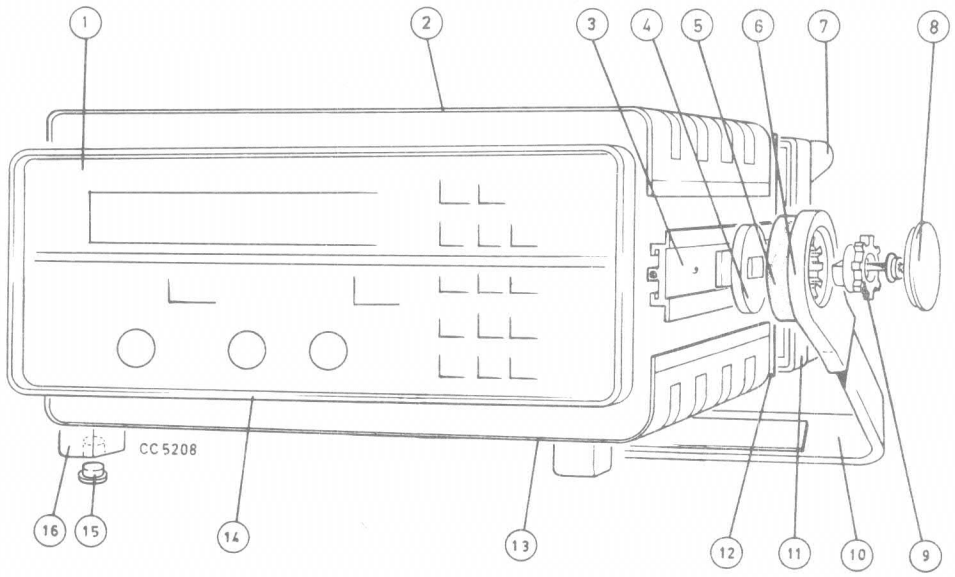


Fig. 1 Miscellaneous mechanical parts

Chapter 7

SERVICING DIAGRAMS

CONTENTS

CIRCUIT NOTES

1. Component values

Resistors : Code letter R = ohms, k = kilohms (10^3), M = megohms (10^6).

Capacitors : Code letter m = millifarads (10^{-3}), μ = microfarads (10^{-6}), n = nanofarads (10^{-9}), p = picofarads (10^{-12}).

Inductors : Code letter H = henrys, m = millihenrys (10^{-3}), μ = microhenrys (10^{-6}), n = nanohenrys (10^{-9}).

† SIC : value selected during test, nominal value shown.

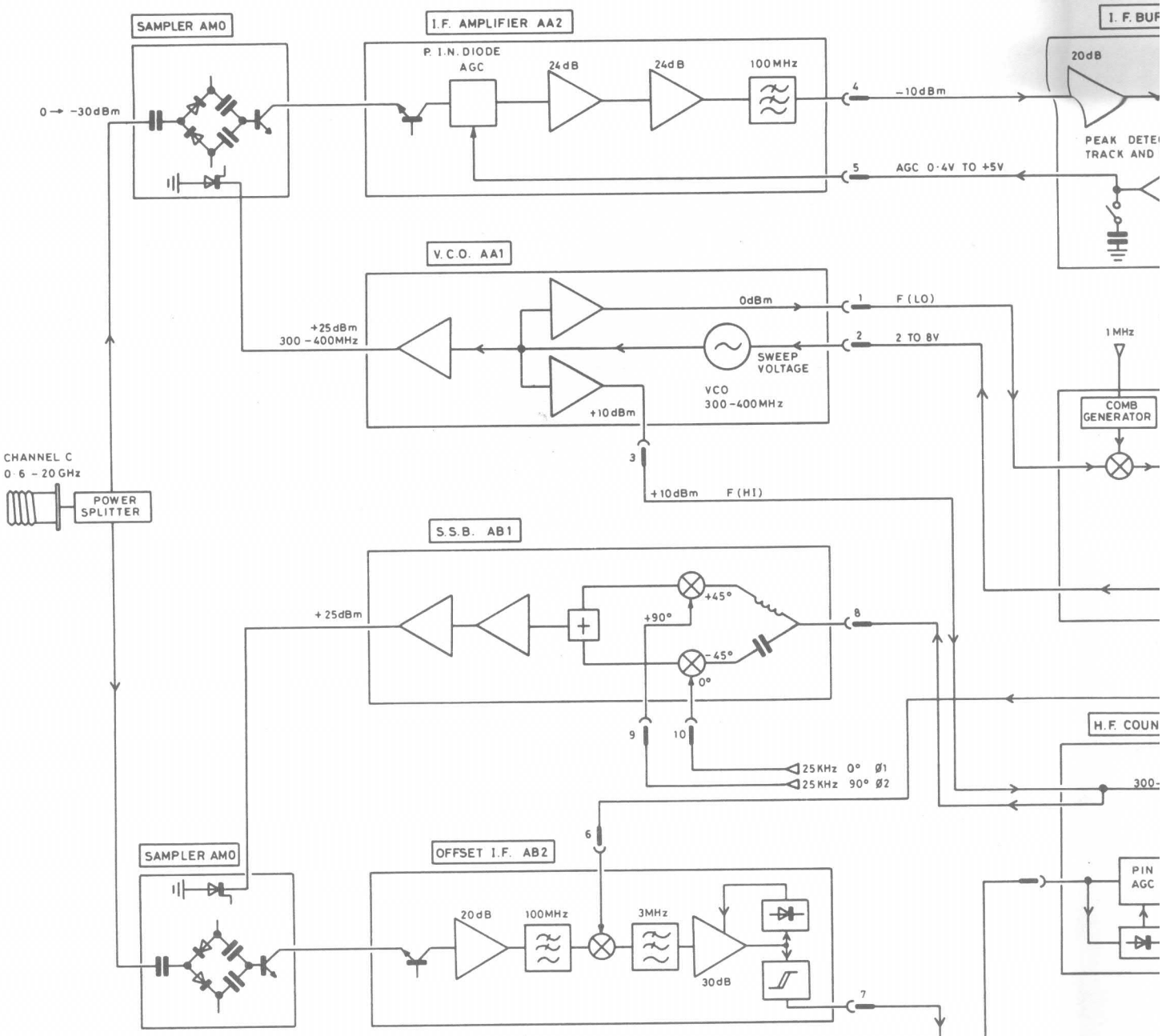
2. Components are marked normally with two, three or four figures according to the accuracy limit ±10%, ±1% or ±0.1%. The code letter used indicates the multiplier and replaces the decimal point. Because a marking 4m7 could be interpreted as milliohms, millifarads or millihenrys all values are placed near to its related symbol.

3. Symbols

Symbols are based on the provisions of BS 3939 with the following additions :

⚠ warning, see page (iv), Notes and Cautions.

(A1) unit identification number.



DESIGNATOR	CIRCUIT
A1	Z 44828 - 624L
A2	Z 44828 - 626F
A3	Z 44828 - 625J
A4	Z 44828 - 630G
A5	Z 44828 - 632S
A6	Z 44828 - 634D
A7	Z 44828 - 635T
A8	Z 44828 - 637X
AA1	Z 44828 - 643R
AA2	Z 44828 - 644B
AB1	Z 44828 - 631V
AB2	Z 44828 - 628V
AM0	Z 44990 - 471A

Z52440-900N Iss. 2

2440 block dia

Fig. 1

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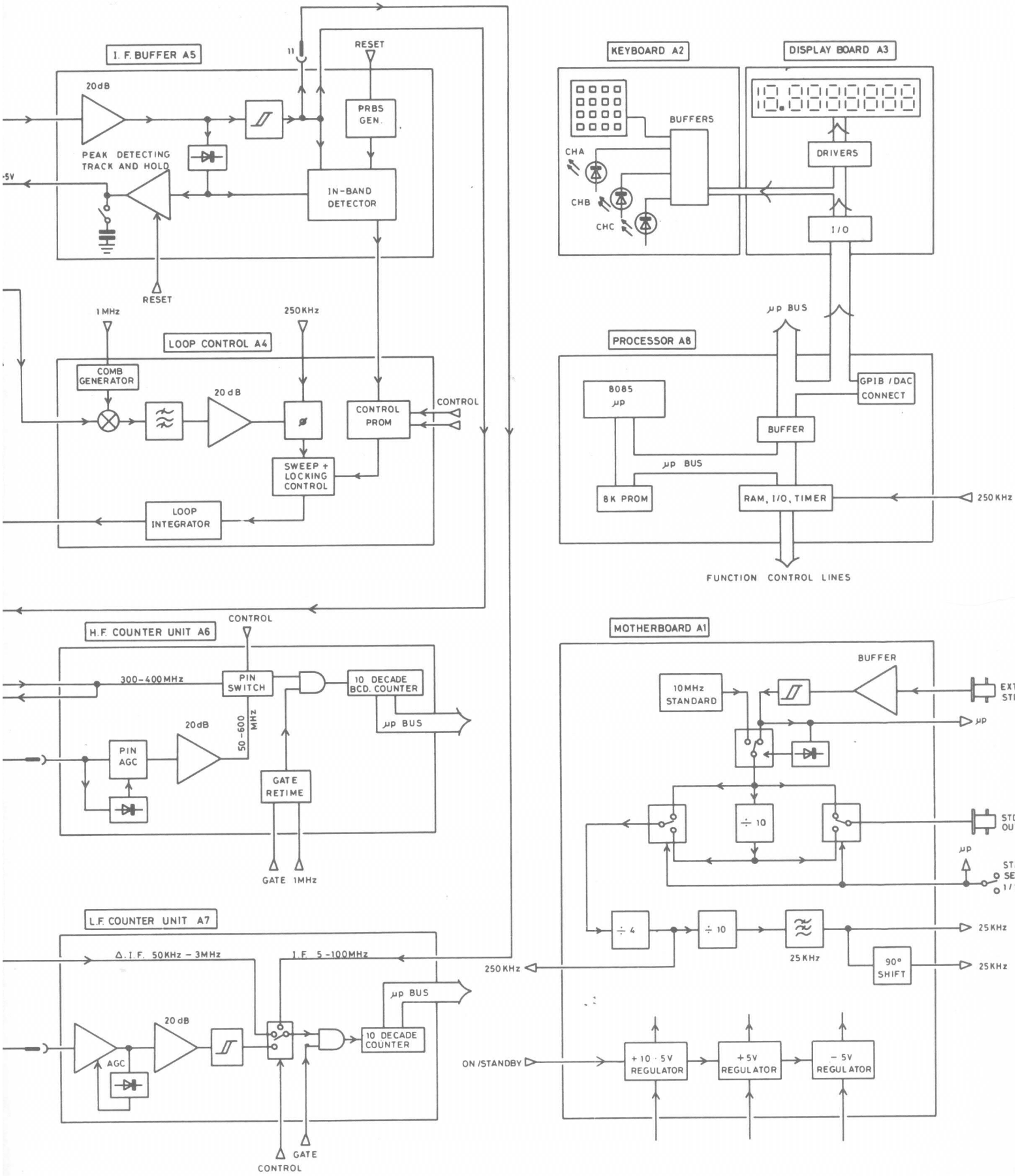

2440 block diagram, sheet 1

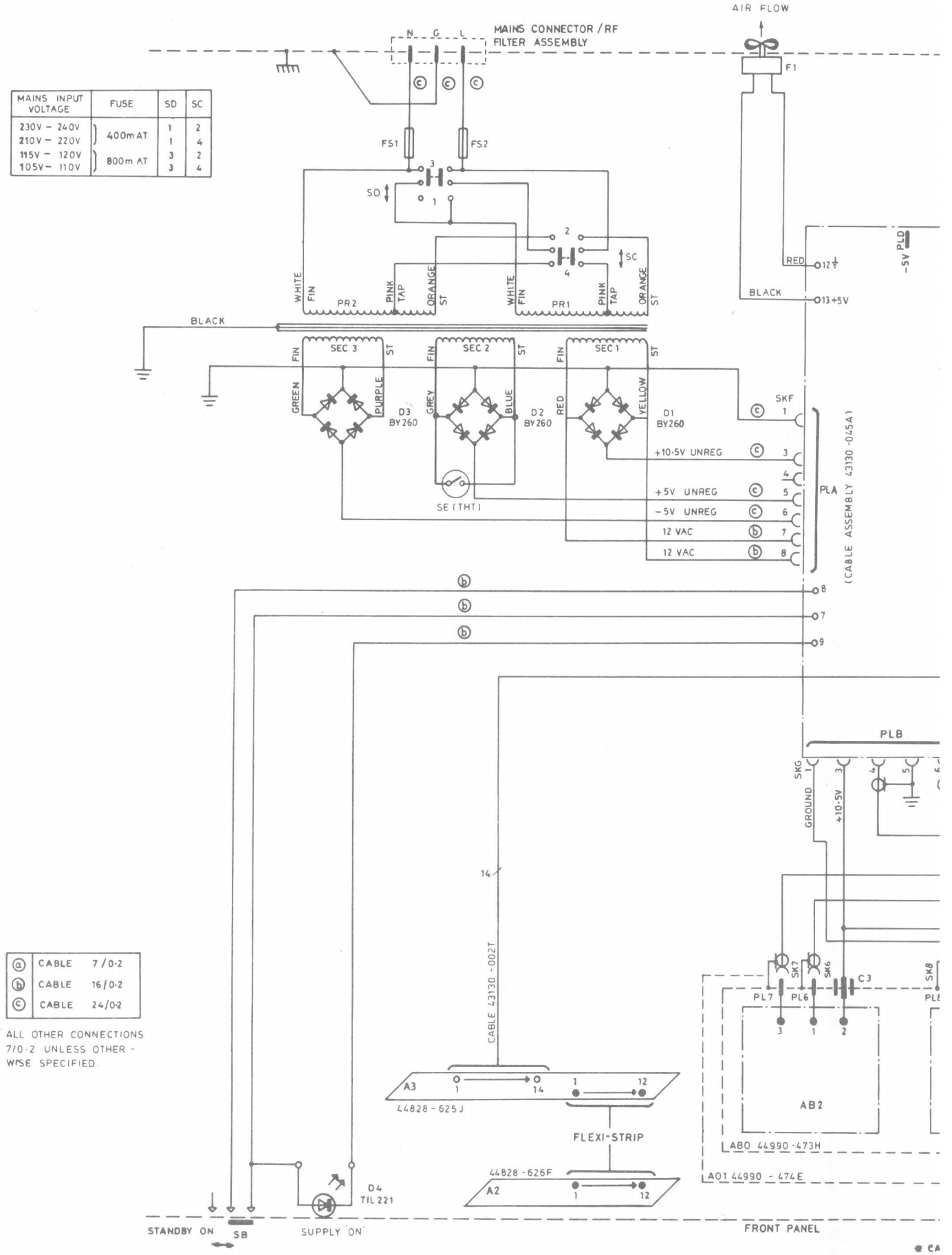

Fig. 2 Z52440-900N Iss. 4 AO 2440 interconnection dia

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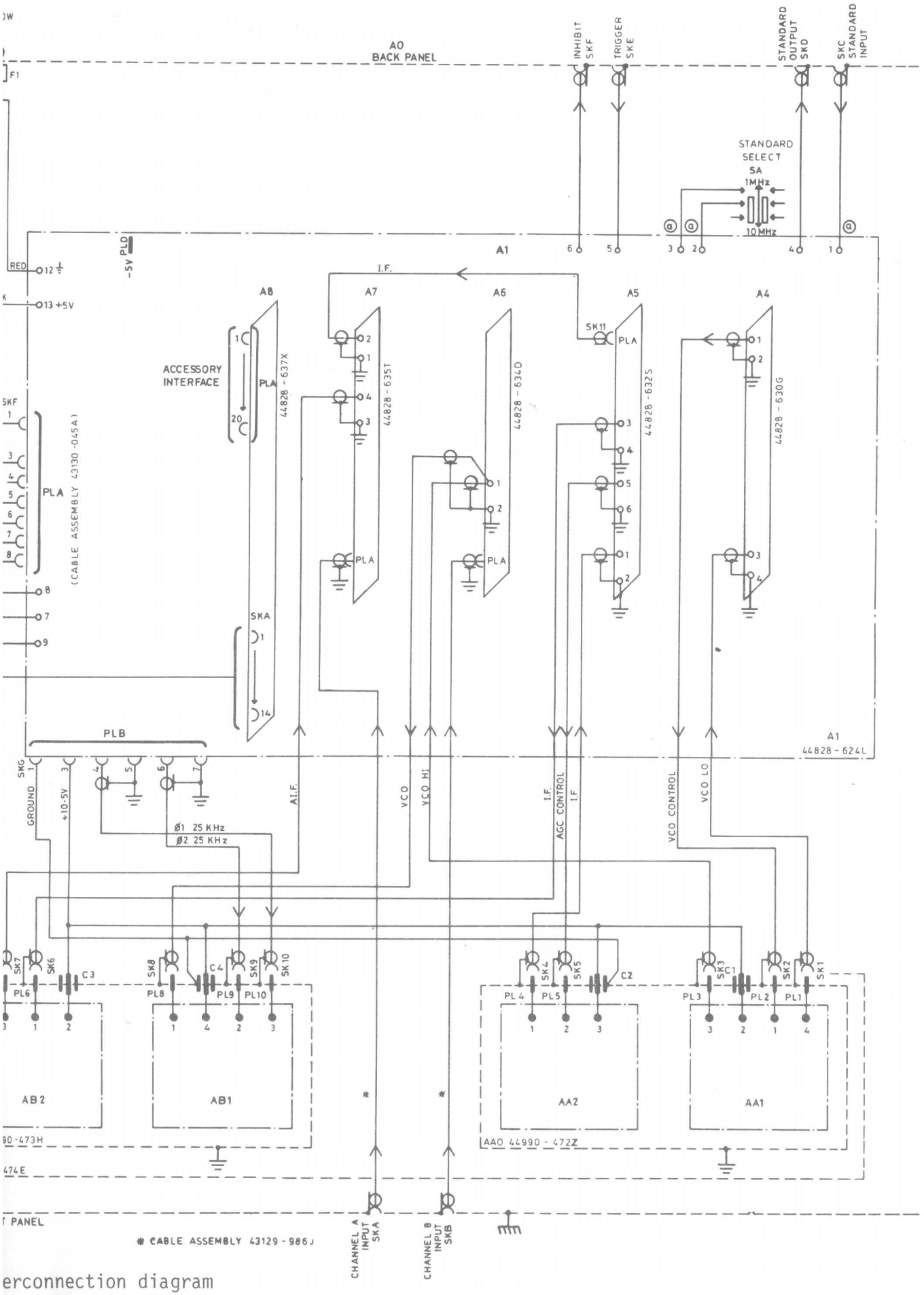
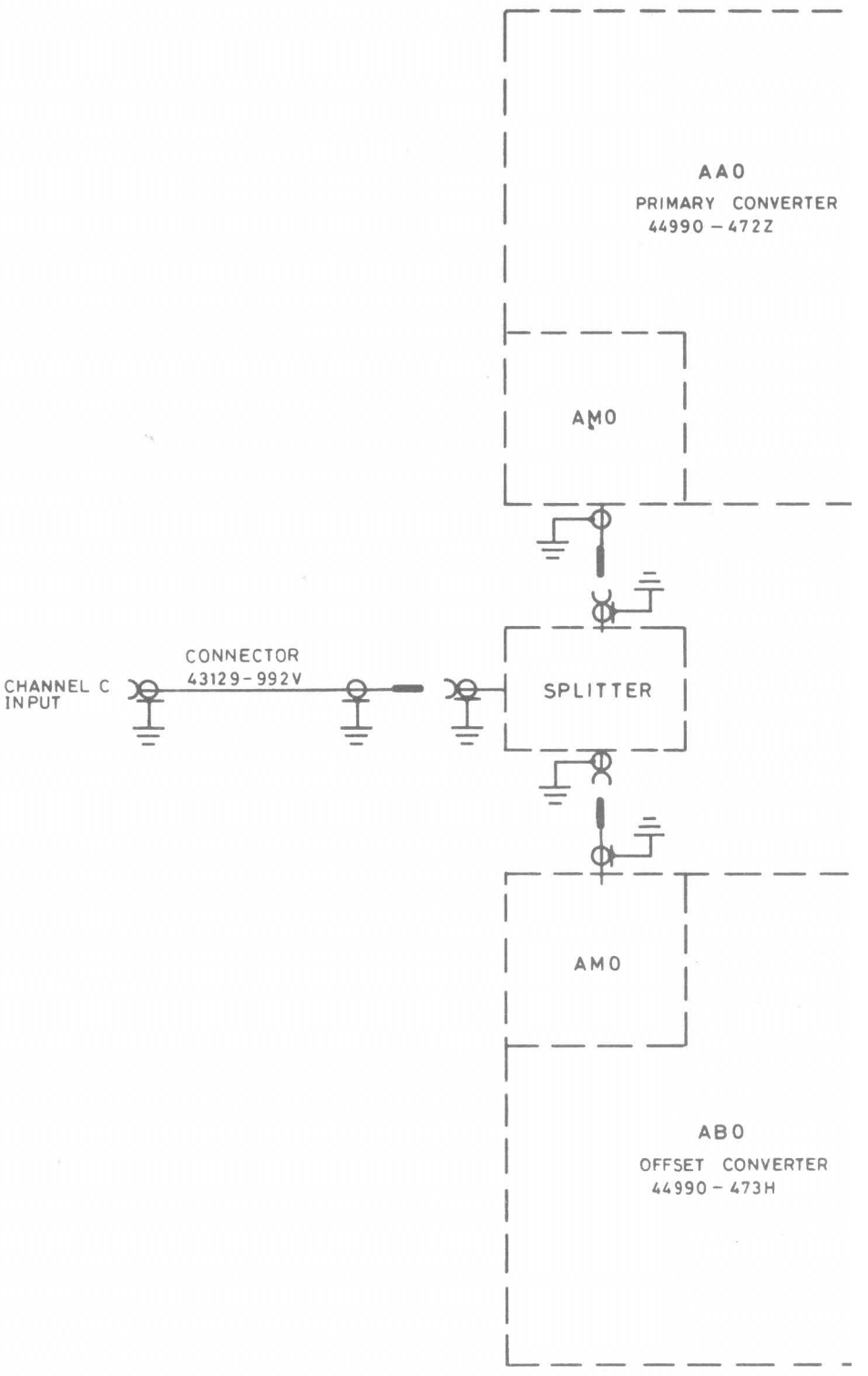


erconnection diagram

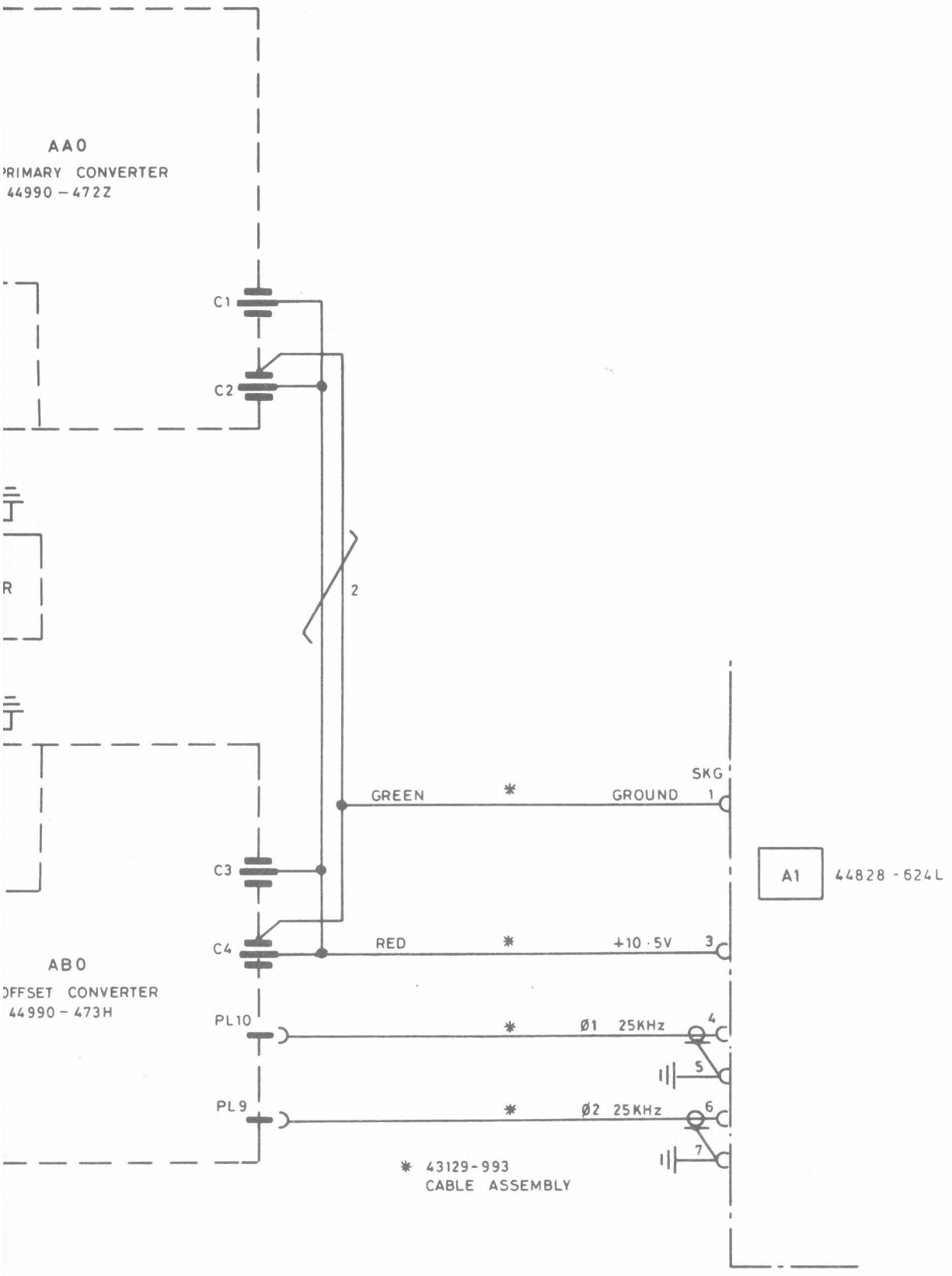


Z44990-474E Iss. 3

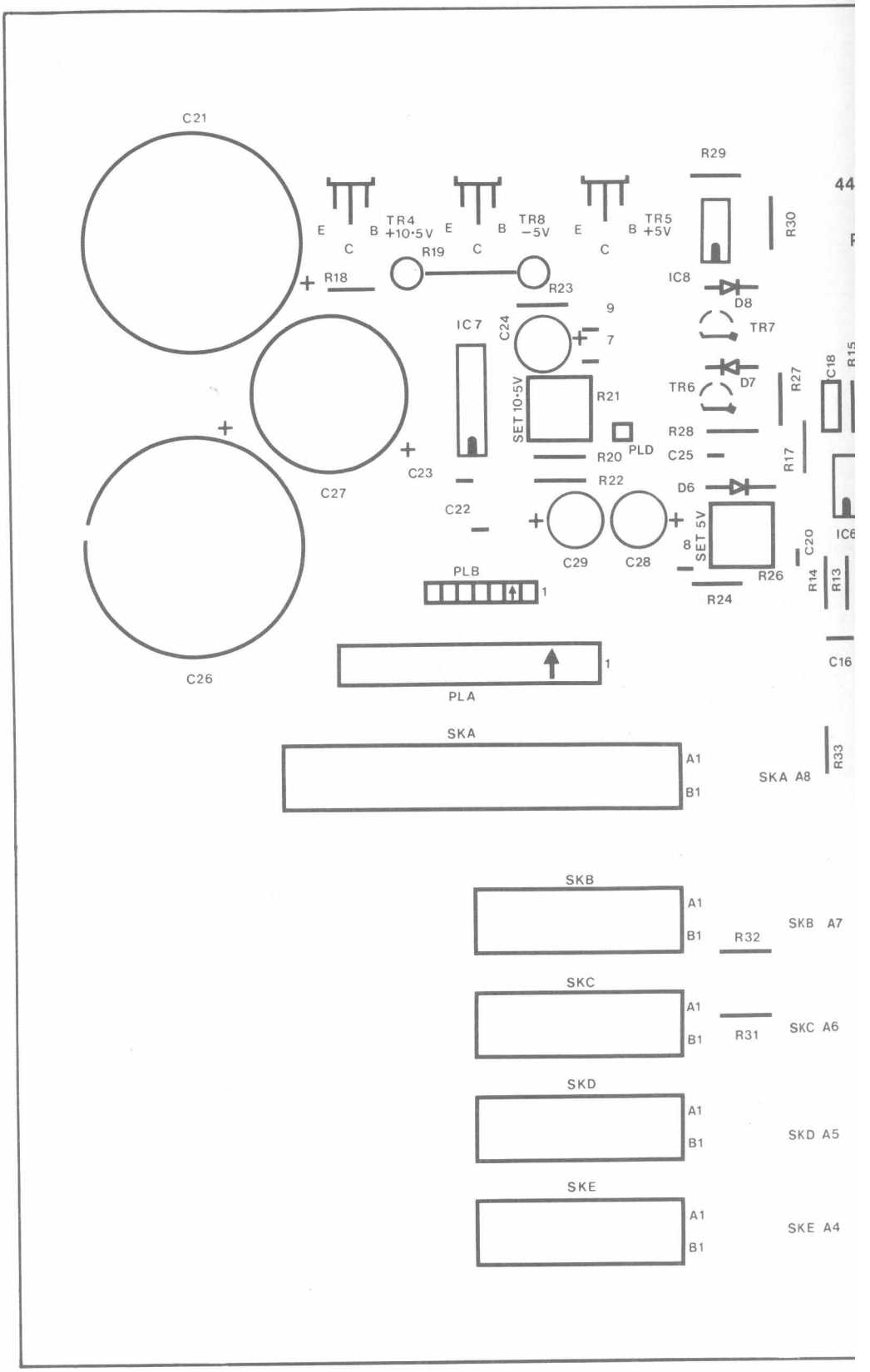
A01 Microwave tray, interc

Fig. 3

Jan. 85

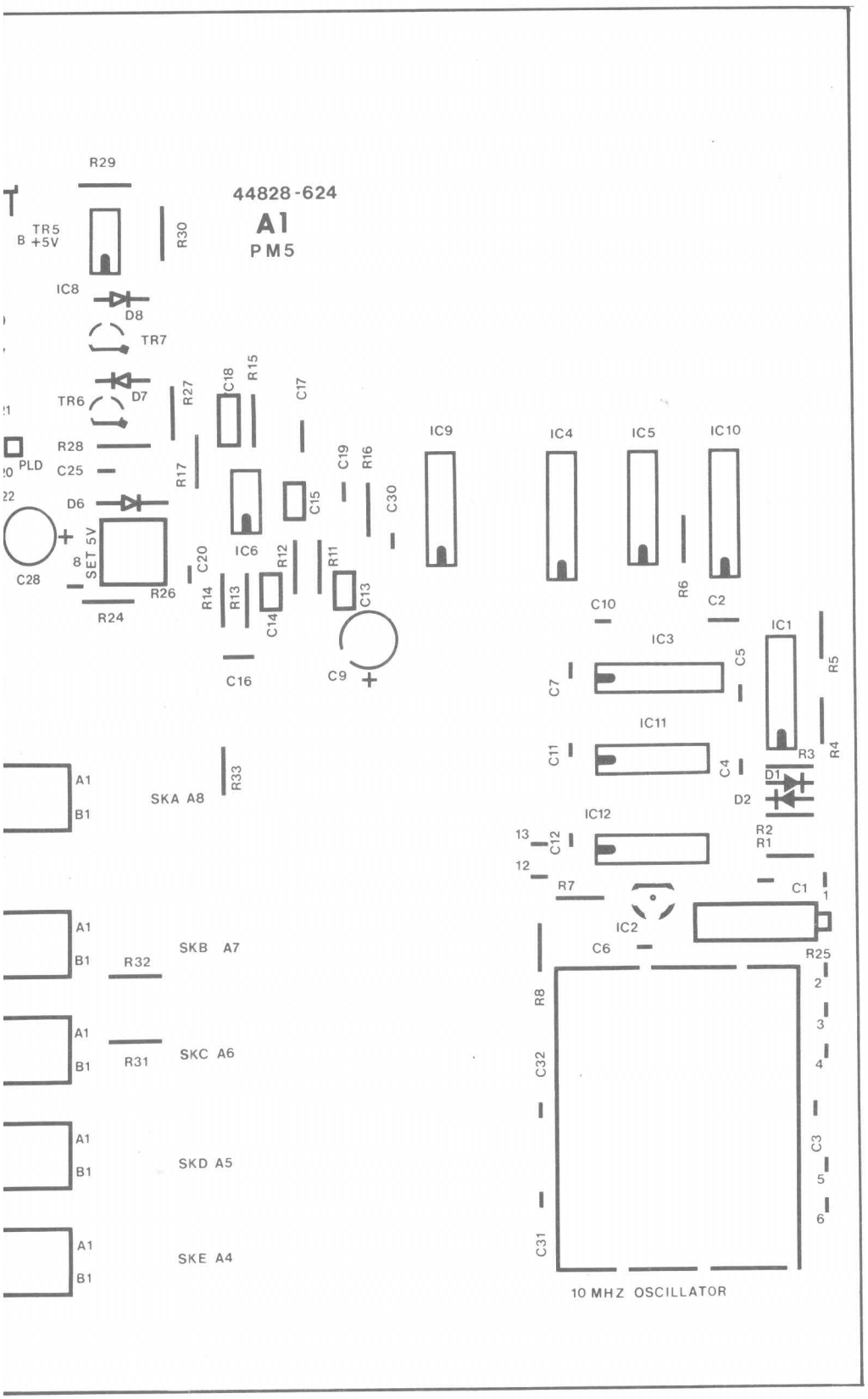


ve tray, interconnection diagram



A1 Motherboard, compone

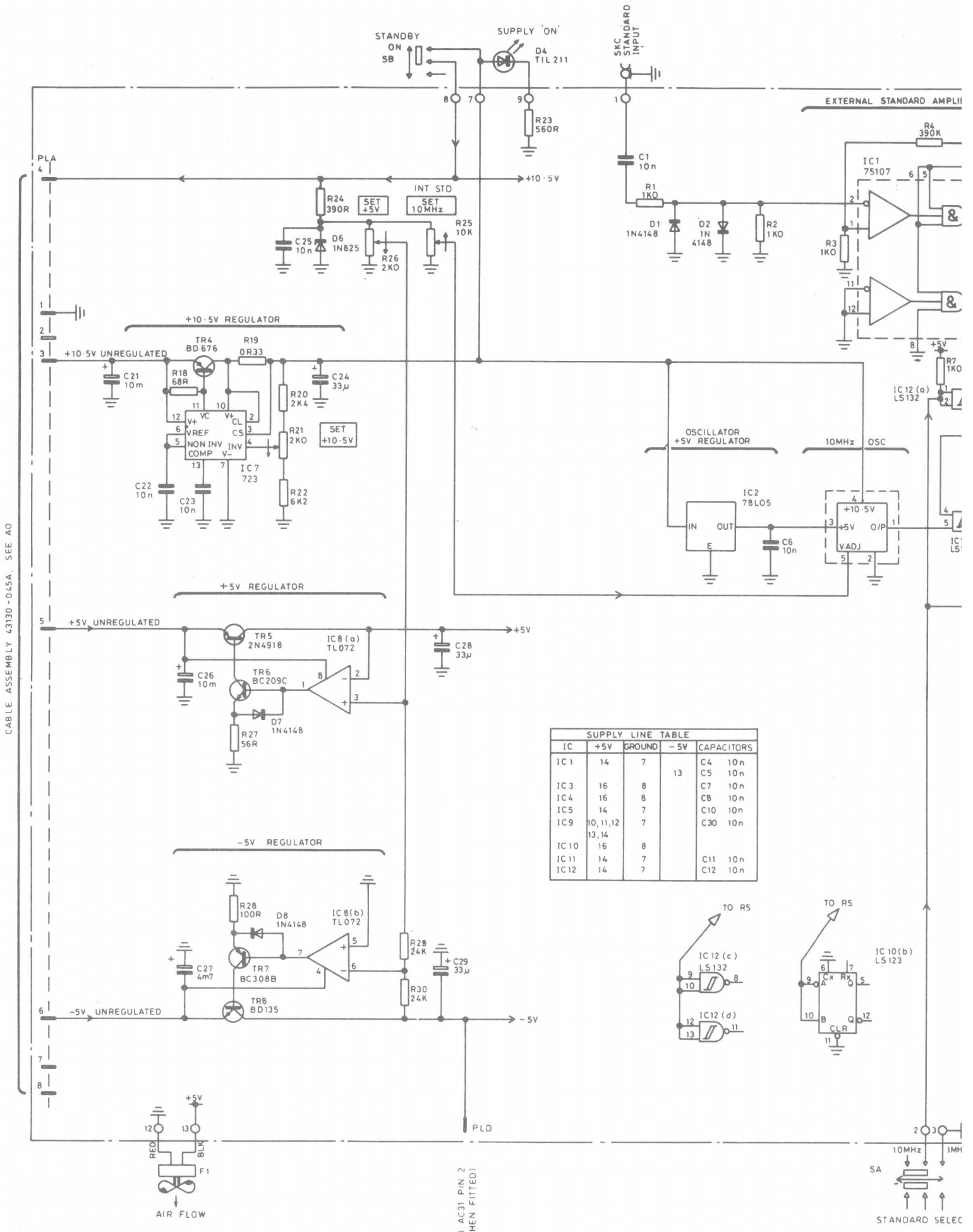
Fig. 4
Chap. 7
Page 8



otherboard, component layout

Fig. 4

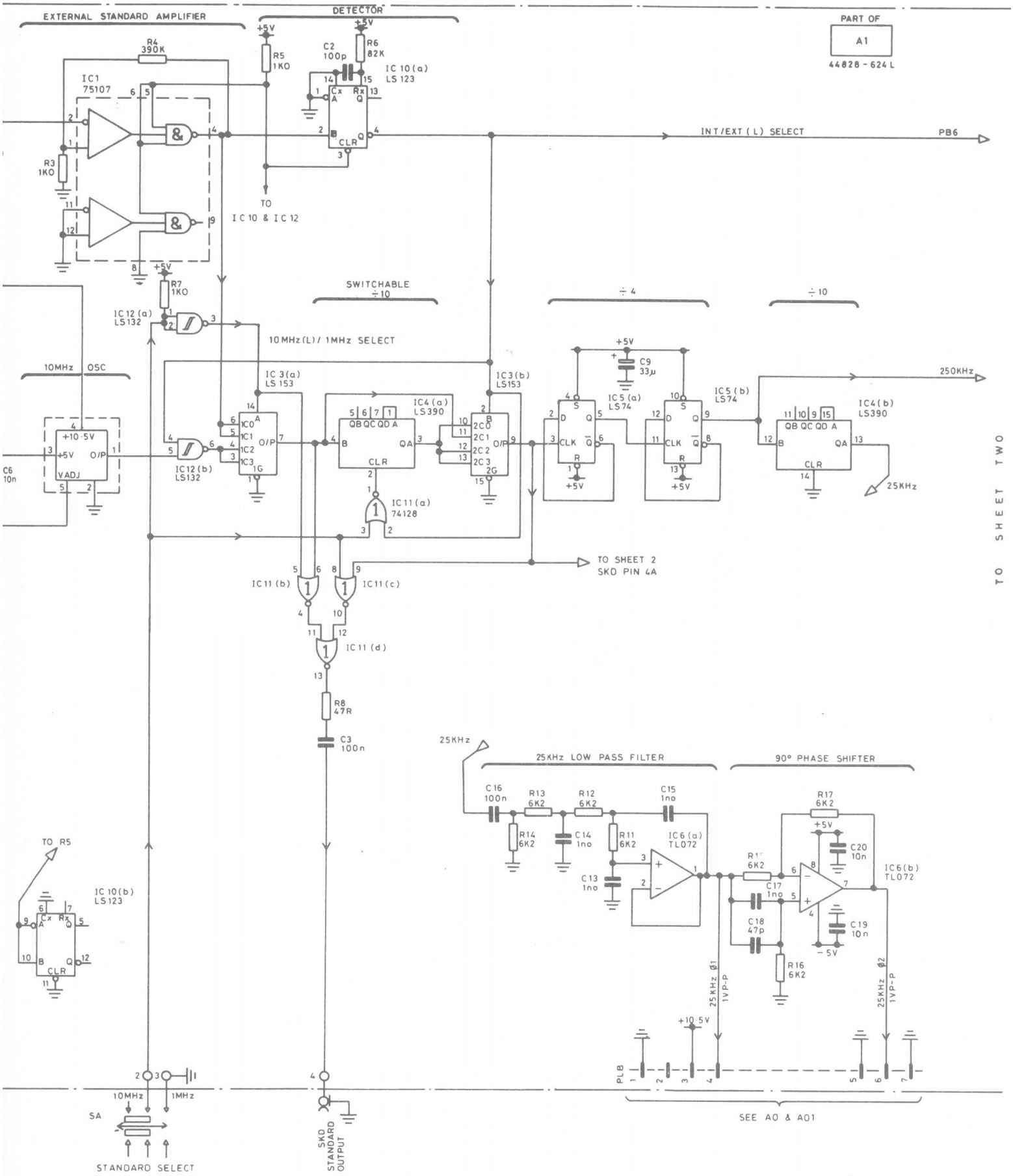
Jan. 85



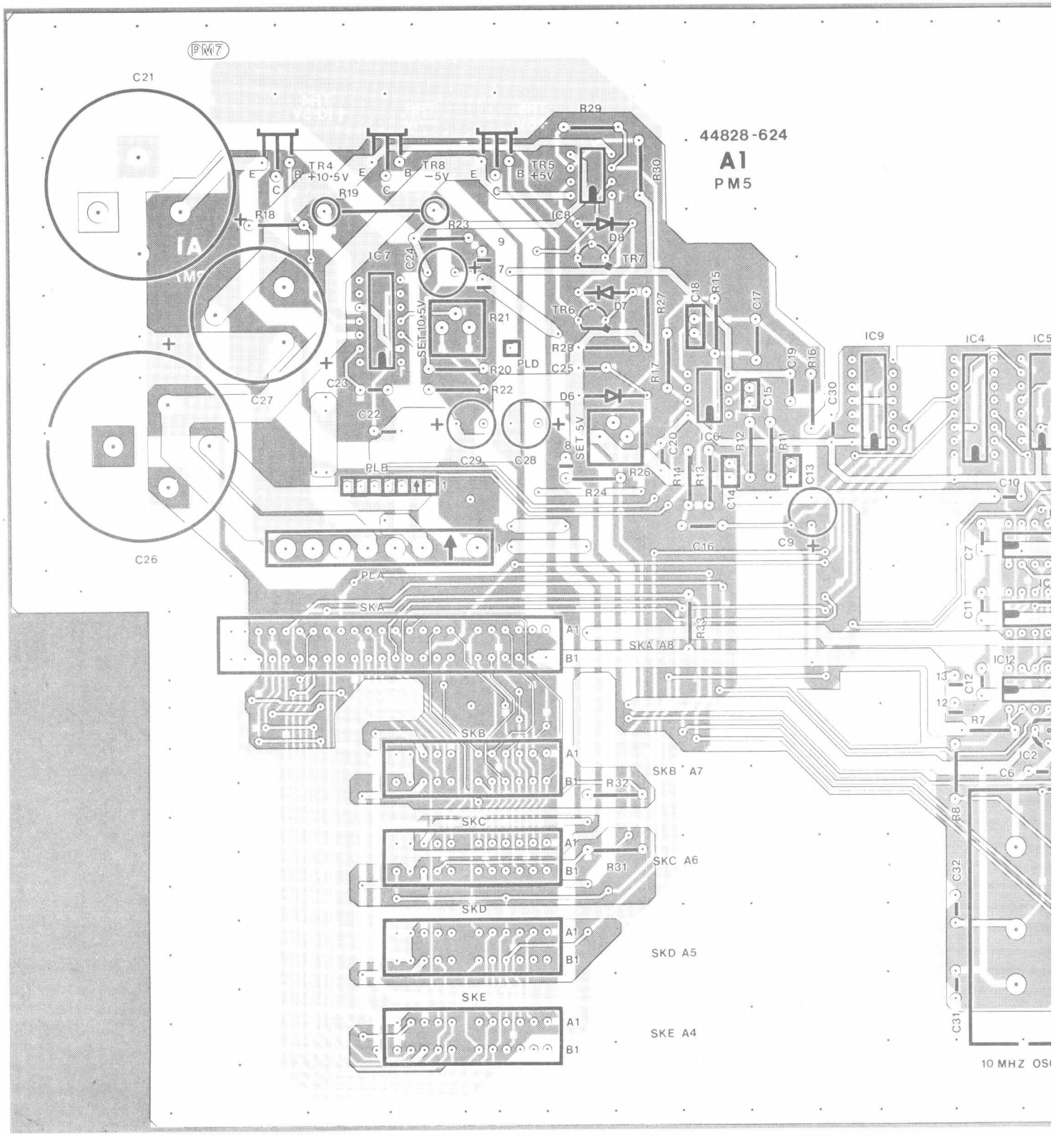
SUPPLY LINE TABLE				
IC	+5V	GROUND	-5V	CAPACITORS
IC1	14	7	13	C4 10n C5 10n
IC3	16	8		C7 10n
IC4	16	8		C8 10n
IC5	14	7		C10 10n
IC9	10, 11, 12 13, 14	7		C30 10n
IC10	16	8		
IC11	14	7		C11 10n
IC12	14	7		C12 10n

Fig. 5 Z44828-624L Iss. 6 A1 Motherboard, circuit diagr

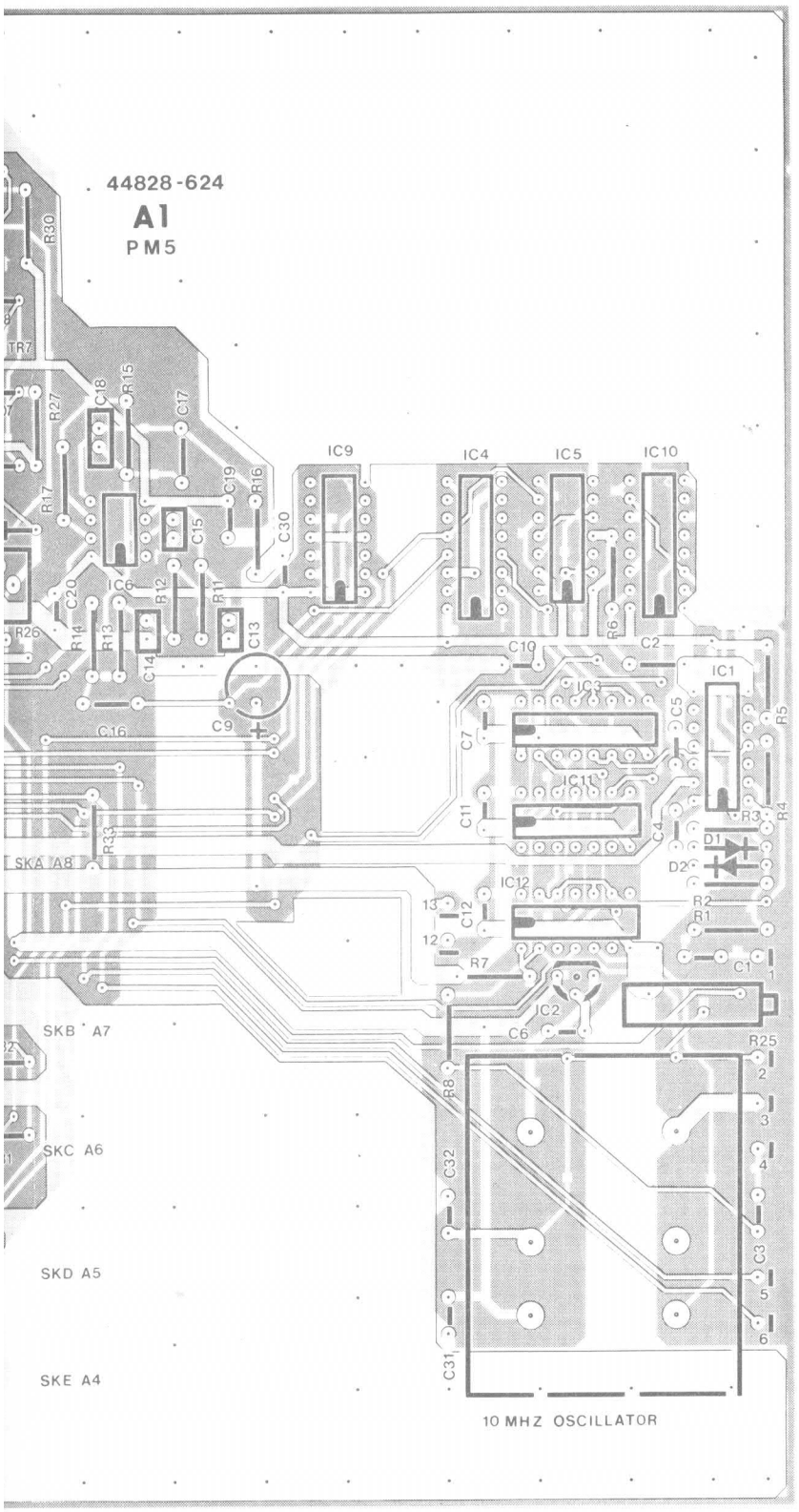
Jan. 85



oard, circuit diagram, sheet 1



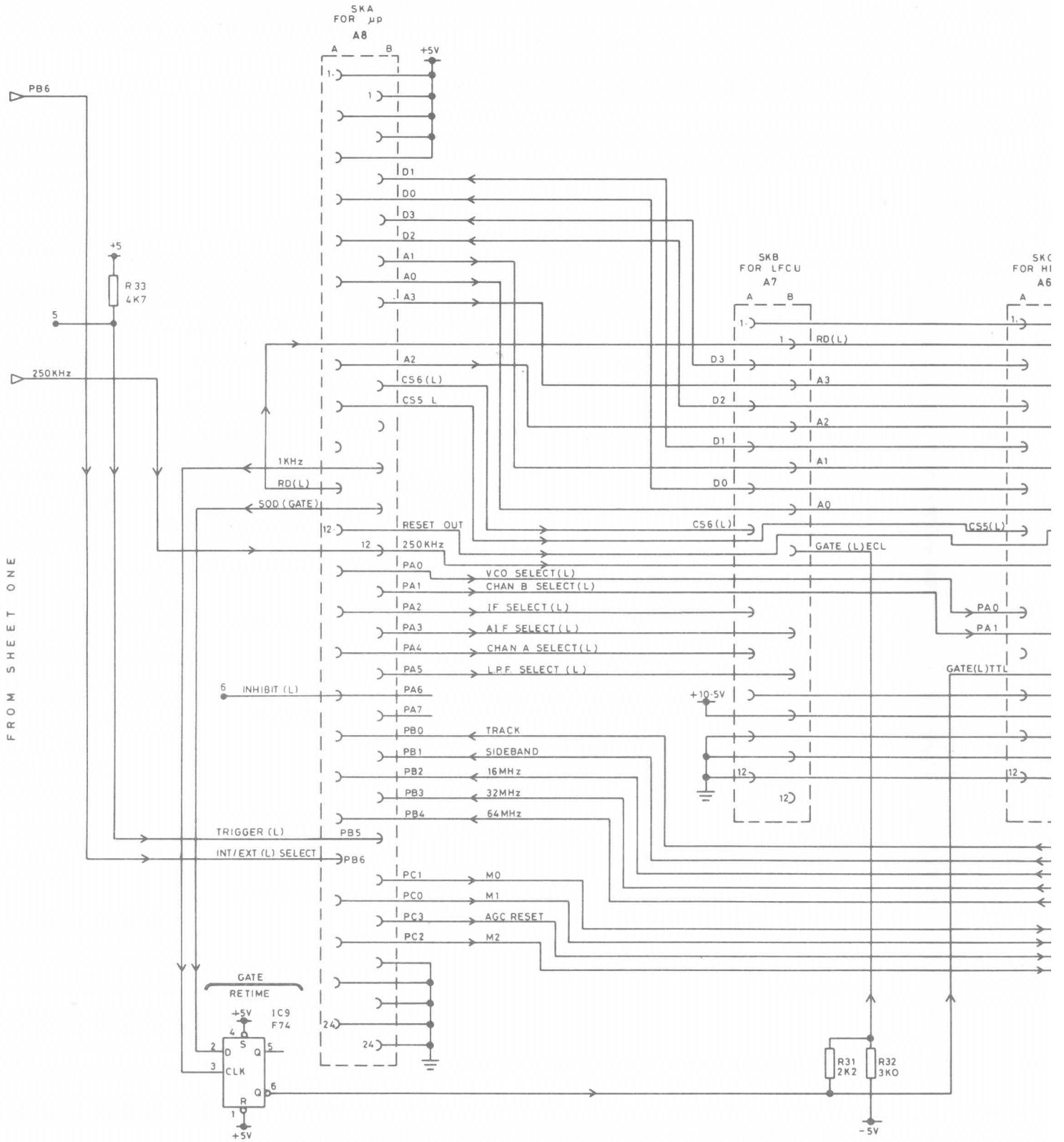
A1 Motherboard, p.c.b. layout



rd, p.c.b. layout

Fig. 6

Jan. 85

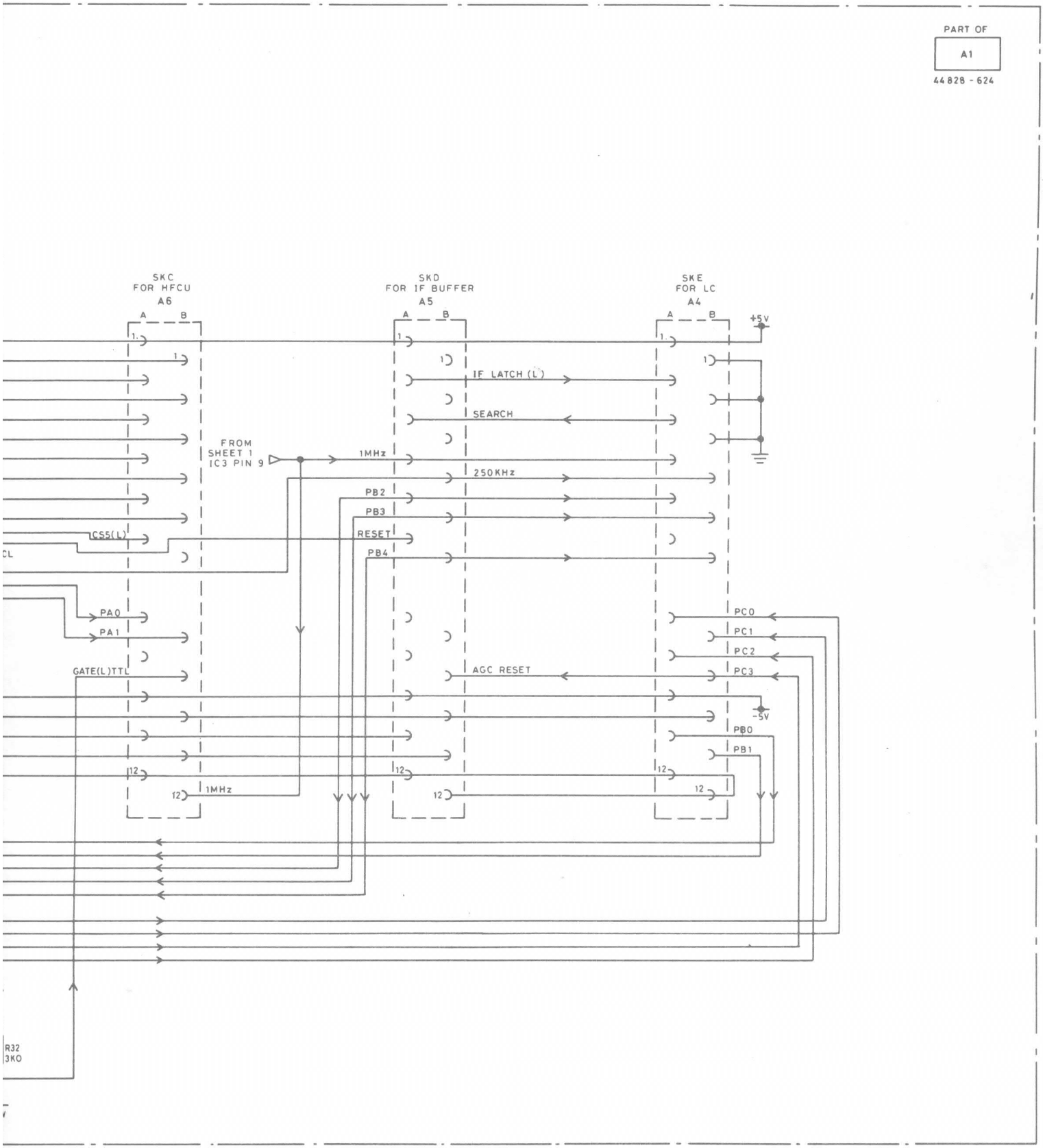


Z44828-624L Iss. 6

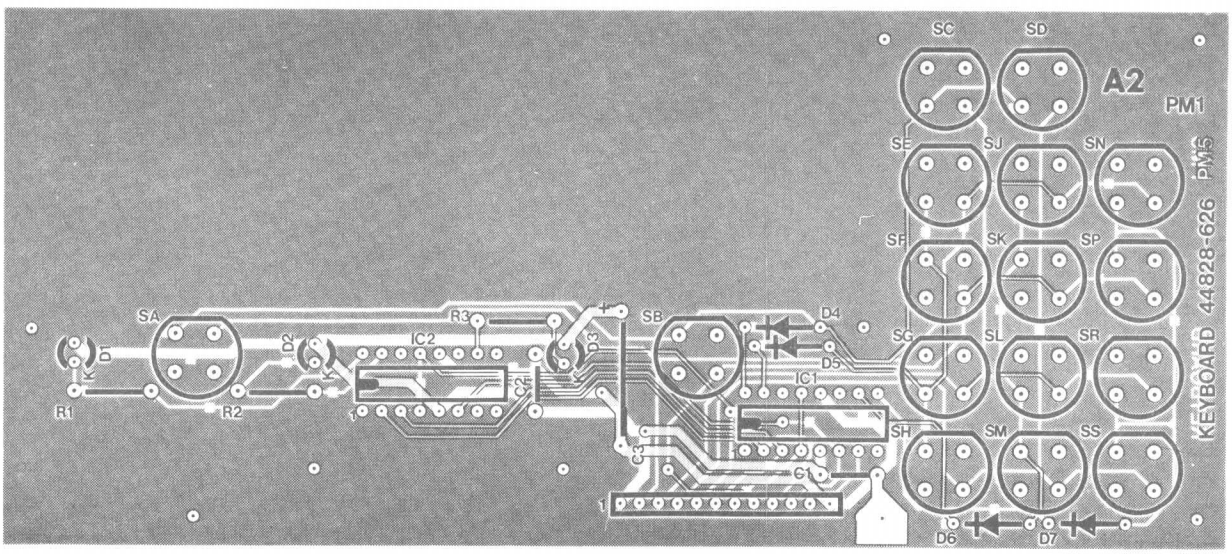
A1 Motherboard, circuit dia

Fig. 7

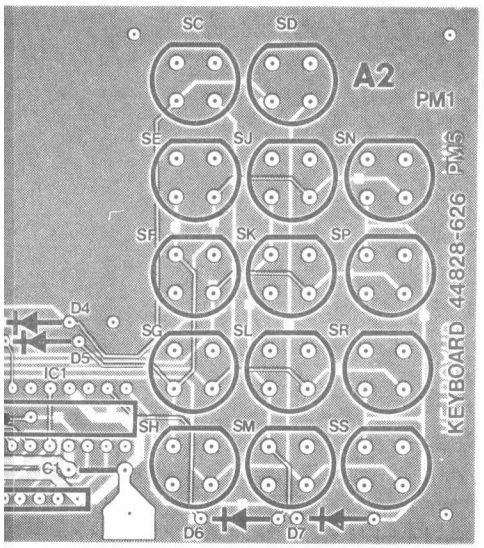
Jan. 85



ard, circuit diagram, sheet 2



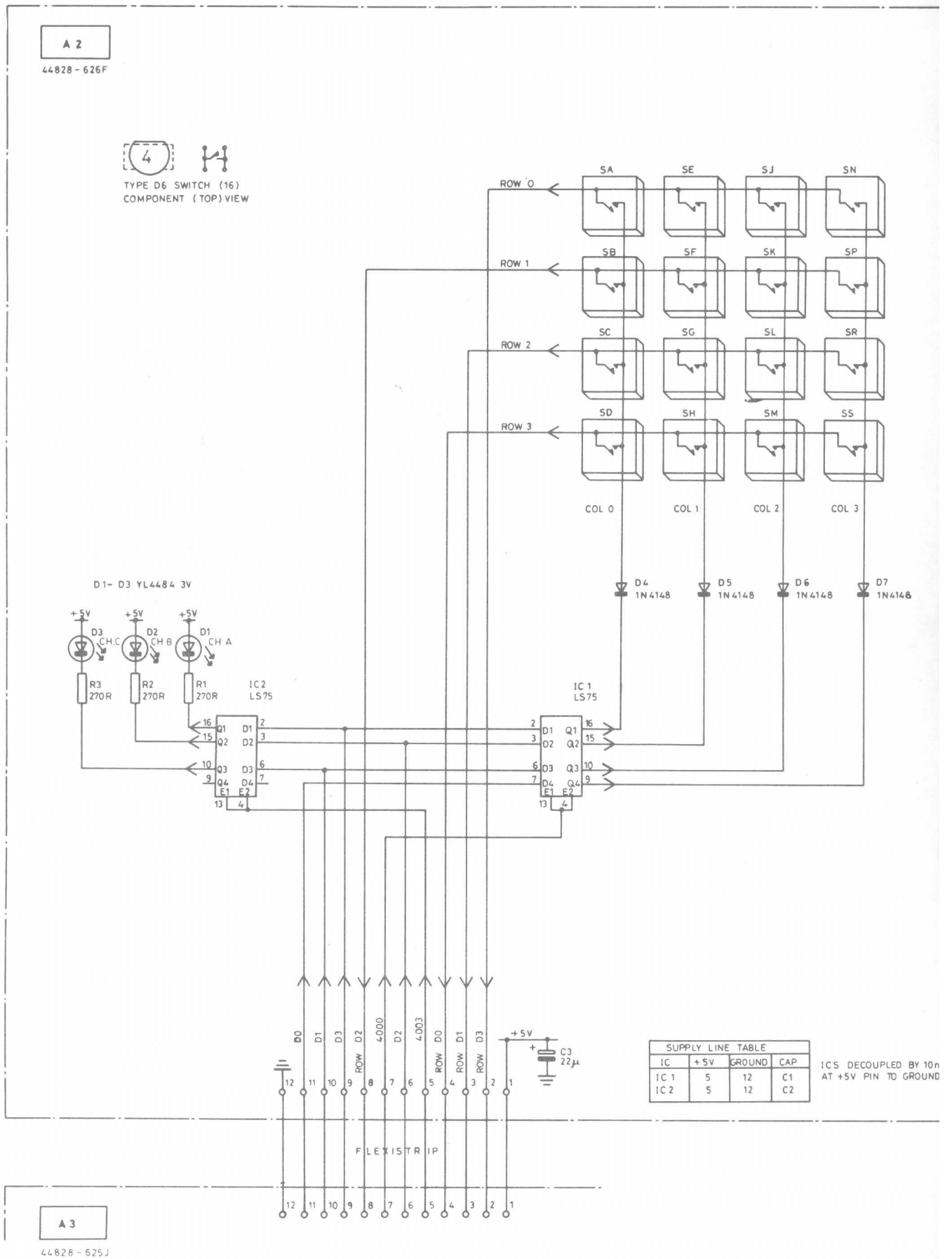
A2 Keyboard, p.c.b. layout



layout

Fig. 8

Jan. 85



SUPPLY LINE TABLE			
IC	+5V	GROUND	CAP
IC 1	5	12	C1
IC 2	5	12	C2

ICS DECOUPLED BY 10n
AT +5V PIN TO GROUND

Z44828-626F Iss. 3

A2 Keyboard, circuit diagr

Fig. 9

Jan. 85

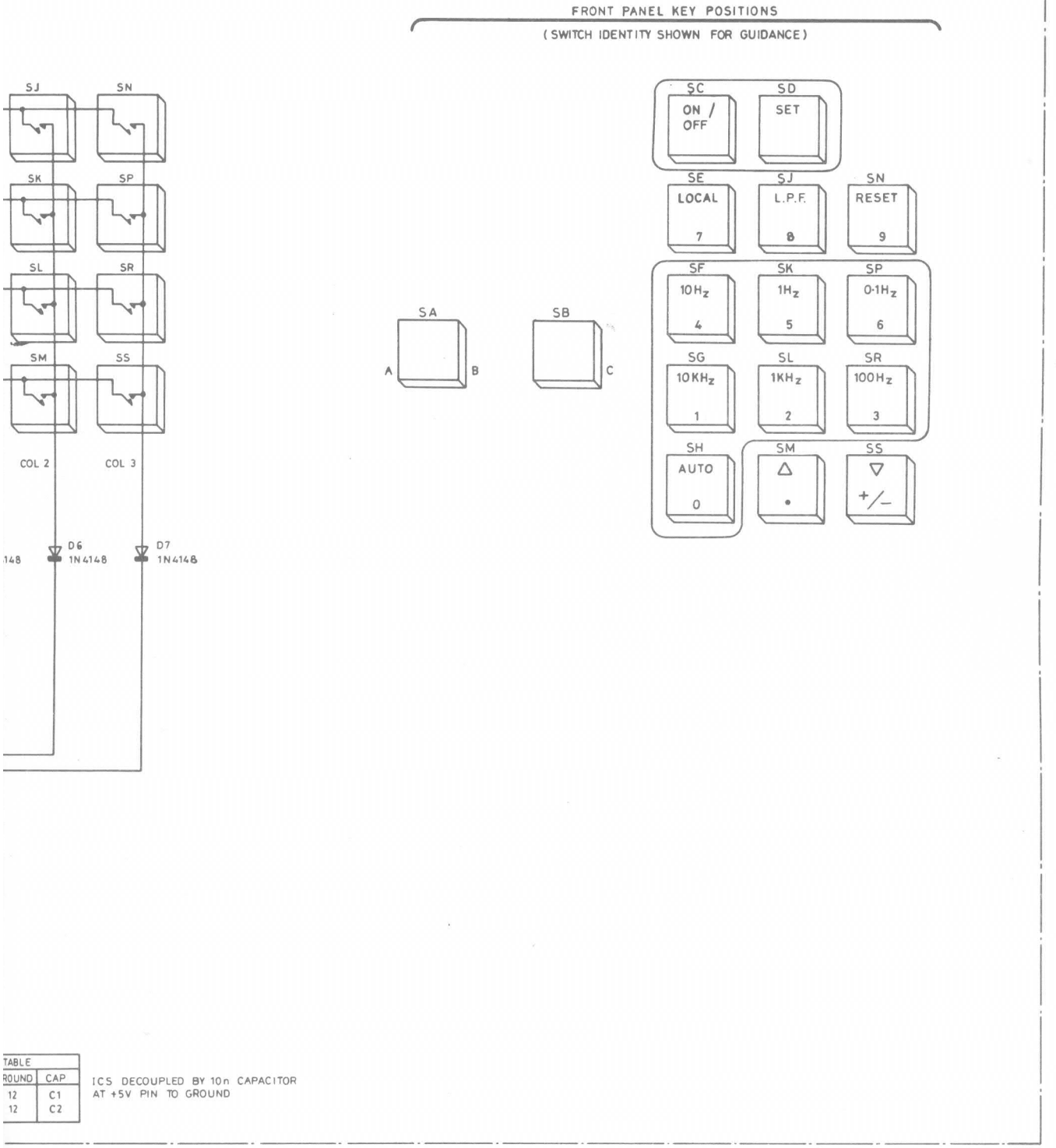
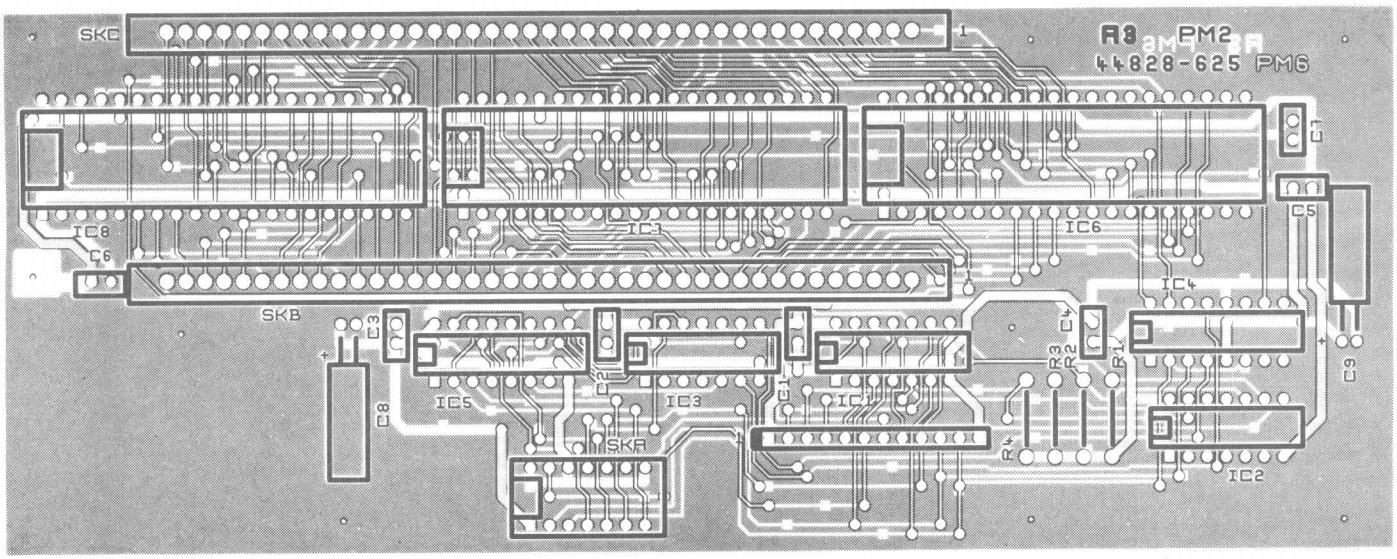


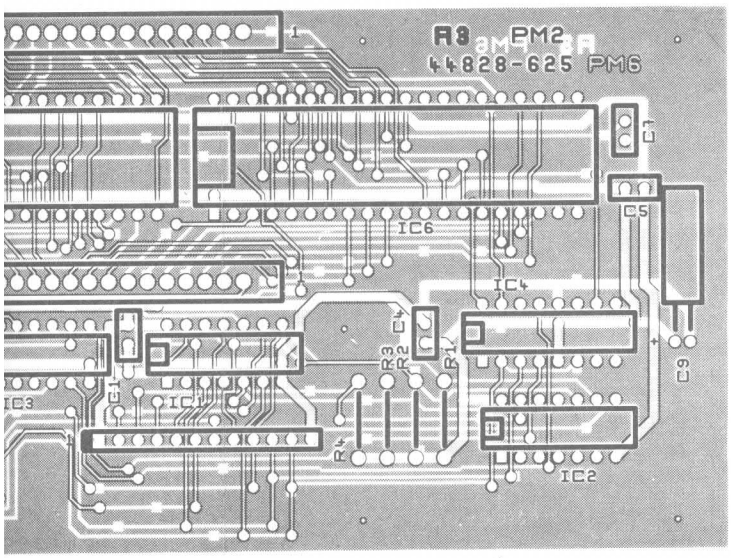
TABLE	
ROUND	CAP
12	C1
12	C2

ICS DECOUPLED BY 10n CAPACITOR AT +5V PIN TO GROUND

ɔard, circuit diagram



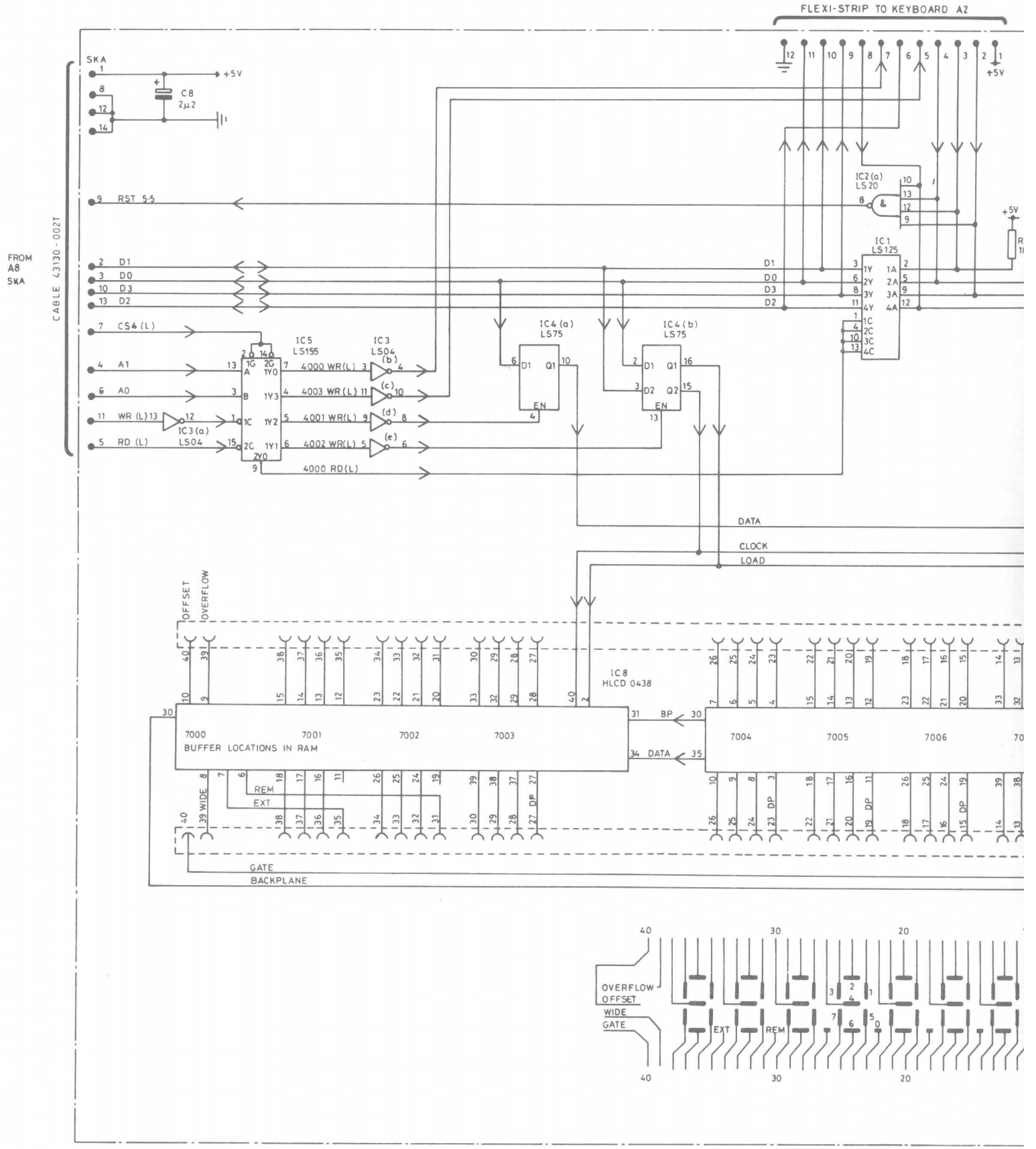
A3 Display board, p.c.b. layout



board, p.c.b. layout

Fig. 1

Jan. 8

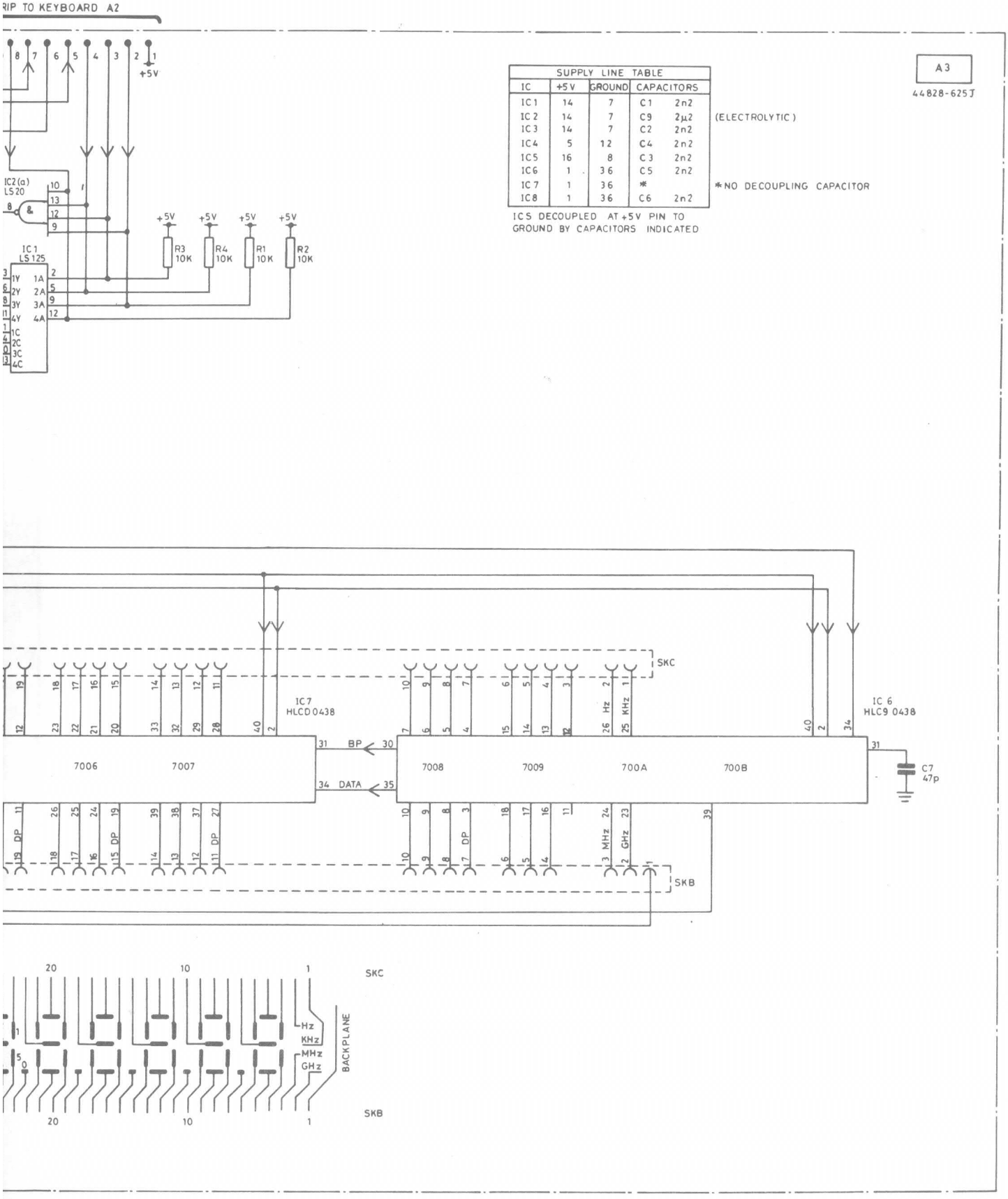


Z44828-625J Iss. 1

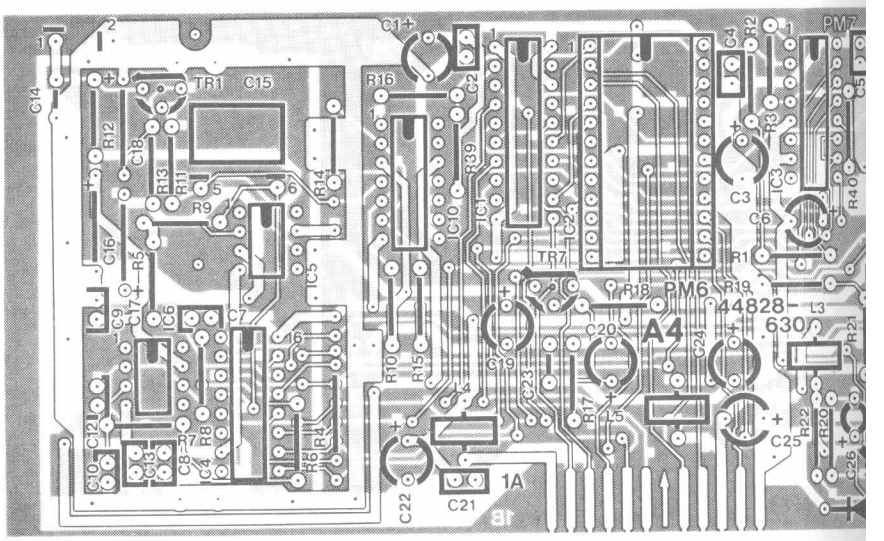
A3 Display board, circuit d

Fig. 11

Jan. 85



board, circuit diagram



A4 Loop control board, p.c.b

Fig. 12
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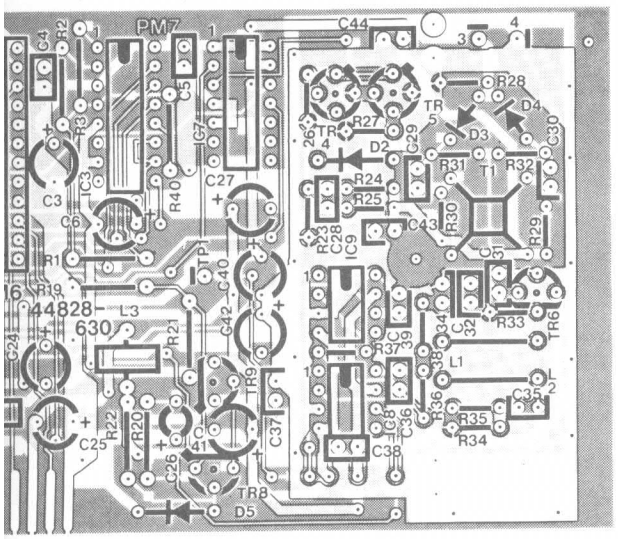


board, p.c.b. layout

Fig. 12

Jan. 85

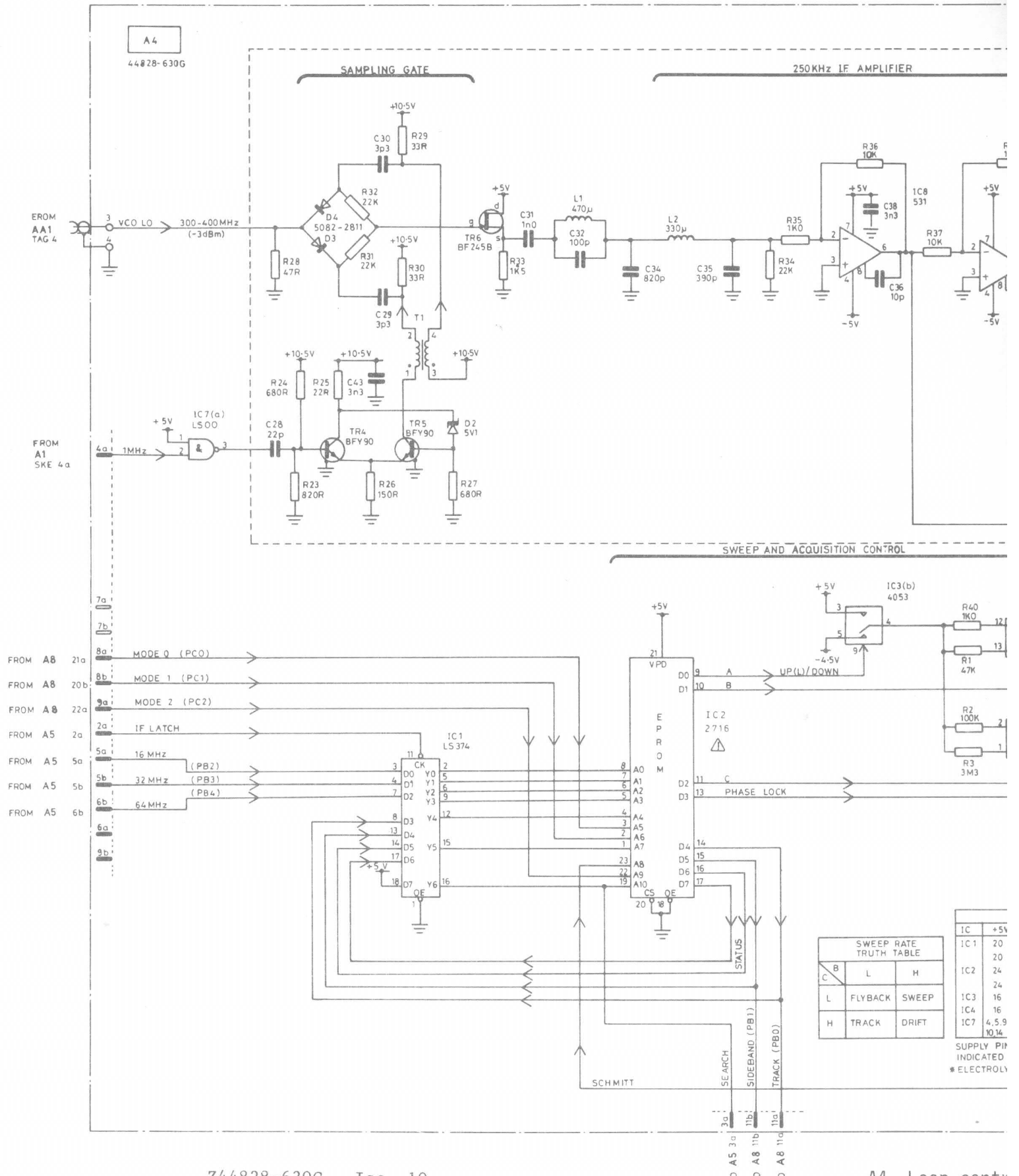
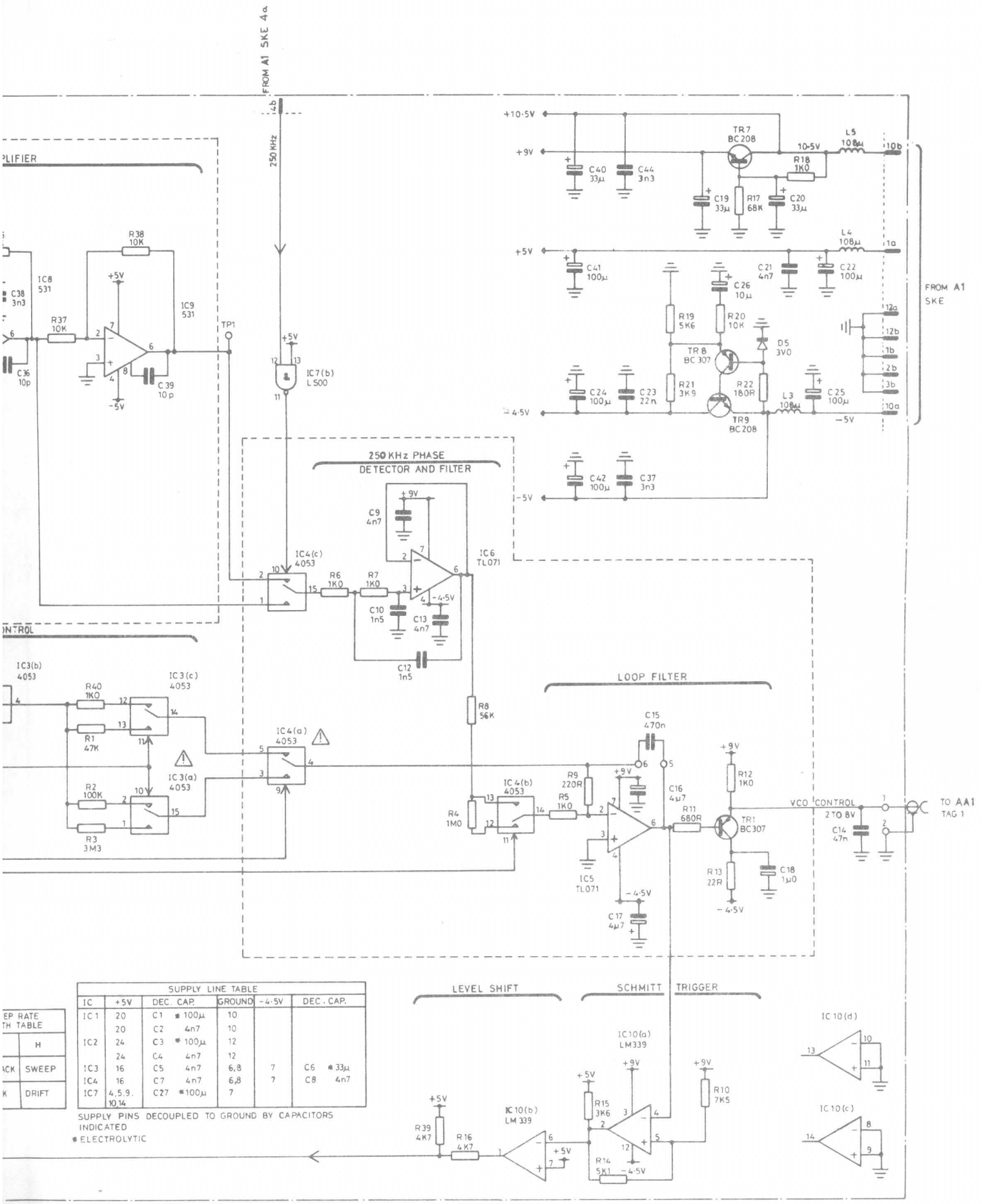


Fig. 13 Z44828-630G Iss. 10 A4 Loop contr

Jan. 85

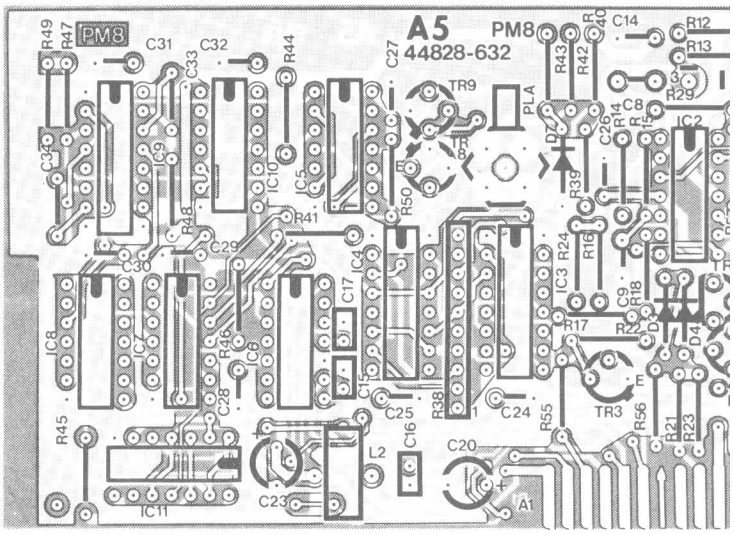


SUPPLY LINE TABLE						
IC	+5V	DEC. CAP.	GROUND	-4·5V	DEC. CAP.	
IC1	20	C1 * 100µ	10			
	20	C2 4n7	10			
IC2	24	C3 * 100µ	12			
	24	C4 4n7	12			
IC3	16	C5 4n7	6,8	7	C6 * 33µ	
IC4	16	C7 4n7	6,8	7	C8 4n7	
IC7	4,5,9, 10,14	C27 *100µ	7			

SUPPLY PINS DECOUPLED TO GROUND BY CAPACITORS INDICATED
* ELECTROLYTIC

EP RATE TH TABLE	
	H
ACK	SWEEP
K	DRIFT

A4 Loop control board, circuit diagram



A5 IF buffer board,

Fig. 14
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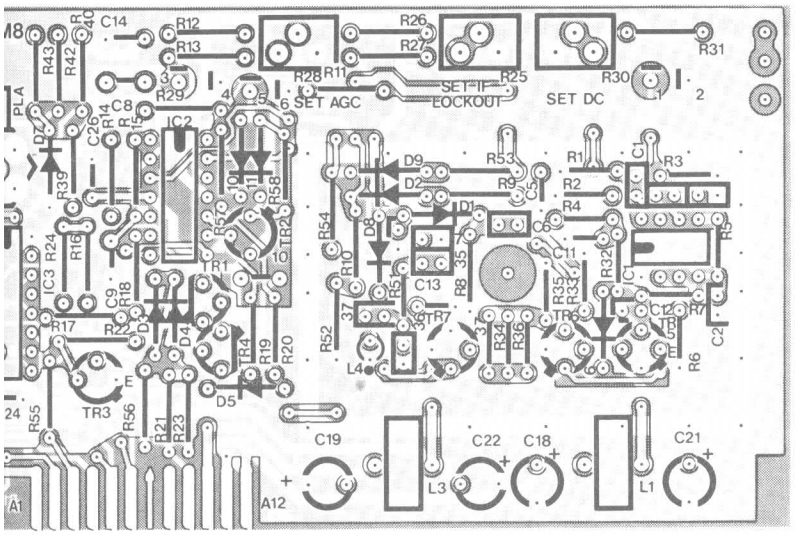
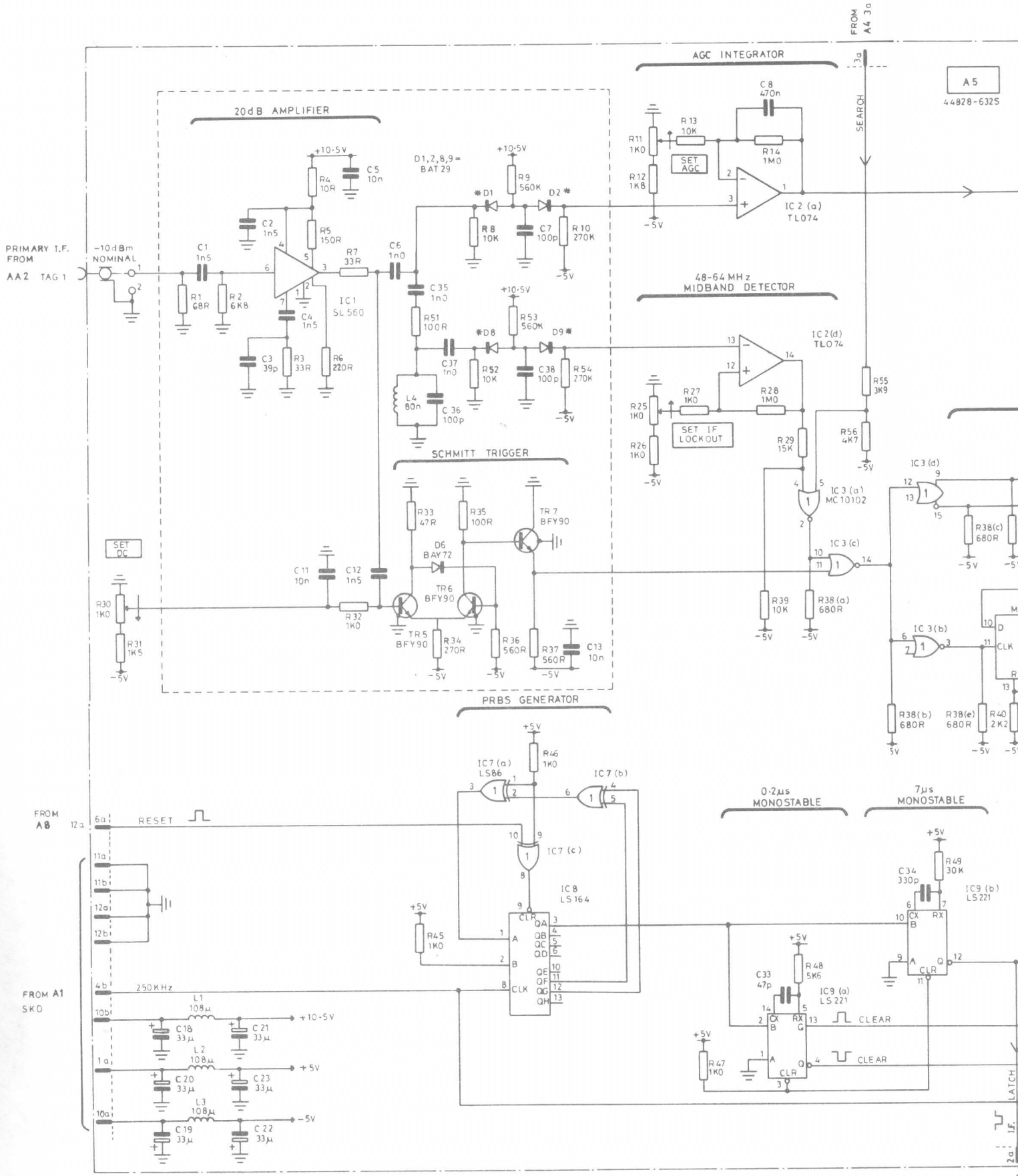


buffer board, p.c.b. layout

Fig. 1

Jan. 8

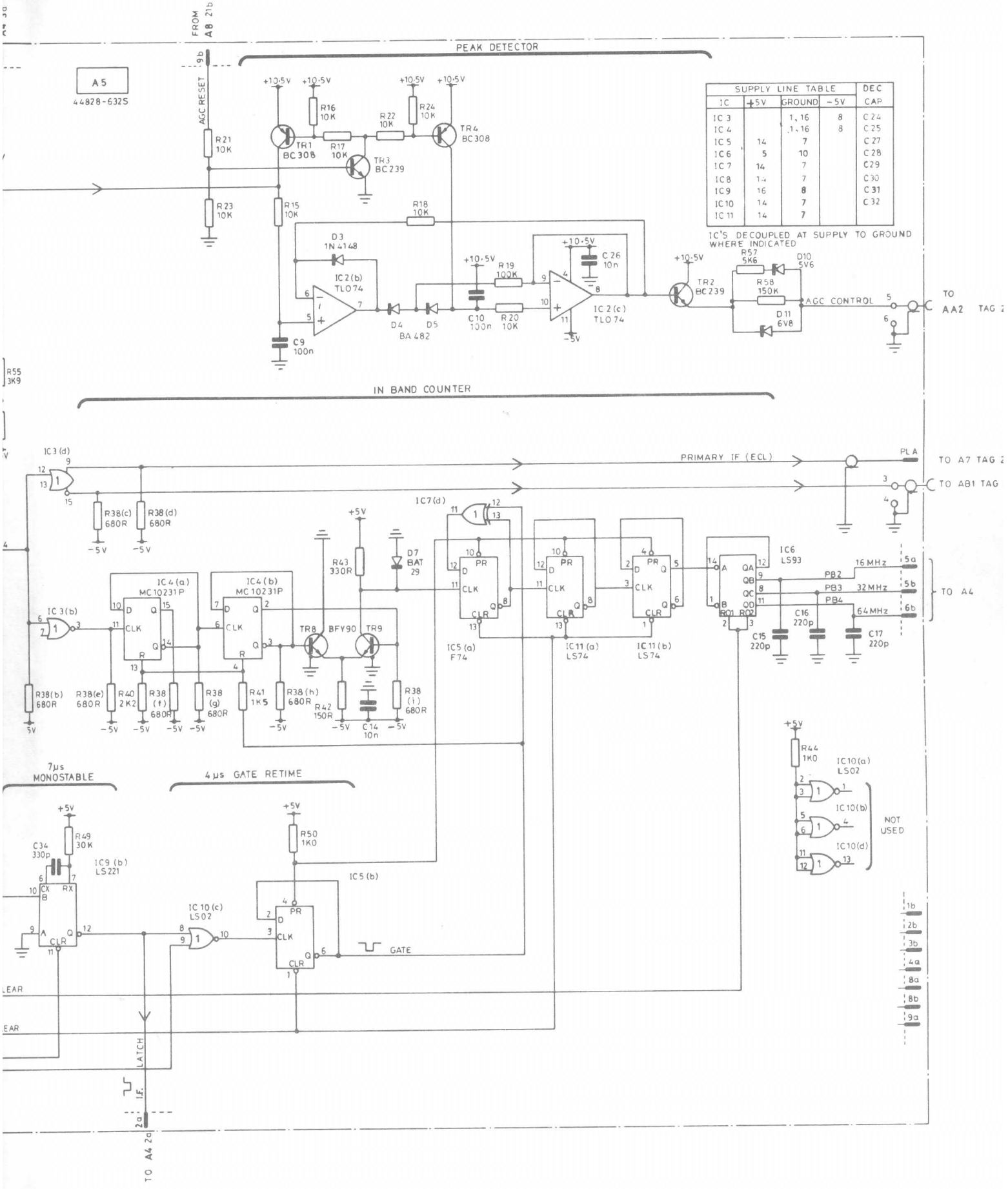


Z44828-632S Iss. 6

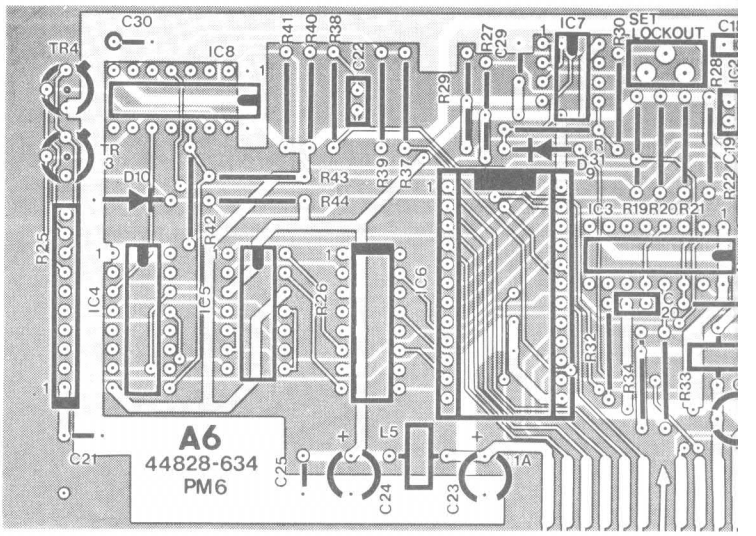
A5 IF buffer board, ci

Fig. 15

Jan. 85



ffer board, circuit diagram



A6 High frequency counter un

Fig. 16
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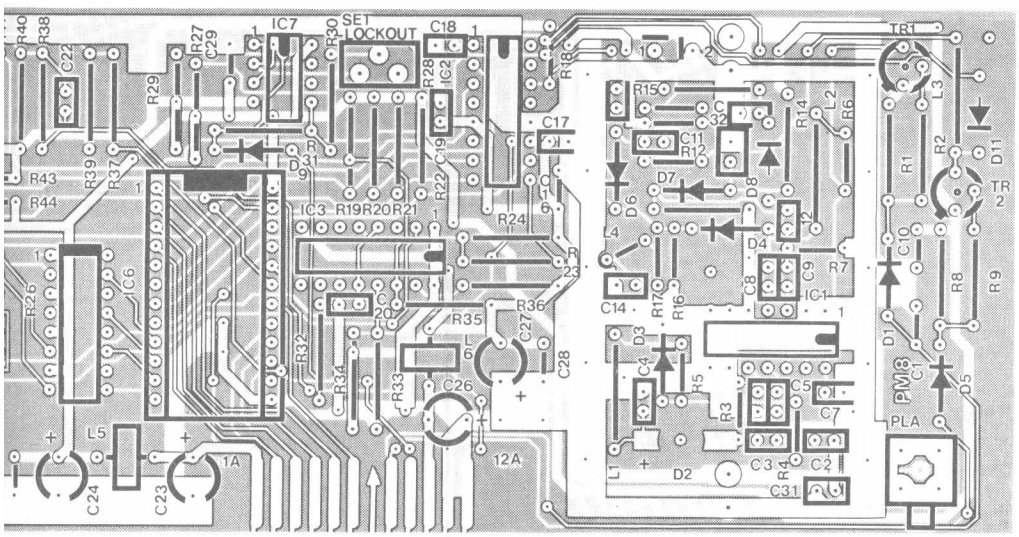
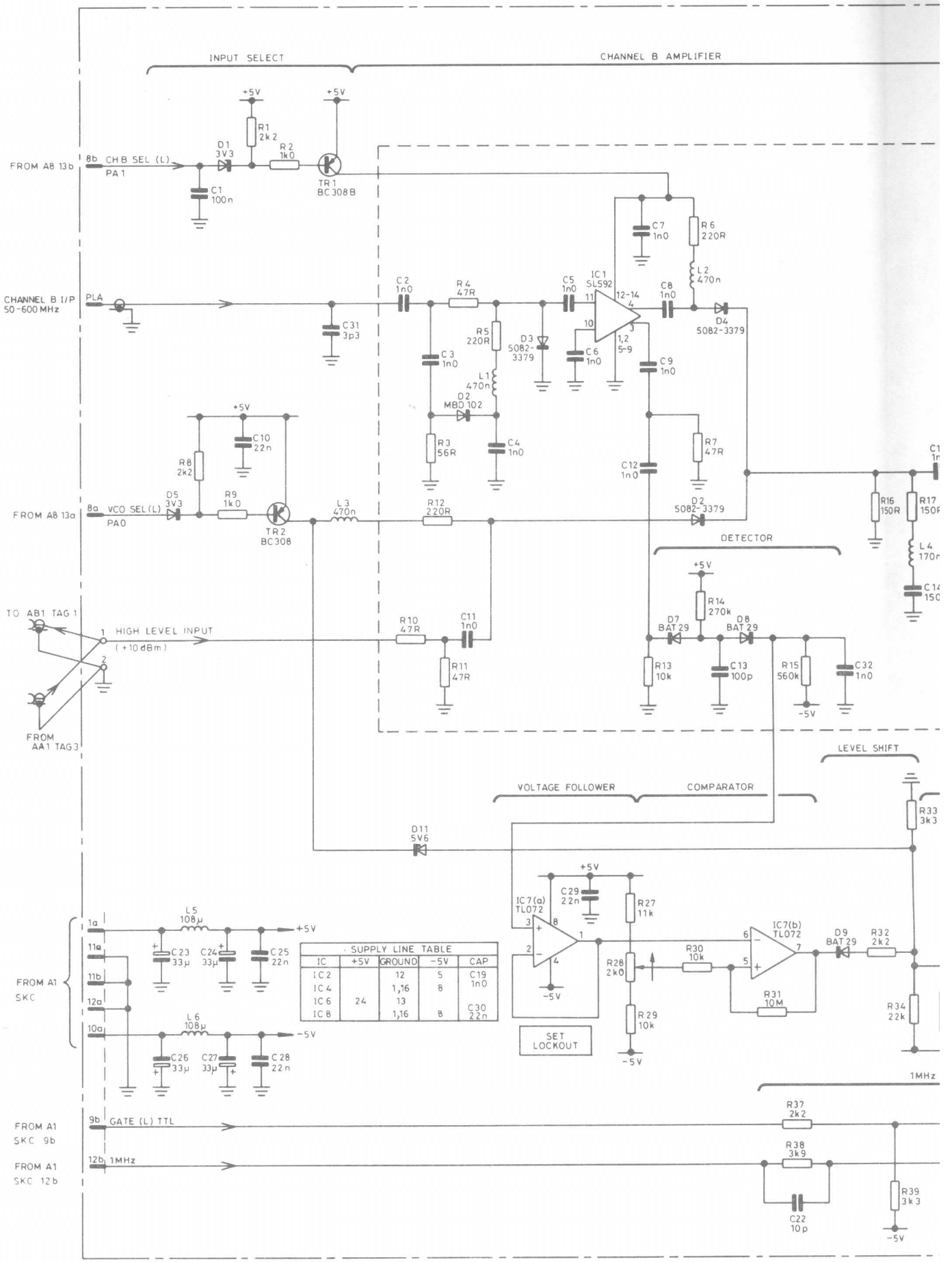


A6 High frequency counter unit, p.c.b. layout

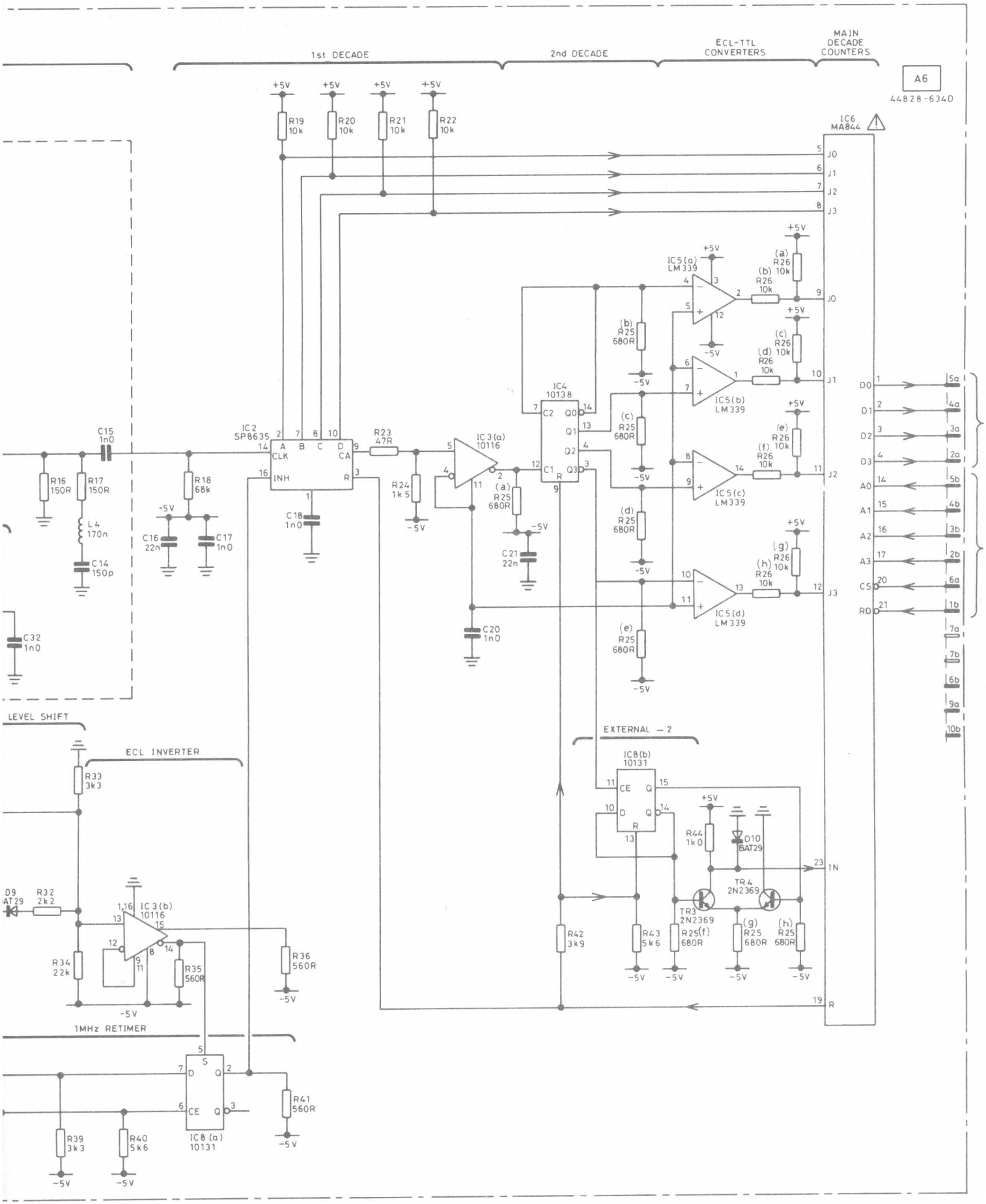


Z44828-634D Iss. 8

A6 High frequency

Fig. 17

Jan. 85



frequency counter unit, circuit diagram

Fig.
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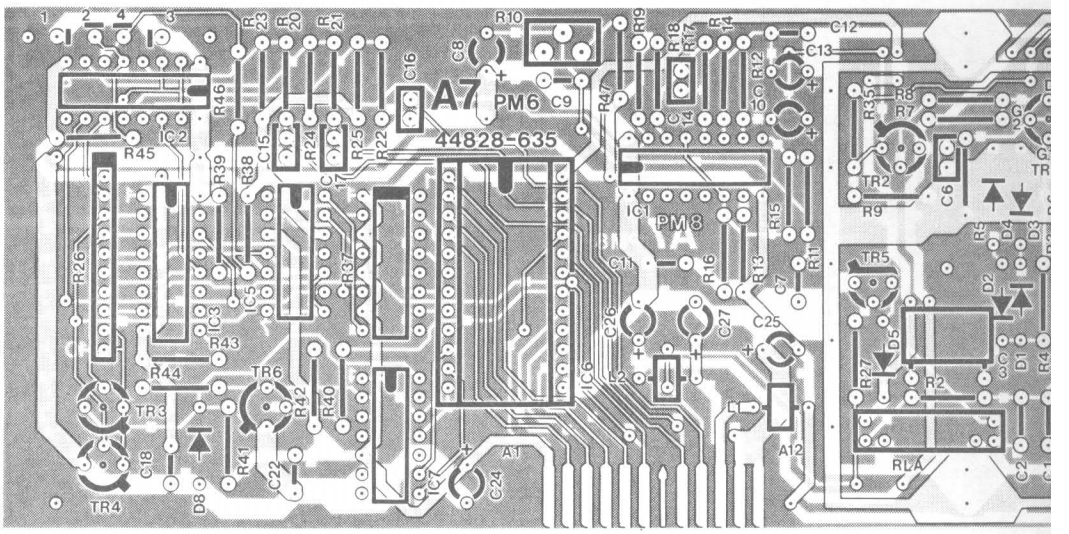
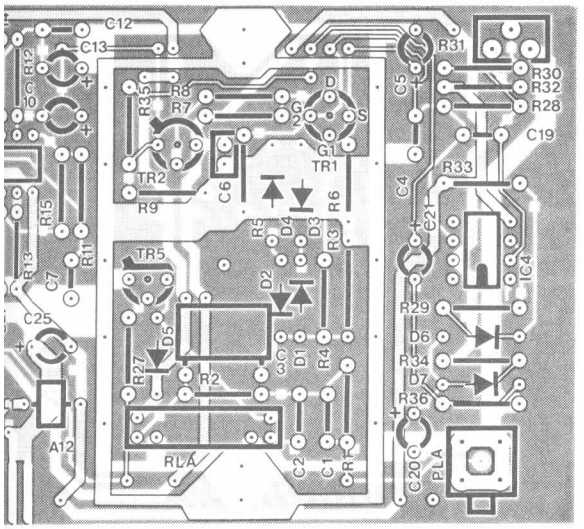
Page



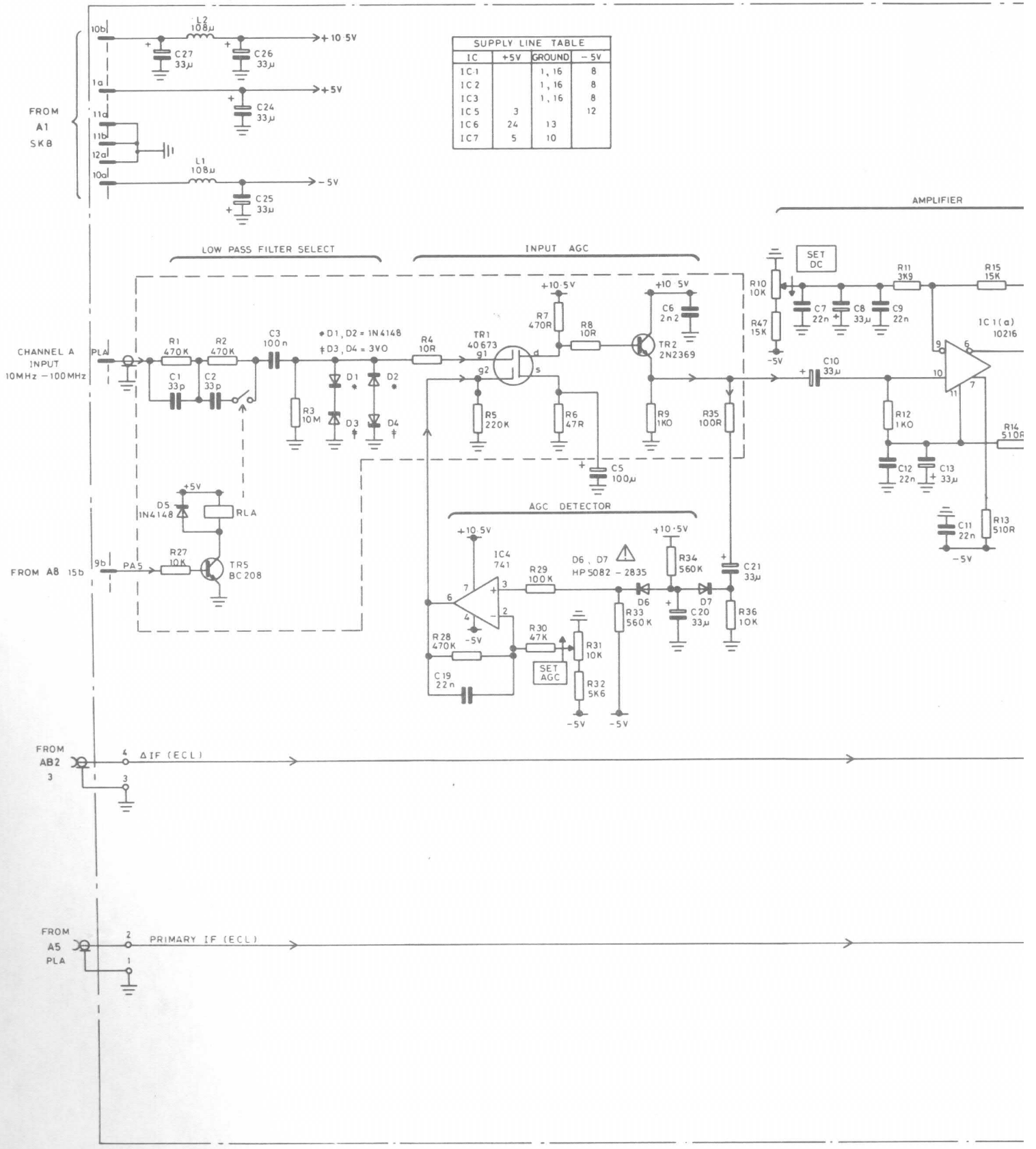
A7 Low frequency counter unit, p.c.b. layout



r unit, p.c.b. layout

Fig. 18

Jan. 85

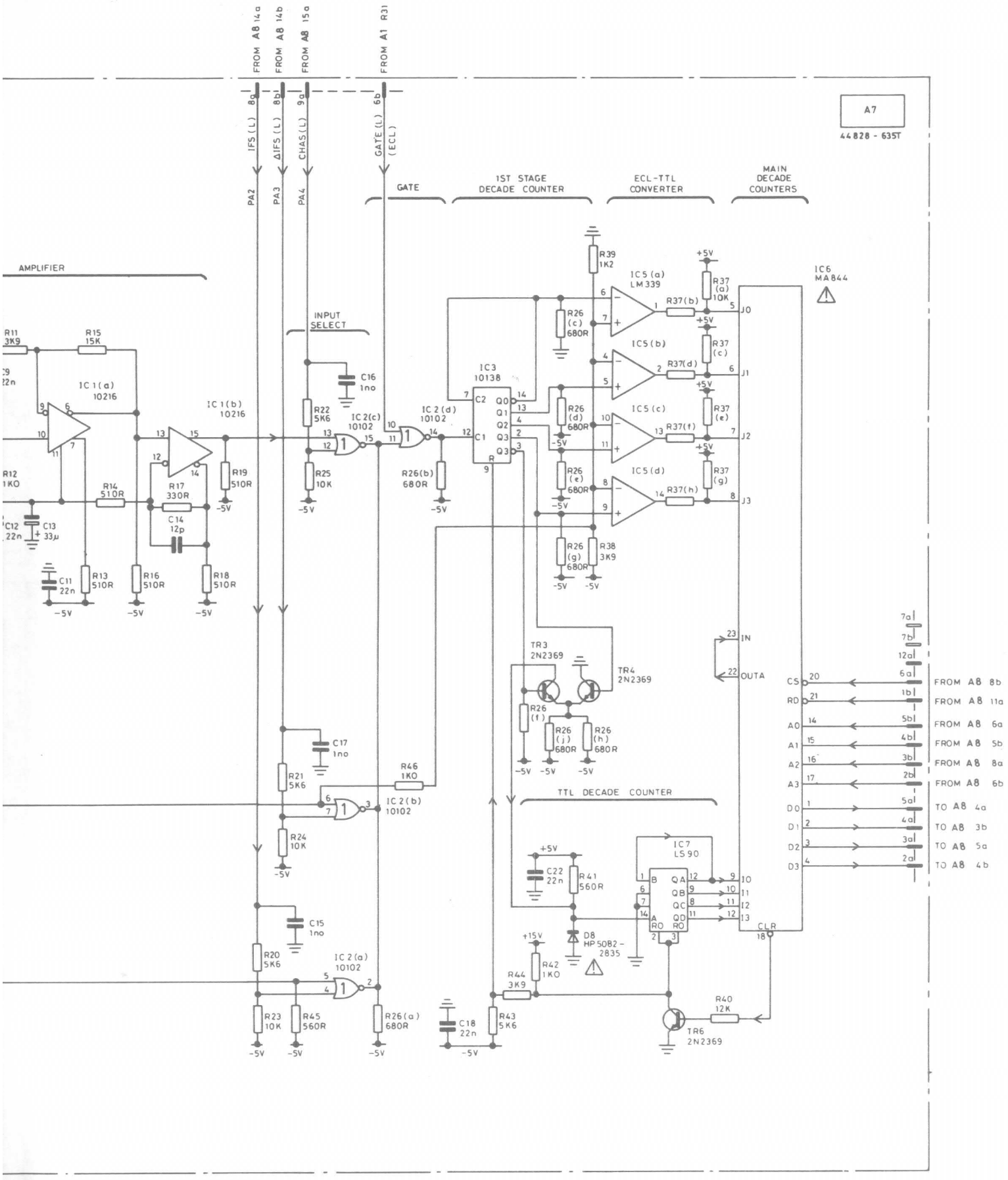


Z44828-635T Iss. 9

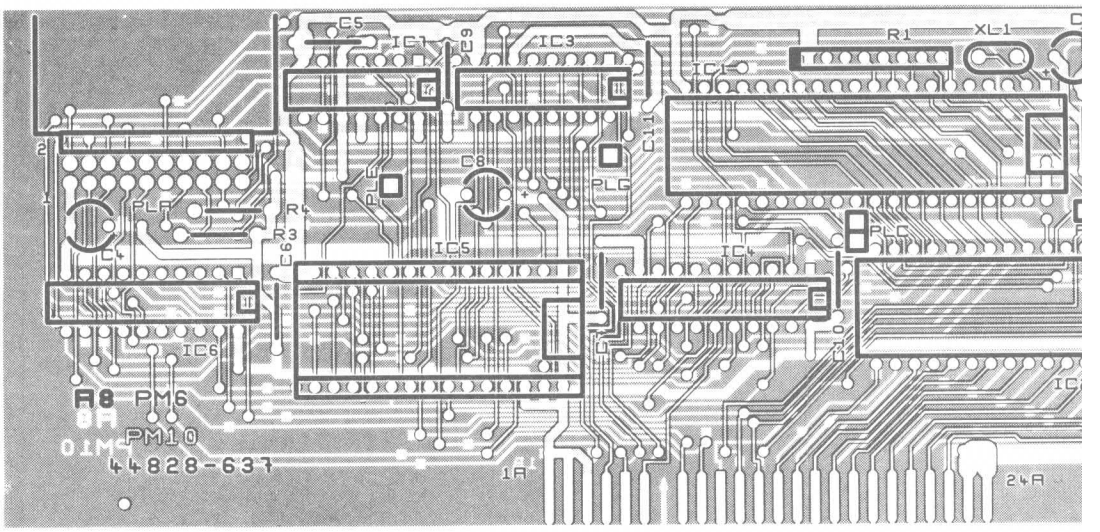
A7 Low frequency counter u

Fig. 19

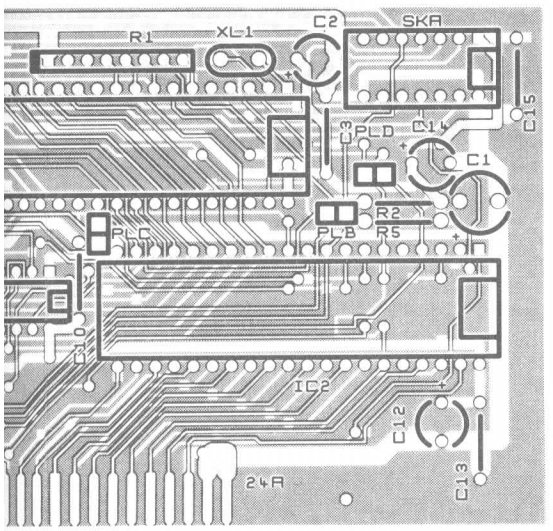
Jan. 85



cy counter unit, circuit diagram



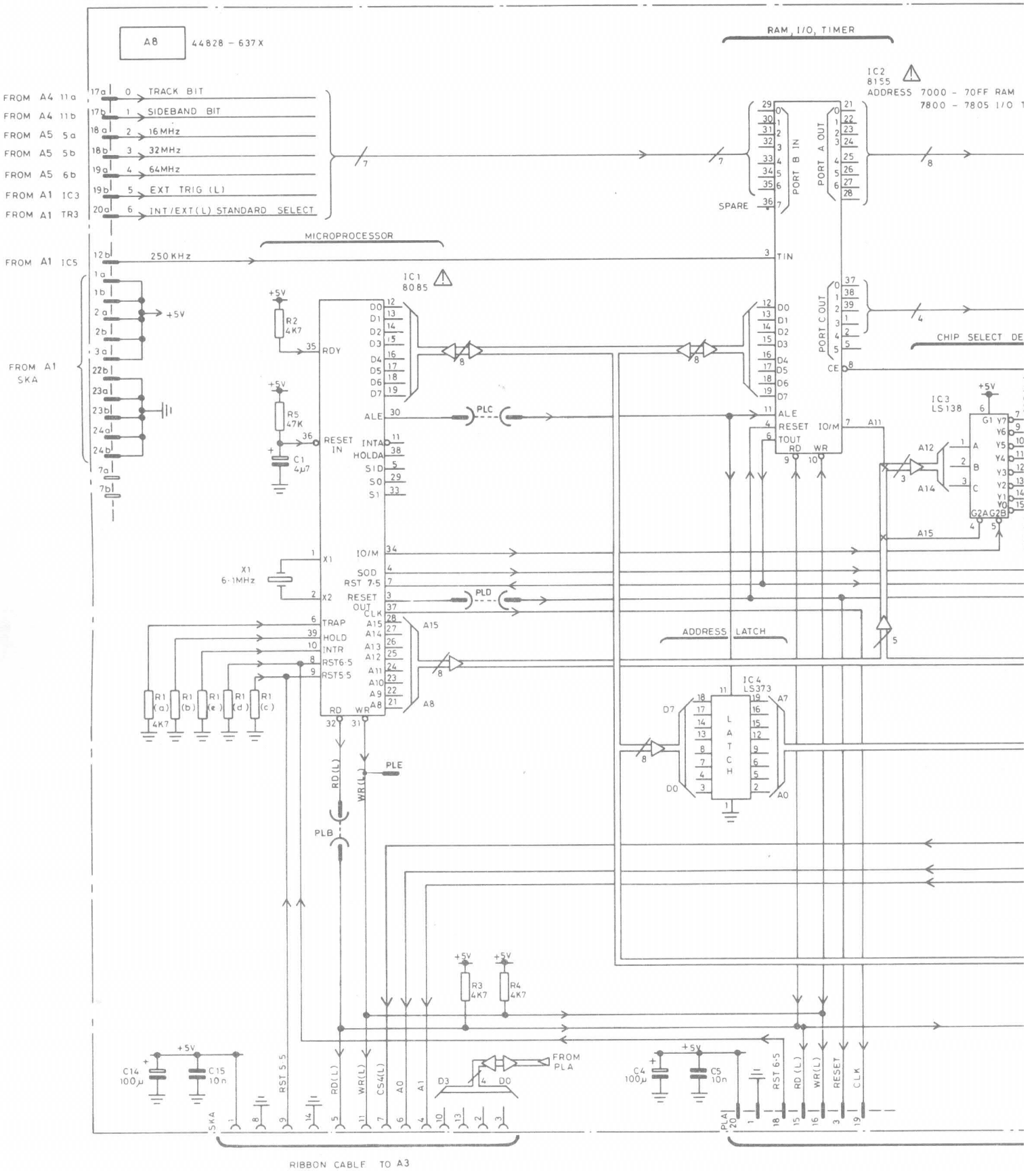
A8 Microprocessor board, p.c.b. layout



, p.c.b. layout

Fig. 20

Jan. 85

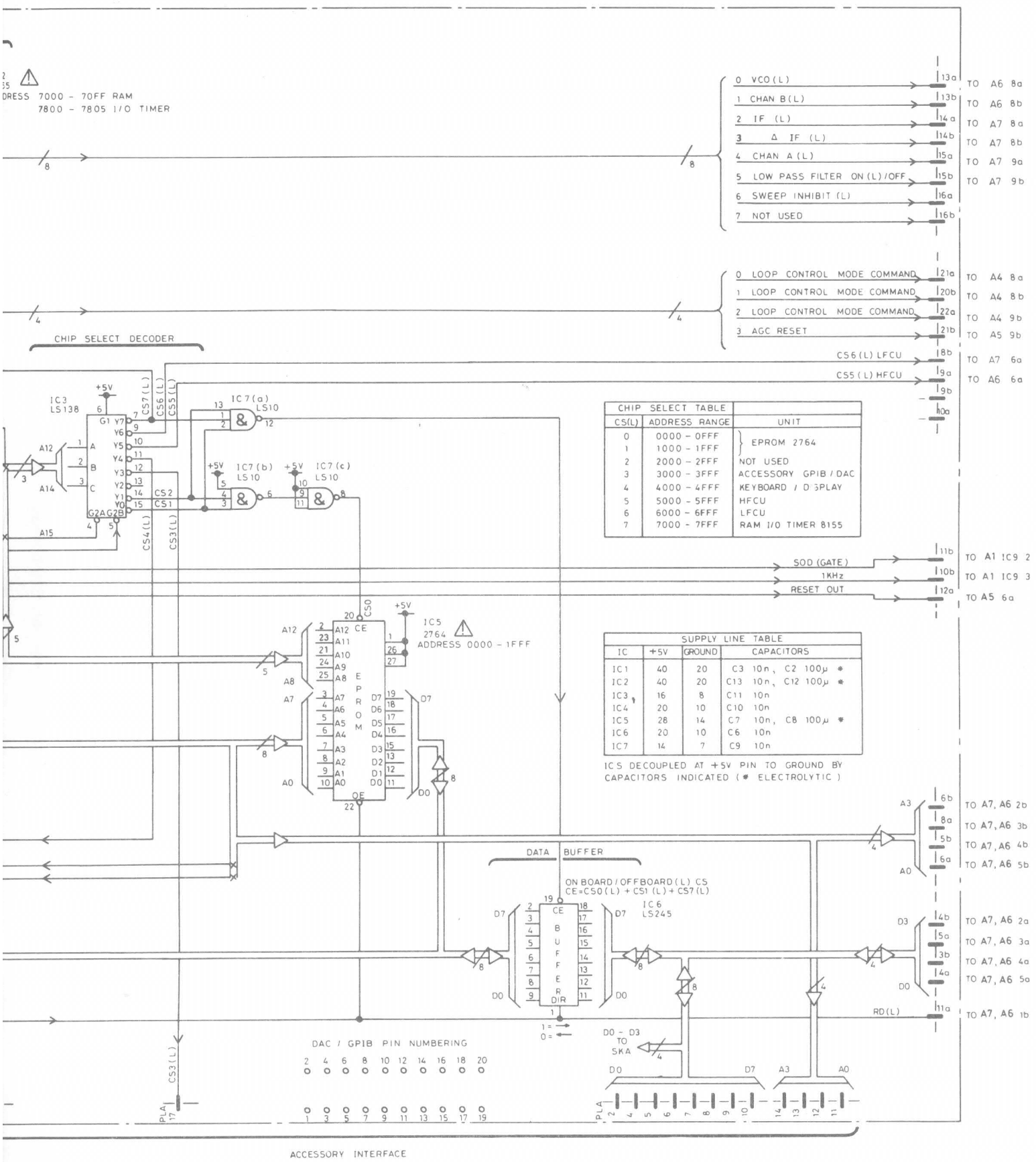


Z44828-637X Iss. 5

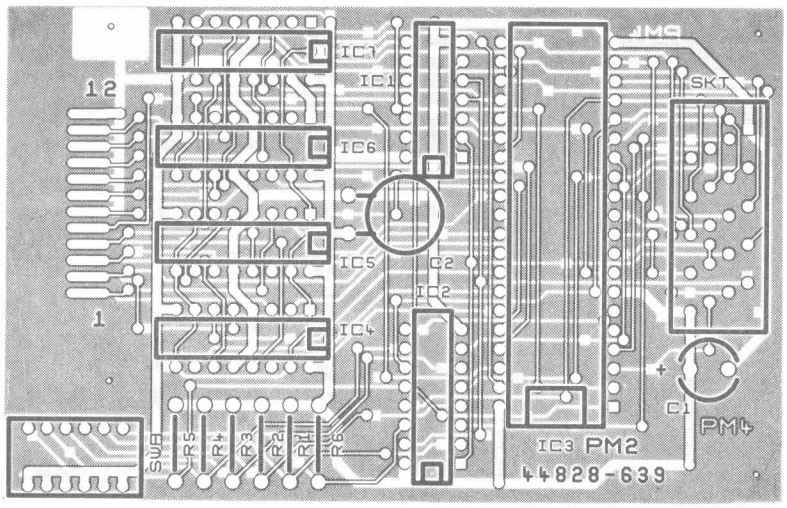
A8 Microprocessor board

Fig. 21

Jan. 85



rocessor board, circuit diagram



ACO GPIB board, p.c.b. layout

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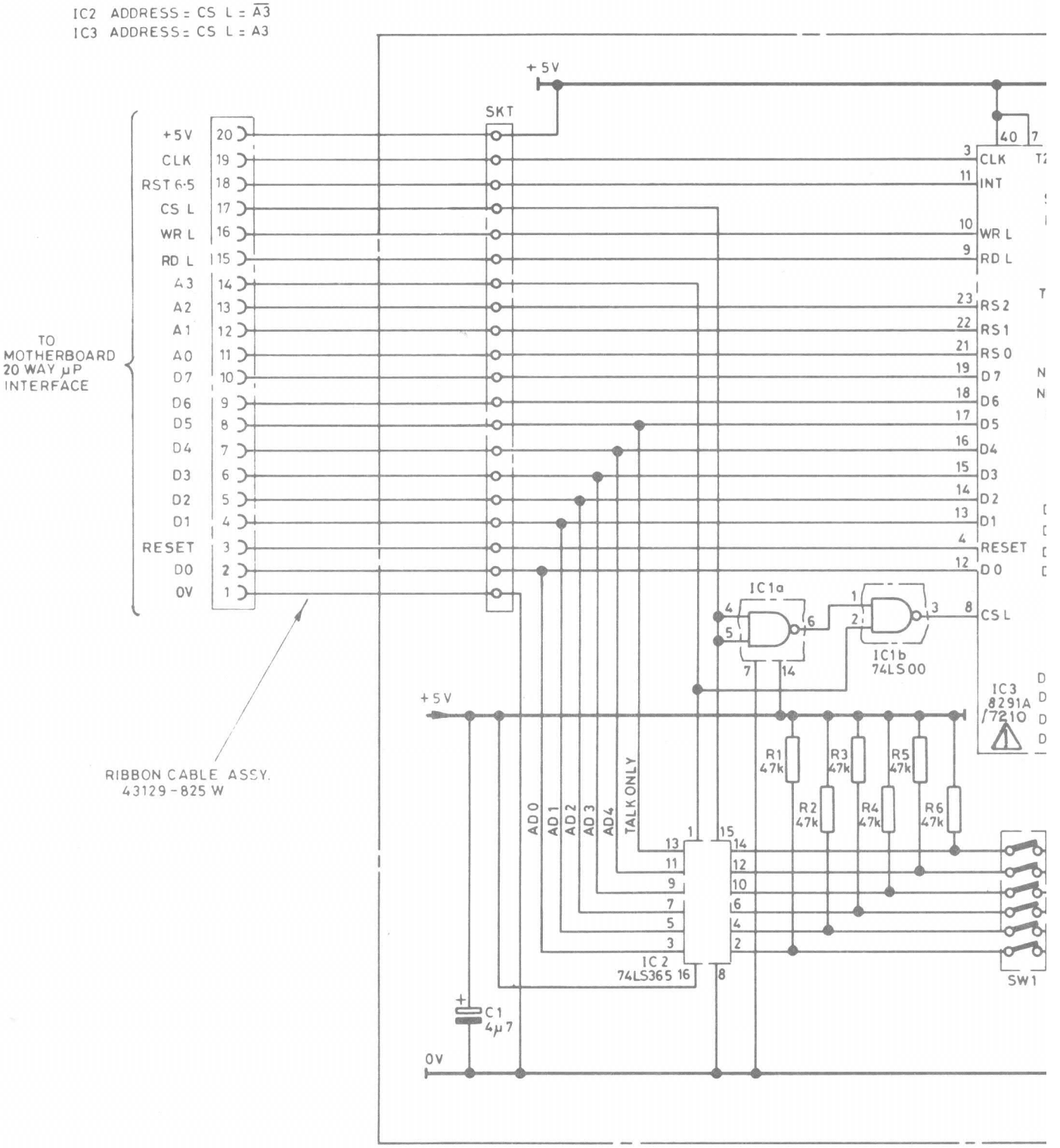
IC2 ADDRESS = CS L = $\overline{A3}$
IC3 ADDRESS = CS L = A3
TO MOTHERBOARD 20 WAY µP INTERFACE
+5V
CLK
RST 6·5
CS L
WR L
RD L
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
RESET
D0
0V
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
SKT
RIBBON CABLE ASSY. 43129-825 W
IC1a
IC1b 74LS00
IC3 8291A /7210
CS L
RESET
D0
D1
D2
D3
D4
D5
D6
D7
INT
WR L
RD L
CLK
RS2
RS1
RS0
R1 47k
R2 47k
R3 47k
R4 47k
R5 47k
R6 47k
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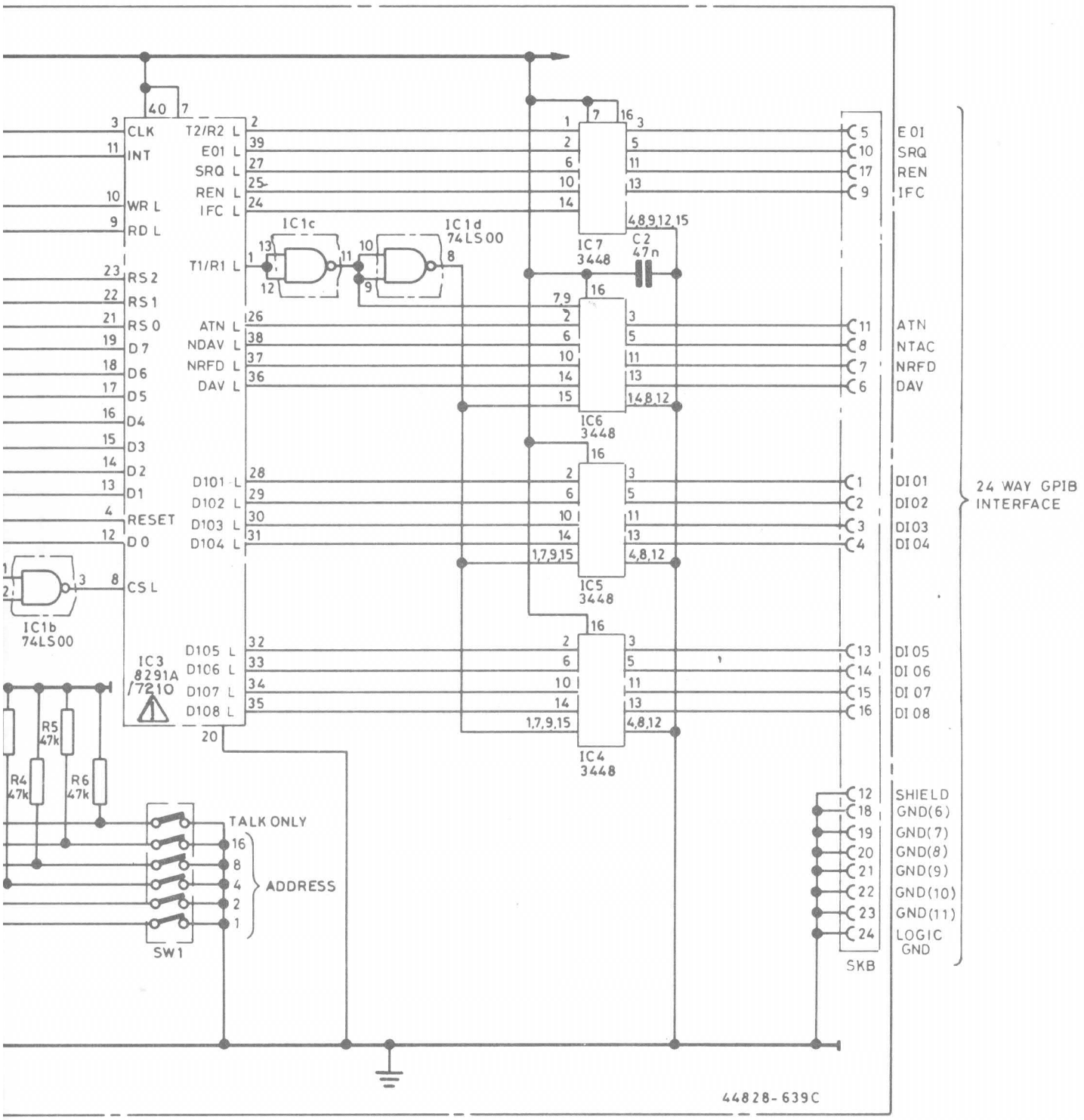
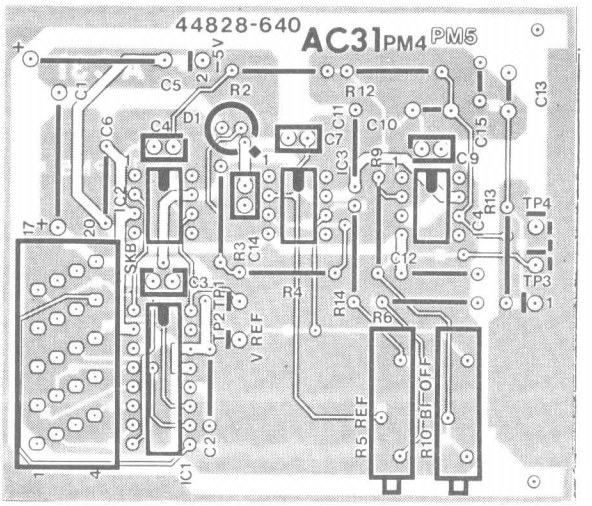
AD3
AD4
TALK ONLY
IC2 74LS365 16
SW1
C1 4µ7



GPIB unit, circuit diagram



AC31 D to A converter board, p.c.b. layout

Fig. 24
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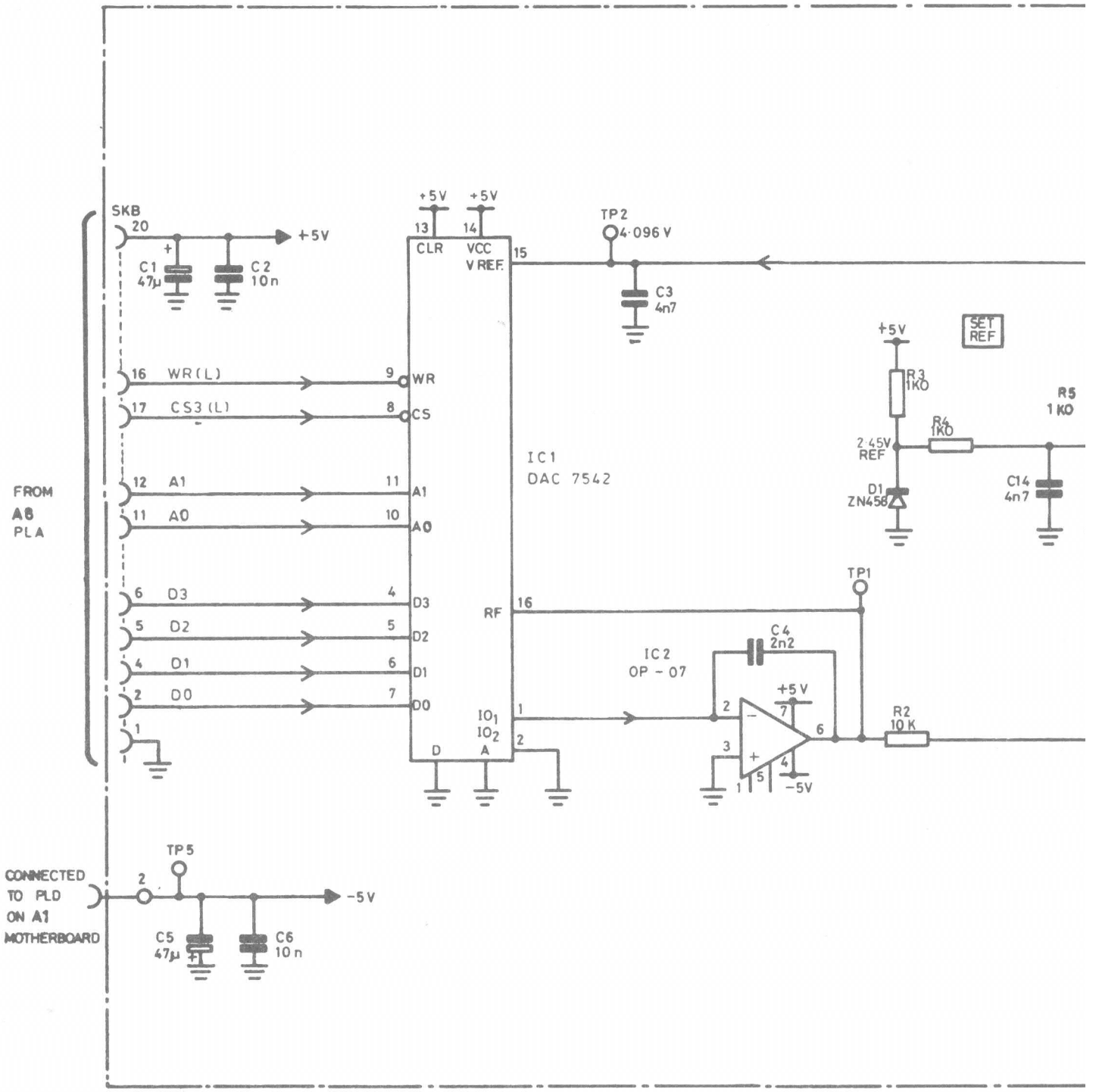
Jan. 85

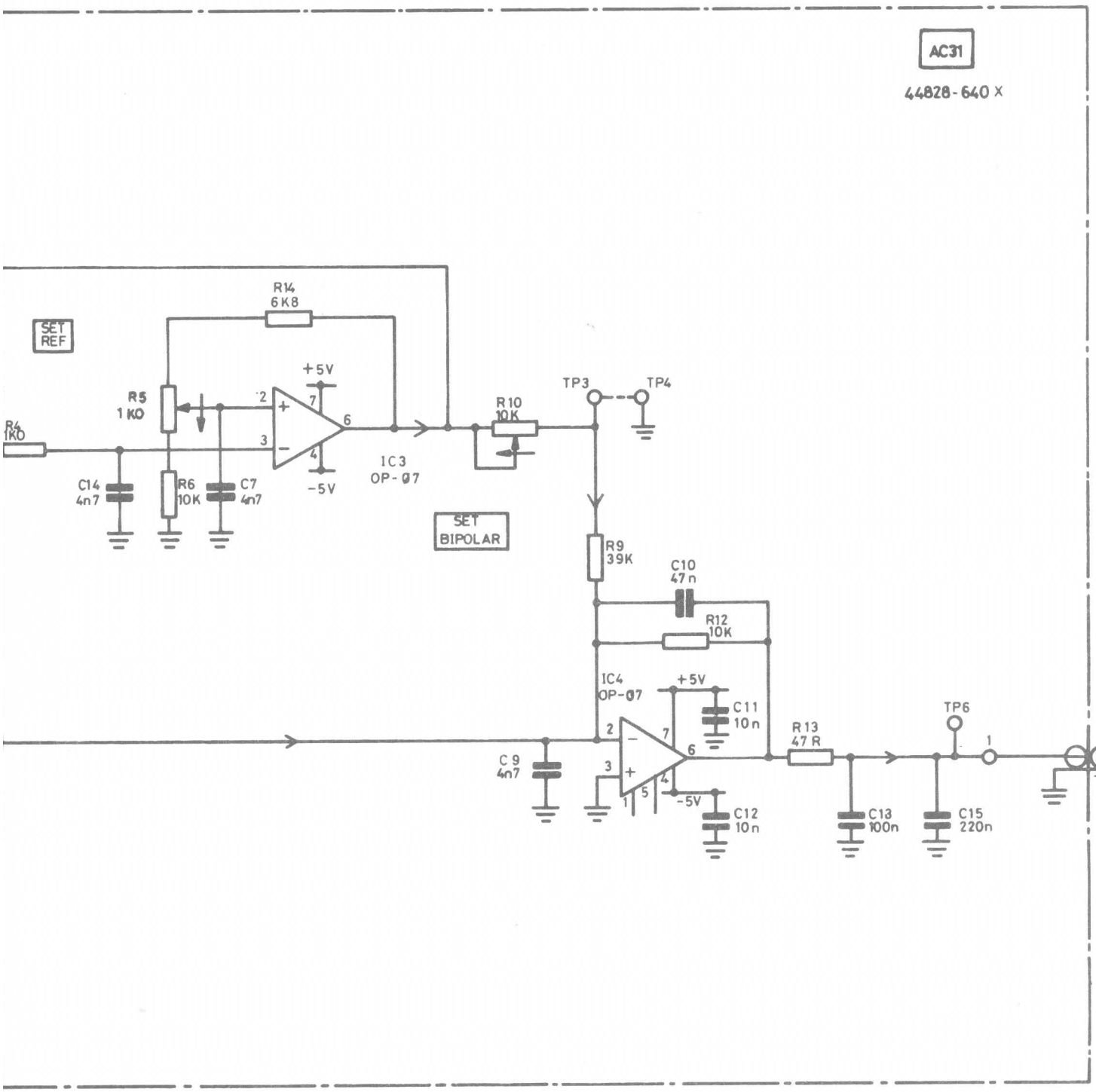


Z44828-640X Iss. 3

AC31 D to A converter bo

Fig. 25

Jan. 85



converter board, circuit diagram

Fig. 2
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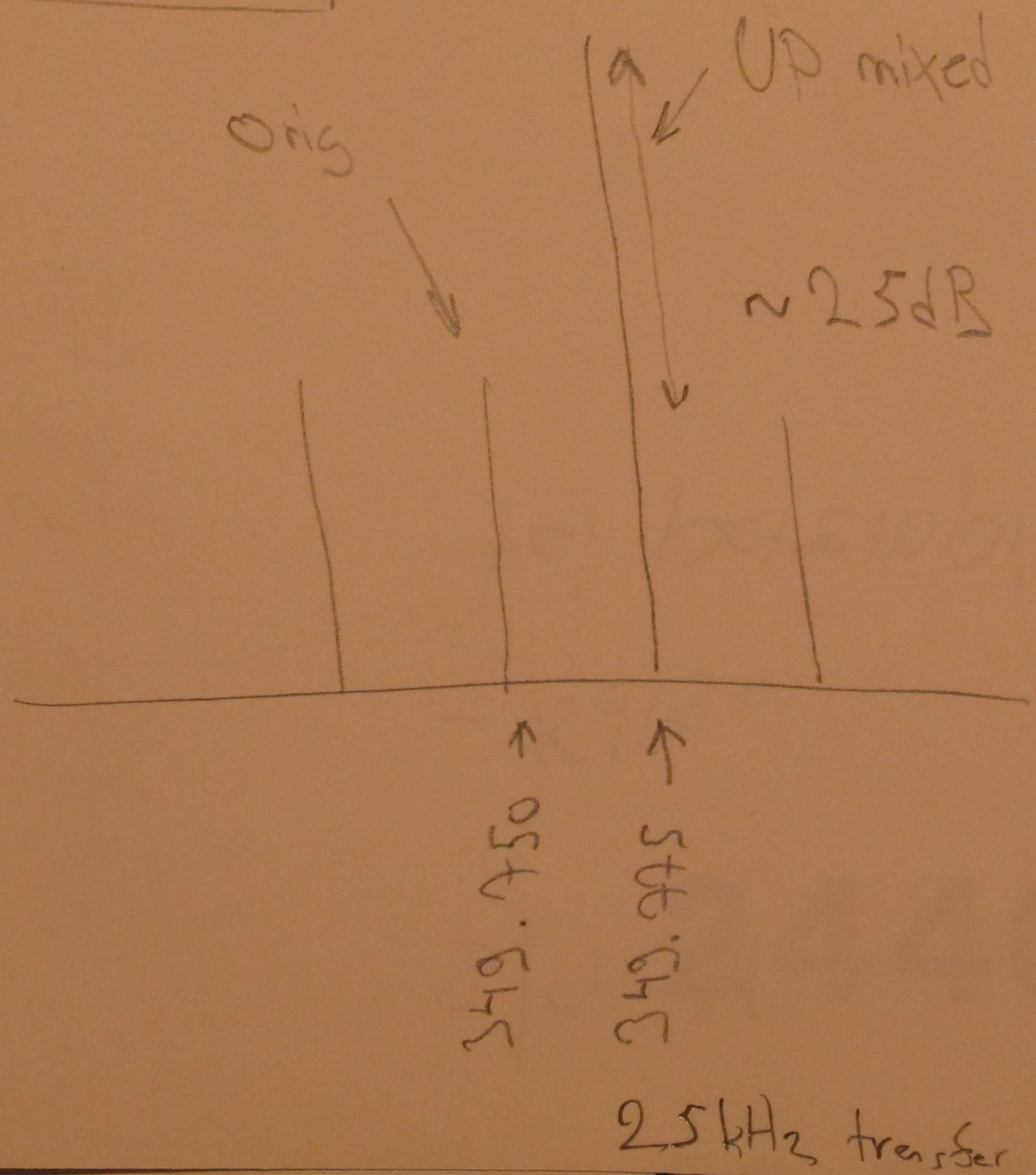
1000MHz in



20 GHz