Marconi
Instruments

2833A

Digital Line Monitor

Instruction Manual

DIGITAL LINE MONITOR 2833A

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CONTENTS

PRELIMINARIES

CHAPTERS

HAZARD WARNING SYMBOLS

The following symbols appear on the equipment.

Symbol	*Type of hazard*	*Reference in manual*
	Static sensitive device	Page (iv), Chap. 7, page 2
	Risk of electric shock	Page (iii)

Note...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ► ..... ◄ to show the extent of the change. When a chapter is reissued the triangles do not appear.

Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers 

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be discharged; to discharge mains filter capacitors, if fitted, short together the L (live) and N (neutral) pins of the mains plug.

Mains plug 

The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Fuses

BT versions. Note that the supply fuse is connected in series with the brown (live) wire of the supply lead. If the equipment is connected to the supply via a two-pin plug, it will be possible for the fuse to become connected to the neutral side depending upon the orientation of the plug in its socket. In these circumstances certain parts of the instrument could remain at supply potential even after the fuse has ruptured.

Proprietary versions. Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol  on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange discs, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disc or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.

Metallic tools earthed either permanently or by repeated discharges.

A low-voltage earthed soldering iron.

An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

WARNING : TOXIC HAZARD

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

Chapter 1

GENERAL INFORMATION

CONTENTS

INTRODUCTION

1. The 2833A Digital Line Monitor is a combined p.c.m. error detector for 2048/8448 kbit/s systems and alignment and signalling monitor for 2048 kbit/s systems. The instrument provides in-service measurement and analysis of systems using HDB3 code format and has five measurement modes which are as follows:-

(i) HDB3 line-code error detector at 2048 kbit/s, (2M CODE).

(ii) HDB3 line-code error detector at 8448 kbit/s, (8M CODE).

(iii) Frame alignment monitor at 2048 kbit/s, (2M ALIGN).

(iv) Signalling code monitor at 2048 kbit/s, (2M SIG).

(v) Counter for an external input, (EXT. COUNT).

Fig. 1 Digital Line Monitor 2833A

Line-code error measurement (2M CODE and 8M CODE modes)

2. The p.c.m. bit stream is monitored and code violations of the HDB3 format are detected. The errors are either totalized and displayed on a six digit counter or displayed as an error ratio in the form of a mantissa and exponent from 0 in 10^7 to 1 in 10^1.

3. The totalization of errors continues when the mode is switched to error ratio, enabling error ratio to be measured without interfering with a long-term monitoring sequence. The totalizing count can be stopped then continued or reset. Count overflow is indicated by an LED.

4. A self-test facility, which provides an internally generated signal with a known error ratio, enables you to check for correct operation of the instrument. A lamp-test facility when selected will illuminate all LED's and displays.

Frame alignment error measurement (2M ALIGN mode)

5. The frame alignment signal in the 2048 kbit/s bit stream is monitored and errors are determined. The display of errors is similar to the line-code error measurement mode in that totalization and error ratio facilities can be switch selected and also totalization continues when error ratio is selected. Unused bits of the frame and multiframe alignment words can be accessed via a socket on the rear panel.

Channel signalling monitor (2M SIG mode)

6. It is possible to monitor Time-Slot 16 of a selected channel whereby the 4-bit signalling code, either present or previous, may be displayed as a decimal equivalent. In this configuration the last number dialled may also be displayed.

Alarm state indication (2M ALIGN and 2M SIG modes)

7. LED lamps illuminate corresponding with the following error conditions listed in order of priority : Line, AIS, Frame, Errors (Frame word), Multiframe, Distant Frame, Distant Multiframe. If more than one error condition occurs simultaneously, only the highest priority lamp is lit. The lamps can be self extinguishing following clearance of the error, or can be set to remain lit by selecting a lamp lock facility.

External count input (EXT. COUNT mode)

8. An external count input connector on the rear panel may be used to totalize error pulses from a multiplex alarm monitor point.

Error Free Seconds mode (EFS)

9. When the 2833A is switched on it automatically monitors the input signal for code or frame word errors. When EFS is selected - via a front panel key sequence - the number of complete seconds in which no errors occurred in the period since the 2833A was switched on, mode changed or RESET, is presented as a percentage of the total number of seconds in that period. EFS is displayed if ERRORS-RATIO is selected and printed if a printer is connected.

Printer output

10. The 2833A can be connected to a printer to record events and measurement results applicable to the mode selected. Up to four 2833A's can be connected to one printer at the same time via a commercially available printer or modem sharing unit. Two instruments sharing one printer would be useful for separate monitoring of transmit and receive paths of digital links. Instrument identity is switch selectable and is printed with each print event. Alternatively the printer output can be connected directly to a modem for remote monitoring.

64 kbit/s co-directional output (2M ALIGN and 2M SIG modes)

11. Any channel time-slot from 0 to 31 can be selected and the information present in the time-slot is accessed via rear panel output sockets as a 64 kbit/s co-directional signal (CCITT Rec. G732). This signal provides an interface for associated test equipment.

Alarm detector output (2M ALIGN and 2M SIG modes)

12. A t.t.l. signal is produced when an alarm is detected in the 2M ALIGN or 2M SIG modes. This can be used in conjunction with Digital Simulator 2828A to test receive multiplex frame alignment sequences. This output is available via a terminal on the rear panel.

Miscellaneous outputs

13. The following outputs are available via a 15-way D-type connector on the rear panel.

Pen recorder (All modes)

14. An output for a current drive pen recorder enabling long-term monitoring of signal alarms and error conditions.

Errors (2MALIGN and 2M SIG modes)

15. A pulse output coincident with a Frame Alignment Word error or signalling code error for use as an external count drive or trigger source for an oscilloscope.

64 kbit/s sync. (2M ALIGN and 2M SIG modes)

16. A synchronizing pulse output for an oscilloscope monitoring data from the 64 kbit/s output.

Unassigned Bits

17. The following are available at t.t.l. levels on individual lines:-

'Frame' word : Unassigned Bit 1 of the Frame word in Time Slot 0.

'Not Frame' word : Unassigned Bits 1, 4, 5, 6, 7, and 8 of the Not Frame Word in Time Slot 0. Bit 3 (Distant Alarm) is also available.

'Multiframe' word : Unassigned Bits 5, 7 and 8 of the Multiframe word in Frame 0, Time Slot 16.

Signal lamp and buzzer

18. A valid signal applied to the input is indicated by a lamp and maybe enforced by the use of an audible warning provided by an internal buzzer. The buzzer will also indicate errors detected, change of signalling code state and the presence of external count input pulses.

Power supply and signal input impedance

19. The instrument may be powered from an a.c. supply or from an external 12 V battery. The p.c.m. signal can be connected to either a 75 Ω unbalanced or a 120 Ω balanced input on the front panel.

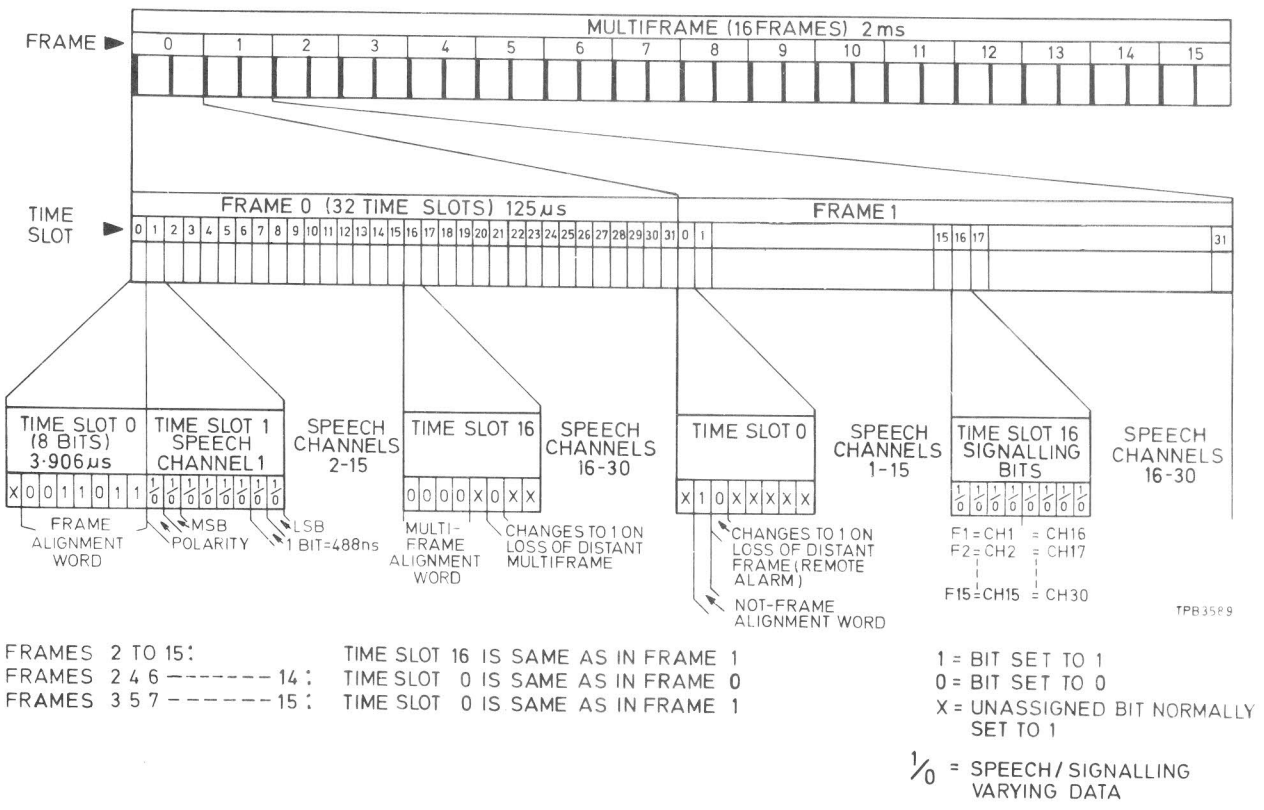


Fig. 2 CCITT standard frame structure for a 30-channel 2.048 Mbit/s system

Note...

The CCITT frame structure allows the positions of the frame alignment word and the not-frame alignment word to be transposed. Receive sections in p.c.m. multiplex equipment are designed to have independent frame and multiframe locking circuits and will work with either configuration.

PERFORMANCE DATA

20. Signal input

Format :

A high density bipolar (HDB3) coded p.c.m. signal conforming to CCITT Rec. G703, with or without frame structures to G732 at 2048 kbit/s, or to G742 at 8448 kbit/s. AMI is switch selectable.

Bit rates :

2048 kbit/s ±50 p.p.m.
8448 kbit/s ±30 p.p.m.

Amplitude :

Switch selected sensitivity for terminating a 75 Ω or 120 Ω source directly or from monitor points with source impedances of 2400 Ω (75 Ω input) or 3000 Ω (120 Ω input). The nominal attenuation of the signal from a monitor point is 33 to 1 (≃ 30 dB).

Source impedance	Nominal peak amplitude
75 Ω	2.37 V
120 Ω	3.00 V
2400 Ω	72 mV
3000 Ω	91 mV

The input sensitivity also allows for further loss from a feed cable having a 6 dB attenuation at half the bit rate.

Jitter :

Jitter tolerance to CCITT Recommendation G703.

Signal lamp :

A valid signal is indicated by a signal lamp. The lamp will extinguish when the input signal is attenuated by 5 dB more than the 6 dB cable loss. The lamp will also discriminate against a wrong bit rate being applied. If set to 2M CODE, an all zeroes signal in an 8448 kbit/s HDB3 coded signal will illuminate the SIGNAL lamp.

Audible alarm :

An internal buzzer can be set to indicate the same conditions as the signal lamp.

21. Input impedance/return loss

75 Ω unbal :

75 Ω unbalanced, BNC connector.

Return loss greater than 15 dB from 50 kHz to 100 kHz, and greater than 20 dB from 100 kHz to 12 MHz.

120 Ω bal :

120 Ω balanced, Siemens type connectors. Return loss greater than 20 dB at 1 MHz.

Measurement modes

22. HDB3 line code error detector at 2048 kbit/s :

Detects HDB3 line code errors in a 2048 kbit/s digital stream and displays the totalized errors, error ratio or percentage error free seconds. AMI is selectable via an internal link.

Error ratio :

Error ratio is displayed in the form of a mantissa and exponent from 0 in 10^7 to 1 in 10^1.

Totalize :

Errors are totalized on a 6 digit counter with overflow indication and stop, continue and reset to zero facilities.

The totalizing counter will continue to function when the display is set to error ratio.

Error free seconds :

Percentage error free seconds are displayed as a four digit indication selected by depressing LAMP TEST and CHANNEL.

Audible alarm :

Internal buzzer may be switched into circuit and set to give an indication of either signal present or error detected.

23. HDB3 line code error detector at 8448 kbit/s :

As 2048 kbit/s but for an 8448 kbit/s digital stream.

24. Frame alignment monitor at 2048 kbit/s :

Checks the frame structure of a 2048 kbit/s digital stream to CCITT Rec. G732. AMI is switch selectable.

Displays any frame or multiframe alarms found and monitors the frame word for errors which are displayed as a totalized count, error ratio or percentage error free seconds. The 2833A automatically aligns itself to the incoming signal.

The channel time-slot can also be selected and its number is displayed.

Frame word error ratio : Error ratios of greater than 0 in 10^7, 1 in 10^7, 1 in 10^6, 1 in 10^5, 1 in 10^4 and 1 in 10^3 are indicated on the display. The error ratio for the frame alignment word is calculated statistically on the assumption that the digital input signal contains errors which have a Poisson distribution. The operation of the error ratio display is summarized below.

Error ratio indication	*Average error ratio in input signal*	*Probability (%) of indication illuminating or extinguishing within the periods (seconds) stated below.*	
		Illuminate	Extinguish
1 in 10^3	1 in 10^3	>50% within 0.3s	<5% within 0.3s
	5 in 10^4	<5% within 0.3s	-
	1 in 10^4	-	>95% within 0.3s
1 in 10^4	1 in 10^4	>50% within 3s	<5% within 3s
	5 in 10^5	<5% within 3s	-
	1 in 10^5	-	>95% within 3s
1 in 10^5	1 in 10^5	>50% within 30s	<5% within 30s
	5 in 10^6	<5% within 30s	-
	1 in 10^6	-	>95% within 30s
1 in 10^6	1 in 10^6	>50% within 5 min.	<5% within 5 min.
	5 in 10^7	<5% within 5 min.	-
	1 in 10^7	-	>95% within 5 min.
1 in 10^7	1 in 10^7	>50% within 50 min	<5% within 50 min.
	5 in 10^8	<5% within 50 min	-
	1 in 10^8	-	>95% within 50 min.

Frame word error totalizing : Frame word errors are totalized on a six digit counter with overflow indication and stop, continue and reset to zero facilities.

The totalizing counter will continue to function when the display is set to error ratio.

Error free seconds : Represents the probable performance of a single 64 kbit/s channel by extrapolation of detected frame word errors within time slot 0 only. The result does not relate directly to the error free performance for the entire 2048 kbit/s digital stream.

Audible alarm : An internal buzzer may be switched into circuit and set to give an indication of signal present or alarm conditions.

Alarm indications : Lamps will light when alarms are detected. The alarm indications are listed in the signalling monitor mode section.

25. Signalling monitor at 2048 kbit/s :

Displays the signalling code for a selected channel in a 2048 kbit/s digital stream to CCITT Rec. G732.

Signalling code :

The present signalling code (binary) in the selected channel is displayed as its decimal equivalent. The previous signalling code may be recalled.

Last number dialled :

When a circuit seized signalling condition is present, the signalling code is monitored for dial breaks and the last number dialled is displayed.

During dialling, the 2833A can detect errors listed in the following table and flashes the corresponding error code on the display on and off for approx. 5 secs.

Limits can be specified for use on various PTT systems.

Error code	*Error*
1	Detected signalling code not Circuit Seized or Dial Break.
2	Dial Break pulse too narrow.
3	Dial Break pulse too wide.
4	Interdial Break too narrow.
5	Interdial Break too wide.
6	11 or more Dial Break pulses.

Channel selection :

The channel can be selected and its number displayed.

Audible alarm :

Internal buzzer may be switched into circuit and set to give an indication of signal present or change of signalling code.

Frame errors :

When switched to 2M SIG mode, from the 2M ALIGN mode, the 2833A continues to count frame alignment errors which can be displayed as error ratio, total errors or percentage error free seconds on switching directly back to 2M ALIGN mode.

Alarm indications :

Lamps will light if the following alarms are detected :-

(Alarm indications also function in 2M ALIGN mode.)

Alarm priority : When more than one alarm condition is detected only the highest priority alarm condition is indicated, the priorities are listed in descending order below :-

Line : Lamp will light when no signal is present (defined as eleven or more consecutive zeros or low level), or a wrong bit rate is present.

Alarm indication signal AIS : Lamp will light when the signal is all 1's (defined as signal with less than 3 zeros in 512 bits).

Frame : Lamp will light when three consecutive frame alignment words have been received each with one or more errors. The lamp will extinguish when a sequence of correct frame, not-frame and frame alignment words has been detected.

Errors : Lamp will light if the error ratio in the frame alignment word is greater than 1 in 10^5 (averaged over a 30 s period).

Recovery is checked over a 30 s period, so up to 60 s may elapse before alarm clears on removal of errors. This delay may be overriden by selecting AUTO RESET.

Multiframe : Lamp will light when two consecutive multiframe alignment words have been received each with one or more errors. The lamp will extinguish when one correct multiframe alignment word has been received.

Distant : Lamp will light when the distant frame alarm is received on at least two consecutive occasions. The lamp will extinguish when the non-alarm condition is detected (see Note).

Distant multiframe : Lamp will light when the distant multiframe alarm is received on two consecutive occasions. The lamp will extinguish when the non-alarm condition is detected (see Note).

Note...

Multiframe and distant multiframe alarms may be inhibited by internal links.

Indication mode : Switch selected to AUTO RESET or LAMP LOCK.

Auto reset : Lamp is on for the length of time an alarm condition exists with a minimum of 300 ms unless overridden by a higher priority alarm. Only one alarm is displayed at any one time.

Lamp lock : Lamp remains on after alarm clears. An alarm condition must clear before the possible occurrence of another alarm condition can be indicated. Lamps remain on until they are reset by selecting AUTO RESET.

26. External count input : Accepts incoming pulses from an external source and displays totalized result or percentage error free seconds. The count can be stopped, started or reset to zero.

Rate : 0 to 4 kHz.

Format : Positive t.t.l. pulses of 2 to 5 V peak amplitude from 200 to 600 ns duration.

Impedance : 75 Ω unbalanced; return loss greater than 20 dB over the range 40 kHz to 3 MHz.

Connector : BNC connector.

Audible alarm : Internal buzzer may be switched into circuit and set to give an indication of input pulses.

Miscellaneous

27. Self checks : An internally generated signal of 2048 kbit/s with a known error ratio of 1 in 10^5 checks the input and line code error detector circuits.

Lamp check : A lamp check button will illuminate all panel lamps and displays.

28. RS-232-C output : This output is suitable for direct connection to a modem for remote monitoring or to a local printer via a null modem connector.

Connector : 25-way D connector to ISO/IS21 10 (1980). (Male)

Implementation : RS-232-C (V.24 ,V.28)

Circuit	*CCITT Circuit*	*Pin No.*	*Function*
CA	105	4	Request to send
CB	106	5	Clear to send
CD	108/2	20	Data Terminal Ready
CF	109	8	Received line signal detector
AB	102	7	Signal ground
BA	103	2	Transmitted Data
CC	107	6	Data Set Ready
AA	101	1	Protective Ground

Transmission rate : 9600, 1200, 600 and 300 Baud.
Switch selectable.

Code : ASCII 8 data bits - no parity.
1, 1.5 and 2 stop bits.
Switch selectable.

Format : 24 and 40 characters per line.
Switch selectable.

Level : Corresponding to CCITT Recommendation V.28.

Identification : Instrument identification is switch selectable to 1, 2, 3 or 4.

Time reference : Where printers have real time capability, time and date will be printed at the end of each print event.

Time print command : DC4.

Print events and strategies

29. 2M and 8M CODE

Header : IDENT 2M(8M) CODE EVENT ERROR TOTAL

Header printed on mode selection or error total reset.

Print events : No Signal
(No Signal) recovery
Error Ratio >1 in 10^1
Error Ratio >1 in 10^2
Error Ratio >1 in 10^3
Error Ratio >1 in 10^4
Error Ratio >1 in 10^5
Error Ratio >1 in 10^6
Error Ratio >1 in 10^7
Error Ratio <1 in 10^7
N error(s)

Strategy :

Single errors printed when the error ratio is below 1 in 10^6.

Error total updated at each print event, except (No Signal) Recovery.

In Percentage Error Free Seconds mode a Percentage Error Free Seconds result will be printed only after a print event at any time within a period not exceeding 10 seconds after a print event occurs. The count is reset after 12 hours and the event recorded.

Instrument identification printed at each print event.

30. 2M ALIGN

Header :

IDENT 2M ALIGNMENT EVENT ERROR TOTAL

Header printed on mode selection or error total reset.

Print events :

Loss of input
AIS
Loss of Frame Alignment
Error Ratio >1 in 10^3
Error Ratio >1 in 10^4
Error Ratio >1 in 10^5
Multiframe
Distant Alarm
Distant Multiframe
Error Ratio >1 in 10^6 } Advisory only
Error Ratio >1 in 10^7 } Advisory only
Error Ratio <1 in 10^7 } Advisory only
N Errors
Alarm Recovery

Strategy :

When multiple alarms are present only the highest priority alarm is printed. For the list above, the priority extends to Distant Multiframe.

The advisory only terms can be printed coincidentally with Multiframe, Distant and Distant Multiframe Alarms.

Single errors printed when the error ratio is below 1 in 10^5.

Error total updated at each print event, except alarm recovery.

In Percentage Error Free Seconds mode a Percentage Error Free Seconds result will be printed only after a print event at any time within a period not exceeding 10 seconds after a print event occurs. The count is reset after 12 hours and the event recorded. Percentage error free seconds print-out available on demand.

Instrument identification printed at each print event.

31. 2M SIG

Header : IDENT 2M SIGNALLING EVENT ERROR TOTAL

Header printed on mode selection or error total reset.

Print Data :
Channel number
Current signalling code
Digit dialled
Error code
Alarm - Loss of Input
AIS
Loss of Frame Alignment
Error Ratio >1 in 10^3
Error Ratio >1 in 10^4
Error Ratio >1 in 10^5
Multiframe
Distant Alarm
Distant Multiframe
Alarm recovery

Print event :
Selection of 2M Signalling mode
Channel Selection
Change of signalling code
Dialling
Alarm
Alarm recovery

Strategy :
Current signalling and channel number printed except for dialling.

For dialling, the digit dialled or error code is printed. For multiple digit sequences, channel number is printed at end of sequence provided that time between digits does not exceed 4 seconds.

When multiple alarms are present, only the highest priority alarm is printed. See priority list above.

Error total updated at each print event, except alarm recovery.

32. EXT COUNT

Header :

IDENT EXTERNAL COUNT TOTAL

Header printed on mode selection.

Strategy :

The count total is printed only after a count input at any time within a period not exceeding 10 seconds after the count input occurs.

In Percentage Error Free Seconds mode a Percentage Error Free Seconds result will be printed only after a print event at any time within a period not exceeding 10 seconds after a print event occurs. The count is reset after 12 hours and the event recorded. Percentage error free seconds print-out available on demand.

Instrument identification printed at each print event.

33. 64 kbit/s co-directional signal output :

The eight bit data word of a selected time-slot (push button selected) is converted to a 64 kbit/s co-directional output signal conforming to CCITT Rec. G.732.

Impedance :

120 Ω balanced.

Connectors :

Siemens type in parallel with ITT Cannon RTG 16 socket.

Balance :

Greater than 40 dB from 40 kHz to 400 kHz.

Jitter :

Less than 0.06 bit/s peak to peak in the frequency range 20 Hz to 20 kHz with a jitter free input signal.

34. Alarm detector output :

An output t.t.l. signal of +5 V is produced when an alarm is detected in the 2M ALIGN or 2M SIG mode. It is not affected by LAMP LOCK.

35. 15-way output socket :

The following outputs are available from a 15-way D-type connector on the rear panel.

Pen recorder :

A recorder output is available for monitoring code error ratio or frame structure alarms. The f.s.d. current may be internally set at 1 mA or 5 mA by internal links (normally set to 1 mA). Maximum current is produced by selecting TEST LAMP.

Mode		*Output current*	
2M/8M CODE	*2M ALIGN/2M SIG*	*5mA max.*	*1mA max.*
No signal	Line alarm	0	0
-	AIS alarm	1	0.2
-	Frame alarm	1.5	0.3
Error ratio 1 in 10^3	Error ratio 1 in 10^3	2	0.4
Error ratio 1 in 10^4	Error ratio 1 in 10^4	2.5	0.5
Error ratio 1 in 10^5	Error ratio 1 in 10^5	3.0	0.6
Error ratio 1 in 10^6	Multiframe alarm	3.5	0.7
Error ratio 1 in 10^7	Distant alarm	4.0	0.8
-	Distant m.f. alarm	4.5	0.9
Signal - no errors	Signal - no errors	5.0	1.0

Error rates less than 1 in 10^7 single errors cause an output current (4.0 mA) to be generated for a short period of time (line code errors only).

The pen-recorder output is automatically set to AUTO RESET. The priority of alarms is the order given above, i.e. lower current = higher priority.

Accuracy ±0.1mA (+0.1mA, -0 at 0mA)

Accuracy ±0.03mA (+0.03mA, -0 at 0mA)

Errors output : An output pulse is provided every Frame alignment word error and code error via the 15-way OUTPUTS connector.

Pulse amplitude : TTL.

Pulse width :
8M CODE : 120 ns.
2M CODE : 490 ns.
2M ALIGN : 245 ns.
2M SIG : 245 ns.

64 kbit/s sync output : A negative-going t.t.l. pulse is available, the negative edge of which corresponds to the start of the octet of data in the selected channel via the 64 kbit/s co-directional output.

'Frame' word : Unassigned bit 1 of the frame word in Time Slot 0, is available on an individual line at t.t.l. level.

'Not Frame' word : Unassigned bits 1, 4, 5, 6, 7 and 8 of the not frame word in Time Slot 0, are available on individual lines at t.t.l. levels.

Bit 3 (Distant alarm) is also available.

'Multiframe' word : Unassigned bits 5, 7 and 8 of the multiframe word in Frame 0 Time Slot 16, are available on individual lines at t.t.l. levels.

36. Power requirements

AC supply :	115 V or 230 V nominal.
Voltage range :	95 V to 130 V and 190 V to 264 V a.c.
Frequency :	50 Hz to 400 Hz.
Consumption (a.c.) :	18 VA.
External d.c. :	12 V d.c. nominal. Supply may be connected to terminals on the rear panel.
Consumption (d.c.) :	15 VA (nominal).

37. Dimensions and weight

Height	Width	Depth	Weight
110 mm	260 mm	340 mm*	3.2 kg
4.3 in	10.25 in	13.4 in	7.1 lb

*410 mm (16.1 in) with cover.

38. Safety : Complies with IEC 348 safety requirements.

Environmental

39. Temperature range

Limits of operation : 0° to 55°C.

40. Conditions of storage and transport

Temperature :	-40°C to +70°C.
Humidity :	Up to 90% r.h.
Altitude :	Up to 2500 m, i.e. pressurized freight at 27 kN/m^2 (3.9 lbf/in^2) differential.

41. Radio frequency interference : Conforms to the requirements of EEC Directive 76/889 as to limits of r.f. interference.

ACCESSORIES

42. Supplied accessories

43129-163L	3 metre lead assembly (side entry) for a.c. power supplies.
46881-589V	Instruction manual.
46881-626G	Operating card.
23435-574T	Gender changer (Female to Female) for RS-232-C Male connector.

43. Optional accessories

54124-022L	Protective front panel cover assembly.
46883-514A	D-type plug 15-way assembly.
46883-513K	Flexible extender board assembly for servicing printed circuit boards.
46883-401T	Rack mounting kit.
44419-001N	75 Ω high impedance probe. A 2k4Ω series resistance (1/4 W, 2%) with BNC connectors, for monitoring 75 Ω systems.
43130-224U	120 Ω high impedance probe. A 3-pin plug assembly with a free end for fitting to an appropriate connector provided by the customer.
43130-228J	BNC to SMB lead assembly. A lead assembly with a male BNC connector at one end and a female SMB connector at the other.
43130-296F	Null Modem Lead. A lead assembly with female connectors at both ends.
43130-297G	RS-232-C Lead. A lead assembly with a female connector at one end and a male connector at the other.
46883-801L	D-type plug 25-way assembly.
46883-824Z	Gender changer (Female to Female) for RS-232-C Male connector.
46883-852R	RS-232-C Null Modem adapter.
44419-002L	75 Ω high impedance probe. A 1 kΩ series resistance (1/4 W, 2%) with BNC connectors, for monitoring 75 Ω systems.

ALTERNATIVE VERSIONS

44. The following alternative versions of the 2833A are available.

52833-910Z	Digital Line Monitor 2833A Standard Version.
52833-314X	Digital Line Monitor 2833A SAPO signalling.
52833-316C	Digital Line Monitor 2833A Swedish signalling.
52833-317R	Digital Line Monitor 2833A JTAS Denmark signalling.
52833-319K	Digital Line Monitor 2833A Telecom Eireann signalling.
52833-320R	Digital Line Monitor 2833A NZPO signalling.
52833-322K	Digital Line Monitor 2833A Tester No. 246C/MKA/2.
52833-323A	Digital Line Monitor 2833A Cable and Wireless signalling.
52833-324Z	Digital Line Monitor 2833A PTT India signalling.

Chapter 2

INSTALLATION

CONTENTS

UNPACKING AND REPACKING

1. Retain the container, packing material and the packing instruction note (if included) in case it is necessary to reship the instrument.

2. If the instrument is to be returned for servicing attach a label indicating the service required, type or model number (on rear label), serial number and your return address. Pack the instrument in accordance with the general instructions below or with the more detailed information in the packing instruction note.

(1) Place a pad in the bottom of the container.

(2) Place pads in the front and rear ends of the container with the plywood load spreader(s) facing inwards.

(3) Put the polythene cover over the instrument and place it in the container with the front handles and rear projections (where applicable) against the plywood load spreaders.

(4) Place pads in the two sides of the container with cushioning facing inwards.

(5) Place the top pad in position.

(6) Wrap the container in waterproof paper and secure with adhesive tape.

(7) Mark the package FRAGILE to encourage careful handling.

Note...

If the original container or materials are not available, use a strong double-wall carton packed with a 7 to 10 cm layer of shock absorbing material around all sides of the instrument to hold it firmly. Protect the front panel controls with a plywood or cardboard load spreader; if the rear panel has guard plates or other projections a rear load spreader is also advisable.

AC MAINS OPERATION

3. Before connecting the instrument to the a.c. supply, check the position of the voltage selector on the rear panel. The instrument is normally supplied with the selector set in the range 210 V to 240 V and fuses of 250 mA (slow blow). To change the voltage rating to the range 105 V to 120 V, reverse the L-shaped plate on the rear panel and switch the slide-switch to the 115 V position. For this voltage range the supply fuses must be changed to 500 mA slow blow.

4. The free a.c. supply cable is fitted at one end with a female plug which mates with the a.c. connector at the rear of the instrument. When fitting a supply plug ensure that conductors are connected as follows:

Earth - Green/Yellow
Neutral - Blue
Live - Brown

5. When attaching the mains lead to a non-solder type plug, it is recommended that the tinned ends of the lead are first cut off, owing to the danger of cold flow causing intermittent connections.

SAFETY TESTING

6. Where safety tests on the mains input circuit are required, the following procedures can be applied. These comply with BS 4743 and IEC Publication 348. Tests are to be carried out as follows and in the order given, under ambient conditions, to ensure that mains input circuit components and wiring (including earthing) are safe.

(1) Earth lead continuity test from any part of the metal frame to the bared end of the flexible lead for the earth pin of the user's mains plug. Preferably a heavy current (about 25 A) should be applied for not more than 5 seconds.

Test limit : not greater than 0.5 Ω.

(2) 500 V d.c. insulation test from the mains circuit to earth.

Test limit : not less than 2 MΩ.

DC OPERATION

7. The instrument can operate from an external 12 V d.c. supply, connected to the terminals marked + and - on the rear panel. Check that a 2 A (slow blow) rated supply fuse is fitted.

Chapter 3

OPERATION

CONTENTS

CONTROLS AND CONNECTORS

1. All functions, except for supply on/off, are selected by push-button switches on the front panel.

Notes...

(1) In certain cases a push-button switch selects one function when depressed and another one when released. This is indicated on the panel by the symbol ▬ for the depressed function and ▭ for the released function.

(2) To release a depressed button, press it again.

2. Front panel (see Fig. 1)

(1) SUPPLY ON/OFF switch. Set to ON, the display will initially indicate the number 2833A and the software number when a.c. or d.c. supplies are connected.

(2) DISPLAY. Gives numerical display of totalized errors, mantissa and exponent value of the error ratio, channel and time-slot number, decimal equivalent of the signalling code and last number dialled, depending on measurement mode selected.

(3) 75 Ω unbalanced INPUT connector. Connection for a p.c.m. digital signal from a 75 Ω system.

(4) 120 Ω balanced INPUT connectors. Connection for a p.c.m. digital signal from a 120 Ω system.

(5) SOURCE impedance switches. Select 75 Ω and 120 Ω load for terminated measurements or corresponding 2400 Ω and 3000 Ω when accessing monitor points. Used to compensate for signal level when the 2833A measurement configuration is to terminate or access 75 Ω or 120 Ω p.c.m. systems.

(6) SIGNAL lamp. Illuminates when a valid HDB3 p.c.m. signal of the correct amplitude and bit density is present.

(7) FUNCTION - UP/DOWN switches. Select any one of the five modes by incrementing upwards/downwards in single steps.

(8) Mode indicator lamps. Individual lamps illuminate corresponding to the mode selected by switches (7).

(9) TEST - SELF switch. Automatically selects the 2M CODE mode, and displays the error ratio of an internally generated line-code signal with an error ratio of 1 in 10^5. The instrument stays in 2M CODE until another mode is selected by (7).

(10) TEST - LAMP switch. Illuminates all lamps on the front panel and provides an FSD current at the pen recorder output on the rear panel.

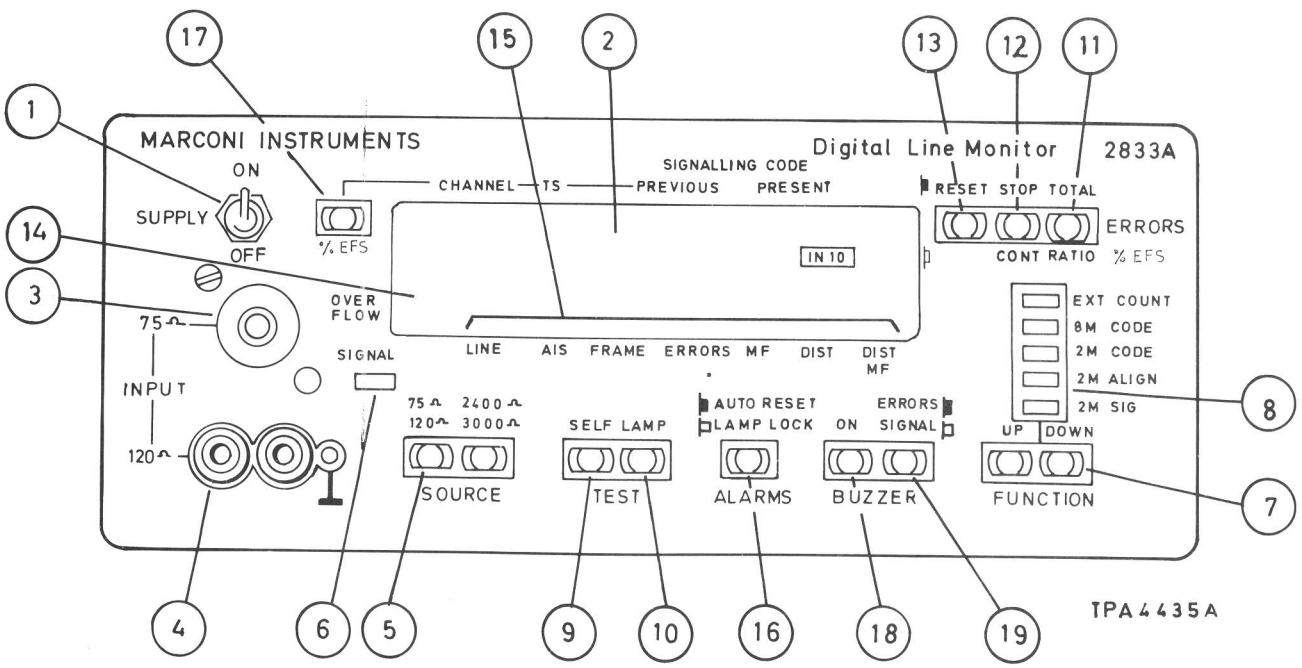


Fig. 1 Front panel controls

(11) ERRORS - TOTAL/RATIO switch. Set to TOTAL, displays totalizing count of errors in modes 2M CODE, 8M CODE, 2M ALIGN and EXT. COUNT, read from the six-digit display. Set to RATIO, displays the error ratio in modes 2M CODE, 8M CODE and 2M ALIGN.

(12) ERRORS - STOP/CONT switch. Set to STOP, prevents continuation of totalizing count and holds display reading. Set to CONT, allows totalizing count to continue.

(13) ERRORS - RESET switch. Returns counter and display to zero. Will also clear OVERFLOW lamp (14).

(14) OVERFLOW lamp. Illuminated when counter display has reached full capacity. Display returns to all zero indication before continuing count.

(15) Alarm lamps. Illuminated to indicate alarm states present in the p.c.m. signal and operate in order of priority.

(16) ALARMS AUTO RESET/LAMP LOCK switch.

(a) Set to AUTO RESET, an alarm condition will be indicated by alarm lamps (15). When the alarm clears, the lamp is extinguished.

(b) Set to LAMP LOCK, an alarm condition is indicated by alarm lamps (15) and will continue to be indicated after the alarm is cleared. The alarm lamps are reset by selecting AUTO RESET and reselecting LAMP LOCK.

(17) CHANNEL/TS select switch. Increments or decrements the channel or time-slot number indicated on the display in the 2M ALIGN and 2M SIG modes. Also used to select the previous signalling code.

(18) BUZZER - ON switch. Enables an internal buzzer to indicate presence of either signal or errors as determined by (19).

(19) BUZZER ERROR/SIGNAL switch. Set to SIGNAL, gives audible indication of a signal present at the 75 Ω or 120 Ω inputs. Set to ERROR, gives audible indication of errors present for 2M and 8M CODE, 2M ALIGN modes, change of signalling code in 2M SIG mode and indication for an external count signal in the EXT. COUNT mode. Operates for approx. 0.5 s on detection of a single error and retriggered for successive errors.

3. Rear panel (see Fig. 2)

(1) Mains input connector. Accommodates a.c. supply lead connector.

(2) Voltage selector switch. Selects either 105 to 120 V or 210 to 240 V range to suit local a.c. supply.

(3) Fuses. AC mains input fuses rated at 250 mA (slow-blow) for 210 to 240 V or 500 mA (slow-blow) for 105 to 120 V.

(4) EXT. BATTERY terminals. Input connection for a 12 V d.c. supply (negative is connected to chassis). Current drain is approximately 1.25 A.

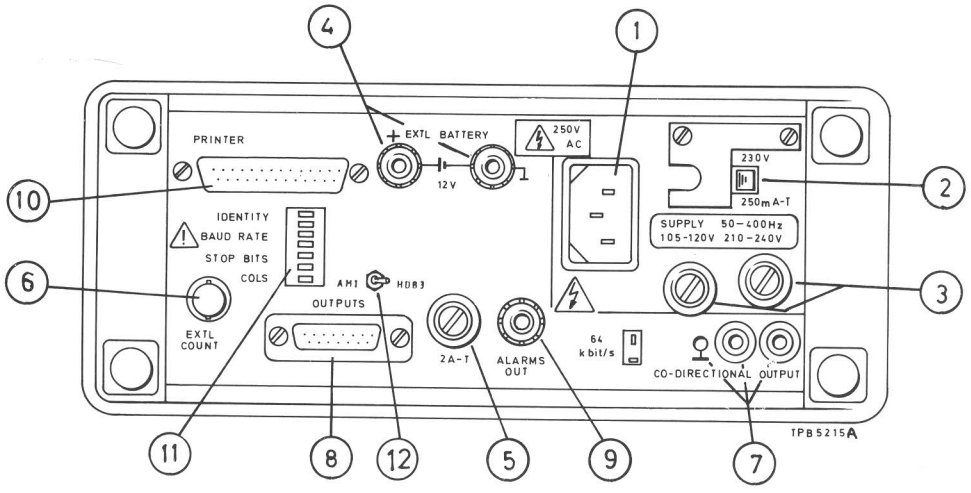


Fig. 2 Rear panel controls and connectors

(5) Battery fuse. Battery input fuse rated at 2 A (slow-blow).

(6) EXT. COUNT connector. 75 Ω unbalanced input for positive t.t.l. pulses when FUNCTION switch is set to EXT. COUNT.

(7) CO-DIRECTIONAL O/P, 64 kbit/s. Siemens type sockets in parallel with BT Jack Test 43 provide an output for monitoring channel time-slot information at 64 kbit/s rate.

(8) OUTPUTS 15-way D-type connector. Provides the following outputs:-

Pen recorder:- Provides a current output corresponding to error ratio and frame structure alarms. Can be internally set for a f.s.d. of 1 or 5 mA.

Error output:- Provides an output pulse coincident with a frame alignment word error or signalling code error. For use as an external count drive or trigger source for an oscilloscope.

64 kbit/s sync:- Provides a negative-going t.t.l. pulse, the negative edge of which corresponds to the start of the octet data in the selected channel output via the 64 kbit/s co-directional output.

Unassigned bits:- The following are available on individual lines at t.t.l. levels:-

Bit 1 of Frame Word in TS0.
Bits 1, 4, 5, 6, 7 and 8 of Not Frame Word in TS0. Also Bit 3 (Distant Alarm).
Bits 5, 7 and 8 of Multiframe Word in TS16 of Frame 0.

(9) ALARMS OUT terminal. Output line provides a signal when any alarm is detected in the 2M ALIGN mode. This output may be used for connection to TEST LEAD TO TF 2829 input terminal of the TF 2828A to check 2833A performance using TF 2828A sequence tests.

Note...

The output is taken directly from an alarms detector and has no additional delay introduced.

(10) PRINTER 25-way D-type connector. Output connection to a printer. Output level is specified to Recommendation V.28 and Interface circuits configured to Recommendation V.24 of CCITT Recommendations in the Yellow-book Vol. VIII - 1 1980.

(11) Printer function switches. Eight miniature switches used for setting PRINTER output for 2833A identification, Baud rate, Stop bits and number of print out columns.

(12) AMI/HDB3 switch. Two position toggle switch. Set switch for either AMI or HDB3 line code operation.

OPERATING PROCEDURES

4. Set SUPPLY switch to ON. The display indicates 2833A and the software number prior to automatic selection of 2M CODE.

5. Connect the p.c.m. signal to the 120 Ω or 75 Ω INPUT. For 75 Ω systems connect the signal to the 75 Ω INPUT. If the 2833A is to terminate a 75 Ω system, depress SOURCE 75 Ω/120 Ω switch to select 75 Ω termination. If the 2833A is required to monitor a 75 Ω system via a 2.4 kΩ resistance, depress SOURCE 2400 Ω/3000 Ω switch to select 2400 Ω (see Fig. 3).

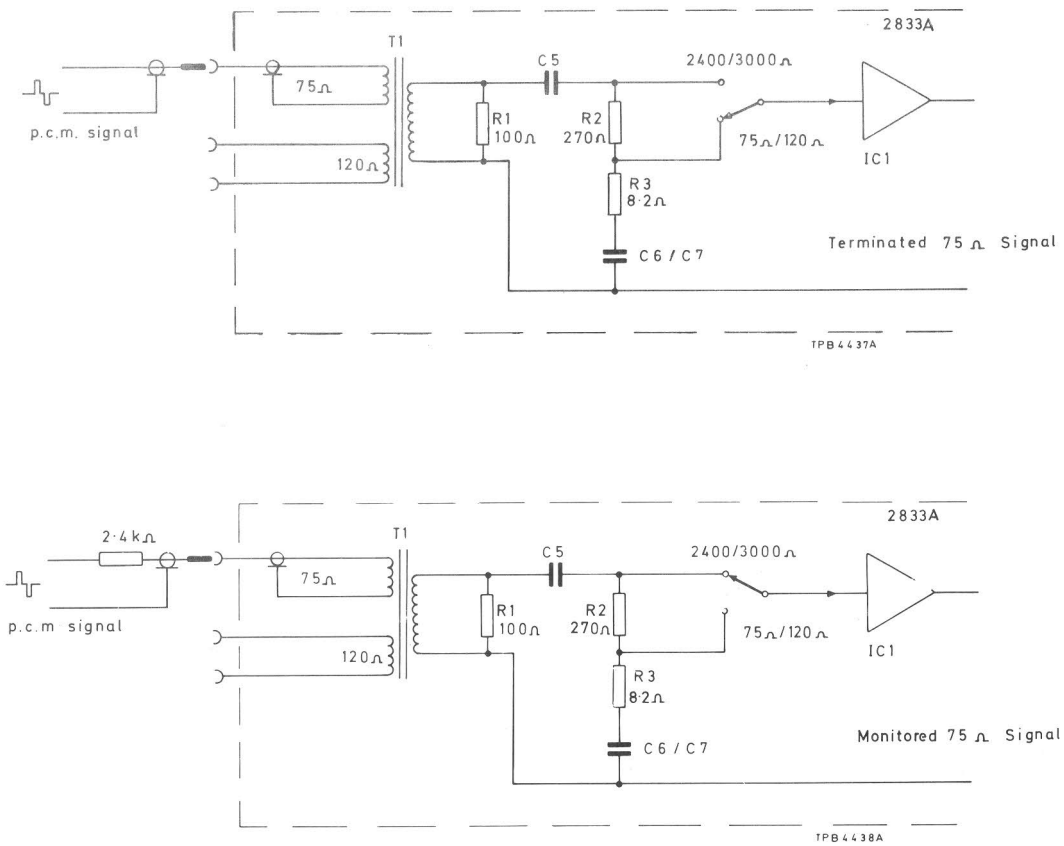


Fig. 3 Terminated and Monitor modes for 75 Ω systems

6. For 120 Ω systems, connect the signal to the 120 Ω INPUT. If the 2833A is to terminate a 120 Ω system, depress SOURCE 75 Ω/120 Ω switch to select 120 Ω termination. If the 2833A is required to monitor a 120 Ω system via a 3 kΩ resistance, depress SOURCE 2400 Ω/3000 Ω switch to select 3000 Ω (see Fig. 4).

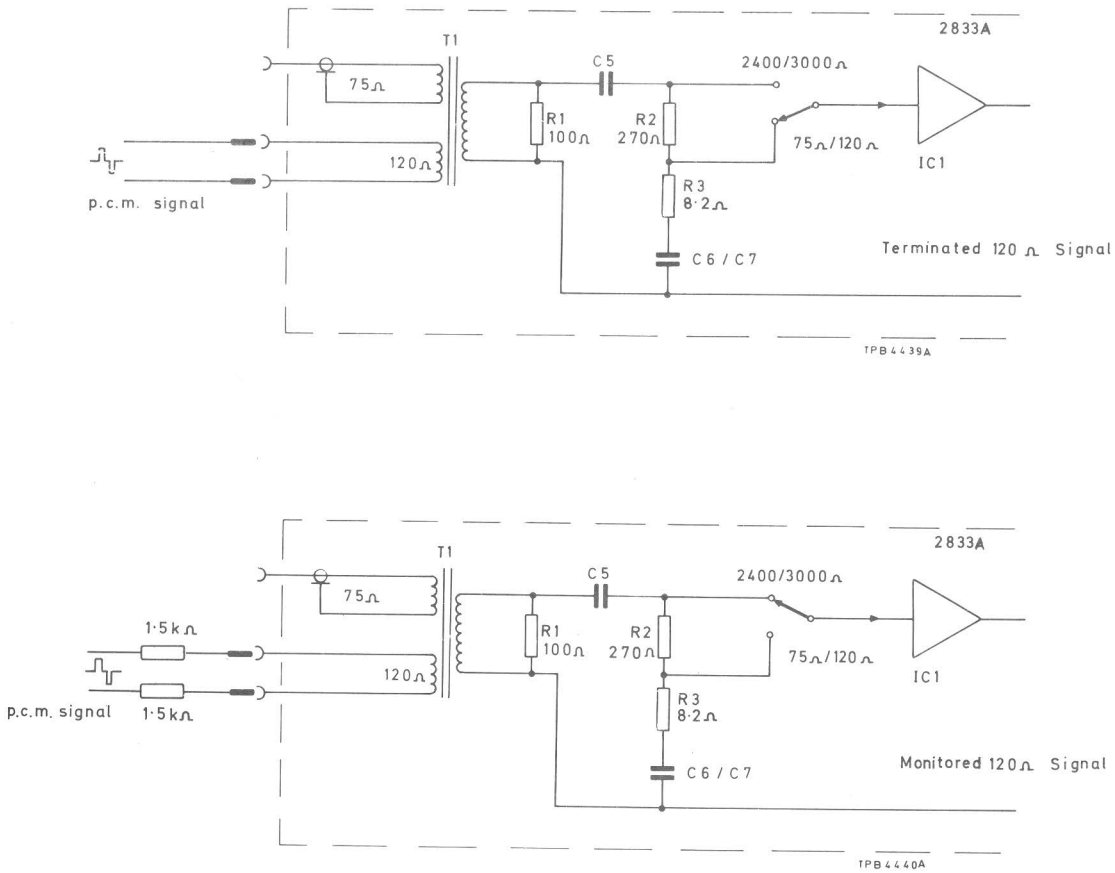


Fig. 4 Terminated and Monitor modes for 120 Ω systems

7. Depress SELF TEST switch and check that the 2M CODE is selected and that the display indicates an error ratio of 1 in 10^5. The ERRORS switches are overridden during this test.

8. Depress LAMP TEST switch and check that all panel lamps and display digits are illuminated. The PROM part number and program issue can be displayed by holding LAMP TEST depressed and switching SUPPLY to ON.

OPERATION OF MEASUREMENT MODES

9. The operation of the following measurement modes are described with the aid of front panel diagrams highlighting the controls and functions relevant to each mode.

10. HDB3 line code error detector at 2048 kbit/s (2M CODE)

(1) Select 2M CODE by operating FUNCTION UP/DOWN switches.

(2) Check the SIGNAL lamp is illuminated indicating that a valid signal at the correct bit rate and amplitude is present. The BUZZER-ON SIGNAL switches may also be set for the same purpose.

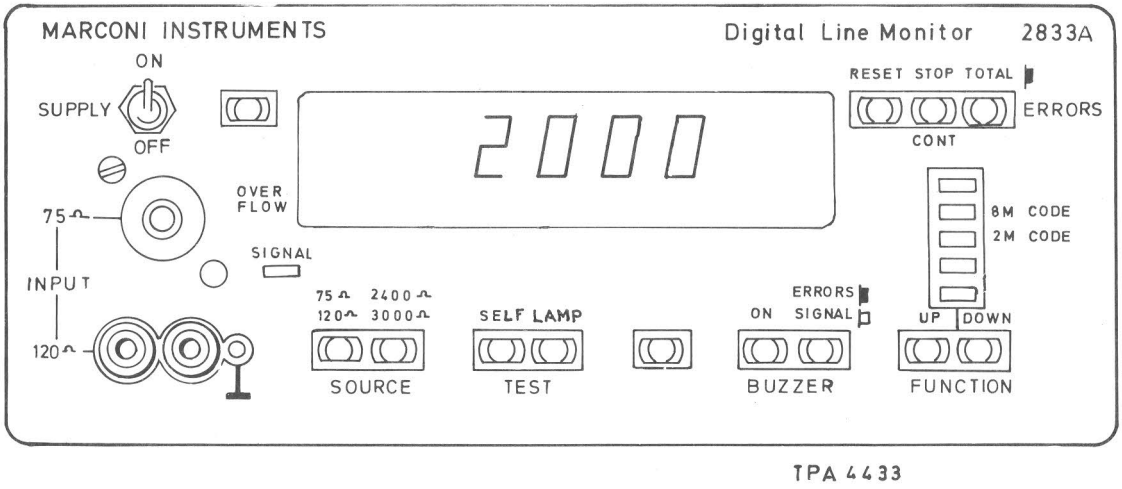


Fig. 5 Line code error totalization selected

(3) To display totalization of errors, select ERRORS - TOTAL. If no errors are detected, a zero is displayed by the right-hand digit. If errors are present, the counter will totalize. To hold count display, select STOP. To continue count, select CONT. To reset count display to zero, select RESET.

Note ...

Totalization and error ratio measurements operate simultaneously as two separate functions in the selected mode on the instant a valid signal is present at the 2833 INPUT.

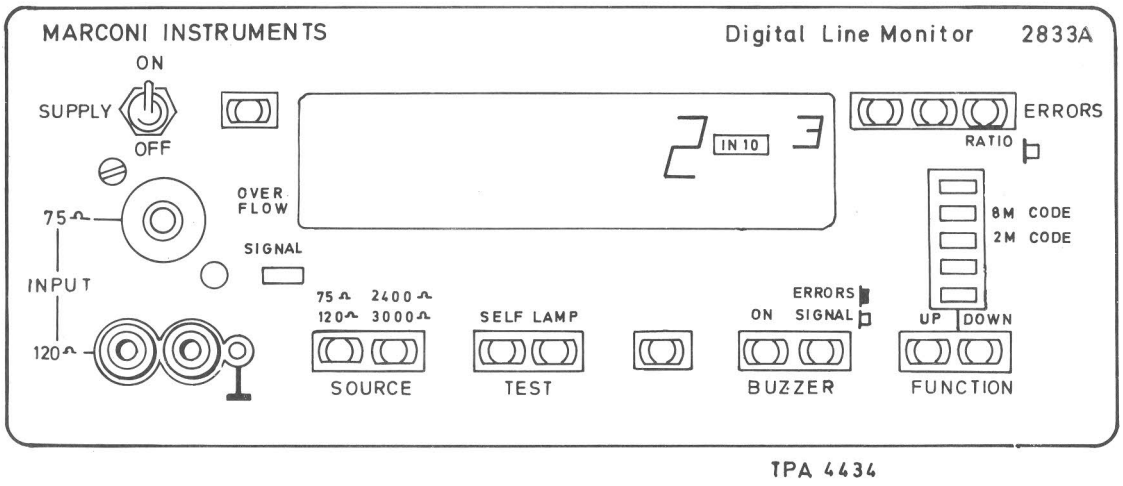


Fig. 6 Line code error ratio selected

(4) To display error ratio, select ERRORS - RATIO. If no errors are detected, 0 in 10^7 is displayed by the right-hand digit and exponent digit. Totalization of errors continues in the error ratio function and can be restored by selecting ERRORS - TOTAL.

Note...

In RATIO; STOP, CONT and RESET will operate on the totalizing count without having the totalizing count displayed.

(5) If the signal is 'lost' or removed during error measurement, the display will go blank. Upon recovery of the signal, the display indicates the error state the counter had reached before the signal was removed and resumes error measurement.

(6) To enable an audible indication of errors detected, select BUZZER - ON and - ERROR, the BUZZER will sound for the duration of errors detected or for a minimum of 0.5 seconds.

(7) For long term monitoring of errors, connect a pen recorder to the to the OUTPUTS connector on the rear panel of the 2833A. Refer to Chap. 3, Fig. 17 and Chap. 1, Page 15.

11. HDB3 line code error detector at 8448 kbit/s (8M CODE)

The operation procedure is identical to the 2M CODE mode, but applies to an 8448 kbit/s signal input.

12. Frame alignment monitor at 2048 kbit/s (2M ALIGN)

(1) Select 2M ALIGN by operating FUNCTION UP/DOWN switches.

(2) Check the SIGNAL lamp is illuminated, indicating that a valid signal at the correct bit rate and amplitude is present. The BUZZER - ON SIGNAL switches may also be set for the same purpose.

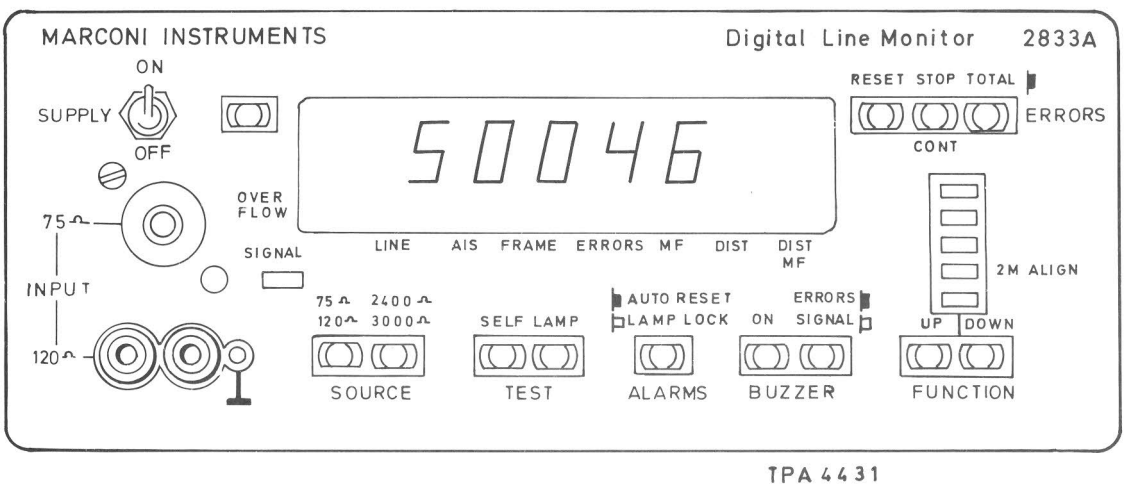


Fig. 7 Frame word error totalization selected

(3) To display totalization of frame word errors, select ERRORS - TOTAL. To hold count display, select STOP. To continue count, select CONT. To reset count display to zero, select RESET.

Note...

Totalization and error ratio measurements operate simultaneously as two separate functions in the selected mode on the instant a valid signal is present at the 2833 INPUT.

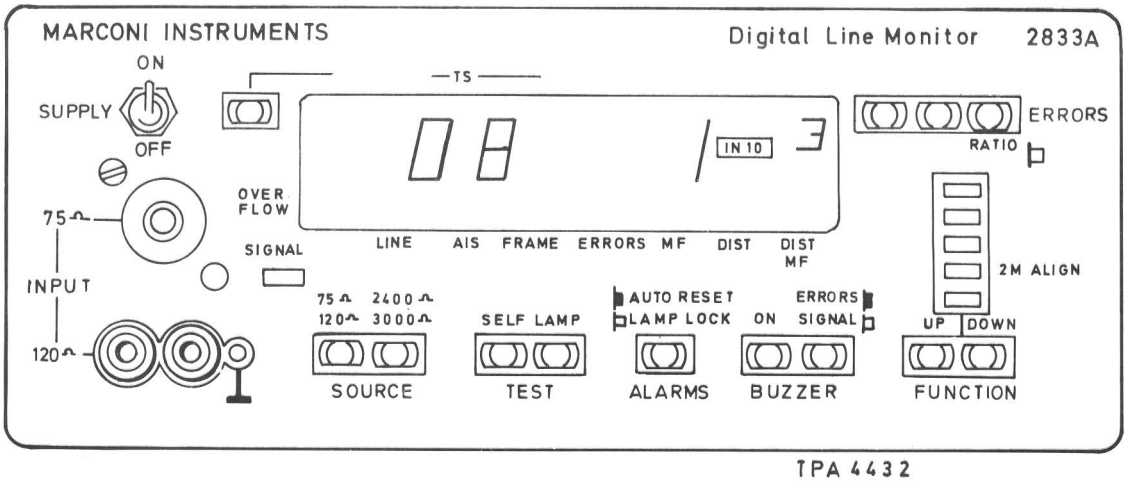


Fig. 8 Frame word error ratio selected

(4) To display frame word error ratio, select ERRORS - RATIO. The time-slot number is also displayed (see para. 9). Totalization of errors continues in the error ratio function and can be restored by selecting ERRORS - TOTAL. The time-slot display is overridden during totalization of errors.

Note...

In RATIO; STOP, CONT and RESET will operate on the totalizing count without having the totalizing count displayed.

(5) If during an error ratio measurement, LINE, AIS or FRAME alarms are detected, the display will go blank. Upon clearance of LINE, AIS or FRAME alarms, the error ratio display initializes to 0 in 10^7.

Note...

The ERRORS alarm is illuminated if the error ratio is greater than or equal to 1 in 10^5.

(6) To enable an audible indication of detected alarms, select BUZZER - ON and - ERROR.

(7) The alarm indicator lamps may be set to extinguish, following the clearance of detected alarms by selecting ALARMS - AUTO RESET. To sustain alarms, select LAMP LOCK.

(8) When any alarm is detected, the ALARMS OUT terminal on the rear panel produces a t.t.l. level of +5 V, for connection to other equipment.

Note...

The ALARMS OUT is not affected by LAMP LOCK.

(9) To select a particular time-slot between 0 and 31, depress the CHANNEL-TS switch; the display will begin counting towards 31 for the duration the switch is depressed. To reverse the direction of the count, release and depress the switch again. If the ERROR TOTAL function is in use, the error display will be overridden when the CHANNEL-TS switch is briefly depressed, whereby the time-slot is displayed. If the switch is kept depressed the time-slot will change.

(10) The information present in the time-slot of the selected channel is accessed as an encoded 64 kbit/s signal via the 64 kbit/s co-directional output sockets on the rear panel; however this output will be inhibited when a FRAME alarm is detected i.e. frame alignment has been lost or a higher priority alarm has been detected.

(11) When the mode is changed directly from 2M ALIGN to 2M SIG, the selected time-slot display will change to indicate the corresponding channel as shown below.

2M ALIGN mode display	- mode change to	2M SIG mode display
Time-Slot 0	→	Channel 1
Time-Slots 1 to 15	→	Channels 1 to 15
Time-Slot 16	→	Channel 16
Time-Slot 17	→	Channel 16
Time-Slot 18	→	Channel 17
Time-Slots 19 to 31	→	Channels 18 to 30

(12) For long-term monitoring of errors, connect a pen recorder to the OUTPUTS connector on the rear panel of the 2833A. Refer to Chap. 3, Fig. 17 and Chap. 1, page 15.

Note. The pen recorder output is automatically set to AUTO-RESET.

13. Incorrect termination. If when the 2833A is set to 2M ALIGN and 2400/3000 Ω monitor mode a full level signal - i.e. without a 2.4 kΩ or 3 kΩ external resistance in series - from a 75 Ω or 120 Ω source is connected to the 2833A 75 Ω or 120 Ω INPUT, the display could lock up on AIS or FRAME alarm indication. To clear the alarm, select the correct termination then select 2M CODE then re-select 2M ALIGN.

14. Signalling code monitor at 2048 kbit/s (2M SIG)

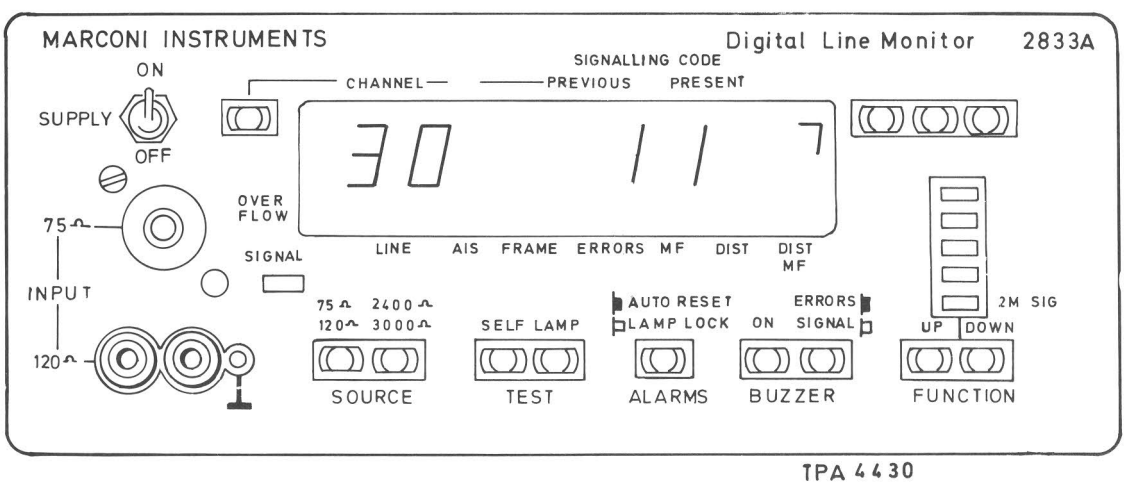


Fig. 9 Signalling code monitor mode selected

(1) Select 2M SIG by operating FUNCTION UP/DOWN switches.

(2) Check the SIGNAL lamp is illuminated, indicating that a valid signal at the correct bit rate and amplitude is present. The BUZZER - ON SIGNAL switches may also be set for the same purpose.

(3) Select desired channel from 1 to 30 by depressing CHANNEL-TS switch. Present and previous signalling codes are not displayed when the channel is changing.

(4) The selected channel signalling code is displayed as its decimal equivalent and may be interpreted by referring to Table 1. While monitoring a particular channel, a circuit seized condition may occur (indicated by Signalling Code 3), followed by a dial break (Signalling Code 11) during which the exponent digit in the display goes blank. After each number is dialled, assuming there are no dialling errors the last number dialled between 0 - 9 is displayed by the exponent digit.

(5) Errors may be detected when a number is dialled and the error code displayed by the exponent digit. When an error code is displayed, the exponent digit will flash the error code on and off. Table 2 lists the possible errors with their associated codes.

TABLE 1 INTERPRETATION OF BRITISH TELECOM SIGNALLING CODES

Decimal signal displayed	*Binary state*	*Signalling condition*	
		Forward	*Back*
0	0000		
1	0001	Trunk offer	Manual hold
2	0010		-
3	0011	Circuit seized	Called-subscriber answer
4	0100	-	-
5	0101	Earth	Earth
6	0110	-	-
7	0111	-	Circuit free
8	1000	-	-
9	1001	-	Coin fee check
10	1010	-	-
11	1011	Dial break	-
12	1100	-	-
13	1101	Disconnection	Disconnection
14	1110	-	-
15	1111	Circuit idle	Circuit busy

TABLE 2 BRITISH TELECOM ERROR CODES

Error code	*Error*
1	Detected signalling code not 3 or 11.
2	Dial break pulse less than or equal to 56 ms.
3	Dial break pulse greater than or equal to 82 ms.
4	Inter dial break less than or equal to 24 ms.
5	Inter dial break greater than or equal to 42 ms and less than or equal to 250 ms.
6	11 or more dial break pulses.

(6) To obtain the previous signalling code display of the selected channel, briefly depress the CHANNEL-TS switch.

Note...

If the CHANNEL-TS switch is kept depressed for more than a few seconds, the next channel is selected.

(7) The time-slot information present in the selected channel is accessed as an encoded 64 kbit/s signal via the 64 kbit/s co-directional output on the rear panel. To check which time-slot is being accessed, select 2M ALIGN, the display indicates the time-slot associated with the channel selected in the 2M SIG. mode as shown below.

2M SIG mode display - mode changed to	2M ALIGN mode display
Channels 1 to 15 ⟶	Time-Slots 1 to 15
Channels 16 to 30 ⟶	Time-Slots 17 to 31

Note...

The 64 kbit/s output is overridden when a Frame alarm or a higher priority alarm is detected.

(8) To enable an audible indication of a change in the signalling code for a selected channel, select BUZZER-ON and ERRORS.

(9) The alarm indicator lamps may be set to extinguish, following the clearance of detected alarms by selecting ALARMS-AUTORESET. To sustain alarms, select LAMP LOCK.

(10) Frame word error measurement continues in the 2M SIG mode and may be referred to at any time by selecting 2M ALIGN. The display may be set to indicate error totalization or error ratio.

Note...

If any mode other than 2M ALIGN is selected, frame word error information is lost.

(11) For long-term monitoring of errors, connect a pen recorder to the OUTPUTS connector on the rear panel of the 2833A. Refer to Chap. 3, Fig. 17 and Chap. 1, page 15.

Note...

The pen recorder output is automatically set to AUTO-RESET.

15. Counter for an external input (EXT. COUNT)

(1) Select EXT. COUNT by operating FUNCTION UP/DOWN switches.

(2) Connect the signal line to the 75 Ω EXTL COUNT socket on the rear panel. The count function will operate with a pulse amplitude of betweeen 2 to 5 V at a frequency up to 4 kHz.

Note...

The SIGNAL lamp and BUZZER SIGNAL is disabled in EXT. COUNT mode.

(3) To count the number of pulses received, select ERRORS-TOTAL. To hold count display, select STOP. To continue count, select CONT. To reset count display to zero, select RESET.

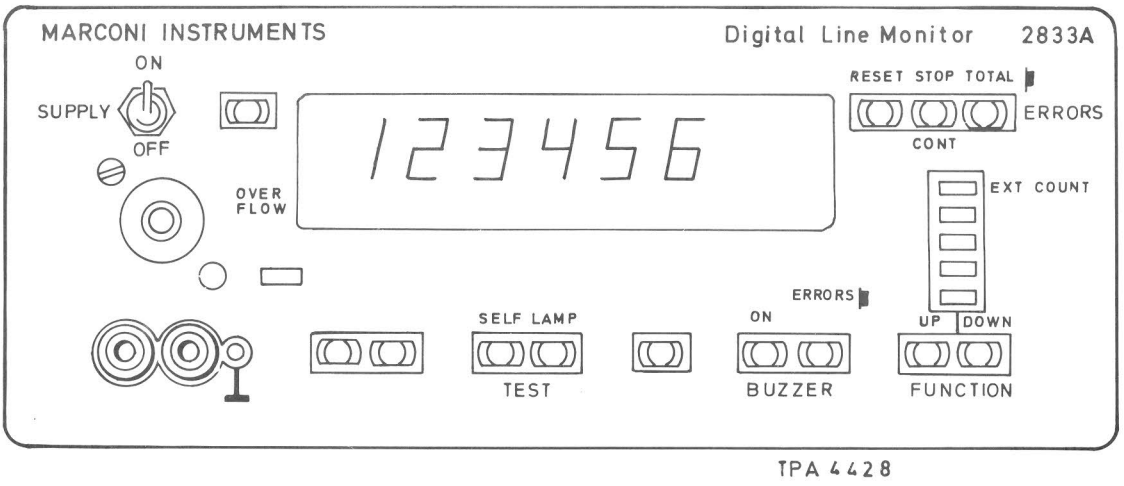


Fig. 10 External count mode selected

(4) To enable an audible indication of pulses received, select BUZZER-ON and ERROR.

Note...

The pen recorder output is disabled in EXT. COUNT mode.

Error Free Seconds mode (EFS)

16. When the 2833A is switched on it automatically monitors the input signal for code or frame word errors. When EFS is selected - via a front panel key sequence - the number of complete seconds in which no errors occurred in the period since the 2833A was switched on, mode changed or RESET, is presented as a percentage of the total number of seconds in that period. EFS is displayed if ERRORS-RATIO is selected and printed if a printer is connected.

(1) Select or deselect EFS display mode by holding LAMP TEST depressed and depress CHANNEL.

(2) If ERRORS - RATIO is selected, the four left-hand display digits will indicate EFS percentage.

Note...

EFS percentage is not displayed in ERRORS - TOTAL.

(3) Calculation of EFS continues even if the result is not displayed.

(4) The internal EFS counters are automatically reset when a period of 12 hours has elapsed. This illuminates the OVERFLOW lamp if ERRORS - RATIO is selected and if 2833A is connected to a printer a message is printed irrespective of mode selected.

(5) Extinguish OVERFLOW lamp by depressing RESET.

(6) The EFS counters can be manually reset by depressing RESET.

(7) An instant EFS printout can be obtained by selecting ERRORS - TOTAL and then selecting ERRORS - RATIO.

Error Free Second mode accuracy

17. In EFS mode the 2833A checks the input signal for the presence of errors at a regular rate and period that is close to but not exactly one second. The timing for this function is determined by the measurement mode selected. In the 2M ALIGN, 2M SIG and 2M/8M CODE modes the timing rate is obtained by counting the clock periods of the incoming bit stream. In EXT COUNT mode the timing rate is obtained by counting the microprocessor clock periods.

18. Table 3 gives the actual measuring period based on the nominal input signal bit rate or processor clock frequency where applicable. The bit rate and processor clock would be subject to small deviations from the nominal and would therefore contribute to further inaccuracies.

19. In Table 3 the measuring rate for 2M ALIGN and 2M SIG modes is the nominal timing rate of the 64 kbit/s stream. However, the display update rate is lower by a factor of 16 to 7 caused by relating the errors detected in the 7-bit Frame alignment word to the 'Framing' Time Slots - over 2 frames - totalling 16-bits.

20. For practical measurement purposes these errors are not significant and are reproduced in the table for guidance.

Note...

Due to the cumulative effect of the timing errors some inaccuracies are corrected by the instrument software enabling a more accurate 12 hour reset period. However, the remaining timing errors at the end of the 12 hour period are listed in Table 3.

TABLE 3 ERROR FREE SECONDS MODE ACCURACY

Measurement mode	*Actual measuring period 'second' (to 4 d.p.)*	*Percentage error (to 2 d.p.)*	*Actual 12 hour period reset time error to the nearest second*
2M CODE	0.9767	-2.33	-16 min 46 s
8M CODE	0.9943	-0.57	-4 min 6 s
2M ALIGN	0.9800	-2.00	+1 s
2M SIG	0.9800	-2.00	+1 s
EXT COUNT	1.0173	+1.73	+12 min 27 s

PRINTER OUTPUT

21. The RS-232-C PRINTER output enables results of measurements and alarms to be recorded via a 24 or 40 character per line printer. A maximum of 37 columns will be printed irrespective of printer capability above 24 column capability. Alternatively, the PRINTER output information can be routed to a remote printer or processor by connecting the PRINTER output directly to a modem link.

22. The 2833A can be connected to a printer via the PRINTER 25-way D-type connector on the rear panel and a Null-Modem connector. Information is printed whenever a print event occurs. Print events are listed in Table 4. If the printer is fitted with real time capability, the time and date is printed at the end of each print event.

Printer Date and Time

23. A print message from the 2833A to the printer is followed by a date and time print command. However, Date and Time will only be printed if the printer has a built-in Date and Time facility. The standard print message format is 'Message', Carriage Return, Line Feed, Print Date and Time command. The print Date and Time command for the standard 2833A is the ASCII command DC4 (equivalent to Control T ($\hat{T}$) or Character 14).

24. Other Date and Time print command options may be possible by amending the instrument software to the user's requirements, contact Marconi Instruments, Longacres, St. Albans for further information.

Shared printer

25. Up to four 2833A's can be connected to a single printer at the same time via a commercially available printer or modem sharing unit. Each 2833A is identified by a single digit which precedes each print message. The identification digit is set by a switch on the 2833A rear panel.

Bi-directional monitoring

26. It is often useful to monitor both transmit and receive paths of a digital link, for example, to compare events between send and return signalling paths of a particular channel. This can be achieved using two 2833A's connected to a single printer via a printer or modem connector, see Fig. 11.

Table 4 PRINT EVENTS AND STRATEGY

2833A mode selected	*Print event*	*Strategy*
2M CODE 8M CODE	Signal loss or recovery. Error ratio change (in range 1 in 10^1 to 0 in 10^7). Individual errors when error ratio is less than 1 in 10^6.	Error total updated at each print event except on recovery of signal.
2M ALIGN	Alarms:- LINE AIS FRAME ERRORS >1 in 10^3 " >1 in 10^4 " >1 in 10^5 MF DIST DIST MF Alarm recovery. Error ratio >1 in 10^6 >1 in 10^7 <1 in 10^7 Individual errors when error ratio <1 in 10^5 } Advisory only	1. When more than one alarm occurs, only the highest priority alarm is printed for Alarms:- LINE to DIST MF. 2. Advisory print events can be printed coincident with MF, DIST and DIST MF Alarms. 3. Frame Word error total updated at each print event except on Alarm recovery.

Table 4 PRINT EVENTS AND STRATEGY (contd.)

2833A mode selected	*Print event*	*Strategy*
2M SIG	Selection of 2M SIG mode. Channel change. Signalling code change (except during dialling). Dialling in progress (digit dialled or error code printed). Alarm or Alarm recovery. Frame Word error ratio change when >1 in 10^5.	1. Current signalling code and channel number printed except during dialling. 2. During dialling sequence, the digit dialled or error code is printed. 3. At the end of a multiple digit dialling sequence, the channel no. is printed at end of sequence provided the time between digits does not exceed 4 seconds. 4. When more than one alarm occurs, only the highest priority alarm is printed. 5. The Frame Word error total is updated at each print event except on alarm recovery.
EXT COUNT	Input pulse counted. Change Mode or RESET-ERRORS TOTAL (will print Header)	The count total is printed only after a count input at any time within a period not exceeding 10 seconds after the count input occurs.
Error Free Seconds	As for 2M CODE, 8M CODE, 2M ALIGN, EXT COUNT	EFS percentage printed only after a print event at any time within a period not exceeding 10 seconds after a print event occurs. EFS count is reset after 12 hours.

Notes... When error ratio changes by a decade, error ratio, error free seconds and error total are printed together.
When error total has overflowed, the count is continued and a printout of total errors is preceded by '*'.

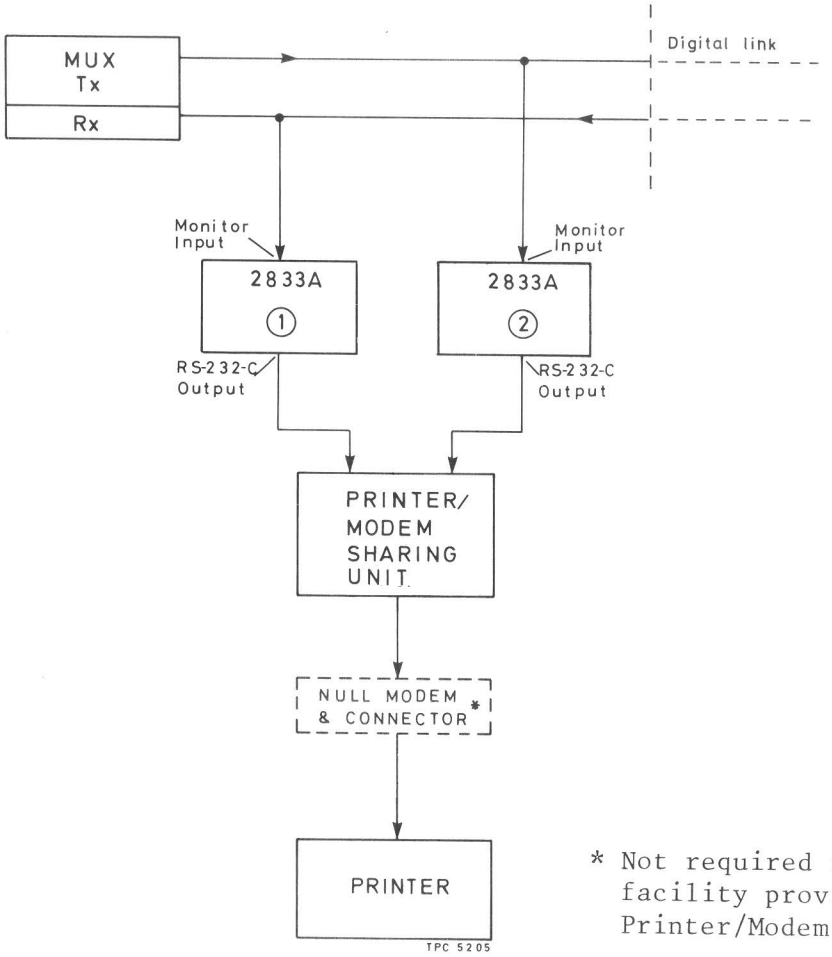


Fig. 11 Bi-directional monitoring using two 2833A's

Four 2833A's using one printer

27. Four 2833A's can be connected to a single printer using a printer/modem sharing unit. In Fig. 12 four 2833A's are used to monitor four Multiplex receivers at the same location. Each 2833A output is connected to a printer/modem sharing unit which is connected to a remote printer via a single modem link.

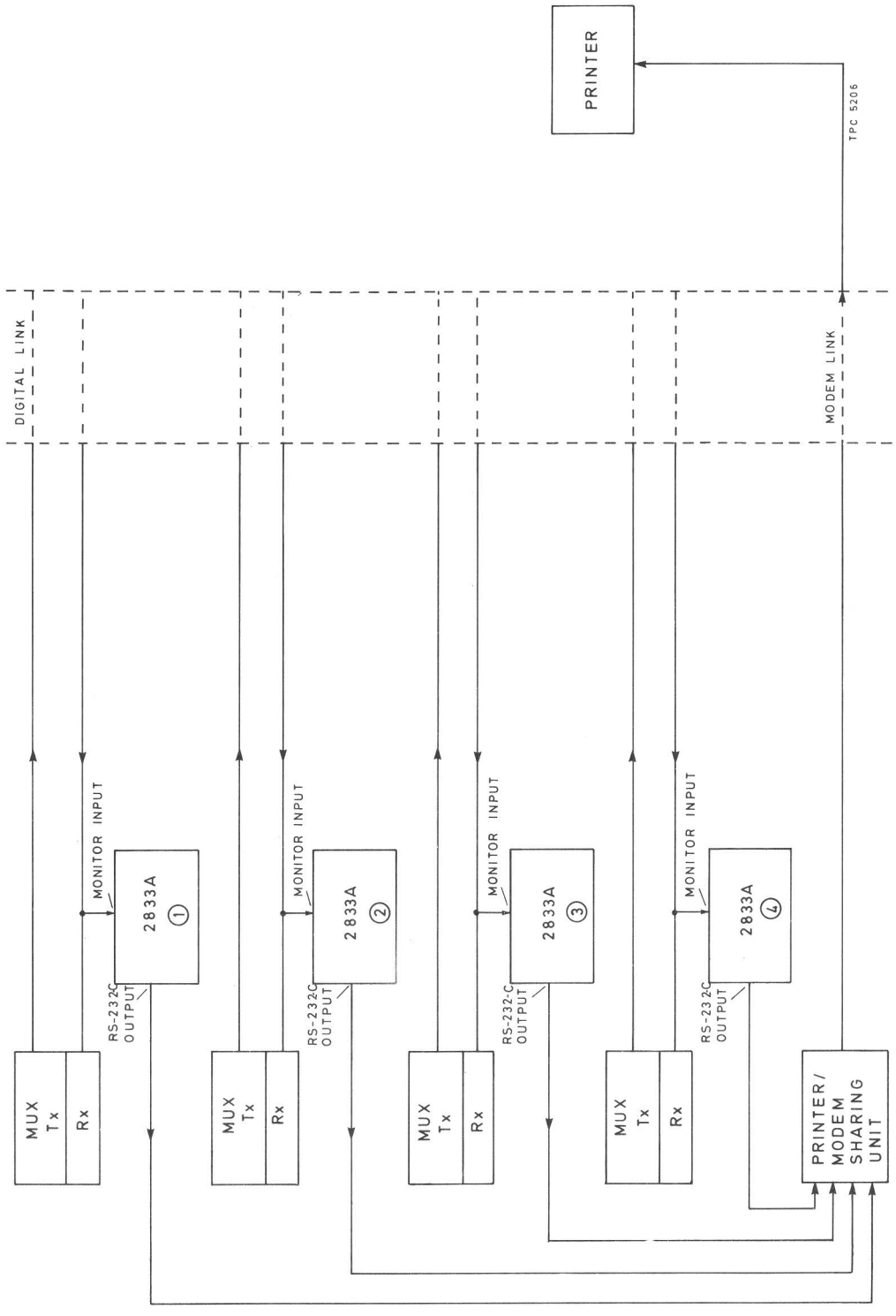


Fig. 12 Four 2833A's using one printer

Printer output settings

28. The printer output of the 2833A can be set up using a series of miniature function switches on the rear panel. The switch functions are shown in Table 5 below.

TABLE 5 PRINTER OUTPUT SETTINGS

OUTPUT FUNCTION	*TOP SWITCH*	*BOTTOM SWITCH*	*SETTING*
IDENTITY	0	0	Instrument 1
	0	1	" 2
	1	0	" 3
	1	1	" 4
BAUD RATE	0	0	300 Baud
	0	1	600 "
	1	0	1200 Baud
	1	1	9600 "
STOP BITS	0	0	Invalid
	0	1	1 stop bit
	1	0	1 1/2 stop bits
	1	1	2 stop bits
NUMBER OF COLUMNS	0		*24 columns
	1		40 columns

Notes... 1 = switch open or off.
* Print messages are abbreviated.

TIME

```
18.12.84 16:15:19
2   E.F.S. = 60.00%

18.12.84 16:15:08
2   E.F.S. = 64.71%

18.12.84 16:15:00
2   E.F.S. = 68.28%

18.12.84 16:14:52
2  ERROR RATIO >1 IN 10 E 3   328393

18.12.84 16:14:45
2  ERROR RATIO >1 IN 10 E 2    33219

18.12.84 16:14:42
2  ERROR RATIO >1 IN 10 E 3     3539

18.12.84 16:14:38
2  ERROR RATIO >1 IN 10 E 4      368

18.12.84 16:14:35
2  ERROR RATIO >1 IN 10 E 5       59

18.12.84 16:14:26
2  ERROR RATIO >1 IN 10 E 6       15

18.12.84 16:14:25
2          5 ERRORS               12

18.12.84 16:13:52
2  ERROR RATIO >1 IN 10 E 7        7

18.12.84 16:13:51
2          5 ERRORS                7

18.12.84 16:13:27
2          2 ERRORS                2

18.12.84 16:12:40
2  ERROR RATIO <1 IN 10 E 7        0

18.12.84 16:12:39
2 2M CODE      EVENT     ERROR TOTAL


13.12.84 04:09:09
2   12 HOURS. EFS RESET

12.12.84 16:26:07
2   E.F.S. = 100.0%

12.12.84 16:26:00
2 2M CODE      EVENT       ERROR TOTAL
```

EFS 12 HOUR RESET

```
18.12.84 16:17:33
2       DISTANT ALARM          END

18.12.84 16:17:33
2       DISTANT ALARM          175

18.12.84 16:17:22
2         MULTIFRAME           END

18.12.84 16:17:22
2         MULTIFRAME           175

18.12.84 16:17:19
2  ERROR RATIO >1 IN 10 E 6    175

18.12.84 16:16:51
2  ERROR RATIO >1 IN 10 E 5    175

18.12.84 16:16:45
2  ERROR RATIO >1 IN 10 E 4    166

18.12.84 16:16:40
2  ERROR RATIO >1 IN 10 E 3     17

18.12.84 16:16:40
2          2 ERRORS              9

18.12.84 16:16:32
2   LOSS OF FRAME ALIGNMENT    END

18.12.84 16:16:32
2   LOSS OF FRAME ALIGNMENT      1

18.12.84 16:16:27
2            AIS               END

18.12.84 16:16:24
2            AIS                 0

18.12.84 16:16:20
2       LOSS OF INPUT          END

18.12.84 16:16:18
2       LOSS OF INPUT            0

18.12.84 16:16:11
2  ERROR RATIO <1 IN 10 E 7      0

18.12.84 16:16:10
2 2M ALIGNMENT  EVENT     ERROR TOTAL
```

Fig. 13 Examples of print-outs

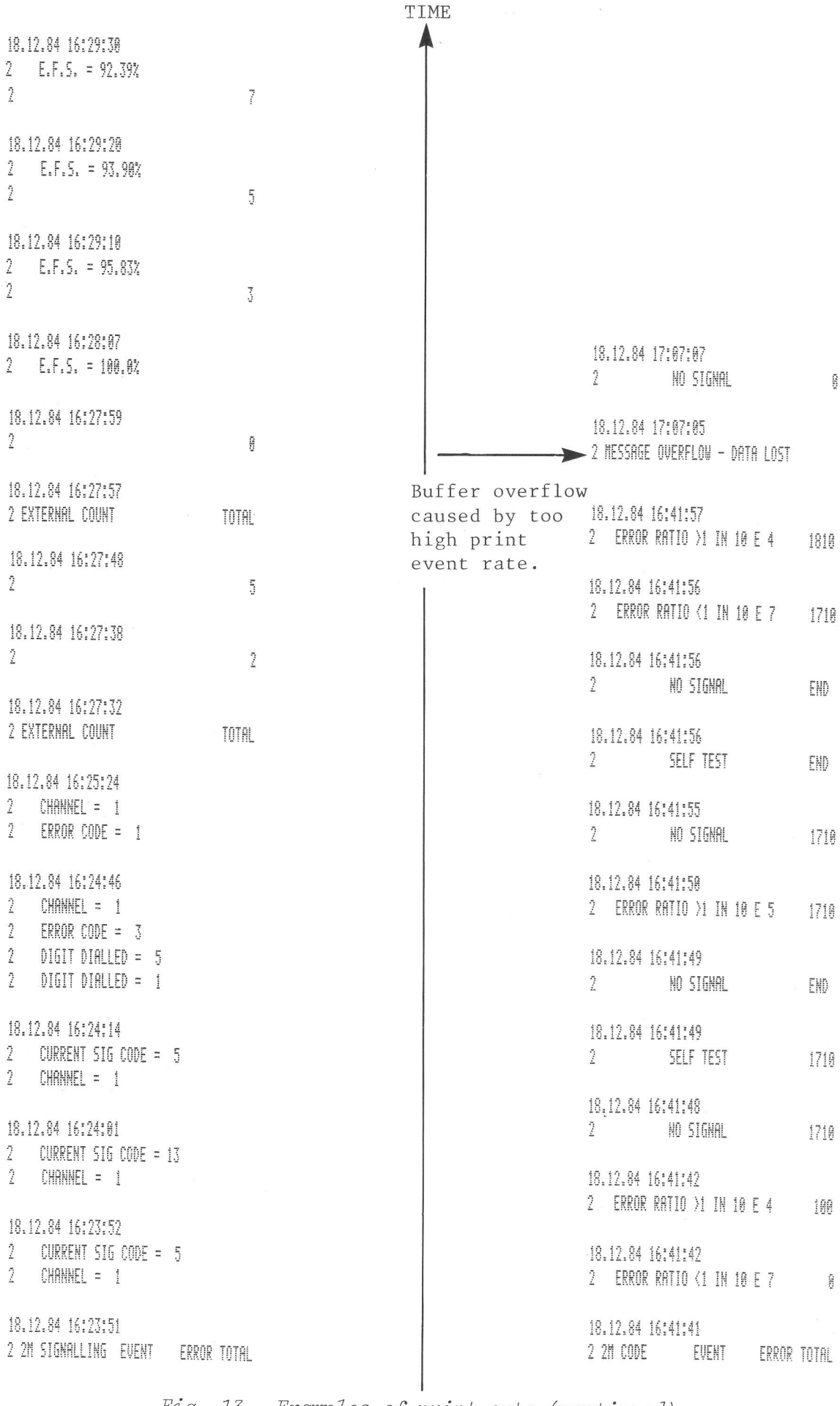


Fig. 13 Examples of print-outs (continued)

RS-232-C CONNECTIONS

29. The RS-232-C connector wiring and input/output circuit on AA12 board is shown in Fig. 14. The RS-232-C Pin out assignments are shown in Fig. 17.

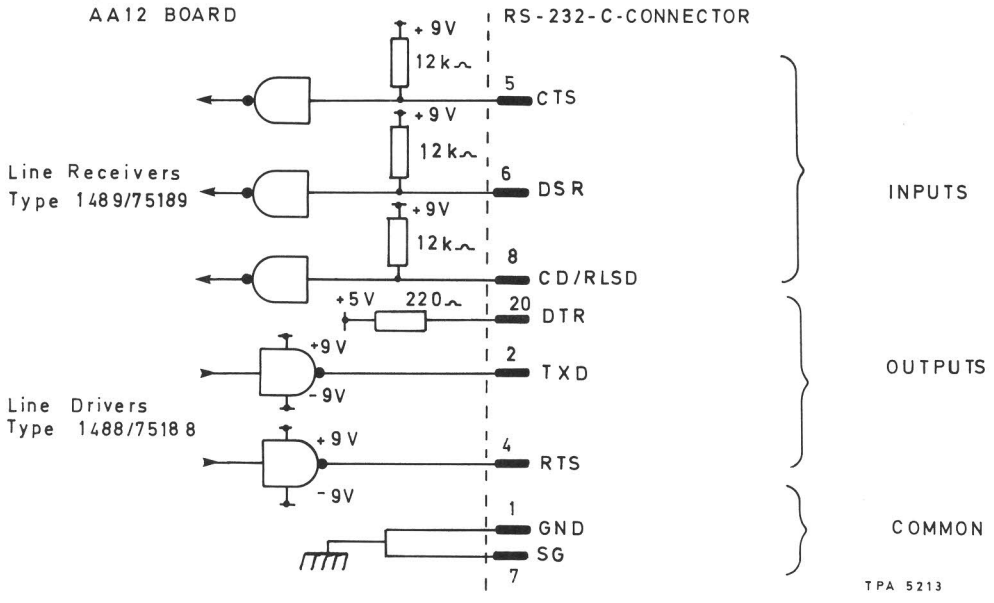
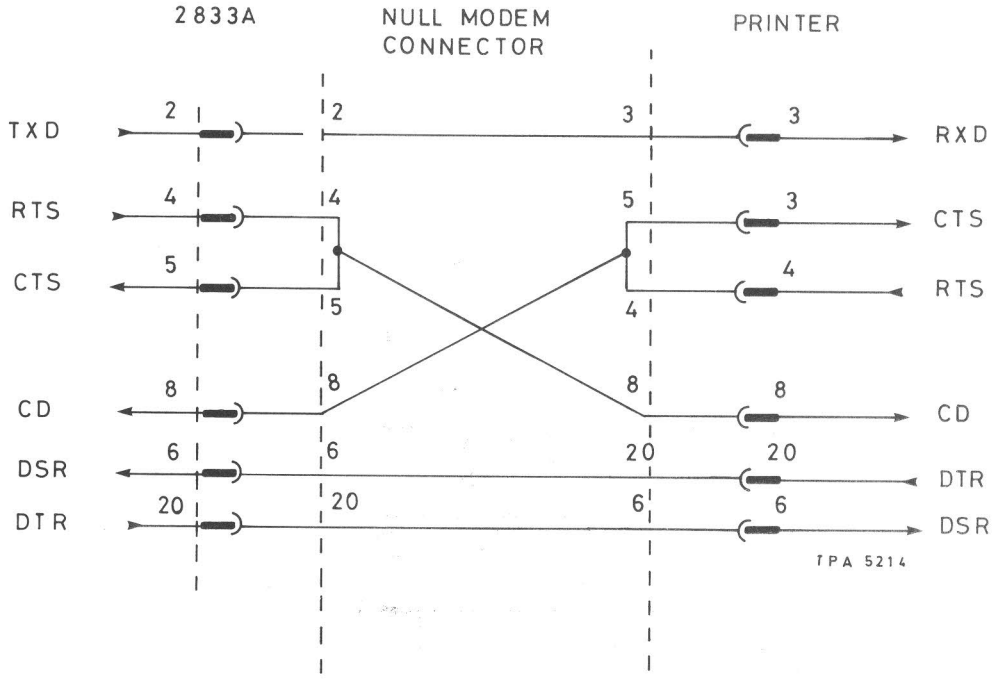


Fig. 14 RS-232-C connector input/output circuit

Null modem connector

30. The RS-232-C connector wiring is configured to connect directly to a modem interface and cannot be connected directly to a printer except via a Null-Modem interface. The interconnections are shown in Fig. 15.

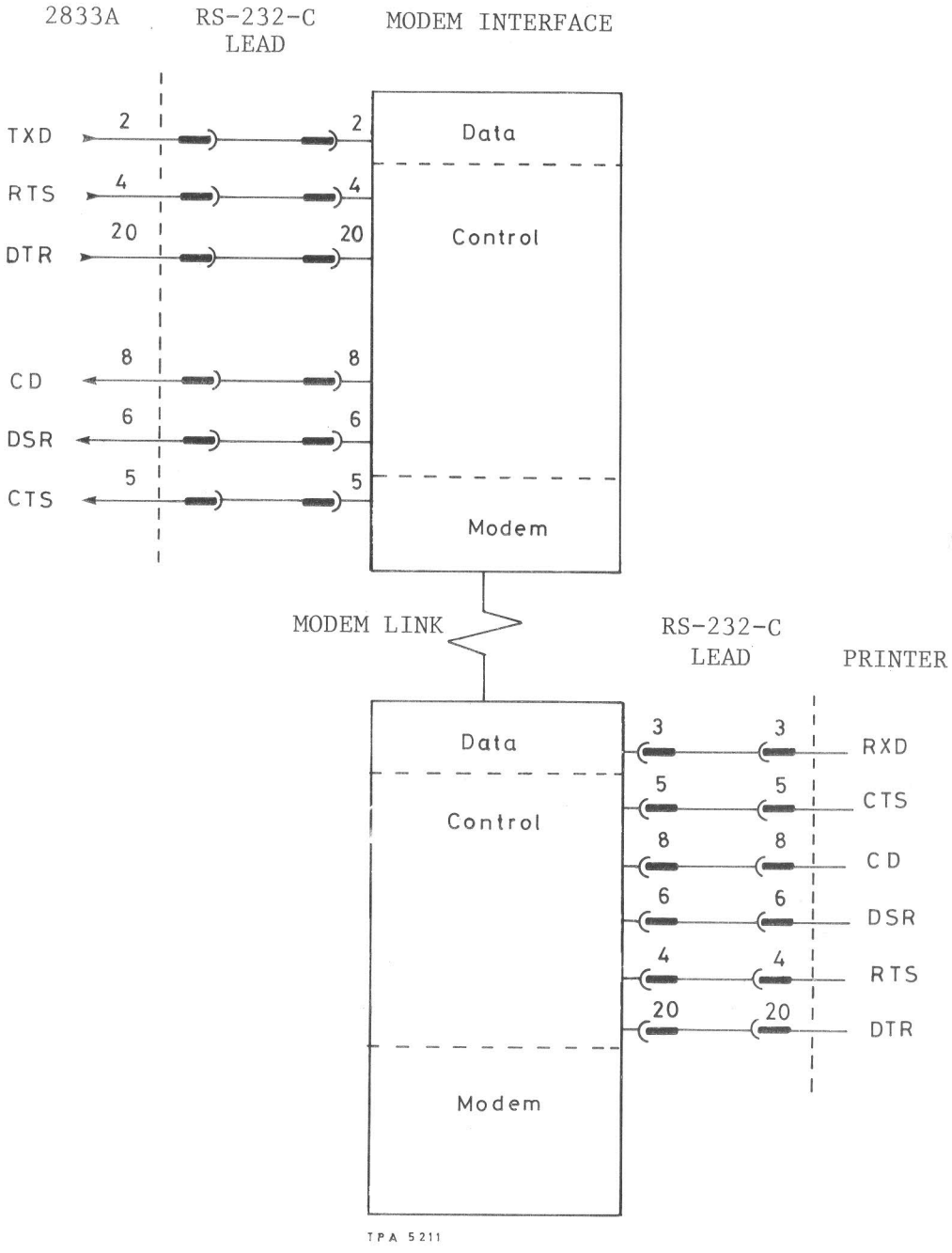


Note.. Grounds not shown.

Fig. 15 Null modem connector

Modem interconnections

31. For modem operation the 2833A RS-232-C connector is connected to a modem interface via an RS-232-C lead (available as an optional accessory). At the remote end a printer is connected to the modem interface also via an RS-232-C lead. The interconnections are shown in Fig. 16.



Note.. Grounds not shown.

Fig. 16 Modem interconnections

CONNECTOR PIN ASSIGNMENTS

32.

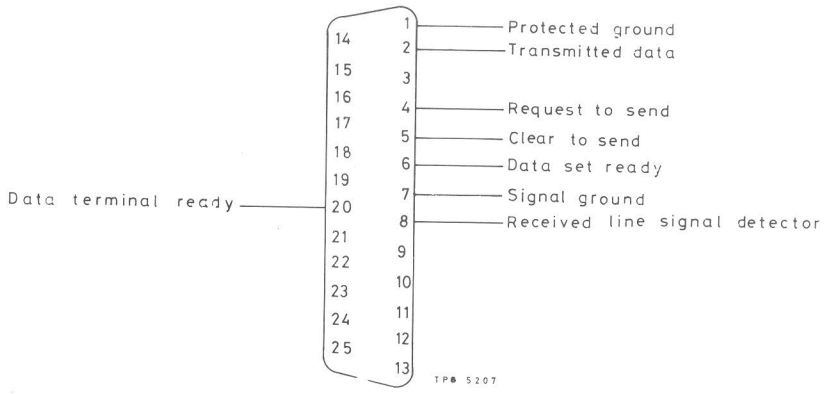


Fig. 17 Printer connector pin assignments

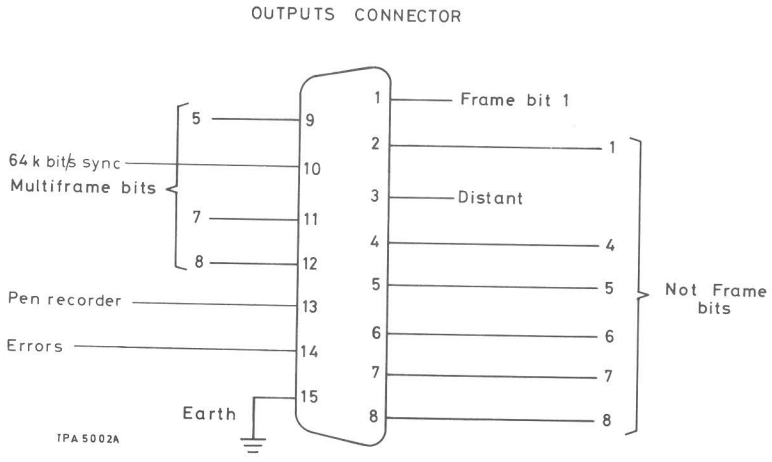


Fig. 18 Outputs connector pin assignments

Chapter 4

TECHNICAL DESCRIPTION

CONTENTS

AMI AND HDB SIGNAL CODES

1. Pulse code modulation systems digitize an analogue signal and transmit the digital pulse stream to the receiving terminal. This signal is transmitted via ordinary telephone cables, but as the waveform deteriorates rapidly it is necessary to insert regenerators at intervals along the line.

2. The function of a regenerator is to lock on to the input pulse stream and transmit a pulse of well defined amplitude and duration for each degraded pulse received. In order to reduce the bandwidth requirement and the d.c. component of the signal on the line, the polarity of alternate pulses is inverted. This is termed Alternate Mark Inversion (AMI).

3. Using this technique, it is possible to have long sequences of zeros which affect the performance of the clock extraction circuits in the regenerators. The small errors in the frequency setting of the regenerators cause jitter in the p.c.m. signal and eventual loss of information as retiming errors increase. With High Density Bipolar (HDB) codes, only a limited number of zeros are allowed to occur; usually two or three (HDB2 or HDB3). If a further zero occurs it is replaced by an extra (violation) pulse which violates the AMI bipolar sequence.

4. In order to maintain the mean level of the signal at zero volts, successive HDB violations are made to be of alternate polarity. To ensure that successive HDB violation pulses are of alternate polarity, the number of pulses between each successive HDB violation pulse must always be odd. For this reason an additional (B) pulse may be added. Fig. 1 shows a basic block diagram of an encoder showing how these pulses are produced.

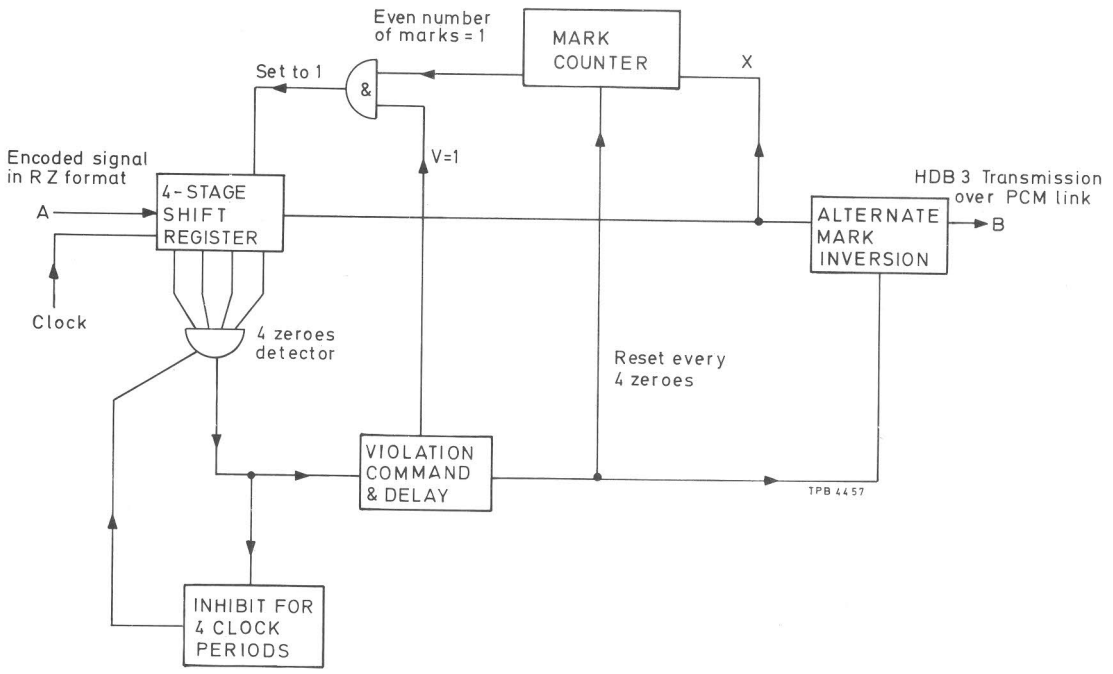


Fig. 1 Simplified block diagram of HDB3 encoder

5. Errors will be produced in a p.c.m. stream if a regenerator generates a mark when a zero was originally transmitted or vice versa. In AMI systems each error of this type will cause a violation to occur in the pulse stream which may be identified and registered. Since in HDB systems successive violations should be of opposite polarity (see Fig. 2) it is possible to identify most errors on the line.

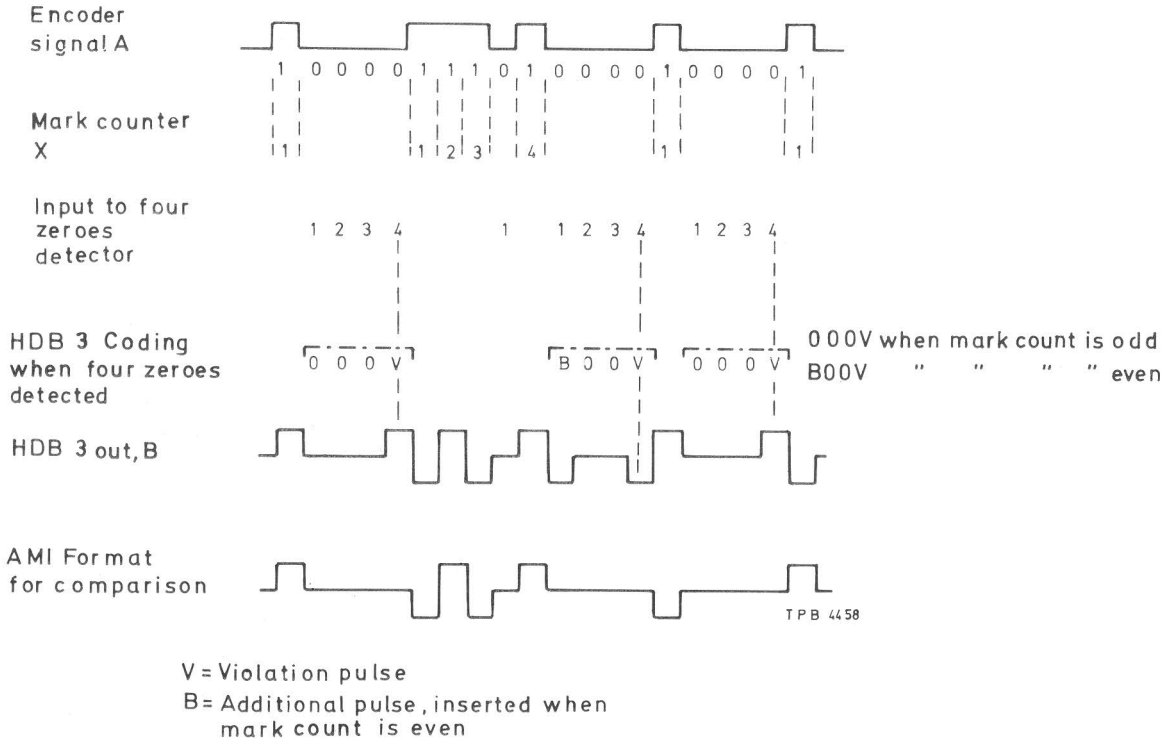


Fig. 2 Timing diagram illustrating HDB3 coding

INTRODUCTION

6. The following description should be read in conjunction with the accompanying block diagrams in this chapter and the circuit diagrams in Chap. 7.

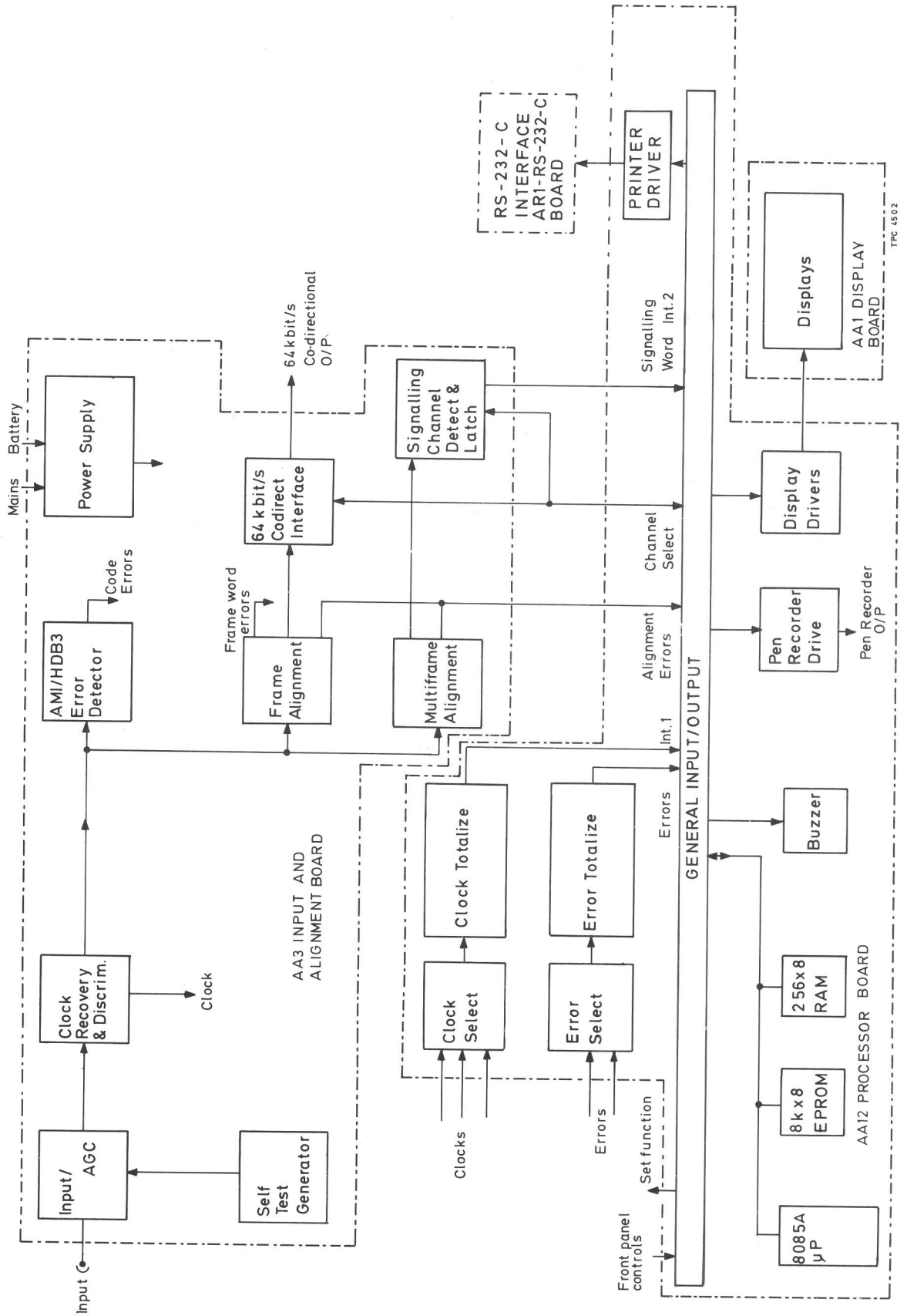
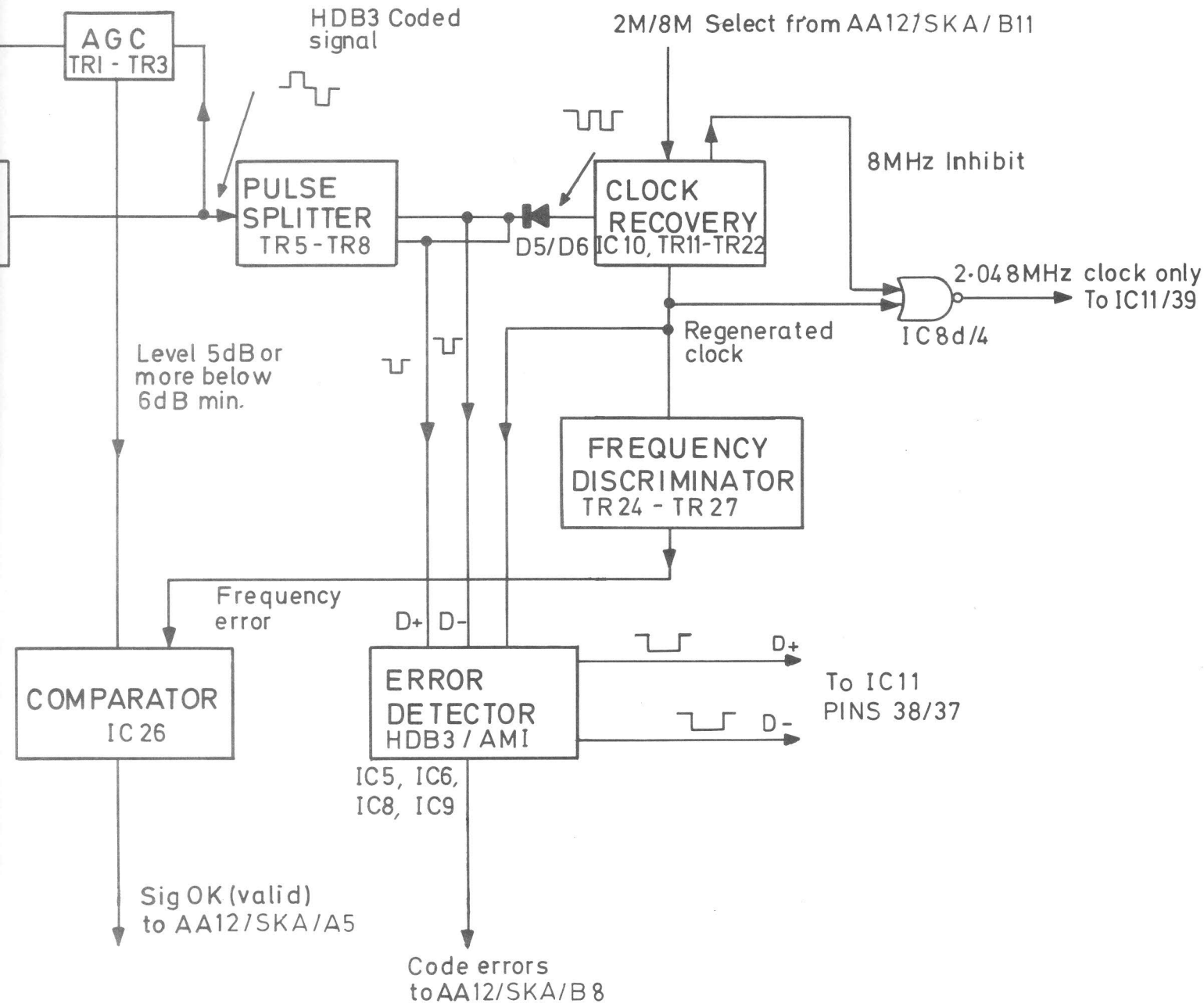
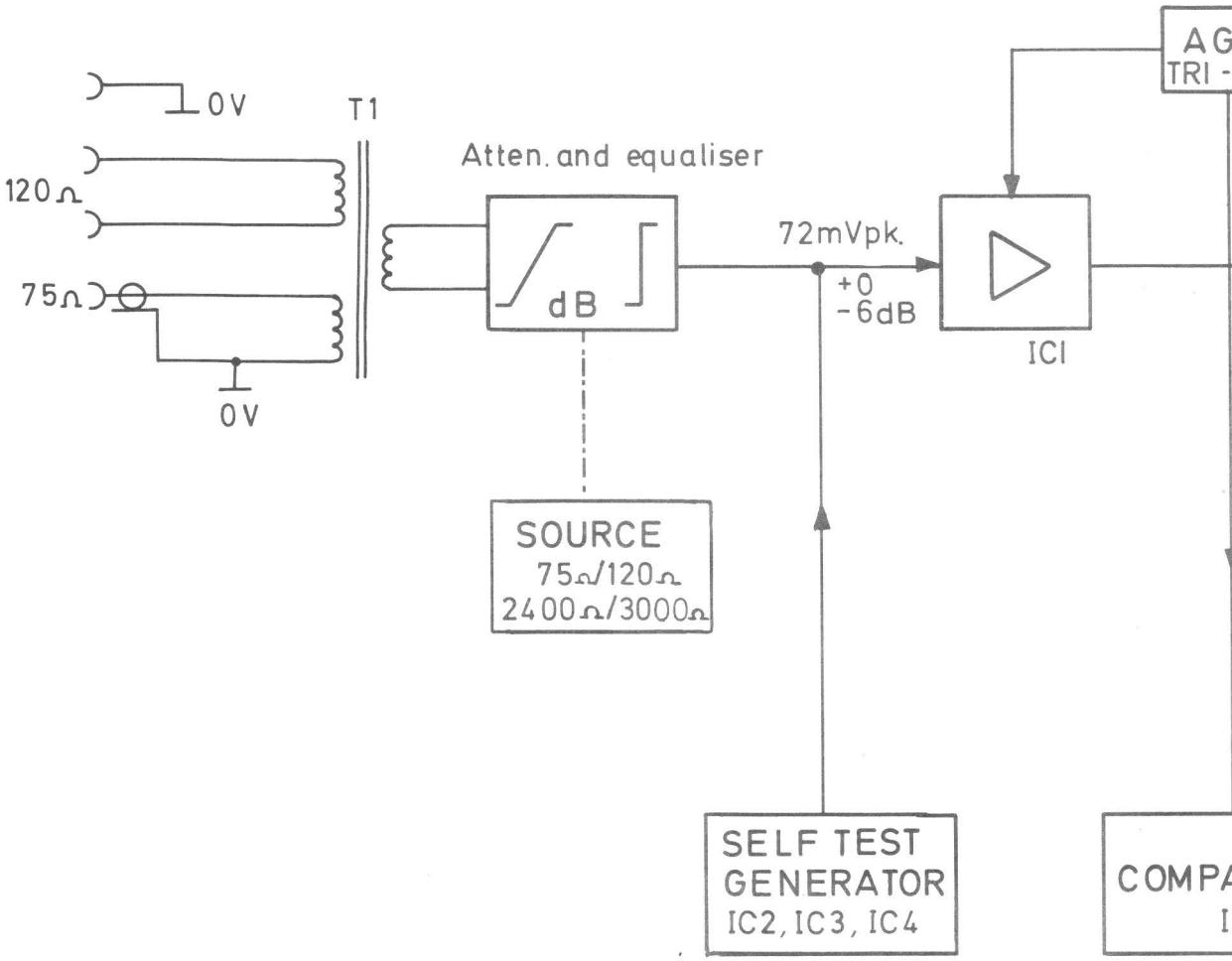


Fig. 3 Simplified overall block diagram of the 2833A



gram showing input section of AA3 board



TPC 4481

Fig. 4 Block diagram showi

POWER SUPPLY (on board AA3)

7. Power may be derived from either the a.c. mains supply or from an external 12 V battery. For a.c. mains operation, the supply is fed via a filter and a transformer to two separate full-wave rectifiers D19-22 and D23-26. Voltage regulators IC27 and IC28 provide two separate d.c. lines at +5 V. Voltage regulator circuit IC26a/3 and series transistor TR32 provide a +9 V d.c. line.

8. For d.c. operation, the supply is fed via voltage protection diodes D17 and D18, which bypass the full-wave rectifiers and feed the regulator inputs.

INPUT AND ALIGNMENT BOARD AA3

Block diagram Fig. 4 and circuit diagram Chap. 7, Fig. 2

9. The HDB3 or AMI encoded p.c.m. signal is applied to either of the two inputs of 75 Ω or 120 Ω. The signal is coupled via isolating/impedance matching transformer T1 and switch selected for terminating or monitoring modes by the SOURCE switches. The input impedance is set at 75 Ω by R1, R2 and R3. For terminating 75 Ω or 120 Ω inputs, R2 is switched in by the SOURCE 75/120 Ω switch as a series resistance, attenuating the signal by a factor of 33 providing a level of 72 mV peak at IC1 pin 1. For monitoring modes, external monitoring resistors attenuate the input signal and R2 is bypassed by selecting SOURCE 2400 Ω/3000 Ω.

AGC

10. The signal is amplified by wide-band amplifier IC1 and buffered by TR4. The level of the signal at TR4 emitter is held at 0.7 V pk by the action of the a.g.c. circuit consisting of TR1, TR2 and TR3. A d.c. average of the feedback voltage from TR4 emitter controls the gate voltage of TR1, varying the resistance between gain select pins 4 and 11 of IC1. By this means, the gain of IC1 is adjusted and compensates for signal level fluctuations within the range of +0 to -6 dB. If the signal begins to fall, the voltage at TR2 emitter begins to rise. This voltage is fed via D9 to comparator IC26. If however, the signal level falls by a total of 11 dB, TR2 emitter voltage rises to a threshold level causing IC26 to produce a high t.t.l. output level. The output of IC26 is routed to AA2 Processor board via SKA/A5.

11. The bipolar signal is separated into its positive and negative components by feeding differential amplifiers TR5, TR6, TR7 and TR8 via a resistor network and diode D4. TR5 is made to conduct more current by negative pulses at its base, producing positive pulses across R19. Positive pulses at the base of TR8 make it conduct less, increasing the conduction of TR7 which produces positive pulses across R21. The positive pulses are routed to the bases of TR9 and TR10.

Clock recovery

12. The positive pulses representing the positive and negative data components of the original p.c.m. signal, are converted to TTL levels by TR9 and TR10. The data is combined by D5 and D6 and fed to the two base inputs of IC10 transistors a/b. IC10 transistor pairs a/c and b/d are selectively turned on by TR11 and TR12. When 8M CODE is selected, a low level is applied to TR11 base from Processor board AA2, turning TR12 and IC10 transistors b/d on. This enables the negative pulse stream to pump the 8.448 MHz tuned

oscillator formed by L3 and C15. For 2M CODE, ALIGN and SIG modes a high level at TR11 base turns on IC10 transistors a/c which drive 2.048 MHz tuned oscillator L4,C16. The 8.448 MHz regenerated clock is phase shifted and restored to a more stable level by TR13, R40, C18 and TR15. The 2.048 MHz regenerated clock is phase shifted and restored to a more stable level by TR14, R41, C19 and TR16. Buffers TR17, TR18 and TR19 feed TTL converter TR20, TR21 and TR22.

Frequency discriminator

13. The regenerated clock is checked as a means of detecting an incorrect bit rate being applied at the 2833A input. Long tailed pair TR24 and TR25 a.c. coupled by C24 from R48 convert the sinusoidal regenerated clock to square wave. D8 and TR26 detect the amplitude of the negative pulses and bias TR27 to give a low output if the amplitude is low or a high output if the amplitude is high. A low amplitude indicates an unstable sinusoid, generated by an incorrect bit density driving one of the selected tuned circuits. The output from TR27 collector is routed to comparator IC26, which produces a high output to AA2, SKA/A5 when an incorrect bit density is detected.

HDB3/AMI error detector

14. This circuit detects line code errors in the 2 or 8M CODE modes. The separated data (negative pulses) are routed from the collectors of TR9 and TR10 to dual bistable IC5. Bistables IC5 and IC9 are clocked by the rising edge of the inverted regenerated clock coincident with the clocking of bistable IC6 by the negative edge of the non-inverted clock. IC5 extends the pulse periods of the data applied to its D inputs which are routed to IC11 via its Q outputs. By referring to the timing diagram Fig. 5, it can be seen that for two consecutive pulses of the same polarity of the D+ or D- input data, an AMI error is detected at outputs E or F. An HDB3 error is detected at outputs I or J.

15. Note. In AMI code, an error pulse is that pulse having the same polarity as the pulse preceding it. In HDB3 code, an error pulse is that pulse (not a violation pulse) having the same polarity as the pulse preceding it or a violation pulse having the same polarity as the violation pulse preceding it.

16. The detected errors are clocked through IC9 to remove unwanted glitches and routed to Processor board AA2, SKA/B8. The 2.048 MHz regenerated clock is routed to IC11 but inhibited by NOR gate IC8d when 8M CODE is selected. The 2.048 MHz or 8.448 MHz regenerated clock is also routed from NOR gate IC8a to AA2, SKA/B5.

Self test generator

17. This circuit generates a 2048 kbit/s bipolar signal with an error ratio of 1 in 10^5. The 2048 kbit/s self-test clock is generated by oscillator IC2a, L2, C21 and C22. By referring to Fig. 6 it can be seen that bistable IC3a and NOR gates IC2b, c and d produce a bipolar signal by the addition of outputs C and E across resistors R59 and R60. To attenuate the self test signal and set the voltage swing to vary around +5 V, the output is connected to the +5V line via R56.

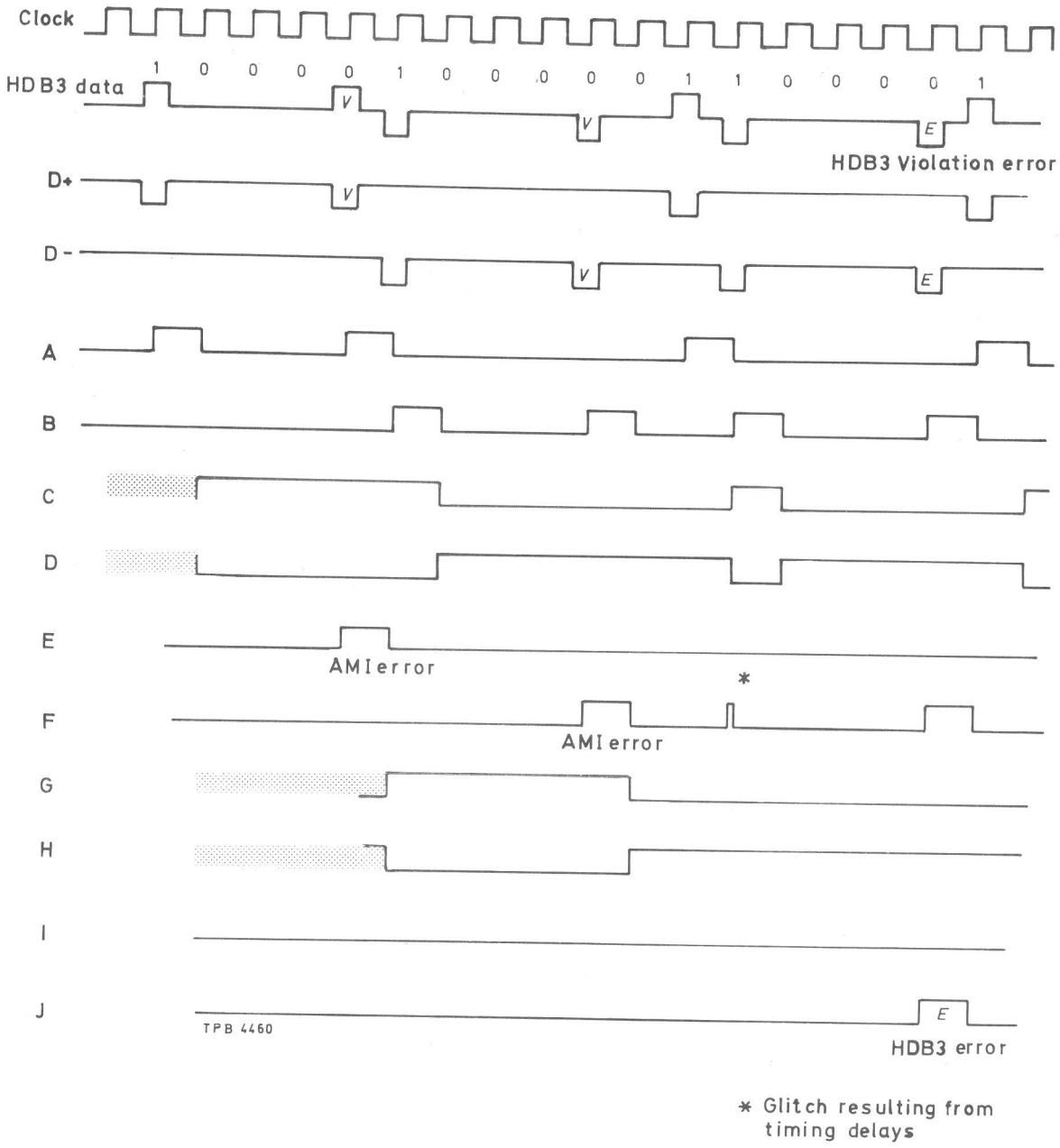


Fig. 5 Timing diagram for HDB3/AMI error detector

18. Errors are introduced into the bipolar signal by injecting pulses occurring at a 1 in 10^5 rate at SKA/B30. These pulses are inverted by TR23 and clock IC3b. Fig. 6 shows that when output G goes high IC3a is held at Reset, resulting in an extra positive pulse at C. This extra pulse always occurs in the same polarity and will therefore be detected by the HDB3/AMI error detector as a violation of the HDB and AMI code.

Frame alignment and frame word errors

Block diagram Fig. 7 and circuit diagram Chap. 7, Fig. 3

19. IC11 and IC12 are two mask programmed ULA (uncommitted logic array) integrated circuits. IC11 processes the data concerned mainly with the 2M ALIGN mode, and IC12 is concerned with data for the 2M SIG mode. Due to the complex nature of these circuits a simplified description will only be discussed.

20. The separated data pulses are clocked in with the 2.048 MHz regenerated clock on IC11 pins 37, 38 and 39 respectively. The data are HDB3 decoded before being processed for frame alignment and detection of AIS, FRAME and DISTANT alarms. The frame alignment word is checked for errors and corresponding output pulses are produced at pin 21. Unused bit 1 of the frame word and bits 1, 4 to 8 of the not-frame word are available as outputs from IC11 pins 26, 28 and 30 to 34 via SKB and the 15-way OUTPUTS socket on the rear panel.

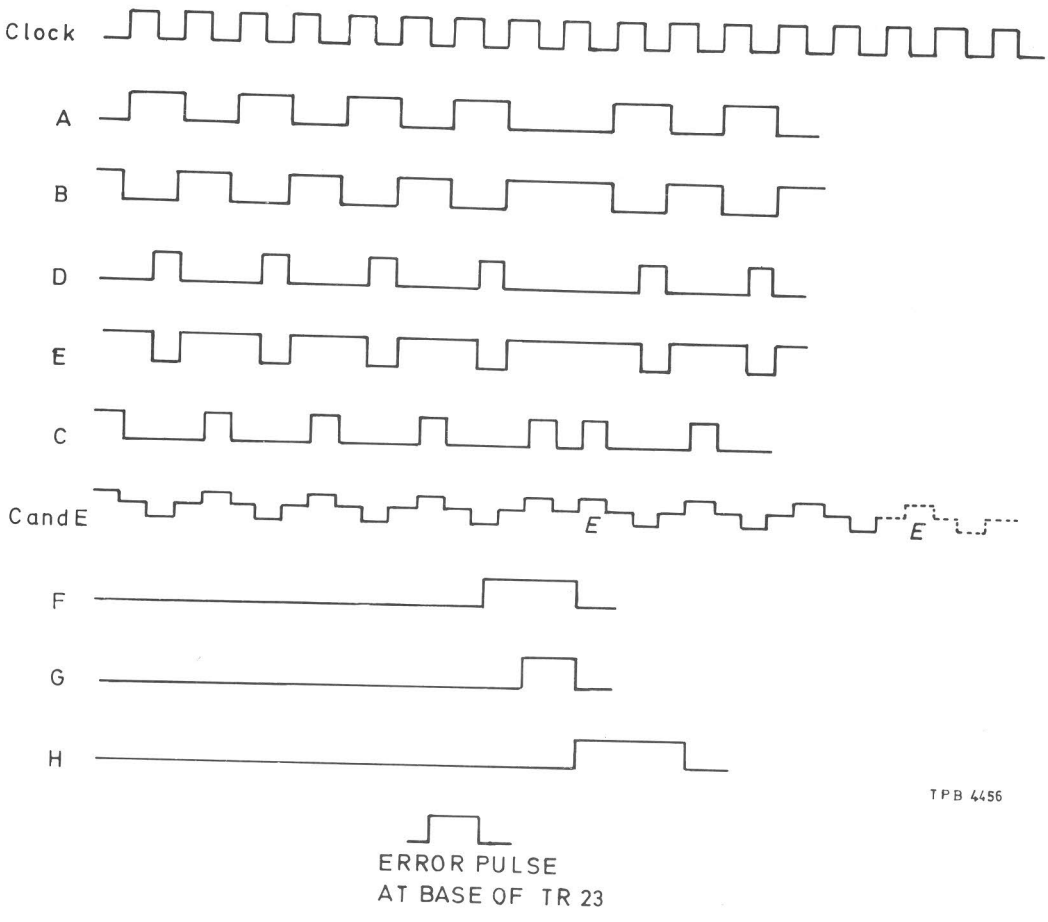
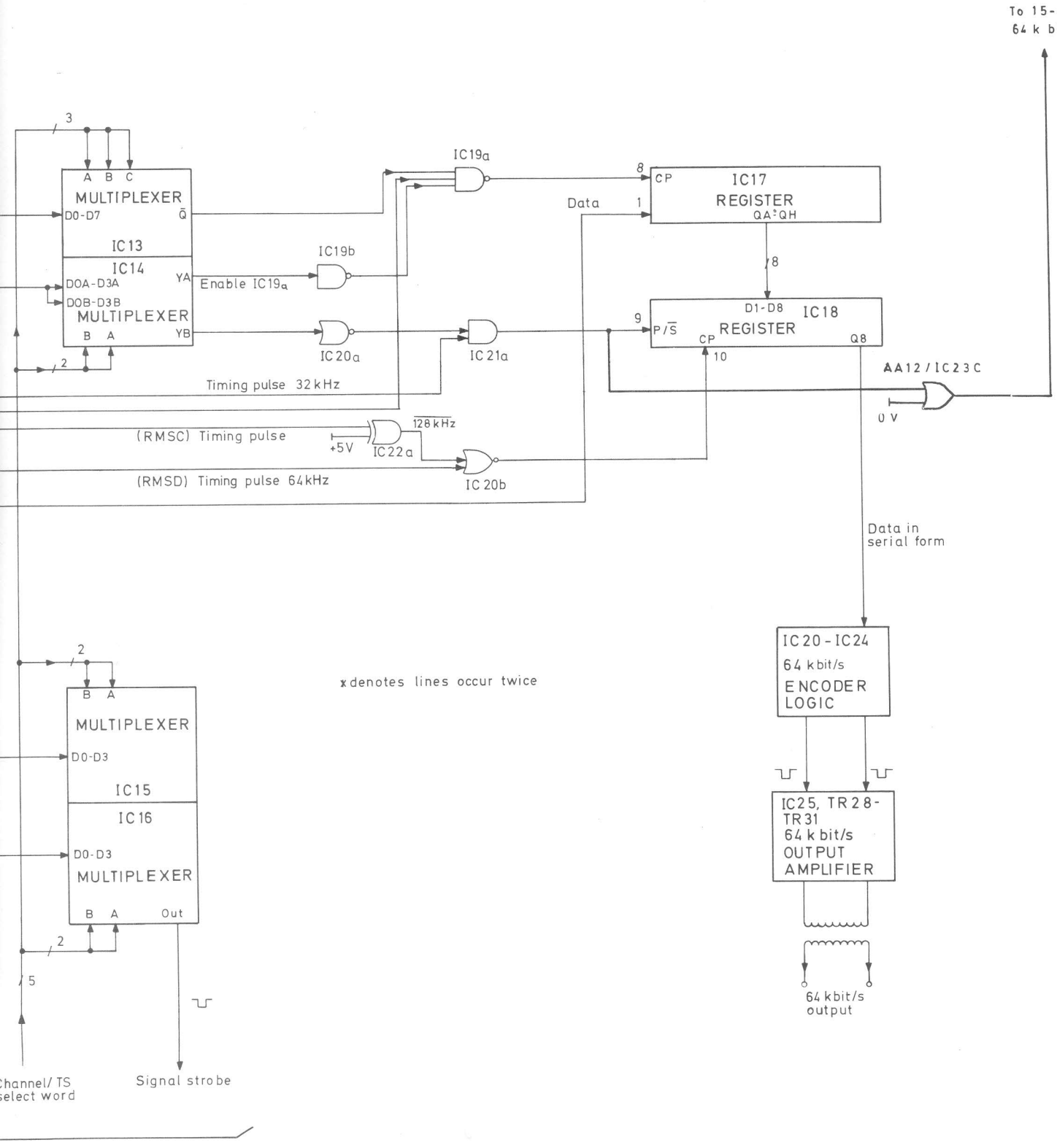


Fig. 6 Timing diagram of self-test generator



. 7 Block diagram showing alignment section of AA3 board

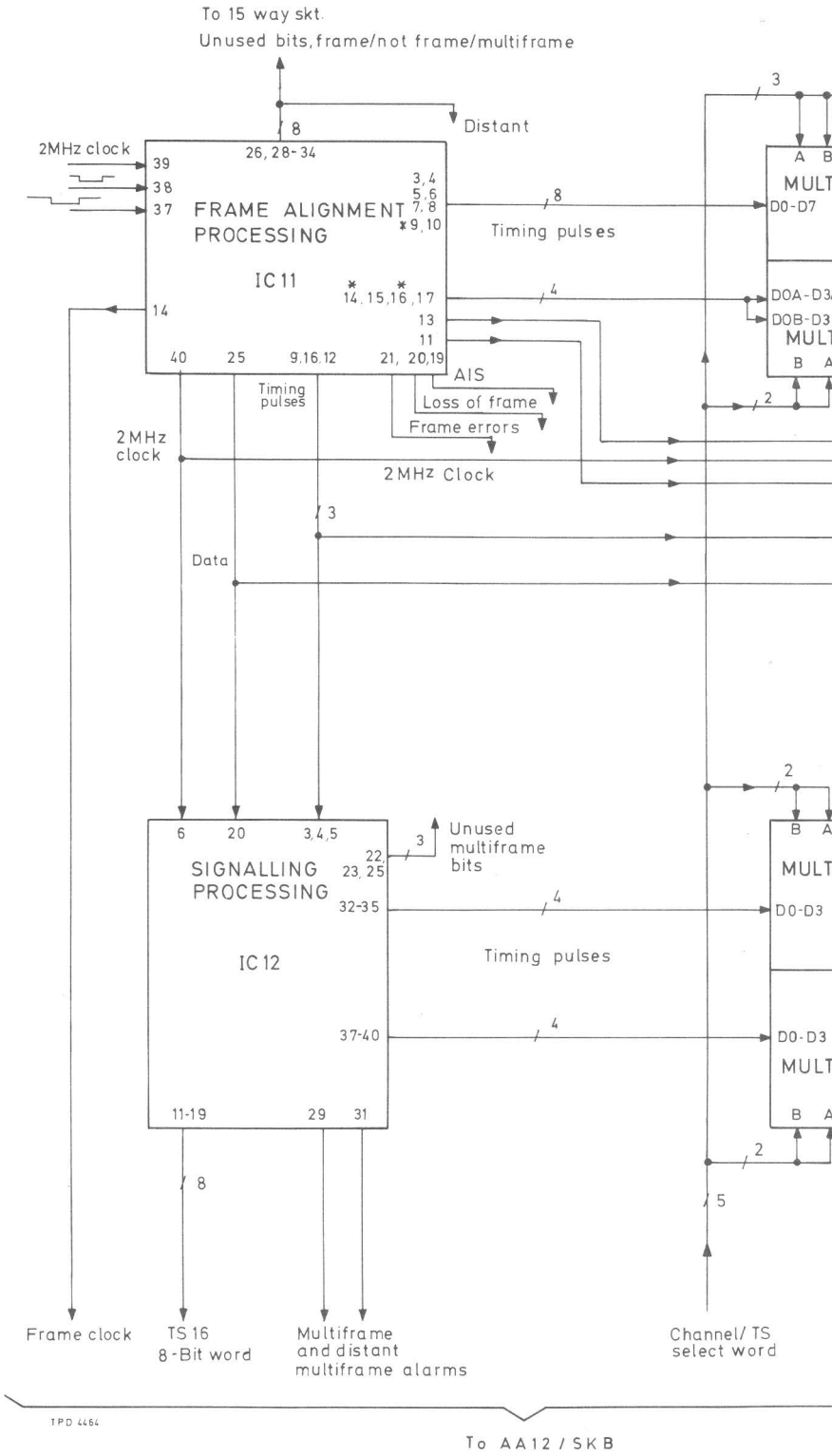

To 15 way skt.
Unused bits, frame/not frame/multiframe
Distant
8
26, 28-34
2MHz clock
39
38
37
FRAME ALIGNMENT PROCESSING
IC 11
3, 4
5, 6
7, 8
9, 10
14, 15, 16, 17
13
11
14
40
25
9, 16, 12
21, 20, 19
Timing pulses
AIS
Loss of frame
Frame errors
2MHz clock
2MHz Clock
Data
Timing pulses
3
4
2
Unused multiframe bits
6
20
3, 4, 5
22, 23, 25
SIGNALLING PROCESSING
IC 12
32-35
37-40
11-19
29
31
8
5
Frame clock
TS 16 8-Bit word
Multiframe and distant multiframe alarms
Channel/ TS select word
MULT
D0-D7
D0A-D3
D0B-D3
D0-D3
A B
B A
TPD 4464
To AA12 / SKB

Fig. 7 Bloc

21. The HDB3 decoded data and 2.048 MHz clock are routed to IC12 from IC11 pins 40 and 25 respectively. Timing signals generated by IC11 are routed to IC12 pins 3, 4 and 5. Multiframe alignment is achieved and associated alarms are detected, with alarm outputs representing MF and DMF from IC12 pins 29 and 31. Unused bits 5, 7 and 8 of the multiframe word are made available via the OUTPUTS socket on the rear panel. Some p.c.m. systems do not require MF and DMF alignment, in which case these alarm outputs may be inhibited by links.

Signalling code

22. In the 2M SIG mode the signalling code in Time-Slot 16 can be selected for any of the 30 channels in each frame. Timing pulses are generated by IC12 relating to the occurrence of Time-Slot 16 in each frame of the multiframe sequence and are present at IC12 pins 32 to 35 and 37 to 40. The timing signals are applied to D0-D3 inputs of multiplexers IC15 and IC16 and individually selected by the 2-bit word present at each of the data select inputs A and B on pins 10 and 11. When a particular channel is selected by the CHANNEL-TS switch, a 5 bit word from AA2 Processor board is present at SKA/A25 to A29. One of the four timing signals from IC12 pins 32 to 35 is selected by IC15 and at the same time, one of the four timing signals from IC12 pins 37 to 40 is selected by IC16. However the output of IC16 at pin 3 is inhibited when the selected timing signal of IC15 is high and internally routed to IC15/OUT, connected to INH (inhibit) of IC16. When IC15 timing pulse is low, IC16 timing pulse is routed to the OUT port, where it is buffered by exclusive OR gate IC22c and routed as the signalling strobe to AA2 via SKA/B27. The signalling strobe pulse when low, allows the two 4-bit signalling codes present on IC12 pins 11 to 14 and 16 to 19 to be latched into IC17 on AA2. The Processor board selects one of the two signalling codes that corresponds to the channel selected for decimal conversion and display.

Dialling errors

23. The detection of dialling errors relies entirely upon the operation of the software contained on board AA2. During a dialling sequence a succession of Signalling Codes 3 (circuit seized or inter dial break) and 11 (dial break) occur in TS16 of the selected channel. The signalling codes appear at the outputs of IC12 and are updated every 2 ms i.e. every multiframe. The Processor board counts the number of dial break pulses and inter-dial break pulses received, and compares the result against time masks relating to specific tolerances. If an error exists, the masks determine which error code is required for display. For a complete list of the possible errors, refer to Chap. 3, Table 2.

64 kbit/s encoding

24. When frame alignment has been attained, the information contained in each channel time-slot is converted to a 64 kbit/s co-directional signal and accessed via the rear panel. Timing signals relating to the time-slots in each frame are generated by IC11 and applied to the D inputs of multiplexers IC13 and IC14. When a time-slot is selected by the CHANNEL/TS switch, a 5-bit word from AA12 board on SKA/A25 to A29 is routed to data select pins A, B of IC14 and A, B, C of IC13. One of the 8 timing signals applied to the inputs of IC13 is selected and appears at its output $\overline{Q}$. At the same time, IC14 selects one of the 4 timing signals applied to its twin inputs which appear at outputs YA and YB respectively.

25. The two lines from IC13/$\overline{Q}$ and IC14/YA with the 2.048 MHz clock from IC11/40 are routed to NAND gate IC19a. When IC13/$\overline{Q}$ is low and the 2.048 MHz clock pulse is low, NAND gate IC19a is enabled when IC14/YA is high and inverted by NAND gate IC19b. The output of IC19a goes high at 0.244 µs intervals as the 2.048 MHz clock pulse goes low, and provides the clock pulse to the register IC17. The HDB3 decoded TS data from IC11/25 consists of a serial 8-bit word, where each bit has a duration of 0.244 µs. Therefore the TS data is serially clocked in to IC17 after eight clock pulses.

26. At half the frame period away from the selected time-slot, the timing signal at IC14/YB goes low, inverted by NOR gate IC20a and connected to AND gate IC21a. When timing signal RMSE from IC11/13 is high, IC21a output goes high and enables register IC18 to latch in the 8-bit data word in parallel form from IC17. This pulse is also routed to the 15-way outputs connector via SKB/10 for use as a synchronizing pulse for the 64 kbit/s data output. The data word is clocked out of IC18 in serial form to bistable IC23a by a 64 kHz clock pulse CP. The 64 kHz clock pulse is derived by inversion of a 128 kHz timing signal (RMSC) by exclusive OR gate IC22a and NOR gated by IC20b with a 64 kHz timing signal (RMSD) from IC11 pins 11 and 12 respectively.

27. The following description may be read in conjunction with timing diagram Fig. 8. Timing signals $\overline{\text{RMSC}}$ and RMSD designated A and B from exclusive-OR gate outputs IC22a and IC22b are routed to AND gates IC21b and IC21c. The time-slot data from IC23a/2 designated C and $\overline{Q}$ outputs are AND gated with signals A and $\overline{B}$ and NOR gated by IC20c. NOR gate IC20c selects $\overline{A}$ signal when C is low and $\overline{B}$ when C is high, producing signal D. The 64 kHz clock pulse CP is AND gated with D by IC21d producing E which clocks bistable IC23b. The outputs from IC23b of $\overline{Q}$ and Q (denoted by signal F) toggle when clocked by E and are OR gated with signal D by IC24a and IC24b. On the 8th clock pulse E, AND gate IC21a output goes high producing G which enables new data from the last frame to be latched into shift register IC18. The G pulse is exclusive OR gated by IC22d with output $\overline{Q}$ of IC23b and routed to the D input of IC23b. For either logic state of $\overline{Q}$, IC23b $\overline{Q}$ and Q outputs are prevented from changing on the next clock pulse E, thereby introducing the 8th bit violation in the 64 kbit/s encoded signal. When frame alignment has been lost, IC11/20 goes high and effectively disables NOR gates IC24a and IC24b by forcing both outputs to a high level.

64 kbit/s output

28. The 64 kbit/s co-directional signal pulses denoted by D1 and D2 at IC24a and IC24b outputs are routed to the bases of IC25 transistors d and e whose emitters are held at a constant level by the action of TR31 and potential divider R91 to R94. TR28 and TR29 are arranged to be balanced by the base bias circuit of R87, R88, D12, D13, R90 and TR30 whose base bias voltage is set by preset R92. When D1 pulse is low D2 level is high, IC25/TRd switches off, causing TR29 to conduct more current through T2 primary to earth via current mirror IC25/TRb. Similarly when D2 pulse is low, D1 pulse is high, switching on IC25/TRd and turning IC25/TRe off. TR28 conducts more current in the opposite direction through T2 primary to earth via current mirror IC25/TRc. The secondary of T2 is connected to two output connectors on the rear panel.

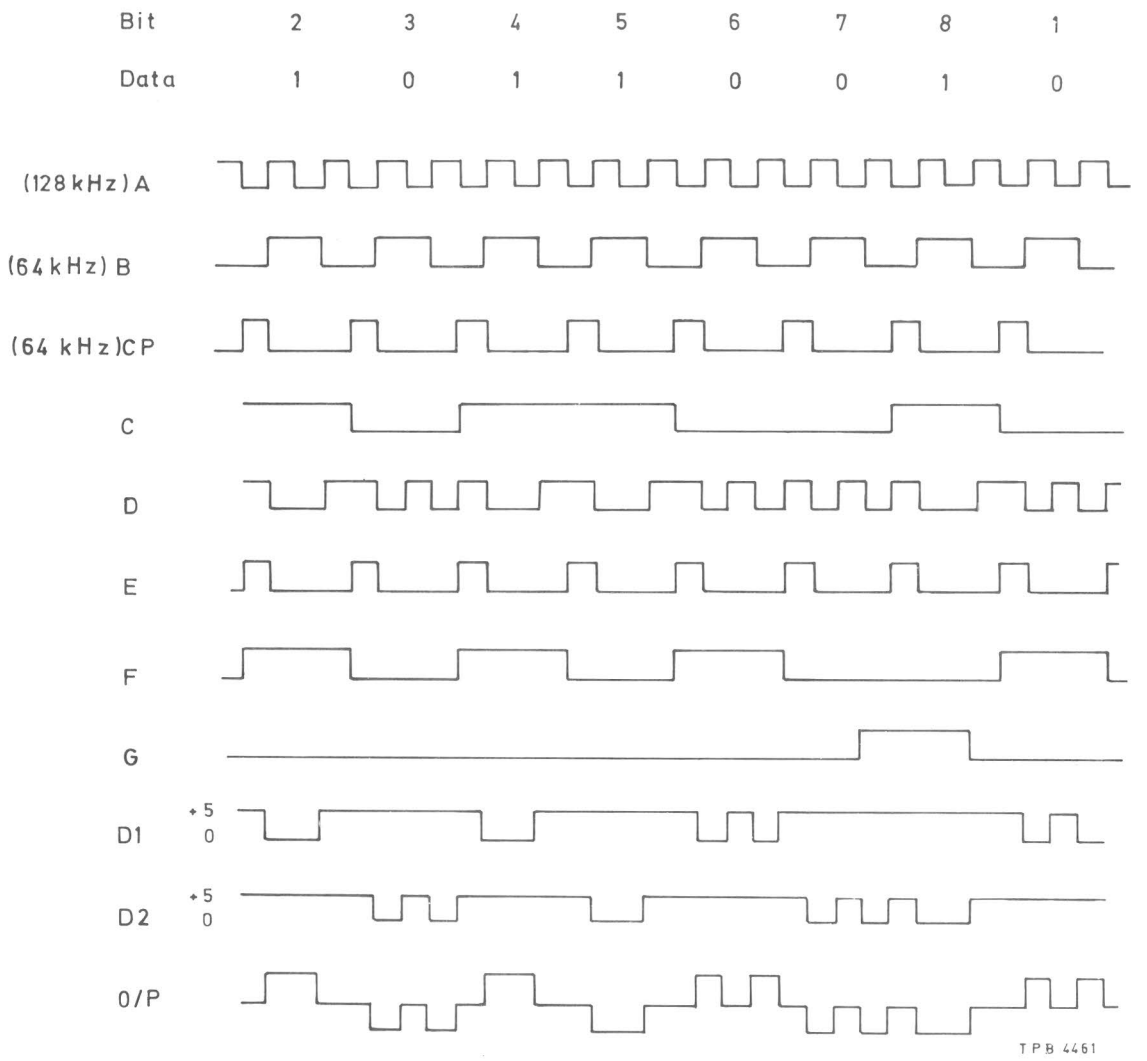


Fig. 8 Timing diagram for 64 kbit/s encoder on AA3 board

Note. Code conversion rules; Step 1 : A 64 kbit/s bit period is divided into four unit intervals.

Step 2 : A binary one is coded as a block of the following four bits : 1100.

Step 3 : A binary zero is coded as a block of the following four bits : 1010.

Step 4 : The binary signal is converted into a three-level signal by alternating the polarity of consecutive blocks.

Step 5 : The alternation in polarity of the blocks is violated every 8th block. The violation block marks the last bit in an octet.

PROCESSOR BOARD AA12

Introduction

29. The overall operation of the 2833A is controlled by AA12 board which contains an 8085A processor, Program memory EPROM, Programmable Error Counter with RAM, Programmable Peripheral Interface (PPI) and driver stages for the display, printer and pen recorder.

Processor

30. The internal clock generator of processor IC1 operates at a clock frequency of 2.4576 MHz derived from a 4.9152 MHz crystal oscillator XL1 via inputs X1 and X2.

31. IC1 HOLD, SID, TRAP, INTR and RST 5.5 are held low and READY is held high via R38.

Reset circuit

32. At power on, IC1 is reset by supply voltage supervisor IC21. A timer within IC21 delays the reset inactive state to ensure the processor and other periphery circuits have time to reset. This delay is set by the value of C1 and is approx. 60 ms.

33. IC21 also monitors the +5 V supply line and will activate a reset if the supply level falls to +4.75 V and maintains the reset until the supply voltage returns to the correct level. This prevents loss or corruption of data in the registers of the processor or other periphery devices. Periphery devices are reset via IC1 RESET OUT.

Address bus

34. IC1 Address/Data lines AD0 to AD7 provide a common 8-bit address bus via address latch IC3. The address is latched onto the output of IC3 on the negative edge of ALE inverted from a positive edge by NAND gate inverter IC18a.

35. IC1 address ports A8 to A12 provide the high 5-bit address to 8k x 8 EPROM IC5. Address ports A13 to A15 provide a 3-bit address to 3 to 8 line decoder IC4 for the selective enabling of peripheral devices.

Data bus

36. An 8-bit bi-directional data bus is provided via ports AD0 to AD7 when the processor is in non-address mode.

Control bus

37. The control bus comprises outputs RDL (Read), WR L (Write), ALE (Address Latch Enable) and IO/(M L) (Input Output/Memory).

Program and working store

38. Program data is permanently stored in an 8k x 8 EPROM IC5 and is addressed via IC1 ports AD0 to AD12. IC5 is read when its CE L (Chip Enable) and RD L inputs are both low. A working store is provided by the 256 x 8 RAM in the Error Counter/Timer IC7.

PPI

39. Programmable Peripheral Interface device IC16 has three ports A, B and C which interface AA12 with AA3 board. Each port is set to be in input or output mode by the processor via the 8-bit data bus, 2-bit address and the control bus.

Port functions

40. In 2M ALIGN and 2M SIG mode, Ports A0 to A4 respectively output a Time slot or Channel select 5-bit address to AA3 via SKA. The 5-bit address is incremented or decremented in value for the duration that key SA is held depressed.

41. Port A5 drives the buzzer X7. Port A7 provides a timing pulse output to counter IC12 described under the heading 'Error count and timing'.

42. Port A6 outputs the ERRORS alarm. This alarm is activated by the processor when it decides the error ratio has exceeded 1 in 10^5. To aid faster software operation Port A6 is read via input port C3.

43. The SIGNAL L line from IC26/AA3 is routed to Port C0. When the 2833A INPUT signal level is at the correct amplitude and bit rate, SIGNAL L is low. IC1/AA3 activates the SIGNAL 1.e.d. via Display board AA1 and if enabled by the BUZZER ON and BUZZ SIGNAL switch lines the buzzer is activated via PA5. If the 2833A INPUT signal level goes too low or has an incorrect bit rate, SIGNAL L goes high. The processor responds by extinguishing the SIGNAL 1.e.d. (and BUZZER if selected) and if the 2833A is in either 2M ALIGN or 2M SIG modes illuminates the LINE alarm 1.e.d. via Display board AA1.

44. Ports C1, C2 and C4 to C6 are input ports for the Alarm lines from AA3. All Alarm lines and SIGNAL L are also routed to OR gates IC2a and b and to the ALARMS OUTPUT connector on the rear panel via output buffer OR gate IC19d.

45. Port B0 is not used and held at 0 V by pull down resistor R48d. Ports B1 and B3 to B7 are inputs from keys LAMPLOCK/AUTO RESET, BUZZER SIGNAL/ ERRORS, BUZZER ON, FUNCTION UP/DOWN and LAMP TEST.

Signalling word latch

46. In 2M SIG mode, the 8-bit signalling code from IC12 on AA3 is latched into 8-bit latch IC17 when signal strobe pulse at IC17/11 is low and read out when RD L and IC4/Y6 are both low. The strobe pulse is also routed to IC1/ RST 7.5 which informs the processor a new signalling code is available. When requested to be read by IC1, the signalling code is placed onto the data bus.

Error count and timing

47. The external count input, detected code errors, frame errors, regenerated clock, frame clock from AA3 and the AA12 processor clock are routed to 8 to 2 multiplexer IC14 on AA12. These inputs are selected by control inputs A and B from Ports C3 and C4 of IC7.

2M and 8M CODE

48. In 2M or 8M CODE modes the line code error pulses and regenerated clock are selected on to IC14 output pins 9 and 7 respectively. The clock signal is divided by 10 by counter IC13b and routed to IC7 CLK IN via inverter NAND gate IC18d. IC7 is programmed via the data bus to divide the clock signal by 1×10^4 producing a TIMER PULSE at pin 6 every 1×10^5 regenerated clock pulses. This pulse is used as a timing pulse for the self-test generator circuit on AA3 and is routed back to AA12 via SKA/30.

49. Code errors are routed to input pin 15 of divide by 10 counter IC13a and to the ERRORS OUTPUT via output buffer OR gate IC23b. The QD output of IC13a is connected to divide by 1×10^3 counter/latch IC12 clock via OR gate IC20.

50. On the rising edge of the TIMER PULSE the least significant 4-bit b.c.d. number of the code error count present at outputs QA to QD of IC13a is latched into IC7 Ports A0 to A3. At the same time the TIMER PULSE on IC12 latch enable input causes its 3-digit count to be internally latched. Both IC13a and IC12 counters are reset by the delayed TIMER PULSE from the Q outputs of monostables IC11a and IC11b applied to IC13a/CLR and IC12/MR inputs respectively. If the number of errors exceeds the capabilities of the counter, any further clock pulses are inhibited by the routeing of IC12 overflow output to the input of OR gate IC20 which holds IC12 clock input high.

51. The TIMER PULSE is read by IC7 Port C2 and routed via Port C0 to the RST 6.5 interrupt of IC1. This informs the procesor that count data is available. In response to the interrupt, IC1 addresses IC7 Port A latch in order to read the LSB count. IC1 reads the data via address/data lines D0 - D7 and stores it in IC7 RAM. IC1 then reads the next error count digit from IC12 by addressing IC7 Port B. The two remaining more significant count digits are stored in latches within IC12. A latched count is read out by making IC12 C1A high from IC16 Port A7.

52. For error ratio measurements, the processor compares the total number of errors counted with up to 1×10^8 regenerated clock pulses. If the error rate is high the period is limited to 1×10^6 regenerated clock pulses. This is implemented by totalizing the error count over a period of ten 1×10^5 or one hundred 1×10^5 TIMER pulses depending on the signal error rate. The error count is stored in IC7 RAM. At the end of the timing period, IC7 asserts interrupt RST 6.5 and in response the processor reads the total count. The error ratio is displayed when SB1 key is depressed.

2M ALIGN

53. In 2M ALIGN mode, multiplexer IC14 selects the frame alignment word error pulses and the regenerated frame clock onto IC14 output pins 9 and 7 respectively. The error count is identical in operation to line code errors except timer IC7 is programmed to divide the frame clock by 112, producing TIMER PULSES every 1120 regenerated clock pulses. The TIMER PULSES produced every 2240 regenerated clock pulses are used for measuring frame word error ratio on the assumption that errors occur in a random manner and follow a Poisson distribution. The TIMER PULSES produced every 1120 regenerated clock pulses are used for software operation in Error Free Seconds mode. Note that the Frame Alignment Word occurs every other frame and frame clock is at frame frequency.

EXT COUNT

54. In EXT COUNT mode, multiplexer IC14 selects the external count pulses from TR33 on AA3 and the processorclock from IC1 onto IC14 output pins 9 and 7 respectively. The processor clock is used to drive the timing chain and errors are counted and totalized as for 2M and 8M CODE modes.

Printer driver

55. This circuit comprises a USART Programmable Communication Interface IC26 for generating serial data, a Baud rate generator using a dual 4-bit binary counter IC22 and 1 of 8 multiplexer IC24, and an 8-line buffer IC25 which interfaces the data bus with the output function switches on the rear panel.

56. Before data transmission the 8-bit word on IC25 outputs Y0 to Y7 representing the function switch settings is read by IC1 and determines the control data format sent by the processor to the USART.

USART

57. The USART Read/Write operation is controlled by the WR L, RD L, RESET and C/(D L) inputs. When control data is to be written or read, the C/(D L) (Control/Data) input controlled via Address A0 goes high. For Transmit data C/(D L) goes low. USART internal timing is derived from the processor clock of 2.4576 MHz.

Modem control

58. The modem operation is controlled by three inputs and one output via the RS-232-C connector; DSR (Data Set Ready), inverted to DSR L via NAND gate IC28b, CTS (Clear to Send), inverted to CTS L via NAND gate IC28c, CD (Carrier detect)/RLSD (Received line signal detect) inverted by IC28a to CD L/RSD L and RTS L (Request to Send) inverted to RTS via NAND gate IC27b respectively.

59. The transmitter clock (Tx C L) controls the rate at which a data character is to be transmitted and is derived from the processor clock via dual 4-bit binary counter IC22 and 1 of 8 multiplexer IC24. IC22 sequentially divides the processor clock by 4, 16, 32 and 64 giving four separate outputs of 614.4 kHz, 153.6 kHz, 76.8 kHz and 38.4 kHz respectively.

60. To facilitate baud rates of 9600, 1200, 600 and 300, multiplexer IC24 routes the appropriate count output from counter IC22 to the transmitter clock input. A count input is selected by a 2-bit word set by the two Baud Rate switches on the rear panel. Table 1 shows the clock selected for each baud rate and selection word.

TABLE 1 TRANSMITTER CLOCK SELECTION

BAUD RATE	*TRANSMITTER CLOCK FREQUENCY*	*IC24 COUNT SELECT WORD*	
		A	*B*
300	38.4 kHz	0	0
600	76.8 kHz	1	0
1200	153.6 kHz	0	1
9600	614.4 kHz	1	1

61. Finally, the transmitted serial data stream from IC26 Tx D comprises a data character preceded by an automatically inserted start bit and followed by a programmed number of stop bits.

Pen recorder driver

62. Pen recorder data is transferred via the data bus to 4-bit latch IC8 and clocked out when WR L and IC4/Y4 are both low. The Q outputs of IC8 are connected to the non-inverting input of op-amp. IC15 via a resistor or resistors (R19 to R25) whose effective resistance determines the amount of current through and consequently volts drop across R18 when a Q output goes low. The voltage developed across the resistor network and via IC15 determines the bias voltage between base and emitter of TR3 which correspondingly determines the amount of charging current through C16. The maximum (f.s.d.) current is determined by series resistors R9, R10 or R29, R32 depending on which group is in circuit via link LK x. Preset R29 sets the f.s.d. current to 1 mA and preset R10 sets the f.s.d. current to 5 mA. Lines A14 to A17 are used for test purposes.

Display drive

63. Display driver multiplexer IC9, provides a multiplexed drive to the Display board AA1 via SKB and a 25-way flexible wire connector. IC9 is connected to the data bus via 8-data lines ID0 - ID7, with 2 lines from the control bus to $\overline{WR}$ and MODE at pins 8 and 9 respectively. Before data from the processor can be displayed, a 4-bit control word is applied to inputs ID4 to ID7 when $\overline{WR}$ is low and MODE is high. The control word indicates to the multiplexer that display data will follow to be stored in the 8 x 8 RAM store in IC9. For this particular design configuration the control word is required to be high at ID4, ID5 and ID7 (ID6 may be either). Once the control word has been read by IC9 a 7-bit display data word is written into the 8 x 8 RAM contained in IC9 when $\overline{WR}$ and MODE are both low. The display data is updated and read eight times into the RAM locations where it is stored before being multiplexed out to the display. Fig. 9a shows the control word, information contained in the display data word and the relationship between the

data input and output pins. It can be seen that the 7-bit display data word is divided into smaller data words which, when read out are drive signals for specific destinations on the Display board AA1. Each byte is read out with a self generated strobe pulse from IC9/D0-D7 separated by an inter-digit blanking pulse. The strobe pulses sequentially enable the cathodes of each display digit, overflow and alarms LEDs and indirectly enable SIGNAL and (IN10) LEDs (see Fig. 9b).

64. The 8-bit latch and decoder IC10 is connected via 8 data lines D0 - D7 to the data bus. When a particular FUNCTION is selected, a 5-bit word from IC1 is latched in at D0 - D4 when IC10/CK input is low. The clock pulse is derived from the output of OR gate IC19, enabling data to be latched only when $\overline{WR}$ and IC4/Y5 lines are both low. The Q outputs of IC10 are routed via current limiting resistors R11 and R15 and connector SKB to drive the cathodes of the FUNCTION display LEDs on AA1. Because only one FUNCTION LED is on at any one time, only one of the five Q outputs is active i.e. logic 0.

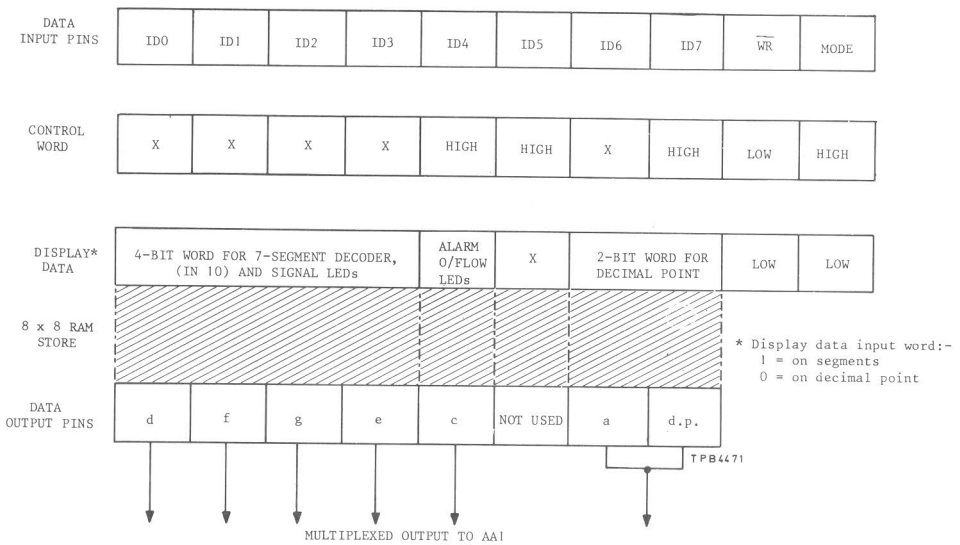


Fig. 9a AA12/IC9 display data and control word

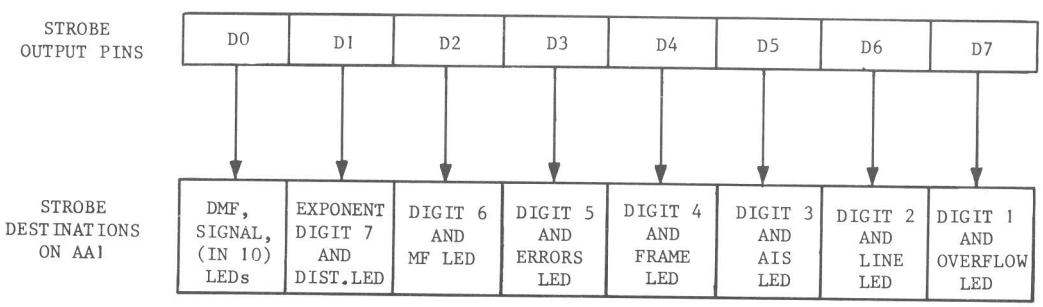


Fig. 9b AA12/IC9 strobe output destinations

DISPLAY BOARD AA1

Circuit diagram : Chap. 7, Fig. 5

65. The display drive and enable lines are routed from AA2/SKB to connector LK1 on AA1 via the 25-way flexible wire connector. The 4-bit BCD word routed to LK1/20-23 is decoded by IC1 providing 7 common multiplexed drive lines a-g to the 7 segments in each of the 7 digit displays. Two bits of the 4-bit word input to IC1 also provide enable lines to TR1 and TR2 via resistors R8 and R9 respectively. When turned on, TR1 and TR2 enable the (IN10) display D22 and SIGNAL LED D15 by connecting their cathodes to earth. The anodes of the OVERFLOW and ALARM LEDs D8 - D14 and D16 are connected to a common drive line from LK1/25. The OVERFLOW, ALARMS and digit LEDs are enabled by strobe lines from LK1/10-17 which are connected to their cathodes. The strobe line from LK1/10 is also routed to the base of TR3 via R5. When TR3 is strobed, it allows a +5 V supply line to feed current to the anodes of the SIGNAL and (IN10) LEDs which are turned on when enabled by the action of TR1 and TR2 mentioned above. The FUNCTION LEDs D17 - D21 are enabled by a logic 0 on one of the five lines connected to their cathodes from LK1/1-5.

RS-232-C BOARD AR1

Circuit diagram : Chap. 7, Fig.

66. This board interconnects the printer driver on AA12 board with the RS-232-C connector PLA on the instrument rear panel via AA12/PLB and AR1/FLA.

67. The printer driver output lines comprise Tx D, DTR and RTS. External handshake control to the printer driver on AA12 is routed via the RS-232-C connector on lines DTR, CTS, DSR and CD.

68. The remaining inputs to the printer driver are individually controlled by the 7-bit function switch SA.

Chapter 5

MAINTENANCE

CONTENTS

INTRODUCTION

1. This chapter contains information for checking the instrument's overall performance, and to assist in fault finding and repairing the instrument. For these purposes this chapter should be read in conjunction with the Technical Description, Chap. 4, and the Circuit Diagrams, Chap. 7.

2. Integrated circuits and semiconductor devices are used throughout this instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reversed polarity and excessive heat or radiation. Avoid hazards such as prolonged soldering, strong r.f. fields or other forms of radiation and the use of insulation testers.

Note...

Static sensitive components are marked with the symbol ⚠ in this equipment. These devices can be damaged by an accumulation of static charge. Follow the instructions given in Notes and Cautions on page (iv).

3. In case of difficulties which cannot be resolved with the aid of this book, please contact our Service Division at the address given inside the rear cover, or your nearest Marconi Instruments' representative. Always quote the type and serial number found on the data plate at the rear of the instrument.

PERFORMANCE TESTS

4. Test procedures described in this chapter may be simplified and of restricted range compared with those that relate to the generally more comprehensive factory test facilities which are necessary to demonstrate complete compliance with the specifications.

5. Performance limits quoted are for guidance and should not be taken as guaranteed performance specifications unless they are also quoted in the Performance Data in Chap. 1.

6. When making tests to verify that the instrument meets the stated performance limits, allowance must always be made for the uncertainty of the test equipment used.

TEST EQUIPMENT

7. The test equipment required for the maintenance and repair of the instrument is listed below. Where a specific instrument is not essential, the general requirements are described.

Item	*Description*
a	Word generator capable of providing a p.c.m. pattern at bit rates of 2.048 Mbit/s and 8.448 Mbit/s at error rates of 1 in 10^3, 1 in 10^4, 1 in 10^5 and 1 in 10^6. The errors must be in the form of bipolar violations.
b	Pattern generator capable of operating at a bit rate of 8.448 Mbit/s and 2.048 Mbit/s, e.g. TF 2808/1.
c	Pattern generator capable of operating at a bit rate of 1.536 Mbit/s and 2.048 Mbit/s, e.g. TF 2802/2.
d	Jittered clock generator capable of providing a signal with jitter of up to 1.5 bits peak-to-peak at 2 kHz for 2.048 Mbit/s and 8.45 kHz for 8.448 Mbit/s rates.

Item	*Description*
e	75 Ω attenuator covering 0 - 50 dB and suitable for use at frequencies up to 50 MHz e.g. TF 1073A/2S.
f	75 Ω/120 Ω Balun transformer suitable for use in the frequency range 50 kHz - 10 MHz.
g	TTL pulse generator e.g. Logic Pulser HP 546A.
h	Return loss measuring set for 75 Ω coaxial circuits capable of measuring return loss ratio up to and above 20 dB at frequencies up to 12 MHz and 120 Ω balanced circuit capable of measuring return loss ratio up to and above 20 dB at frequencies up to 3 MHz.
i	Signal generator covering 40 kHz to 12 MHz providing an output level of at least 200 mV, e.g. TF 2016A.
j	Video voltmeter with a voltage range of 1 mV f.s.d. to 10 V f.s.d. and suitable for use at frequencies up to 3 MHz e.g. TF 2600B.
k	Digital Simulator TF 2828A.
l	Multimeter with a d.c. current range down to at least 0.01 mA e.g. FET Multimeter TF 2650.
m	Dual trace measuring oscilloscope with a sensitivity of at least 10 mV/cm and suitable for use at frequencies up to 50 MHz.
n	RF voltmeter and probe with a voltage range of 1 mV to 1 V r.m.s. f.s.d. and suitable for use at frequencies up to 12 MHz e.g. TF 2603.
o	Summing amplifier for use in noise immunity test.
p	White noise generator for use in noise immunity test.
q	Mixer for interference immunity test.
r	Filters simulating near end crosstalk response for 2.048 Mbit/s and 8.448 Mbit/s signal rates.
s	Stopwatch or Timer.
t	75 Ω to 50 Ω pad.
u	75 Ω return loss probe.
v	120 Ω return loss probe.

2M CODE

Test equipment : items a,b,c,d,e,f,k and s.

8. The following tests check line code error measurements and the associated functional controls.

Checking error ratio

(1) Select 2M CODE and connect the output of the word generator to the 75 Ω INPUT of the 2833A. Set the 2833A controls to SOURCE 75 Ω and ERRORS-RATIO.

(2) Set the word generator to 2.048 Mbit/s and error ratio to 1 in 10^6. Check 1 in 10^6 is displayed by the 2833A.

(3) Check the 2833A displays the following error ratios when selected on the word generator; 1 in 10^5, 1 in 10^4 and 1 in 10^3.

Checking error totalization and associated controls

(4) Set the 2833A to ERRORS-TOTAL and the word generator to an error ratio of 1 in 10^3. Check the 2833A display is totalizing.

(5) Set the 2833A to ERRORS-RESET. Using a stopwatch or timer, check after a 10 second period, the display reading is within ±1% of 20480.

(6) Check the 2833A totalizing display can be discontinued by selecting ERRORS-STOP and continued by selecting ERRORS-CONT.

Overflow

(7) Set the word generator to the highest error ratio position and check the 2833A display reaches 999999, resets to zero and activates the OVERFLOW LED which should stay illuminated as the count recommences. Reset the OVERFLOW LED by selecting ERRORS-RESET.

Buzzer test

(8) Select 2833A BUZZER-ERROR and check that an audible alarm indicates errors detected in either ERRORS-TOTAL or RATIO modes.

9. The following tests check frequency discrimination, jitter and signal level operation.

Frequency discrimination

(1) Connect a p.c.m. pattern generator with a 1.536 and 8.448 Mbit/s bit rate capability to the 75 Ω INPUT of the 2833A.

(2) Set the output of the p.c.m. pattern generator to 1.536 Mbit/s. If the TF 2808/1 pattern generator is used, connect the SEND 75 Ω output

to the 75 Ω INPUT of the 2833A and set the controls of the TF 2808/1 as follows :

MODE	:	SEND
BIT RATE	:	LOWER (1.536 Mbit/s if available)
FORMAT	:	HDB3
BINARY PATTERN	:	PSEUDO-RANDOM
ERROR INJECTION	:	OFF

(3) If the TF 2802/2 pattern generator is used, connect the 75 Ω PATTERN OUTPUT to the 75 Ω INPUT of the 2833A and set the controls of the 2802/2 as follows:

BIT RATE	:	1.536 Mbit/s
PATTERN	:	HDB3 PSEUDO-RANDOM

(4) Check the display and SIGNAL LED on the 2833A are no longer illuminated which indicates that an incorrect bit-rate p.c.m. signal is present.

(5) Repeat the above steps with the p.c.m. pattern generator bit-rate set to 8.448 Mbit/s.

Jitter test (This test can be omitted if a jittered clock generator is not available).

(6) Connect the OUTPUT of the jittered clock generator to the 75 Ω INPUT of the 2833A and set to 1.5 bits peak-to-peak jitter at 1 kHz.

(7) Check no errors or alarms are indicated on the 2833A display.

Signal level

75 Ω input

(8) Connect the equipment as shown in Fig. 1.

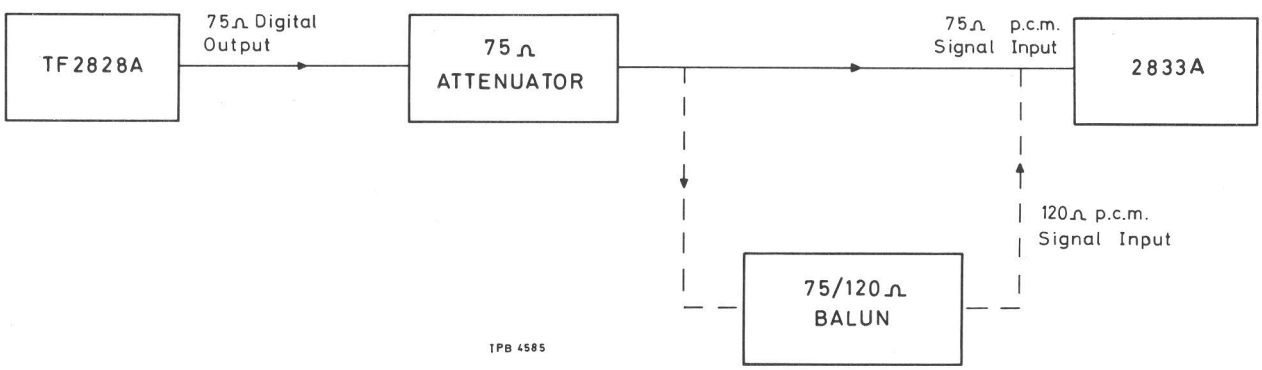


Fig. 1 Signal levels test

(9) Set the controls of the TF 2828A as follows :

CONTROL : Mode 1
DIGITAL OUTPUT : 75 Ω and 6 dB loss
ALL CHANNELS SELECTED

(10) Set the attenuator to 0 dB and check the 2833A display and SIGNAL LED are illuminated.

(11) Increase the attenuation until the display or SIGNAL LED are no longer illuminated on the 2833A and note the attenuation. The attenuator should not read higher than 5 dB.

120 Ω input

(12) Repeat steps (10) and (11) with the 75 Ω to 120 Ω Balun connected between the 75 Ω attenuator and the 120 Ω INPUT of the 2833A. Select SOURCE 120 Ω on the 2833A. The attenuator should not read higher than 5 dB.

8M CODE

Test equipment : items a,b,c,d,e,f and s.

10. The following line code error tests can be made if a word generator capable of operating at an 8.448 Mbit/s rate is available.

Checking error ratio

(1) Select 8M CODE and connect the output of the word generator to the 75 Ω INPUT of the 2833A. Set the 2833A controls to SOURCE 75 Ω and ERRORS-RATIO.

(2) Set the word generator to 8.448 Mbit/s and error ratio to 1 in 10^6. Check 1 in 10^6 is displayed by the 2833A.

(3) Check the 2833A displays the following error ratios when selected on the word generator; 1 in 10^5, 1 in 10^4 and 1 in 10^3.

Checking error totalization and associated controls

(4) Set the 2833A to ERRORS-TOTAL and the word generator to an error ratio of 1 in 10^3. Check the 2833A display is totalizing.

(5) Set the 2833A to ERRORS-RESET. Using a stopwatch or timer, check after a 10 second period, the display reading is within ±1% of 84480.

(6) Check the 2833A totalizing display can be discontinued by selecting ERRORS-STOP and continued by selecting ERRORS-CONT.

Overflow

(7) Set the word generator to the highest error ratio position and check the 2833A display reaches 999999, resets to zero and activates the OVERFLOW LED which should stay illuminated as the count recommences. Reset the OVERFLOW LED by selecting ERRORS-RESET.

Buzzer test

(8) Select 2833A BUZZER-ERROR and check that an audible alarm indicates errors detected in either ERRORS-TOTAL or RATIO modes.

11. The following tests check freque cy discrimination, jitter and signal level operation.

Frequency discrimination

(1) Connect a p.c.m. pattern generator with a 1.536 and 2.048 Mbit/s bit rate capability to the 75 Ω INPUT of the 2833A.

(2) Set the output of the p.c.m. pattern generator to 1.536 Mbit/s. If the TF 2802/2 pattern generator is used, connect the 75 Ω PATTERN OUTPUT to the 75 Ω INPUT of the 2833A and set the controls of the TF 2802/2 as follows :

BIT RATE	:	1.536 Mbit/s
PATTERN	:	HDB3 PSEUDO-RANDOM

(3) Check the display and SIGNAL LED on the 2833A are no longer illuminated which indicates that an incorrect bit rate p.c.m. signal is present.

(4) Repeat the above steps with the p.c.m. pattern generator bit rate set to 2.048 Mbit/s.

Jitter test (This test can be omitted if a jittered clock generator is not available).

(5) Connect the output of the jittered clock generator to the 75 Ω INPUT of the 2833A and set to 1.5 bits peak-to-peak jitter at 8.45 kHz.

(6) Check no errors or alarms are indicated on the 2833A display.

Signal level

75 Ω input

(7) Connect the equipment as shown in Fig. 2.

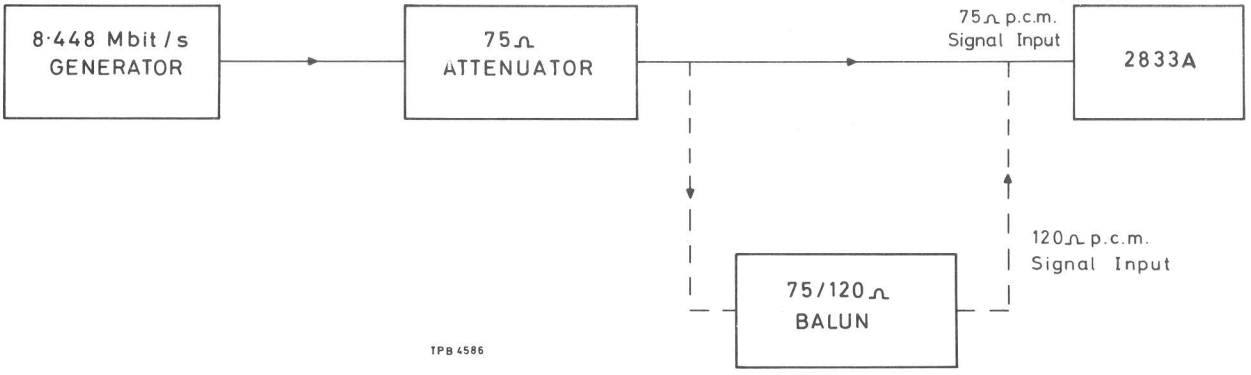


Fig. 2 Signal levels test (8M CODE)

(8) If the TF 2808/1 is used, set the controls as follows :

MODE	:	SEND
BIT RATE	:	UPPER (8.448 Mbit/s if available)
FORMAT	:	HDB3
BINARY PATTERN	:	PSEUDO-RANDOM
ERROR INJECTION	:	OFF

(9) Set the attenuator to 0 dB and check the 2833A display and SIGNAL LED are illuminated.

(10) Increase the attenuation until the display or SIGNAL LED are no longer illuminated on the 2833A and note the attenuation. The attenuator should not read higher than 11 dB.

120 Ω input

(11) Repeat steps (9) and (10) with the 75 Ω to 120 Ω Balun connected between the 75 Ω attenuator and the 120 Ω INPUT of the 2833A. Select SOURCE 120 Ω on the 2833A. The attenuator should not read higher than 5 dB.

EXT COUNT

Test equipment : items g,h or (i,j,t and u).

12. The following tests check the operation of the external count mode and the EXT COUNT input return loss.

(1) Apply t.t.l. pulses from a t.t.l. pulse generator e.g. Logic Pulser HP 546A to the EXT. COUNT input on the rear panel of the 2833A.

(2) Check the totalized external pulses are displayed in ERRORS-TOTAL or RATIO modes when EFS mode is not selected.

(3) If EFS mode is selected, ERRORS-RATIO will display EFS Percentage.

Return loss

(4) If a return loss measuring set is not available, the following test equipment can be used as shown in Fig. 3.

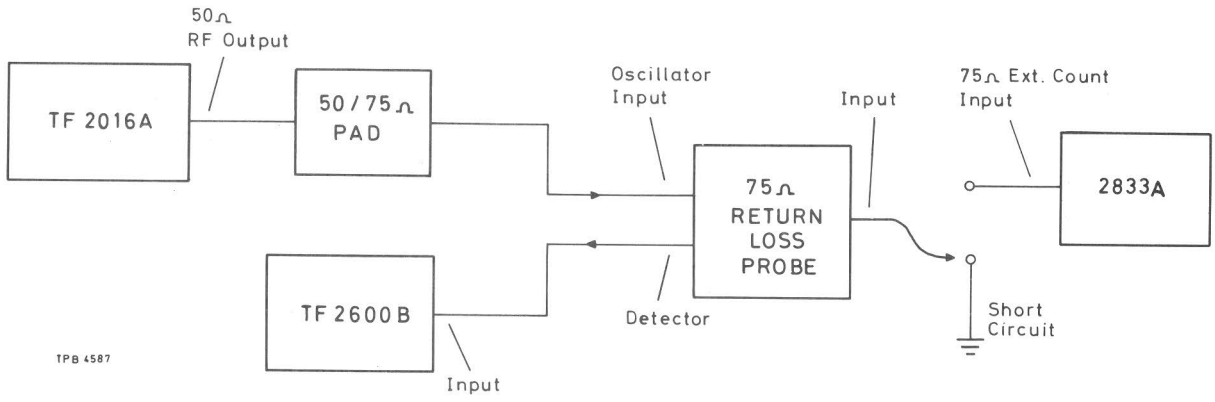


Fig. 3 Measuring EXT COUNT input return loss

(5) Short circuit the INPUT of the return loss probe and set the controls of the TF 2016A as follows:-

FUNCTION : CW
CARRIER FREQUENCY : 40 kHz
CARRIER switch : ON

(6) Adjust the RF OUTPUT to give a suitable 0 dB reference on the voltmeter.

(7) Remove the short circuit and connect the INPUT of the return loss probe to the 75 Ω EXT COUNT input of the 2833A.

(8) Observe the change in level indicated by the voltmeter. The measured level should be greater than 20 dB down on the original 0 dB reference.

(9) Repeat steps (5) to (8) with CARRIER FREQUENCY set to 3 MHz.

2M ALIGN

Test equipment : items k,l.m.

13. The following tests check the alarm LED s, error display and pen recorder output.

Alarms test

(1) Select 2M ALIGN. Connect the 75 Ω DIGITAL OUTPUT of the TF 2828A to the 75 Ω INPUT of the 2833A and connect ALARMS OUT on the 2833A to TEST LEAD TO TF 2829 connector on the TF 2828A.

(2) Select SOURCE 75 Ω and ALARMS - AUTO RESET on the 2833A. Select LINE on the TF 2828A and depress CONTROL Mode 4. Check the LINE alarm LED on the 2833A illuminates and extinguishes after the alarm condition clears.

(3) Select AIS on the TF 2828A and depress CONTROL Mode 4. Check the AIS LED on the 2833A illuminates.

(4) When the AIS LED has extinguished, repeat step (3) for each of the frame word error alarm sequence tests 1 in 10^3, 1 in 10^4 and 1 in 10^5. Check that the ERRORS LED on the 2833A illuminates and clears in each case.

Note that long periods of up to 60 seconds may be encountered before the ERRORS LED extinguishes.

(5) Select sequence test FRAME on the TF 2828A and depress CONTROL Mode 4. Check that the FRAME alarm LED on the 2833A illuminates and extinguishes after the alarm condition clears. Check the PASS lamp on the TF 2828A illuminates.

(6) Repeat step (5) for DISTANT, MULTIFRAME and DISTANT MULTIFRAME sequence tests on the TF 2828A.

(7) Repeat steps (2) to (6) with ALARMS-LAMP LOCK selected on the 2833A. In each case check the ALARM LED remains illuminated after the alarm condition has cleared.

Frame word error display

(8) Select ERRORS 1 in 10^3 on the TF 2828A and depress CONTROL Mode 4. Select ERRORS-RATIO on the 2833A. Check the ERRORS LED is illuminated and 1 in 10^3 is displayed.

(9) Select ERRORS-TOTAL on the 2833A. Check the 2833A display is totalizing and can be stopped by selecting ERRORS-STOP, reset by selecting ERRORS-RESET and continued by selecting ERRORS-CONT.

Pen recorder (1 mA f.s.d.)

(10) Connect a multimeter in series with a resistance of approximately 500 Ω to the Pen recorder output pins on the OUTPUTS connector on the rear panel of the 2833A. Set the range of the multimeter to DC current. See Chap. 3, Fig. 15.

(11) Select LINE on the TF 2828A and depress CONTROL Mode 4. Check that the output current displayed by the multimeter is 0 mA +0.03 mA, -0.00 mA.

(12) Repeat step (11) for each of the alarm tests in CONTROL Mode 4 on the TF 2828A and check the output current readings correspond to those in Chap. 1, para. 24.

Pen recorder (5 mA f.s.d.)

(13) Select LINE on the TF 2828A and depress CONTROL Mode 4. Check that the output current displayed by the multimeter is 0 mA +0.1 mA -0.00 mA.

(14) Repeat step (13) for each of the alarm tests in CONTROL Mode 4 on the TF 2828A and check the output current readings correspond to those in Chap. 1, para. 24.

14. The following tests check the unassigned bits (OUTPUTS), time-slot selection and the 64 kbit/s output.

Unassigned bits output (see Chap. 3, Fig. 11)

(1) Select FRAME TS0 on the TF 2828A and depress CONTROL Mode 5.

(2) Monitor unassigned bit 1 of the frame alignment word using an oscilloscope with a probe connected to pin 1 of the OUTPUTS connector on the rear panel of the 2833A.

(3) On the TF 2828A, set the WORD INVERSION Bit 1 switch (reading from left to right) to the NORMAL position and check its indicator LAMP is illuminated. Check the oscilloscope display indicates a t.t.l. logic 1 i.e., a voltage level between 2.4 V and 5 V.

(4) On the TF 2828A, set the WORD INVERSION Bit 1 switch to INVERT and check the level on the oscilloscope display changes to indicate a logic 0.

(5) Repeat steps (2), (3) and (4) for unassigned Bits 1, 4, 5, 6, 7 and 8 of the not-frame word and unassigned Bits 5, 7 and 8 of the multiframe word. In each case when the WORD INVERSION bit switches are set to NORMAL, the unassigned bits are set to logic 1.

Time-slot selection

(6) Depress the CHANNEL-TS switch on the 2833A and check that the display increments the time-slot display up to 31 for the duration the switch is depressed. Reverse the direction of the count by releasing and depressing the CHANNEL-TS switch and check the display decrements to 00.

64 kbit/s output

(7) Connect the equipment as shown in Fig. 4.

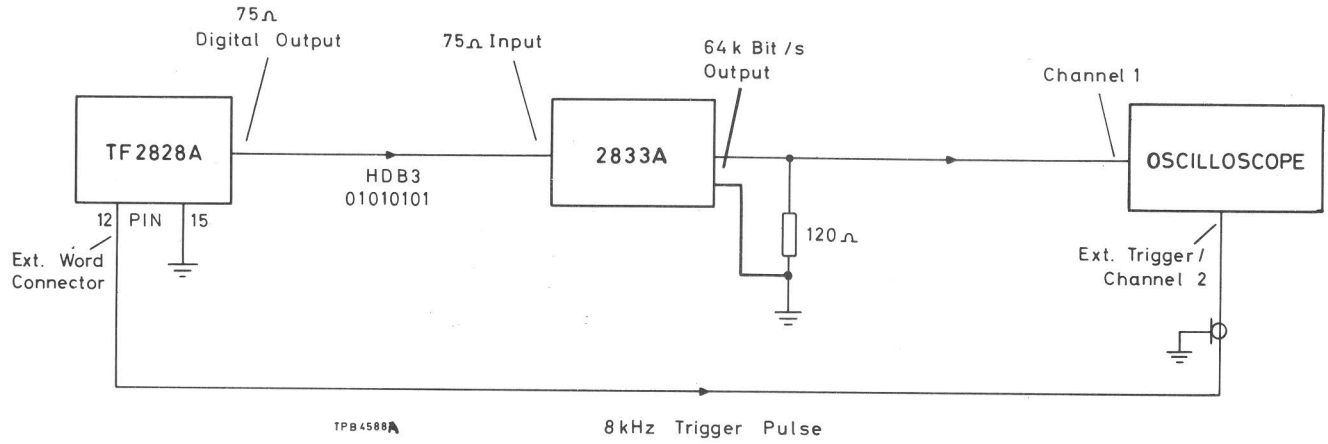


Fig. 4 Checking the 64 kbit/s output

(8) Set the controls of the TF 2828A as follows :

CONTROL : Mode 3
EXT WORD
SELECTED CHANNEL switches : CHANNEL 1
UNSELECTED CHANNELS : ZERO LEVEL
DIGITAL OUTPUT : 75 Ω

(9) Set the controls of the oscilloscope as follows :

Time/Div : 10 µs
Volts/Div : 500 mV

(10) The eight EXT WORD INPUT contact pins on the TF 2828A when not connected to an external word source are automatically set to logic 0. The 8 bit word to be loaded on to Channel 1 is therefore 00000000 alternate digit inverted to 01010101 and transmitted as an HDB3 coded signal to the input of the 2833A. The 01010101 signal is 64 kbit/s encoded by the 2833A and monitored by the oscilloscope. A logic 0 is represented by 1010 and a logic 1 is represented by 1100. The polarity of consecutive four digit blocks are alternated to convert the signal to three levels. The 8th block is violated to mark the last bit in each 8-bit word.

(11) Observe the oscilloscope display. Identify the beginning and end of the 64 kbit/s encoded 01010101 8-bit word. It may be useful to vary the width of the waveform using the oscilloscope time base cal/variable time control. Check the waveform pattern is similar to that shown in Fig. 5.

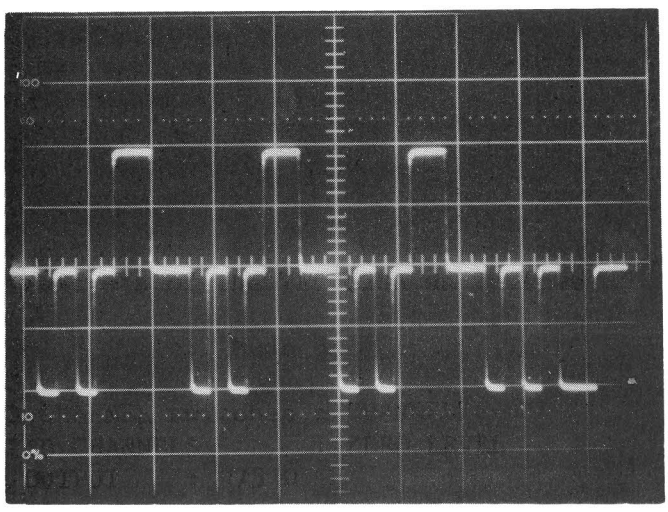


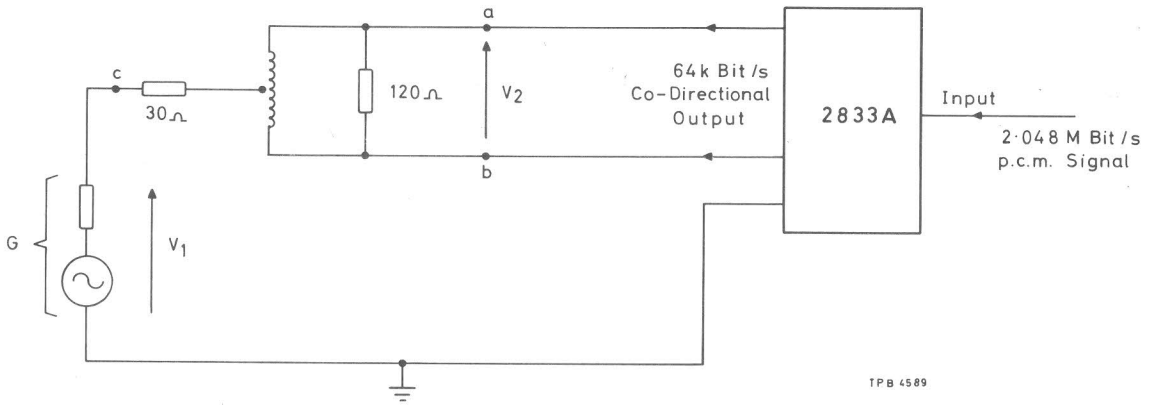
Fig. 5 64 kbit/s encoded 01010101 8-bit word

Measuring the 64 kbit/s output impedance balance ratio

(12) The CCITT recommends the measuring method shown in Fig. 6.

Note...

To make a correct measurement, a 2.048 Mbit/s p.c.m. signal should be present at the input of the 2833A.



$$\text{Balance} = 20 \log_{10} \frac{V1}{V2}$$

Fig. 6 Measuring the 64 kbit/s output impedance balance ratio

2M SIG

Test equipment : item k.

15. The following tests check the signalling word display and the associated functional controls.

Signalling word

(1) Connect the 75 Ω DIGITAL OUTPUT of the TF 2828A to the 75 Ω INPUT of the 2833A. Select SOURCE 75 Ω on the 2833A.

(2) Select a desired channel between 1 and 15 by depressing the CHANNEL-TS switch on the 2833A.

(3) Set the controls of the TF 2828A as follows :

CONTROL Mode 3
LEVEL TEST 2
SELECTIVE SIGNALLING
SELECTED CHANNEL switches : Desired channel as selected on 2833A
UNSELECTED CHANNELS : ZERO LEVEL
DIGITAL OUTPUT : 75 Ω

(4) On the TF 2828A, set the signalling word to the binary state 0110 (alternate bit inverted to 0011) by setting the first four word switches (starting from left to right). Check that Signalling Code 3 (circuit seized) is displayed by the 2833A.

(5) Select a desired channel between 16 and 30 by depressing the CHANNEL-TS switch on the 2833A. Check when first depressing the CHANNEL-TS switch that the previous Signalling Code 3 is briefly displayed by the 2833A.

(6) On the TF 2828A select the channel as selected on the 2833A in step (5) and change the signalling word to the state 1110 (alternate bit inverted to 1011) by setting the last four word switches. Check that Signal Code 11 (dial break) is displayed by the 2833A. On the TF 2828A, change the signalling word to represent another code and check it is displayed by the 2833A.

Note...

> If the signalling word is set to 0000, it is possible for the p.c.m. receiver, in this case the 2833A to mistake it for the multiframe alignment word, resulting in incorrect multiframe alignment. In practical p.c.m. systems, an all zero signalling word is not normally allowed to be transmitted.

(7) Depress the CHANNEL-TS switch and check that the previous Signalling Code 11 is briefly displayed by the 2833A.

Dialling errors

(8) It is possible to check the capability of the 2833A to detect dialling errors by using a program that simulates dialling error codes. The program can be implemented using a GPIB controller connected to the TF 2828A via the GPIB BUS CONTROL socket. Alternatively, a purpose built jig can be used to generate dialling error codes and connected to the TF 2828A via the REMOTE CONTROL INTERFACE socket (see Fig. 7).

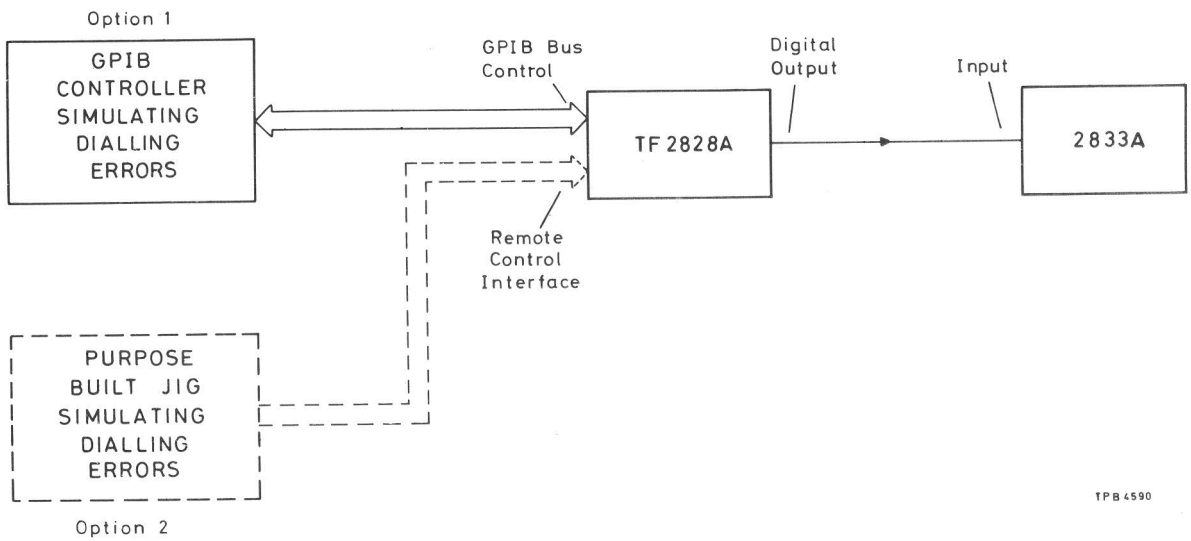
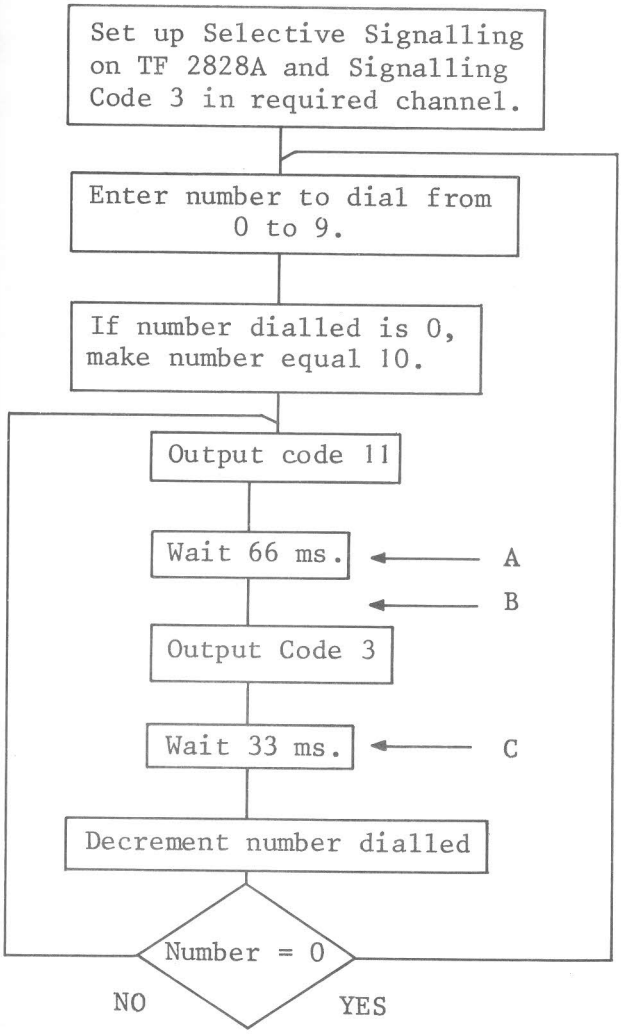


Fig. 7 Simulating dialling errors

Flow chart

(9) The following flow chart can be used as a useful guide for writing a GPIB controller program simulating dialling error codes. A full set of GPIB commands for the TF 2828A are available in Chap. 3 of the TF 2828A Instruction Manual (Part No. 46881-397R).



i.e. Command code mkjQnj6k0A1

e.g. Data word j>k0 (Channels 1 to 15)

e.g. Data word j6k0 (Channels 1 to 15)

Loop once for a dialled 1.
" twice " " " 2 etc.
Loop ten times for a dialled 0.

To simulate Error Code 1. Insert a brief non 3/11 code e.g. code 5 (j0k0) and wait 3 ms at step B.

To simulate Error Code 2. Change step A to wait 50 ms.

To simulate Error Code 3. Change step A to wait 85 ms.

To simulate Error Code 4. Change step C to wait 20 ms.

To simulate Error Code 5. Change step C to wait 50 ms.

To simulate Error Code 6. Allow the loop to be executed 11 times.

MISCELLANEOUS

Test equipment : items b,c,e,h or (i,n,t,u) plus k,o,p,q,r and s.

16. The following tests check the p.c.m. signal input return loss.

Input return loss

75 Ω input (using a 75 Ω return loss probe)

(1) Connect the test equipment as shown in Fig. 8.

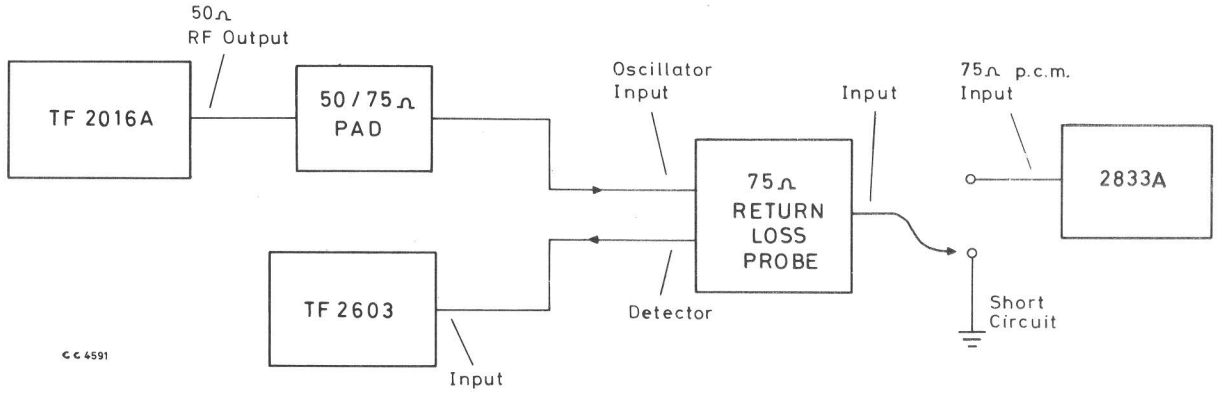


Fig. 8 Measuring return loss on the 75 Ω p.c.m. input

(2) Short circuit the return loss probe input and set the controls of the TF 2016A as follows :

FUNCTION	:	CW
CARRIER FREQUENCY	:	50 kHz
CARRIER switch	:	ON
RF OUTPUT	:	Set to provide a suitable 0 dB reference on the voltmeter

(3) Remove the short circuit and connect the return loss probe input to the 75 Ω INPUT of the 2833A. Set the 2833A SOURCE to 75 Ω.

(4) Note the change in level indicated by the voltmeter. The change measured should be greater than 15 dB down on the original 0 dB reference.

(5) Repeat steps (2) to (4) with the TF 2016A CARRIER FREQUENCY set to 100 kHz, 3 MHz and 12 MHz. The change in level should be greater than 20 dB at these frequencies.

120 Ω input (using a 120 Ω return loss probe)

(6) Repeat step (2) with the TF 2016A CARRIER FREQUENCY set to 100 kHz.

(7) Remove the short circuit and connect the return loss probe input to the 120 Ω INPUT of the 2833A. Set the 2833A SOURCE to 120 Ω.

(8) Note the change in level indicated by the voltmeter. The change measured should be greater than 20 dB down on the original 0 dB reference.

(9) Repeat steps (6), (7) and (8) with the TF 2016A CARRIER FREQUENCY set to 3 MHz. The change in level should be greater than 20 dB.

17. The following tests, check noise and interference immunity.

Noise immunity

2M CODE

(1) Connect the test equipment as shown in Fig. 9.

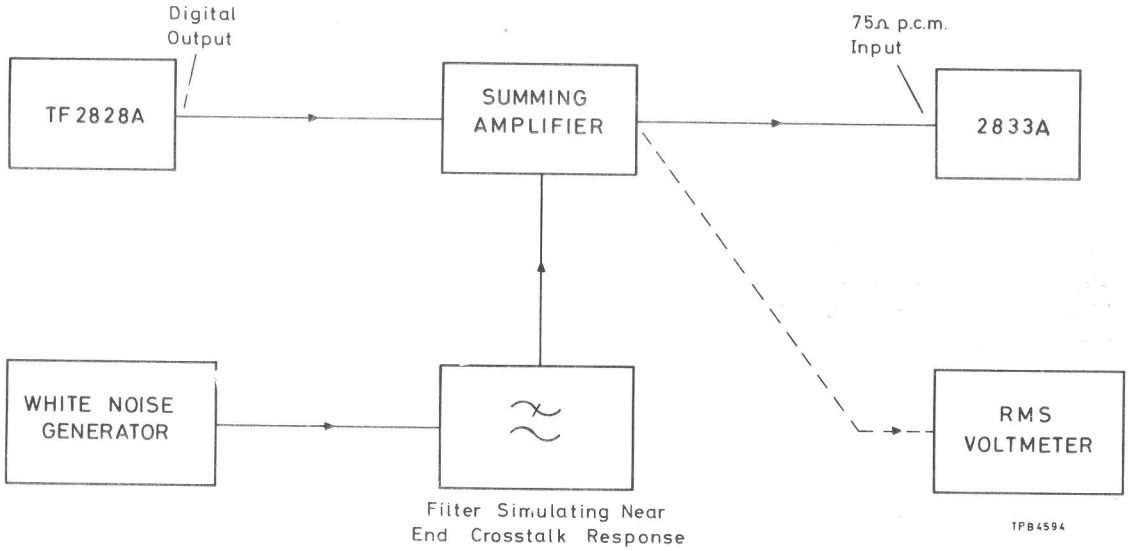


Fig. 9 Measuring noise immunity at 2.048 Mbit/s

(2) Set the controls of the 2833A to 2M CODE, ERRORS-TOTAL and SOURCE-75 Ω.

(3) Set the controls of the TF 2828A as follows :

CONTROL : Mode 2
850 Hz SINE/NOISE switch : SINE
ALL CHANNELS SELECTED.

(4) Connect the r.m.s. voltmeter terminated in 75 Ω to the output of the summing amplifier. Disconnect the output of the noise generator. Set the voltmeter to display a suitable 0 dB reference and note the reading on the scale.

(5) Disconnect the output of the TF 2828A and connect the output of the noise generator to the 2.048 Mbit/s NEXT simulating filter. Adjust the noise generator output level to give a voltmeter reading 20 dB down on the original reading obtained in (4) above.

(6) Disconnect the voltmeter and connect the 2833A. Connect the TF 2828A to the summing amplifier. Reset the 2833A error display and activate a stopwatch or timer. Observe the 2833A display after a time period of 3 minutes and check that the number of totalized errors are less than 36.

8M CODE (Using an 8.448 Mbit/s p.c.m. generator and NEXT simulating filter).

(7) Set the controls of the 2833A to 8M CODE and ERRORS-TOTAL.

(8) If the TF 2808/1 Pattern Generator is used, set the controls as follows :

MODE	:	SEND
BIT RATE	:	UPPER (8.448 Mbit/s)
FORMAT	:	HDB3
BINARY PATTERN	:	PSEUDO-RANDOM
ERROR INJECTION	:	OFF

(9) Repeat step (4).

(10) Disconnect the output of the 8.448 Mbit/s p.c.m. generator and connect the output of the noise generator to the 8.448 Mbit/s NEXT simulating filter. Adjust the noise generator output level to give a voltmeter reading 20 dB down on the original reading obtained in step (4).

(11) Disconnect the voltmeter and connect the 2833A. Connect the 8.448 Mbit/s p.c.m. generator to the summing amplifier. Reset the 2833A error display and activate a stopwatch or timer. Observe the 2833A display after a time period of 3 minutes and check that the number of totalized errors are less than 36.

Interference immunity

2M CODE

(1) Connect the test equipment as in Fig. 10.

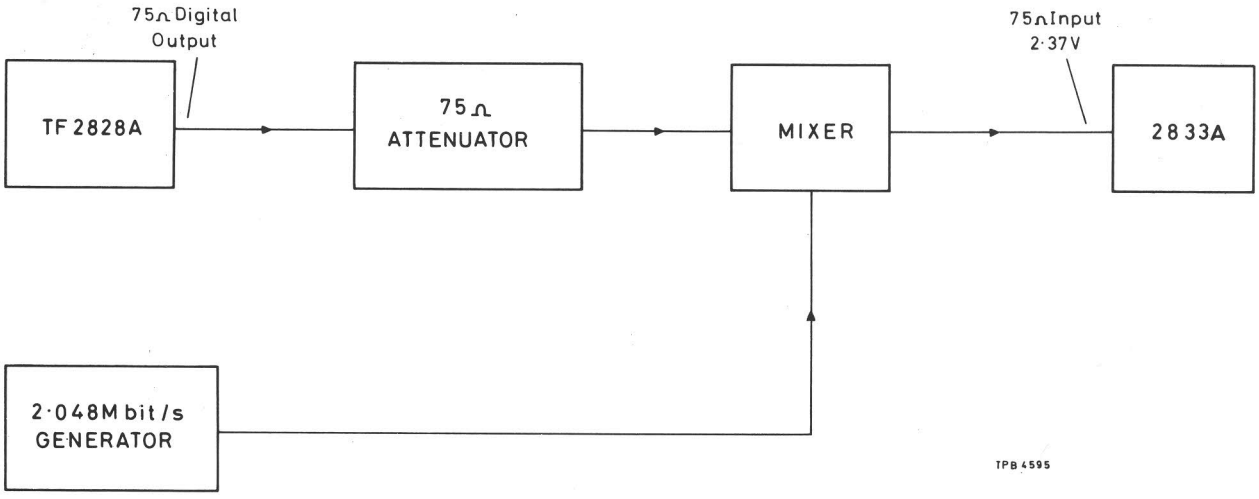


Fig. 10 Measuring interference immunity at 2.048 Mbit/s

(2) Set the controls of the 2833A to 2M CODE, ERRORS-TOTAL and SOURCE 75 Ω.

(3) Set the controls of the TF 2828A as follows :

CONTROL	:	Mode 2
850 Hz SINE/NOISE switch	:	SINE
ALL CHANNELS SELECTED		
DIGITAL OUTPUT	:	75 Ω

(4) If the TF 2802/2 Pattern Generator is used, set the controls as follows :

BIT RATE	:	2.048 Mbit/s
PATTERN	:	HDB3 PSEUDO-RANDOM

(5) Use the attenuator to reduce the output signal from the TF 2828A by 18 dB but maintain the signal level input to the 2833A at 2.37 V. Check that no errors are displayed by the 2833A.

8M CODE

(6) Set the controls of the 2833A to 8M CODE, ERRORS-TOTAL and SOURCE 75 Ω

(7) If the TF 2808/1 Pattern Generator is used as an 8.448 Mbit/s source, set the controls as follows :

MODE	:	SEND
BIT RATE	:	UPPER
FORMAT	:	HDB3
BINARY PATTERN	:	PSEUDO-RANDOM
ERROR INJECTION	:	OFF

(8) Repeat step (5).

Lamp and self-test

TEST LAMP

18. (1) Select TEST-LAMP on the 2833A and check all the display LED s on the front panel are illuminated.

(2) Select TEST-SELF on the 2833A and check that 2M CODE is selected and that the display indicates an error ratio of 1 in 10^5.

ACCESS TO BOARDS AND COMPONENTS

Removal of case

WARNING.

Disconnect the a.c. mains supply before removing the case.

19. The case surrounds all sides of the instrument except the front and rear panels. The instrument and case assembly are held in place by the two rubber feet mounting brackets secured to the rear panel by a single screw in each bracket. To remove the instrument from the case, remove the feet mounting brackets and replace the screws to secure the rear panel. Carefully withdraw the instrument front first from the case.

Access to boards

20. To access the printed circuit boards, the top board AA12 (roughly three quarters of the length of the bottom board AA3) must first be removed. Remove the six screws securing the AA12 board to the side frames and remove the board, taking care in the process to disconnect the interconnecting board locating in the edge connector SKA on the component side of AA12. Place AA12 to one side of the instrument component side up. The display board AA1 is attached to AA12 and may be separated by loosening the two securing nuts and removing the two screws holding the two boards together.

21. To access the rear section of the bottom board AA3, unscrew the seven screws securing the transformer chassis to the side panels, rear panel and heat sink. Lift out the transformer chassis with the transformer affixed and stand it away from the rear panel, see Fig. 11.

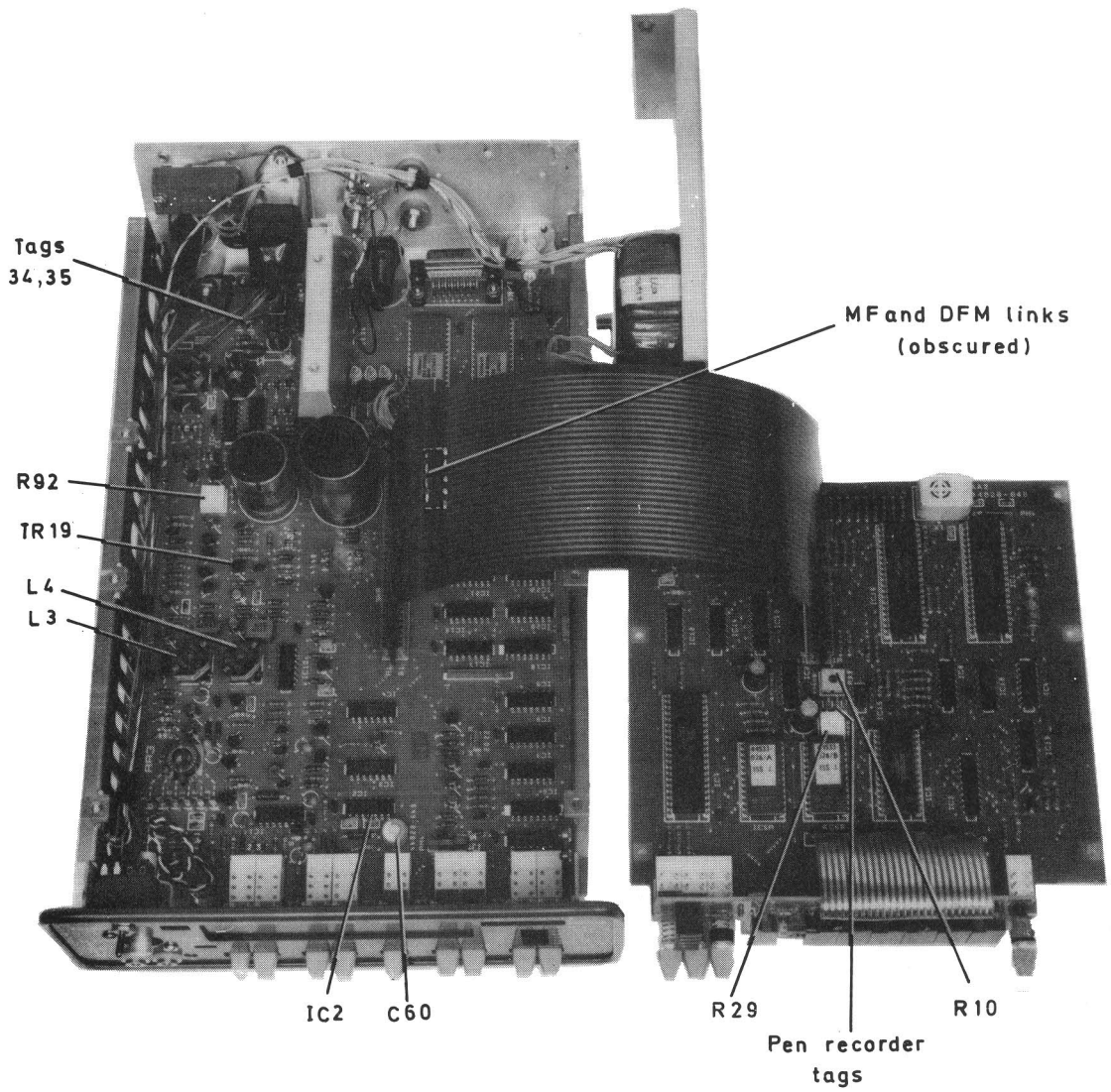


Fig. 11 Access layout of circuit boards, adjustment and test points

22. For further access to the rear section of AA3, the rear panel may be opened outwards by removing the two original feet mounting screws and two smaller screws attached to the heat sink.

ADJUSTMENTS AND TEST POINTS

23. Adjustment and testing of the printed circuit boards can be carried out when the boards have been made accessible. Remove the interconnecting board from SKA on AA3 and fit the flexible extender board (part no. 46883-513K supplied as an optional accessory) between edge connectors SKA on boards AA12 and AA3. Fig. 11 shows the layout and position of the adjustment and test points on boards AA1, AA12 and AA3.

Adjustments

24. The following items can be checked and, if necessary, adjusted to meet the limits quoted in the Performance Data section of Chap. 1. The purpose of several links which can be set to suit the user's particular requirements are also included.

CAUTION.

Take care not to short circuit components to the p.c.b. earth plane when connecting probes to component leads situated within the p.c.b. earth plane area.

Clock recovery

25. The resonant frequency of the 2.048 MHz and 8.448 MHz sine wave clock recovery oscillators on AA3 can be checked and adjusted as follows.

(1) 2M oscillator. Connect a 2.048 Mbit/s p.c.m. signal at the correct amplitude to the input of the 2833A and select 2M CODE.

(2) Connect a probe from an oscilloscope to the emitter of TR19, and earth to the earth plane.

(3) Tune L4 to indicate a peak sine wave on the oscilloscope display. The sine wave should have a nominal peak-to-peak value of 1.8 V on a d.c. level of 4.3 V (nominal).

(4) 8M oscillator. Connect a 8.448 Mbit/s p.c.m. signal at the correct amplitude to the input of the 2833A and select 8M CODE.

(5) Monitor the emitter of TR19 and tune L3 to indicate a peak sine wave on the oscilloscope display as above.

Note...

In both cases, it is important to check that the applied p.c.m. signal is at the correct frequency so that correct adjustment of the clock recovery oscillator can be made.

64 kbit/s output

26. The 64 kbit/s co-directional output signal voltage on AA3 can be checked and adjusted as follows.

(1) Connect a 2.048 Mbit/s p.c.m. signal at the correct amplitude to the input of the 2833A and select 2M ALIGN.

(2) Check frame alignment is present i.e. the FRAME alarm is not illuminated.

(3) Connect a probe and earth from an oscilloscope to tags 34 and 35 on AA3.

(4) Adjust preset R92 to give a 2 V peak-to-peak signal on the oscilloscope display.

Self-test generator

27. The oscillator frequency section of the self-test generator circuit on AA3 can be checked and adjusted as follows.

(1) Connect a high impedance probe from a frequency counter to pin 3 of IC2.

(2) Adjust trimmer C60 to give a frequency reading of 2048 kHz ±2 kHz on the counter display.

Pen recorder (AA12)

28. The f.s.d. current can be checked and adjusted as follows.

(1) Connect a multimeter in series with a resistance of approximately 500 Ω to the PEN RECORDER output pins on the rear panel OUTPUTS connector. Set the range of the multimeter to DC current.

(2) 1 mA f.s.d. With the pen recorder output set to operate in the 1 mA range i.e. with pin 2 linked to pin 3, hold TEST-LAMP depressed and adjust preset R29 to give a reading of 1 mA.

(3) 5 mA f.s.d. With the pen recorder output set to operate in the 5 mA range i.e. with pin 2 linked to pin 1, hold TEST-LAMP depressed and adjust preset R10 to give a reading of 5 mA.

Isolating strap

29. The isolating strap is a soldered tag which normally connects one side of the 75 Ω p.c.m. signal input to the earth plane via TP7 and TP6 respectively. To isolate the 75 Ω p.c.m. signal input from the instrument to form a floating balanced input, remove the tag.

MF and DMF alarms

30. The multiframe (MF) and distant multiframe (DMF) alarms can be inhibited to comply with some p.c.m. system requirements.

(1) To disable the MF alarm, remove the 2 pin connector linking pins 25 and 26, and position the connector to link pins 24 and 25.

(2) To disable the DMF alarm, remove the 2 pin connector linking pins 28 and 29, and position the connector to link pins 27 and 28.

TRANSISTOR AND DIODE CHECKING

31. Transistors may be checked by measuring the electrode voltages and/or by measuring the resistance between electrodes by means of a multimeter. So that the meter voltage does not damage the transistors or diodes, use the lowest voltage and the maximum source resistance available, e.g. the Ω range on the SEI selectest super 50.

FAULT DIAGNOSIS

32. This section includes an overall fault-finding chart designed as an initial guide to help identify fault symptoms and to direct the test engineer to the general area or areas on each p.c.b. likely to be causing a particular fault.

33. A list of useful test points with circuit voltages and waveforms obtained under normal instrument working conditions are also provided to aid fault diagnosis down to component level.

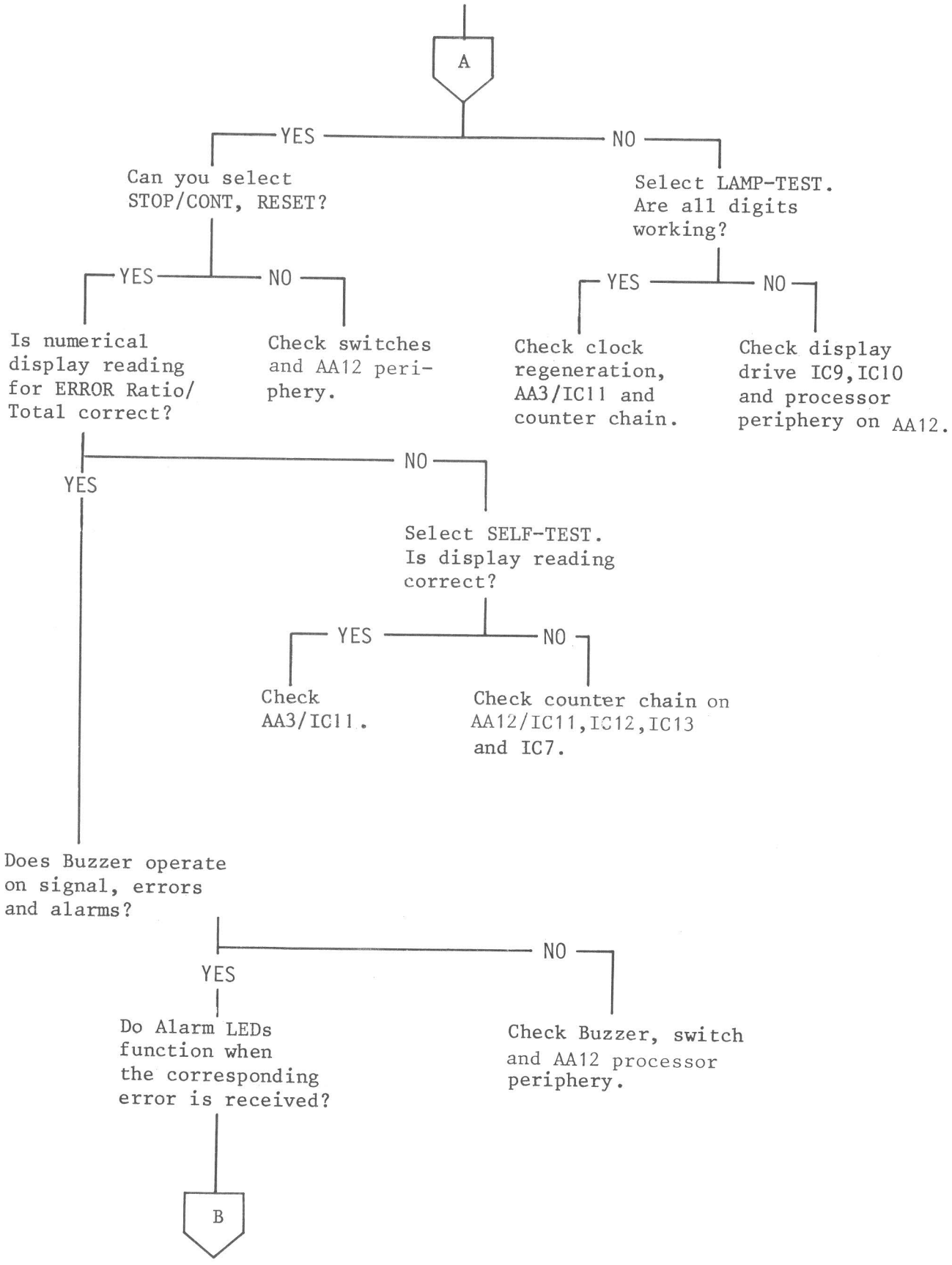
34. Finally, the processor and peripheral circuits on AA12 board can be checked for suspected faults by running a series of diagnostic self test programs stored in the EPROMs. A signature analysis test is also provided.

Overall fault finding chart

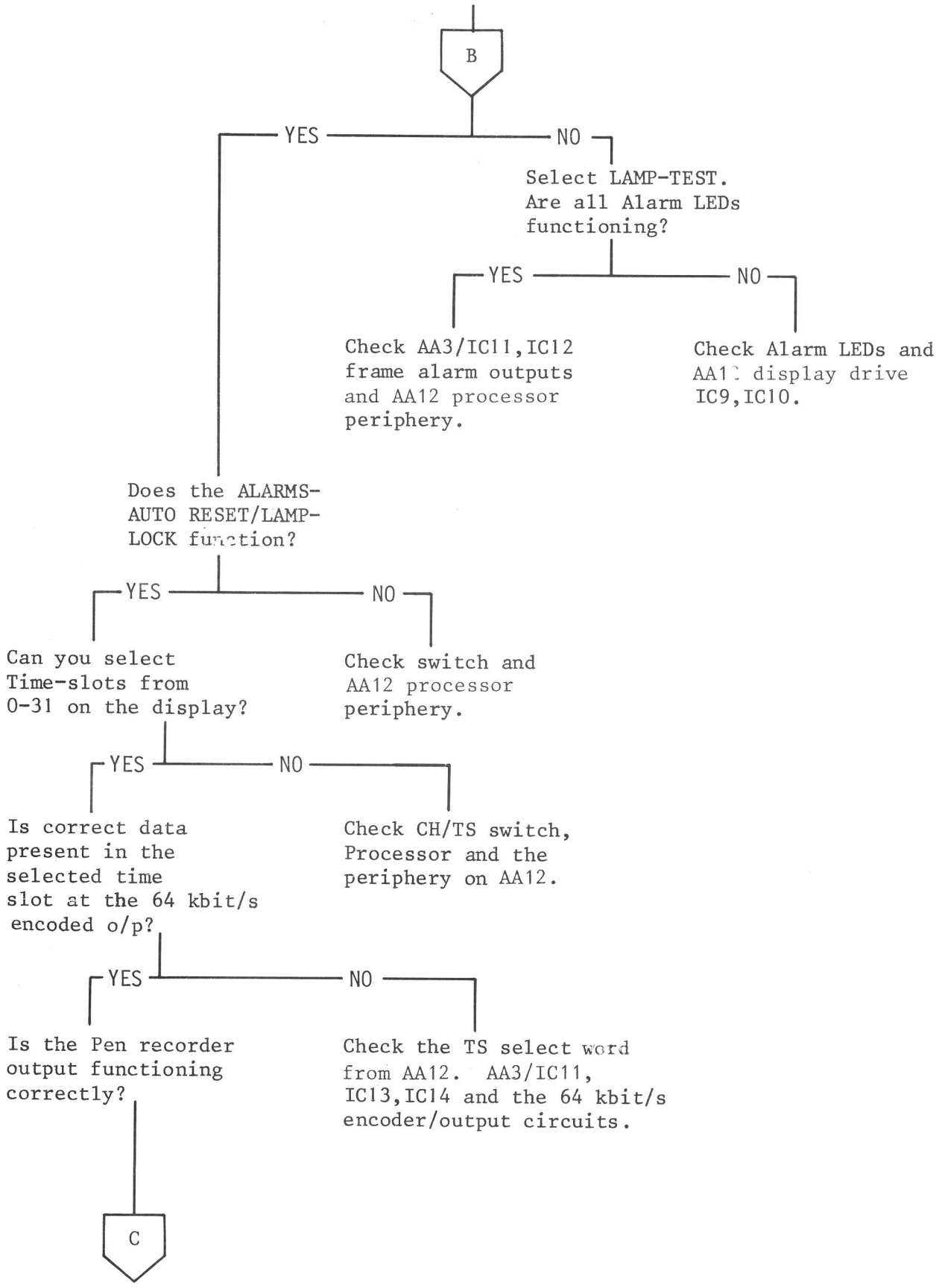
With a p.c.m. signal at the correct bit-rate present at the 2833A INPUT, is SIGNAL LED and numerical display on?

- YES → Can you select 2M ALIGN?
  - NO → Check FUNCTION switch or AA12 processor periphery.
  - YES → Can you select ERRORS-TOTAL or RATIO?
    - YES → With frame errors present in signal, is display reading coherent, e.g. not scrambled?
      - YES → A
      - NO → Check switches and AA12 processor periphery.
    - NO → Check switches and AA12 processor periphery.
- NO → Select SELF-TEST. Does SIGNAL LED and the correct numerical display come on?
  - YES → 1. Check p.c.m. signal is present and at correct bit-rate and amplitude.
    2. Check SOURCE switches. INPUT connectors and T1 on AA3.
  - NO → Does numerical display and SIGNAL LED come on with LAMP TEST?
    - YES → Check all signal input ccts. on AA3.
    - NO → Check power supply and display drive AA12

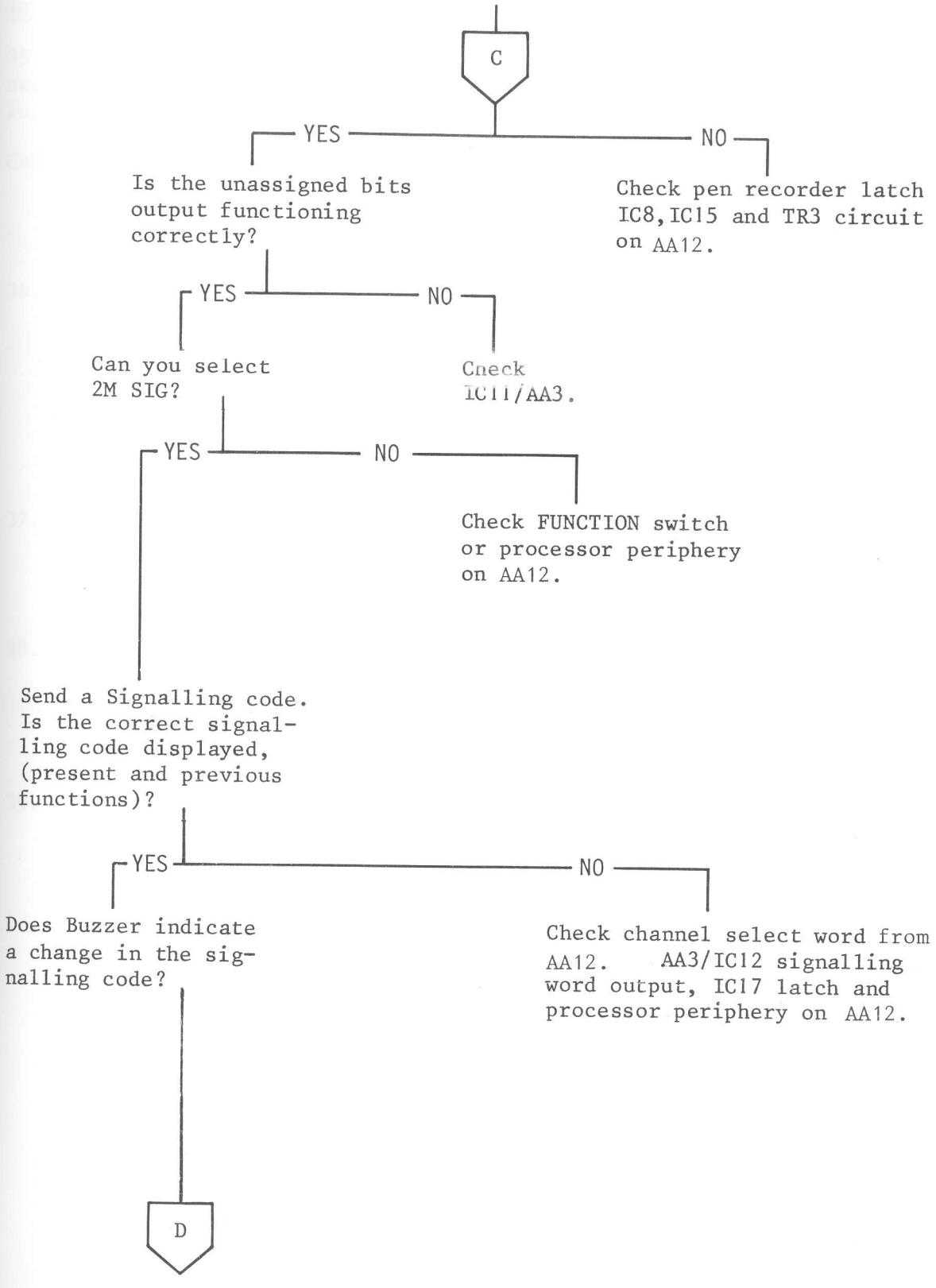
Indicates continuation of chart to next page.



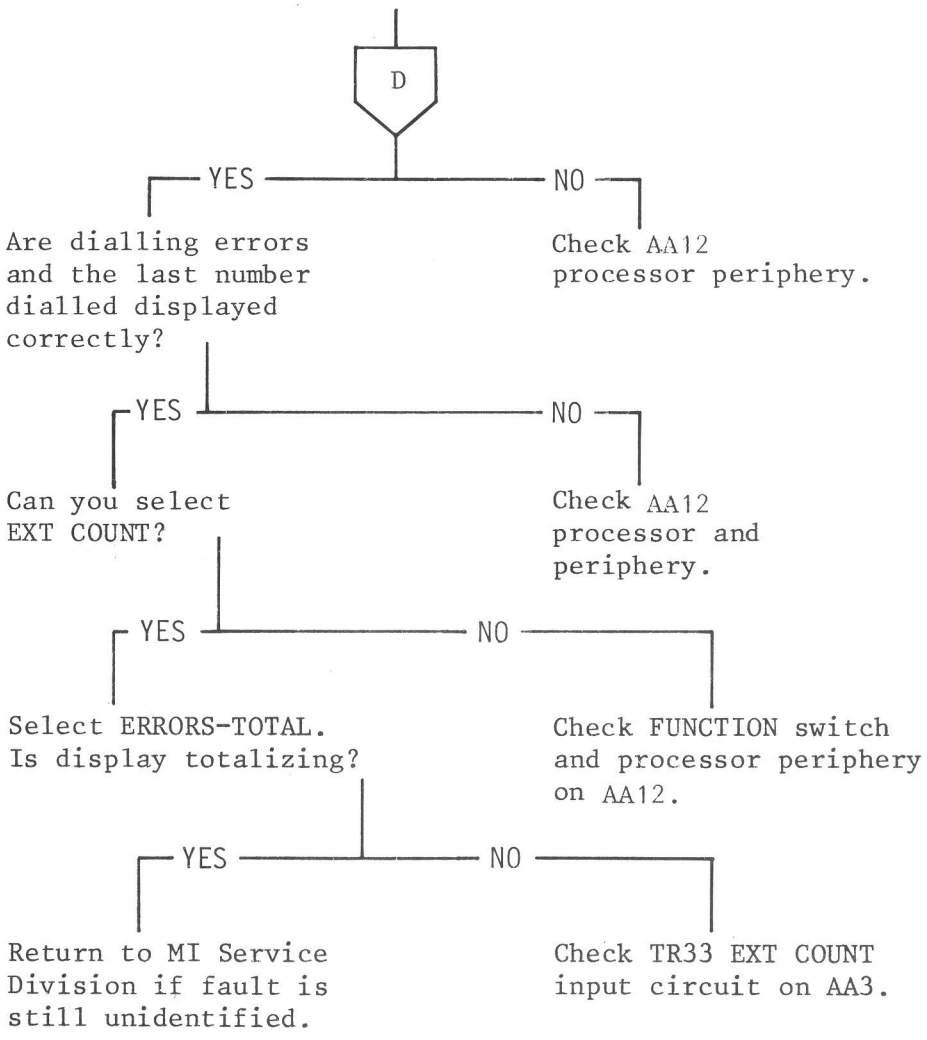
Overall fault finding chart (continued)



Overall fault finding chart (continued)



Overall fault finding chart (continued)



Overall fault finding chart (concluded)

Input and alignment board AA3

35. See component layout and circuit diagram Fig. 2 and 3 in Chap. 7. Connect a 2.048 Mbit/s p.c.m. signal at a peak amplitude of 2.37 V to the 75 Ω input of the 2833A.

CAUTION.

Take care not to short circuit components to the p.c.b. earth plane when connecting probes to component leads situated within the p.c.b. earth plane area.

36. Supply lines.

	Suitable test points	*Correct reading (nominal)*
+5 V (1)	Tag 45 and 46	+5 V ±0.25 V
+5 V (2)	SKA pin 1	+5 V ±0.25 V
+9.15 V	Tag 47 and 48	+9.15 V ±0.5 V

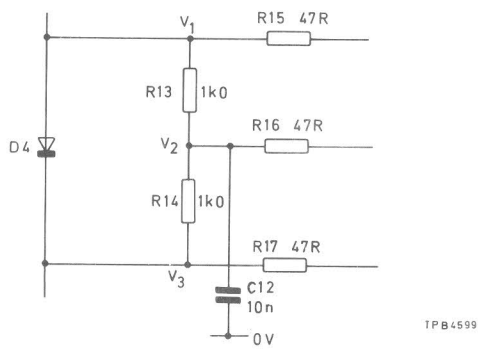
37. Input transformer T1.

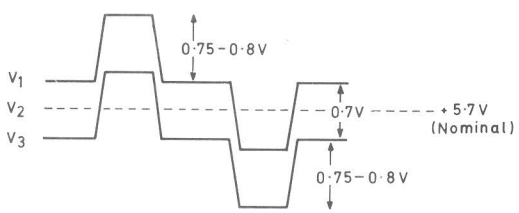
Across TP8 and TP13	2.37 V peak ±0.1 V

38. AGC.

IC1 pin 8	6.7 V d.c. with pulses of ±0.75 to ±0.85 V peak with up to 6 dB of attenuation at input of 2833A.

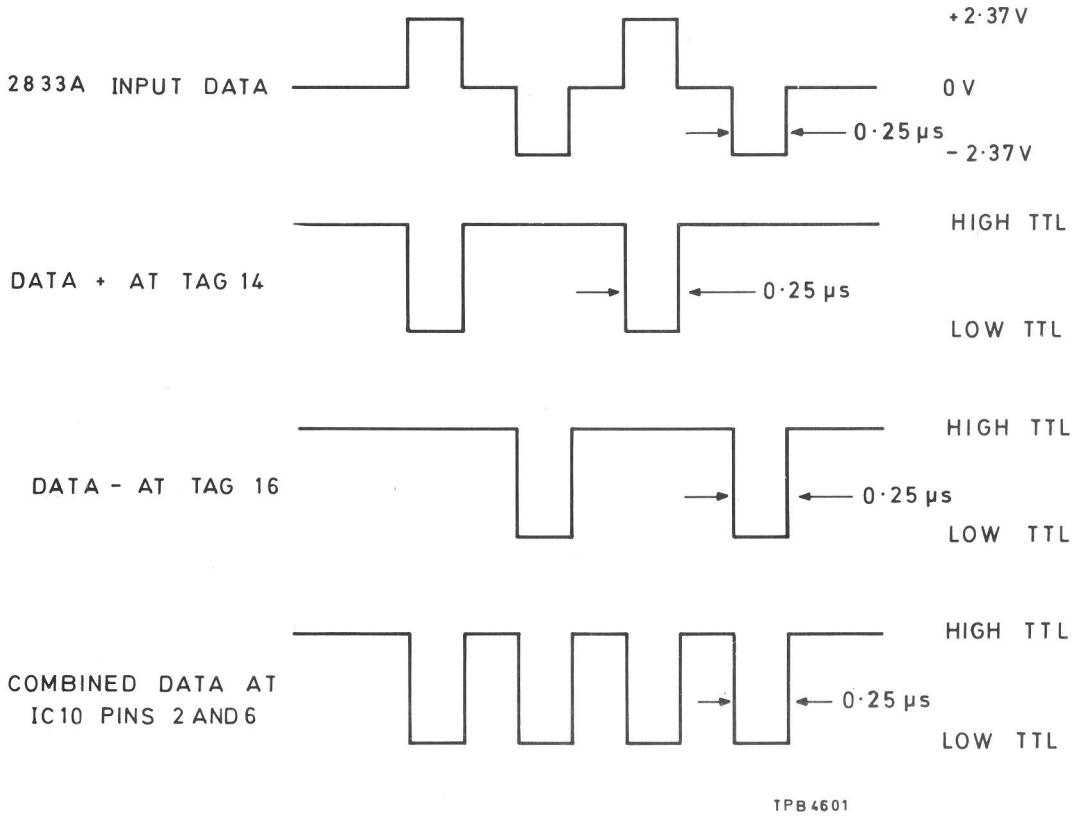
39. Data splitter.





V2 should be approximately equidistant between V1 and V3.

Remove the links connecting tags 14 and 15, 16 and 17 to enable probe access.



40. Clock recovery.

	Suitable test points	*Correct reading (nominal)*
With L4 tuned for a peak voltage	IC10 pin 5	2.048 MHz sine wave at 3.5 V peak to peak with a d.c. level of +5 V.
	TR19 emitter	2.048 MHz sine wave at 1.8 V peak to peak with a d.c. level of +4.3 V.

	Suitable test points	*Correct reading (nominal)*
Remove the link connecting tag 18 and 19 to enable probe access	Tag 18	2.048 MHz square wave, t.t.l. compatible.

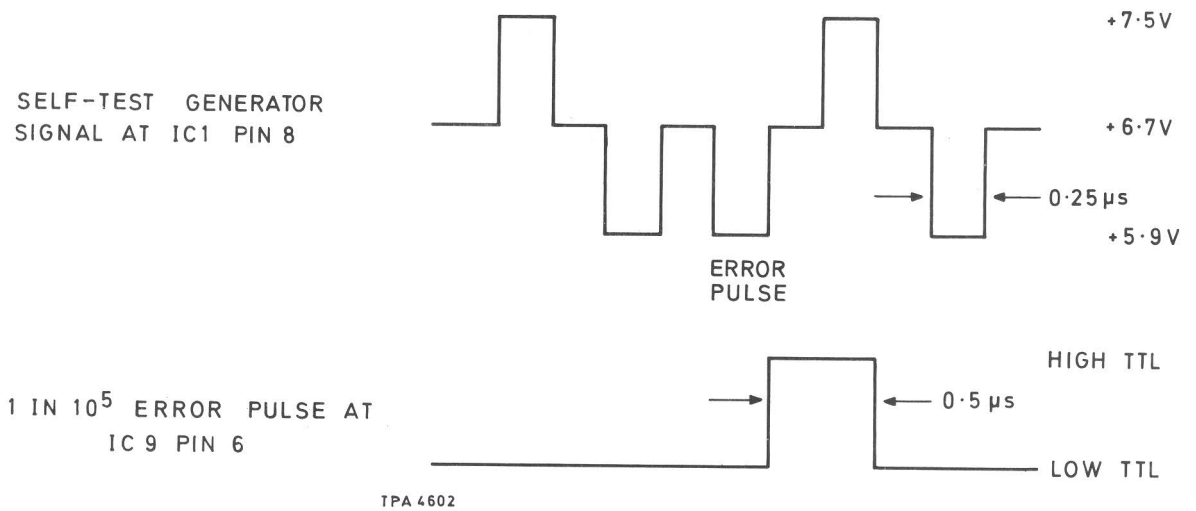
41. Signal OK control line.

Voltage reference	IC26 pin 6	4.2 V
Signal OK control line	SKA pin 5	Less than voltage reference with up to 8 dB of attenuation at input of 2833A. Greater than voltage reference with up to 11 dB of attenuation at input of 2833A.

Replace links connecting tags 14 and 15, 16 and 17, 18 and 19.

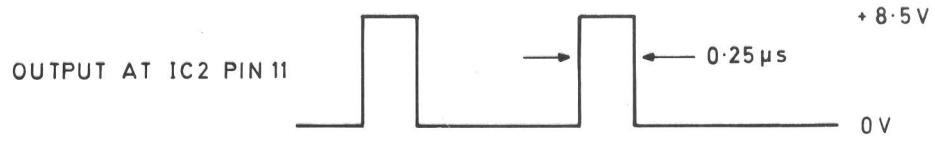
42. Self-test generator.

(1) Trigger oscilloscope using the TIMER pulse at the end of R57 connected to SKA pin 30 and set oscilloscope time base to 1 µs/div.

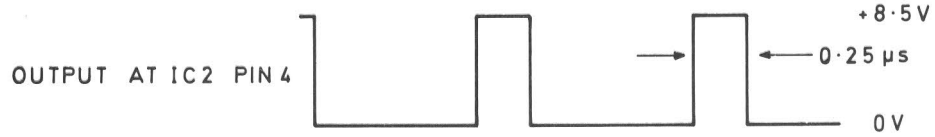


Note that these signals do not give a very bright or stable display.

(2) Trigger oscilloscope at IC2 pin 4.



(3) Trigger oscilloscope at IC2 pin 11.



TPA 4603

43. AMI/HDB3 error detector.

See timing diagram Chap. 4, Fig. 5.

44. Frame alignment IC11.

Notes.

The following notes provide useful information concerning the operation of IC11 (see Chap. 7, Fig. 3).

44.1 Legend: RMS - Receive Multiplex Select pulse. (Usually followed by An, Bn, C, etc. where n is an integer between 1 and 8).

TSO - Time Slot 0.

BnF - nth bit of Time Slot 0 in the frame containing the frame alignment word.

BnNF - nth bit of Time Slot 0 in the frame not containing the frame alignment word.

RBP - Receive Bipolar signal.

44.2 All spare data bit outputs are updated at the end of their respective TSO periods.

44.3 With the TSO DATA CONTROL (pin 18) in the logic 0 state (0 V), B1F is updated every frame and therefore alternates B1F information with B1NF information, but this does not affect the B1NF output.

44.4 For AIS and frame alarm outputs, the alarm state is a logic 1 (nominally +V_{CC}) and the non-alarm state is a logic 0 (nominally (0 V GND).

44.5 The frame error pulse is a positive-going pulse, nominally 244 ns wide, occurring at the end of the TS0 period in the frame not containing a frame alignment word whenever a frame alignment word is in error.

45. Timing diagrams.

(1) Connect a frame aligned p.c.m. signal to the INPUT of the 2833A e.g. connect the 75 Ω DIGITAL OUTPUT of the TF 2828A to the 75 Ω INPUT of the 2833A and select 2M ALIGN.

(2) The correct waveforms that should be present at the pins of IC11 are shown in Fig. 12.

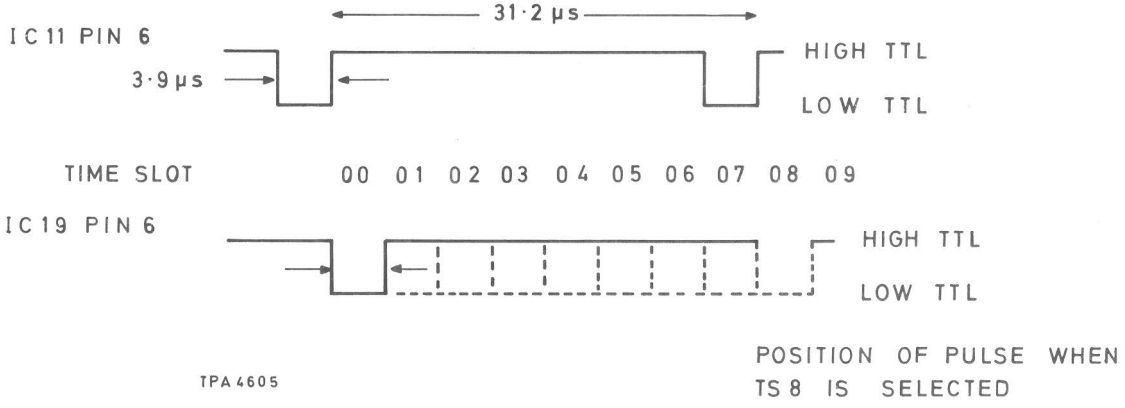
Note...

Paragraphs 46 to 49 contain measurements made with a frame aligned p.c.m. signal present at the 2833A INPUT and with 2M ALIGN selected.

64 kbit/s encoder

46. See also, timing diagram Chap. 4, Fig. 8.

(1) Trigger oscilloscope at IC11 pin 6 and set the time base to 10 µs/div.



IC19 pin 6, Notes...

1. Pulse moves from left to right when incrementing time slots.
2. Pulse moves from right to left when decrementing time slots.
3. Increments/decrements one pulse width per time slot.
4. The pulse contains eight pulses of 0.244 µs duration.

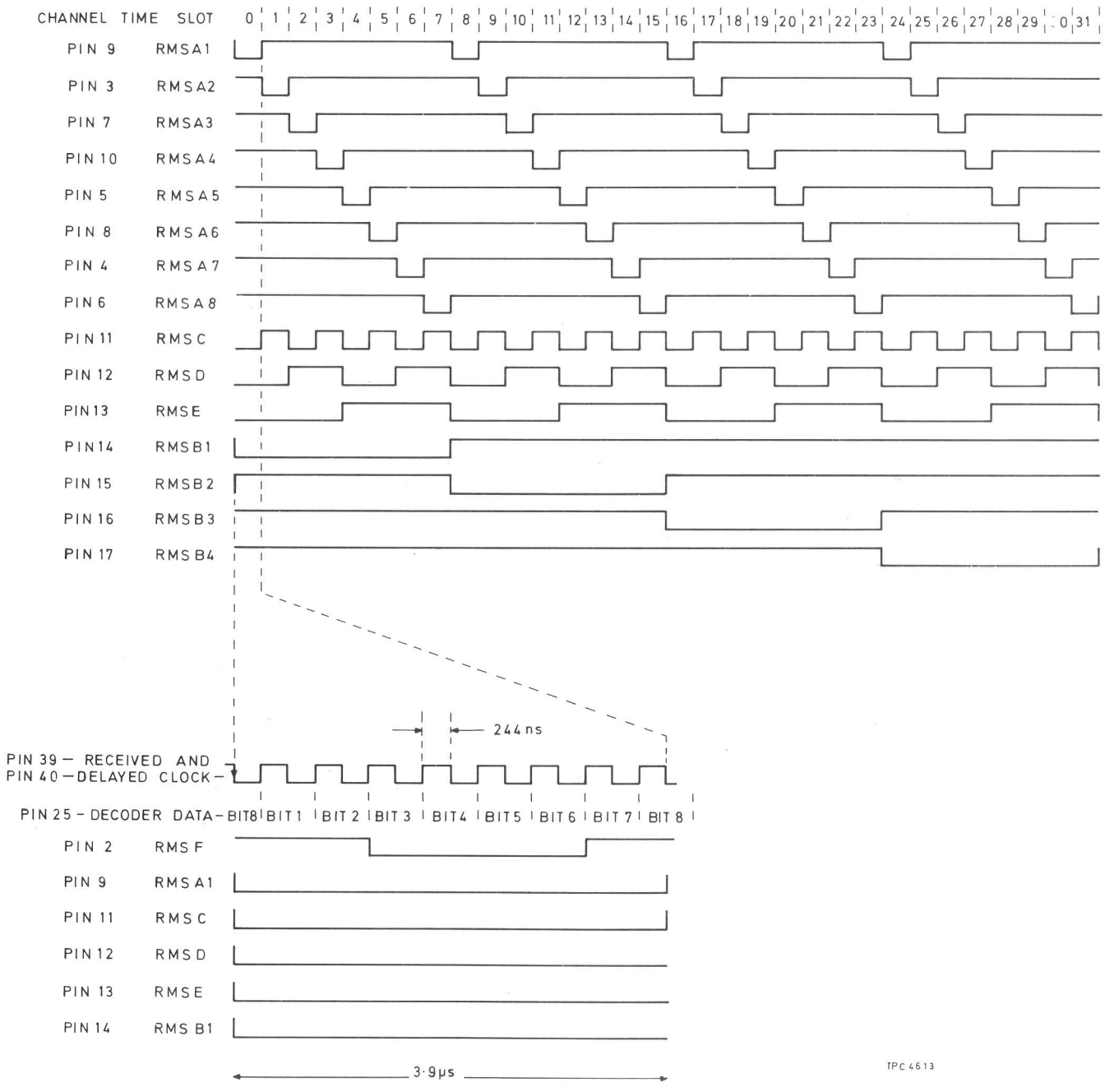
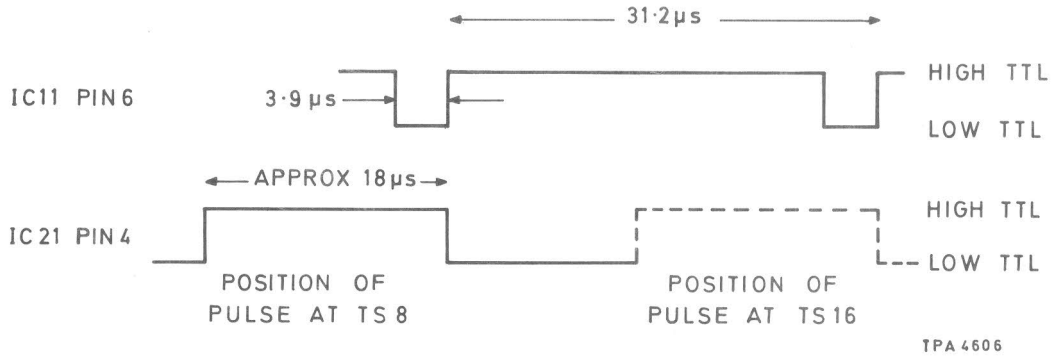


Fig. 12 Timing diagrams for IC11

(2) Set oscilloscope time base to 20 µs/div.



IC21 pin 4, Notes...

1. Pulse moves from left to right when incrementing time slots.
2. Pulse moves from right to left when decrementing time slots.
3. Increments/decrements in 31.2 µs steps every 8th time slot starting at TS0.

64 kbit/s output amplifier

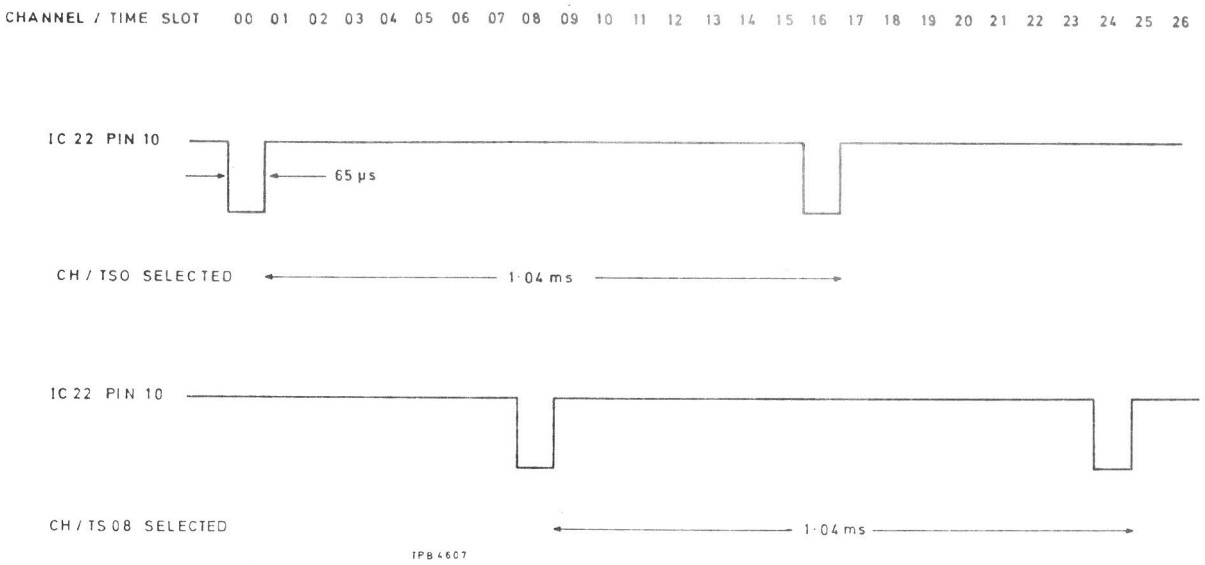
47.

Test point	*Correct reading*
IC25 pin 3	+1.7 V.
IC25 pin 1	+2 V d.c. with +ve going pulses of 2 V amplitude.
IC25 pin 5	As pin 1.
TR30 emitter	+3.35 V.

Signalling strobe

48. (1) Select 2M SIG.

(2) Trigger oscilloscope at IC11 pin 6.



Notes...

1. Pulses move from left to right when incrementing CH/TS.
2. Pulses move from right to left when decrementing CH/TS.

Note...

The eight timing signals from IC12 (RSSB1 to B4 and RSSA1 to A4) cannot be easily seen individually without connecting a 15 kΩ pull-up resistor from the +5 V line to the timing signal output pin required to be monitored.

Processor board AA12

Counter chain

49. A further test for the counter chain is available in Test 7 of the diagnostic test routines.

(1) Select AIS on the TF 2828A.

(2) Set the controls of the 2833A to 2M CODE and ERRORS-RATIO.

(3) A more accurate error ratio display, i.e. up to 4 decimal places, is obtained by depressing LAMP TEST and then depressing RESET.

(4) Remove the link connecting tags 14 and 15 on AA3 board.

(5) Depress Mode 4 button on the TF 2828A, the error ratio display on the 2833A should read 9.9900 in 10^2.

(6) Replace the link connecting tags 14 and 15, and remove the link connecting tags 16 and 17.

(7) Depress Mode 4 button on the TF 2828A, the error ratio display on the 2833A should read 9.9990 in 10^2.

(8) To return to normal error ratio mode, select another mode by depressing the FUNCTION switch.

Diagnostic test routines

50. The purpose of the following diagnostic test routines is to provide an additional aid to identifying a fault symptom on the processor board AA12 and to enable a practical means of monitoring the interaction between the processor and periphery.

51. It must be noted that the tests are limited and can not cover every possible fault. In some cases it may not be possible to run the program due to the inhibiting action of the fault e.g.

(a) Faulty processor.

(b) Faulty EPROM.

(c) Faulty address or chip enable decoders } (Holding down bus lines)

(d) Broken or shorted buses.

52. The following tests are performed:-

Test	*Title*
0	Processor running check
1	Chip enable check
2	Display and pen recorder check
3	RAM check
4	EPROM check
5	Input lines check
6	Output lines check
7	Counter check

53. Starting the test sequence. The test sequence can be started by either one of the following two ways:-

(1) Assuming the processor is able to read the switches on the front panel, switch SUPPLY to ON while holding CHANNEL depressed.

(2) On AA12 board, connect IC1 pin 6 (TRAP) momentarily to a +5 V line.

54. All the tests are performed in chronological order as listed above and in some cases, the test number is displayed by the exponent digit on the front panel display. The test sequence stops automatically when the last test in the sequence is completed i.e. Test number 7.

55. Stopping the test sequence. It is possible to stop at a desired test in the sequence for monitoring purposes by depressing STOP or by connecting IC1 pin 5 (SID) to a +5 V line. To continue the test sequence, release STOP or remove +5 V from SID. A variation on this method can be applied to Test 5 and successive tests and are explained in each test description.

56. Exit from the test sequence. To exit from the test sequence before the program ends, switch SUPPLY to OFF. To exit from the test sequence when Test 7 is completed, select RESET or switch SUPPLY to OFF, the 2833A should select 2M CODE. To restart the test sequence, hold CHANNEL depressed and depress RESET, the sequence will start at Test 0.

Test descriptions

57. Display format. Fig. 13 shows the positions of the 2833A display digits as referred to in the following test descriptions.

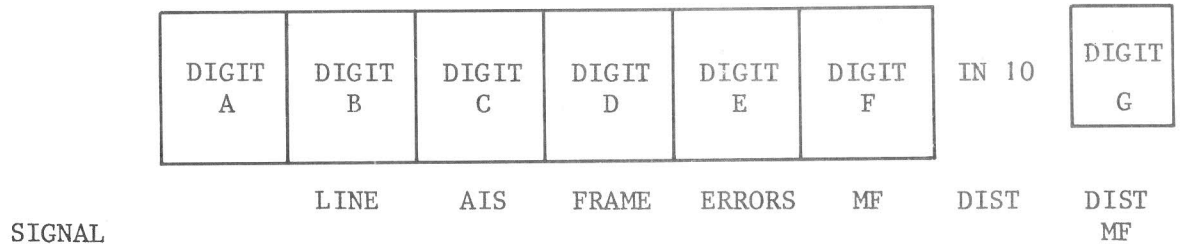


Fig. 13 Display format for test routines

58. Test 0 - Processor running test. The LED displays on the 2833A front panel are all turned on and off at a 1 Hz rate with the exception of the five FUNCTION LED s which all turn on and off at the same rate but exactly out of phase with the rest of the displays. On the 8th alternation between the two display groups the Buzzer is activated and the test sequence commences Test 1. However if STOP is depressed or IC1 pin 5 (SID) is connected to a +5 V line, Test 0 is repeated until STOP is deselected or SID is removed.

59. If any one of these three actions is operating correctly, it is probable that the processor is running. If any of the above three operations are faulty, further tests can be carried out at this stage or at its individual test later on.

60. Test 1 - Chip enable test. This test allows the chip enable decoding to be monitored with an oscilloscope. The displays should all be illuminated, but this may not be the case depending on the fault.

(1) Connect the oscilloscope to IC1 pin 4 (SOD) and use this as a trigger. The signal should be a positive pulse occurring every 90 µs.

(2) Adjust the controls of the oscilloscope so that a pulse can be seen at each side of the screen.

(3) With the oscilloscope, monitor the chip enable output pins on IC4 except for pin 15. There should be a negative pulse at the left side of the screen for pin 14, the pulse successively moving across to the right side of the screen for each of the intermediate pins up to pin 7. Some of the lines may exhibit occasional extra pulses and glitches. The chip enable lines can be monitored at the input of each device but if the lines are gated with read or write lines, the chip enable pulses will be narrower.

61. Test 2 - Display and pen recorder test. This test checks both display chips (IC9 and IC10) and the pen recorder circuit (IC8 and IC15). The test is a sequence of eleven steps where it is possible to stop at each one if required, by selecting STOP or connecting SID to +5 V. The correct sequence is shown in Table 1.

62. If the pen recorder f.s.d. range is set to 1 mA, divide the output current readings in Table 1 by 5.

Note...

This test enables the outputs of display multiplexer IC9 to be monitored i.e. the information it assumes it has received. It is not possible to check the data at the inputs of IC9.

TABLE 1 DISPLAY AND PEN RECORDER TEST SEQUENCE

Sub test	*All digits*	*Decimal point*	*Alarm LED*	*Function*	*Other LEDs*	*Pen recorder output*	
						Rear panel (mA)	*IC8 pins 3,6,11 and 14*
1						0.0	1111
2	Zero		OVERFLOW	EXT COUNT	IN 10	0.5	0111
3	One		LINE	8M CODE		1.0	1011
4	Two	Digit F	AIS	2M CODE	SIGNAL	1.5	0011
5	Three	Digit E	FRAME	2M ALIGN		2.0	1101
6	Four	Digit D	ERRORS	2M SIG	BOTH	2.5	0101
7	Five	Digit C	MF	EXT COUNT		3.0	1001
8	Six	Digit B	DIST	8M CODE	SIGNAL	3.5	0001
9	Seven	Digit A	DMF	2M CODE		4.0	1110
10	Eight			2M ALIGN	IN 10	4.5	0110
11	Nine			2M SIG		5.0	1010

63. Test 3 - RAM test. This test fills the RAM with data and checks that this RAM data is correct. The RAM is then filled with the complement of the first data and checks that this data is also correct. During the test, the test number 3 is displayed by digit G. If the test passes, the number 3 is displayed by digit F. If the test fails, the number 1 or 2 is displayed by digit F.

64. Test 4 - EPROM test. This test checks the two halves of the EPROM by adding up all of the data contained in each half. A check sum is performed using modulo 256 i.e.

$$\text{Check sum (remainder)} = \frac{\text{Total number of data (bytes)}}{256}$$

65. During the test, the test number 4 is displayed by digit G. The check sum for the first half is displayed by digits A to C and the check sum for the second half is displayed by digits D to F. The check sum value depends on the software version of the 2833A. The check sum for the standard version is listed below.

EPROM Part No.	*Version*	*Check sum*
44533-171H	1	071 064

66. Test 5 - Input lines test. This test checks whether or not the processor is able to read all of the front panel function input lines and enables a fault condition if present to be monitored. Each display digit from A to F displays the state of one of three input lines by assigning a binary weighting to each line. In this test, the test number 5 is displayed by digit G. Table 2 shows the relationship between the input lines and display digits.

Note...

Due to the nature of this test and because it does not follow a sequence, STOP is not required to prevent commencement of the next test.

TABLE 2 INPUT LINES TEST

Weight	*Digit A*	*Digit B*	*Digit C*	*Digit D*	*Digit E*	*Digit F*
1	STOP	LAMP TEST	BUZZER ON	AUTO RESET	MF	LINE
2	RESET	SELF TEST	FUNCTION UP	CHANNEL	DIST	AIS
4	TOTAL	-	FUNCTION DOWN	BUZZER-ERRORS	DMF	FRAME

67. Example. If FUNCTION UP and FUNCTION DOWN are selected simultaneously and BUZZER ON is not selected, digit C will display the number 6, i.e., (2 + 4) = 6. An incorrect number indicates a faulty input line.

Notes...

1. The alarm lines and their corresponding display digits will be undefined apart from LINE unless a frame aligned p.c.m. signal is connected to the 2833A INPUT.
2. If SELF TEST is selected, digit F will display the number 2 (SELF TEST signal represents AIS) together with the number 2 displayed by digit B as expected.
3. When AIS is present and displayed on digit F, it is quite common for MF to also be indicated on digit E. This is a function of the way the 2833A detects the error and is not a fault.

68. Progressing to the next test. If it is desired to stop at the next test, ensure STOP is selected before progressing. To progress to the next test, select RESET and LAMP TEST together.

69. Test 6 - Output lines test. This test consists of a sequence of sub-tests that set the output lines to a predetermined t.t.l. logic level. During the test, the test number 6 is displayed by digit G and the sub-test number by digits E and F. Each sub-test can be stopped for monitoring purposes by selecting STOP. The output lines affected by this test are listed below.

Sub-test	*Line*	*Destination (title)*
00	All output lines high	
01	All output lines low	
02	Only PC3 8155 (IC7 pin 1) high	(IC14A)
03	Only PC4 8155 (IC7 pin 2) high	(IC14B)
04	Only PC5 8155 (IC7 pin 5) high	(2/8L)
05	Only PA0 8255 (IC16 pin 4) high	(CH/TS0)
06	Only PA1 8255 (IC16 pin 3) high	(CH/TS1)

Sub-test	*Line*	*Destination (title)*
07	Only PA2 8255 (IC16 pin 2) high	(CH/TS2)
10	Only PA3 8255 (IC16 pin 1) high	(CH/TS3)
11	Only PA4 8255 (IC16 pin 40) high	(CH/TS4)
12	Only PA5 8255 (IC16 pin 39) high	(BUZZER)
13	Only PA6 8255 (IC16 pin 38) high	(Alarms)
14	Only PA7 8255 (IC16 pin 37) high	(C1A)

Notes.

1. Sub-tests 00 and 12 activate the buzzer.

2. To initiate the next test after sub-test 14, de-select STOP.

70. Test 7 - Counter test. This test enables the errors counting chain to be checked and requires no p.c.m. signal at the 2833 A INPUT. Pulses generated by a logic pulser can be fed into the code error counter chain and the total count is displayed by the 2833A. The clock counting chain i.e. IC13b,IC18 etc. can be checked when the instrument is functioning normally. Test number 7 is displayed by digit G.

71. Multiplexer IC14 is set up to accept pulses at IC14 pin 11 and to route them to IC14 pin 9.

(1) Insert pulses from a logic pulser to IC14 pin 11. IC13a and IC12 will count the pulses.

(2) When a desired number of pulses have been fed in, apply a single pulse to IC7 pin 39 to latch in the count and to reset the counters.

(3) Depress CHANNEL, the total number of pulses should be displayed by digits C to F. If the count is incorrect, the number displayed should help to localize the fault.

72. Monitoring counter output pins. Because IC13a latches its count into IC7, the monitoring of its output pins should be made before applying a pulse to IC7 pin 39. The least significant decade can be monitored at IC13a output pins 9, 10, 11 and 12.

73. IC12 latches its count internally and therefore to monitor its output, IC7 pin 39 must be pulsed first. Each of the three more significant decades can be checked separately at output pins 5, 6, 7 and 9 by pulsing C1A IC12 pin 4. To check which decade is being latched out, monitor IC12 pin 2, 1 and 15. The conditions are as follows:-

When pin 2 is low, the least significant digit should be present at IC12 output.

When pin 1 is low, the middle digit should be present at IC12 output.

When 15 is low, the most significant digit should be present at IC12 output.

Note. Test 7 can be repeated for as many times as is required.

FUSE REPLACEMENT

74. Two a.c. mains cartridge-type fuses are located on the rear panel. These a.c. main supply fuses are sloe-blow, 500 mA for 105 to 120 V range and 250 mA for 210 to 240 V range. In addition to the two a.c. main supply fuses, a 2 A slow-blow cartridge-type fuse is fitted in the 12 V d.c. supply.

REPLACEMENT OF SUPPLY ON/OFF SWITCH

75. *WARNING.*

If the power SUPPLY ON/OFF switch has to be replaced, it is important to ensure that the incoming a.c. supply and d.c. supply leads are connected to the bottom row of tags on the back of the switch. The outgoing leads should be connected to the centre row of tags. If the incoming and outgoing leads become transposed, the top row of tags will be live when the instrument is switched off.

Chapter 6

REPLACEABLE PARTS

CONTENTS

INTRODUCTION

1. Each sub-assembly or printed circuit board in this equipment has been allocated a reference designator code, e.g. A0, A1, A2 etc.

2. The complete component reference includes its reference designator as a prefix e.g. A3C1 (capacitor C1 on sub-assembly A3) but for convenience in the text and diagrams the prefix is omitted unless it is needed to avoid confusion. However when ordering replacements or in correspondence the complete component reference must be quoted.

ABBREVIATIONS

3. Electrical components are listed in alpha-numerical order of their complete circuit reference and the following standard abbreviations are used:

ADC	analogue-digital converter
CAP	capacitor
CARR	carrier
CARB	carbon
CC	carbon composition
CDE CNV	code converter
CER	ceramic
CERM	cermet
CF	carbon film

COAX	coaxial
CON	connector
CTR	counter
DAC	digital-analogue converter
DEC/DMX	decoder/demultiplexer
DECOD	decoder
DIL	dual in-line
DIV	divider
DRIV	driver
ELEC	electrolytic
ENCOD	encoder
FEM	female
FF	flip-flop (bistable)
FILTERCON	filtering capacitor
GER	germanium
GP	general purpose
ICA	integrated circuit, analogue
ICD	integrated circuit, digital
IND	inductor
INV	inverter
MF	metal film
MG	metal glaze
MISC	miscellaneous
MO	metal oxide
MP	microprocessor
MP SUPP	microprocessor support
MUX	multiplexer
NET	network
PLAS	plastic
PLL	phase-locked loop
Q/ACT	quick acting
RECT	rectifier
RES	resistor
RV	resistor, variable
RX	receiver
SAPPH	sapphire
SEC	secondary
SH REG	shift register
SIL	silicon
SW	switch
T/LAG	time lag
TANT	tantalum
TOG	toggle
TRANS	transistor
TX	transmitter

VAR	variable
VREG	voltage regulator
WW	wirewound
!	static sensitive component

COMPONENT VALUES

4. One or more of the components fitted in the equipment may differ from those listed in this chapter for any of the following reasons:

(a) Components indicated by a * have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the equipment is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the equipment.

ORDERING

6. When ordering replacements, address the order to our Service Division (address on rear cover) or nearest agent and specify the following for each component required:-

(1) Type[#] and serial number of equipment.

(2) Complete circuit reference.

(3) Description.

(4) Part number.

[#] As given on the serial number label at the rear of the equipment; if this is superseded by a model number label, quote the model number instead of the type number.

Circuit Ref	Description	Part Number
Unit A0	OVERALL ASSEMBLY	(52833-910Z)
	7. When ordering, prefix circuit reference with A0.	
FS1	FUSE T/LAG .25A 20X5MM	23411-055P
FS2	FUSE T/LAG .25A 20X5MM	23411-055P
FS3	FUSE T/LAG 2.0A 20X5MM	23411-060M
PLA	CON PWR MALE 3 FXD RF FILTER	23423-150L
SA	SW SLIDE DPCO PANEL MTG	23467-161W
SB	SW TOG 4P2W MIN ON-ON	23462-266S
SC	SW TOG 3 CO MIN LOCK LEVER	23462-303V
SKA	CON MIN FEM 1 FXD 4MM WHITE	23421-153W
SKB	CON MIN FEM 1 FXD 4MM WHITE	23421-153W
SKC	CON RF BNC FEM 50 BKHD	23443-442B
SKD	CON RF BNC FEM 50 BKHD	23443-442B
T1	MAINS TRANSFORMER	43490-077U
X55	PCB INTERCONNECTION BOARD	31828-650R
Unit A1	DISPLAY BOARD	
	8. When ordering, prefix circuit reference with A1.	
	Complete unit	44828-647Z
D1	DIODE LED 7653 2.2V RED 7SEG	28624-225E
D2	DIODE LED 7653 2.2V RED 7SEG	28624-225E
D3	DIODE LED 7653 2.2V RED 7SEG	28624-225E
D4	DIODE LED 7653 2.2V RED 7SEG	28624-225E
D5	DIODE LED 7653 2.2V RED 7SEG	28624-225E
D6	DIODE LED 7653 2.2V RED 7SEG	28624-221K
D7	DIODE LED 7613 2V RED 7SEG	28624-220B
D8	DIODE LED HLMP0301 3V RED	28624-118Z
D9	DIODE LED HLMP0301 3V RED	28624-118Z
D10	DIODE LED HLMP0301 3V RED	28624-118Z
D11	DIODE LED HLMP0301 3V RED	28624-118Z
D12	DIODE LED HLMP0301 3V RED	28624-118Z
D13	DIODE LED HLMP0301 3V RED	28624-118Z
D14	DIODE LED HLMP0301 3V RED	28624-118Z
D15	DIODE LED HLMP0301 3V RED	28624-118Z

Circuit Ref	Description	Part Number
Unit A1	DISPLAY BOARD	(Contd.)
D16	DIODE LED HLMP0301 3V RED	28624-118Z
D17	DIODE LED HLMP0301 3V RED	28624-118Z
D18	DIODE LED HLMP0301 3V RED	28624-118Z
D19	DIODE LED HLMP0301 3V RED	28624-118Z
D20	DIODE LED HLMP0301 3V RED	28624-118Z
D21	DIODE LED HLMP0301 3V RED	28624-118Z
D22	DIODE LED 2300 1.9V RED BAR	28624-123E
IC1	ICD DECOD 4511 BCD-7SEG	28465-014K
LK1	CON JUMP MALE 25 FREE 3"LG	23436-110G
R1	RES MF 100K 1/4W 2%	24773-321L
R2	RES MF 100K 1/4W 2%	24773-321L
R3	RES MF 100K 1/4W 2%	24773-321L
R4	RES MF 100K 1/4W 2%	24773-321L
R5	RES MF 1KO 1/4W 2%	24773-273A
R6	RES MF 47R 1/4W 2%	24773-241A
R7	RES MF 30R 1/4W 2%	24773-236B
R8	RES MF 1KO 1/4W 2%	24773-273A
R9	RES MF 1KO 1/4W 2%	24773-273A
R10	RES MF 4R7 1/4W 2%	24773-217J
TR1	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR2	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR3	TRANS PNP SIL BC308 25V	28433-455R

Circuit Ref	Description		Part Number
Unit A12	PROCESSOR BOARD		
9. When ordering, prefix circuit reference with A12.			
	Complete unit		44829-143X
C1	CAP ELEC 4U7 35V 20% SUBMIN		26421-108A
C2	CAP CER 33P 63V 5% PLATE		26343-471Y
C3	CAP CER 100P 63V 2% PLATE		26343-477V
C4	CAP CER 330P 63V 2% PLATE		26343-483D
C5	CAP CER 10N 25V 20% DISC		26383-006C
C6	CAP ELEC 220U 16V 20%+ PCB		26421-124G
C7	CAP CER 10N 25V 20% DISC		26383-006C
C8	CAP CER 10N 25V 20% DISC		26383-006C
C9	CAP CER 10N 25V 20% DISC		26383-006C
C10	CAP CER 10N 25V 20% DISC		26383-006C
C11	CAP CER 10N 25V 20% DISC		26383-006C
C12	CAP CER 10N 25V 20% DISC		26383-006C
C13	CAP CER 10N 25V 20% DISC		26383-006C
C14	CAP CER 10N 25V 20% DISC		26383-006C
C15	CAP CER 10N 25V 20% DISC		26383-006C
C16	CAP ELEC 22U 100V 20%+ PCB		26421-120N
C17	CAP CER 100N 30V 20% DISC		26383-031S
C18	CAP CER 10N 25V 20% DISC		26383-006C
C19	CAP CER 10N 25V 20% DISC		26383-006C
C20	CAP CER 10N 25V 20% DISC		26383-006C
C21	CAP CER 10N 25V 20% DISC		26383-006C
C22	CAP CER 10N 25V 20% DISC		26383-006C
C23	CAP CER 10N 25V 20% DISC		26383-006C
C24	CAP CER 10N 25V 20% DISC		26383-006C
C25	CAP CER 10N 25V 20% DISC		26383-006C
C26	CAP CER 10N 25V 20% DISC		26383-006C
C27	CAP CER 1N0 63V 10% PLATE		26383-585M
C28	CAP CER 1N0 63V 10% PLATE		26383-585M
C29	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
C30	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
D1	DI SIL 1N4148 75V JUNC		28336-676J
IC1	ICD MP P8085A 8BIT NMOS	!	28469-396K
IC2	ICD OR 4072 DUAL 4INP	!	28466-106H
IC3	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC4	ICD DEC/DMX 74LS138 3-8		28465-027F
IC5	ICD PROM 2764 8x8K 250NS UV	!	44533-171H

Circuit Ref	Description		Part Number
Unit A12	PROCESSOR BOARD		(Contd.)
IC6	ICA VREG 7660 POS-NEG CONVTR	!	28461-742G
IC7	ICD MP SUP 8155 2KRAM+I/O+TIM	!	28469-304E
IC8	ICD FF D 40175 QUAD	!	28462-617N
IC9	ICD DRIV 7218 8 DIGIT LED	!	28467-009X
IC10	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC11	ICD MONO 74LS123 DUAL RETR		28468-309B
IC12	ICD CTR 4553 3 DIGIT BCD	!	28464-131B
IC13	ICD CTR 74LS390 DUAL 4BIT DEC		28464-127R
IC14	ICD MUX 74LS153 DUAL 4INP		28469-711K
IC15	ICA AMP UA741CN GP DIL8		28461-304T
IC16	ICD MP SUP 8255A PROG PERI INT	!	28467-002G
IC17	ICD FF D 74LS374 OCT +E TR 3ST		28462-618L
IC18	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC19	ICD OR 74LS32 QUAD 2INP		28466-108U
IC20	ICD OR 4071 QUAD 2INP BI	!	28466-403P
IC21	ICA MISC TL7705 SUPPLY MONITOR		28461-930R
IC22	ICD CTR 74LS393 DUAL 4BIT BIN		28464-130R
IC23	ICD OR 74LS32 QUAD 2INP		28466-108U
IC24	ICD MUX 74LS151 8INP		28469-715E
IC25	ICD BUFF 74LS244 OCT 3ST		28469-182T
IC26	ICD MP SUP 8251A USART DIL28	!	28469-189K
IC27	ICD DRIV 75188 QUAD RS232		28469-167N
IC28	ICD RX 75189 QUAD RS232		28469-165U
R1	RES MF 15K 1/4W 2% 100PPM		24773-301P
R2	RES MF 15K 1/4W 2% 100PPM		24773-301P
R3	RES MF 15K 1/4W 2% 100PPM		24773-301P
R4	RES MF 15K 1/4W 2% 100PPM		24773-301P
R5	RES MF 10R 1/4W 2% 100PPM		24773-225W
R6	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R7	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R8	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R9	RES MF 180R 1/4W 2% 100PPM		24773-255V
R10	RV CERM 50R LIN .5W 10% HORZ		25711-634N
R11	RES MF 200R 1/4W 2% 100PPM		24773-256S
R12	RES MF 200R 1/4W 2% 100PPM		24773-256S
R13	RES MF 200R 1/4W 2% 100PPM		24773-256S
R14	RES MF 200R 1/4W 2% 100PPM		24773-256S
R15	RES MF 200R 1/4W 2% 100PPM		24773-256S
R16	RES MF 24K 1/4W 2% 100PPM		24773-306B
R17	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R18	RES MF 12K 1/4W 2% 100PPM		24773-299R
R19	RES MF 200K 1/4W 2% 100PPM		24773-328D
R20	RES MF 200K 1/4W 2% 100PPM		24773-328D

Circuit Ref	Description	Part Number
Unit A12	PROCESSOR BOARD	(Contd.)
R21	RES MF 100K 1/4W 2% 100PPM	24773-321L
R22	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R23	RES MF 200K 1/4W 2% 100PPM	24773-328D
R24	RES MF 100K 1/4W 2% 100PPM	24773-321L
R25	RES MF 100K 1/4W 2% 100PPM	24773-321L
R26	RES MF 470R 1/4W 2% 100PPM	24773-265M
R27	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R28	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R29	RV CERM 200R LIN .5W 10% HORZ	25711-636J
R30	RES MF 100K 1/4W 2% 100PPM	24773-321L
R31	RES MF 100K 1/4W 2% 100PPM	24773-321L
R32	RES MF 910R 1/4W 2% 100PPM	24773-272K
R33	RES NET 10K 5% 9SIP	24681-640V
R34	RES NET 100KO 5% 9SIP	24681-634J
R35	RES MF 100K 1/4W 2% 100PPM	24773-321L
R36	RES MF 15K 1/4W 2% 100PPM	24773-301P
R37	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R38	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R39	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R40	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R41	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R42	RES MF 12K 1/4W 2% 100PPM	24773-299R
R43	RES MF 12K 1/4W 2% 100PPM	24773-299R
R44	RES MF 12K 1/4W 2% 100PPM	24773-299R
R45	RES MF 220R 1/4W 2% 100PPM	24773-257W
R46	RES NET 4K7 5% 9SIP	24681-611D
R47	RES MF 100K 1/4W 2% 100PPM	24773-321L
R48	RES NET 100KO 5% 9SIP	24681-634J
R49	RES MF 100K 1/4W 2% 100PPM	24773-321L
R50	RES MF 100K 1/4W 2% 100PPM	24773-321L
R51	RES MF 10K 1/4W 2% 100PPM	24773-297M
R52	RES MF 10K 1/4W 2% 100PPM	24773-297M
R53	RES MF 10K 1/4W 2% 100PPM	24773-297M
R54	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R55	RES MF 4K7 1/4W 2% 100PPM	24773-289W
SA	SW PUSH -	44338-115A
SB	SW PUSH -	44338-116Z
SKA	CON EDGE FEM 30 FXD .1" 2S K18	23435-063X
SKB	CON PCB FEM 25 FXD FLEX WIRE	23436-196E
TR1	TR NSI BC209C 20V 150M - GEN	28452-771P
TR2	TR PSI BC308B 20V 130M - GEN	28433-455R
TR3	TR PSI BC308B 20V 130M - GEN	28433-455R

Circuit Ref	Description	Part Number
Unit A12	PROCESSOR BOARD	(Contd.)
X7	BUZZER 6V 18MA 400HZ PCB	23646-150L
XL1	XTAL 4.9152M P30P 50R	28312-099M
	CON JUMP FEM 2 1 ROW	23435-990X
	S/C ACC SKT DIL40 LOW PROFILE	28488-046J
	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
Unit A3	INPUT AND ALIGNMENT BOARD	
10. When ordering, prefix circuit reference with A3.		
	Complete unit	44828-649E
C3	CAP CER 1.8PF 63V .5PF PLATE	26343-456C
C4	CAP CER 18PF 63V .5PF PLATE	26343-468Y
C5	CAP CER 0.047UF 25V 20% DISC	26383-017U
C6	CAP CER 0.01UF 25V 20% DISC	26383-006C
C7	CAP TANT 2.2UF 35V 20% DISC	26486-214V
C8	CAP CER 0.01UF 25V 20% DISC	26383-006C
C9	CAP TANT 2.2UF 35V 20% DISC	26486-214V
C10	CAP TANT 1.0UF 35V 20% DISC	26486-209F
C11	CAP CER 0.01UF 25V 20% DISC	26383-006C
C12	CAP CER 0.01UF 25V 20% DISC	26383-006C
C13	CAP CER 270PF 63V 2% PLATE	26343-482W
C14	CAP CER 270PF 63V 2% PLATE	26343-482W
C15	CAP PLAS 150PF 63V 2%	26538-571R
C16	CAP PLAS 620PF 63V 2%	26538-832G
C17	CAP CER 0.01UF 25V 20% DISC	26383-006C
C18	CAP CER 12PF 63V 5% PLATE	26343-466E
C19	CAP CER 56PF 63V 2% PLATE	26343-474J
C20	CAP CER 0.01UF 25V 20% DISC	26383-006C
C21	CAP CER 82PF 63V 2% PLATE	26343-476G
C22	CAP CER 47PF 63V 5% PLATE	26343-473L
C23	CAP CER 0.01UF 25V 20% DISC	26383-006C
C24	CAP CER 0.01UF 25V 20% DISC	26383-006C
C25	CAP CER 0.01UF 25V 20% DISC	26383-006C
C26	CAP CER 0.01UF 25V 20% DISC	26383-006C
C27	CAP CER 0.01UF 25V 20% DISC	26383-006C
C28	CAP CER 0.01UF 25V 20% DISC	26383-006C
C29	CAP CER 0.01UF 25V 20% DISC	26383-006C
C30	CAP CER 0.01UF 25V 20% DISC	26383-006C
C31	CAP CER 0.01UF 25V 20% DISC	26383-006C
C32	CAP CER 0.01UF 25V 20% DISC	26383-006C

Circuit Ref	Description	Part Number
UNIT A3	INPUT AND ALIGNMENT BOARD	(Contd.)
C33	CAP CER 0.01UF 25V 20% DISC	26383-006C
C34	CAP CER 0.01UF 25V 20% DISC	26383-006C
C35	CAP CER 0.01UF 25V 20% DISC	26383-006C
C36	CAP CER 0.01UF 25V 20% DISC	26383-006C
C37	CAP CER 0.01UF 25V 20% DISC	26383-006C
C38	CAP CER 0.01UF 25V 20% DISC	26383-006C
C39	CAP CER 0.01UF 25V 20% DISC	26383-006C
C40	CAP CER 0.01UF 25V 20% DISC	26383-006C
C41	CAP CER 0.01UF 25V 20% DISC	26383-006C
C42	CAP CER 0.01UF 25V 20% DISC	26383-006C
C43	CAP ELEC 2200UF 25V -10+30%	26422-322D
C44	CAP ELEC 1UF 63V 20%+ P/CCT	26423-201V
C45	CAP ELEC 4700UF 25V -10+30%	26422-323T
C46	CAP CER 0.01UF 25V 20% DISC	26383-006C
C47	CAP ELEC 1UF 63V 20%+ P/CCT	26423-201V
C48	CAP CER 0.01UF 25V 20% DISC	26383-006C
C49	CAP ELEC 1UF 63V 20%+ P/CCT	26423-201V
C50	CAP CER 100PF 63V 2% PLATE	26343-437N
C51	CAP CER 100PF 63V 2% PLATE	26343-477V
C52	CAP TANT 2.2UF 35V 20% DISC	26486-214V
C53	CAP CER 100PF 63V 2% PLATE	26343-477V
C54	CAP CER 0.01UF 25V 20% DISC	26383-006C
C55	CAP TANT 2.2UF 35V 20% DISC	26486-214V
C56	CAP TANT 2.2UF 35V 20% DISC	26486-214V
C57	CAP CER 0.01UF 25V 20% DISC	26383-006C
C58	CAP CER .0022UF 63V 10% PLATE	26383-587R
C59	CAP CER .0022UF 63V 10% PLATE	26383-587R
C60	CAP VAR CER 60PF-10PF TRIM	26847-267D
D1	DIODE SIL 1N4148 100V JUNC	28336-676J
D2	DIODE SIL 1N4148 100V JUNC	28336-676J
D3	DIODE SIL 1N4148 100V JUNC	28336-676J
D4	DIODE SIL 1N4148 100V JUNC	28336-676J
D5	DIODE SIL 1N4148 100V JUNC	28336-676J
D6	DIODE SIL 1N4148 100V JUNC	28336-676J
D7	DIODE SIL 1N4148 100V JUNC	28336-676J
D8	DIODE HOT CARR BAT 29	28349-014L
D9	DIODE SIL 1N4148 100V JUNC	28336-676J
D10	DIODE SIL 1N4148 100V JUNC	28336-676J
D11	DIODE SIL 1N4148 100V JUNC	28336-676J
D12	DIODE SIL 1N4148 100V JUNC	28336-676J
D13	DIODE SIL 1N4148 100V JUNC	28336-676J
D14	DIODE SIL 1N4148 100V JUNC	28336-676J
D17	DIODE RECT 1N5401 100V	28355-723N

Circuit Ref	Description		Part Number
Unit A3	INPUT AND ALIGNMENT BOARD		(Contd.)
D18	DIODE RECT 1N4004 400V		28357-028K
D19	DIODE RECT 1N4004 400V		28357-028K
D20	DIODE RECT 1N4004 400V		28357-028K
D21	DIODE RECT 1N4004 400V		28357-028K
D22	DIODE RECT 1N4004 400V		28357-028K
D23	DIODE RECT 1N5401 100V		28355-723N
D24	DIODE RECT 1N5401 100V		28355-723N
D25	DIODE RECT 1N5401 100V		28355-723N
D26	DIODE RECT 1N5401 100V		28355-723N
D27	DIODE ZENER BZX79 C4V7 5%		28371-371F
IC1	ICA AMP UA733PC DIF VID DIL14		28461-910N
IC2	ICD NOR 4001 QUAD 2INP	!	28466-207Z
IC3	ICD FF D 4013 DUAL	!	28462-608A
IC4	ICD FF D 4013 DUAL	!	28462-608A
IC5	ICD FF D 74S74 DUAL +EDG TR		28462-607K
IC6	ICD FF JK 74LS76 DUAL M/SLAVE		28462-019R
IC7	ICD AND 74LS08 QUAD 2INP		28466-012L
IC8	ICD NOR 74LS02 QUAD 2INP		28466-214Y
IC9	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC10	ICA ARRAY CA3046 5 NPN TRAN		28461-901A
IC11	ICD MISC ZNA5H016J ULA PCM RX		28469-408Y
IC12	ICD MISC ZNA2H086J ULA PCM DEC		28469-407U
IC13	ICD MUX 74LS151 8 I/P		28469-715E
IC14	ICD MUX 74LS153 DUAL 4INP		28469-711K
IC15	ICA MUX 4051 8INP	!	28469-708K
IC16	ICA MUX 4051 8INP	!	28469-708K
IC17	ICD SH REG 74LS164 8BIT SIPO		28467-515G
IC18	ICD SH REG 4014 8BIT PISO	!	28467-520S
IC19	ICD NAND 74LS10 TRIP 3INP		28466-351Y
IC20	ICD NOR 4001 QUAD 2INP	!	28466-207Z
IC21	ICD AND 4081 QUAD 2INP	!	28466-009L
IC22	ICD XOR 4070 QUAD 2INP	!	28466-402T
IC23	ICD FF D 4013 DUAL	!	28462-608A
IC24	ICD OR 4075 TRIP 3INP	!	28466-107E
IC25	ICA ARRAY CA3046 5 NPN TRAN		28461-901A
IC26	ICA AMP LM324N QUAD GP DIL14		28461-322U
IC27	ICA VREG+ MC7805CT 5V 1A TO220		28461-707G
IC28	ICA VREG+ MC7805CT 5V 1A TO220		28461-707G
L1	IND CHOKE 4.7UH 10% LAQ		23642-553J
L2	IND CHOKE 150UH 10% LAQ		23642-562D
L3	INDUCTOR		44290-855H
L4	INDUCTOR		44290-856E
L5	IND CHOKE 4.7UH 10% LAQ		23642-553J

Circuit Ref	Description	Part Number
Unit A3	INPUT AND ALIGNMENT BOARD	(Contd.)
L6	IND CHOKE 4.7UH 10% LAQ	23642-553J
R1	RES MF 100R 1/4W 2%	24773-249J
R2	RES MF 270R 1/4W 2%	24773-259T
R3	RES MF 8R2 1/4W 2%	24773-223V
R4	RES MF 300R 1/4W 2%	24773-260W
R5	RES MF 430R 1/4W 2% *	24773-264X
R6	RES MF 220R 1/4W 2% *	24773-257W
R7	RES MF 100K 1/4W 2%	24773-321L
R8	RES MF 10K 1/4W 2%	24773-297M
R9	RES MF 560K 1/4W 2%	24773-340R
R10	RES MF 430R 1/4W 2%	24773-264X
R11	RES MF 1KO 1/4W 2%	24773-273A
R12	RES MF 750R 1/4W 2%	24773-270R
R13	RES MF 1KO 1/4W 2%	24773-273A
R14	RES MF 1KO 1/4W 2%	24773-273A
R15	RES MF 47R 1/4W 2%	24773-241A
R16	RES MF 47R 1/4W 2%	24773-241A
R17	RES MF 47R 1/4W 2%	24773-241A
R18	RES MF 620R 1/4W 2%	24773-268B
R19	RES MF 300R 1/4W 2%	24773-260W
R20	RES MF 560R 1/4W 2%	24773-267R
R21	RES MF 300R 1/4W 2%	24773-260W
R22	RES MF 390R 1/4W 2%	24773-263P
R23	RES MF 390R 1/4W 2%	24773-263P
R24	RES MF 470R 1/4W 2%	24773-265M
R25	RES MF 12K 1/4W 2%	24773-299R
R26	RES MF 6K8 1/4W 2%	24773-293D
R27	RES MF 510R 1/4W 2%	24773-266C
R28	RES MF 510R 1/4W 2%	24773-266C
R29	RES MF 2K7 1/4W 2%	24773-283L
R30	RES MF 2K7 1/4W 2%	24773-283L
R31	RES MF 4K7 1/4W 2%	24773-286G
R32	RES MF 9K1 1/4W 2%	24773-296X
R33	RES MF 1K3 1/4W 2%	24773-276E
R34	RES MF 470R 1/4W 2%	24773-265M
R35	RES MF 470R 1/4W 2%	24773-265M
R36	RES MF 470R 1/4W 2%	24773-265M
R37	RES MF 470R 1/4W 2%	24773-265M
R38	RES MF 560R 1/4W 2%	24773-267R
R39	RES MF 680R 1/4W 2%	24773-269K

Circuit Ref	Description	Part Number
Unit A3	INPUT AND ALIGNMENT BOARD	(Contd.)
R40	RES MF 200R 1/4W 2%	24773-256S
R41	RES MF 1K3 1/4W 2%	24773-276E
R42	RES MF 680R 1/4W 2%	24773-269K
R43	RES MF 560R 1/4W 2%	24773-267R
R44	RES MF 1KO 1/4W 2%	24773-273A
R45	RES MF 1KO 1/4W 2%	24773-273A
R46	RES MF 1KO 1/4W 2%	24773-273A
R47	RES MF 1KO 1/4W 2%	24773-273A
R48	RES MF 1KO 1/4W 2%	24773-273A
R49	RES MF 680R 1/4W 2%	24773-269K
R50	RES MF 200R 1/4W 2%	24773-256S
R51	RES MF 1K5 1/4W 2%	24773-277U
R52	RES MF 100K 1/4W 2%	24773-321L
R53	RES MF 270R 1/4W 2%	24773-259T
R54	RES MF 15K 1/4W 2%	24773-301P
R55	RES MF 15K 1/4W 2%	24773-301P
R56	RES MF 100R 1/4W 2%	24773-249J
R57	RES MF 22K 1/4W 2%	24773-305R
R58	RES MF 22K 1/4W 2%	24773-305R
R59	RES MF 12K 1/4W 2%	24773-299R
R60	RES MF 12K 1/4W 2%	24773-299R
R61	RES MF 1KO 1/4W 2%	24773-273A
R62	RES MF 2K7 1/4W 2%	24773-283L
R63	RES MF 680R 1/4W 2%	24773-269K
R64	RES MF 62R 1/4W 2%	24773-244E
R65	RES MF 62R 1/4W 2%	24773-244E
R66	RES MF 1KO 1/4W 2%	24773-273A
R67	RES MF 2K7 1/4W 2%	24773-283L
R68	RES MF 100K 1/4W 2%	24773-321L
R69	RES MF 100K 1/4W 2%	24773-321L
R70	RES MF 100K 1/4W 2%	24773-321L
R71	RES MF 4K7 1/4W 2%	24773-289W
R72	RES MF 4K7 1/4W 2%	24773-289W
R74	RES MF 4K7 1/4W 2%	24773-289W
R75	RES NET 15KO 5% 9SIP 5%	24681-603F
R76	RES NET 15KO 5% 9SIP 5%	24681-603F
R77	RES MF 2KO 1/4W 2%	24773-280U
R78	RES MF 4K7 1/4W 2%	24773-289W
R79	RES MF 5K6 1/4W 2%	24773-291S
R80	RES MF 4K7 1/4W 2%	24773-289W

Circuit Ref	Description	Part Number
Unit A3	INPUT AND ALIGNMENT BOARD (Contd.)	
R81	RES MF 2K0 1/4W 2%	24773-280U
R82	RES MF 4K7 1/4W 2%	24773-289W
R83	RES MF 4K7 1/4W 2%	24773-289W
R84	RES MF 56R 1/4W 2%	24773-243H
R85	RES MF 56R 1/4W 2%	24773-243H
R86	RES MF 300R 1/4W 2%	24773-260W
R87	RES MF 5K6 1/4W 2%	24773-291S
R88	RES MF 5K6 1/4W 2%	24773-291S
R89	RES MF 10K 1/4W 2%	24773-297M
R90	RES MF 470R 1/4W 2%	24773-265M
R91	RES MF 5K6 1/4W 2%	24773-291S
R92	RV CERM 1K0 LIN .5W 10% HORZ	25711-638G
R93	RES MF 2K0 1/4W 2%	24773-280U
R94	RES MF 150R 1/4W 2%	24773-253F
R95	RES MF 7K5 1/4W 2%	24773-294T
R96	RES MF 2K0 1/4W 2%	24773-280U
R97	RES MF 4K7 1/4W 2%	24773-289W
R98	RES MF 4K7 1/4W 2%	24773-289W
R99	RES MF 2K0 1/4W 2%	24773-280U
R100	RES MF 75R 1/4W 2%	24773-246Y
R101	RES MF 4K7 1/4W 2%	24773-289W
R102	RES MF 3K9 1/4W 2%	24773-287V
R103	RES MF 4K7 1/4W 2%	24773-289W
R104	RES MO 150R 1/2W 2%	24573-053K
R105	RES MF 15K 1/4W 2%	24773-301P
R106	RES MF 15K 1/4W 2%	24773-301P
SA	SWITCH	44338-117H
SKA	CON EDGE FEM 30 FXD .1 2S K18	23435-063X
SKB	CON D FEM 15 FXD	23435-494J
SKC	CON PO FEM 2 FXD PCB TYPE 43	23435-100P
TR1	TRANS FET BF244B 30V	28459-011S
TR2	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR3	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR4	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR5	TRANS PNP SIL MPSL08 12V	28431-767E
TR6	TRANS PNP SIL MPSL08 12V	28431-767E
TR7	TRANS PNP SIL MPSL08 12V	28431-767E
TR8	TRANS PNP SIL MPSL08 12V	28431-767E
TR9	TRANS NPN SIL 2N2369 15V	28452-197H
TR10	TRANS NPN SIL 2N2369 15V	28452-197H

Circuit Ref	Description	Part Number
Unit A3	INPUT AND ALIGNMENT BOARD	(Contd.)
TR11	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR12	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR13	TRANS NPN SIL 2N2369 15V	28452-197H
TR14	TRANS NPN SIL 2N2369 15V	28452-197H
TR15	TRANS NPN SIL 2N2369 15V	28452-197H
TR16	TRANS NPN SIL 2N2369 15V	28452-197H
TR17	TRANS PNP SIL MPSL08 12V	28431-767E
TR18	TRANS PNP SIL MPSL08 12V	28431-767E
TR19	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR20	TRANS PNP SIL MPSL08 12V	28431-767E
TR21	TRANS PNP SIL MPSL08 12V	28431-767E
TR22	TRANS NPN SIL 2N2369 15V	28452-197H
TR23	TRANS NPN SIL 2N2369 15V	28452-197H
TR24	TRANS NPN SIL 2N2369 15V	28452-197H
TR25	TRANS NPN SIL 2N2369 15V	28452-197H
TR26	TRANS NPN SIL 2N2369 15V	28452-197H
TR27	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR28	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR29	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR30	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR31	TRANS NPN SIL ZTX109CL 20V	28452-771P
TR32	TRANS PNP SIL 2N2905A 40V	28435-868C
TR33	TRANS NPN SIL ZTX109CL 20V	28452-771P
T1	TRANSFORMER	43590-113F
T2	TRANSFORMER	43590-109J
Unit AR1	RS-232-C BOARD	
11. When ordering, prefix circuit reference with AR1.		
	Complete unit	44829-142P
FLA		43130-237D
PLA	CON D-MALE 25 FXD PCB STRT	23435-546C
SA	SW SLIDE 7NO 25V DIL	23467-311R

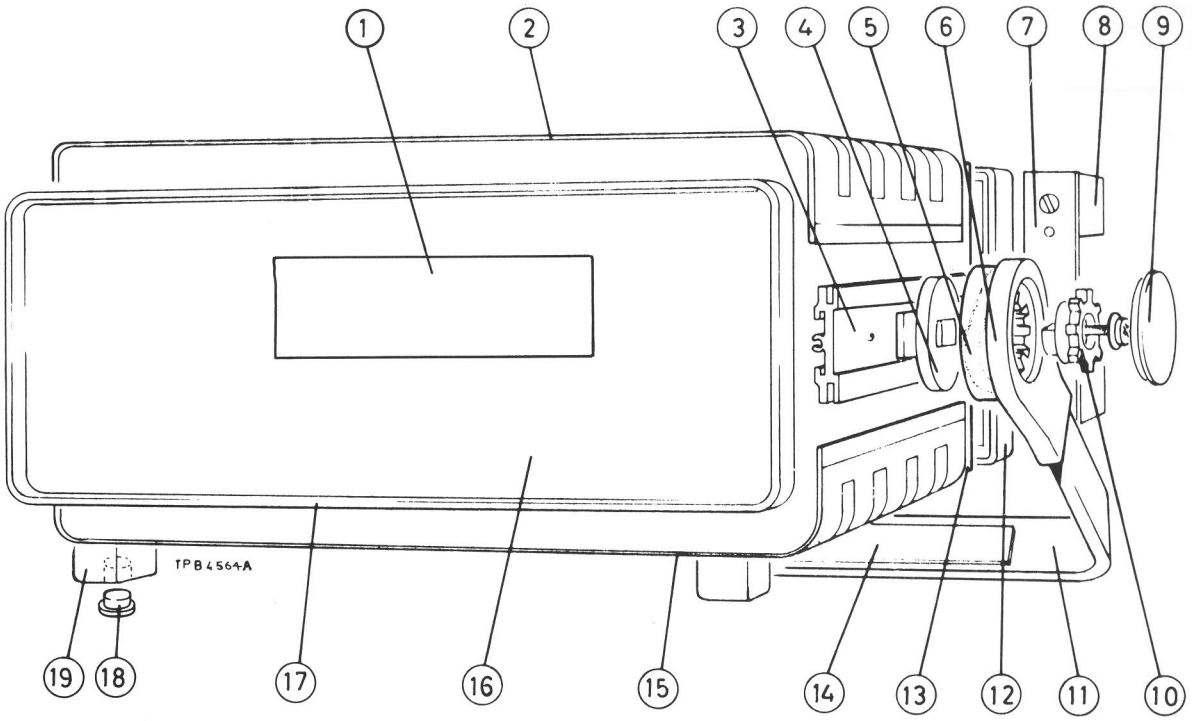


Fig. 1 2833 Mechanical parts

Item No.	*Description*	*Part No.*
MECHANICAL PARTS (see Fig. 1)		
12.	Order without prefix.	
1	Window	37490-559G
2	Top cover,	35904-009F
3	Side rail, (1 of 2)	34900- 949U
4	Flange (1 of 2)	37590-221X
5	Spring washer (1 of 2)	31119-045W
6	Arm (1 of 2)	37590-222M
7	Rear plate fixing	35902-219T
8	Rear foot	37590-225B
9	Cap (1 of 2)	37590-219M
10	Boss (1 of 2)	37590-220P
11	Handle	35904-912D
12	Rear frame casting	35890-083B
	Strip, r.f. seal (1 of 2)	35902-969W
13	Rear panel assembly	35905-422M

Item No.	Description	Part No.
14	Handle moulding (1 of 2)	37590-226K
15	Bottom cover	35904-010L
16	Front panel assembly	35904-917c
17	Front frame casting	35890-083B
18	Stud (1 of 4)	37590-223C
19	Foot (1 of 4)	37590-224R

SEMICONDUCTOR EQUIVALENTS

13. The following semiconductors are listed in numeric-alphabetical order of their product codes. Not all of the product code numbers under the heading "Type used" include manufacturers prefix codes. Where applicable, prefixes have been included in order to conform with those numbers quoted in the electrical parts list.

Type used	Code number	Equivalents (or Suppliers)
14. Diodes		
1N4004	28357-028K	RC 6233:2A22.
1N4148	28336-676J	RC 6233 : 1A44,1A45,1A95. BS 9300 : C0756.
1N5390	28349-005Z	Supplier : Fairchild, Semiconductor devices.
1N5401	28355-723N	Supplier : Westinghouse, ITT.
LEDs		
2300	28624-123E	Supplier : Hewlett Packard.
HLMP0301	28624-118Z	Supplier : Hewlett Packard.
Numeric displays		
7613	28624-220B	Supplier : Hewlett Packard.
7653	28624-221K	Supplier : Hewlett Packard.
15. Integrated circuits		
4001 !	28466-207Z	RC 6233 : 3J14,3J15,3J87,3J167,3J181. BS 9490 : F2511 to F2514,F2518 to F2520.
4013 !	28462-608A	RC 6233 : 3J7,3J8,3J9,3J92,3J164,3J170,3J184, 3J194. BS 9490 : F0027,F0028,F1353 to F1357.
4014 !	28467-520S	BS 9490 : F0067,F0068,F1365 to F1369.
40175 !	28462-617N	Supplier : Fairchild, Mullard.
4051 !	28469-708K	RC 6233 : 3J110,3J203.
4070 !	28466-402T	RC 6233 : 3J119,3J146. BS 9490 : F0337,F0338,F1726 to F1730.
4071 !	28466-403P	RC 6233 : 3J120,3J137,3J247,3J251. BS 9490 : F0018,F1741,F1742,F2623 to F2626. F2630 to F2632.

Type used	*Code number*	*Equivalents (or Suppliers)*
4072 !	28466-106H	Supplier : RCA, Motorola, National, SGS, Fairchild, Texas, Mullard.
4075 !	28466-107E	Supplier : RCA, Motorola, SGS, National, Fairchild, Texas, Mullard.
4081 !	28466-009L	RC 6233 : 3J147,3J237,3J242. BS 9490 : F0019,F1827,F1828,F2637 to F2640, F2644 to F2646.
4511 !	28465-014K	RC 6233 : 3J125, 3J142, 3J148, 3J233, 3J234.
4553 !	28464-131B	Supplier : Motorola.
7218 !	28467-009X	Supplier : Intersil.
74LS00	28466-345H	RC 6233 : 3G1,3G2,3G3. BS 9401 : F0695 to F0698.
74LS02	28466-214Y	RC 6233 : 3G7,3G8,3G9. BS 9401 : F0721 to F0724.
74LS08	28466-012L	RC 6233 : 3G13,3G14. BS 9401 : F0734 to F0737.
74LS10	28466-351Y	RC 6233 : 3G15,3G16,3G17. BS 9401 : F0747 to F0750.
74LS123	28468-309B	RC 6233 : 3G65,3G88. BS 9440 : F0388 to F0391.
74LS138	28465-027F	RC 6233 : 3G105,3G108. BS 9405 : F0499 to F0502.
74LS151	28469-715E	RC 6233 : 3G61,3G79.
74LS153	28469-711K	BS 9405 : F0538 to F0541.
74LS164	28467-515G	RC 6233 : 3G66. BS 9440 : F0401 to F0404.
74LS273	28462-615U	Supplier : Texas, Signetics, Fairchild, Motorola.
74LS32	28466-108U	BS 9401 : F0825 to F0828.
74LS374	28462-618L	Supplier : Texas, Signetics, Fairchild, Motorola, AMD, National.
74LS390	28464-127R	BS 9442 : F0952 to F0955.
74LS74	28462-611A	RC 6233 : 3G39 to 3G41. BS 9420 : F0332 to F0335.
74LS76	28462-019R	BS 9420 : F0345 to F0348.
8155 !	28469-304E	Supplier : Intel, Siemens, Advanced micro devices.
8255A !	28467-002G	Supplier : Intel.
CA3046	28461-901A	Supplier : RCA.
LM324N	28461-322U	RC 6233 : 3H78,3H104,3H122.
MC7805CT	28461-707G	BS 9300 : C0805.
P8085A !	28469-396K	Supplier : Intel, Advanced micro devices, Toshiba.
ZNA2H086J	28469-407U	Supplier : Marconi Instruments only.
ZNA5H016J	28469-408Y	Supplier : Marconi Instruments only.
µA733PC	28461-910N	RC 6233 : 3H82.

Type used	*Code number*	*Equivalents (or Suppliers)*
µA741CN	28461-304T	RC 6233 : 3H24,3H70. BS 9460 : F0073 to F0076,F0079,F0279 to F0288.

16. Transistors

2N2369/BSX20	28452-197H	RC 6233 : 2A122 to 2A126. CECC50004 : -023. BS 9300 : C0555.
2N2905	28434-879X	RC 6233 : 2A135 to 2A141,2A330. BS 9300 : C0670,C0672. CECC50002 : -102.
BC244B	28459-011S	Supplier : Texas.
BC308	28433-455R	CECC50002 : -026.
MPSL08/2N4258	28431-767E	Supplier : Motorola, Fairchild.
ZTX109CL	28452-771P	Supplier : ITT-BC173. SGS-BC209C,BC509C. Fairchild-BC209C.

Chapter 7

CIRCUIT DIAGRAMS

CONTENTS

CIRCUIT NOTES

1. The complete electrical construction of the instrument is illustrated by circuit and composite layout diagrams of the individual printed boards and by a wiring diagram of the chassis showing the general interconnections.

2. Electrical connections between the two main printed circuit boards AA12 and A3 are made via an interconnecting board locating at either end into an edge connector designated SKA on each board respectively. Pin connections on AA12 are identified by a code consisting of a letter, either A or B followed by a number e.g. B5 or A20, the destination of which is identified on A3 board by an identical code e.g. B5 or A20.

Component values

3. The letter in the component value code replaces the decimal point and indicates the multiplier and unit as follows:-

Resistors : Code letter R = ohms, k = kilohms (10^3), M = megohms (10^6).

Capacitors : Code letter m = millifarads (10^{-3}), µ = microfarads (10^{-6}), n = nanofarads (10^{-9}), p = picofarads (10^{-12}).

Inductors : Code letter H = henrys, m = millihenrys (10^{-3}) µ = microhenrys (10^{-6}), n = nanohenrys (10^{-9}).

* SIC : Value selected during test, nominal value shown.

4. Components are marked normally with two, three or four figures according to the accuracy limit ±10%, ±1% or ±0.1%. Because a value 4m7 could be interpreted as 4.7 milliohms, millifarads or millihenrys, each value on circuit diagrams is placed near to its related symbol.

Symbols

5. Circuit diagram symbols are generally in accordance with BS 3939.

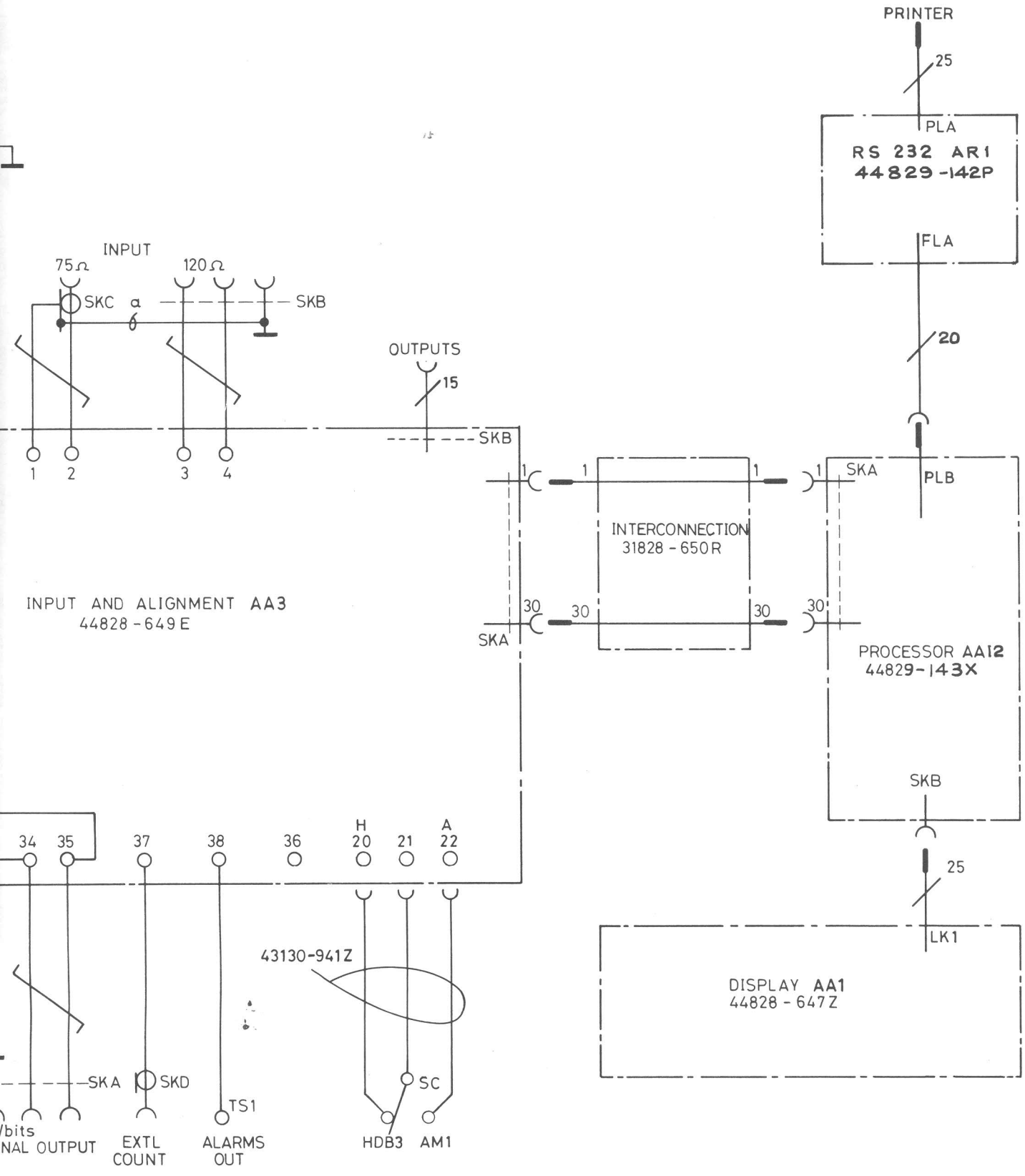
denotes static sensitive device - see page (iv), notes and cautions.

Signal titles

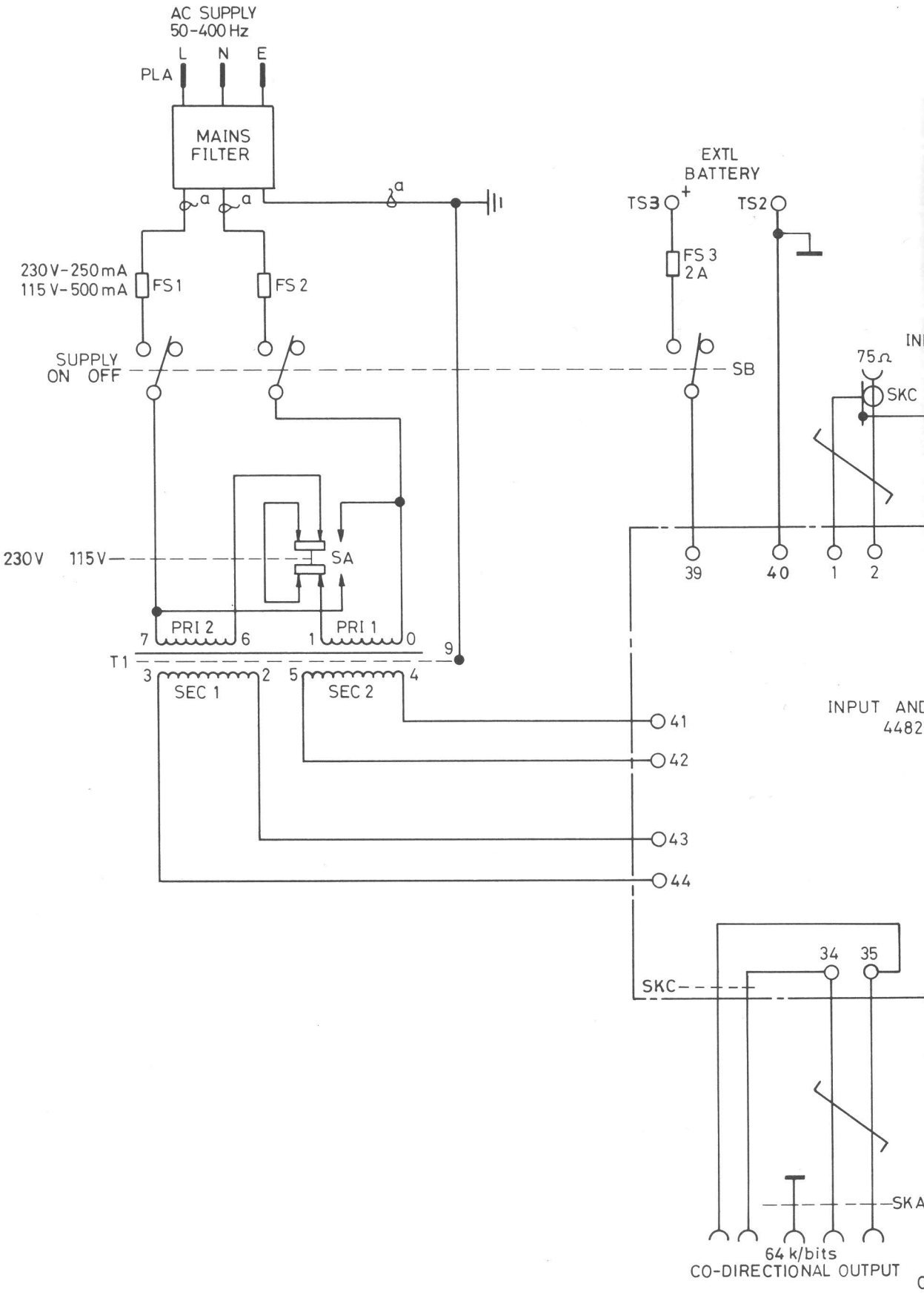
6. Low asserted logic signal names use the suffix L instead of the overline convention e.g. ERRORS is written ERRORS L. The absence of a suffix implies a high-asserted signal.

NOTES.

1. WIRE TO BE 7/0,20 PVC INS UNLESS STATED. ♂ 24/0,20 PVC INS.

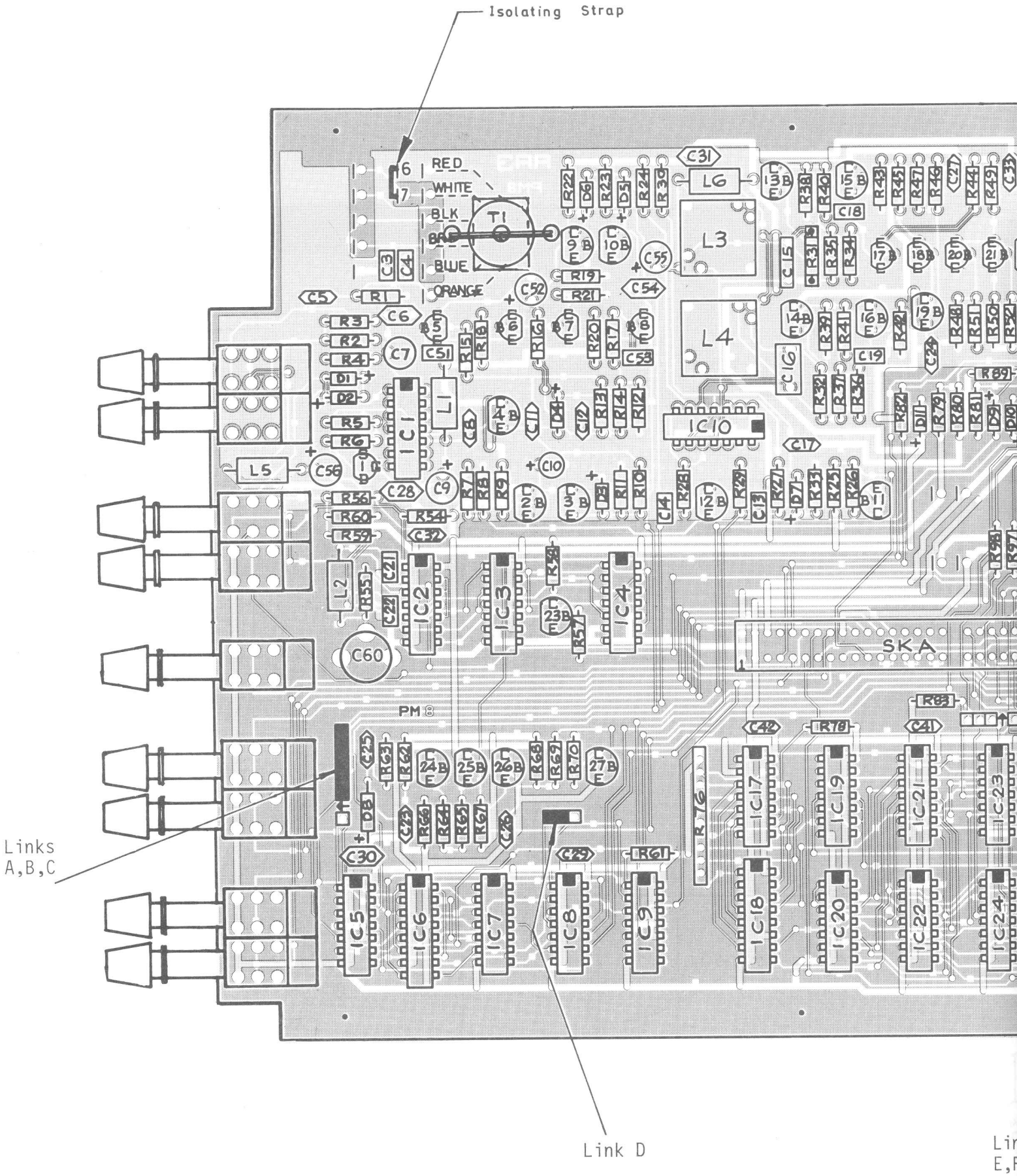


Interconnection diagram

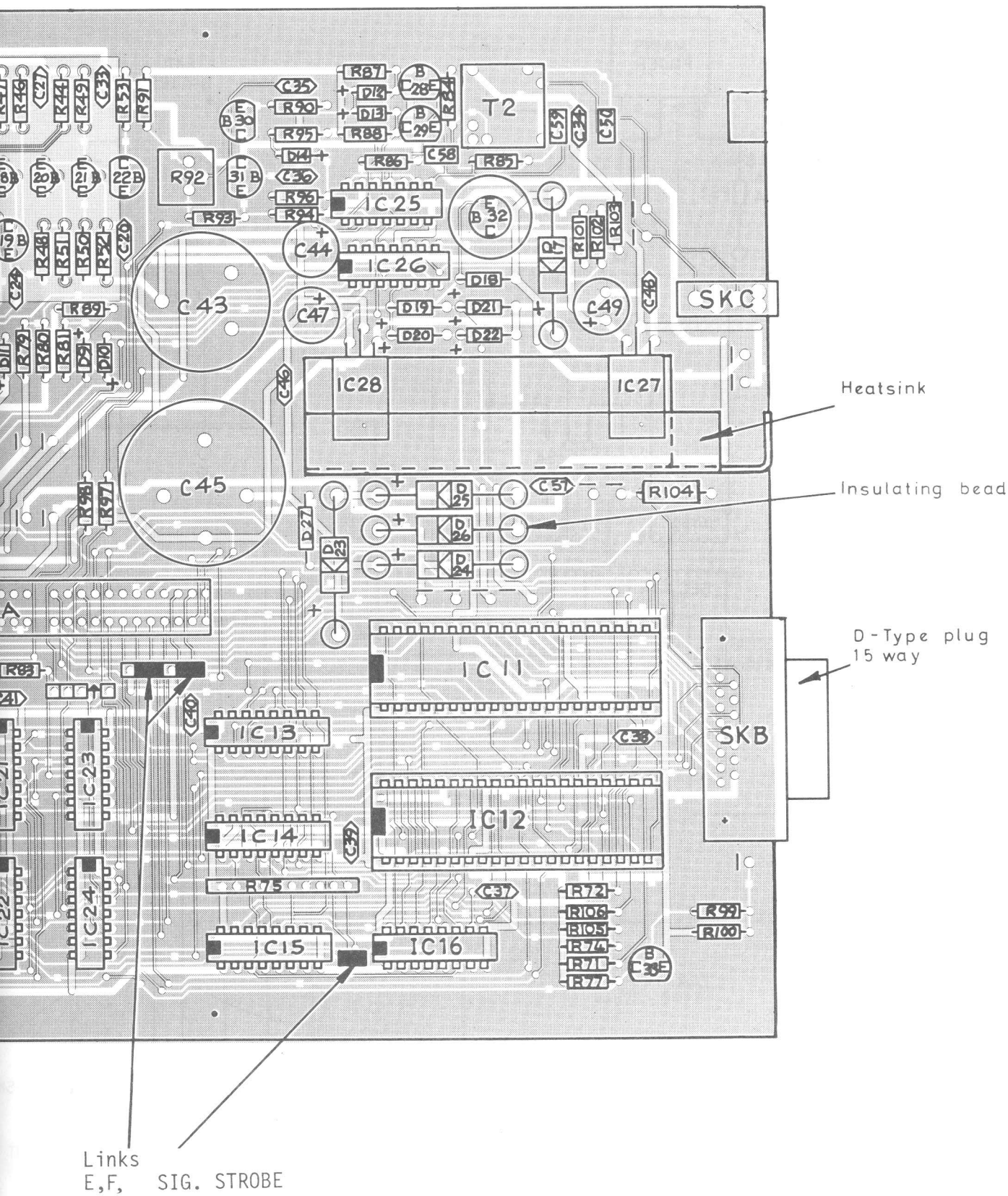


Drg. No. SZ 52833-910Z Sht. 1 of 1, Issue 3

Fig. 1



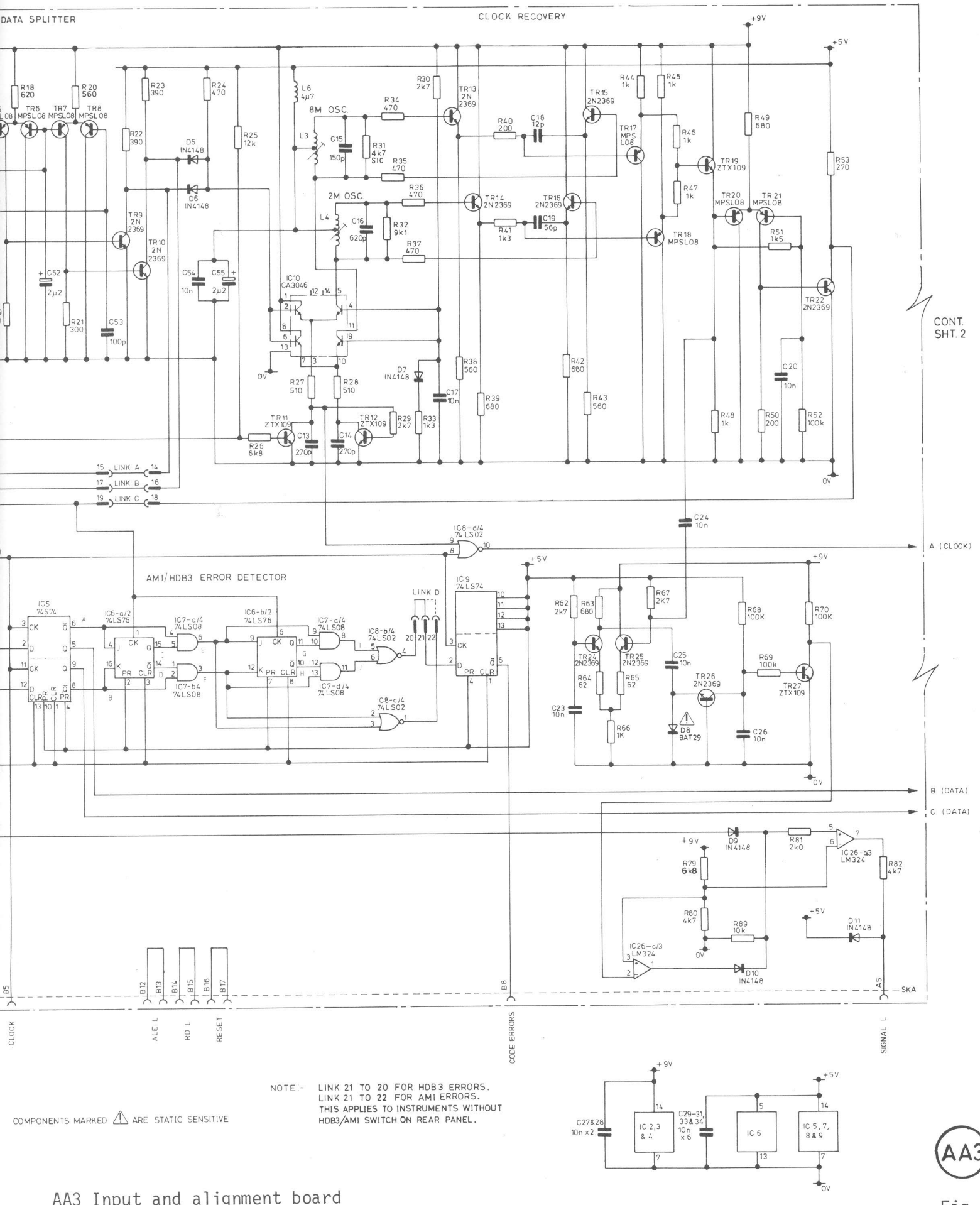
PCB layout, AA3 (viewed



A3 (viewed from component side)

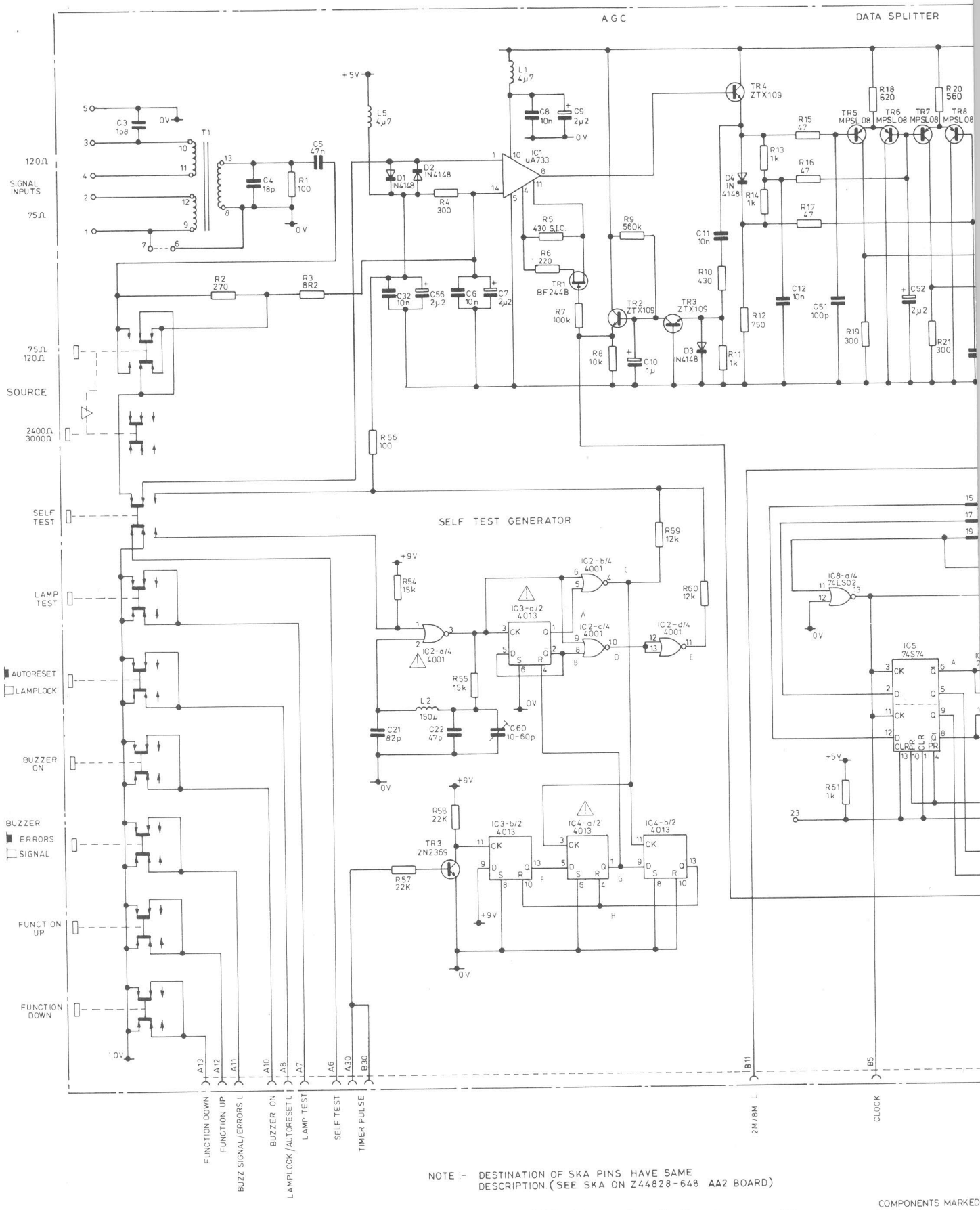
Fig. 2a

Dec. 84



AA3

AA3 Input and alignment board



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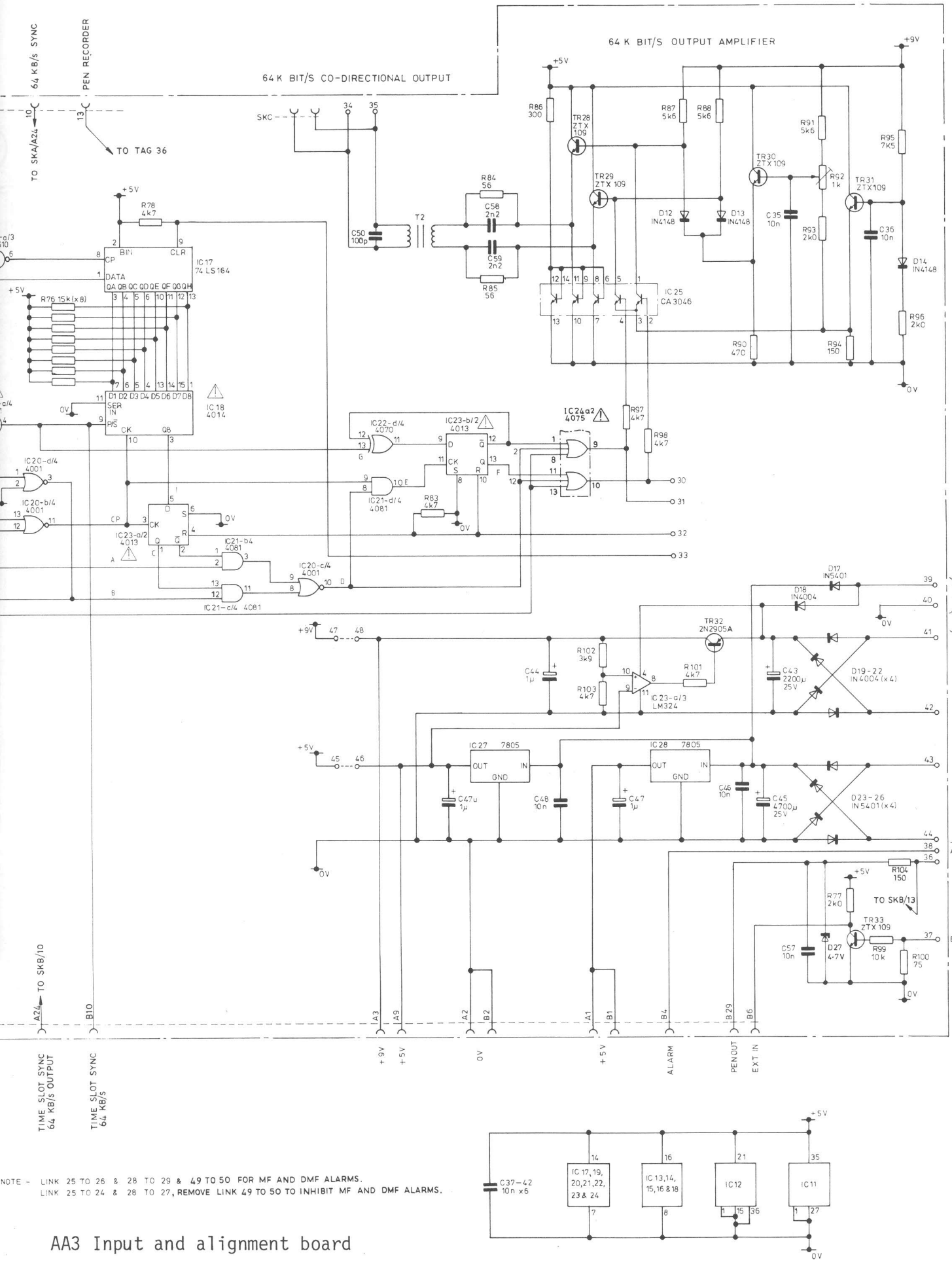
AA3 Is

Fig. 2

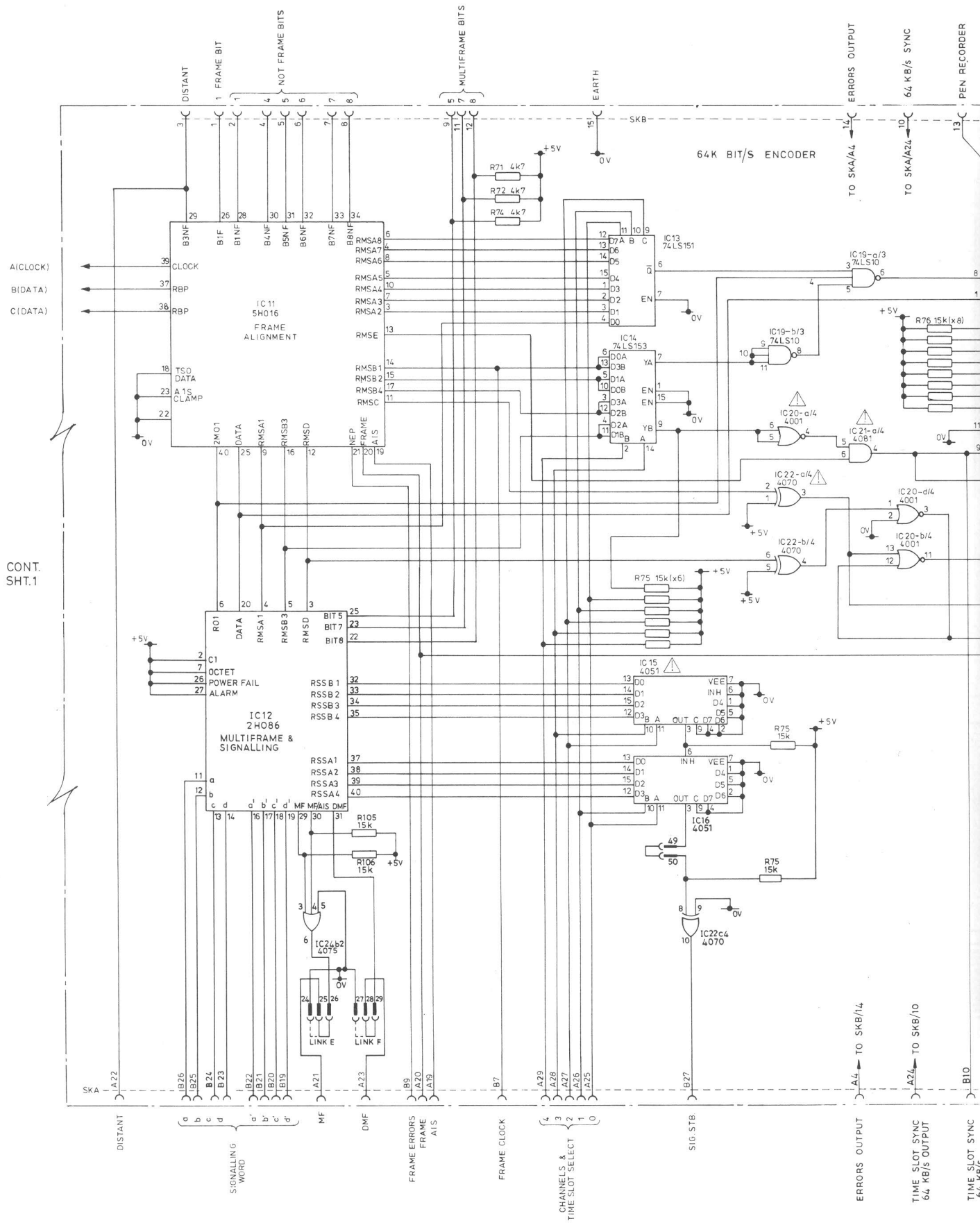
July 86 (Am. 2)



NOTE - LINK 25 TO 26 & 28 TO 29 & 49 TO 50 FOR MF AND DMF ALARMS.
LINK 25 TO 24 & 28 TO 27, REMOVE LINK 49 TO 50 TO INHIBIT MF AND DMF ALARMS.

AA3 Input and alignment board

AA3



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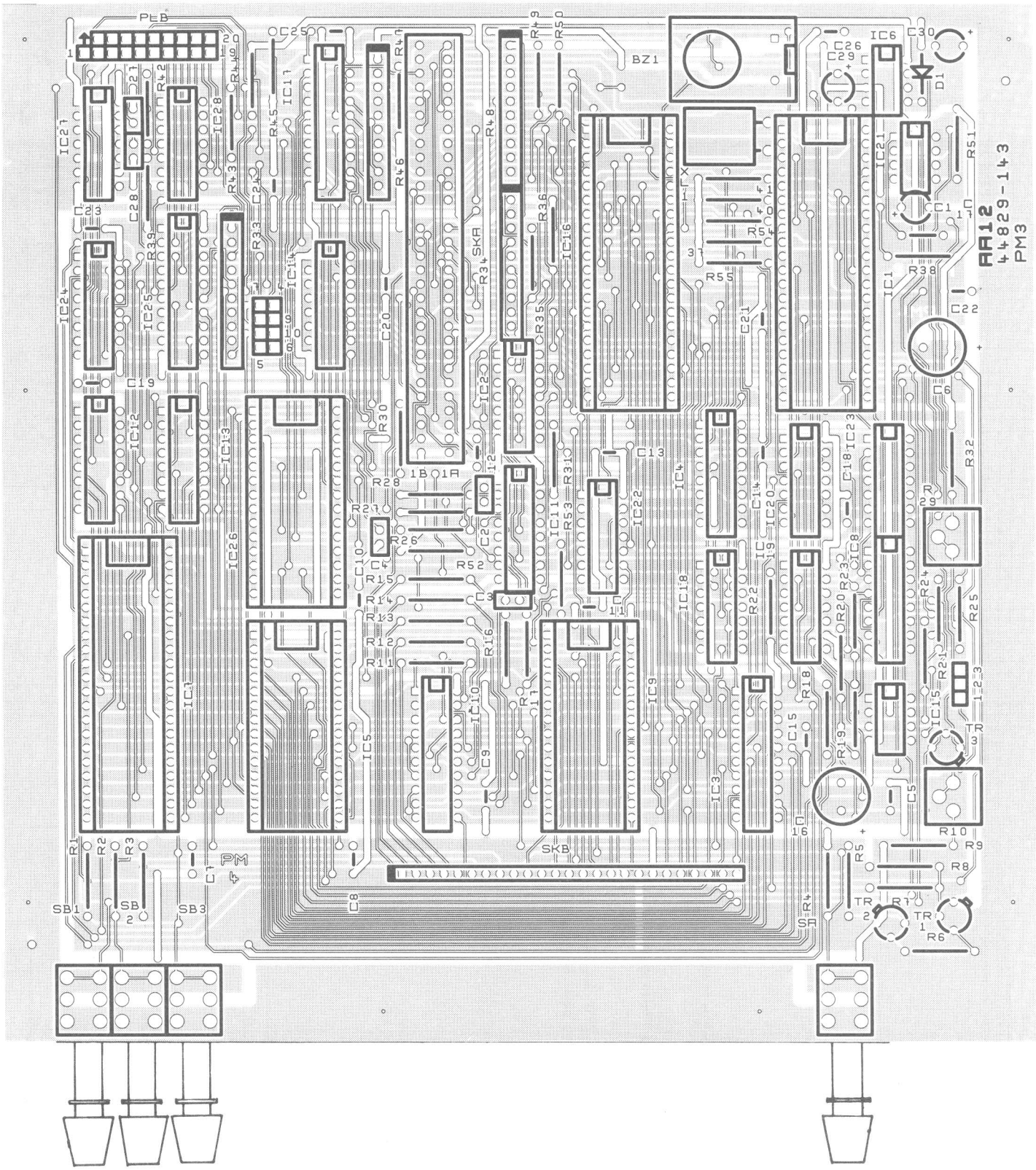
NOTE - LINK 25 TO 26
LINK 25 TO 24

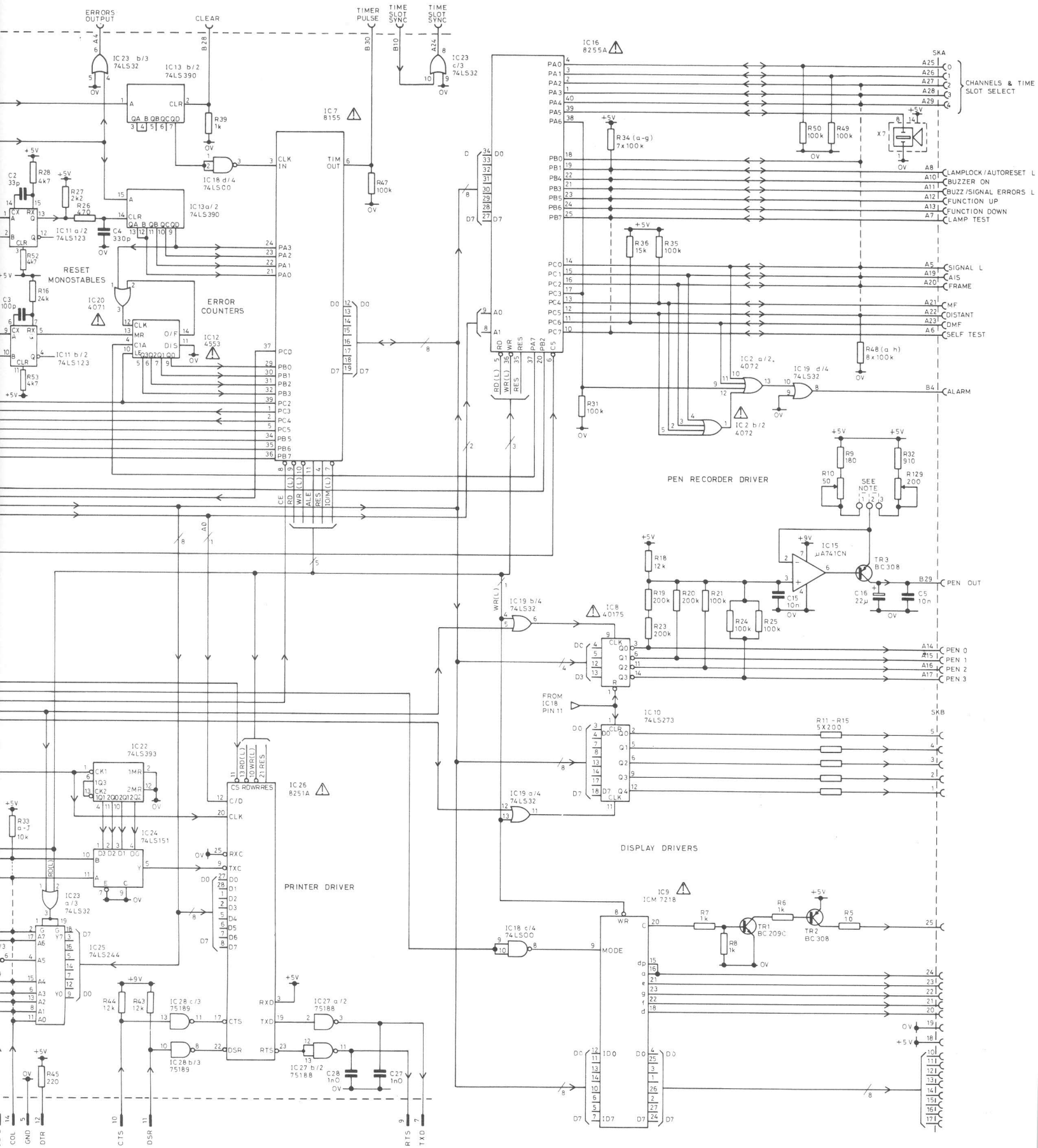
AA3 I

Fig. 3

July 86 (Am. 2)

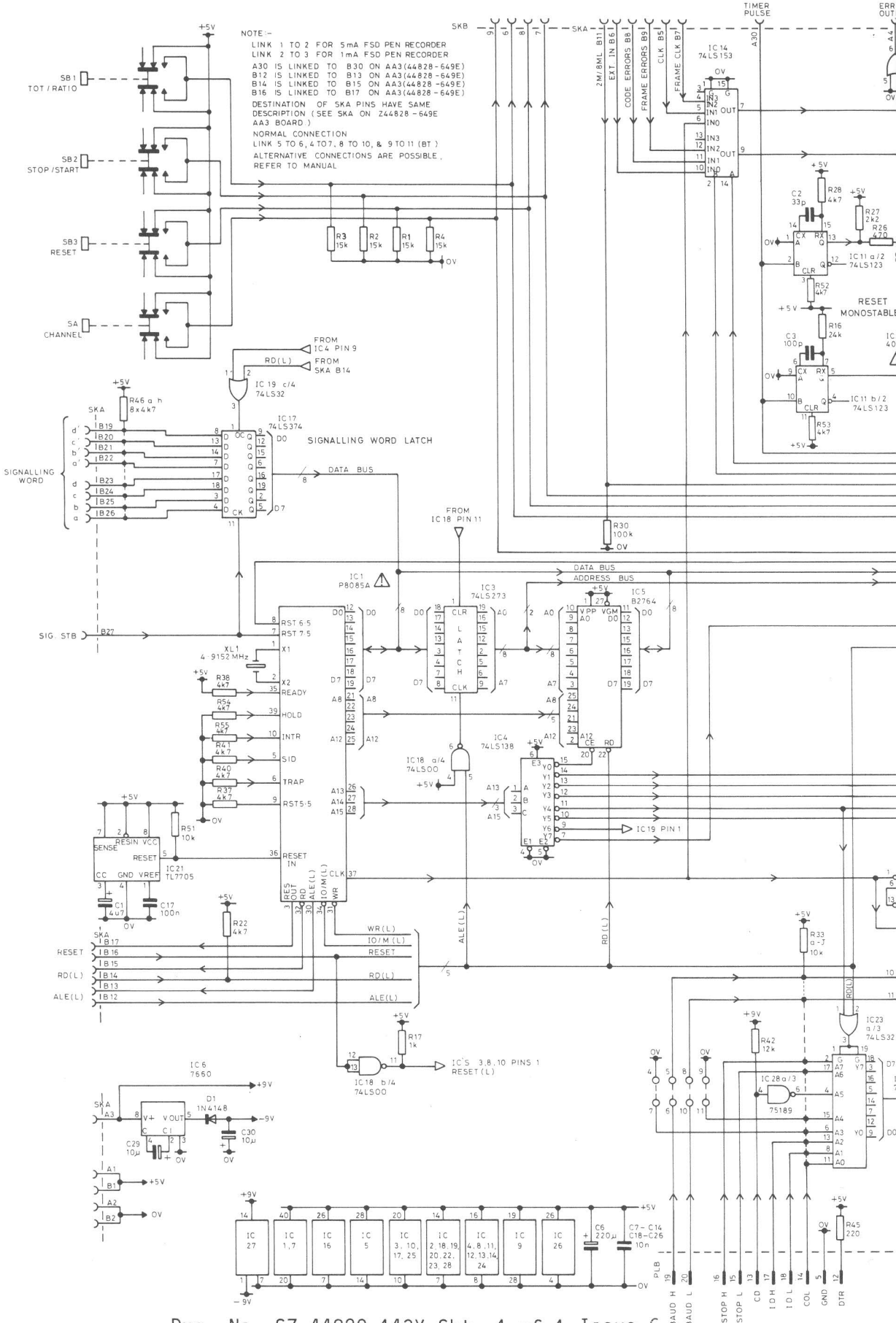


PCB layout, AA12 (viewed from component side)



AA12 Processor board

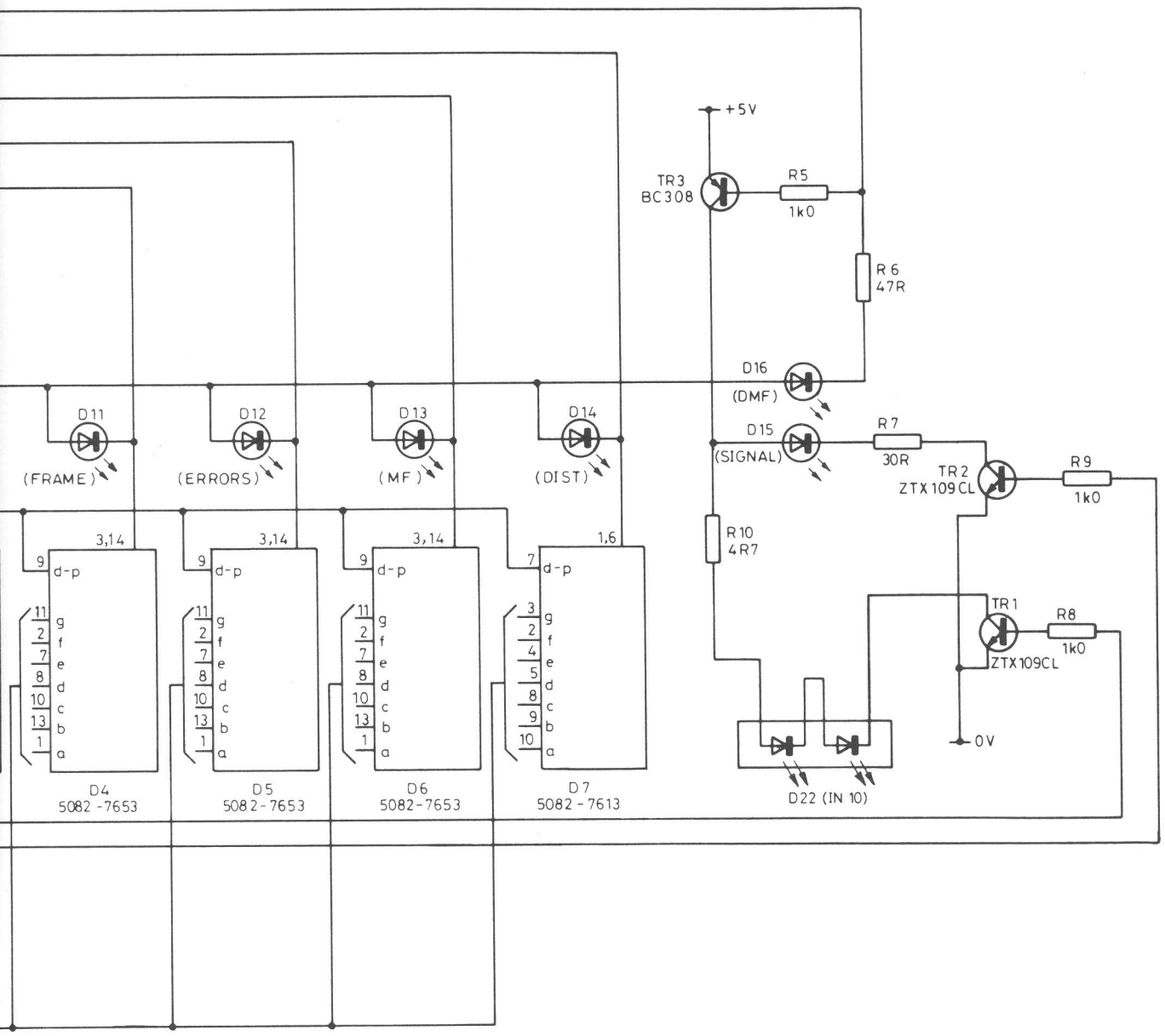
AA12



Drg. No. SZ 44829-143X Sht. 1 of 1, Issue 6

Fig. 4

Nov. 87 (Am. 3)



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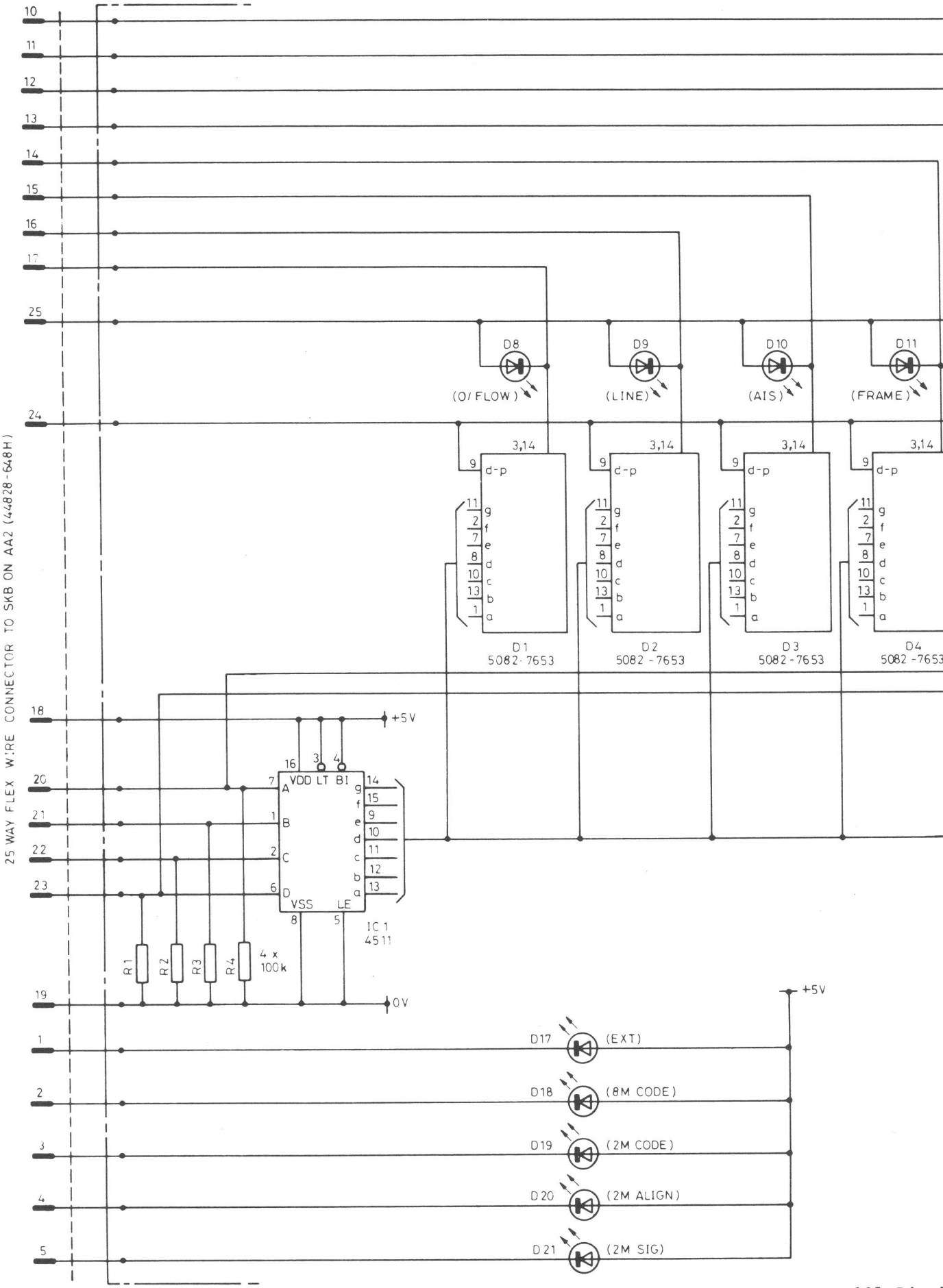
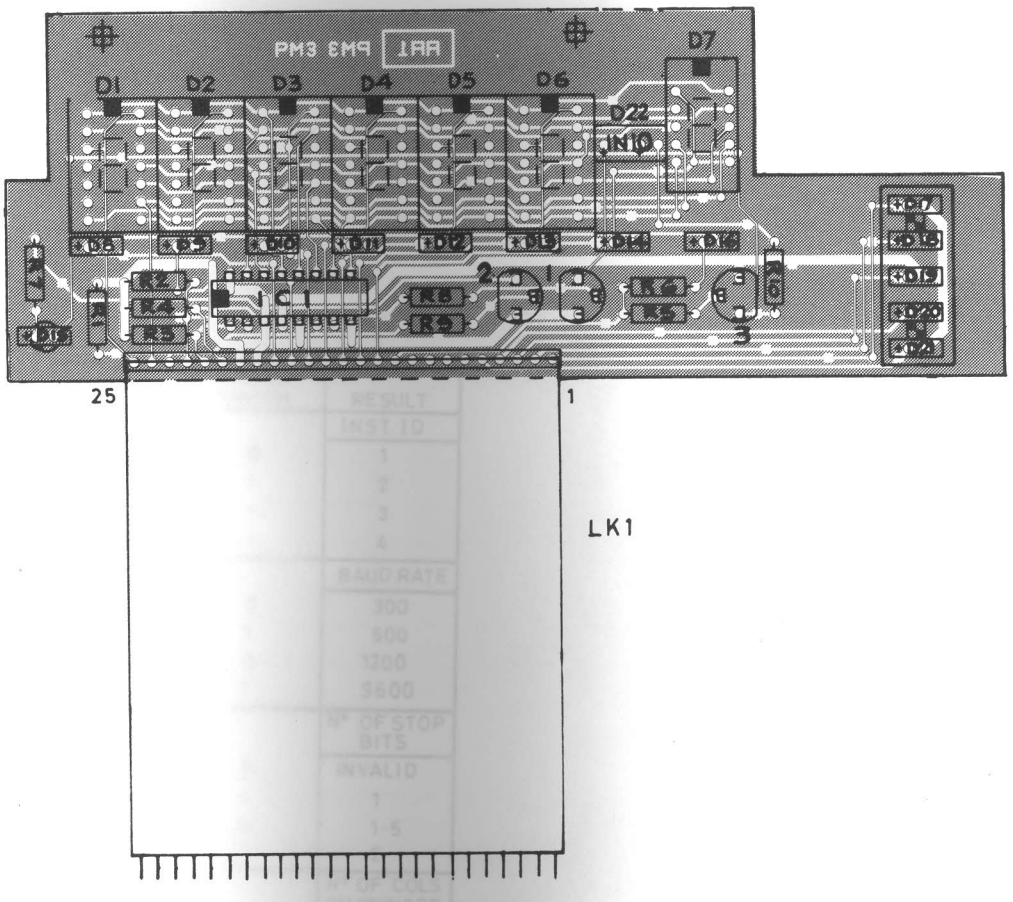
AA1

AA1 Display board


25 WAY FLEX WIRE CONNECTOR TO SKB ON AA2 (44828-648H)
10
11
12
13
14
15
16
17
25
24
18
20
21
22
23
19
1
2
3
4
5
D8
(O/FLOW)
D9
(LINE)
D10
(AIS)
D11
(FRAME)
3,14
d-p
g
f
e
d
c
b
a
D1
5082-7653
D2
5082-7653
D3
5082-7653
D4
5082-7653
+5V
VDD LT BI
VSS LE
IC 1
4511
R1
R2
R3
R4
4 x
100k
0V
D17
(EXT)
D18
(8M CODE)
D19
(2M CODE)
D20
(2M ALIGN)
D21
(2M SIG)

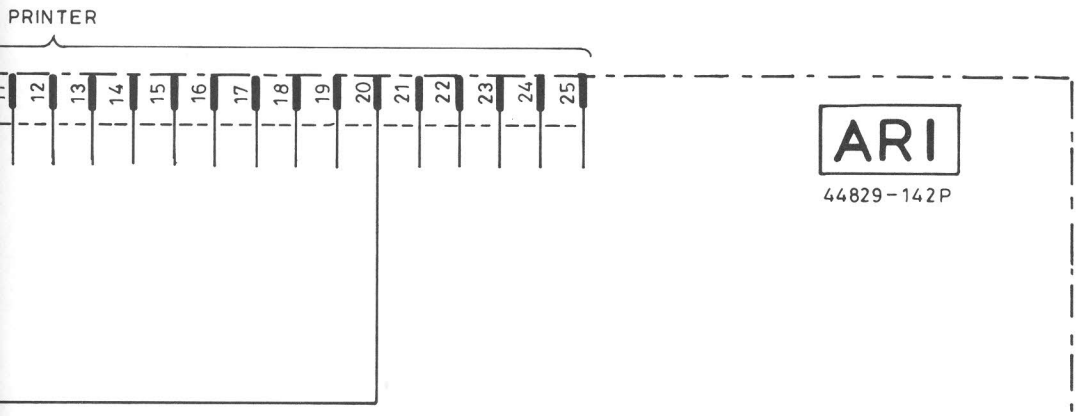
AA1 Displ



PCB layout, AA1 (viewed from component side)

Fig. 5

Dec. 84



VED
PANEL

IDENTITY

BAUD RATE

STOP BITS

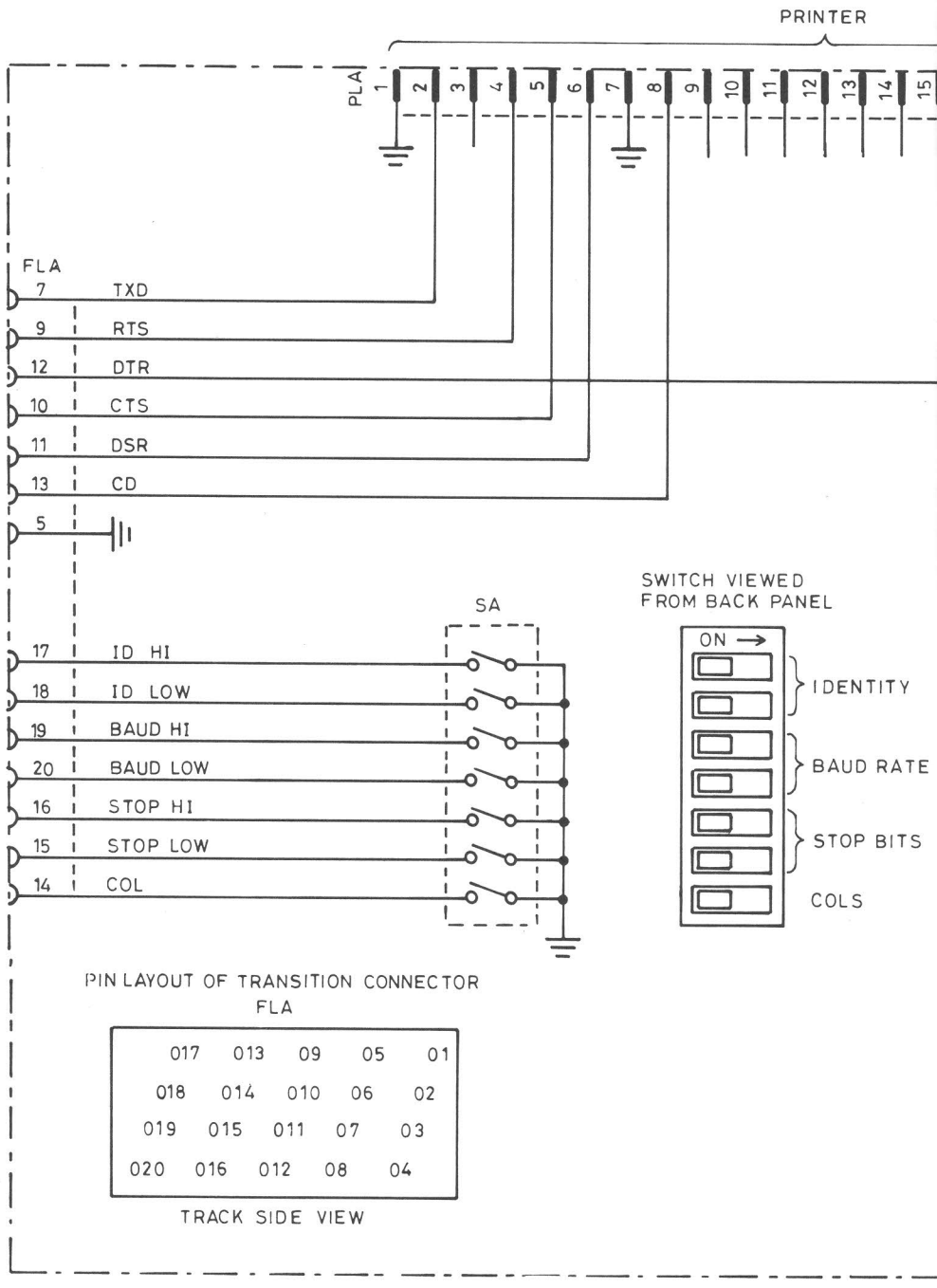
COLS

TOP SWITCH	BOTTOM SWITCH	RESULT
		INST. ID
0	0	1
0	1	2
1	0	3
1	1	4
		BAUD RATE
0	0	300
0	1	600
1	0	1200
1	1	9600
		N° OF STOP BITS
0	0	INVALID
0	1	1
1	0	1·5
1	1	2
		N° OF COLS ON PRINTER
0	–	24
1	–	40

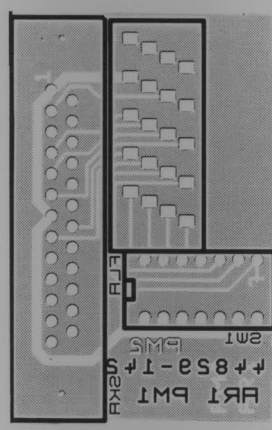
NOTE :- 1 = SWITCH OPEN OR OFF (PRODUCES LOGIC 1)
0 = SWITCH CLOSED OR ON (PRODUCES LOGIC 0)

AR1

AR1 Connector board



Drg. No. SZ 44829-142P Sht. 1 of 1, Issue 1



PCB layout, AR1 (viewed from component side)

Fig. 6a
Dec. 84

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