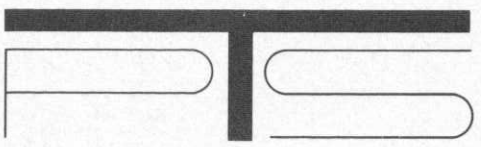
GPIB INTERFACE SEC 1022 SER 1023 SECTION



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INTRODUCTION

The GPIB interface implements a standardized form of serial remote control and provides the necessary hardware to connect an instrument to the GPIB, also referred to as the 488-bus.

Functional Purpose

The GPIB interface allows remote programming of the synthesizer via the GPIB (General Purpose Interface Bus) in accordance with the IEEE Std 488-1978.

The following subset describes the specific capabilities.

SH0	Source handshake	None
AH1	Acceptor handshake	Complete
T0	Talk	None
L1	Listen	Basic listener; Listen Only
SR0	Service request	None
RL2	Remote/Local	No local lockout
PP0	Parallel poll	None
DC0	Device clear	None
DT0	Device trigger	None
C0	Controller	None
E1	Driver type	Open collector drivers

Three basic functions are accessible through appropriate commands: frequency, output level and Local/Remote mode. In the "LISTEN ONLY" mode **all** valid commands are accepted without regard to the device address, but in the "ADDR'D" mode only commands preceded by the selectable "LISTEN" address.

Physical Aspects

Two piggy-backed and interconnected boards the SEC 1022 and the SER 1023 make up an interface unit.

They are mechanically attached to the rear panel by 4 screws: the SEC facing to the rear with the standard bus connector, a switch for address and listen mode, a "LISTEN" LED, and a second connector intended for an external attenuator or another BCD controlled device.

Internally all ("parallel") connections are made through a single-row header/plug arrangement located on the SER board. These are compatible with the pinout of the PE 1021 (parallel interface) board.

The physical interconnection to the GPIB through the 23 pin rear panel connector has the standard pinout:

PIN	SIGNAL	FUNCTION	
1	DIO1	Bit 1	data bus
2	DIO2	Bit 2	data bus
3	DIO3	Bit 3	data bus
4	DIO4	Bit 4	data bus
5	EOI	End or Identify	management bus —inactive—
6	DAV	Data Valid	byte transfer bus (handshake)
7	NRFD	Not Ready for Data	byte transfer bus (handshake)
8	NDAC	Not Data Accepted	byte transfer bus (handshake)
9	IFC	Interface Clear	management bus
10	SRQ	Service Request	management bus —inactive—
11	ATN	Attention	management bus
12	Shield	Shield	
13	DIO5	Bit 5	data bus
14	DIO6	Bit 6	data bus
15	DIO7	Bit 7	data bus
16	DIO8	Bit 8	data bus —inactive—
17	REN	Remote Enable	management bus
18	GND(6)	Ground return for DAV	
19	GND(7)	Ground return for NRFD	
20	GND(8)	Ground return for NDAC	
21	GND(9)	Ground return for IFC	
22	GND(10)	Ground return for SRQ	
23	GND(11)	Ground return for ATN	
24	GND,LOGIC	Logical ground	

OPERATION

Basically two modes of operation are implemented and are initially selected in the setup procedure:

(a) An "addressed" mode where only "addressed commands" (AC-class) and "device dependant commands" (DD-class) are being executed.

(b) A "LISTEN ONLY" mode where any valid command is carried out non-selectively.

Actual command details depend upon the type of controller which is expected to send the appropriate serial characters and control signals. In any case however, the command string or message consists of a number of serial bytes (characters) with the same general pattern:

[Address] if any
[Code letter for desired function]
[NUMERICAL VALUE, possibly up to 10 digits long]
[Terminator]

The programming section shows examples for two different makes of controller/computers.

Setup

Connect bus cable.

Set rear panel switch "S6" to desired mode: LISTEN ONLY or "ADDR'D".

If the addressed mode of operation is selected, check and set if necessary the 5 bit address switch to the chosen one of 31 numbers.

To set a desired address from 0 to 30 follow this table:

ADDRESS	Equivalent	7bit	ASCII	Switch Settings				
(5bits)	character	dec.	codes	A5	A4	A3	A2	A1
0	SP	32		0	0	0	0	0
1	!	33		0	0	0	0	1
2	"	34		0	0	0	1	0
3	#	35		0	0	0	1	1
4	$	36		0	0	1	0	0
5	%	37		0	0	1	0	1
6	&	38		0	0	1	1	0
7	'	39		0	0	1	1	1
8	(	40		0	1	0	0	0
9	)	41		0	1	0	0	1
10	*	42		0	1	0	1	0
11	+	43		0	1	0	1	1
12	,	44		0	1	1	0	0
13	-	45		0	1	1	0	1
14	.	46		0	1	1	1	0
15	/	47		0	1	1	1	1
16	0	48		1	0	0	0	0
17	1	49		1	0	0	0	1
18	2	50		1	0	0	1	0
19	3	51		1	0	0	1	1
20	4	52		1	0	1	0	0
21	5	53		1	0	1	0	1
22	6	54		1	0	1	1	0
23	7	55		1	0	1	1	1
24	8	56		1	1	0	0	0
25	9	57		1	1	0	0	1
26	:	58		1	1	0	1	0
27	;	59		1	1	0	1	1
28	<	60		1	1	1	0	0
29	=	61		1	1	1	0	1
30	>	62		1	1	1	1	0

Note that 31 is reserved for the "UNLISTEN" command, and cannot be used as a valid Listen address.

Programmable Instrument Functions

The GPIB interface will respond to the following "ADDRESS" (AD) and "ADDRESSED COMMANDS" (AC) which are sent in the command mode with ATN true:

			ASCII		
Mnemonic	Command	Class	char.	dec.code	Resulting action
MLA	My Listen Address	AD	SP to >	32 to 62	Device listens and goes remote on 1st numeric character
UNL	Unlisten	AD	?	63	Device unlistens, but stays in remote.
GTL	Go to local	AC	SOH	1	Returns to local, if in remote. No action if in local.

The following device dependent functions can be controlled by the "DD" type commands with ATN false when in the "LISTEN" state:

FUNCTION	ASCII coded command string (characters)	Notes
(1) Frequency, all 10 digits	F, 10 numerals, LF	1st numeral = MSD
(2) Frequency, N least significant digits	F,N numerals, LF	1st numeral = MSD
(3) Output level only in -dbV, 9 db range in 1 db steps	A, one numeral, LF	numeral = x 1 db
(4) Output level with optional attenuator in -dbV in 1dB steps, range 00 to 99	A, two numerals, LF	1st numeral = x 10 db 2nd numeral = x 1 db
(5) Return to local mode	GTL (SOH)	
(6) Transfer data to output registers	LF	SEE NOTE BELOW

The last character in a command string (LF) affects internal transfer of the stored data word. It is usually appended automatically by the controller.

Note that the additional ASCII characters used in the command strings have these code values:

Character	Dec. code	Character	Dec. code
GTL	1	0	48
LF	10	1	49
A	65	2	50
F	70	3	51
		4	52
		5	53
		6	54
		7	55
		8	56
		9	57

Programming Examples

Keep in mind that the basic data transfer on the bus is bit parallel byte serial, one byte at a time. Any program therefore has to generate data words made up of a string of ASCII characters. Each character represents a specific control code. The required characters for a desired function are listed under Programmable instrument functions (page 00). Specific details for using them depend upon the programming language of the particular controller.

However, in any case, when executing a program the controller has to send the following sequence to the instrument:

1st byte:	MLA (ASCII code range 32-62). Not needed for "LISTEN ONLY".
2nd byte:	ASCII character code for desired function (1, 65 or 70)
3rd byte:	ASCII character code for 1st digit of associated numerical value, if any (between 48 and 57)
4th byte:	ASCII character code for 2nd digit, if any
ith byte:	ASCII character code for last digit, if any
(i + 1)th byte:	ASCII code for other function if any
(i + 2)th byte:	ASCII code for 1st digit relating to "other" function if any
nth byte:	ASCII code for last digit, if any
(n + 1)th byte:	ASCII code for LF (10)
optional byte:	ASCII code for UNL (63)

To give a numerical example, assume we want to set the instrument to: 123.4567890 MHz at a level of -3dbV and use address 13.

The command string would be: (expressed in ASCII decimal code.)

Byte 1 : 45	(-)	MLA	with ATN true	= AD type command
Byte 2 : 70	(F)	DAB 1	with ATN false	= DD type command
Byte 3 : 49	(1)	DAB 2	with ATN false	= DD type command
Byte 4 : 50	(2)	DAB 3	with ATN false	= DD type command
Byte 5 : 51	(3)	DAB 4	with ATN false	= DD type command
Byte 6 : 52	(4)	DAB 5	with ATN false	= DD type command
Byte 7 : 53	(5)	DAB 6	with ATN false	= DD type command
Byte 8 : 54	(6)	DAB 7	with ATN false	= DD type command
Byte 9 : 55	(7)	DAB 8	with ATN false	= DD type command
Byte 10 : 56	(8)	DAB 9	with ATN false	= DD type command
Byte 11 : 57	(9)	DAB 10	with ATN false	= DD type command
Byte 12 : 48	(0)	DAB 11	with ATN false	= DD type command
Byte 13 : 65	(A)	DAB 12	with ATN false	= DD type command
Byte 14 : 51	(3)	DAB 13	with ATN false	= DD type command
Byte 15 : 10	(LF)	DAB 14	with ATN false	= DD type command
optional : 63	(?)	UNL	with ATN true	= AD type command

(Commentary notations)

This example implemented in BASIC with a PET controller would require these program lines:

```
10 OPEN 200, 13   or   OPEN 200, 45
20 PRINT #200, "F1234567890A3"
```

A subsequent change in level to 0dbV would be commanded by

```
30 PRINT #200, "A0"
```

A return to local would be affected by

```
40 PRINT #200, CHR$(1)
```

Note that in this example with PET/BASIC language, the PRINT #200 portion generates the MLA byte, also the LF and UNL bytes are automatically appended.

Using an HP model 9825A calculator as controller would require the following program:

```
0 :  wrt713, "F1234567890A3"        (equivalent of line 20)
1 :  wrt713, "A0"                   (equivalent of line 30)
```

It should also be noted that the sequential order of dual function commands is immaterial.

Note:
A frequency command string with less than the full 10 digits will update only the least significant digits.

Example:
Assume previous setting : 125000680.0 Hz
Next command string containing: F1234
The resulting new frequency setting is: 125 000 123.4 Hz

Note: Only the 4 least significant digits were changed.

PRINCIPLES OF OPERATION

In order to follow the later part better, a general understanding of the GPIB concept is more or less assumed. A very brief summary is included here with the intent to help clarify the other part.

Condensed GPIB Concept

It is a standardized form of a serial digital data transfer system. Messages (addresses, addressed commands and data) are being sent over an 8 bit wide bus from a designated "Talker" to one or more "Listeners" supervised by a controller, usually a computer. The controller uses a set of 5 management lines to keep order and to maintain priorities. One of these lines called ATN (attention) determines how data on the bus are to be interpreted. A Low (also TRUE) state signifies commands of various kinds whereas the high state (False) identifies the message bytes as data, typically functions and related values. Any actual transfer of a message byte is also verified through a 3-line handshake procedure, which is to ensure that no new data are being sent until the last and slowest listener has accepted them and is ready for new data. The rate of transfer is both variable and asynchroneous. Theoretically, rates up to 1MHz are possible.

There can be up to 15 devices on one bus, however, address space is provided for up to 31 talkers and listeners.

Bus connections can be either star-like or in tandem, but are limited in total length to 20m.

The physical connector is a 24 contact ribbon connector with metric hardware. Standard cable plugs have a male/female configuration to facilitate through-connections. The logic convention for all bus signals is negative true, i.e.,

a low state = true = Logic 1 (< 0.8V)
a high state = false = Logic 0 (> 2.0V)

In summary there are:

Line	Mnemonic	Origin of signal
8 lines for data byte	DAB	controller, talker
5 management lines:		
Attention	ATN	controller
Interface clear	IFC	controller
End or Identify	EOI	controller, talker
Service request	SRQ	talker, listener
Remote enable	REN	controller
3 handshake lines:		
Data valid	DAV	talker
Not data accepted	NDAC	listener
Not ready for data	NRFD	listener

Execution of a Valid Bus Command

All data transfers from the GPIB involve an "acceptor handshake" operation. The interface will handshake only under two conditions:

1. when ATN is true (low), which is a universal command in anticipation of an "addressed command".

2. when it is in the "LISTEN" state, set by either S6 to position "LISTEN ONLY", or by the listen flipflop U19. (See schematics Fig. 1 and Fig. 2.)

Either of these conditions forces HSE high and gates NRFD and NDAC signals to be sent out in response to an incoming DAV low signal, which indicates the presence of a valid data byte on the D10 lines. DAV triggers a 1 μs strobe pulse STR from U18 which acts as a master clock within the module. If the handshake is enabled, as described before then STR sets NRFD low and NDAC high, subject to a possible delay by the INH signal from U21. Finally, when DAV goes high again indicating the end of valid data, NDAC clears first, then NRFD is released (goes high).

The associated data byte on the DIO lines is processed depending on the state of ATN. When ATN is low (true) incoming data are handled as addresses or addressed commands. If the received byte matches the address register (switches S1 through S5), the comparator U2, U16 set the MLA line high which allows the listen clock pulse LCK to set the listen flipflop U19, which in turn enables subsequent data acceptance.

Once set to listen, and with ATN high (false), incoming bytes are now handled as functional data in various ways through the STR derived data clock DCK. Comparator U11 discriminates against any other characters but numerals 0 through 9 and gates DCK to become the number clock pulse NCK. Also the remote ff U17 is set by NCK and DAV, putting the module in the REMOTE mode. An UNL byte decoded by U5 does the opposite and clears the listen ff without affecting the remote ff. A GTL command (DD or AC-type) will clear the remote ff U17.

NCK is gated once more and turns into the frequency clock FCK following receipt of the ASCII"F" byte, or becomes the A-clock ACK after receiving the "A" character. Only one of these two clocks can be active at a time. The "A" and "F" characters are decoded by U6 and U14 and cause proper gating of the A & F dual ff U8.

Note that ACK or FCK has as many pulses or transitions as the number of numerals following the "A" or "F" character.

The end of a data string is recognized by the LF character. Decoder U10 and DCK generate the transfer pulse TRA, which in turn triggers reset signals ARES and FRES, all being used eventually in the serial to parallel conversion process on the SER board. The previously mentioned INH signal, also triggered by TRA in U21 is timed to ensure a minimum waiting period of 20 μs before another transmission cycle.

A few more signals are derived from REM. One is called OC for output control and affects the tristate output registers. Another, called FPE for front panel enabling, involves U15 and Q1 and generates nominally 5V in the LOCAL mode. Q2 produces similarly 5V in the REMOTE mode, the signal is called REL for remote LED. Also a monitor signal LIL provides a low state in the LISTEN state.

The circuits described so far are all located on the SEC 1022 board (Serial entry control). The serial to parallel conversion takes place on the SER 1023 (serial register) board as follows.

Four bits of the 7bit (ASCII) byte, called SB1, 2, 4, 8 are passed on for conversion. Since only numerals enable the applicable serial clock nothing else can be converted. Numerical data following "F" are clocked into a set of 10 bit shift registers U11, 19, 14, 22, 4 by FCK, those following "A" are clocked into a set of 2 bit shift registers U6, 13 by ACK. The respective clock pulse also generates an enabling signal, FE1 - 10 in the F-channel with U1, 2, 3, and AE1 - 2 in the A-channel with U5. When the output registers, U9, 17, 10, 18, 12, 20, 15, 23, 24 of the F-channel and U7, 21 of the A-channel are thus enabled, the following transfer pulse TRA stores the available data from the shift registers in the output registers, overwriting any previously stored data. Finally the stored data appear at the output lines whenever OC is low, i.e., being in the REMOTE mode. Otherwise, with OC high, the outputs are in a high impedance state, but stored data are not affected.

Responding to the last digit in the A-channel is a D to A converter implemented by the 10 to 1 decoder U8 and a bank of resistors. The resulting analog voltage ANL is tailored to produce 1db incremental changes in the rf output level of the instrument.

Option 1023/160 uses a BCD to BIN converter U16A to convert the 4 digit #9 lines to a hexadecimal format, equivalent to decimal 0 to 15. (0-150MHz)

Option 1023/200 uses another output register U16B to provide one least significant bit of the 10th digit. (100MHz)

Option 1023/500 (1023 Rev. 2) uses a different enlarged shift register U4 and provides additional output lines for handling the '200' and '400' MHz bits through U16B.

The following list in section 2.3 summarizes the key signals and associated functions.

List of Key Signals

Name	Origin board/IC	Quiesc. State	Comments
AB1	SER/U21	x	Bit weight 1 of A lines, for attenuator control
AB2	SER/U21	x	Bit weight 2 of A lines
AB4	SER/U21	x	Bit weight 4 of A lines
AB8	SER/U21	x	Bit weight 8 of A lines
ACK	SEC/U1	L	STR derived clock pulse for A-channel conversion
AE1	SER/U5	H	ACK triggered enabling signal for digit #1 of A-channel, reset by ARES
AE2	SER/U5	H	ACK triggered enabling signal for digit #2 of A-channel
ANL	SER/U8	x	Analog voltage for level control, appr. range 2V
ATN	Bus,SEC/U7	x	Low in "command mode", high in "DD mode"
ARES	SEC/U1	H	TRA triggered reset pulse for A-channel
DAV	Bus,SEC/U7	H	Goes low after talker has valid data on bus
DCK	SEC/U16	L	STR derived pulse, occurs for each byte in DD mode
FCK	SEC/U1	L	NCK derived pulse, enabled after "F" byte
FE1-10	SER/U1,2,3	H	FCK triggered enabling signal for F-channel
FPE	SEC/Q1	H	Feeds front panel switches & local light. Goes low in remote
FRES	SEC/U18	H	TRA triggered reset pulse for F-channel
GTL	SEC/U12	L	Goes high on data byte with code value 1, clears REMOTE in either AC or DD command mode
HSE	SEC/U20	L	Goes high in command mode (ATN Low) or LISTEN state, enables NDAC and NRFD for handshake
IFCI	Bus,SEC/U1	H	Clears Listen ff on either power-on or bus command
INH	SEC/U21	L	20 μs pulse, TRA triggered, inhibits handshake
LIL	SEC/U13	H	Listen monitoring signal low when in LISTEN mode
LIST	SEC/U19	L	Goes high when addressed, enables DD mode, clears when receiving UNL command
LOC	SEC/U17	H	Goes low when REM is set (high) by NCK, resets high on GTL command or REN high or power-on
MLA	SEC/U16	L	Goes high when receiving address = switch settings
NCK	SEC/U6	L	DCK derived clock pulse, enabled by numerals, one pulse per digit, also sets REM.
NDAC	SEC/U13	x	Controlled by all Listeners, low when enabled by HSE, temporarily high = Data accepted following DAV if LISTENER responds.
NRFD	SER/U13	H	Controlled by all Listeners on bus, pulled Low = Not Ready following DAV, if listener responds. Released high again after NDAC gone low.
OC	SEC/U15	H	Goes low in REMOTE mode, enabling output registers
PUR	SEC/U9	H	Goes temporarily low on power-on.
QHS	SEC/U19	L	Controls handshake signals, goes temp. high in normal handshake cycle.
RCL	SEC/U15	H	Initializing signal, temporarily low only on power-on.
REL	SEC/Q2	L	Feeds REMOTE light on front-panel, goes high in remote.
REM	SEC/U17	L	Complementary signal to LOC, high in REMOTE Mode
REN	Bus,SEC/U9	x	Low in remote enable state, set by controller
SB1	SEC/U4	x	DIO1 derived data bit, weight 1, high when true
SB2	SEC/U4	x	DIO2 derived data bit, weight 2, high when true
SB4	SEC/U4	x	DIO3 derived data bit, weight 4, high when true
SB8	SEC/U4	x	DIO4 derived data bit, weight 8, high when true
STR	SEC/U18	L	DAV derived master clock pulse, one per byte
TRA	SEC/U13	L	DCK derived, LF enabled pulse, stores outputs.

SPECIFICATIONS

The interface consists of the SEC 1022 board and the SER 1023 board.

1. **Interface Functions:**

   Subset implemented as per IEEE-Std 488-1978.

   SH**0**, AH1, T**0**, L1, SR**0**, RL2, PP**0**, DC**0**, DT**0**, C**0**

   Output driver type E1 = Open collector

2. **Inputs:**

   GPIB signals via J1 as per standard with DIO8, EOI and SRQ inactive.

3. **Internal Decoding:**

Name	ASCII char.	ASCII dec.	Function
GTL	SOH	1	Local mode
LF	LF	10	Transfer data
LAD	SP... >	32-62	Listen addresses
Numerals	0-9	48-57	Control parameter
UNL	?	63	Unlisten
A	A	65	Level control code
F	F	70	Frequency control code

4. **Outputs via P1:**

   For **frequency** control, tristate, LS-TTL compatible
   Option/160: 36 parallel bits, digit #1 through digit #8
   BCD coded, digit #9 hexadecimal coded: **0**-F
   Option/200: 37 parallel bits, all digits BCD coded, digit #10 one bit only: **0**-1
   Option/500: 39 parallel bits, all digits BCD coded,
   digit #10 three bits only: **0**-7, (4)

   For **level** control, all options:
   4 parallel bits, BCD coded for attenuator control
   LSTTL compatible, tristate, also available via J2.
   + analog level control voltage, 2V maximum.

   Controlled voltage for panel switches, 5V max. (FPE)

   Monitor signals for REMOTE, LOCAL and LISTEN status.

5. **Power requirements:**

   5.4 V @ 520-540 mA typical

SERVICE

Maintenance

No maintenance is normally required. Only components subject to wear are the external connectors and the address switches. They are expected to outlast the normal life expectancy of the instrument.

Trouble Shooting

General

The interface circuitry is essentially digital, involving basically TTL type integrated circuits. Generally speaking, fault finding techniques require the use of logic probes and or logic analyzers, since many of the digital processes are sequential in nature.

Furthermore, with any bus controlled instrument, malfunctions may also be caused by the controller, by program errors (software) and possibly by other devices on the bus. Such possible causes have to be eliminated first:

Verify, if possible the proper operation of the bus controller. Suitable bus testers are available from several sources.

Check operation without any other devices on the bus to eliminate possible hangup problems caused by another device.

Check operation of the instrument in the "LOCAL" mode with the bus cable disconnected. If this mode cannot be established, as evidenced by the front panel LED, trouble could also be elsewhere in the instrument. If "LOCAL" is O.K., then the interface is most likely at fault.

For most of the following checks we require access to the inside. Remove both covers which allows limited probing on many key points.

Before performing any digital tests, check first:

The 5.4V rail at the power supply board. If O.K., check the supply voltages on pin #6 interconnecting SEC and SER to be the same as on the rail, on an accessible Vcc pin #16 of each board: A1 on SEC, U1 on SER. These voltages are typically 5.0 ± 0.2V. If less than 4.7V, decoupling resistors R23 on SEC and R33, 34 on SER are suspect. Any required repair requires removal of the interface. Proceed further only after the power supply conditions are normal.

Digital Fault Tracking

The following covers a few major fault conditions and related fault finding checks, but limited to what can be diagnosed without removing the interface. Probing points are therefore restricted to those on the bus connector, the contact points on J1, SER, on some IC's at the edge of SER and the output connections P1, SER.

If these tests are inconclusive, return of the suspect unit for factory test repair is recommended. If test results and inspection indicate specific defects, repair may be attempted after removing and disassembling the interface.

In the following test procedures we try first static checks using simple logic probes or a voltmeter. Dynamic test are necessary to check on sequential logic and require at least a pulse indicating probe; a transition counter would be useful in tracing more subtle faults. When a signal name is referred to in capital letters, consult also the list of key signals for more information which should prove helpful in diagnosing the problem.

For static tests good/bad limits are:

State	Good	Bad
Low	>0V, <.8V	>0.8V
High	>2.4V	<2.4V

unless otherwise noted. Note that with a good Low, there is a small positive voltage, never 0. A 0 voltage indicates a **short.**

Major Faults

1: No "LOCAL" control function

Disconnect bus cable. Static tests. Check progressively.

Signal	At	On	Good State	Possible defects if test result is bad
FPE	Coll. Q1	SEC	>4V	short, Q1, U15, R22, OC stuck low
FPE	17J1	SER	>4V	interconnection open, shorts
FPE	34P1	SER	>4V	track on SER, shorts
FPE	common rail on front panel switches		>4V	track on SER, shorts
OC	16J1	SER	High	U15, shorts (SEC,SER)
LOC	19J1	SER	High	Shorts, U17
RCL	R29, C7	SEC	Low	U7, 9, 15

The following tests are done with bus connected, but no other devices on bus.

2: No response to commands, does not go remote

Verify first proper match of address setting on rear panel switch with address used by controller/talker.

If O.K., set switch to "LISTEN ONLY" and execute a command sequence. If instrument responds, trouble could be in address related circuits on SEC; suspects are S1-5, U2, 3, 4, 5, 9, 16. However, there could also be a controller problem, not sending the correct address. If no response, reset switch to "ADD'D" position, and try first:

Static Tests, with controller idling, but REN asserted (low).

Check progressively.

Signal	At	On	Good State	Possible defects, if bad	Comments
REN	pin 17	bus	Low	controller	
	15A1	SEC	Low	connection	
RCL	R29,C7	SEC	High	U7, 9, U15, C7	
IFC	pin 9	bus	High	controller, short	
IFCI	14U9	SEC	High	C2,U19	
ATN	pin 11	bus	High	controller, short	
$\overline{\text{ATN}}$	2U20	SEC	Low	U7, open	
ATN	3U16	SEC	High	U7, short	
NRFD	pin 7	bus	High	controller, short, U13	Handshake
QHS	5U19	SEC	Low	U19, U9	related
PUR	4U19	SEC	High	U9, 19, C1, shorts	related
HSE	11U20	SEC	Low	U20, 7	related
DAV	pin G	bus	High	controller, short	
NDAC	pin 8	bus	High	controller, short, U13	related
$\overline{\text{DAV}}$	2U18	bus	Low	U7	related
DIO7	pin 15	bus	High	controller, short	affects:
D7	1U165	SEC	High	U3, 7, Open	Listen address
Clock	13U19	SEC	High	U20, short	Listen Clock

If earlier test in LISTEN ONLY mode was good, but addr'd mode was not, check also other data lines.

DIO6	pin 14	bus	High	controller, short	may impair
D6	2U3	SEC	High	U3,U4, Open	
DIO5	pin 13	bus	High	controller, short	proper addressing
D5	4U3	SEC	High	U3, U4, Open	
$\overline{\text{DIO4}}$	pin 4	bus	High	controller, short	proper addressing
$\overline{\text{D4}}$	1OJ1	SER	Low	U4, Open	
$\overline{\text{DIO3}}$	pin 3	bus	High	controller, short	proper addressing
$\overline{\text{D3}}$	9J1	SER	Low	U4, Open	
$\overline{\text{DIO2}}$	pin 2	bus	High	controller, short	proper addresssing
$\overline{\text{D2}}$	8J1	SER	Low	U4, open	
$\overline{\text{DIO1}}$	pin 1	bus	High	controller short	proper addressing
$\overline{\text{D1}}$	7J1	SER	Low	U4, open	

If static tests indicate normal conditions proceed with:

Dynamic Tests

Send a command string containing at least **one** numeral and monitor with a pulse indicating probe at the same time progressively. Command string assumed to end with UNL.

Signal	At	On	Good Condition	Possible defects, if bad	Comments
DAV	pin 6	bus	one ⌐⌙⌐ each byte	controller	All
$\overline{\text{DAV}}$	2U18	SEC	one _⌐⌙_ each byte	U7, conn	functions
STR	5U16	SEC	same as $\overline{\text{DAV}}$	U1R, R45, C3	impaired
MLA	11U19	SEC	_⌐¬_ once/mes.	U2, U16	Listening
LIST	9U19	SEC	_⌐¬_ once/mes.	U19, 20	impaired
HSE	11U20	SEC	_⌐¬_ once/mes.	U20, U13	impaired
LIL	20J1	SER	⌐⌙⌐ once/mes.	U13	Impaired

3: No data transfer (goes remote, but no data transfer or only partial)

Static tests, with interface set to remote state.

Controller idle. Check progressively.

OC	10U15	SEC	Low	U15
OC	16J1	SER	Low	connection
TRA	8U13	SEC	Low	U13
TRA	13J1	SER	Low	connection
FRES	12U18	SEC	High	U18, short
FRES	14J1	SER	High	connection
FCK	11J1	SER	Low	U1,8, connection

If O.K. so far, proceed with:

Dynamic Tests

Send a frequency command with 10 digits, monitor simultaneously progressively.

Signal	At	On	Good	Possible defects, if bad	Comments
TRA	13J1	SER	⎍ once per command	U10,13,R24,49, connection	impairing transfer
TRA	7U9	SER	⎍ once per command	track	to output registers
FRES	12U18	SEC	⎴ once per command	U18, connection	
FRES	14J1	SER	⎴ once per command	connection	
FRES	1U4	SER	⎴ once per command	track	
FCK	11J1	SEC	⎍ 10 times each	U1, 8, 6, 14	impairing serial
FCK	9U4	SER	command	track	conversion
FE2	8U1	SER	⎴ once per command	U1, Conn.	impairing output
FE2	15U17	SER			registers
FE6	14U2	SER	⎴ once per command	U2, U1	
FE6	15U20				
FE100	14U3	SER	⎴ once per command	U3, 2, 1	
FE100	9U16	SER	⎴ once per command		

If all of these checks prove O.K., check continuity of TRA line to all points on SER. If this is O.K., problem is more deep seated.

4: Single digit in error, otherwise OK

Most likely cause if faulty output register or an open control line FEx, TRA or OC to the particular digit. Check operation of these control lines **at the associated pins** of the IC in question, as indicated before. Check also the 4 output bit lines for possible-connection problems, open or shorts.

5: Same bit error in all digits

Example: Only even numbers would implicate bit 1, originating from **SB1** through U11, SER.

Check suspected **SB**xLine for activity. If dead, suspect SEC or interconnection. If O.K., check D1 line for activity. If bad, suspect associated IC, U11 for bit "1", U19 for bit "2", U14 for bit "4", U22 for bit "8".

Most any other problem is likely to be more complex and not expected to be resolved or repaired in the field.

SEC-1022 Parts List

Schematic Design	Description	PTS P/N
	CAPACITORS	
C1	47uF, El. Tant. 6V	30-5102
C2	10nF, 80/20%, 50V, 25V	23-0103
C3	47pF, 10%, 500V, X5F	22-0470
C4	100pF, 10%, 500V, X5F	22-0101
C5	1nF, 10%, 500V, X5F	22-0102
C6	6.8uF, El. Tant. 16V	30-5101
C7	10nF, 80/20%, 50V, Z5V	23-0103
C8	50nF, 80/20%, 50V, Z5V	23-0503
C9	50nF, 80/20%, 50V, Z5V	23-0503
C10	50nF, 80/20%, 50V, Z5V	23-0503
C11	50nF, 80/20%, 50V, Z5V	23-0503
C12	50nF, 80/20%, 50V, Z5V	23-0503
C13	50nF, 80/20%, 50V, Z5V	23-0503
	DIODES	
CR1	LED, green	88-4955
	CONNECTORS	
J1	24 contact, PC mount	78-1024
J2	5 contact, receptacle	79-1005
P1	header strip, 20 contacts	79-1002
	TRANSISTORS	
Q1	2N2905	42-2905
Q2	2N2905	42-2905
	RESISTORS	
A1	Resistor network, 28 resistors	66-5001
R5	100, 5%, ¼W	10-0101
R12	4.7K, 5%, ¼W	10-0472
R16	100, 5%, ¼W	10-0101
R18	1.5K, 5%, ¼W	10-0152
R19	150, 5%, ¼W	10-0151
R20	4.7K, 5%, ¼W	10-0472
R21	2.2K, 5%, ¼W	10-0222
R22	1K, 5%, ¼W	10-0102
R23	2.2, 5%, ¼W	10-0220
R24	2.2K, 5%, ¼W	10-0222
R29	330, 5%, ¼W	10-0331
R42	4.7K, 5%, ¼W	10-0472
R43	220, 5%, ¼W	10-0221
R44	4.7K, 5%, ¼W	10-0472
R45	6.8K, 5%, ¼W	10-0682
R46	10K, 5%, ¼W	10-0103
R47	6.8K, 5%, ¼W	10-0682

SEC-1022 Parts List (continued)

Schematic Design	Description	PTS P/N
	RESISTORS (cont.)	
R48	15K, 5%, ¼W	10-0153
R49	1.5K, 5%, ¼W	10-0152
R50	22K, 5%, ¼W	10-0223
R51	4.7K, 5%, ¼W	10-0472
R52	4.7K, 5%, ¼W	10-0472
R53	4.7K, 5%, ¼W	10-0472
R54	4.7K, 5%, ¼W	10-0472
R55	4.7K, 5%, ¼W	10-0472
R56	4.7K, 5%, ¼W	10-0472
	SWITCHES	
S1-S6	6 PST DIL	87-1006
	INTEGRATED CIRCUITS	
U1	74LS08	63-0008
U2	93L24	61-0024
U3	74LS04	63-0004
U4	74LS14	63-0014
U5	74LS21	63-0021
U6	74LS21	63-0021
U7	74LS14	63-0014
U8	74LS107	63-0107
U9	74LS04	63-0004
U10	74LS30	63-0030
U11	93L24	61-0024
U12	74LS21	63-0021
U13	7438	60-0038
U14	74LS21	63-0021
U15	7405	60-0005
U16	74LS11	63-0011
U17	74LS51	63-0051
U18	74LS123	63-0123
U19	74LS112	63-0112
U20	74LS00	63-0000
U21	555	64-0555

SER-1023 Parts List

Schematic Design	Description	PTS P/N
	CAPACITORS	
C1	6.8uF, El. Tant. 16V	30-5101
C2	6.8uF, El. Tant., 16V	30-5101
C3	50nF, 80/20%, 50V, Z5V	23-0503
C4	50nF, 80/20%, 50V, Z5V	23-0503
C5	50nF, 80/20%, 50V, Z5V	23-0503
C6	50nF, 80/20%, 50V, Z5V	23-0503
	CONNECTORS	
J1	Connector strip, female, 20 cont.	79-1004
P1	Header strip, 25 contacts	79-1003
	Header strip, 25 contacts	79-1003
	RESISTORS	
R1-R32	2.2K, 5%, ¼W (32x)	10-0222
R33-R34	2.2K, 5%, ¼W (2x)	10-1220
R35	1.21K, 1%	14-5110
R36	1.21K, 1%	14-5110
R37	1K, 10%, .75W	17-5104
R38	100K, 5%, ¼W	10-0104
R39	4.7K, 5%, ¼W	10-0472
R40	2.2K, 5%, ¼W	10-0222
R41	1.3K, 1%	14-5111
R42	866, 1%	14-5109
R43	634, 1%	14-5108
R44	470, 5%	10-0471
R45	365, 1%	14-5107
R46	301, 1%	14-5106
R47	243, 1%	14-5105
R48	2.2K, 5%, ¼W	10-0222
R49	2.2K, 5%, ¼W	10-0222
R50	2.2K, 5%, ¼W	10-0222
R51	2.2K, 5%, ¼W	10-0222

SER-1023 Parts List (continued)

Schematic Design	Description	PTS P/N
	INTEGRATED CIRCUITS	
U1	74LS74	63-0074
U2	74LS175	63-0175
U3	74LS175	63-0175
U4	74LS174	63-0174
U5	74LS74	63-0074
U6	74LS174	63-0174
U7	74LS173	63-0173
U8	74LS145	63-0145
U9	74LS173	63-0173
U10	74LS173	63-0173
U11	74LS164	63-0164
U12	74LS173	63-0173
U13	74LS174	63-0174
U14	74LS164	63-0164
U15	74LS173	63-0173
U16A (160 MHz)	74184	60-0184
or		
U16B (200 MHz)	74LS173	63-0173
U17	74LS173	63-0173
U18	74LS173	63-0173
U19	74LS164	63-0164
U20	74LS173	63-0173
U21	74LS173	63-0173
U22	74LS164	63-0164
U23	74LS173	63-0173
U24	74LS173	63-0173

Rev. 2: Additions or changes

	RESISTORS	
R52-54	2.2K, 5%, ¼W	10-0222
R55	680, 5%, ¼W	10-0681
	INTEGRATED CIRCUITS	
U4	74LS273	63-0273

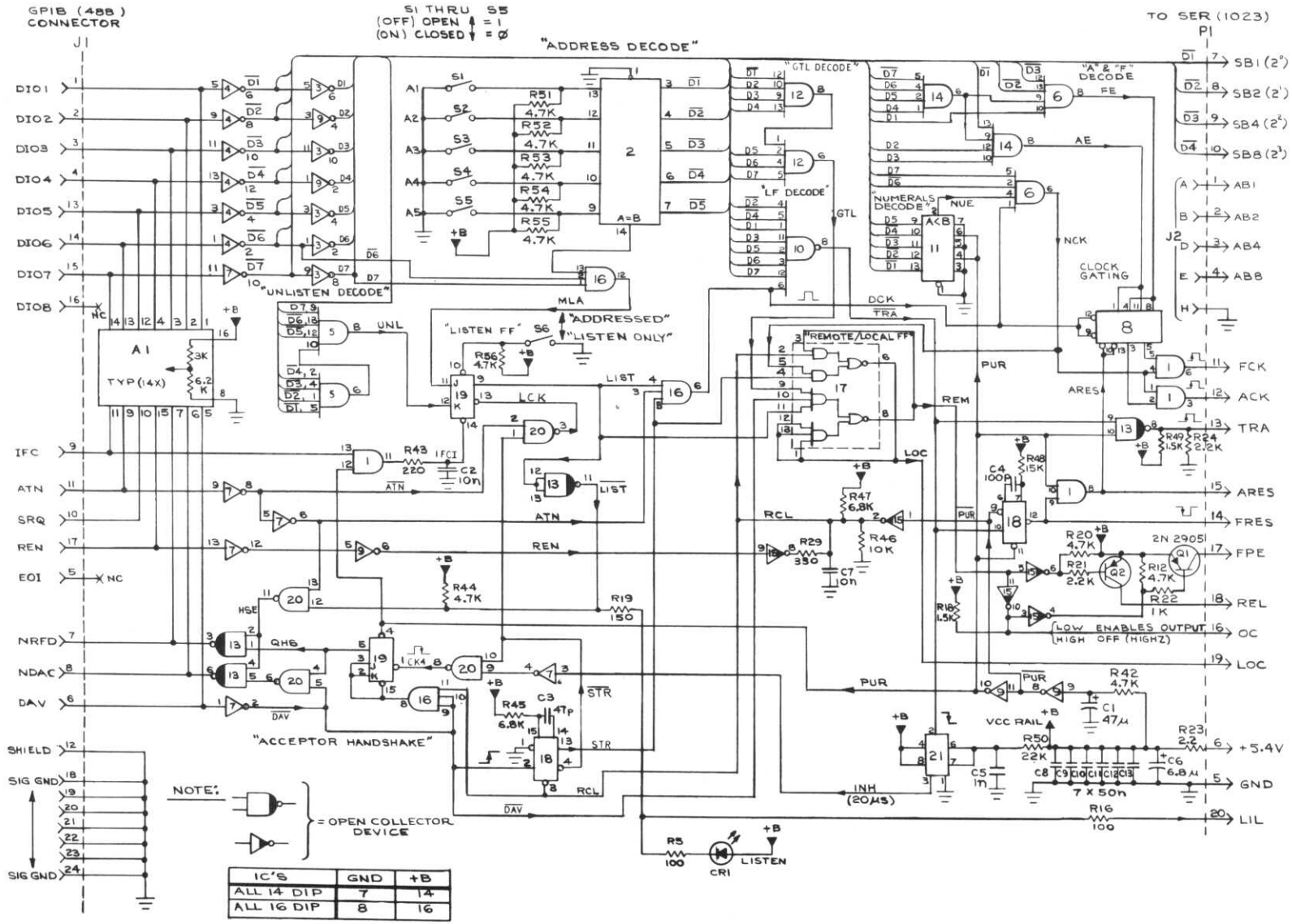
GPIB (488) CONNECTOR
J1
S1 THRU S5
(OFF) OPEN = 1
(ON) CLOSED = 0
"ADDRESS DECODE"
TO SER (1023)
P1
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
"UNLISTEN DECODE"
"GTL DECODE"
"LF DECODE"
"A" & "F" DECODE
"NUMERALS DECODE"
CLOCK GATING
MLA
"ADDRESSED"
"LISTEN ONLY"
"LISTEN FF"
"REMOTE/LOCAL FF"
IFC
ATN
SRQ
REN
EOI
NRFD
NDAC
DAV
SHIELD
SIG GND
"ACCEPTOR HANDSHAKE"
LOW ENABLES OUTPUT
(HIGH OFF (HIGHZ)
VCC RAIL
INH (20µs)
LISTEN
NOTE:
= OPEN COLLECTOR DEVICE
SB1 (2°)
SB2 (2¹)
SB4 (2²)
SB8 (2³)
AB1
AB2
AB4
AB8
FCK
ACK
TRA
ARES
FRES
FPE
REL
OC
LOC
+5.4V
GND
LIL
2N 2905
7 X 50n
IC'S | GND | +B
ALL 14 DIP | 7 | 14
ALL 16 DIP | 8 | 16

Figure 1

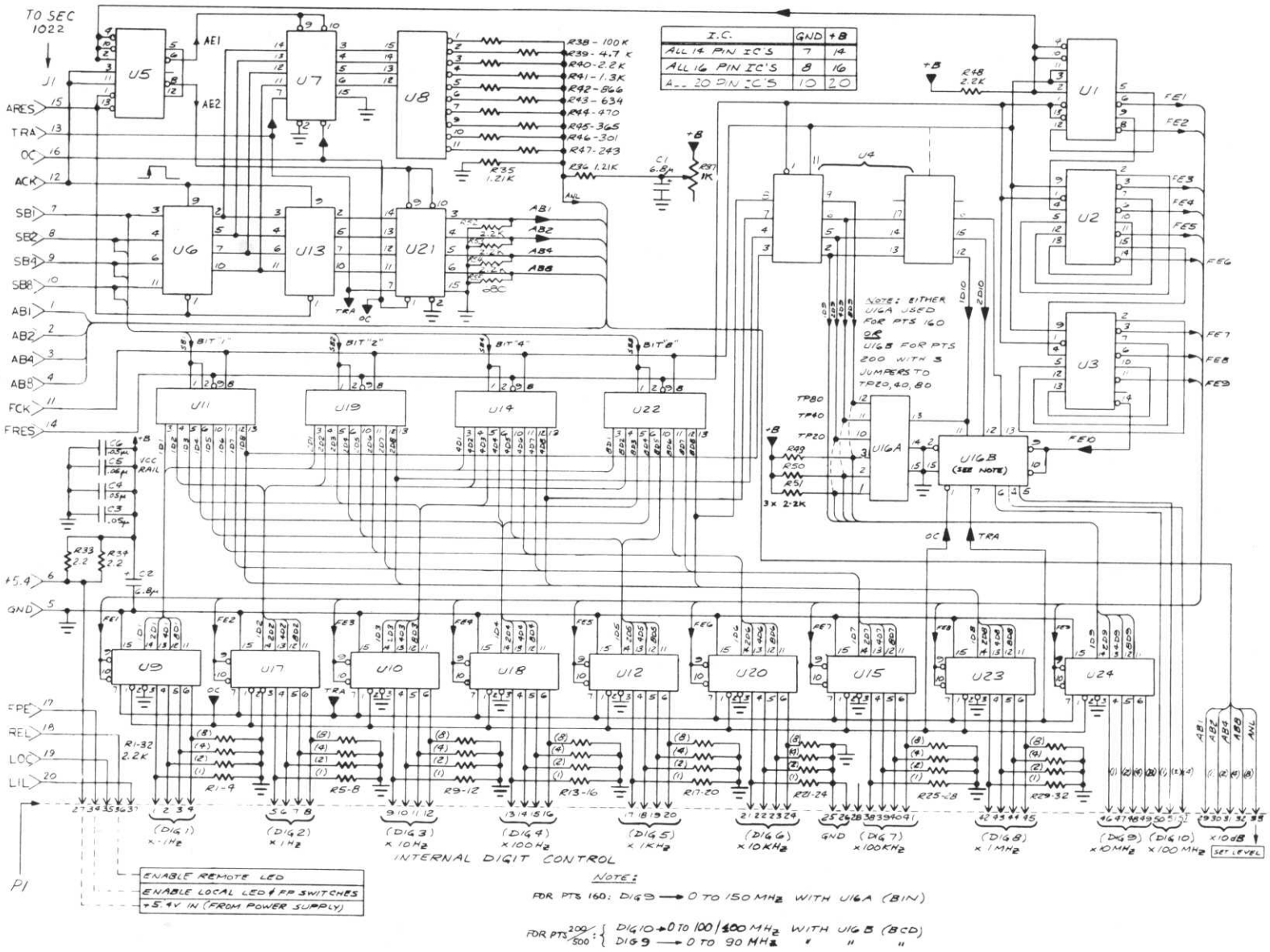
TO SEC 1022
J1
ARES
TRA
OC
ACK
SB1
SB2
SB4
SB8
AB1
AB2
AB4
AB8
FCK
FRES
+5.4
GND
EPE
REL
LOC
LIL
P1
U5
U7
U8
U6
U13
U21
U11
U19
U14
U22
U9
U17
U10
U18
U12
U20
U15
U23
U24
U1
U2
U3
U4
U16A
U16B (SEE NOTE)
I.C. | GND | +B
ALL 14 PIN IC'S | 7 | 14
ALL 16 PIN IC'S | 8 | 16
ALL 20 PIN IC'S | 10 | 20
R38 - 100 K
R39 - 47 K
R40 - 22 K
R41 - 13K
R42 - 866
R43 - 634
R44 - 470
R45 - 365
R46 - 301
R47 - 243
R34 1.21K
R35 1.21K
R48 2.2K
R49
R50
R51
3 x 2.2K
NOTE: EITHER U16A USED FOR PTS 160 OR U16B FOR PTS 200 WITH 3 JUMPERS TO TP20, 40, 80
TP80
TP40
TP20
FE1
FE2
FE3
FE4
FE5
FE6
FE7
FE8
FE9
FE0
BIT "1"
BIT "2"
BIT "4"
BIT "8"
VCC RAIL
ENABLE REMOTE LED
ENABLE LOCAL LED & FP SWITCHES
+5.4V IN (FROM POWER SUPPLY)
INTERNAL DIGIT CONTROL
(DIG 1) x 1 Hz
(DIG 2) x 1 Hz
(DIG 3) x 10 Hz
(DIG 4) x 100 Hz
(DIG 5) x 1 KHz
(DIG 6) x 10 KHz
GND
(DIG 7) x 100 KHz
(DIG 8) x 1 MHz
(DIG 9) x 10 MHz
(DIG 10) x 100 MHz
x 10 dB
SET LEVEL
NOTE:
FOR PTS 160: DIG 9 → 0 TO 150 MHz WITH U16A (BIN)
FOR PTS 200/500: DIG 10 → 0 TO 100/400 MHz WITH U16B (BCD)
DIG 9 → 0 TO 90 MHz " " "

Figure 2

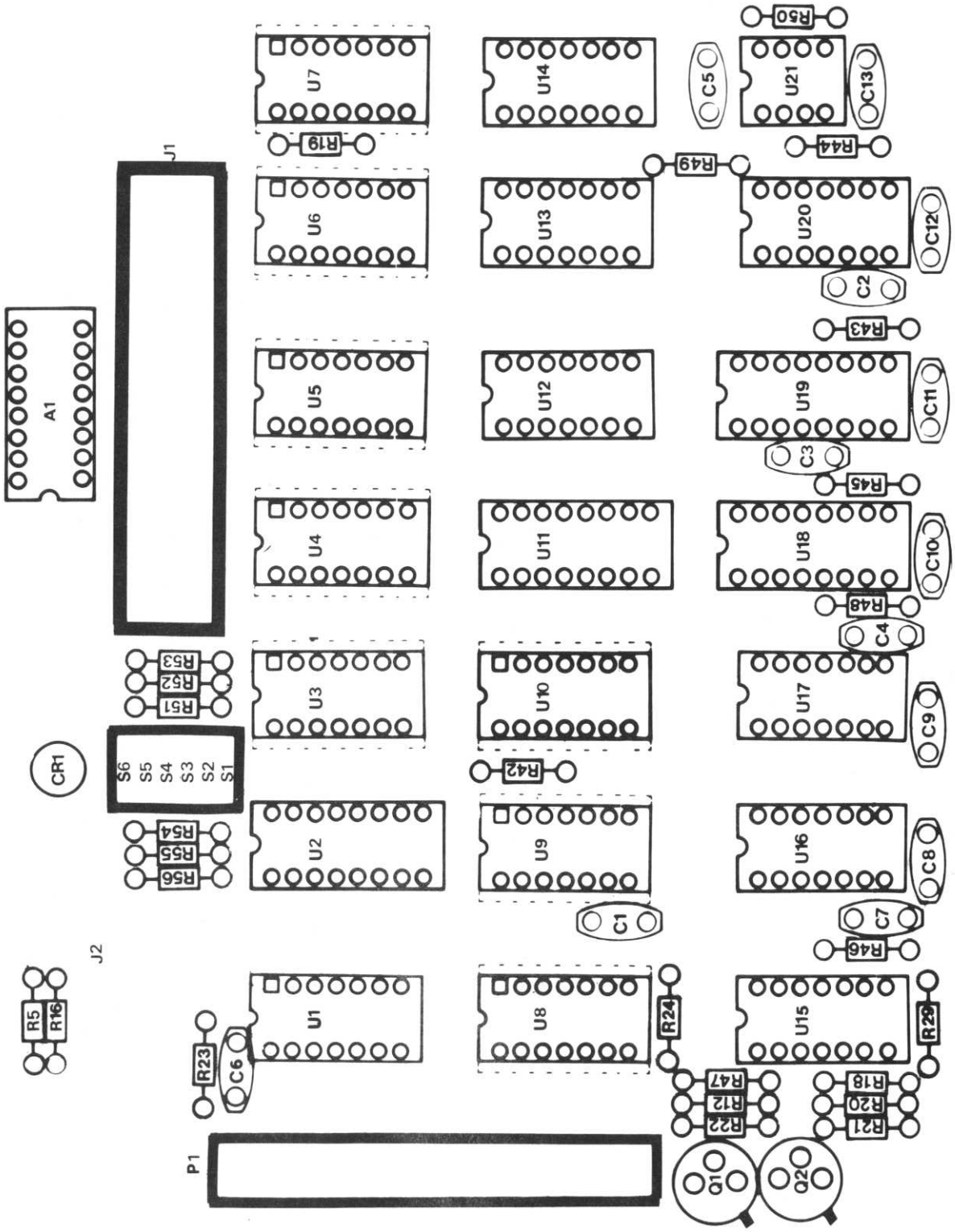
A1
J1
J2
P1
CR1
S6 S5 S4 S3 S2 S1
R5 R16
R23
C6
R51 R52 R53
R54 R55 R56
U1 U2 U3 U4 U5 U6 U7
U8 U9 U10 U11 U12 U13 U14
U15 U16 U17 U18 U19 U20 U21
R19
R24
R42
R49
R50
R44
R43
R45
R48
R46
R47 R12 R22
R18 R20 R21
R29
C1
C2
C3
C4
C5
C7
C8
C9
C10
C11
C12
C13
Q1
Q2

Figure 3

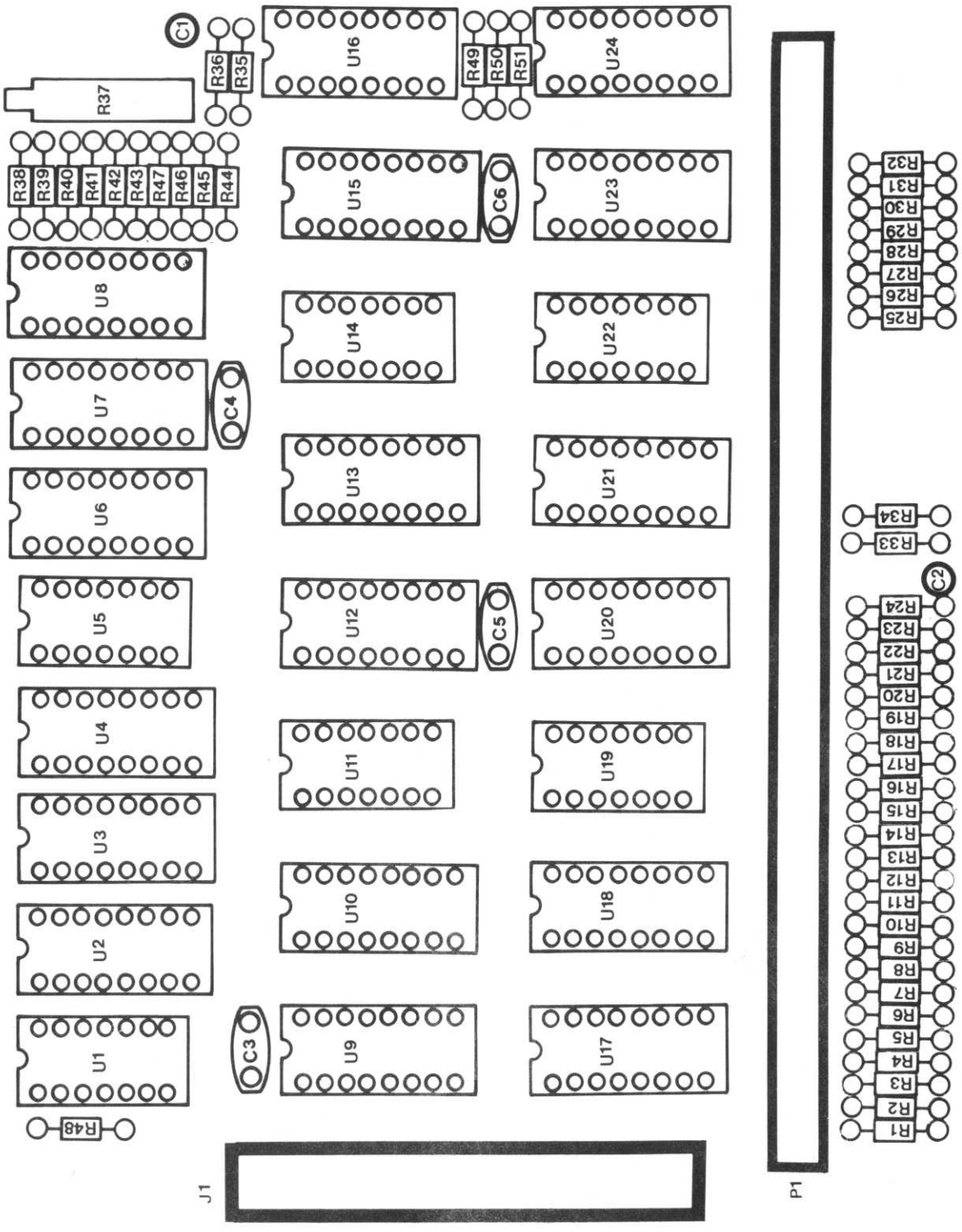
C1
R36
R35
U16
R49
R50
R51
U24
R37
U15
C6
U23
R38
R39
R40
R41
R42
R43
R47
R46
R45
R44
U8
U14
U22
U7
C4
U13
U21
U6
U5
U12
C5
U20
U4
U11
U19
U3
U10
U18
U2
C3
U9
U17
U1
R48
J1
P1
R32
R31
R30
R29
R28
R27
R26
R25
R34
R33
C2
R24
R23
R22
R21
R20
R19
R18
R17
R16
R15
R14
R13
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1

Figure 4