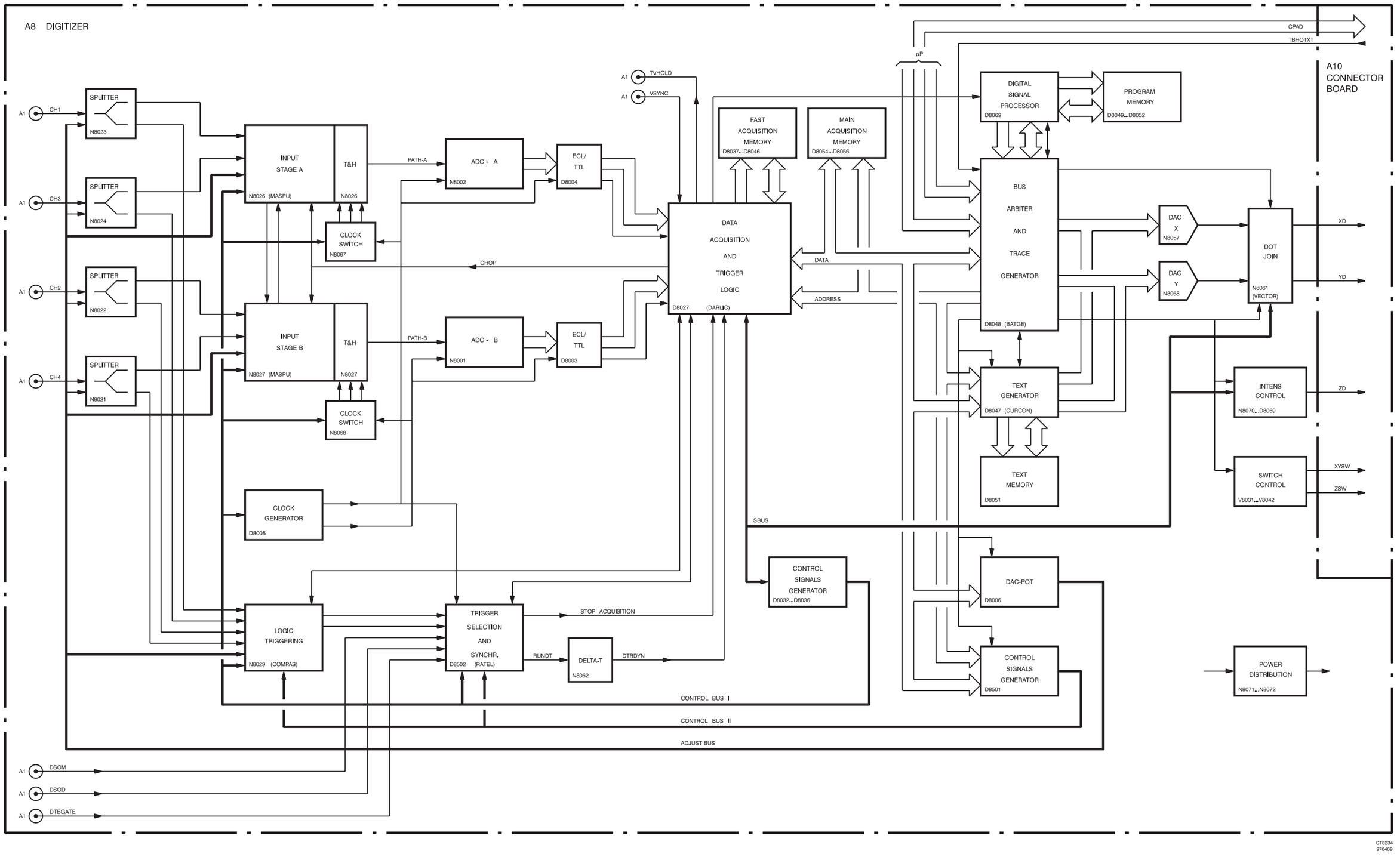

Figure 3.1 Blockdiagram, Digital part

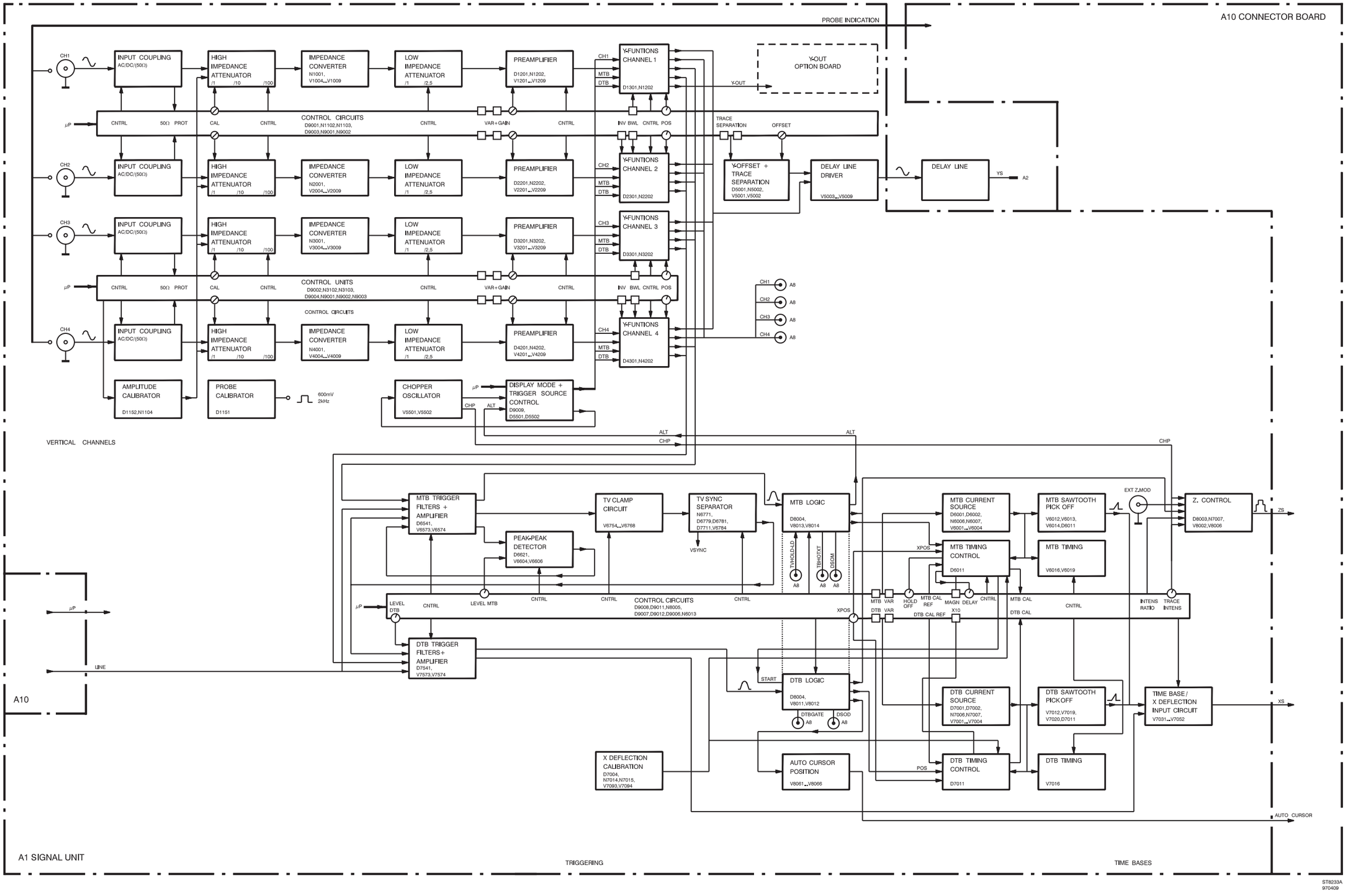

Figure 3.2 Blockdiagram, Analog part 1

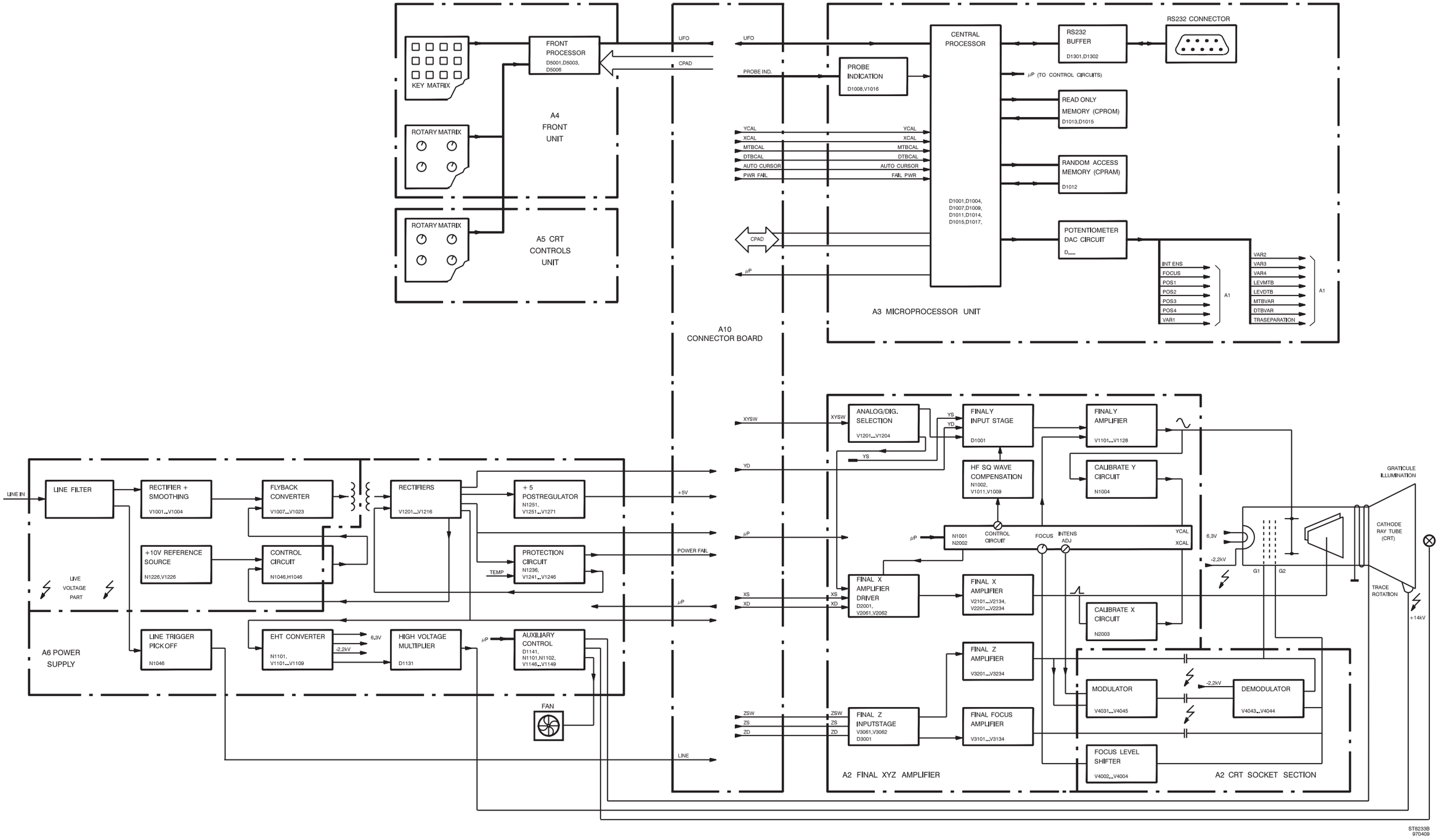

Figure 3.3 Blockdiagram, Analog part 2

3 DESCRIPTIONS

3.1 GENERAL DESCRIPTION

3.1.1 Introduction to oscilloscope family

The family consists of seven digital general purpose oscilloscopes with model numbers PM3370B, PM3380B, PM3384B, PM3390B, and PM3394B. Differences between these models are the vertical bandwidth, the features of the vertical channels and the presence of switcheable 50Ω input impedance.

Vertical bandwidth is 60, 100 or 200 MHz. The 'true 4 channel' oscilloscopes have four channels with a wide range of input sensitivities. The economy versions offer 2 channel and on External Trigger input. The table below explains the differences.

Type number	Bandwidth	Sample rate	Number of channels	Input impedance
PM3370B	60 MHz	200 MS/s	2	1 MΩ
PM3380B	100 MHz	200 MS/s	2	1 MΩ
PM3384B	100 MHz	200 MS/s	4	1 MΩ
PM3390B	200 MHz	200 MS/s	2	1 MΩ/50Ω
PM3394B	200 MHz	200 MS/s	4	1 MΩ/50Ω

The printed circuit boards (units) and mechanical parts in this family of oscilloscopes have a high degree of standardization. The ordering codes for these parts are listed in chapter 4 'Parts'.

3.1.2 Introduction to descriptions

Section 3.2 contains the description of the block diagram. The information in this diagram is presented in such a way that the link with the circuit diagrams in chapter 5 'Unit descriptions' can be found easily.

In chapter 4 'Parts' all general parts are described. These are, for example, the printed circuit boards (units), cables and mechanical parts that are not fixed to a specific unit. Cables are clearly identified on an interconnection diagram.

In chapter 5 the units are described in sequence of their number (A1, A2, A3, ...). Per unit the following information is given:

- Description
- Signal name list
- Unit lay-out (and location raster for the large units)
- Circuit diagrams (see note)
- Parts lists

Note: Some diagrams are dedicated to one or two type numbers. This is indicated in the diagram description at the bottom.

3.1.3 Explanation of signal names

Throughout the circuit diagrams signal names are used. These names make it easier to trace a signal going from one circuit diagram to another. In many cases the signal name and also the component to which a certain node is connected are given in the circuit diagrams.

For every printed circuit board a signal name list is shown in alphabetical order. It shows:
- The meaning/function of the signal.
- The signal source(s).
- The signal destination(s).

Signal names are chosen up in a logical way. Basically signal names (e.g. MTBPPLEV-HD) consist of two parts:
- A functional part with a maximum of 10 characters (e.g. MTBPPLEV). The part is arranged such that recognition is easy.
- An extension with a maximum of 2 characters (e.g. HD). The extension is not always used.

The first characters (e.g. MTB) in the **functional part** indicate the part of the oscilloscope. Examples are:
- AT1, AT2, AT3, AT4: the input attenuators of channel 1, 2, 3, 4.
- PA1, PA2, PA3, PA4: the preamplifiers of channel 1, 2, 3, 4.
- FNC1, FNC2, FNC3, FNC4: the function selection parts of channel 1, 2, 3, 4. MTR: main time base triggering.
- MTB: main time base.
- DTR: delayed time base triggering.
- DTB: delayed time base.

The last set of characters in the **functional part** (e.g. PPLEV) indicates the function: in this example Peak-Peak LEVel triggering is switched on/off.

The first character of the **extension** indicates if the signal is active when high (H), active when low (L) or that this is not fixed (X, for instance the output of a counter).

The second character of the **extension** indicates the kind of logic. Possible abbreviations are:
T (TTL), E (ECL), A (analog signal), C (CMOS 12 ... 15V) and D (CMOS 5V).

3.1.4 Voltage values in the circuit diagrams

Throughout the circuit diagrams voltage values are indicated. This facilitates fault finding in the vertical channels, triggering, time base and final amplifiers. Most of the voltages consist of an AC signal superimposed on a DC biasing voltage. Some of the AC voltages are small. They must be measured with an oscilloscope via a 1:1 probe and AC coupled input. The DC signal component is bigger and must be measured with the measuring oscilloscope with DC coupled input. The nodes where a signal can be measured are indicated with a dot on the p.c.b. lay-outs.

The oscilloscope under test must be prepared as follows:
- Connect the CAL voltage via a 10:1 probe with indication ring to the input of the suspected channel.
- Press the STATUS and TEXT OFF key simultaneously to get a defined starting position.
- Press the AUTOSET key.
- Put AMPL/VAR of the active channel to 0.1 V: this should give 6 vertical divisions of signal on the screen.

Some important notes:
- To measure some signals, it is necessary to unlock units. Refer to chapter 8.5 for details on how to proceed.
- The given AC and DC signals are average values: your oscilloscope under test may deviate from the values given in the circuit diagrams. 100 MHz clock signals and fast switching signals on the digitizer unit A8 require a measuring oscilloscope with a bandwidth of 200 MHz or more.
- Although the oscilloscope is in standard setting, it may be necessary to do manual selections for certain measurements. To measure e.g. the delayed time base and its triggering, it is necessary to activate DTB and to select a channel as DTB trigger source.The same is valid for digitizer functions like logic pattern, timed pattern, double sampling speed (250 ns/div).
- When measuring in the final amplifiers, it advised to switch off all text. This gives 'cleaner' signals at the outputs. The text is written inbetween the signal at a random basis.
- Measuring the outputs of the final Y amplifier must be done with a 10 kΩ resistor between probe tip and signal. This avoids oscillations.
- Refer to chapter 8.11.4.7 (Repair tools/DAC) on how to check the range of DAC-generated adjustment voltages.

3.2 BLOCK DIAGRAM DESCRIPTION

3.2.1 Introduction

This block diagram and description are based upon the most complex version of this family of digital oscilloscopes. Therefore there may be minor differences between your oscilloscope and the block diagram and its description. Where differences may occur it is mentioned in the text.

The item numbers of active components are indicated each block of the diagram. This facilitates to make the link with the circuit diagrams.

The oscilloscope is controlled by a microprocessor that connects to many blocks. Therefore throughout this block diagram CONTROL CIRCUITS can be found that are controlled by the microprocessor. The output signals can be simple on/off signals e.g. to switch a certain vertical channel on and off. There are also adjustable dc voltages e.g. to determine the gain of a vertical channel. Blocks that are under control of the microprocessor have the input signal "µP". In the vertical, horizontal and time base sections, circuits are added for microcomputer controlled automatic calibration.

This description is divided according to the functional blocks that can be distinguished:
- Vertical channels: there are 4 vertical channels (part 1).
- Triggering and time bases: there are sections for main- and delayed time base (part 1).
- Final amplifiers: for vertical (Y) and horizontal (X) deflection, intensity (Z) and focusing contro (part 2)l.
- Front unit and microprocessor unit (part 2).
- Power supply unit (part 2).
- Digitizer unit (part 3).

Also the printed circuit boards (units) are indicated in the blockdiagram. These units are:
- Signal unit A1: is the largest of all and incorporates 4 vertical channels and main- and delayed triggering and time base.
- Final XYZ amplifier A2: all final amplifiers are present here. A separate part is connected to the CRT socket.
- Microprocessor unit A3.
- Front unit A4: incorporates most of the rotary knobs and keys.
- CRT controls unit A5: incorporates the rotary knobs for the display functions.
- Power supply unit A6: supplies various voltages to the other circuit boards.
- Digitizer unit A8: includes all digital storage circuitry.
- Motherboard A10: many signals are routed via this unit.

3.2.2 Vertical channels

There are 4 vertical channels that are mainly identical. A difference is that the 200 MHz oscilloscope versions have a switchable 50Ω input impedance while the 100 MHz and 60 MHztypes do not have this feature.
Another difference is between the 4 channel and the 2 channel versions. The 4 channel scopes have 4 identical vertical channels (CH1, CH2, CH3 and CH4) with an extensive range of input sensitivities. The various input sensitivities are made by combinations of settings of HIGH IMPEDANCE ATTENUATOR, LOW IMPEDANCE ATTENUATOR and PREAMPLIFIER.
The 2 channel versions have 2 identical vertical channels (CH1 and CH2) with an extensive range of input sensitivities. Channel 1 operation and the differences with channels 2, 3 and 4 are now explained.
In the 2 channel versions the channel CH3 is omitted and the EXT TRIG input has 2 switchable input sensitivities.

The CH1 input signal is applied to the INPUT COUPLING block. Here selection between ac or dc coupled input is done. Moreover in the 200 Mhz oscilloscopes selection between 50Ω and 1 MΩ input impedance is done here. A signal 50Ω PROTection signals via the CONTROL CIRCUITS to the microprocessor if the dissipation in the 50Ω termination resistor gets too high.

The block HIGH IMPEDANCE ATTENUATOR incorporates the attenuation coefficients /100, /10 and /1. This block has a fixed attenuation for the ExtTrig channel in the 2 channel oscilloscopes. The input signal originating from the AMPLITUDE CALIBRATOR is used to automatically calibrate the vertical channels. The AMPLITUDE CALIBRATOR is a generator that can deliver 8 different accurate voltages. The HIGH IMPEDANCE ATTENUATOR also comprises a high-frequency square-wave adjustment; this is done by adjustment of dc signal CAL.

The IMPEDANCE CONVERTER converts the input signal at high input impedance into an output signal at a low impedance. This block is followed by a LOW IMPEDANCE ATTENUATOR that makes the attenuation coefficients /2,5 and /1. This block has a fixed attenuation in the ExtTrig channel of the 2 channel oscilloscopes.

The PREAMPLIFIER incorporates gain/attenuation coefficients x1, x5, /2 and also continuous GAIN control via a microprocessor adjustable dc signal. The PREAMPLIFIER is followed by Y-FUNCTIONS CHANNEL 1. In this block the selection is achieved of vertical display via channel 1, Main Time Base (MTB) triggering via channel 1 and Delayed Time Base (DTB) triggering via channel 1. Also the filter for the Bandwidth Limiter (BWL), the vertical position control (POS) and an output to the digitizer (EXT). From Y-FUNCTIONS CHANNEL 1 the signal for the Y- OUTput socket is derived. The Y-FUNCTIONS blocks of channel 2 and 4 have an INVert function for signal inversion.

The selection of the vertical channel, MTB and DTB trigger source is initiated by the block DISPLAY MODE + TRIGGER SOURCE CONTROL. The channels and trigger sources to be displayed are controlled by the microprocessor (μP). In ALTernate display mode the switching between channels/trigger sources occurs at the end of the MTB sweep. The signal ALT controls this. For the vertical display mode CHOPpped a 2MHz CHOPPER OSCILLATOR is present. Display blanking during switching from one channel to another is done via signal CHP.

The selected vertical channel(s) are applied to the DELAY LINE DRIVER. This block is an amplifier that has the correct output impedance to drive the DELAY LINE. The DELAY LINE itself consists of a coaxial cable giving sufficient signal delay so that propagation delay in the trigger circuits is compensated. Because of this leading edges of fast-rising pulses can be made visible. The Y-OFFSET + TRACE SEPARATION block can influence the offset of the signal applied to the DELAY LINE DRIVER. This is used as offset compensation and also for TRACE SEParation in ALTernate Time Base mode.

The PROBE CALIBRATOR is a generator delivering a 2kHz/600mV square- wave signal. This signal can be used to adjust the square-wave response of attenuator probes.

3.2.3 Triggering and time bases

The sections for Main Time Base (MTB) and Delayed Time Base (DTB) are for the greater part identical. Therefore the MTB part is extensively described and then the DTB part briefly. The EXTernal TRIGger input of the 2 channel versions is only different in the attenuator part, after that it is equal to and described as CH4.

Main Time Base Description.
The possible trigger sources are applied to the block MTB TRIGGER FILTERS + AMPLIFIER. The selection for triggering on the vertical channels 1, 2, 3 or 4 is done in the Y-FUNCTIONS blocks in the vertical section. Triggering is also possible on the LINE trigger signal that is derived from the mains. The MTB TRIGGER FILTERS + AMPLIFIER incorporates filters for HF- reject, LF-reject and ac or dc signal coupling. The block also incorporates the +/- slope selection. The dc control signal LEVEL MTB originating from the CONTROL CIRCUITS is routed via the PEAK-PEAK DETECTOR. This block limits in peak-peak mode the LEVEL MTB range just within the peak-peak value of the signal. For this purpose the trigger signal is applied to an input of the detector. The LEVEL MTB control signal is not limited if the peak-peak mode is inactive.

For triggering on TV synchronization pulses the blocks TV CLAMP CIRCUIT and TV SYNC SEPARATOR are used. The CLAMP CIRCUIT separates the synchronization pulses from the composite video signal. The video information is not necessary for triggering. The TV SYNC SEPARATOR filters out line, frame and field pulses. This is done for various TV systems including HDTV. A VSYNC output is connected to digitizer unit A8.

The block MTB TRIGGER FILTERS + AMPLIFIER sends trigger pulses to the MTB LOGIC. This logic is combined with the DTB LOGIC. The three output signals are used to start MTB (applied to MTB TIMING CONTROL), to switch intensity on and off (applied to Z CONTROL) and for ALTernate display switching (applied to DISPLAY MODE + TRIGGER SOURCE CONTROL). TV HOLD-LD is received from digitizer A8. TB40TXT and MTB trigger DSOM are applied to A8.

The MTB is based on the principle that selectable capacitors (inside block MTB TIMING) are charged with a selectable constant current (from MTB CURRENT SOURCE). This results in a sawtooth voltage across the capacitor(s) that rises linearly with the time. As a consequence a time-linear horizontal deflection is obtained. The sawtooth voltage is routed to the horizontal deflection part via the MTB SAWTOOTH PICK OFF. This block serves as a high to low impedance converter so that the load to the timing capacitor(s) is minimal. Various time base sweep speeds are obtained by selecting different combinations of current values and timing capacitors. The function MTB VARiable works via the MTB CURRENT SOURCE.

The MTB TIMING CONTROL discharges the capacitor(s) if the maximum level of the sawtooth is reached. The MTB TIMING CONTROL allows the charging process to start again if a trigger occurs. The functions X POSition, HOLD OFF and 10x MAGN are applied to and realized in the MTB TIMING CONTROL. HOLD OFF determines the time between discharge of the timing capacitors and the moment that a trigger pulse is allowed to start the MTB again.

The MTB TIMING CONTROL accomplishes the DELAY time function. The sawtooth voltage is compared with an adjustable dc voltage. The DTB is started where both voltages have the same level: this condition is signalled to the DTB LOGIC via signal START.

The MTB TIMING CONTROL also plays a role in the automatic MTB calibration. A reference voltage MTBCALREF is compared with the sawtooth voltage. The time necessary for the sawtooth to reach the MTBCALREF level is monitored by the microprocessor via signal MTBCAL. If necessary the MTB is readjusted. Automatic calibration of the X-path (including output circuit of MTB TIMING CONTROL) is done with accurate voltages from the block X DEFLECTION CALIBRATION.

Delayed Time Base Description.
The function of DTB TRIGGER FILTERS + AMPLIFIER is identical to the corresponding block in the MTB part. A "peak-peak detector" for LEVEL DTB is not present. The range of this control is always fixed and not related to the peak-peak level of the signal. Blocks for TV triggering are not present in the DTB section. TV triggering of the DTB occurs via output signals from the TV SYNC SEPARATOR in the MTB section.

An output signal from DTB TRIGGER FILTERS + AMPLIFIERS can be used for X DEFLection (MTB and DTB are off then) via the block TIME BASE / X DEFLECTION INPUT CIRCUIT.

The function of DTB CURRENT SOURCE, DTB TIMING and DTB SAWTOOTH PICK OFF is identical to the corresponding blocks in the MTB section. For the DTB LOGIC there is an extra input signal START to start the DTB directly after the adjusted delay time. The START signal originates from the MTB TIMING CONTROL. DTB GATE and DTB trigger DSOD are applied to A8.
The block AUTO CURSOR POSITION is used to position the voltage cursors automatically on the top and bottom level of the signal. The top and bottom levels are detected via the DTB triggering: the microprocessor scans the waveform by successively changing the DTB LEVEL and checking if triggers are still detected. Automatic calibration of the X-path (including output circuit of DTB TIMING CONTROL) is done with accurate voltages from the block X DEFLECTION CALIBRATION.

The DTB TIMING CONTROL is simpler than the corresponding block in the MTB. The functions DELAY and HOLD OFF are not present. DTB uses the MTB hold off time. This is due to the fact that the DTB can not run while the MTB does not.

X deflection selection and intensity control.
The block TIME BASE/X DEFLECTION INPUT CIRCUIT permits selection between horizontal deflection via MTB/DTB or via a signal selected via the DTB triggering (X DEFL mode).

The block Z-CONTROL controls the intensity of the signal on the screen. This also affects the focusing. Signal intensity and the intensity of text is determined in the final amplifier section.

The signal intensity is determined by the MTB LOGIC (light on/off) and DTB LOGIC (intensified part during run of DTB). The ratio between intensity of MTB and DTB is determined by control signal INTENS RATIO. Input signal CHP gives display blanking in vertical display mode chopped when switching from one channel to another. The control signal TRACE INTENS is influenced by the control with the same name. Intensity can also externally be controlled via input socket EXT Z MOD.

3.2.4 Final amplifiers

The final amplifier can be split up in parts for vertical (Y) and horizontal (X) deflection and parts for intensity (Z) and focusing control. Input signals originate from the analog as well as the digital vertical (Y) channels and time bases (X). The signals that determine X, Y and Z of the text originate from the text generator on the digitizer unit. The signal that switches between analog and digital (XYSW signal) display originates also from the digitizer. The outputs of the final amplifiers drive the Cathode Ray Tube (CRT). The various sections are explained now in sequence.

Vertical deflection.
The FINAL Y INPUT STAGE receives input signal for signal display (YS) from the DELAY LINE. A second input signal (YD) determines the vertical component of the digital trace and text information. The input signal that comes from AN/DIG SELECTION controls switching between analog and digital display. The HF SQ WAVE COMPENSATION is controlled by the microcomputer provides that signal distortion from the DELAY LINE is compensated in the FINAL Y INPUT STAGE. The FINAL Y AMPLIFIER drives the vertical deflection plates of the CRT. The voltage applied to these plates is measured by the block CALIBRATE Y CIRCUIT. Its output signal YCAL is applied to the microprocessor; this is part of the automatic vertical calibration facility.

Horizontal deflection.
The FINAL X AMPLIFIER DRIVER receives input signal for signal display (XS) from the Main and Delayed Time Base sections. A second input signal (XD) determines the horizontal (X) component of the digital trace and text information. The input signal that comes from AN/DIG SELECTION controls switching between analog and digital display. The FINAL X AMPLIFIER drives the horizonal deflection plates of the CRT. The voltage applied to these plates is measured by the block CALIBRATE X CIRCUIT. Its output signal XCAL is applied to the microprocessor; this is part of the automatic horizontal calibration facility.

Intensity and focusing.
The FINAL Z INPUT STAGE receives input signal for trace intensity (ZS) from the Z CONTROL block in the time base section. A second input signal (ZD) determines the intensity (Z) component of the text information. An input signal ZSW that comes from the digitizer allows switching between analog and digital intensity. The FINAL Z AMPLIFIER drives the intensity control electrode G1 of the CRT. This electrode is at a very negative -2.2kV voltage level. It is for that reason that a high-voltage blocking capacitor is necessary between G1 and the output of the FINAL Z AMPLIFIER. However only the ac component in the signal can pass through the capacitor. The dc and lf components are applied to the MODULATOR and modulated on a high-frequency carrier. Now they can pass through a capacitor, are demodulated in the DEMODULATOR and then the dc, lf and hf components are recombined.

The FINAL Z INPUT STAGE drives, in parallel with the FINAL Z AMPLIFIER, the FINAL FOCUS AMPLIFIER. This has the result that a well-focused spot over a large intensity range is obtained. The FINAL FOCUS AMPLIFIER drives the intensity control electrode G3 of the CRT. This electrode is at a very negative -2.2kV voltage level. It is for that reason that a high-voltage blocking capacitor is necessary between G3 and the output of the FINAL FOCUS AMPLIFIER. The ac component in the focusing signal passes through a high-voltage capacitor. The lf and dc components are derived from the DEMODULATOR that is also used in the intensity part. Focus control is possible via the FOCUS LEVEL SHIFTER.

3.2.5 Front unit and microprocessor

The front unit and microprocessor are the sections where all oscilloscope functions are controlled. Also the generation of text and the automatic calibration is controlled by the microprocessor. The operations performed by the microprocessor are determined by the ROTARY MATRIX and KEY MATRIX. Also commands from an external computer connected to the RS232 connector have the same result.

The ROTARY MATRIX and keys in the KEY MATRIX present at front unit A4 are read by the FRONT PROCESSOR. Also the ROTARY MATRIX that is present on the CRT controls unit A5 is read by the FRONT PROCESSOR. The CENTRAL PROCESSOR on the MICROPROCESSOR UNIT A6 is informed by the FRONT PROCESSOR of the settings selected with the front panel controls. Incorporated in the CENTRAL PROCESSOR is a complete RS232 interface. Serial communication is possible via the RS232 BUFFER.

The CENTRAL PROCESSOR has many inputs and outputs and forms the heart of the oscilloscope's control section. First of all there are a READ ONLY MEMORY (CPROM) and a RANDOM ACCESS MEMORY (CPRAM). The POTENTIOMETER DAC CIRCUIT is able to produce 16 independently adjustable dc voltages. These voltages are used for continuous controllable functions such as POSition, FOCUS and VARiable.

The CENTRAL PROCESSOR also has a number of analog inputs that are internally converted into digital. These inputs are used for automatic calibration (YCAL, XCAL, MTBCAL and DTBCAL), AUTOCURsor position, power fail and probe indication (via PROBE DETECTION block). An important output is the "µP" output. It is via this output that the CONTROL CIRCUIT blocks found throughout the block diagram are controlled.

The CENTRAL PROCESSOR communicates to the TEXT/CURSOR CONTROL which text and cursors have to be displayed. This information is stored in the TEXT/CURSOR MEMORY.

3.2.6 Power supply

The power supply is a switched mode type and has high efficiency. It can function on a wide range of LINE input voltages. An important part of the power supply is directly connected to the mains. This part carries LIVE VOLTAGE and measurements and repairs must be carried out via a separation transformer by a qualified technician.

The LINE IN voltage is applied to the LINE FILTER. This block prevents line interference from entering the supply unit. Also interference generated by the power supply does not enter the mains. An output signal of the filter is applied to the LINE TRIGGER PICK OFF in order to facilitate line triggering of the time bases.

The other output signal is applied to RECTIFIER + SMOOTHING: the output of this block has a dc voltage of which the height depends on the applied line voltage. This dc voltage is applied to the FLYBACK CONVERTER. This block incorporates a high voltage switching element that converts the dc voltage into a high-frequency ac voltage. This ac voltage is applied to the primary winding of a transformer. The secondary winding has many taps with connected RECTIFIERS: this gives the required supply voltages for the oscilloscope. The +5V POSTREGULATOR gives additional stabilization of the +5V supply voltage.

Stabilization of the output voltages at different line voltages is achieved by varying the on/off ratio of the switching element in the FLYBACK CONVERTER. The on/off ratio is determined in the CONTROL CIRCUIT by comparing the accurate output voltage of the +10V REFERENCE SOURCE and an output voltage of the RECTIFIERS.

The EHT CONVERTER generates the 6.3V heater voltage and -2.2kV cathode voltage for the Cathode Ray Tube (CRT). The +14kV final accelerator voltage for the CRT is generated in the HIGH VOLTAGE MULTIPLIER.

The AUXILIARY CONTROL is controlled by the microprocessor (μP) and generates three dc voltages that are used for TRACE ROTATION adjustment, GRATICULE ILLUMINATION adjustment and speed control for the FAN.

The PROTECTION CIRCUIT switches the power supply off in case of over and under output voltage, too low line voltage and too high temperature.

3.2.7 Digitizer

Blockdiagram description of the digitizer unit A8, which contains all digital storage circuits of the oscilloscope.

Main sections of the digitizer are:
- Input Stage
- Analog to Digital Converter and Clock Generator
- Control-signal Generator
- Trigger Comparator, Source Selector and Delta-t circuit
- Data Acquisition and Trigger Logic and Fast Acquisition Memory
- Main Acquisition Memory
- Digital Signal Processor and Program Memory
- Bus Arbiter and Trace Generator
- Text Generator and Text Memory
- X- and Y- Output DAC, Dotjoin circuit and Intensity Control

The digitizer unit contains a large number of integrated circuits that consists of a large amount of functions. It is not possible to measure around inside these circuits and therefore a detailed description of the functions in these integrated circuits is not given.

The functioning of the digitizer is explained using a separate blockdiagram.

In the blockdiagram description as much links as possible are made to the different components in the circuit diagrams and their item numbers.

3.2.7.1 Input stage

Four input channel signals for channels 1, 2, 3, and 4 from the analog oscilloscope section are applied to the digitizer unit via eight coaxial cables. Each of these symmetrical input channel signals is splitted in two equal signals by a signal buffer and SPLITTER.
One signal is going to an INPUT STAGE into the vertical signal data path, the other signal is supplied to pattern and state comparators in the LOGIC TRIGGERING block in the trigger signal path.

The MASPU's (Main Analog Signal Processing Unit) A and B take care of the channel switching.
The input channel signals 1 and 3 are limited and amplified to be multiplexed by the chopper circuit in MASPU-A. The same for input channel signals 2 and 4 in MASPU-B.
The multiplexed signal is amplified and split in two equal parts again. Part one is fed to a combiner in MASPU-A. Part two is fed to the combiner in the other MASPU-B.
Each channel combiner has two modes, selected by control signals.
In the first mode it supplies its own signal to a variable gain circuit and in the second mode it supplies the signal from the other MASPU to the variable gain circuit.
Via the VAR control circuit the vertical gain information for each path is applied to the circuit.
The output signal from each variable gain circuit is converted into an asymmetric signal, that is fed to a Track and Hold circuit T&H. This circuit is needed to offer a stable input signal to the analog to digital converter behind it. The T&H control signal is a 100MHz clock.

3.2.7.2 Analog to Digital Converter and Clock Generator

The T&H circuit offers a stable input signal to an analog to digital converter (ADC).
Both the ADC-A and the ADC-B are under all circumstances continuously clocked by a 100 MHz clocksignal which is generated by a CLOCK GENERATOR. The ECL output data signals of the ADC's are buffered and converted into TTL data signals by ECL/TTL translators.

3.2.7.3 Control-signal Generator

A number of control, mode and selection signals come from CONTROL SIGNAL GENERATORs via an SBUS (serial bus interface) and a serial to parallel converter. These control signals have functions in almost all circuits.

3.2.7.4 Trigger Comparator, Source Selector and Delta-t circuit

Acquisition of new signal information is stopped on receipt of an active trigger and this is completely controlled by the fully programmable trigger circuits. The time relation between the freezeing of the acquisition and the signal STOPACQ depends on the choosen trigger delay.

The trigger signal path provides for three additional trigger modes to the modes which are already present in the analog front end. It are Pattern triggering, Timed-Pattern triggering and State triggering.

The four input channel signals from the buffers and SPLITTERs are applied to four level comparators in the LOGIC TRIGGERING block.
They are compared to a user-defined pattern in a Pattern and Edge selector. When the user-defined pattern conditions are met, an internal PATTERN signal becomes active and is applied to the TRIGGER SELECTION and SYNCHRONIZATION circuit, to Timer circuits and to Timed Pattern and State circuits.

The trigger source selector will select the trigger signal, corresponding with the user-defined trigger mode.

Signals as Main Time Base trigger DSOM, Delayed Time Base trigger DSOD and DTBGATE are derived from the trigger circuits in the analog oscilloscope section.

Trigger selection, mode selection, pattern and control signals are generated via the serial bus interface and a serial to parallel converter. Events clock selection is controlled in the same way.

With events selected, the trigger detection unit catches the first edge. With this edge it enables an event counter in the DATA ACQUISITION AND TRIGGER LOGIC.
When it has finished counting the required number of events, a second stage in the trigger detection unit is enabled to catch the last event clock.

In TV trigger mode the events clock is switched to DSOM. By enabling the event counter with VSYNC (derived from the composite sync signal on DSOM) it is posible to count down with the events counter to any line in a TV signal. In digital mode the events counter is loaded with a count value one less than necessary. Now the trigger sync unit can generate a trigger on the correct TV line. In analog mode the events counter output is fed back to the analog front end as TVHOLD-LD.

In normal trigger mode the event counter is enabled by a signal from the data path. Now we can count trigger pulses for trigger delay activities during the acquisition.

A signal RUNDT is derived from the trigger circuit to start a delta-t measurement by a DELTA-T circuit. This circuit is used to measure the time elapsed between the moment of triggering and the real sample moment. It is a measure to determine the correct location in memory to store the digital code of the first sample of each acquisition cycle.
A DELTA-T counter in the DATA AND ACQUISITION TRIGGER LOGIC is running at the maximum sample clock frequency, enabled by the STOPACQ (stop acquisition) signal. Counting is stopped by the falling edge of the delta-t ready signal DTRDYN from the DELTA-T circuit.

A digital signal processor (DSP)is informed about this completion of the delta-t measurement by an interrupt signal. It then reads the value of the measurement in the DELTA-T counter and it resets the counter to zero again in order to be ready for the next DELTA-T measurement. The measurement is very important for the positioning of the sample in memory as well as on the CRT screen.

3.2.7.5 Data Acquisition and Trigger Logic and Fast Acquisition Memory

The output data from the ECL/TTL translators is applied to the DATA ACQUISITION AND TRIGGER LOGIC circuit (DARLIC), which contains a data path and a trigger engine. The data path is responsible for the total acquisition process from ADC to memory, including time-base generation and the trigger engine is responsible for the generation of a start/stop acquisition signal that is fed to the data path.

The data is latched by a register and checked on over/underflow by a detector.
Peak detectors determine minimum and maximum values of the signal. When peak is off, this circuit will pass on all the samples. A data junction lowers the data rate from 100 MHz streams to eight 25MHz data streams and guides the data from the peak circuit properly to output latches.

Data will directly be stored in a FAST ACQUISITION MEMORY (FAM) which consists of 8x a 2kx8 bit SRAM.

The FAM is addressed by two 18 bit wide address pointers, the acquisition pointer and the display pointer.

The acquisition pointer is active during the writing of new signal data information into the FAM. The write cycle starts, if enough bytes have been received. The pointer is loaded by the digital signal processor with the address of the first sample of a display cycle.

FAM data is read, 64 bits at a time, when no write actions are performed and enough time-space is available between two write actions of the acquisition path. The FAM is then addressed by the display pointer, which is automatically presetted with the address where the display should start. A kind of handshake control is responsible for correct operation.

The acquisition control logic separates the time around the trigger point in, gathering of pre- and post trigger information, and the counting down of a specific extra trigger delay.

The SBUS (serial bus interface) is part of the DARLIC circuit. It is supporting a very limited number of capabilities. Its register is controlling two open collector I/O pins, SDA (serial data) and SCL (serial clock), and a select line SSEL. The buffer enables the DSP to read the status on the SDA and SCL lines.

The SBUS is connected to a CONTROL SIGNAL GENERATOR, the DOT JOIN circuit and to the INTENSITY CONTROL circuit.

All interrupt sources within DARLIC's data path, trigger path, and other features are gathered in the interrupt register.

The DSP can write an interrupt mask into the interrupt enable registers. There are two interrupt enable registers, so that different interrupt causes can generate interrupts with different destinations. Bits in these registers that are set, enable the corresponding bit in the interrupt register to generate an interrupt.
Every bit in the interrupt register can be cleared separately by the interface clear control. They can also automatically be cleared upon a read of the interrupt register via the interrupt status buffer.

3.2.7.6 Main Acquisition Memory

The converted analog signals are stored directly from the ADC's into a FAST ACQUISITION MEMORY. Acquired data has later to be transferred to a MAIN ACQUISITION MEMORY (MAM) by means of a DIGITAL SIGNAL PROCESSOR (DSP). The MAM consists of 2x a 32kx8 bit SRAM, is non volatile and contains all trace registers. It contains an acquisition memory part as well as a display memory part and contains the data which is ready for display on the CRT screen.

3.2.7.7 Digital Signal Processor and Program Memory

The DIGITAL SIGNAL PROCESSOR (DSP) has the control over the entire DIGITIZER and performs all necessary signal processing activities, which are not available in hardware.
Signal processing functions are functions like:
- Pre-processing: Average, envelope
- Postprocessing: Mathematical functions, interpolation, filters
- Other functions: Display memory refresh, X-position control, delta-t processing and so on

One of its main tasks is the composition of the trace information out of the available registers. The SYSTEM ENGINE is responsible for the text data.
The Text and Trace Generator takes care of generating the appropriate X, Y and Z information for the vector oriented CRT.

Although the DSP has full control over the DIGITIZER the SYSTEM ENGINE is able to access all circuits in the same way.

At any point in time, the DIGITAL SIGNAL PROCESSOR can force an exit to the idle state. Under certain conditions the DSP can force a change from state three to state four.
The DSP can also write an interrupt mask into the interrupt enable registers.

The DSP uses its own PROGRAM MEMORY which consists of 2x an 8kx8 bit SRAM. It is a volatile memory and can not be accessed by any other device.

3.2.7.8 Bus Arbiter and Trace Generator

The major function of the BUS ARBITER AND TRACE GENERATOR (BATGE) is the arbitration between multiple processors, multiple memories and memory mapped I/O with a minimum of interference.
Wait cycles for memory devices are programmable and active devices like the DARLIC circuit for example, generate a "not ready signal".

The BATGE circuit is also responsible for interconnecting all address, data and control busses of the DSP, SYSTEM BUS, TEXT AND TRACE GENERATOR, DARLIC and MAM.

The eight traces are generated by the TRACE GENERATOR in the BATGE circuit.

3.2.7.9 Text Generator and Text Memory

The SYSTEM ENGINE is responsible for the text data and the Text and Trace Generator takes care of generating the appropriate X, Y and Z information in vector notation for the vector oriented CRT.

Text and cursor information to be displayed on the CRT screen, is stored in a TEXT MEMORY which consists of one 8kx8 bit SRAM circuit.

3.2.7.10 X- and Y- Output DAC, Dotjoin circuit and Intensity Control

Digital signal and text data from the MAM display part, to be displayed on the CRT screen, is via the BATGE circuit applied to the digital to analog converters DAC X and DAC Y where it is converted into analog signals. They pass a DOTS/DOTJOIN circuit and are fed to the final X- and Y- amplifier stages in the analog oscilloscope section. A switch signal for switching between analog oscilloscope operation and digital oscilloscope operation is generated by the SWITCH CONTROL circuit and fed to the X- and Y- stage. The DOTJOIN circuit is controlled via the BATGE circuit and the SBUS.

All conditions under which the INTENSITY CONTROL has to blank and unblank the CRT beam, are combined in this circuit. Information comes partly via the SBUS and partly via the BATGE circuit. The final intensity signal is fed to the final Z- amplifier stage in the analog oscilloscope section. A switch signal for switching between the analog and the digital intensity signal is generated by the SWITCH CONTROL and fed to the Z-stage.