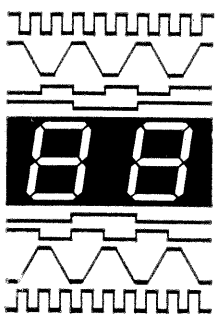
PHILIPS



Universal counters PM 6611

9446 066 110.1

PM 6613

9446 066 130.1

PM 6614

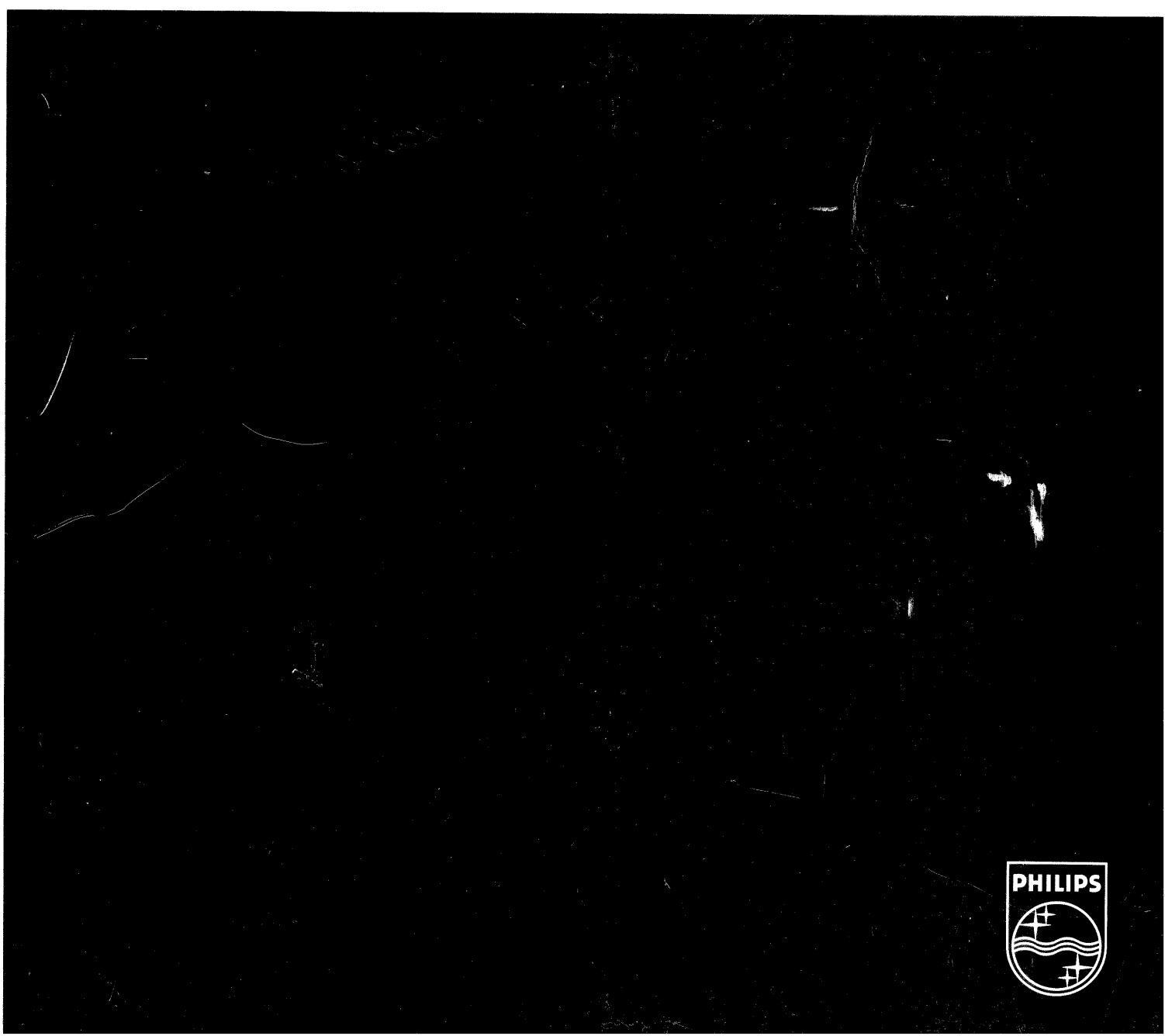
9446 066 140.1

PM 6615

9446 066 150.1

Ordering number of this manual 9499 460 07702

751215/1/2



PHILIPS



PM 6611

9446 066 110.1



PM 6613

9446 066 130.1

Instruction manual
Anleitung
Notice d'emploi et d'entretien



PM 6614

9446 066 140.1



PM 6615

9446 066 150.1

Ordering number of this manual
9499 460 07702

751215/1/2

IMPORTANT

In correspondence concerning this instrument, please quote the type number and the serial number as given on the type plate on the rear of the instrument.

WICHTIG

Beim Schriftwechsel über dieses Gerät gebeten, die genaue Typenbezeichnung und Seriennummer anzugeben. Diese befinden sich auf dem Typenschild an der Rückseite des Gerätes.

IMPORTANT

Dans votre correspondance et dans vos réclamations se rapportant à cet appareil, veuillez TOUJOURS indiquer le n° de type et le n° de série que son marquées sur la plaquette de caractéristiques fixée sur la paroi arrière de l'appareil.

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I. INTRODUCTION

The counters in the PM 6610-series have frequency ranges from 10 Hz up to 80 MHz, 250 MHz, 520 MHz and 1 GHz respectively for the PM 6611, PM 6613, PM 6614 and PM 6615.
The VHF and UHF counters PM 6613, PM 6614 and PM 6615 offer two different signal inputs for RF- and LF-signals.
All models can measure frequency, period, ratio and have a totalizing mode.
Optional accessories such as four different oscillators, a battery unit, a BCD output unit and a D/A converter extend the field of application.

II. TECHNICAL DATA

Properties expressed in numerical values with statement of tolerances are guaranteed. Numerical values without tolerances are intended for information purposes only and indicate the properties of an average instrument. The numerical values hold good for the nominal mains voltage.

A. MEASUREMENTS

Frequency

Range	10 Hz—80 MHz, PM 6611 10 Hz—250 MHz, PM 6613 10 Hz—520 MHz, PM 6614 10 Hz—1000 MHz, PM 6615
Gate times	10 ms,100 ms, 1 s and 10 s, INPUT A The gate time is multiplied with a prescaling factor if input B is used.
Resolution	100 Hz, 10 Hz, 1 Hz and 0.1 Hz
Accuracy	± 1 count ± time base error

Single period A

Range	100 ns—100 s
Frequency counted	10 MHz
Time resolution	100 ns
Accuracy	± 1 count ± trigger error* ± time base error

---

* Trigger error is $\leq 3 \times 10^{-3}$ for signals with signal to noise ratio of $\geq$ 40dB.

Period average A

Range	Sine wave: 10 Hz—10 MHz pulses: 1 Hz—10 MHz
Frequency counted	10 MHz
Number of averagings	$N = 10^2$ and 10^4 with correct decimal point positioning
Time resolution	$\frac{100\ ns}{N}$
Accuracy	± 1 count ± trigger error/N* ± time base error

Count A

Range	1 to 999999999
Mode	Accumulates pulses during manual start — stop interval
Pulse pair resolution	12 ns

Frequency ratio A/C or B/C

Range	f_A : 10 Hz—80 MHz (All models) f_B : 5— 250 MHz, PM 6613 50— 520 MHz, PM 6614 50—1000 MHz, PM 6615 f_C : 1 kHz—10 MHz (All models)
Multiplier	$N = 10^2$ and 10^4
Accuracy	± 1 count ± trigger error* of f_C/N

Check

10 MHz internally applied to channel A
Any measuring function may be selected

Auxiliary functions

Reset	Pushing "RESET" resets the counter. Releasing "RESET" starts new measurement
Start/Stop	In function "COUNT A" the gate time is manually controlled by push-button "START/STOP". The memory is automatically switched off.
Display time	Continuously variable 0.2—5 s and infinite if display time knob is pulled
Stand by	The switch is combined with display time control. Position "STAND BY" keeps an oven oscillator heated.
Memory	Switchable by push-button "MEMORY"

B. INPUT CHARACTERISTICS

Input A

Range	10 Hz—80 MHz full range, 10 Hz—100 kHz when low-pass filter is selected by push-button "< 100 kHz"
Sensitivity	Sine wave: 10 mV_{rms}, 6 dB down at 10 Hz pulses: 30 $mV_{p\text{-}p}$ for pulse width ≧ 6 ns and rise time ≦ 1 ms
Impedance	1 MΩ//25 pF
Coupling	AC
Attenuation	Continuously variable between ×1—×400 in two ranges
Trigger mode (level)	Depending on signal duty factor: > 25%—< 75%: ~ (zero crossing) < 25%: ⎍ (on leading edge) > 75%: ⎍ (on leading edge)
Safe overload	
Attenuation ×1	max. 250 V DC or 230 V_{rms} ≦ 440 Hz > 440 Hz : falling to 12 V_{rms} at > 1 MHz
Attenuation ×20	max. 250 V DC or 230 V_{rms}

---

* Trigger error is ≦ 3×10^{-3} for signals with signal to noise ratio of ≧ 40dB.

Input B (Not present in PM 6611)	*PM 6613*	*PM 6614*	*PM 6615*
Frequency range	5—250 MHz	50—520 MHz	50—1000 MHz
Dynamic input voltage range	10 mV_{rms}—12 V_{rms} (—27 dBm—+35 dBm)	10 mV_{rms}—12 V_{rms} (—27 dBm—+35 dBm)	10 mV_{rms}*—12 V_{rms} (—27 dBm*—+35 dBm)
Impedance	50 Ω	50 Ω	50 Ω
VSWR	< 2	< 2	< 2
Coupling	AC	AC	AC
Attenuation	by automatic PIN diode attenuator, maximum 62 dB.		
Prescaling factor	4	8	16
Safe overload	12 V_{rms}	12 V_{rms}	12 V_{rms}
AM tolerance	98% at ≤ 5 kHz modulation frequency 30% at ≥ 1 MHz modulation frequency	All models	

Input C (rear)

Range	1 kHz—10 MHz
Sensitivity	500 mV_{rms}
Coupling	AC
Impedance	≈ 10 kΩ
Safe overload	50 V_{rms}

Ext. oscillator — Via Input C.

C. OUTPUT CHARACTERISTICS

10 MHz OUT

Output frequency	Internal oscillator frequency (10 MHz)
Signal level	≈ 1 V_{rms} (open circuit)
Output impedance	Approximately 200 Ω (short-circuit proof)
Coupling	AC

Display — 9 digits
In-plane 7 segment gas discharge display with decimal-point indication

Gate lamp — Indicates that main gate is open and counting takes place. In stand-by position, the Gate lamp indicates that mains or battery voltage is connected

D. GENERAL CHARACTERISTICS

Oscillator — See section Accessories and the service manual

Supply

By mains	100—130 V or 200—260 V, 50 to 400 Hz, 15—25 VA
By external battery	+11.8—+28 V, max 1 A—0.5 A at 12 V and 24 V respectively. 100 mA in STAND BY position if oven stabilized oscillator is mounted
Connector	4 mm banana connector
By internal battery option	PM 9673

* Above 960 MHz, the sensitivity of the PM 6615 might drop to 14 mV_{rms} (—24 dBm) at 1 GHz

Environmental characteristics

Temperature	
Storage	—40°C to +70°C —40°C to +50°C (With battery option PM 9673)
Operating	0°C to +50°C (0°C to +40°C with battery option PM 9673)
Mains interference:	Below CISPR
Altitude	Max. 90% RH (26°C dewpoint)
Storage Operating	15000 m (50000 ft) 5000 m (15000 ft)
Humidity	Max. 90% RH (50°C)
Shock	Meets the requirements of the IEC68 Eb recommendations
Vibration	Meets the requirements of the IEC68F recommendations

Dimensions

Width	210 mm (8.25″)
Height	89 mm (3.5″)
Depth	325 mm (12.8″)

Weight Approx. 2.8 kg (6.2 lb)

III. ACCESSORIES

1. Standard accessories supplied with the instrument

1 mains cable

1 manual

1 1.6 A fuse ,fast action

1 "115 V" label

2. Accessories to be ordered separately

2.1. Oscillators

PM 9677 Standard oscillator

PM 9678 TCXO

PM 9679 Oven-enclosed oscillator 1×10^{-7}/month

PM 9690 Oven-enclosed oscillator 1.5×10^{-9}/24 h.

2.2. Output interface units

PM 9674 BCD output unit

PM 9675 D/A converter

2.3. Input interface accessories

PM 9351 Passive measuring probe 10 MΩ./11 pF 220 MHz, attenuation 10×

PM 9353 FET probe, 1MΩ/3.5F, 220 MHz

PM 9584 Resistive mixing piece, 50 Ω, 3 BNC sockets

PM 9346 Active-probe power supply

2.4. Coaxial cables

PM 9074 50 Ω, BNC to BNC,length1 m

PM 9588 Set of 50 Ω cables, BNC to BNC:
5 cables, length 20.7 cm
4 cables, length 40.5 cm
3 cables, length 60.3 cm
3 cables, length 198.6 cm

2.5. Mains cable

PM 9011 3-core detachable mains cable

2.6. 19″-rack mount adapter
PM 9669/01 for one counter
PM 9669/02 for two counters

2.7. Battery unit

PM 9673 Internal battery unit

2.8. Carrying case

PM 9672 Carrying case for the instrument

IV. INSTALLATION

1. Mains voltage conversion

The instrument can be converted into two mains voltage ranges 100—130 V and 200—260 V. The frequency range is 50 to 400 Hz. At delivery the instrument is set to the 200 to 260 V range.
When changing to the 100 to 130 V range the connections of the mains transformer should be changed as shown in figure IV-1, and the label "230 V" covered with the "115 V" label supplied.

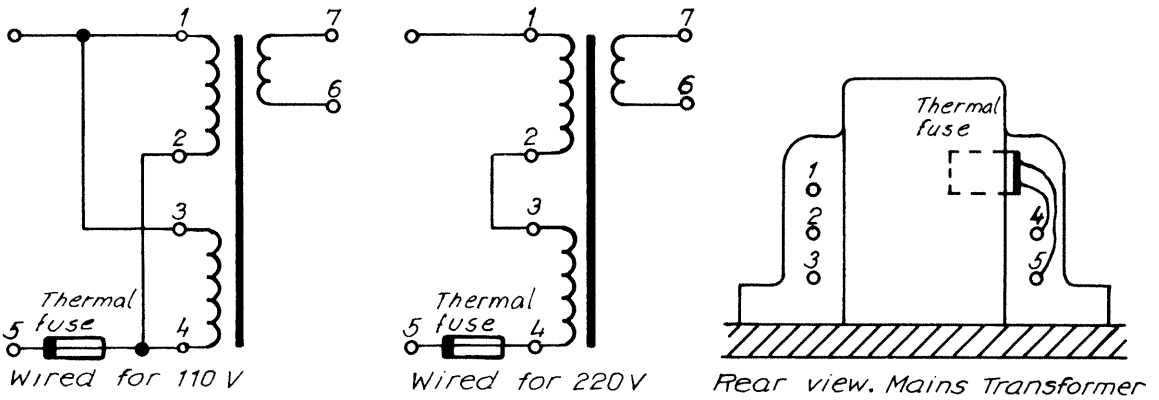


Figure IV-1. Mains transformer connections

2. Earthing

The local safety regulations prescribe how the instrument should be earthed. Two ways are possible:

1. Via the protective earth terminal at the rear panel.
2. Via the three core mains cable plugged into an outlet with protective earth contact.

NOTE: Use only **one** of these alternatives to avoid hum!

3. Fuses

A thermal fuse on the mains transformer and a 1.6 A fuse, fast action, on unit U1 are protecting the power supply. Figures VI-1 to VI-5 on pages 42 and 43.

4. Optional accessories

Refer to installation instruction given in manual for each type number.

V. CONTROLS, INDICATORS AND CONNECTORS

Figures VI-1 to VI-5 on pages 42 and 43

1 DISPLAY TIME

Sets display time between 0.2 and 5 s.
Infinite display time when knob is pulled.
With switch set to position STAND BY the counter is turned off except the oven oscillator.
WARNING: Primary voltage of power supply is on!

2 GATE

Lamp indicating that the main gate is open and that counting takes place. With DISPLAY TIME knob set to position STAND BY the GATE lamp is on permanently indicating that the oven oscillator is on.

3 SENSITIVITY

Sensitivity control for input A. When pushed, this control provides continuous setting of the sensitivity between approximately 4 V and 200 mV. With knob pulled the sensitivity can be set between 220 mV and 10 mV.

4 ⊓

When measuring signals at input A with duty factor > 0.75 this push-button must be depressed to obtain reliable triggering.

5 5—250 MHz, PM 6613
50—520 MHz, PM 6614
50 MHz—1 GHz, PM 6615

Turns on channel B when depressed.
Not present in PM 6611.

6 ⊔

When measuring signals at input A with duty factor < 0.25 this push-button must be depressed to obtain reliable triggering.

7 ~

When measuring signals at input A with duty factor 0.25—0.75 this push-button must be depressed to obtain reliable triggering.

7 10 CHECK

When depressed the instrument is set to self check mode.

8 B

Input B. Signal input for FREQUENCY or RATIO measurement. Frequency range:

PM 6613,	5	MHz	to 250	MHz
PM 6614,	50	MHz	to 520	MHz
PM 6615,	50	MHz	to 1	GHz

Not present in PM 6611.

9 A

Input A. Signal input for COUNT, FREQUENCY, PERIOD and RATIO measurement. Frequency range 10 Hz to 80 MHz.

10 < 100 kHz ~

Low-pass filter. When measuring noisy signals at input A with duty factor ≈ 0.5 and frequency < 100 kHz triggering is improved by depressing this push-button.

⓫ **Function selector**

COUNT A — Sets counter to add the pulses at input A in the time interval between depressing and releasing the START/STOP push-button.

FREQUENCY — Sets counter to measure frequency.
MHz and kHz are measuring units related to the display read-out.
100 Hz, 10 Hz, 1 Hz and 0.1 Hz is the resolution of the least significant digit.

PERIOD A — Sets counter to measure period at input A.
μs is the measuring unit related to the display read out. $n=1$, $n=10^2$ and $n=10^4$ indicates the number of periods being measured.

RATIO A/C and B/C — Sets counter to measure ratio between signals applied to inputs A and C or B and C.
$n=10^2$ and $n=10^4$ indicate the number of decimals displayed.

⓬ **MEMORY START/STOP** — In released position the measurement information is stored until next measurement cycle is completed.
Depressed button makes display follow decade counters continuously.
In COUNT A mode, start/stop operation.

⓭ **RESET** — Resets decade counter and display to zero.

Rear panel

⓮ Mains input.

⓯ **INT.BATT.OFF MAINS/EXT.BATT.** — Turns the internal battery off.
The mains or the external battery is the power source for the instrument.
Internal battery is charged when mains cable is connected.

⓯ **INT.BATT.ON** — Sets power supply to be fed from the internal battery. Turns the mains or the external battery off.

⓰ **INPUT C** — Input C. Signal input for external time base signal 1 kHz to 10 MHz and RATIO measurement.

⓱ **10 MHz OUT** — Output for the internal oscillator signal.

⓲ **BCD** — Input connector for BCD unit.

⓳ ⏚ — Chassis ground.

⓴ − — Minus-pole connection for external battery.

㉑ + — Plus-pole connection for external battery.

㉒ **INT.STD EXT.STD IN VIA C** — Sets counter to operate with either internal or external oscillator (earlier versions have an internal jumper).

㉓ — Connector for D/A converter and BCD unit.

VI. OPERATION

Figures VI-1 to VI-5 on pages 42 and 43

General Information

1. Switch on power

1.1. Mains

Before connecting the counter to the mains check that the mains transformer is wired for the local mains voltage. Refer to chapter IV, INSTALLATION.
Set switch MAINS EXT.BATT./INT.BATT.ON to position MAINS EXT.BATT. ⓯.
Connect mains cable to the counter at ⓮.
Turn DISPLAY TIME control ❶ to ON. Check that GATE lamp ❷ and display are on, indicating that power is on.

1.2. External battery

Set switch MAINS EXT. BATTERY/INT. BATT. ON ⓯ to position MAINS EXT.BATTERY.
Connect the cables from the external battery to sockets EXT.BATT. 12—24 V "+" ㉑ and "—" ⓴.
Check that GATE lamp ❷ and display are on, indicating that power is on.

1.3. Internal battery PM 9673

Set switch MAINS EXT. BATTERY/INT. BATTERY ON ⓯ to position INT.BATTERY ON.
Check that GATE lamp ❷ and display lights indicating that power is on. Blinking display indicates low voltages. Refer to manual PM 9673 for charging instructions.

2. Warm up time

The warm up time from the moment of mains connection is less than 7 minutes to an oscillator error of less than 10^{-7} for instrument equipped with the oven-enclosed oscillators PM 9679 or PM 9690. Instruments equipped with the oscillators PM 9677 or PM 9678 (TCXO) are ready for use at the moment of mains connection. Normally the instrument is switched on from the STAND BY ❶ position. If so, no warm up time is needed, irrespective of which oscillator is employed.

3. External frequency standards

House standards or other frequency standards can be used instead of the internal 10 MHz oscillator. If a time resolution of 100 ns is required, 10 MHz must be used.
When using 1 MHz instead of 10 MHz the decimal point must be shifted one step to the left to interpret the display correctly. To set the counter to external standard the internal jumper SK 131 ㉒, or SK 22 ㉒ at the rear panel, must be set to position EXT.STD.

Measurements

Figures VI-1 to VI-5 on pages 42 and 43

4. CHECK

1. Depress the two CHECK push-buttons ❼ ⓾.
2. Set DISPLAY TIME ❶ to mid-position
3. Rotate switch ⓫ and read display value as follows:

Function	Read (±1 digit)
FREQ 100 Hz	10.0000
FREQ 10 Hz	10.00000
FREQ 1 Hz	10000.000
FREQ 0.1 Hz	10000.0000
PERIOD n = 1	00000000.1
PERIOD n = 10^2	0.100
PERIOD n = 10^4	0.10000

4. Set switch ⓫ to position COUNT A.
5. Depress START/STOP push-button ⓬ : the counter will start totalizing the input pulses and the display will follow the counting continuously until push-button START/STOP ⓬ is released again.

5. FREQ. A

1. Set DISPLAY TIME ❶ to mid position.
2. Set function selector ⓫ to any of the four frequency positions that corresponds to the desired resolution of the measurement.
3. Connect the signal to be measured to input A ❾.
4. Match the input of the counter to the frequency and dutyfactor of the signal to be measured by depressing any of push-buttons ❹ ❻ ❼ ⓾.
5. Adjust SENSITIVITY control ❸ for stable display read-out.

6. FREQ. B (not present in PM 6611)

1. Set DISPLAY TIME ❶ to mid position.
2. Turn on channel B by depressing the push-button ❺.
3. Set function selector ⓫ to any of the four frequency positions that corresponds to the desired resolution of the measurement.
4. Connect the signal to be measured to input B ❽.

7. PERIOD A

1. Set function switch ⓫ to any of the three PERIOD A positions depending on the desired number of periods to be measured.
2. Match the input of the counter to the frequency and dutyfactor of the signal to be measured by depressing any of the push-buttons ❹ ❻ ❼ ⓾.

8. RATIO A/C*

1. Set function switch ⓫ to any of the two RATIO positions depending on the desired number of decimals of the display read-out.
2. Set DISPLAY TIME ❶ to mid position.
3. Connect the signal with the highest frequency to input A ❾.
4. Match the input of the counter to the frequency and duty factor of the signal to be measured by depressing any of the push-buttons ❹ ❻ ❼ ⓾.
5. Connect the signal with the lowest frequency to input C ⓰.
6. Adjust SENSITIVITY control ❸ for stable display read-out.

9. RATIO B/C* (not present in PM 6611)

1. Set function switch ⓫ to any of the two RATIO positions depending on the desired number of decimals of the display read-out.
2. Set DISPLAY TIME ❶ to mid-position.
3. Connect the signal with the highest frequency to input B ❽.
4. Turn on channel B by depressing the push-button ❺.
5. Connect the signal with the lowest frequency to input C ⓰.

10. TOTALIZE (COUNT A)

1. Set function switch ⓫ to position COUNT A.
2. Connect the signal to be measured to input A ❾.
3. Match the input of the counter to the frequency and duty factor of the signal to be measured by depressing any of the push-buttons ❹ ❻ ❼ ⓾.
4. Set DISPLAY TIME ❶ to mid position.
5. Depress START/STOP push-button ⓬.
6. When depressing the START/STOP push-button ⓬ the counter will start totalizing the input pulses until push-button START/STOP ⓬ is released again. The display will show the number of pulses counted in the time interval between depressing and releasing the START/STOP push-button ⓬.

* **NOTE**

Multiplier factors 10^5, 10^6, 10^7 and 10^8 are possible in the frequency mode by using input C as the external time base reference input. (set the internal jumper switch ㉒ or switch ㉒ at the rear panel to position EXT.STD.)
The decimal point is then incorrectly positioned.

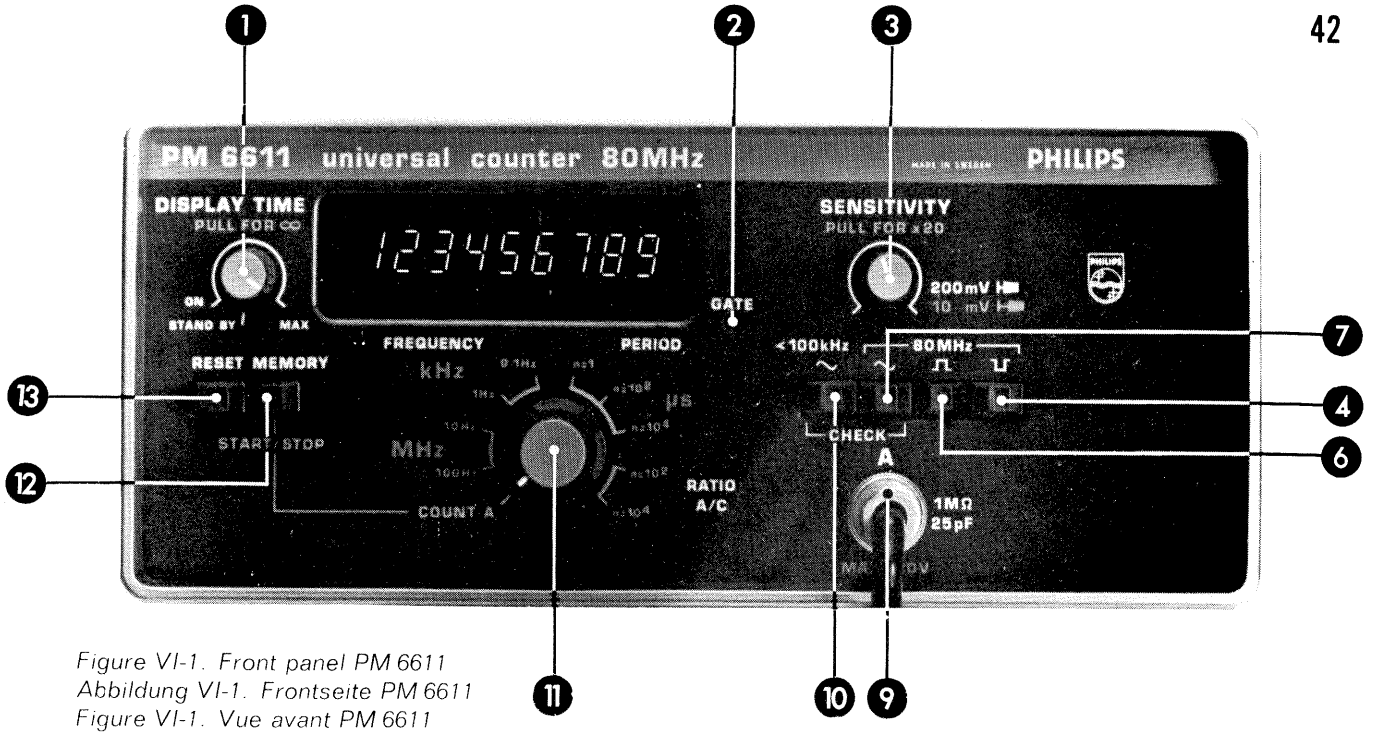


Figure VI-1. Front panel PM 6611
Abbildung VI-1. Frontseite PM 6611
Figure VI-1. Vue avant PM 6611

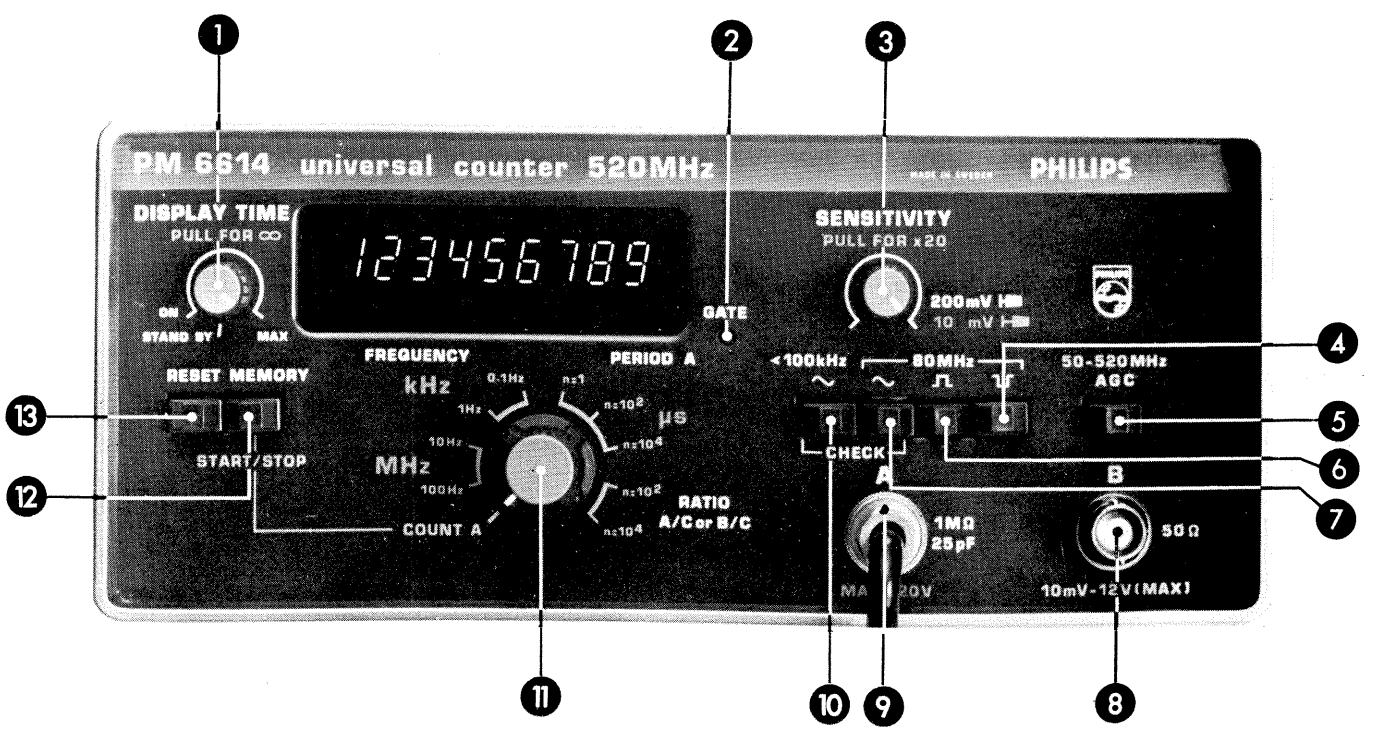


Figure VI-2. Front panel PM 6613, PM 6614 and PM 6615
Abbildung VI-2. Frontseite PM 6613, PM 3614 und PM 6615
Figure VI-2. Vue avant PM 6613, PM 6614 et PM 6615

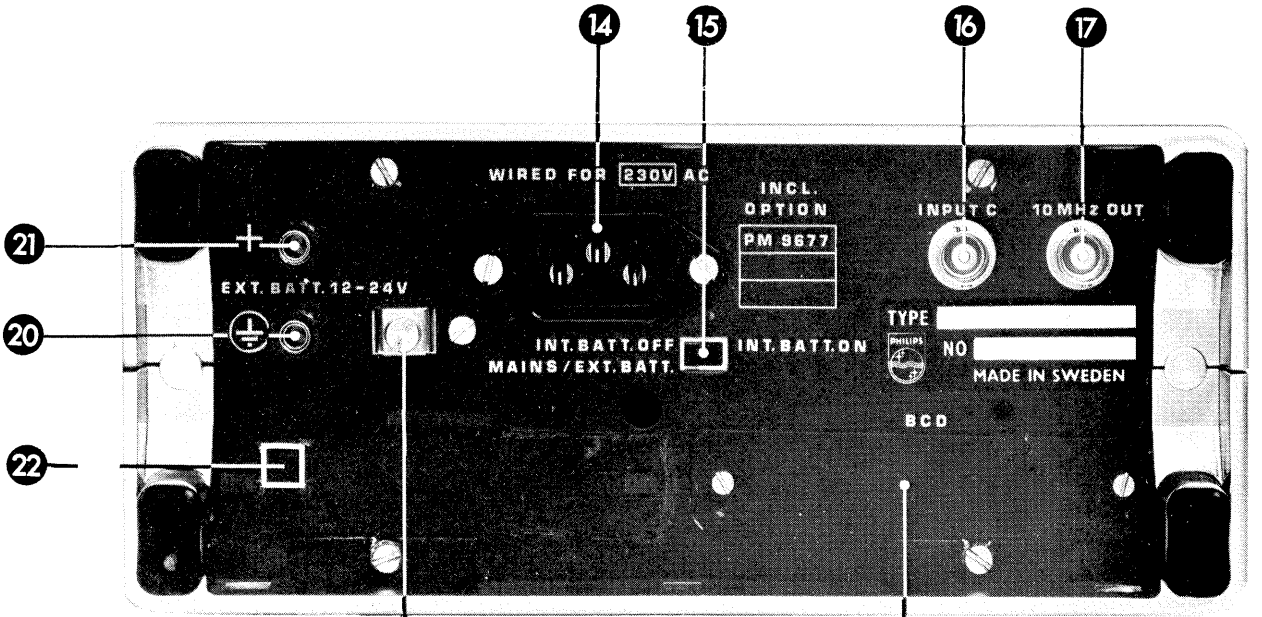


Figure VI-3. Rear panel
Abbildung VI-3. Rückseite
Figure VI-3. Vue arrière

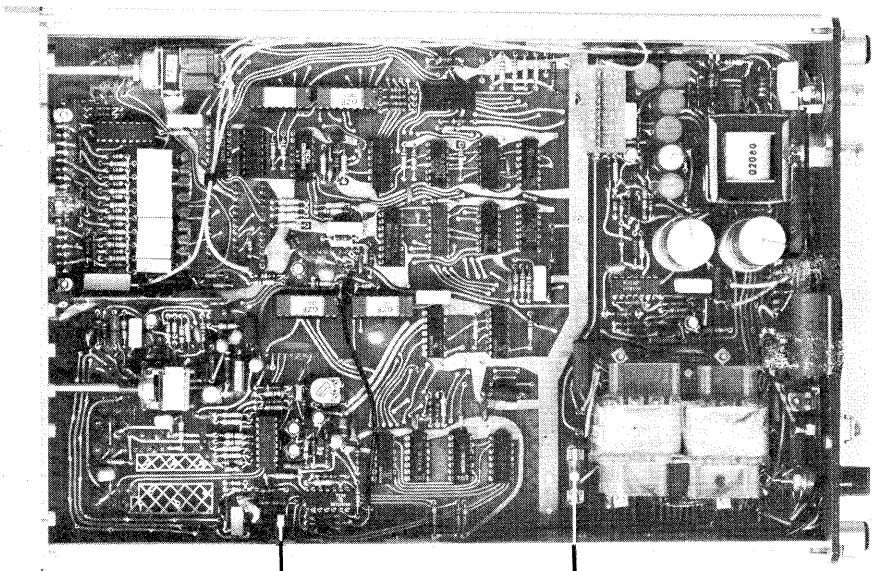


Figure VI-4. Top view
Abbildung VI-4. Ansicht von oben
Figure VI-4. Vue dessus

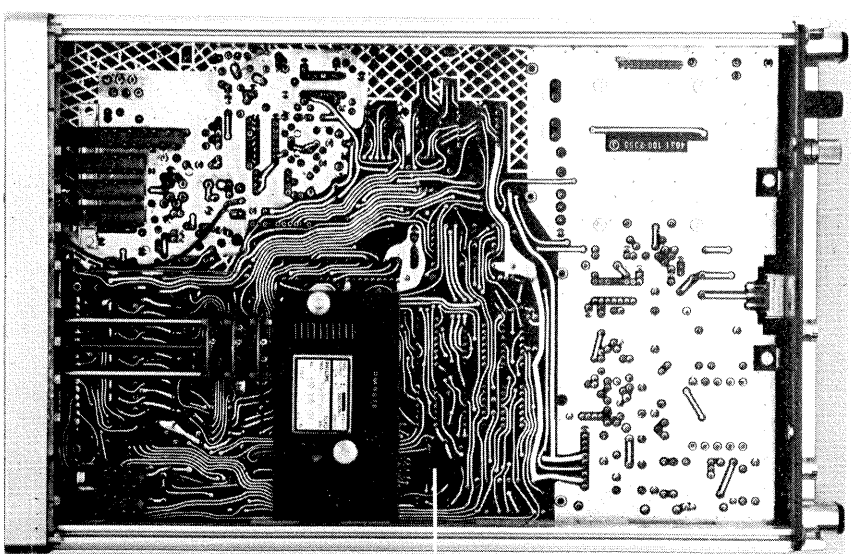


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VII. SURVEY OF CONNECTORS, SOCKETS, SWITCHES AND POTENTIOMETERS

BU 1	Input socket channel A
BU 2	Input socket channel B. Not present in PM 6611
BU 21	Input socket plus pole external battery
BU 22	Input socket minus pole external battery
BU 23	Mains input socket
BU 24	Input socket channel C
BU 25	10 MHz output socket
BU 26	Earth clamp
BU 102	Connects unit U2 to unit U1. Combined connector: male and female.. Not present in PM 6611
BU 103	Connects oscillator to unit U1. Male
BU 104	Jumper connector for d.c. voltages. Male
BU 105	Connector for internal battery. Male
BU 106	Connector for BCD and D/A converter. Female
BU 107	Connector for d.c. voltages. Female
BU 201	Connects unit U2 to unit U1. Female. Not present in PM 6611
SK 22	EXTERNAL/INTERNAL STANDARD switch
SK 101	DISPLAY TIME switch
SK 102	STAND BY switch
SK 103	RESET switch
SK 104	MEMORY and START/STOP switch
SK 105	FUNCTION selector switch
SK 106	SENSITIVITY switch
SK 107	LOW FREQUENCY FILTER switch
SK 108	SINE WAVE triggering switch
SK 109	POSITIVE PULSE triggering switch
SK 110	NEGATIVE PULSE triggering switch
SK 111	CHANNEL B switch. Not present in PM 6611
SK 121	INTERNAL BATTERY/MAINS OR EXTERNAL BATTERY switch
SK 131	Jumper connector for EXTERNAL/INTERNAL STANDARD (only present in earlier version of the instrument)
R 107	SENSITIVITY potentiometer
R 1157	DISPLAY TIME potentiometer

VIII. CIRCUIT DESCRIPTION

1. 80 MHz input amplifier

Refer to the circuit diagram fig. XIII-3.

The 80 MHz input amplifier is identical for all models PM 6611, PM 6613, PM 6614 and PM 6615. One only exception is switch SK 111 which is not present in PM 6611.

The measuring signal enters the amplifier at BNC socket INPUT A. The DC component of the signal is blocked by C 101. A two-position attenuator R 101, R 139, C 102, C 103 is controlled by switch SK 106. C 102 sets the frequency compensation.

Input protection is provided by R 102, C 104, R 103 and clipping diodes GR 101, 102, 103 and 106. Field-effect transistor TS 101 converts the input impedance together with emitter-follower TS 102 providing a low-ohmic output to the amplifier circuits. R 111, L 103 and C 132 form a 100 kHz low-pass filter which is operated with switch SK 107. R 107 sets the input sensitivity. When SK 107 is released, SK 108 has no function.

However, when both switches are depressed at the same time, the time base reference signal from IC 123:8 (see circuit diagram Time Base Dividers) is applied to the amplifier section via R 110, R 124, SK 107:3, 2 and SK 108:6, 5.

The next switch SK 111, which is not present in PM 6611, controls the prescaler unit U2 of PM 6613, PM 6614, or PM 6615. When SK 111 is released, the prescaler section is inoperative, because a LOW CLEAR level is provided from SK 111:4, via BU 102:6 and BU 201:6 to the D flip-flops of the prescaler. See the relevant circuit diagram of unit U2. Moreover, since SK 111:6 is open, a HIGH level is fed via BU 102:5 and BU 201:5 to the supply voltage control transistor in U2. The supply voltage of U2 is then interrupted.

When SK 111 is depressed, the signal path of the 80 MHz amplifier is shorted to earth via SK 111:2 and 3. The supply voltage of U2 is switched in and the CLEAR inputs of the prescaler D flip-flops go HIGH. See also the description of the Time Base Divider section.

Switches SK 110 and SK 109 are principally polarity shifters selecting the normal (12) or inverting (13) input of line receiver IC 101.

When the input signal is a sine wave or pulses with the duty factor 25 to 75 %, both SK 110 and SK 109 should be released. The signal path is then from SK 108 through SK 111, C 117, pins 5 and 4 of SK 110, and R 116 to the non-inverting input 12 of the first amplifier IC 101. The signal is available at both outputs 14 and 15.

When the input signal is a pulse train with a duty factor exceeding 75 %, switch SK 110 should be depressed. The signal now goes through pins 5 and 6 of SK 110 and via R 115 to the inverting input 13 of IC 101. The dc reference level is shifted outside the triggering window of the amplifier because pins 2 and 3 of SK 110 are connecting R 112 to earth.

SK 109 should be depressed when the input signal is a pulse train with duty factor below 25 %. Notice that SK 109 and SK 110 are interacting, so that SK 110 is automatically released when SK 109 is depressed. The signal path is now via C 117, pins 5 and 4 of SK 110, and R 116 to input 12 of IC 101. The only active function of SK 109 is to connect R 112 to earth to set the dc reference level of IC 101 outside the trigger window. Symmetrical feedback of the first amplifier stage IC 101 is provided by R 113 and R 114. At outputs 14 and 15, R 118 and R 119 are pull-down resistors for the emitter follower outputs.

The next amplifier stage of IC 101 with inputs 9 and 10 is not symmetrically fed back to prevent interference from Schmitt trigger TS 104, TS 103, from reaching the amplifier.

Input 10 also accepts the prescaled signal from unit U2 of PM 6613, PM 6614 or PM 6615. Variable resistor R 127 sets the d.c. balance of the amplifier.

Output 7 provides the signal for Schmitt trigger TS 104, TS 103. GR 110 ensures temperature stabilisation. TS 105 is interfacing the Schmitt trigger output to TTL level. Before the choke L 101 at the collector of TS 105, the signal A 1 is taken out to the DCU. L 101 is filtering frequencies above 10 MHz. Output signal A 2 is used as the time base signal in the PERIOD mode.

2. Unit U2, PM 6613

Refer to the circuit diagram fig. XIII-8.

Unit U2 contains the 250 MHz amplifier and prescaler circuits, and also two D flip-flops IC 201 dividing the time base signal generated on unit U1.

The signal to be measured enters the input amplifier at socket BU 2. After AC coupling capacitor C 201, a resistive atteuator network R 201 . . . R 204 is incorporated which maintains he VSWR of the input and also serves as a series impedance for the PIN diode attentuator GR 201 and GR 202. Schottky diodes GR 203 and GR 204 are clipping the signal but generate also current to the PIN diodes which provide automatically the proper attenuation of high-amplitude signals.

At low amplitude the signal passes this first PIN diode attenuator unchanged to the next PIN diode attenuator GR 205 . . . GR 207. Here the amplitude is reduced further before the signal is entering the input amplifier. The input amplifier consists of four cascade transistors TS 202 . . . TS 205. At the collector of TS 205, the signal is tapped off through C 212 and symmetrically detected by GR 209, 210. The detected negative and positive half-periods are fed to two operational amplifiers IC 202 and IC 203. IC 202 is the Automatic Gain Control amplifier connected as a Miller integrator. It is baised by a current supplied from the +12 V line through R 212, GR 209, GR 210 and R 215.

When the detected level is sufficient, IC 202 starts controlling the PIN diode attenuator GR 205 . . . GR 207. Transistor TS 201 ensures a linear attenuator response within the input signal range.

A special case is if the measuring signal level is very high at low frequencies so that TS 205 becomes saturated. This is detected by diodes GR 212, 213 which are biasing the AGC amplifier IC 202. The PIN

diode attenuator GR 205 . . . 207 then reduces the amplitude to a proper level. The detected signal from GR 209, 210 is also fed to operationel amplifier IC 203 performing a Schmitt trigger function. When no measuring signal is present or at a low detected level, output IC 203:6 is positive. TS 207 is then turned on, shorts the output line to earth, and turns off TS 206. When the detected signal from GR 209, 210 has reached a sufficient level, IC 203:6 goes LOW and TS 207 is turned off.
The measuring signal goes from TS 205 via C 219 and C 234 — R 226 to input 7 of divide-by-four circuit IC 204. The second input 6 is DC reference and diodes GR 214, GR 215 are limiters. The divided signal at IC 204:3 is fed via TS 206 to the output line BU 201:1 which is connected to BU 102:1 in the 80 MHz input amplifier. TS 208 is the supply voltage switch transistor described in section "80 MHz input amplifier". TS 208 also controls the —5.2 V switch TS 209. IC 201 contains the both D flip-flops providing the division by 4 of the time base signal as described in section "Time Base Dividers".

3. PM 6614, Unit U2

Refer to the circuit diagram fig. XIII-11.

The input conditioning section of the 520 MHz amplifier up to IC 201 and the AGC and Schmitt trigger circuits are principally the same as in the 250 MHz amplifier of PM 6613. Refer to the description.
After input conditioning, the measuring signal is applied to two cascade wide-band amplifiers IC 201 and IC 202. The signal level at IC 202 is detected by GR 209, GR 210 controlling the AGC amplifier IC 204 and Schmitt trigger IC 205.
Via R 213, C 213 and amplifier TS 203 the signal is fed to input 10 of divide-by-eight circuit IC 203. Output 1 provides the divided signal to the 80 MHz input omplifier, BU 102.
TS 202 is controlled by switch SK 111 (see the circuit diagram of 80 MHz input amplifier). When the switch is released, the level at BU 201:5, PRESCALER, goes HIGH which turns TS 202 off. Via R 230 and GR 211, also TS 205 is switched off. No supply voltage for the amplifier is present until switch SK 111 is depressed and BU 201:5 goes LOW.
The two D flip-flops of IC 206 and one D flip-flop of IC 207 provide the division by 8 of the time base frequency TB 1. Refer to the description of the Time Base Divider.

4. PM 6615, Unit U2

Refer to the circuit diagram fig. XIII-14.

The input conditioning section of the 1 GHz amplifier up to IC 201 and the AGC and Schmitt trigger circuits are principally the same as in the 250 MHz amplifier of PM 6613. Refer to that description.
After input conditioning, the measuring signal is applied to two cascade wide-band amplifiers IC 201 and IC 202. The signal level at IC 202:7 is detected by GR 209, GR 210 controlling the AGC amplifier IC 204 and Schmitt trigger IC 205.
Via R 213, C 213 and amplifier TS 203, the signal is fed to input 4 of divide-by-four circuit IC 203. The complementary outputs 10 and 11 of this circuit provide the signal to the next 4-divider IC 208 via zeners GR 214, GR 215. These diodes are interfacing the +1 V output of IC 203 with the —3 V input requirement of IC 208. The measuring signal frequencty, now divided by 16, is fed via TS 206 to the output line BU 201:1 which is connected with BU 102:1 to the 80 MHz input amplifier.
TS 202 is controlled by switch SK 111 (see the circuit diagram of the 80 MHz input amplifier). When the switch is released, the level at BU 201:5, PRESCALER, goes HIGH which turns TS 202 off. Via R 230 and GR 211 also TS 205 is switched off. No supply voltage for the amplifier is present until SK 111 is depressed and BU 201:5 goes LOW.
The four D flip-flops of IC 206 and IC 207 provide the division by 16 of the time base frequency TB 1. Refer to the description of the Time Base Divider.

5. Time base divider

5.1. General (see circuit diagram fig. XIII-4)

A dual line receiver IC 120 is used to transfer the internal or external time base reference signals to the time base divider section.
The line receiver consists of two identical stages, each with a differential amplifier converting the input signal into appropriate TTL level, and a NAND gate controlled by the INT/EXT switch and the Function switch SK 105.
In the FREQUENCY mode using the internal oscillator, the 10 MHz signal from BU 103:5 is fed to input 2 of IC 120. After amplification, the signal is fed to the NAND gate of IC 120 being enabled because the two control inputs 5 and 6 of the gate are HIGH. Any signal applied to INPUT C is blocked at the second NAND gate of IC 120 because control input IC 120:8 has a LOW state originating from NAND gate 1/4 IC 122:6. From output IC 120:4 the 10 MHz signal is applied to input 9 of NAND gate IC 123. The second input 10 of this gate is HIGH in the FREQ. mode. When an external time base is used or in the RATIO mode the signal applied to BU 24, INPUT C, is fed to terminal 11 of the line receiver IC 120.
The INT/EXT switch or the Function switch (RATIO) SK 105 inhibits the internal 10 MHz signal because control input IC 120:5 goes LOW. Simultaneously, gate IC 122:6 provides a HIGH state to input IC 120:8 which is enabling the NAND gate. The INPUT C signal can then pass through and via IC 120:9 reach input 10 of NAND IC 123.
Either the 10 MHz signal or the INPUT C signal will be fed from IC 123:8 to the 10 MHz OUT connector BU 25 and to input 4 of AND-NOR configuration ½ IC 121. In all modes except PERIOD mode, control inputs IC 121:5 is HIGH and IC 121:2 is LOW. This means that the measuring signal from the 80 MHz input, used as the time base signal in he PERIOD mode, is inhibited whereas the ordinary time base signal at IC 121:4 can pass through and enter the time base divider section. Via output IC 122:11 and R 134 the signal is fed to the time base dividers consisting of two LOCMOS quad decade counters IC 124 and IC 125. The function of these circuits is described under section 6. Decimal counting unit and Display.

The division factor is set with the Function switch SK 105 which controls the Decade Select inputs indicated M 0, M 1 and the Enable inputs as illustrated in the truth table below.

The divided signal corresponds to the D bit of the relevant decade counter and is available at terminal 18 of each circuit IC 124 or IC 125. Via transistor TS 120 it is fed to the AND-NOR gate configuration IC 121, input 13. The second input 1 is permanently HIGH except in the PERIOD n = 1 and COUNT A modes. In these modes input IC 121:10 is HIGH allowing the time base signal from IC 121:6 to pass through to IC 121:8.

Next, the time base signal is gated through NAND gate IC 123 to NOR gate IC 126:2. The signal is also taken out via BU 102:3 indicated TB 1 to the B input amplifier U2 of either PM 6613, PM 6614 or PM 6615. After prescaling, the time base signal is fed back as TB 2 to BU 102:2 and is applied to IC 126:9. When input B is used, this signal is gated through IC 126 to control the Main Gate flip-flop. This is achieved when switch SK 111 in the 80 MHz input amplifier is depressed which generates a disabling "1" at IC 126:3. Then the normal time base signal can not pass through until after prescaling when it is applied to IC 126:8, 9. In PM 6611, which has no B input amplifier, a pull-up resistor R 1131 is included at IC 126:8, 9.

The time base signal, normal or prescaled, is applied to clock input 3 of the Main Gate flip-flop IC 183, which is controlling the main gate via complementary Q output 6. The Q output 5 controls the Gate indicator LED GR 189 via monostable multivibrator IC 182 and transistor TS 170. The second flip-flop of IC 183 is clocked at terminal 11 by the Main Gate flip-flop and is used as the Display Time flip-flop.

MODE		ENABLE IC 124	ENABLE IC 125	DECADE SELECT INPUTS		SELECT DECADE OF	
				M 0	M 1	IC 124	IC 125
COUNT A		L	H	H	L		D 2
FREQ. A	100 Hz	L	H	L	L		D 1
	10 Hz	L	H	H	L		D 2
	1 Hz	L	H	L	H		D 3
	0.1 Hz	L	H	H	H		D 4
PERIOD A	n = 1	L	H	H	H		D 4
	$n = 10^2$	H	L	H	L	D 2	
	$n = 10^4$	H	L	H	H	D 4	
RATIO	$n = 10^2$	H	L	H	L	D 2	
	$n = 10^4$	H	L	H	L	D 4	

H = HIGH level, L = LOW level.

5.2. Synchronized preset

Refer to the simplified diagram fig. VIII-1.
During the display time interval, the time base dividers are preset to 9999. When the display time interval is ended and the RESET signal goes HIGH, the next clock pulse will trigger the decade counters of the time base dividers. Randomly, the display time interval may end during a clock pulse which might imply uncertain triggering of the dividers. To prevent this, the preset function is synchronized to the leading edge of he clock pulse.
The circuit achieving this consists of NAND gates IC 123 forming a latch configuration and NAND gate IC 122 with output terminal 3. The CLOCK signal applied to IC 122:12, 13 is also fed to IC 123:12. The RESET signal is applied to inputs IC 123:5 and IC 122:2. This means that the latch is controlled by the RESET signal. For example, when the RESET signal is LOW, output IC 122:3 providing the PRESET signal to IC 124:12 is HIGH, independent of the state of the CLOCK signal.

However, output IC 122:3 PRESET, goes LOW only when both inputs 1 and 2 go HIGH. This means, that when RESET goes HIGH during the time the CLOCK signal is also HIGH, input IC 122:1 is still LOW and the PRESET signal at IC 122:3 HIGH. But when the CLOCK signal goes LOW, the PRESET signal will be LOW.

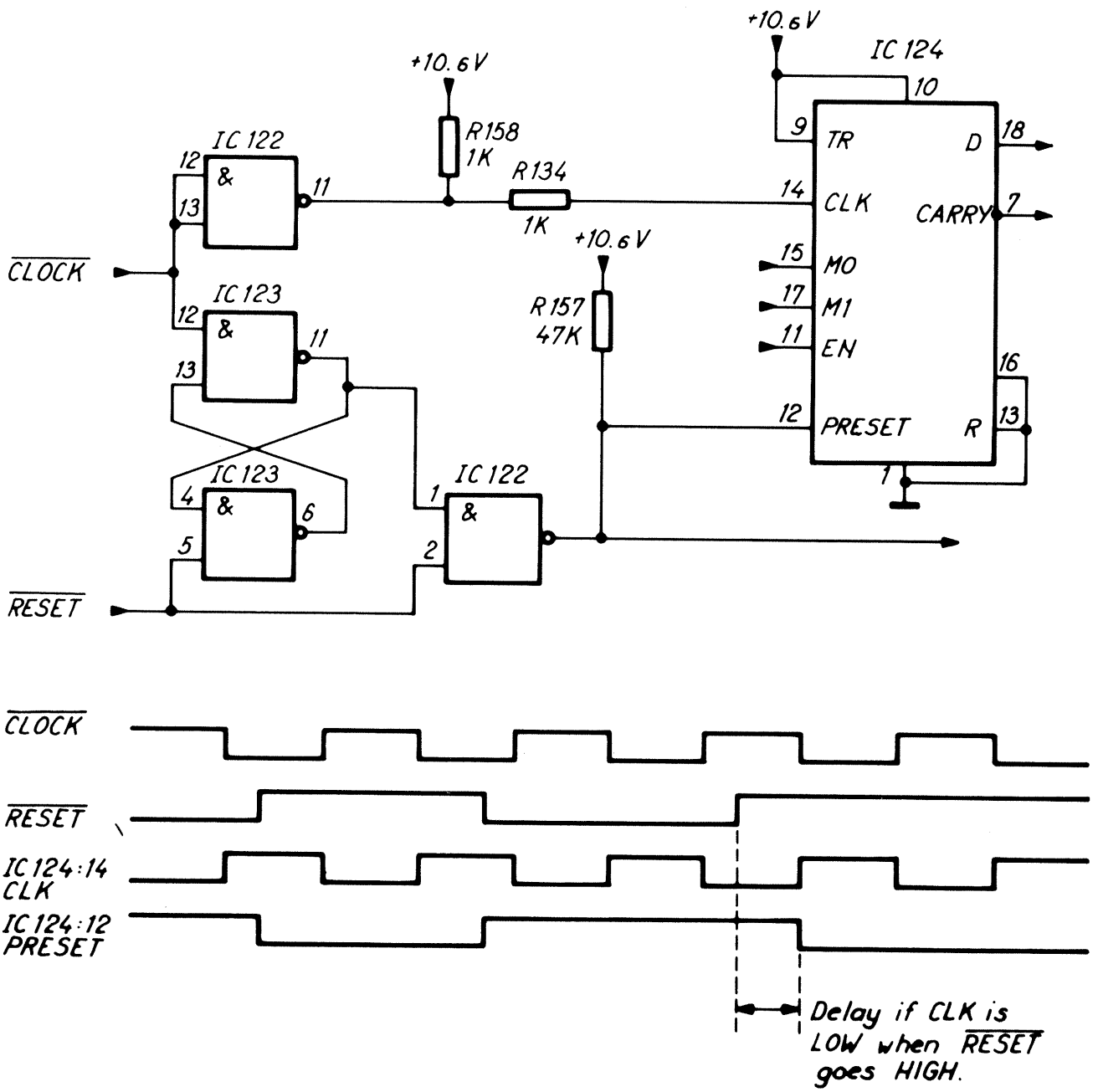


Fig. VIII-1. Preset sync circuit

5.3. Main gate and display time control

IC 183 is a dual D-flip-flop, containing the Main Gate FF and the Display FF. Both flip-flops are triggered by the positive going edge of their clock signal.
In all operating modes except COUNT A, a time base signal is applied to the clock input 3 of the Main Gate FF. The complementary output $\overline{Q}$, pin 6, is connected to the main gate in the DCU section. The main gate is closed when $\overline{Q}$ is HIGH, but will open when $\overline{Q}$ goes LOW.
Assume that $\overline{Q}$, pin 6, is HIGH. Then the D input pin 2 is also HIGH. At the next positive-going edge of the time base signal, output $\overline{Q}$ goes LOW and the main gate opens, i.e. the counting interval starts. The second output IC 183:5, Q, controls the Gate LED Multivibrator via input 13 of NOR gate IC 182. This monostable multivibrator controls the Gate LED GR 189 via TS 170. The LED can also be turned on by the front panel DISPLAY TIME switch when set to the STAND BY position. The monostable multivibrator is stretching the pulse at the shortest gate time settings so that the blinking of the LED becomes visible.
At the next positive-going edge of the clock signal at IC 183:3, the Main Gate flip-flop switches over, the complementary output IC 183:6 goes HIGH and the main gate is closed.
At this moment the display time interval starts. During this interval a TRANSFER pulse should be generated to the decade counters in the decimal counting unit, and a RESET pulse should be generated before the next counting interval starts.
The timing diagram fig. VIII-2 shows the sequence of these events. The Display Time flip-flop IC 183 is triggered by the positive-going edge of the MAIN-GATE signal from IC 183:6. Output IC 183:9 goes HIGH and provides a LOW CLEAR pulse to the Main Gate flip-flop input 1 via NOR gate IC 184:10. The output state of the Main Gate flip-flop is then maintained. The complementary output IC 183:8 of the Display Time flip-flop is LOW which normally would have set NOR gate output IC 185:10 to a HIGH level, causing the generation of a TRANSFER pulse via C 173 and R 1156. However, an INHIBIT LOW signal is assumed to be applied (e.g. from an automatic measuring system) via BU 106:5. Via IC 185:2 and 9, output 10 is latched to a LOW level until the INHIBIT signal goes HIGH. Then IC 185:10 goes HIGH and is latched to this state by the feed-back to input 3 eliminating the influence of another INHIBIT LOW signal that may appear. The positive-going edge is differentiated by C 173—R 1156, and a TRANSFER pulse is generated and fed to the DCU via IC 184:6. The positive-going edge from IC 185:10 is also fed to the Display Time multivibrator input IC 182:6 via R 1156. Capacitator C 172 starts charging and at the threshold level of IC 182:6, the multivibrator is triggered. Output IC 177:10 generates a sloping pulse which is converted to a proper RESET pulse at NOR gate output IC 178:13. Inverter IC 178:1 provides the RESET pulse to the DCU.

The RESET pulse is resetting the Time Base Dividers IC 124 and IC 125 via NAND gate IC 122, output 3. The Display Time flip-flop IC 183 is cleared by the RESET pulse at input 13, i.e. output IC 183:9 goes LOW. When the RESET pulse ends, the time base dividers generate clock pulses for the Main Gate flip-flop and the cycle is repeated. However, as illustrated in the second sequence of the timing diagram fig. VIII-2, the TRANSFER pulse appears immediately when the main gate is closing.

A third alternative occurs when the MEMORY push-button switch SK 104 is depressed, i.e. the memory is switched off. Then the main gate flip-flop output IC 183:6 is directly connected via pins 3 and 2 of SK 104 to input 5 of NAND gate IC 184. The TRANSFER pulse will then coincide with the main gate pulse plus the additional short pulse at the beginning of display time interval. Manual RESET is generated by push-button SK 103. Latch configuration IC 184:3 and 11 prevents contact bounce interference.

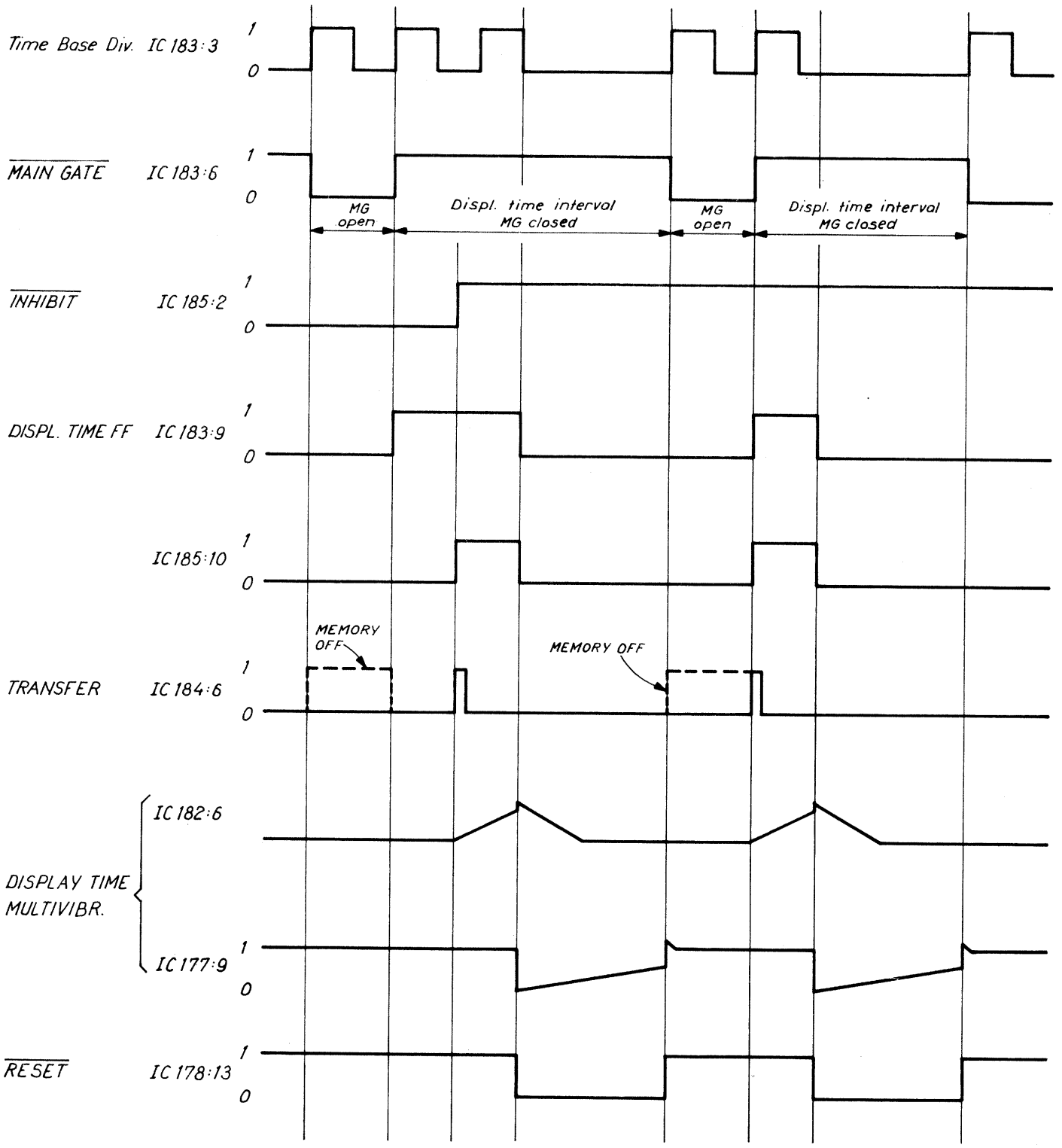


Fig. VIII-2. Timing diagram, main gate and display time control

6. Decimal counting unit—DCU—and display unit

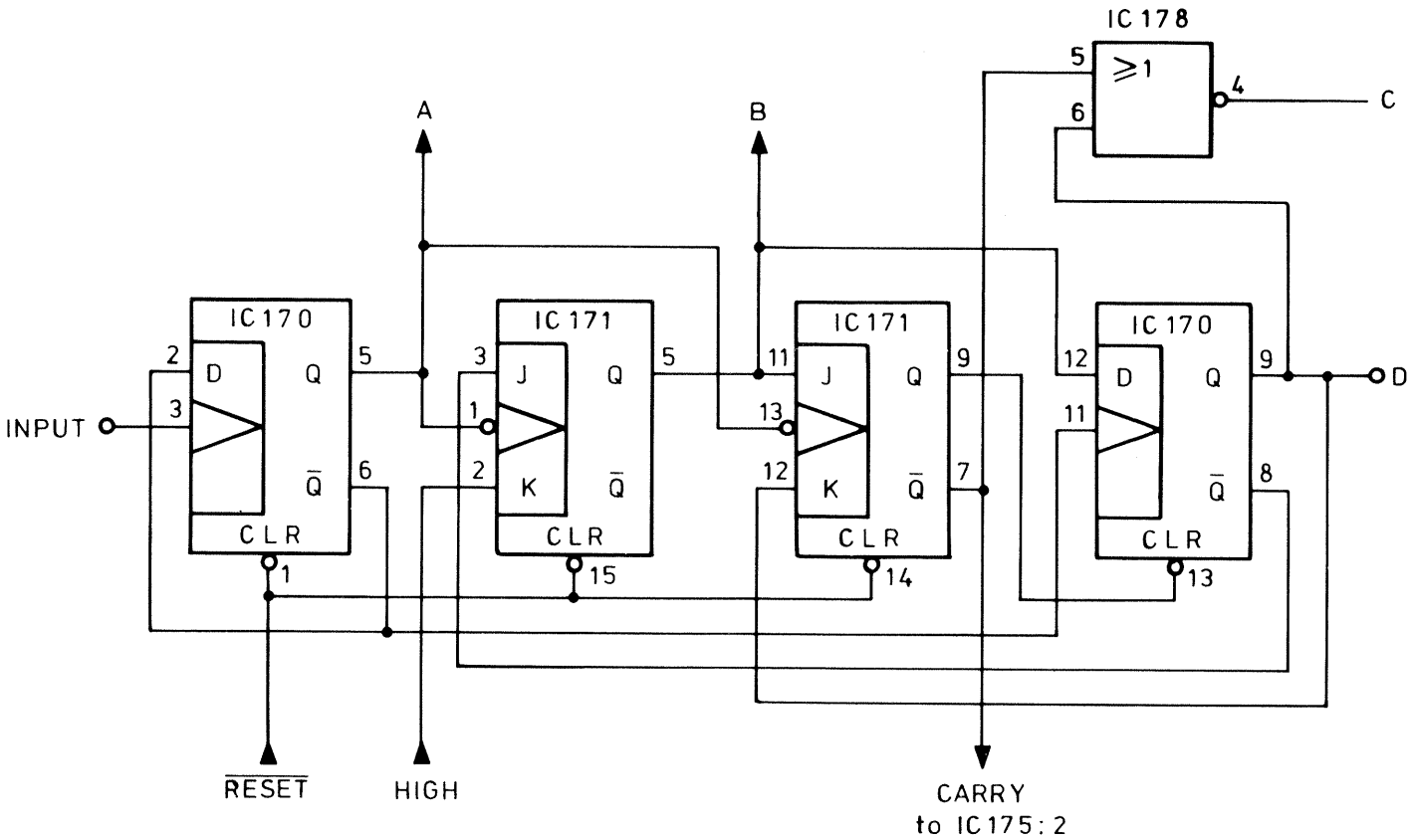
6.1. General

Refer to the circuit diagram fig. XIII-5.
The DCU consists of an 80 MHz decade IC 170, IC 171 for the least significant digit and two LOCMOS circuits IC 175, IC 176 each containing four complete decades. An address counter IC 179 generates the ENABLE signals for the 80 MHz decade the quad decades IC 175, IC 176 and also the scanning pulse sequence for the display via a BCD to 1 of 10 decoder IC 180.
The four-line BCD code provided by the decades is applied to the display via a BCD to 7 segment decoder IC 181. The outputs of this circuit are connected each to one segment of the 9 parallel connected digits including the decimal point.

6.2. 80 MHz decade

Refer to the circuit diagram fig. XIII-5 and the timing diagram fig. VIII-3.
2 D-type flip-flops IC 170, two edge-triggered JK flip-flops and a decoder NOR gate IC 178 form the 80 MHz decade. The input signal comes from the main gate IC 172 and triggers the first D flip-flop IC 170 which generates the A bit of the four-line BCD code. Next, the flip-flop IC 171 generates the B bit. When triggered by the negative edge of the A signal and the JK inputs are HIGH, i.e. when the complementary D bit at input J is HIGH. The K input is permanently HIGH.
The third flip-flop in the row, also a JK IC 171, produces the CARRY signal when triggered by the negative edge of the A pulse and the output of this flip-flop changes according to the state of the JK inputs at the time of triggering.
The fourth flip-flop, a D-type IC 170, produce the D bit at IC 170:9 when triggered by the complementary A bit assuming the B bit applied to the Data input IC 170:12 is HIGH.

Both the CARRY and D signals are applied to NOR gate decoder 1/4 IC 178 which generates the C bit as indicated in the timing diagram fig. VIII-3.
The four-line BCD information from the 80 MHz decade is then stored in the latch flip-flop IC 173. When the gate time ends, a TRANSFER pulse enables the latch which supplies the BCD data to the NAND gate network IC 174. These gates are inhibited until the ENABLE signal — D = HIGH — arrives from the address counter IC 179. When enabled, the BCD information are transferred via the data bus line to the BCD to 7 segment decoder IC 181. Refer to the timing diagram fig. VIII-4.



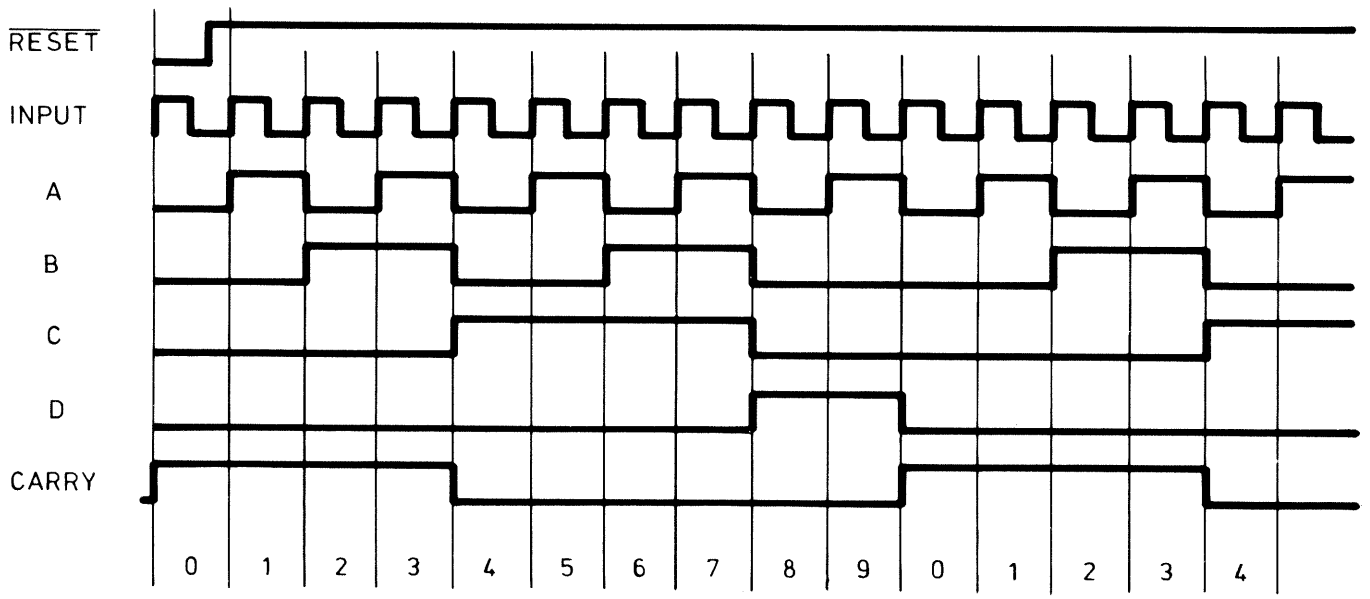


Fig. VIII-3. 80 MHz decade circuit and timing diagram

6.3. LOCMOS quad decades IC 175, IC 176

The CARRY signal from the 80 MHz decade is also used to clock the first decade counter of the LOCMOS circuit IC 175. This decade is referred to as D1 in the timing diagram fig. VIII-4.
DO indicates the 80 MHz decade just described. Each of the four decades contained in the LOCMOS circuit IC 175 or IC 176 functions principally as the 80 MHz decade. However, a brief look at the block diagram fig. VIII-5 will help understanding the special features. The PRESET input is permanently LOW and inactive because it is connected to—2.1 V. The CLOCK signal enters at input 14 and triggers the decades whose outputs are stored in the corresponding latches. When the TRANSFER pulse arrives, the information is fed to the multiplexer. Depending on the states of the Digit Select Inputs M0, M1, M2, the data of one of the decades is transferred to the BCD outputs provided the ENABLE input is HIGH. The truth table in figure VIII-5 indicates the relevant input states. Inputs M0 and M1 are addressed with BCD bits A and B respectively from the Address Counter IC 179. Input M2 is connected to—2.1 V and thus permanently LOW. The ENABLE signal to the first quad decade IC 175 is generated by NOR gate 1/4 IC 182 whose inputs are the C and D bits of the Address Counter IC 179. Thus, when both C and D are LOW as indicated in the timing diagram fig. VIII-4 the ENABLE signal to IC 175 goes HIGH. Assuming that both A and B of the Address Counter are LOW, decade D1 will provide its information to the BCD output and further to the BCD to 7-segment decoder IC 181. In the example given in the timing diagram fig. VIII-4 the digit next to the LSD will display a "2".
The next address from IC 179 will be A = HIGH, which means that the data of decade D2 is transferred to the BCD outputs and digit "0" is displayed. The sequence goes on until decade D4 has been selected. Then the ENABLE signal of IC 175 goes LOW because the C bit of the Address Counter goes HIGH. Instead, the ENABLE signal for quad decade IC 176 goes HIGH. Now the sequence starts again with the Digit Select Inputs M0, M1, M2 all being LOW thus selecting decade D5. Finally, decade D8 is selected corresponding to the Most Significant Digit, MSD.

6.4. Blanking

As indicated in the timing diagram fig. VIII-4, the output signals from the BCD to 7-segment decoder IC 181 contain blanking pulses between each digit information. The blanking is necessary to prevent unwanted glowing of unactivated segments of the display digit, and also to avoid the so-called streamers, which are glowings appearing between adjacent digits. In instruments with serial prefix 1, the blanking pulses are fed to the BCD to 7-segment decoder IC 181 only. From serial prefix 2, the blanking pulses are also applied to the anodes of the display B 101 via transistors TS 180 . . . TS 188.
The timing diagram fig. VIII-6 indicates how the blinking pulses are generated.
The pulses of the display multivibrator 2/6 IC 177 terminal 15 are fed to differentiating network R 191—C 140 via R 190 to the base of transistor TS 139. Its collector is connected to the blanking input 1 of IC 181 and, in instruments with serial prefix 2, via R 189 to the emitters of display driving transistors TS 180 . . . TS 188.
When the pulse on the base of TS 139 is positive the transistor will be turned off and the programmed current in the cathode driver will be zero.

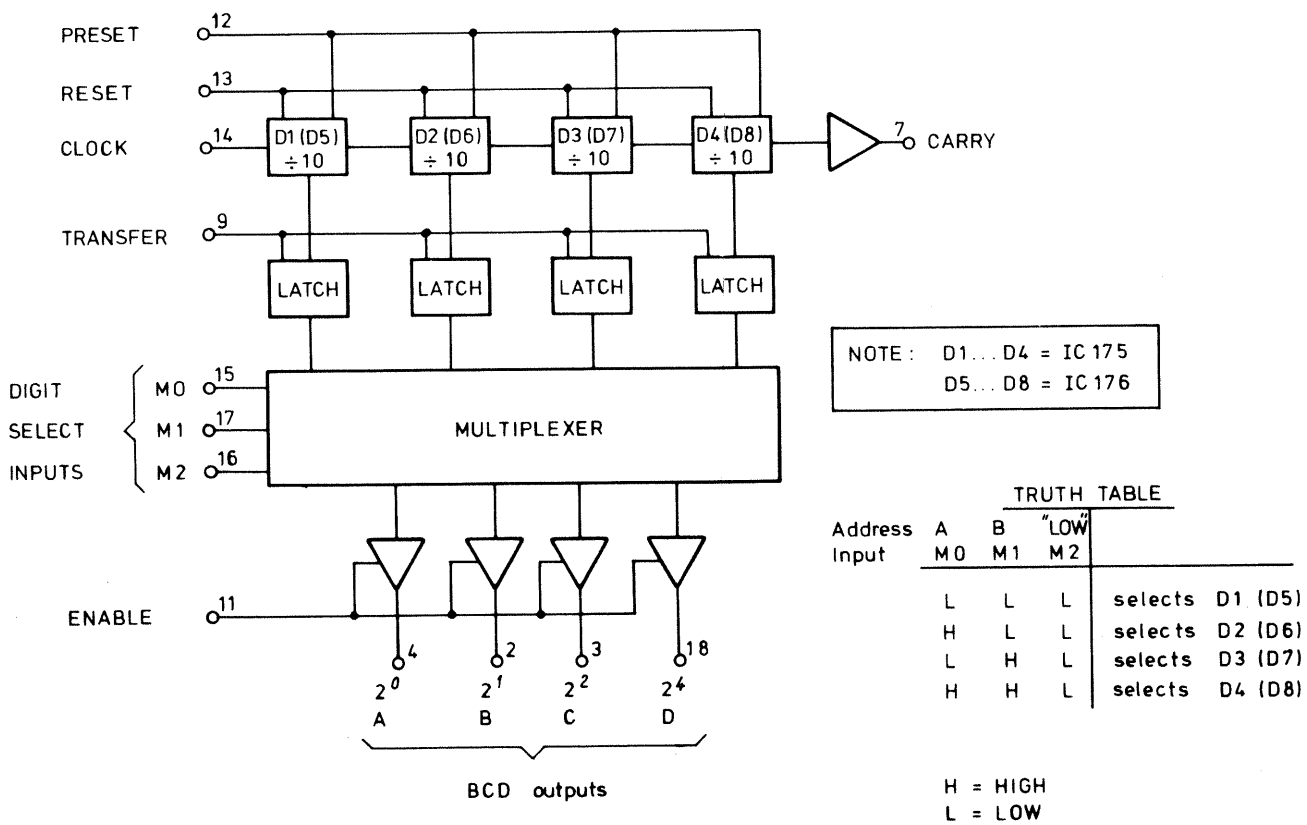


Fig. VIII-5. Block diagram of LOCMOS quad decade

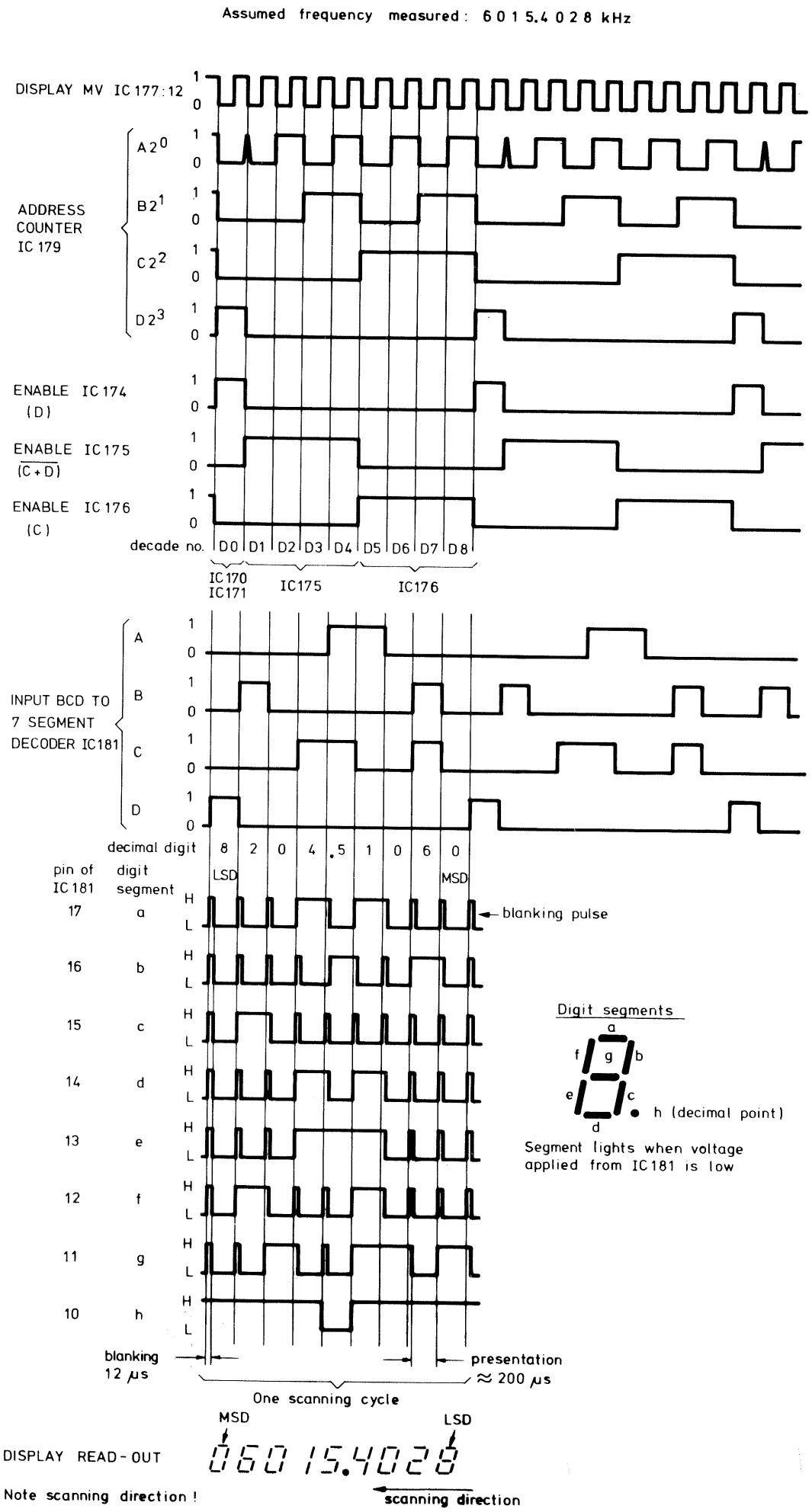


Fig. VIII-4. Timing diagram of display presentation

6.5. *Display scanning*

The display is scanned from the least significant digit —LSD— to the most significant digit—MSD. Only one digit lights at a time.
The pulse sequence controlling the driver transistors for the display digits is obtained from a BCD to 1 of 10 decoder IC 180 supplied with the four-line BCD information generated by the address counter IC 179. The timing diagram fig. VIII-6 illustrates how the digits are scanned. When output terminal 10 of the decoder IC 180 goes LOW, transistor TS 188 turns on and current can flow to the enabled segments of the least significant digit. Capacitor C 188 is connected between —50 V and +120 V and is changed to about 170 V which is sufficient to initiate a discharge of the segments of the display digit. The digit is presented during about 200 μs. At the next address from IC 179, output IC 180:10 goes HIGH again and output IC 180:1 goes LOW which is activating the next digit via TS 187. In the meantime, however, a 12 μs blanking pulse is generated by TS 139 which turns off all digits before the next digit segments are activated.
The scanning of the digits goes on until the most significant digit is turned on. Then the cycle starts all over again.

6.6. *Decimal point setting*

The Function Selector SK 105, controls the decimal point positioning in the display.
The decimal point input DP of the BCD to 7-segment decoder IC 181 is connected to pin 3 of SK 105 wafer 1. As indicated in the table in the circuit diagram fig. XIII-5 pin 3 will be connected to various outputs of the BCD to 1 of 10 decoder IC 180, except in mode COUNT A in which no decimal point is displayed. In mode FREQUENCY A and resolution 100 Hz, pins 3 and 4 are interconnected. When the "enable" pulse for digit number 4 arrives at output 4 of IC 180, it is also fed to the DP input of IC 181. A "decimal point pulse" is then fed from IC 181:10 to the decimal point 4 in the display.

7. Power supply

7.1. *General*

Refer to circuit diagram fig. XIII-6.

The power supply operates from 115 V AC or 230 V AC 50 to 400 Hz *or* from the internal battery PM 9673 *or* from an external battery with an output voltage of 12 to 28 V. It provides five stabilised and overload-protected voltages of +120 V, +12 V, +5 V, —5 V and —50 V.
The power supply may be divided into the *power input circuit* mainly consisting of the mains transformer T 101 and rectifier GR 167, the *over-voltage protection circuit* mainly consisting of thyristors TS 150, TS 151 and zener diode GR 160, the *voltage regulation circuit* mainly consisting of voltage regulator IC 150, thyristor TS 154, the*DC-to-DC converter* mainly consisting of primary side of transformer T 102, driver TS 152 and switch TS 153.

7.2. *Power input circuit*

When the power supply operates from the *mains*, the 115 V AC or 230 V AC is transformed to 20 V AC by transformer T 101, rectified in the diode-bridge GR 167, filtered by C 152 and C 161 and fed to the power supply circuits via switch SK 121 and SK 102.
When the power supply operates from an *external battery* the current to the power supply circuits is fed from BU 21 at the rear panel via protecting diode GR 164 and switches SK 121 and SK 102.
When the internal battery is used the current is fed from pin 8 of BU 105 via SK 121 and SK 102 to the power supply circuits.

7.3. *Over-voltage protection*

The over-voltage protection circuit consists mainly of thyristors TS 150, TS 151 and zener diode GR 160.
The anode of GR 160 is connected to the +5 V output from the power supply. If this voltage increases to 5.6 V . . . 5.8 V, the zener diode GR 160 will start to conduct and a current will flow through resistor R 1121. The voltage drop across R 1121 is fed to the gate of thyristor TS 151 via resistor R 1120. The anode is connected to the +5 V output voltage via resistor R 1118.
The thyristor will switch on and a voltage drop arises across resistor R 1122. This voltage is fed to the gate of thyristor TS 150, whose anode is connected to the d.c. input voltage. The thyristor will switch on and blow fuse VL 150, or, if the counter is operating in the internal battery mode, fuse VL 1 in the battery unit PM 9673. The capacitor across the gate and cathode of thyristor TS 151 prevents transients from the mains to blow fuse VL 150 accidentally.

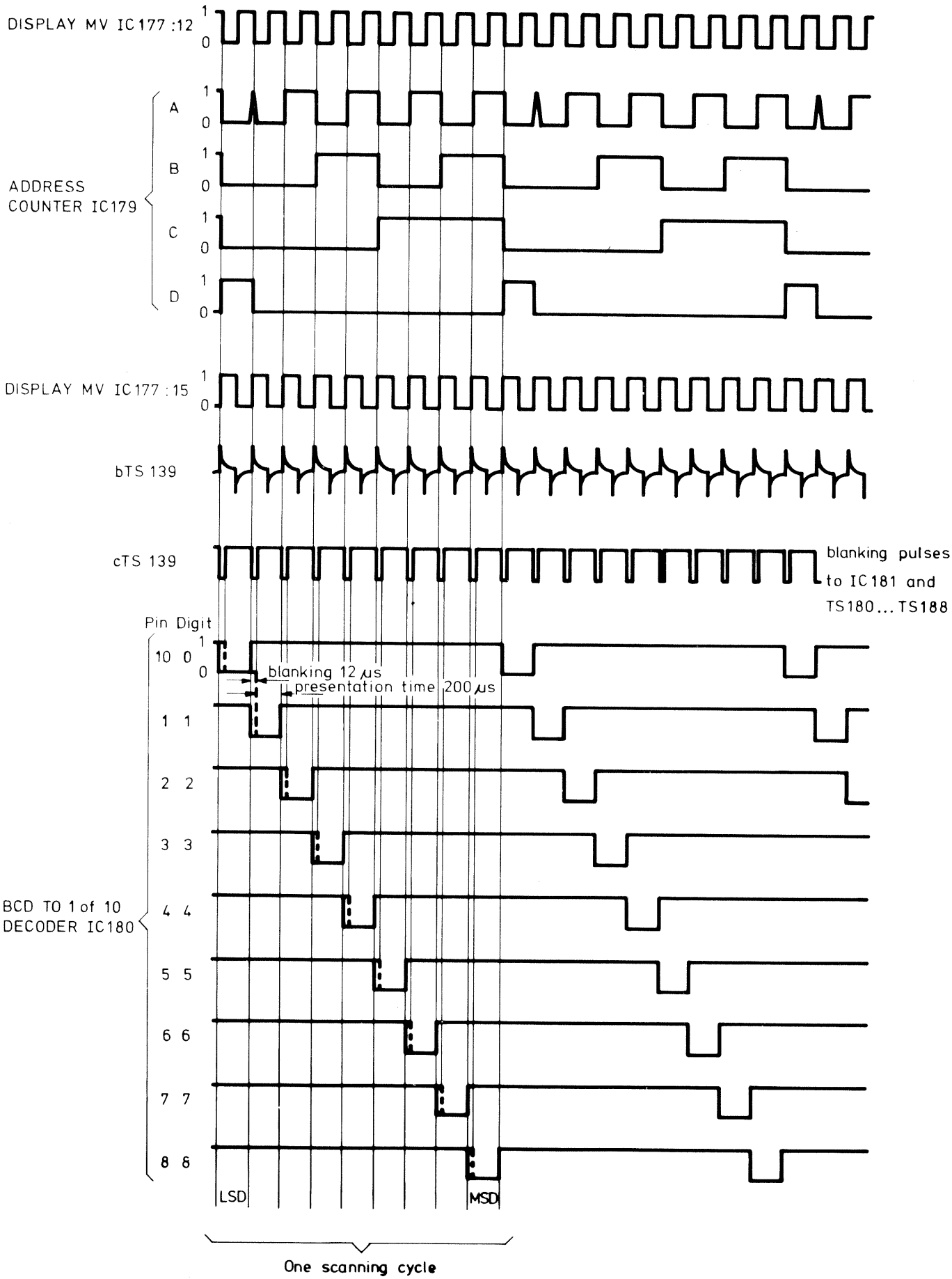


Fig. VIII-6. Timing diagram of display scanning principle and blanking pulse generation

7.4. DC toDC converter

Refer to diagrams fig. VIII-7.

The DC to DC converter is basically a blocking oscillator consisting mainly of switch transistor TS 153 and terminals 4—9 of the transformer T 102. When switch SK 102 is set to position ON, the DC voltage from the *power input circuit* is fed to the transistor TS 155 which works as a constant current source of approximately 1 mA (I_1).
The current I_1 will cause switch transistor TS 153 to start conducting and the linearly increasing current I_2 to flow.
This current I_2 will cause a voltage across terminals 3—8 of the transformer and the current I_3 will start to flow.
This will cause drive transistor TS 152 to saturate switch transistor TS 153. When the transistor no longer can saturate, current I_3 will stop to increase and the induced voltage at terminal 3 of transformer T 102 will disappear.
This will cause TS 153 to switch off and the collector voltage to rise to the same level as the supply voltage. At this moment the magnetic flux will discharge through the secondary windings of T 102 and diodes GR 155—159.

7.5. Output voltage regulation circuit

The output voltage regulation circuit consists mainly of voltage regulator IC 150 and thyristor TS 154.
The purpose of the thyristor TS 154 is to switch off the drive transistor TS 152 in order to regulate the output voltage. The switching moment of thyristor TS 154 is determined by a voltage at the gate of the thyristor which is the sum of a DC regulation voltage from terminal 10 of IC 150 and a sawtooth voltage caused by the emitter current of TS 153 through resistor R 1114//R 1115.
The voltage regulator IC 150 is fed at terminal 12 with the supply voltage and at terminal 7 with a negative voltage, via GR 161, from winding 3—8 of transformer T 102.
IC 150 contains a differential amplifier with inputs at terminals 4 and 5.
The input at terminal 5 is grounded via R 1104 and the input at terminal 4 is connected to a voltage divider that consists of the reference output at terminal 6 and the negative voltage from winding 3—8 of transformer T 102 at terminal 7.
The differential amplifier is in balance when the voltage at terminal 7 is —5 V. When the supply voltage across windings 4—9 of transformer T 102 increases, the voltage at the differential amplifier at terminal 7 of IC 150 will go more negative, the DC regulation voltage at terminal 10 of IC 150 will go positive and turn on thyristor TS 154. This will connect the base of driver transistor to the ground and cause switch transistor TS 153 to switch off. The stored magnetic flux will then discharge in the secondary windings of T 102 and diodes GR 155—GR 159.

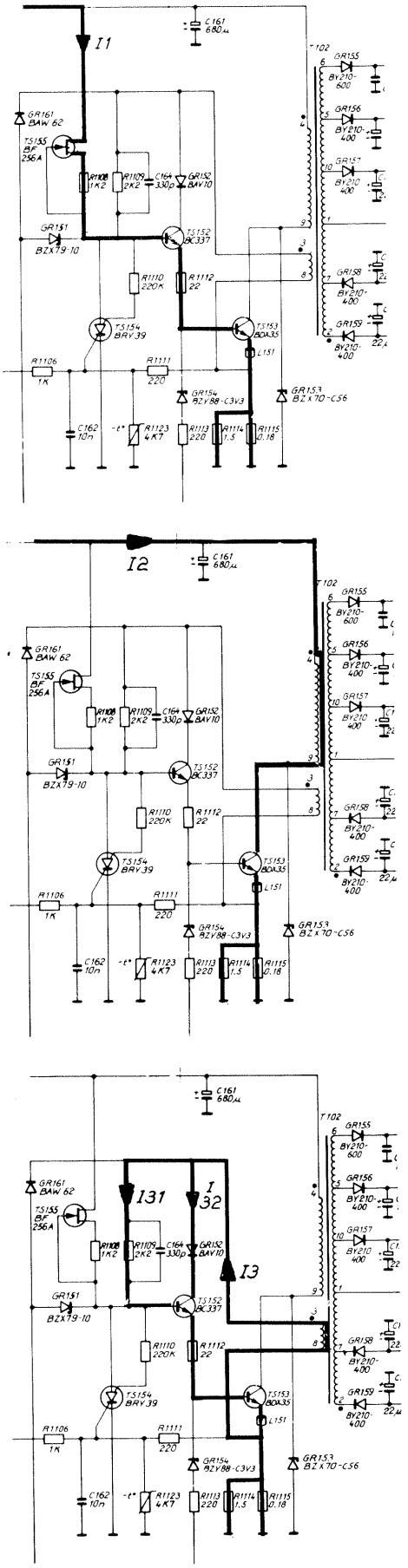


Fig. VIII-7. Current paths in DC-to-DC converter