10. FRONT UNIT (A7-A8)

The front unit consists of:

- the microcomputer control circuit
- the LCD display circuit
- the front panel controls

10.1 MICROCOMPUTER CONTROL CIRCUIT

10.1.1 Introduction to MAB8052 microcomputer

The integrated circuit MAB8052, one of the MSC-51 family of single chip microcomputers, forms the basis of the microcomputer system of the oscilloscope. The MAB8052 has an internal 8 k ROM and 256 bytes RAM with address/data decoding facilities. In addition to this, the 8052 has 32 I/O lines. Data written to these lines remains unchanged until rewritten. Each line is able to serve as input or output, or both, even though outputs are statically latched. To provide specific serial data transfer possibilities, the microcomputer system contains an I^2C bus interface.

10.1.2 Characteristics of the I^2C bus

The I^2C bus is for 2-way, 3-line communication between different ICs or modules. The three lines are a serial data line (SDA), a serial clock line (SCL) and ground. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer:

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

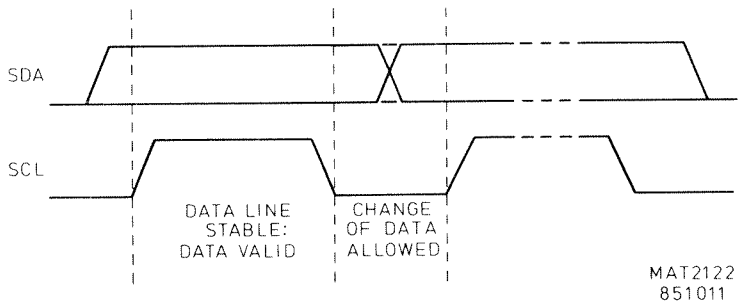

Figure 10.1 Bit transfer

Start and stop conditions:

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

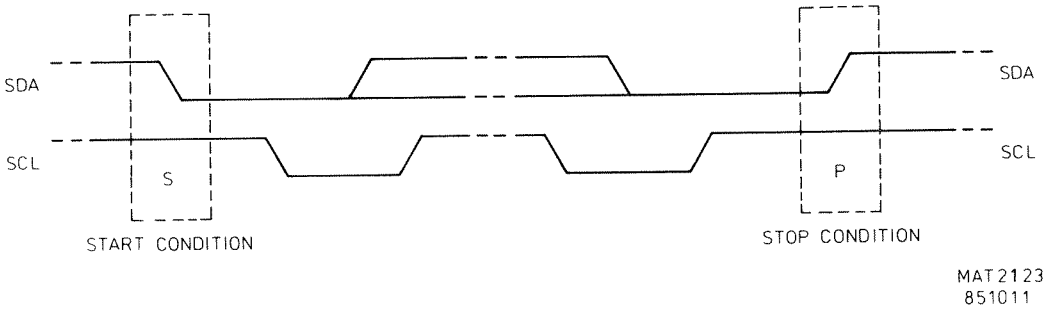

Figure 10.2 Definition of start and stop conditions

10.1.3 I^2C structure

The two lines SDA and SCL are fed to the various circuits, where, depending on the addressing, this serial information is converted into the different control signals (see figure 10.3).

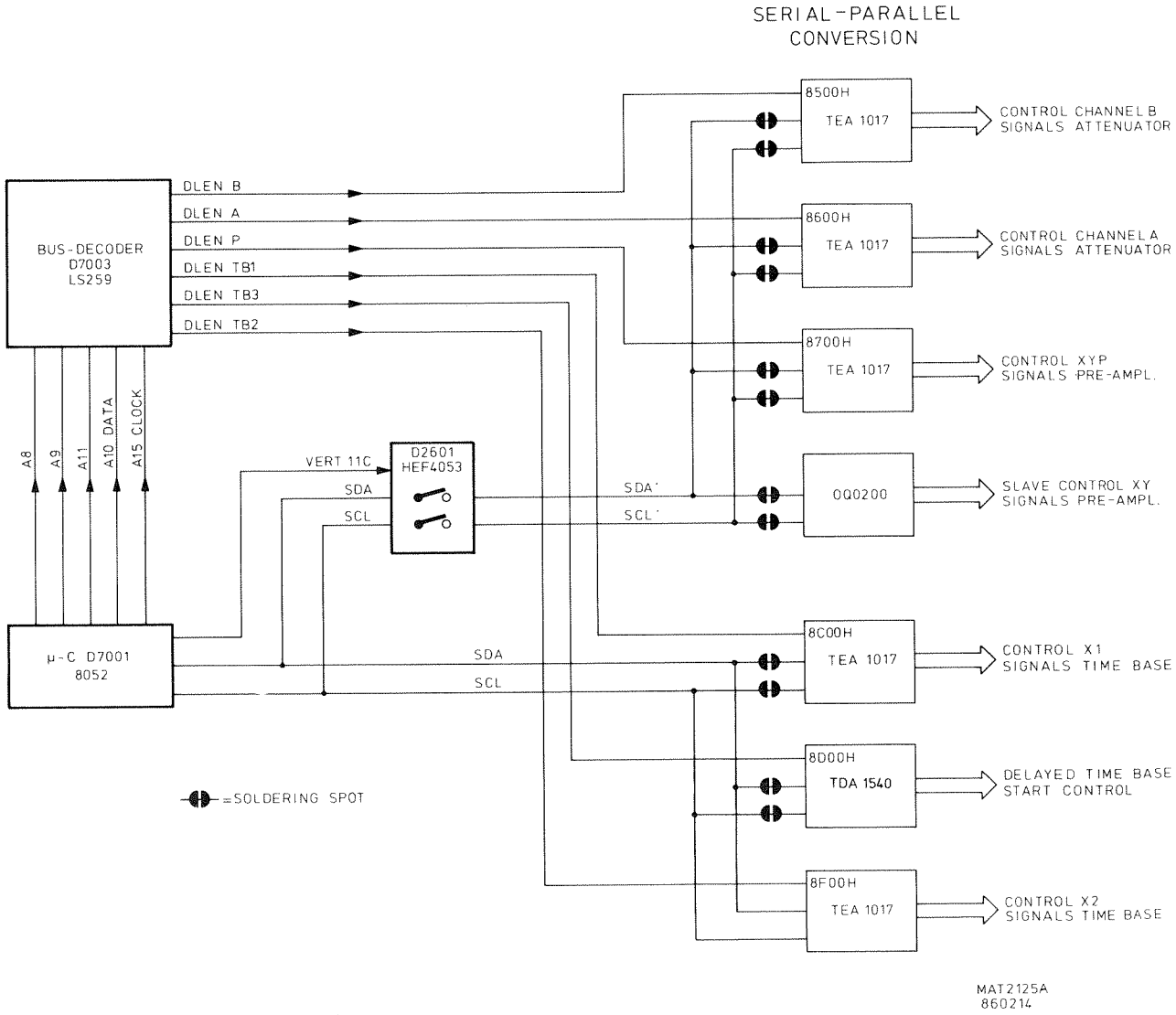

Figure 10.3 I^2C structure

To select the serial-parallel conversion circuits, the bus decoder D7003 decodes the address lines A8, A9 and A11 into the DLEN (Data latch enable) signals according to the next table

ADDRESS LINES A11	A9	A8	DATA A10		
0	0	0	1/0	8400H	SEL IIC
0	0	1	1/0	8500H	DLEN B
0	1	0	1/0	8600H	DLEN A
0	1	1	1/0	8700H	DLEN P
1	0	0	1/0	8C00H	DLEN TB1
1	0	1	1/0	8D00H	DLEN TB3
1	1	0	1/0	8E00H	DLEN TB2
1	1	1	1/0	8F00H	N.C.

To eliminate interference in the vertical circuits, the I^2C bus can be switched off for this circuit by switch D2601. The timing is obtained by the VERT IIC line.
Note that for servicing, solder joints are added in the p.c.b. tracks connecting the circuits. These can be used to localize a fault in the I^2C-bus by means of interrupting the bus connection.

10.1.4. Microcomputer MAB8052

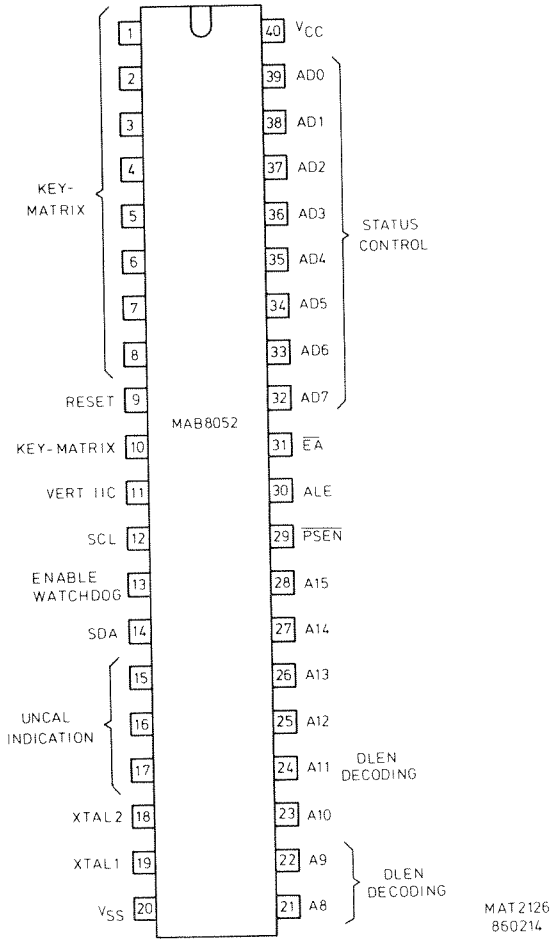

Figure 10.4 Pinning of microcomputer MAB 8052

The microprocessor has the following connections:

* Crystal connections (pin 18 and 19)
  A 12 MHz crystal is connected to the inputs XTAL1 and XTAL2 to provide an accurate timing reference source.

* RESET input (pin 9)
  After switching on a reset level HIGH is applied to this input. This reset signal forces the microcomputer to initiate the main program, beginning at the address 00000H. After the +5 V supply is within its specification, the RESET is released and the microcomputer is ready for use.

* 8-bit quasi bidirectional I/0 port (pin 1...pin 8) and quasi-bidirectional I/0 port (pin 10), used to read the settings of the KEY-MATRIX switches S2...S32 (excl. S12-AUTOSET)

* 3-bit quasi-bidirectional I/0 port (pin 15...pin 17), used to read the UNCAL position of S5, S7 and S9 (UNCAL when logic HIGH).

* WATCHDOG input (pin 13)
  The WATCHDOG is a facility to control the correct function of the software. When HIGH the internal counter will run. The software gives a pulse every 64 ms max. to reset this counter, so that the 64 ms max. cycle starts again. If the software does not function correctly, the internal counter receives no reset pulse and the counter will overflow initiating the main program (start address 0000H).

* 8-bit open drain bidirectional I/0 port (pin 21...pin 28) used for addressing the serial-parallel conversion circuits (see I^2C structure).

* 8-bit quasi-bidirectional I/0 port (pin 32...pin 39) used to read the status input via D7006.

* SDA (pin 14); SCL (pin 12)
  Bidirectional I^2C lines.

* VERT IIC (pin 11)
  Signal used as a digital switch control to switch-off the I^2C bus of the pre-amplifier control.

10.1.5. I^2C decoding

Integrated circuit D7002 serves as a multiplexer to make a separation between the I^2C lines for the LCD drives and the I^2C lines for the other circuits, controlled by the SEL IIC line. Only when SEL IIC is HIGH (address 8400H), are the SDA and SCL lines from the microcomputer connected to unit A8.

10.1.6. Status input

Integrated circuit D7006 serves as an input port to read the following status info:

- TEST OUT, indication for triggered mode, HIGH when triggered.
- FOOTN, remote control for AUTO SET, LOW when active.
- NOPTION, adapts software for optional trigger coupling, LOW when optional triggering.
- REMRQN, remote request line, LOW when active.
- probe indication status, adapts V/DIV reading for probe attenuation.

When the enable inputs (pin 1 and pin 19) become LOW, the status input is read and copied in the accumulator of the microcomputer via the data lines AD0...AD7.

Note that enabling is only possible when D7002-2 is switched-on to D7002-15, i.e. when A15 is HIGH (address 8000H ... FFFFH).

10.1.7 Probe indicator

Integrated circuit D7004 (000044) detects the kind of probe which is connected to the oscilloscope. Depending on the resistance between the probe indication input (pin 3 for channel A and pin 16 for channel B) and ground, the V/DIV reading of the LCD automatically increases according to the next table.

Pin 3 (16)	Pin 6 (17)	Pin 7 (12)	V/DIV attenuation
2k32	0	0	x10
6k98	1	0	x100
7k68	0	1	x1
10k	1	1	x1

10.1.8 C-Bus decoder

This integrated circuit decodes the address lines A8, A9 and A11 into the DLEN signals.
During the power-up all the lines are reset to LOW.

10.2 LCD DISPLAY CIRCUIT

The LCD is driven by three drivers D8001, D8002 and D8003 (PCF8577). The temperature dependent supply voltage VCPCF is 4 V approx. at 25°C. When the temperature increases, this voltage decreases.
The single-pin built-in oscillator on pin 37 of D8001 provides the modulation frequency for the LCD segment driver outputs. Capacitor C7008 and resistor R7038 are connected to this pin to form the oscillator, with a frequency of 150 Hz approx. Pin 36 and pin 37 are used to determine the LCD drivers address in the I^2C bus.

The outputs pin 1...pin 32 directly drive the LCD.

Outputs BP1 and BP2 (pin 33 and pin 34) drive the COMMON pins of the LCD.

10.3 FRONT-PANEL CONTROLS

The front-panel controls give a voltage between 0 V...10 V to the various circuits.
To determine the UNCAL condition of VAR A, VAR B or VAR MTB, the d.c. voltages of the slider of the potentiometers are applied to comparator N7001. When the voltage level of the control is lower than 0,7 V, the microcomputer reads a logic LOW on its input and adapts the LCD display to indicate the CAL status (e.g. no flashing ">" sign visible).

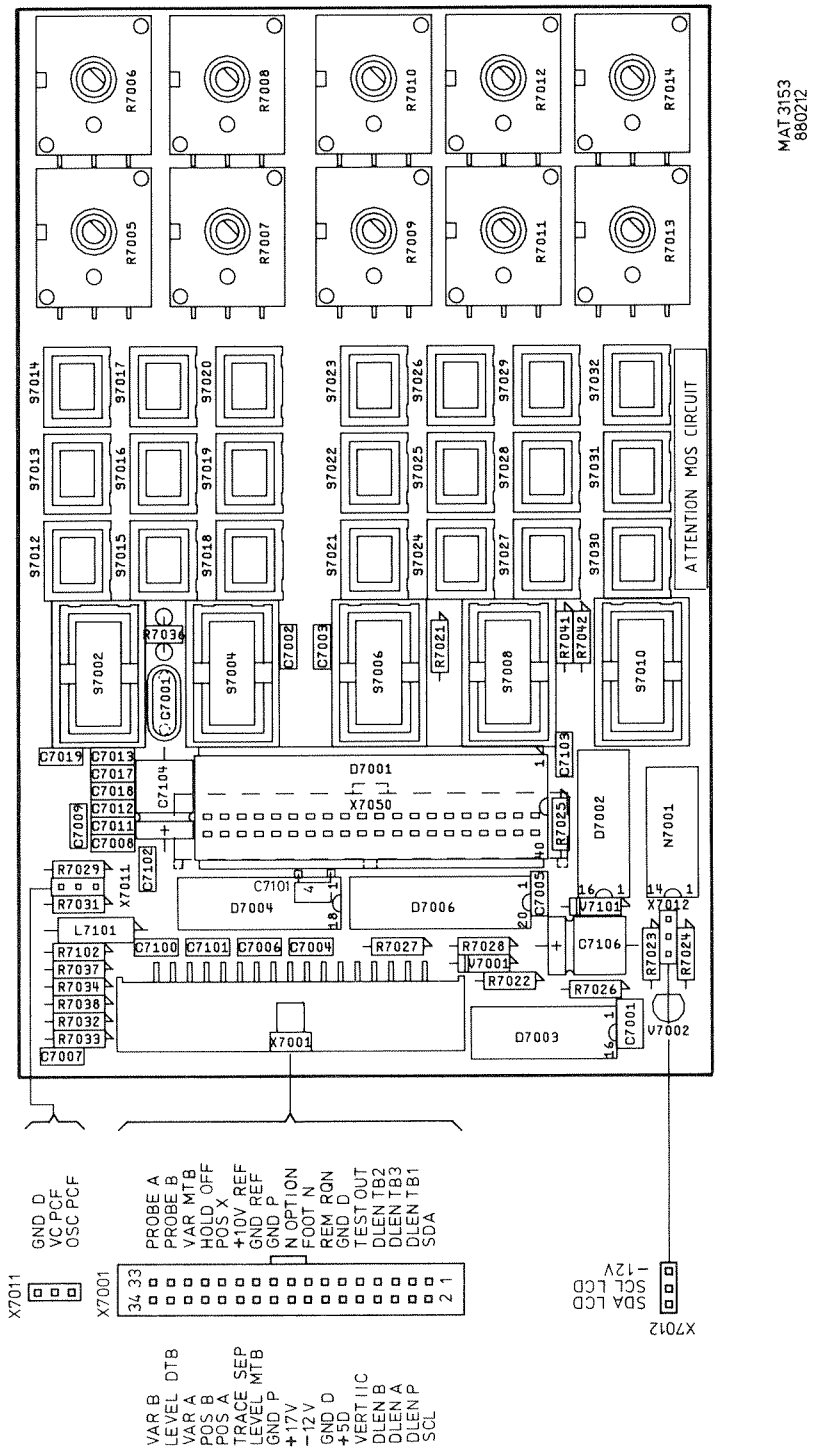

Figure 10.5 Front unit p.c.b.