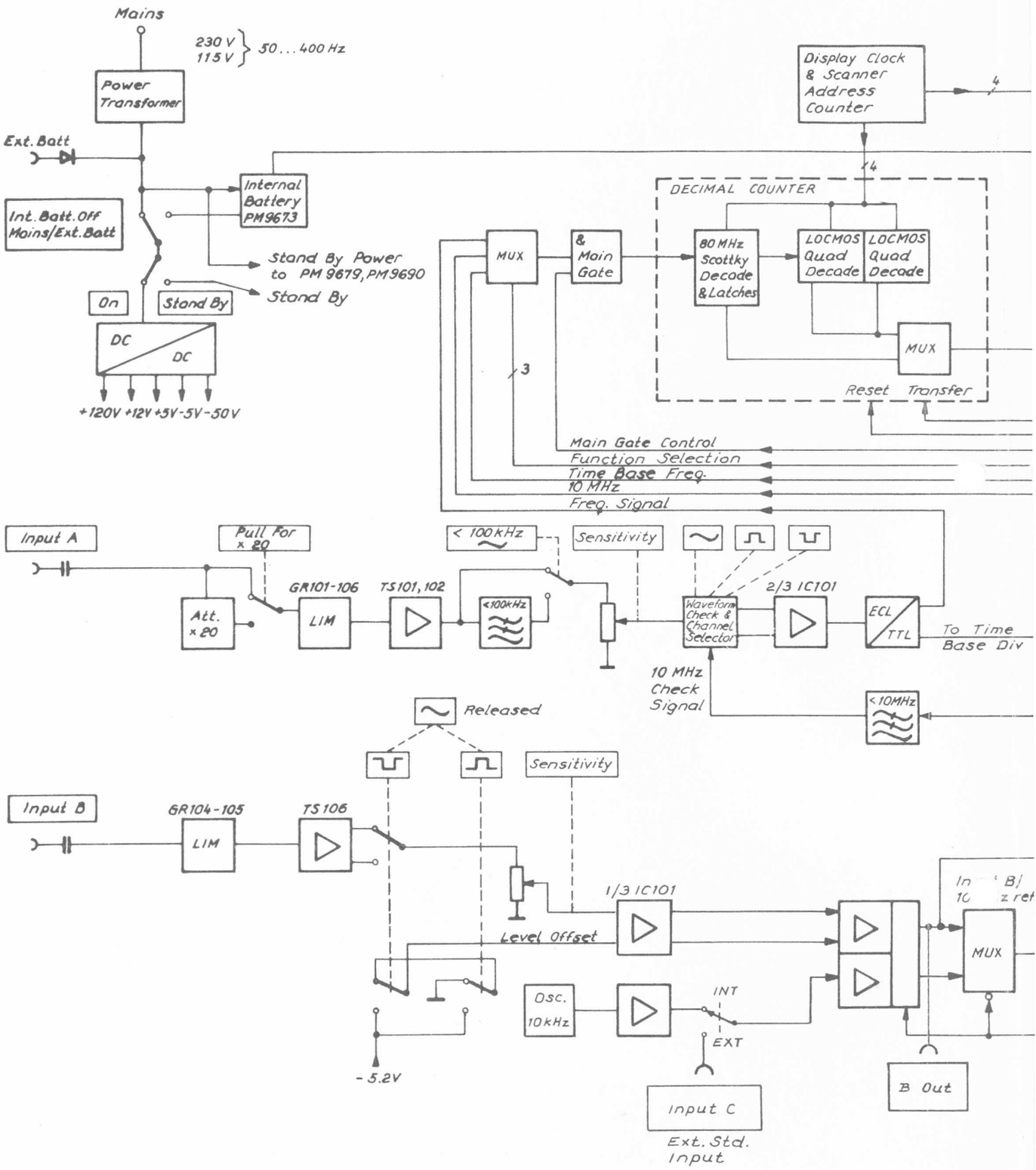

Mains
230 V
115 V
50...400 Hz
Power Transformer
Ext. Batt
Int. Batt. Off Mains/Ext. Batt
Internal Battery PM9673
Stand By Power to PM 9679, PM 9690
Stand By
On
Stand By
DC
DC
+120V +12V +5V -5V -50V
Display Clock & Scanner Address Counter
4
4
DECIMAL COUNTER
MUX
& Main Gate
80 MHz Scottky Decade & Latches
LOCMOS Quad Decade
LOCMOS Quad Decade
MUX
3
Reset Transfer
Main Gate Control
Function Selection
Time Base Freq.
10 MHz
Freq. Signal
Input A
Pull For x 20
Att. x 20
GR101-106
LIM
TS101, 102
< 100kHz
< 100kHz
Sensitivity
Waveform Check & Channel Selector
2/3 IC101
ECL
TTL
To Time Base Div
10 MHz Check Signal
< 10MHz
Released
Sensitivity
Input B
GR104-105
LIM
TS106
1/3 IC101
Level Offset
Osc. 10kHz
INT
EXT
-5.2V
MUX
B Out
Input C
Ext. Std. Input

PM 66 12

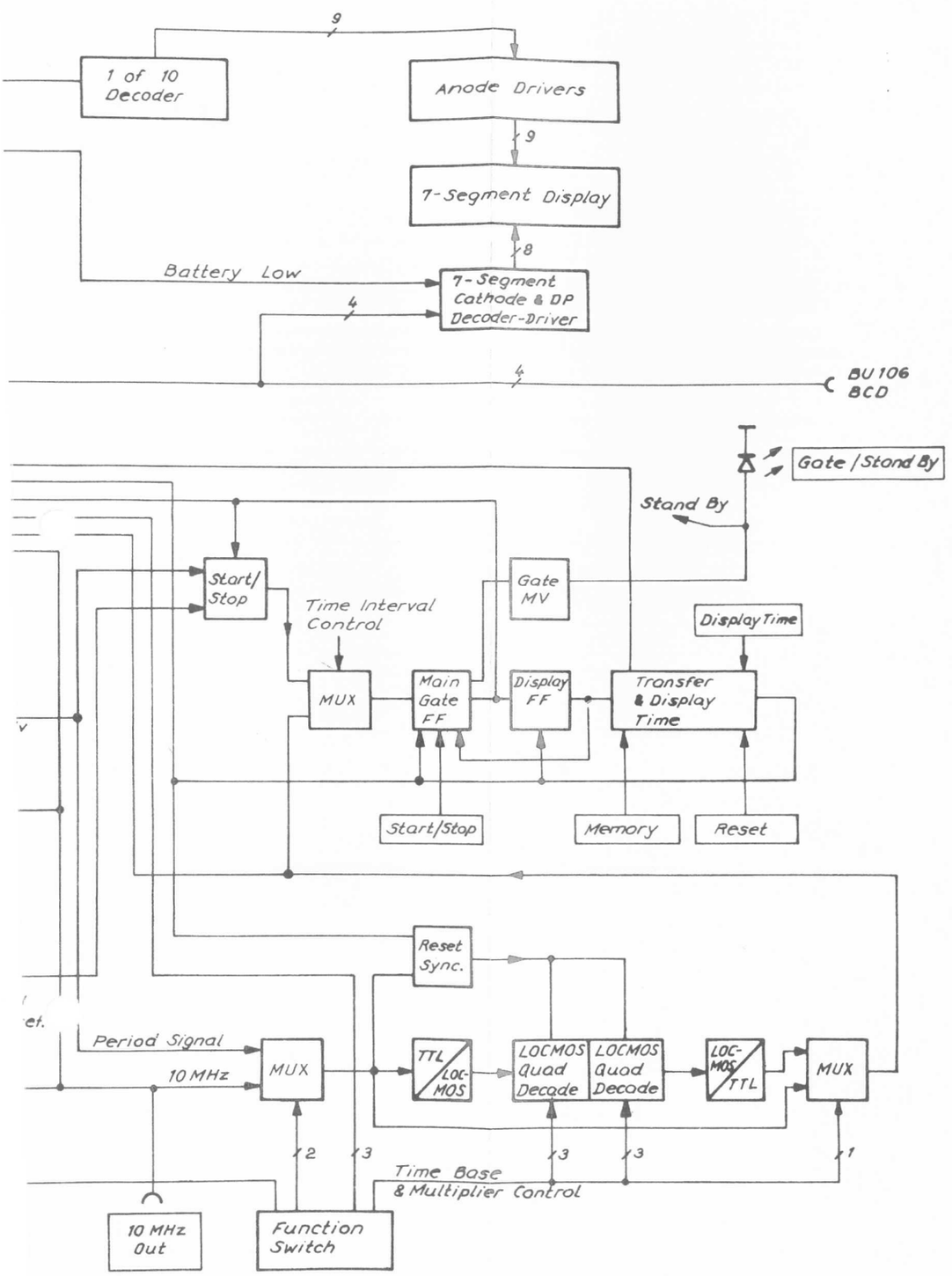


Fig. XIII-1. Block diagram

BU105
GR163
VL150
T101
GR167
R1124
IC123
IC126
IC127
IC122
IC121
IC183
IC172
IC125
IC150
IC185
IC170
IC171
IC173
IC184
IC182
IC178
IC174
C152
C161
C160
C154
C157
C158
C156
C155
T102
C153
TS153
GR153
BU104
BU106
C141
C172
C121
L150
L151
L152
TS150
TS151
TS152
TS154
TS155
Tp3
Tp4
Tp5
Tp6
Tp8
Tp9
Tp10
Tp11

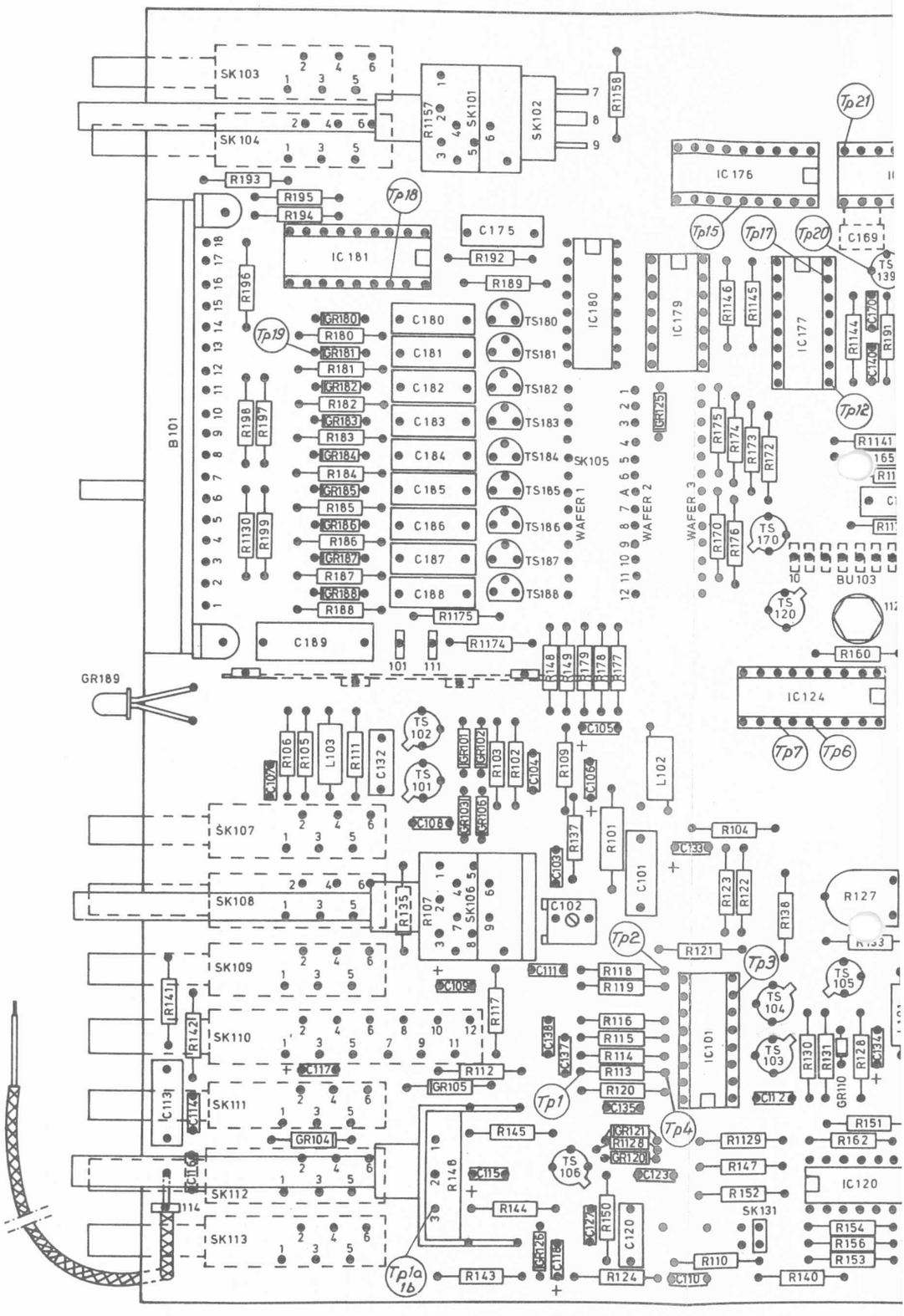
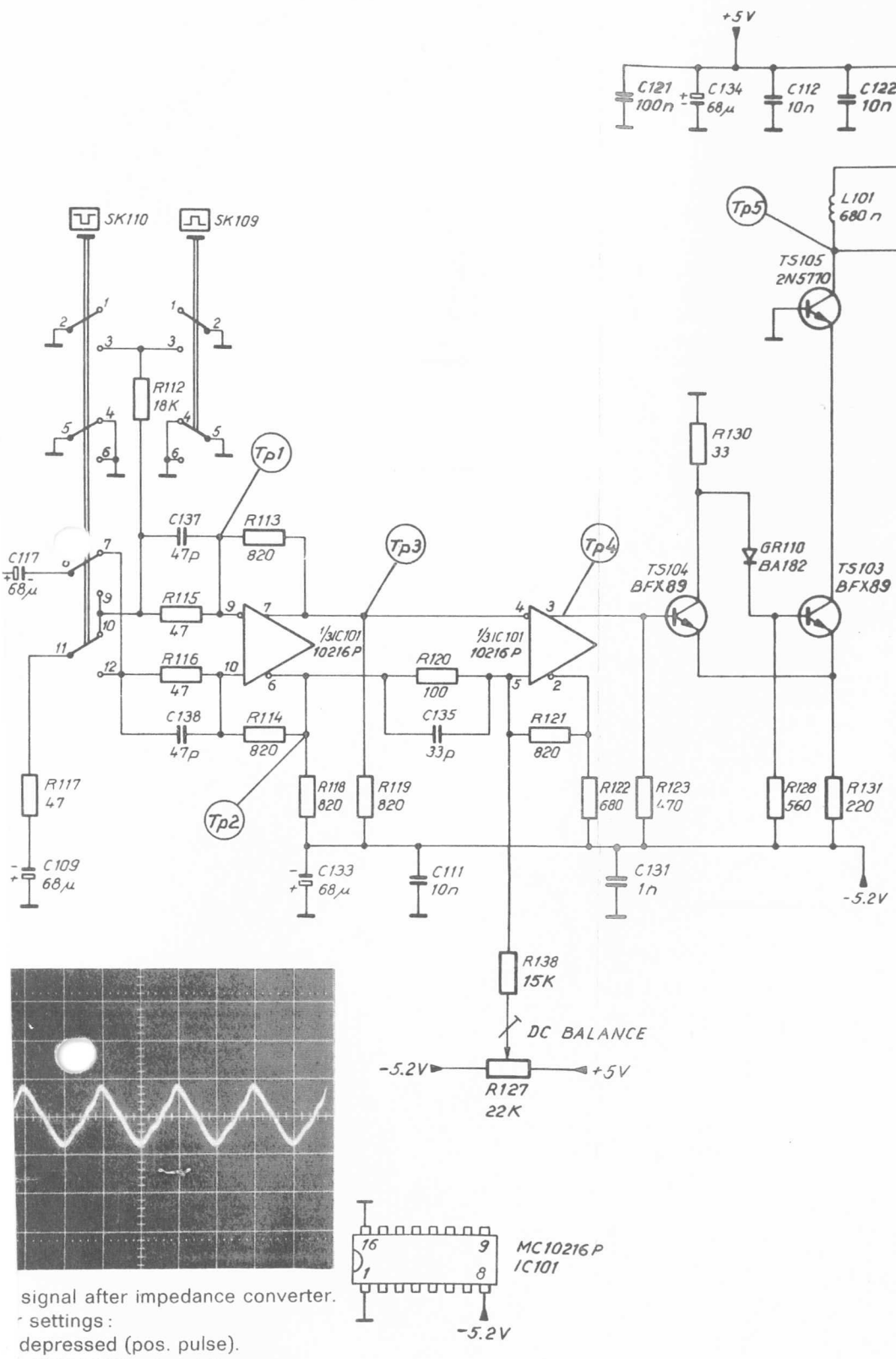
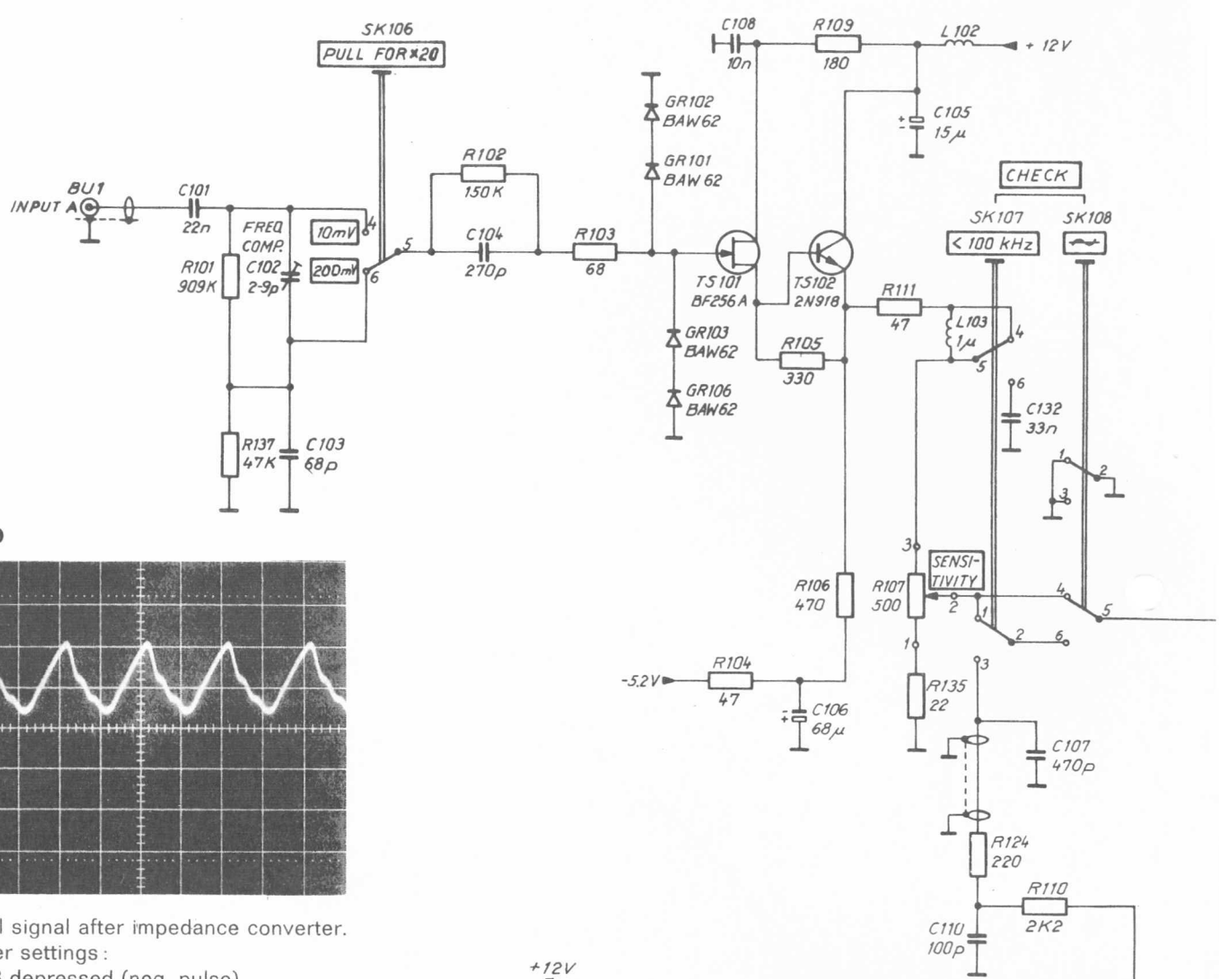


Fig. XIII-2. Component layout



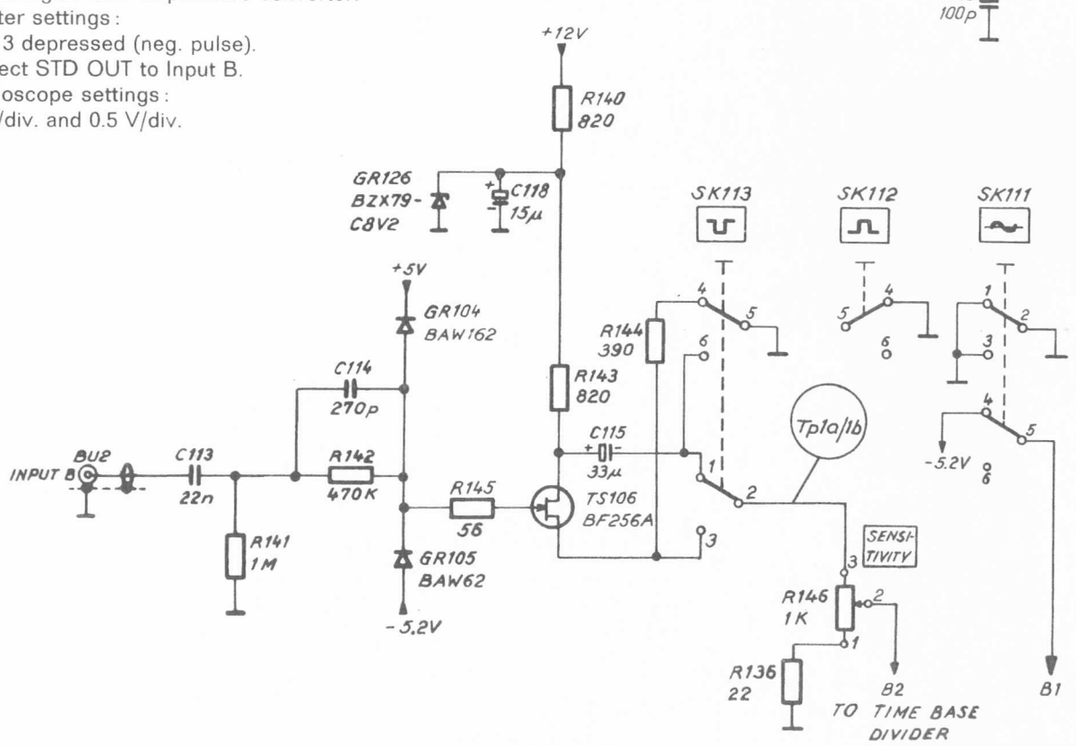
signal after impedance converter.
' settings:
depressed (pos. pulse).
t STD OUT to Input B.
:cope settings:
v. and 0.5 V/div.

Fig. XIII-3. Circuit diagram, input amplifiers A and B

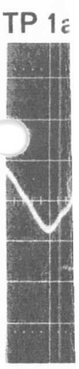


TP 1b

Normal signal after impedance converter.
Counter settings:
SK 113 depressed (neg. pulse).
Connect STD OUT to Input B.
Oscilloscope settings:
50 ns/div. and 0.5 V/div.



TP 1a



Normal
Counte
SK 112
Connec
Oscillo
50 ns/d

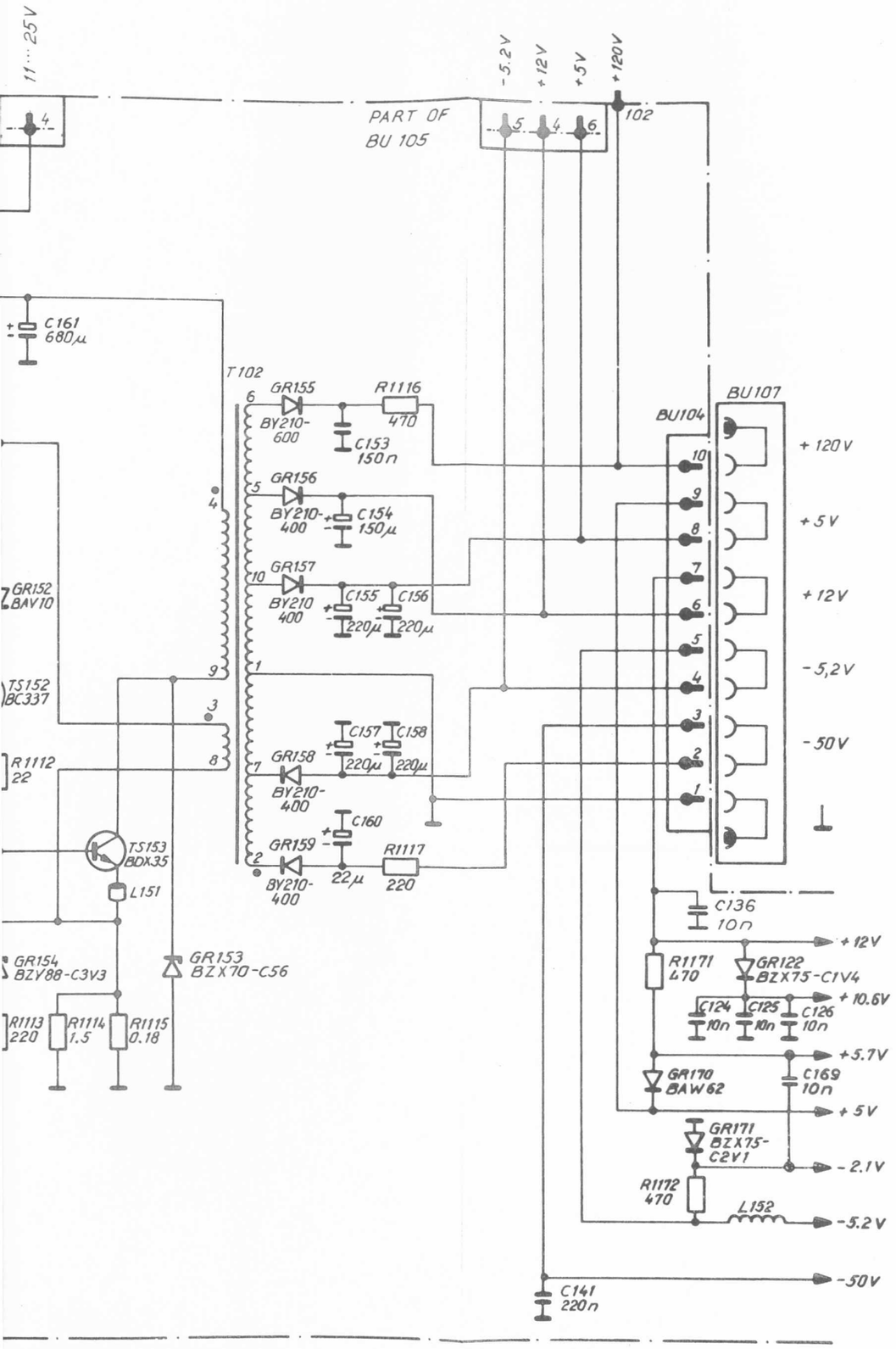
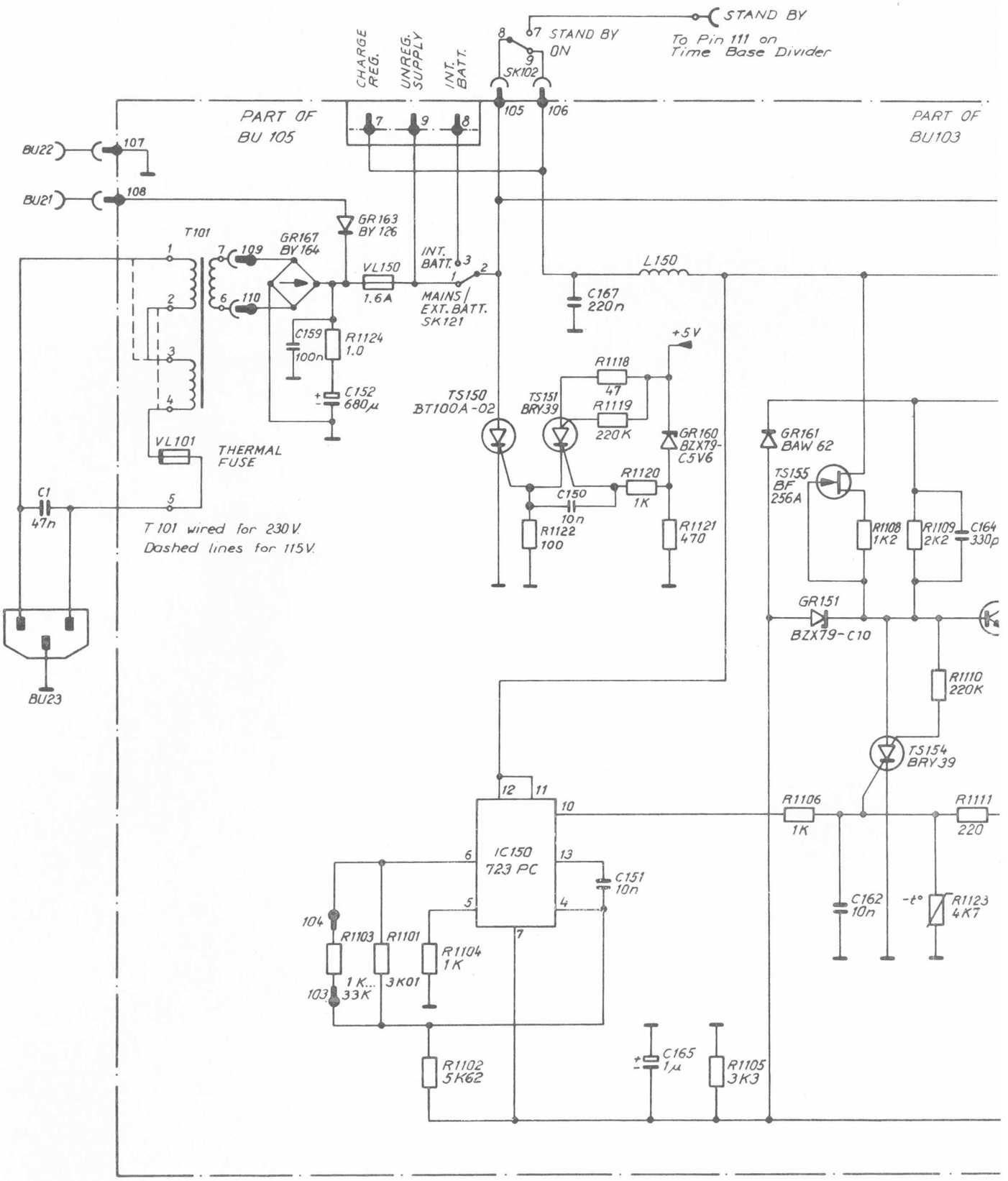
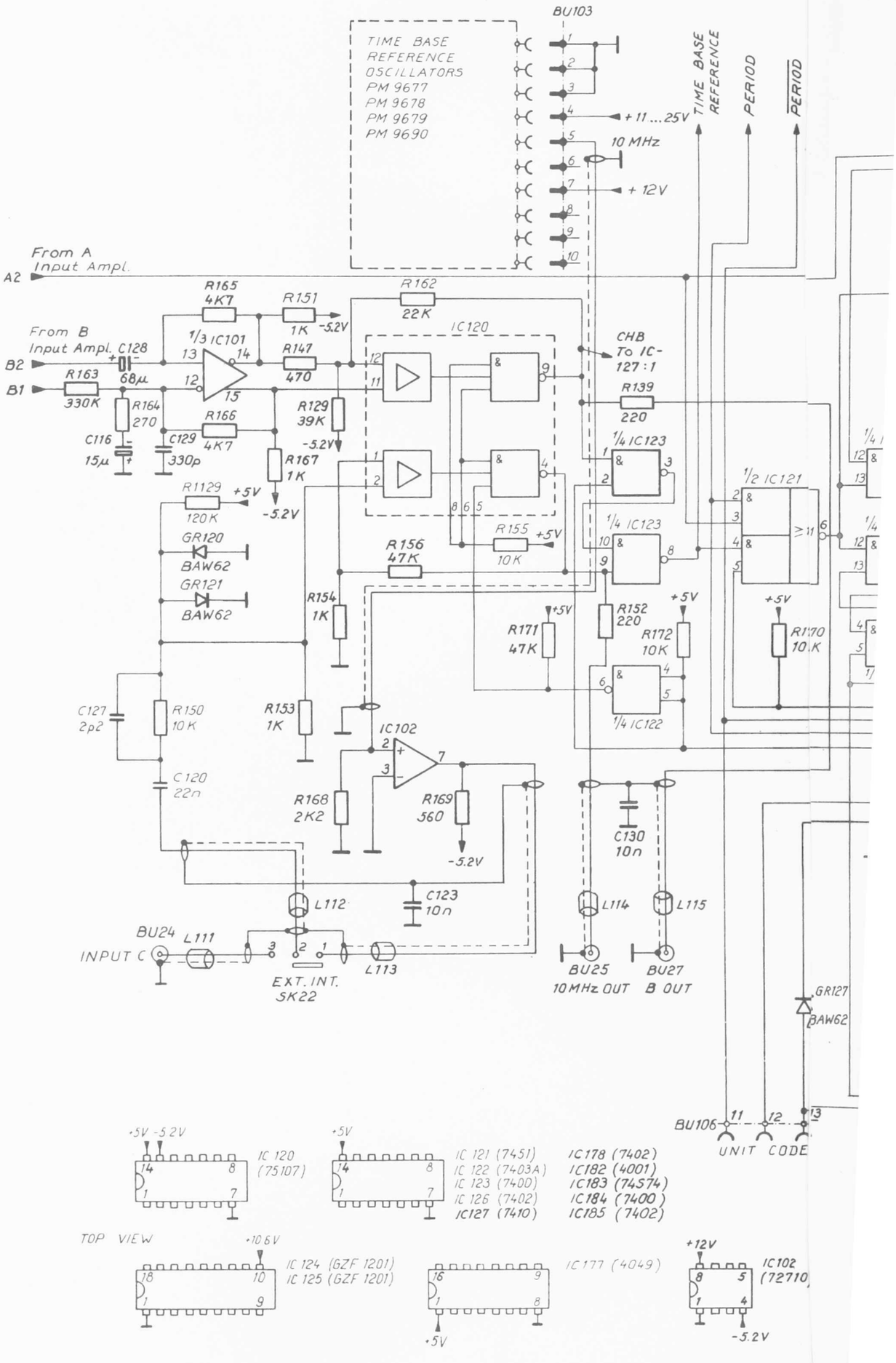
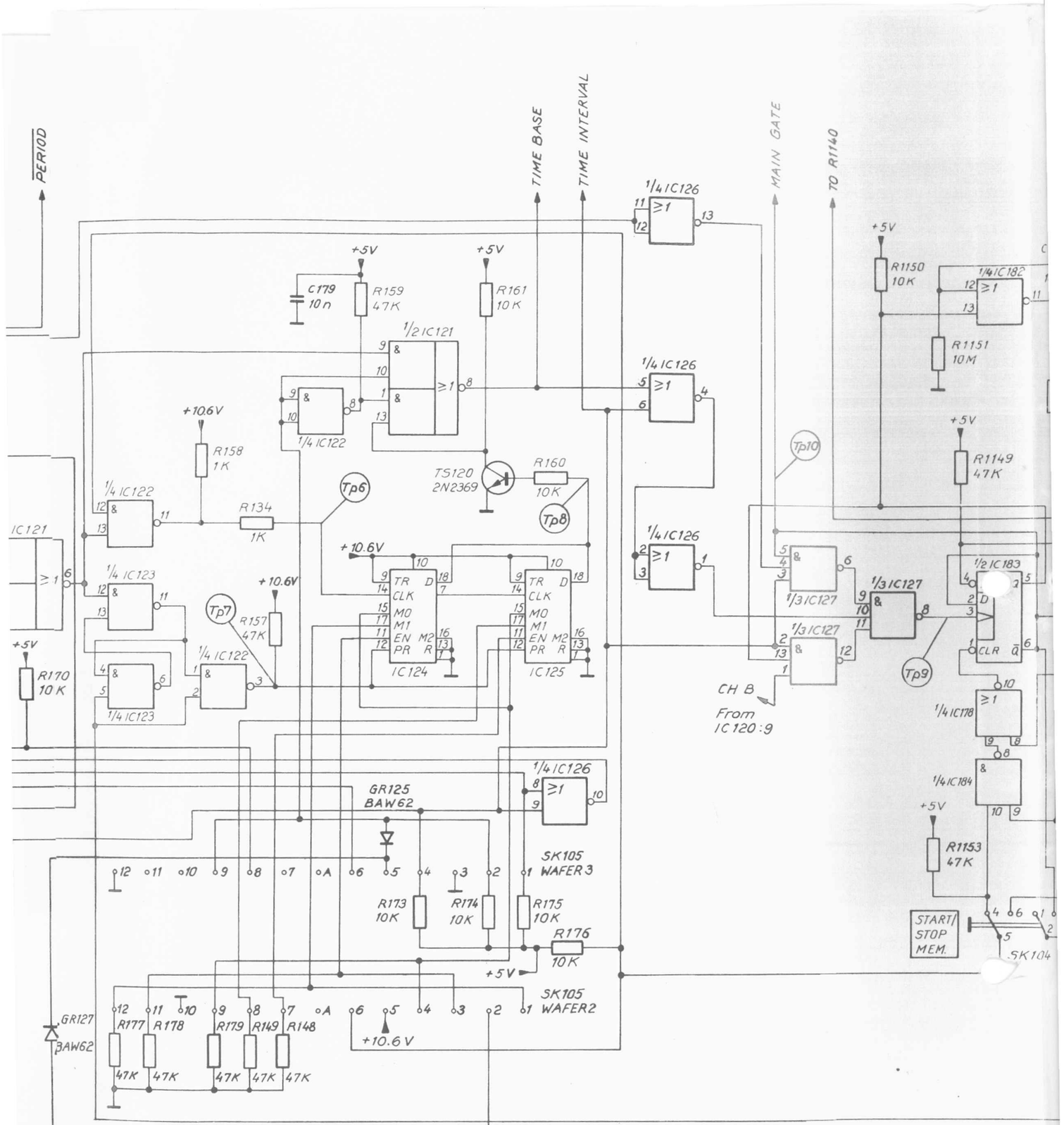


Figure XIII-6. Circuit diagram, power supply

PM66a


STAND BY
To Pin 111 on Time Base Divider
CHARGE REG.
UNREG. SUPPLY
INT. BATT.
8
7 STAND BY ON
9
SK102
105
106
PART OF BU 105
PART OF BU103
BU22
107
BU21
108
GR163 BY 126
T101
GR167 BY 164
109
110
INT. BATT.
VL150
1.6A
MAINS / EXT. BATT. SK121
L150
C167 220n
C159 100n
R1124 1.0
C152 680µ
+5V
R1118 47
R1119 220K
TS150 BT100A-02
TS151 BRY39
GR160 BZX79-C5V6
GR161 BAW 62
TS155 BF 256A
R1120 1K
C150 10n
R1122 100
R1121 470
R1108 1K2
R1109 2K2
C164 330p
VL101
THERMAL FUSE
C1 47n
T 101 wired for 230V.
Dashed lines for 115V.
GR151 BZX79-C10
R1110 220K
TS154 BRY39
BU23
IC150 723 PC
C151 10n
R1106 1K
R1111 220
C162 10n
R1123 4K7
R1103 1K...33K
R1101 3K01
R1104 1K
R1102 5K62
C165 1µ
R1105 3K3


BU103
TIME BASE REFERENCE OSCILLATORS
PM 9677
PM 9678
PM 9679
PM 9690
+ 11 ... 25V
10 MHz
+ 12V
TIME BASE REFERENCE
PERIOD
PERIOD
From A Input Ampl.
A2
From B Input Ampl.
B2
B1
R165 4K7
R151 1K
-5.2V
R162 22K
IC120
1/3 IC101
C128 68µ
R163 330K
R164 270
C116 15µ
R166 4K7
C129 330p
R147 470
R129 39K
-5.2V
R167 1K
CHB To IC-127 : 1
R139 220
1/4 IC123
1/2 IC121
R1129 120K
+5V
-5.2V
GR120 BAW62
GR121 BAW62
R155 10K
+5V
R156 47K
R154 1K
R171 47K
R152 220
R172 10K
R1170 10K
1/4 IC122
C127 2p2
R150 10K
R153 1K
IC102
C120 22n
R168 2K2
R169 360
-5.2V
C130 10n
L112
C123 10n
L114
L115
BU24
INPUT C
L111
EXT. INT. SK22
L113
BU25 10MHz OUT
BU27 B OUT
GR127 BAW62
BU106
UNIT CODE
+5V -5.2V
IC 120 (75107)
+5V
IC 121 (7451)
IC 122 (7403A)
IC 123 (7400)
IC 126 (7402)
IC127 (7410)
IC178 (7402)
IC182 (4001)
IC183 (74S74)
IC184 (7400)
IC185 (7402)
TOP VIEW
+10.6V
IC 124 (GZF 1201)
IC 125 (GZF 1201)
IC 177 (4049)
+5V
+12V
IC102 (72710)
-5.2V



SK105

MODE		PINS CONNECTED	
		WAFER 2	WAFER 3
RATIO A/B	$n=10^4$	1-3-4-5	1-2-3-4
	$n=10^2$	3-4-5	1-2-3-4
COUNT A		3-4-5; 6-10	1-2-3-4-6
FREQ. A	0.1s	4-5-7	1-3-4-5-6
	1s	5-7-8	1-3-4-5-6
	10s	5-7-8-9	1-3-4-5-6
PERIOD A	$n=1$	5-7-8-9	3-4-6-8
	$n=10^2$	5-8-9-11	3-4-6-8-9
	$n=10^4$	5-9-11-12	3-4-6-8-9
T.I. A-B	ms	1-5-11-12	1-3-6-9
	µs	1-5-11-12; 2-6	1-3-6

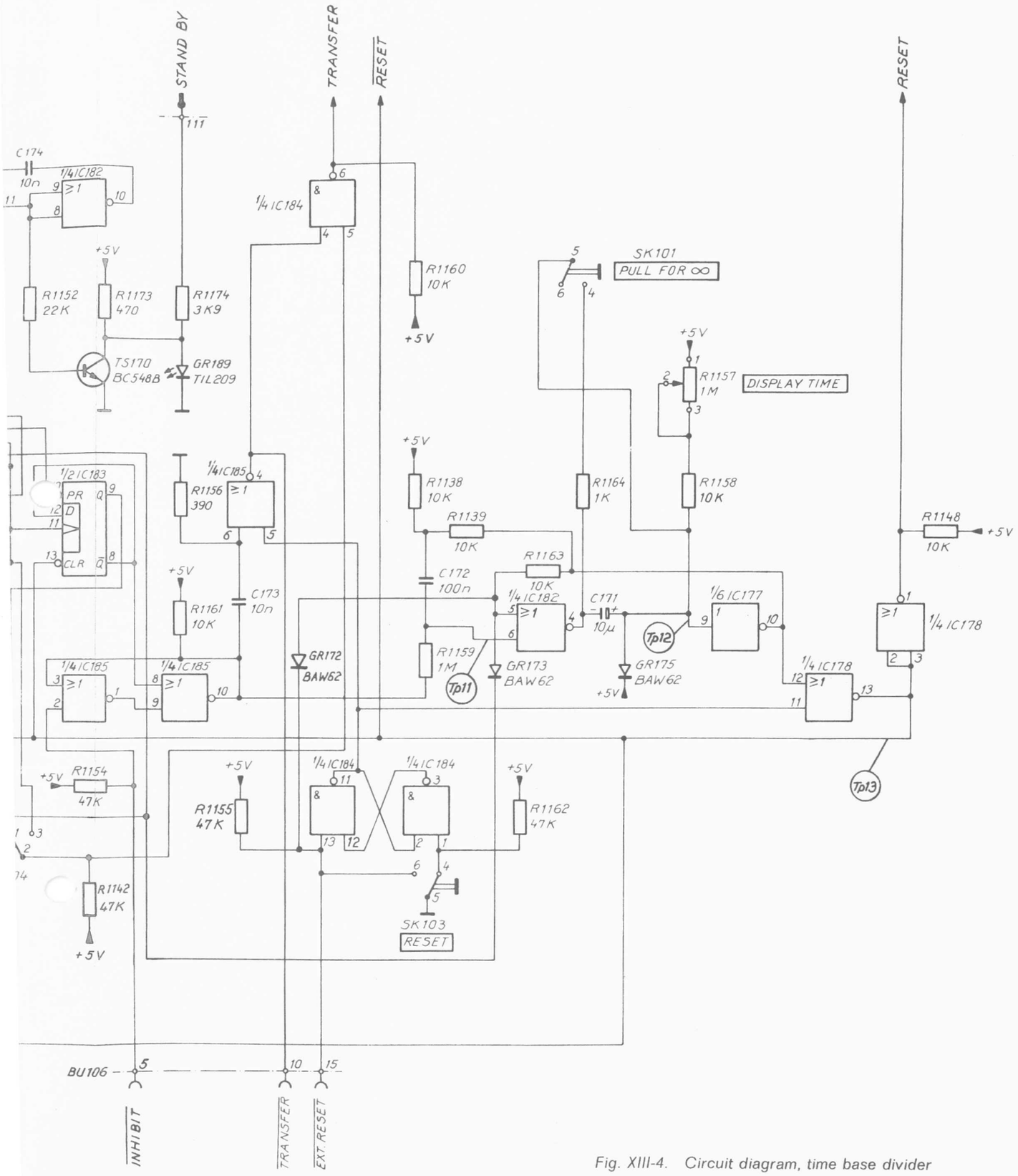
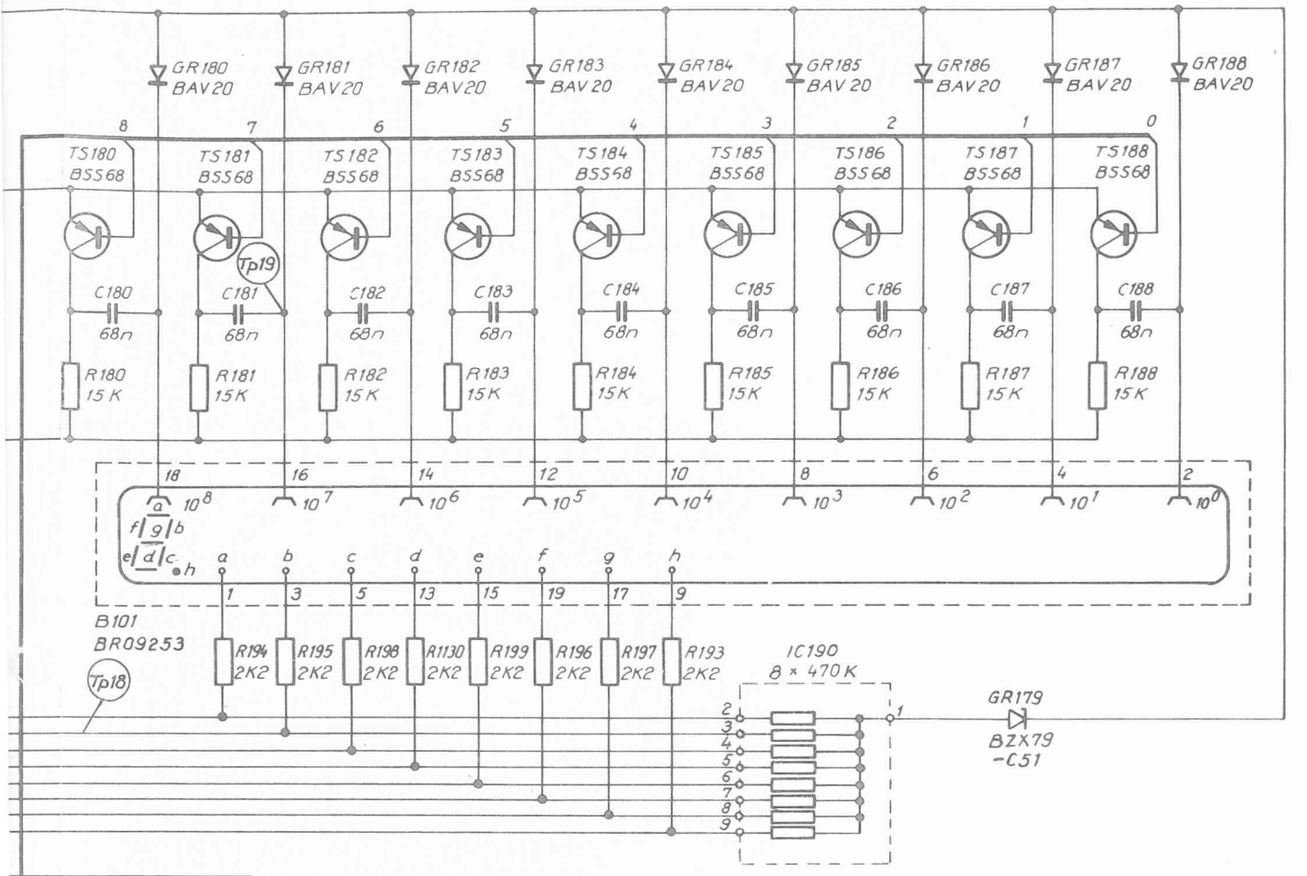
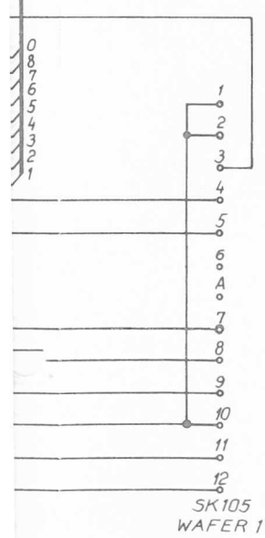


Fig. XIII-4. Circuit diagram, time base divider

PM6672

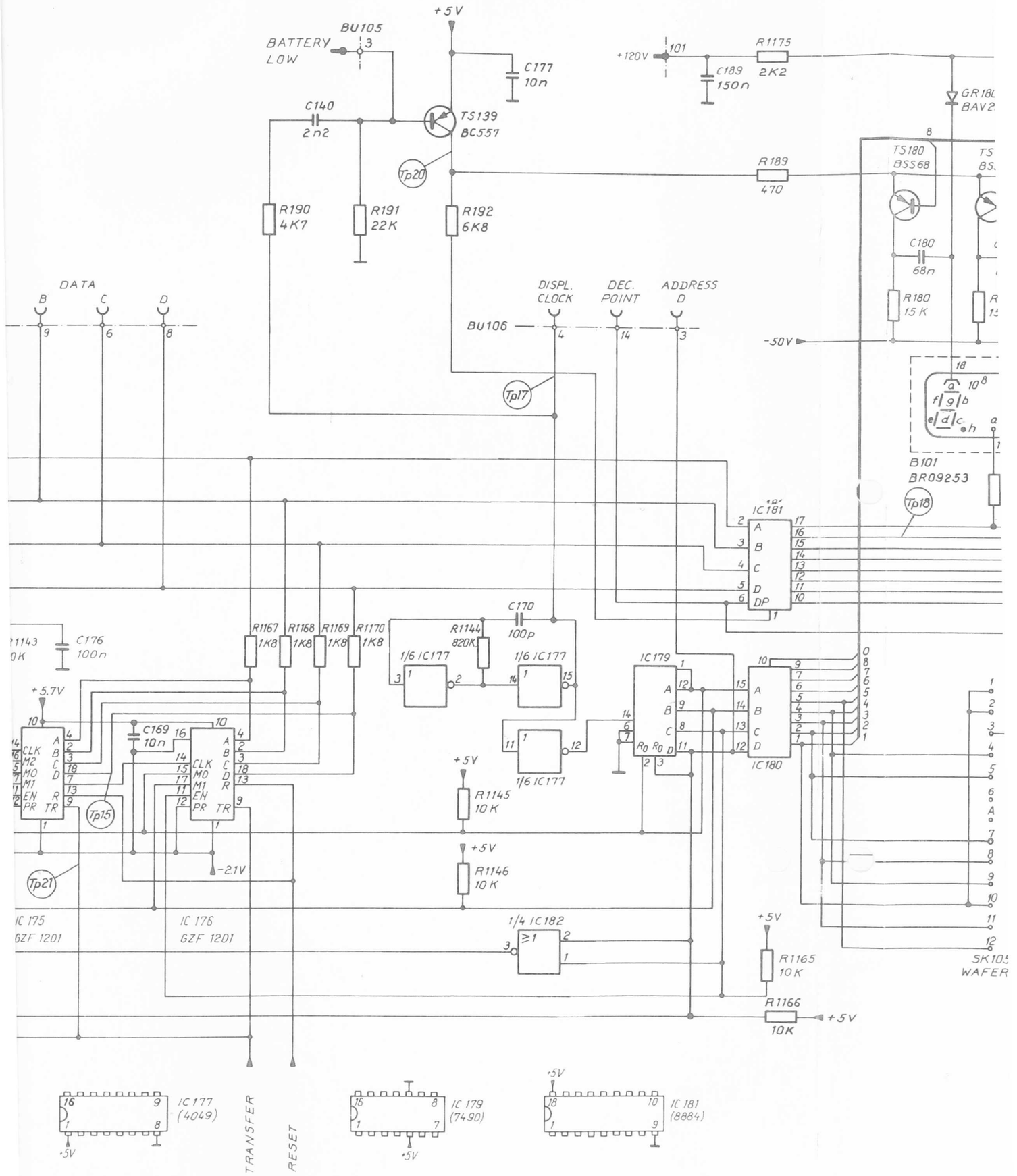


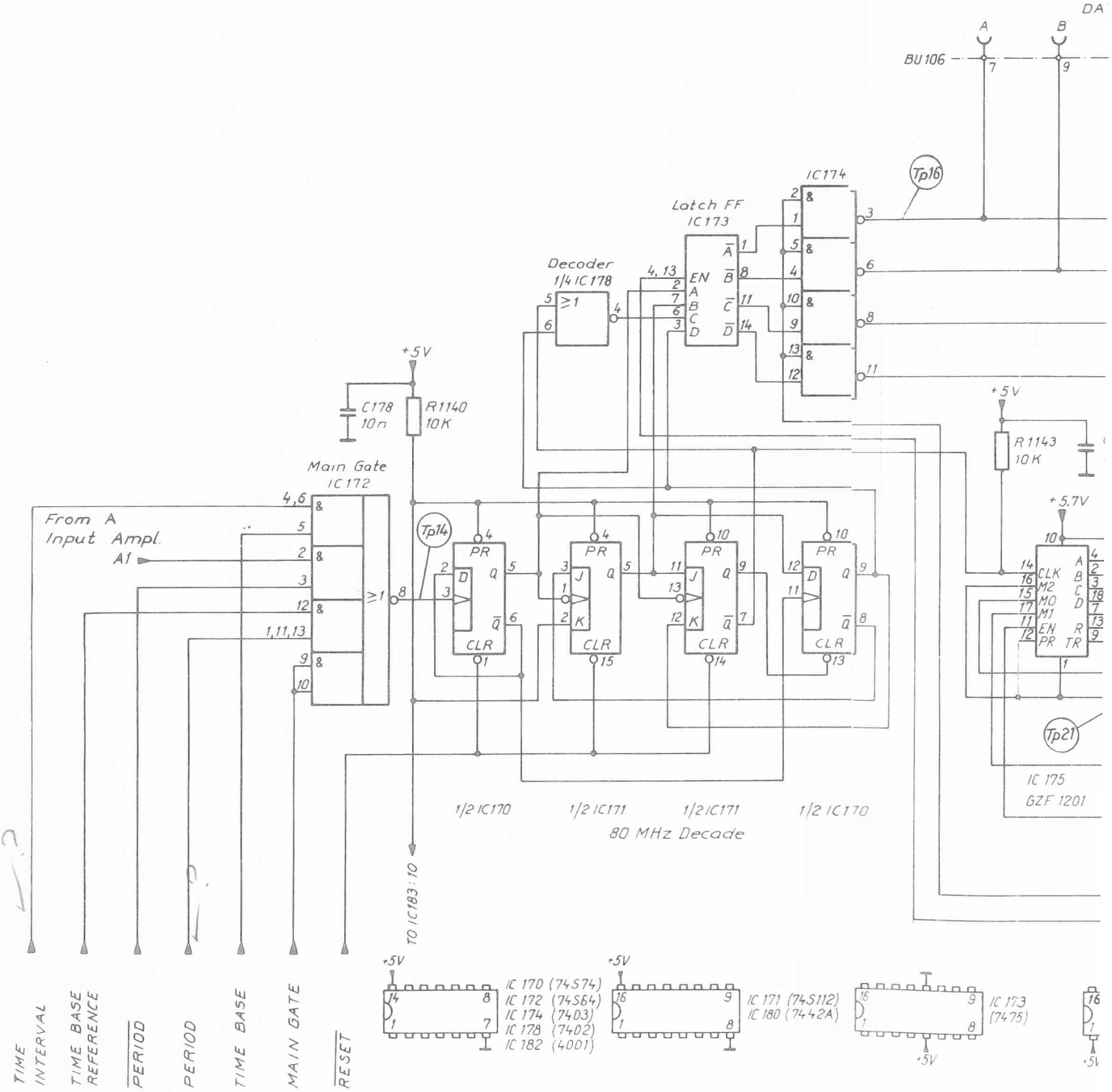


SK105

MODE		PINS CONNECTED ON WAFER1
RATIO A/B	n = 10⁴	3 - 4
	n = 10²	3 - 5
COUNT A		3 - 6
FREQ. A	0.1s	3 - 7
	1 s	3 - 8
	10s	3 - 9
PERIOD A	n = 1	3 - 10
	n = 10²	3 - 11
	n = 10⁴	3 - 12
T.I.A-B	ms	3 - 1
	µs	3 - 2

Fig. XIII-5. Circuit diagram, decimal counting unit and display


+5V
BU105
BATTERY LOW
C177 10n
C140 2n2
TS139 BC557
Tp20
R190 4K7
R191 22K
R192 6K8
+120V
101
C189 150n
R1175 2K2
GR18L BAV2
TS180 BS568
R189 470
C180 68n
R180 15 K
-50V
B101 BR09253
Tp18
DATA
B
C
D
BU106
DISPL. CLOCK
DEC. POINT
ADDRESS D
Tp17
IC181
R1167 1K8
R1168 1K8
R1169 1K8
R1170 1K8
C170 100p
R1144 820K
1/6 IC177
C176 100n
+5.7V
C169 10n
Tp15
Tp21
-2.1V
IC179
IC180
R1145 10 K
R1146 10 K
1/4 IC182
R1165 10 K
R1166 10K
IC 175 GZF 1201
IC 176 GZF 1201
IC 177 (4049)
IC 179 (7490)
IC 181 (8884)
TRANSFER
RESET
SK105 WAFER

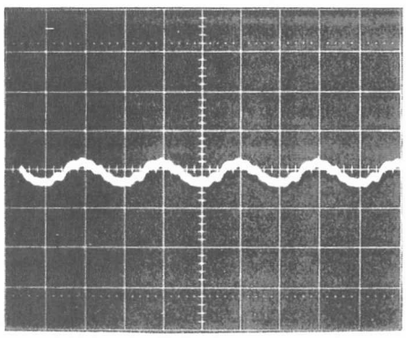

DA
A
B
BU 106
7
9
IC174
Tp16
Latch FF
IC 173
Decoder
1/4 IC 178
4, 13
EN
A
B
C
D
≥1
+5V
C178
10n
R1140
10K
Main Gate
IC 172
From A
Input Ampl.
A1
4,6
5
2
3
12
1,11,13
9
10
&
≥1
8
Tp14
PR
CLR
D
J
K
Q
1/2 IC170
1/2 IC171
1/2 IC171
1/2 IC170
80 MHz Decade
TO IC183 : 10
R 1143
10K
+5.7V
CLK
M2
MO
M1
EN
PR
TR
Tp21
IC 175
GZF 1201
TIME INTERVAL
TIME BASE REFERENCE
PERIOD
PERIOD
TIME BASE
MAIN GATE
RESET
IC 170 (74S74)
IC 172 (74S64)
IC 174 (7403)
IC 178 (7402)
IC 182 (4001)
IC 171 (74S112)
IC 180 (7442A)
IC 173
(7475)

PM 66xx

Testpoints 80 MHz input amplifier

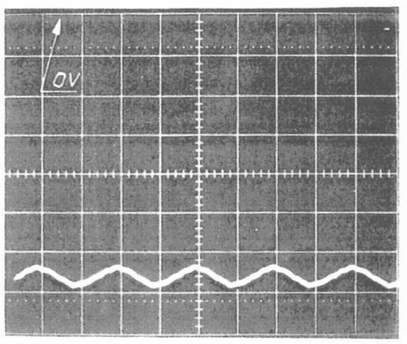
The waveforms are recorded with a 50 MHz oscilloscope PM 3250 including passive 1:10 probe PM 9350 and with the counter set to FREQUENCY 10 Hz, self CHECK mode and min. DISPLAY TIME.
Use figure XIII-2 to identify the location of the test points.

TP 1



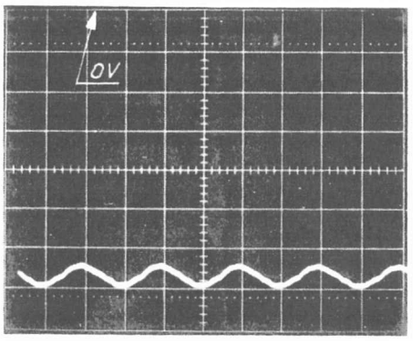
Normal input signal to input amplifier at IC 101:9.
Oscilloscope settings:
2 mV/div. and 50 ns/div. A.C. coupled.
Use 10 MHz OUT from the counter as trigger signal.

TP 2



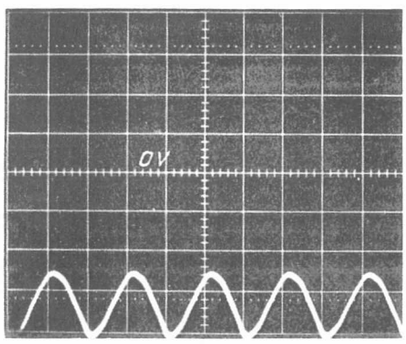
Inverted input signal to input amplifier at IC 101:6.
Oscilloscope settings:
200 mV/div. and 50 ns/div.

TP 3



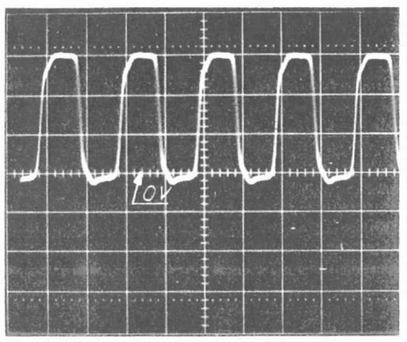
Normal input signal to input amplifier at IC 101:7.
Oscilloscope settings:
200 mV/div. and 50 ns/div.
Use 10 MHz OUT from the counter as trigger signal.

TP 4



Input signal to Schmitt-Trigger at IC 101:3.
Oscilloscope settings:
500 mV/div. and 50 ns/div.

TP 5



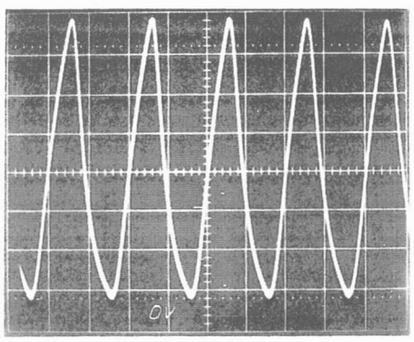
TTL output signal at collector of TS 105.
Oscilloscope settings:
1 V/div. and 50 ns/div.

PM 6612

Testpoints time base divider

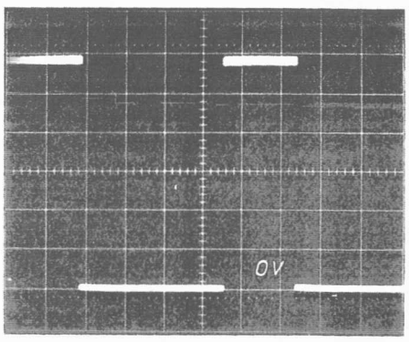
The waveforms are recorded with a 50 MHz oscilloscope PM 3250 including passive 1:10 probe PM 9350 and with the counter set to FREQUENCY 10 Hz, self CHECK mode and min. DISPLAY TIME.
Use figure XIII-2 to identify the location of the test points.

TP 6



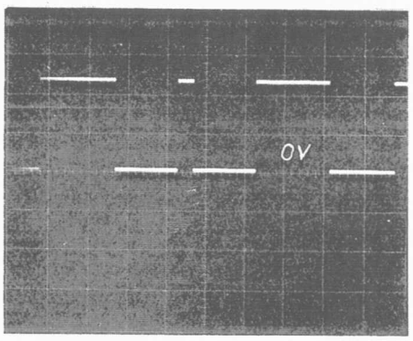
Time base divider input signal at IC 124:14.
Oscilloscope settings:
1 V/div. and 50 ns/div.

TP 7



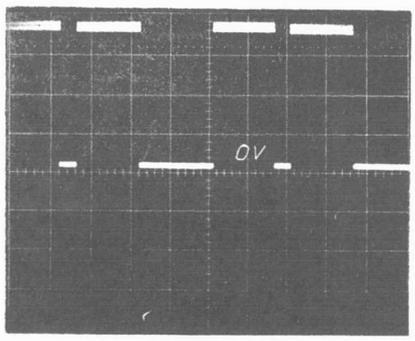
Time base preset signal at IC 124:12.
Oscilloscope settings:
2 V/div. and 50 ms/div.

TP 8



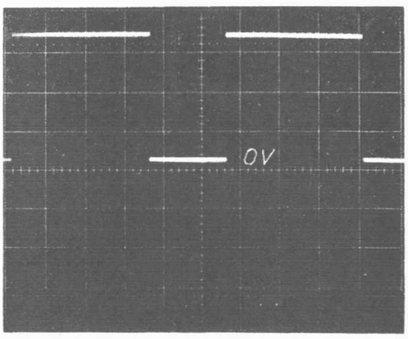
Time base signal at IC 125:18.
Oscilloscope settings:
5 V/div. and 50 ms/div.

TP 9



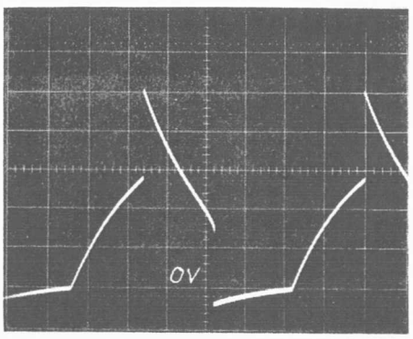
Time base signal at IC 183:3.
Oscilloscope settings:
1 V/div. and 50 ms/div.

TP 10



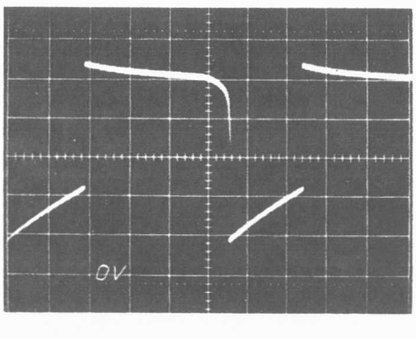
Main gate signal at IC 183:6.
Oscilloscope settings:
1 V/div. and 50 ms/div.

TP 11



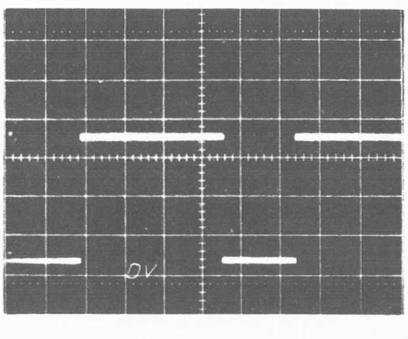
Display time triggering signal at IC 182:6.
Oscilloscope settings:
1 V/div and 50 ms/div.

TP 12



Display time sweep signal at IC 177:9.
Oscilloscope settings:
1 V/div. and 50 ms/div.

TP 13



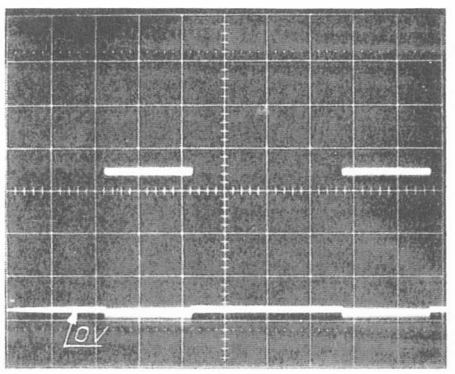
Reset signal at IC 178:2.
Oscilloscope settings:
1 V/div. and 50 ms/div.

PM 66 12

Testpoints decimal counting unit and display

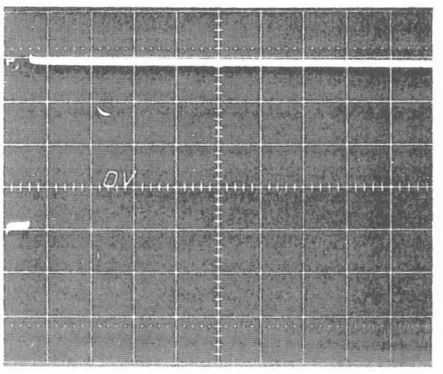
The waveforms are recorded with a 50 MHz oscilloscope PM 3250 including passive 1:10 probe PM 9350 and with the counter set to FREQUENCY 10 Hz, self CHECK mode and min. DISPLAY TIME.
Use figure XIII-2 to identify the location of the test points.

TP 14



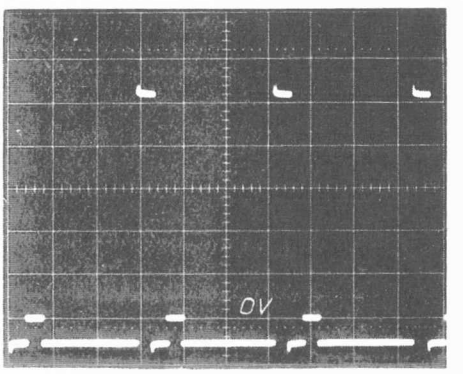
ted input signal at IC 172:8.
Oscilloscope settings:
1 V/div. and 50 ms/div.

TP 15



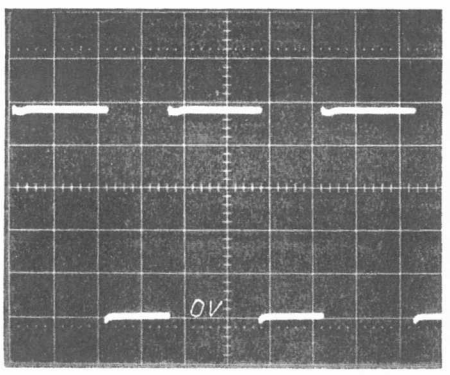
Carry signal $1:10^5$ at IC 176:14.
Oscilloscope settings:
2 V/div. and 2 μs/div.

TP 16



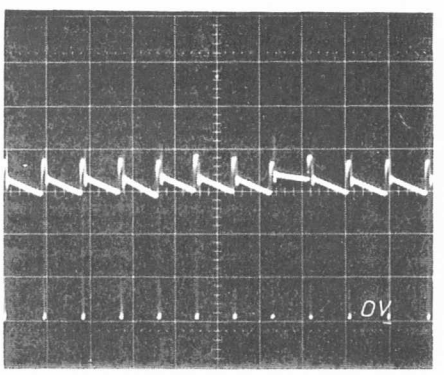
Data A signal at IC 174:3 when last digit is zero.
Oscilloscope settings:
1 V/div. and 0.5 μs/div.

TP 17



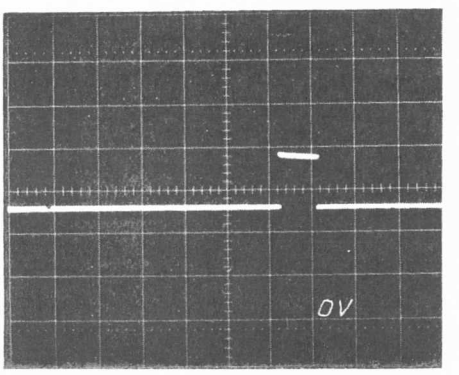
Display clock signal at IC 177:15.
scilloscope settings:
1 V/div. and 50 μs/div.

TP 18



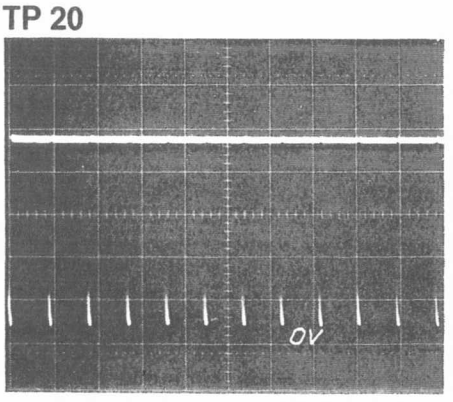
Display cathode signal at IC 181:16 when last digit is zero.
Oscilloscope settings:
20 V/div. and 0.2 ms/div.
Use signal at IC 179:11 as trigger signal.

TP 19



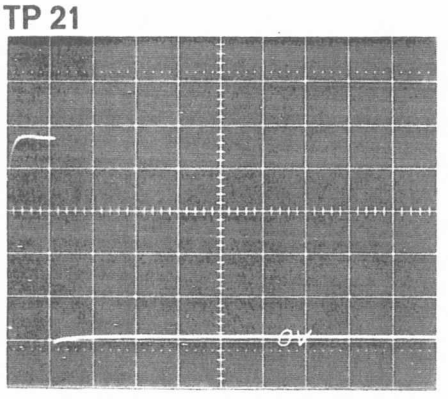
Display anode signal at cathode of GR 181.
Oscilloscope settings:
50 V/div. and 0.2 ms/div.
Use signal at IC 179:11 as trigger signal.

TP 20

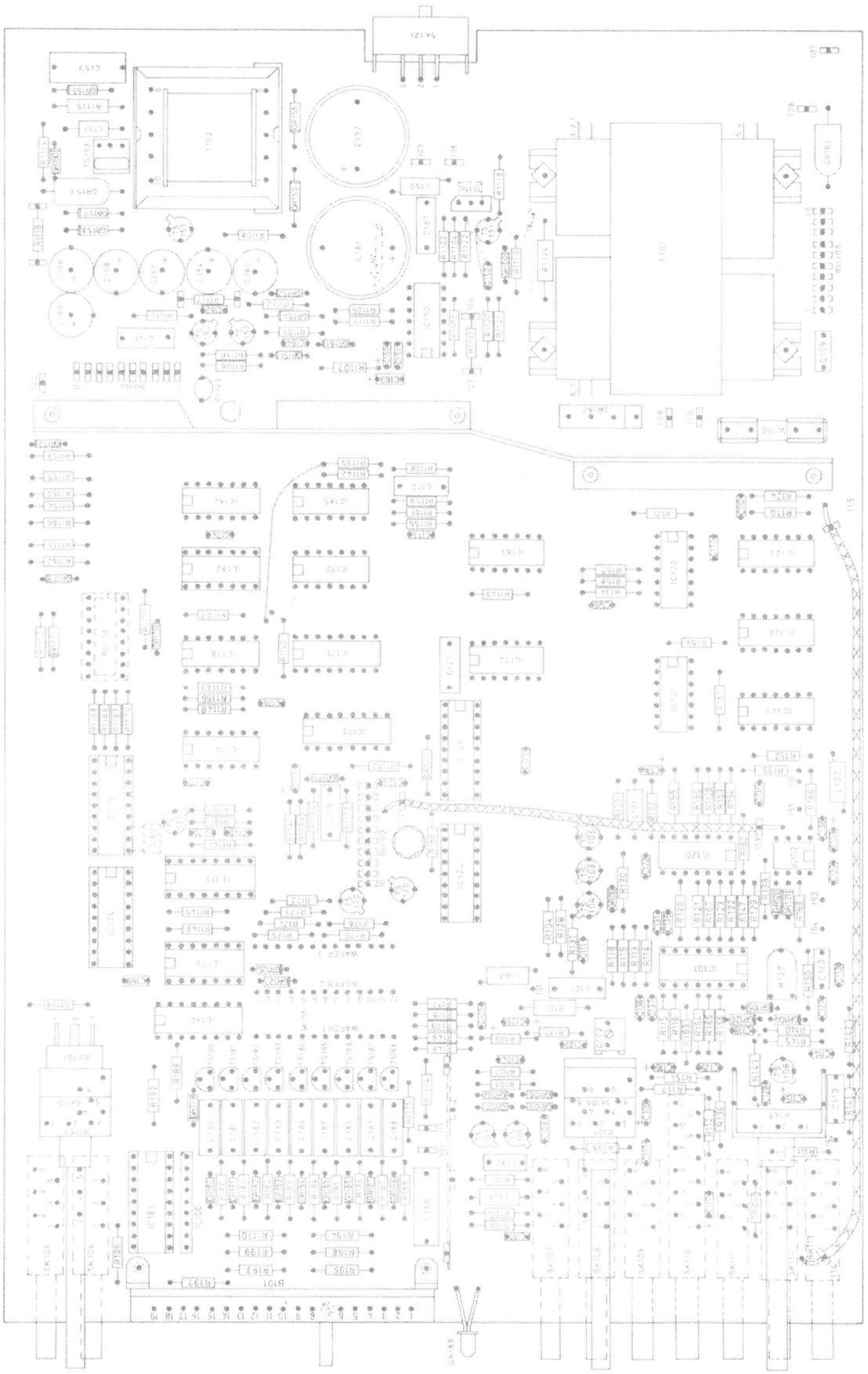


Display blanking signal at collector of TS 139.
Oscilloscope settings:
1 V/div. and 0.2 ms/div.

TP 21



Transfer signal at IC 175:9.
Oscilloscope settings:
1 V/div. and 5 μs/div.



Component layout for instrument with serial number SM 2.