ARCHIEF DOCUMENTATIEDIENST NVHR

Ned. Ver. v. Historie v/d Radio

Mains
230 V / 115 V } 50... 400 Hz
Power Transformer
Ext. Batt.
Int. Batt. Off Mains/Ext. Batt
Internal Battery PM 9673
Stand By Power to PM 9679, PM 9690
Stand By Lamp
On
Stand By
DC DC
+120V +12V +5V -5V -30V

Display Clock & Scanner Address Counter
4
1 of 10 Decoder
9
Anode Drivers
9
7-Segment Display
8
7-Segment Cathode & DP Decoder-Driver
4
BU 106 BCD
Battery Low

DECIMAL COUNTER
Main Gate
80 MHz Schottky Decade & Latches
LOCMOS Quad Decade
LOCMOS Quad Decade
MUX
Reset Transfer

Gate/Stand By
Stand By
Gate MV
Display Time
Main Gate FF
Display FF
Transfer & Display Time
Start/Stop
Memory
Reset

Input A
Pull For x 20
Att. x 20
BR101-106
TS101, 102
LIM
< 100 KHz
Sensitivity
Waveform Check & Channel Selector
ECL / TTL
To Time Base Div.
10 MHz Check Signal
<10MHz
Prescaled Signal *)

UNIT U2 HIGH FREQ. PRESCALER
Input B
Att. 6dB
Pre-Attenuator
PIN Att.
Attenuator
PIN Att.
Divider *)
Pre-Detector
Alt. Control Ampl.
Detector Level Comparator
Enable
Pre-Att. Control
Att. Control
Ref. Level
Supply Switch
+12V, -5V
Channel B Selector
*) PM 6613 ÷ 4
PM 6614 ÷ 8
PM 6615 ÷ 16
Time Base Divider *)

Oven Stand By Power
Ext./Int. SK131
Osc. 10 MHz
Input C
Ext. Std. & Ratio Input
10 MHz Out
Function Switch
Period / Period Selection
Reset Sync.
Channel Selector A, B
MUX
TB1
TB2
TTL / LOCMOS
LOCMOS Quad Decade
LOCMOS Quad Decade
LOCMOS / TTL
MUX
2
3
3
1
Time Base & Multiplier Control

Figure XIII-1. Block diagram

TIME BASE REFERENCE OSCILLATORS
PM 9677
PM 9678
PM 9679
PM 9690

+11...25V
10 MHz
+12V

TIME BASE REFERENCE
PERIOD
PERIOD
TIME BASE
COUNT A
MAIN GATE
TO R1140

From 80 MHz Input Ampl. A2

R151 1K
R162 47K
IC120
R154 1K
R1129 120K +5V
R163 1K
GR120 BAW62
GR121 BAW62
R155 10K +5V
R171 47K +5V
R172 10K +5V
1/4 IC122
1/4 IC123
1/2 IC121
C127 2p2
R150 10K
C120 22n
C123 10n
R153 1K
R152 220
BU24 INPUT C
BU25 10 MHz OUT
INT. EXT SK22

C179 10n
R159 47K +5V
R161 10K +5V
1/2 IC121
1/4 IC122
1/4 IC123
+10.6V
R158 1K
R134 1K
R157 47K +10.6V
TS120 2N2369
R160 10K
Tp6
Tp7
Tp8
IC124
IC125
GR123 BAW62
GR124 BAW62
SK105 WAFER 3
R164 47K +10.6V
R165 47K
R166 47K
R167 47K
SK105 WAFER 2
R170 10K
R169 10K
R168 10K +5V
BU106 13 12 11 UNIT CODE

1/4 IC123
PM 6611 only +5V
R1131 10K
1/4 IC26
1/4 IC178
R1150 10K
1/4 IC183
R1151 10M
R1149 47K
Tp10
Tp9
1/4 IC184
R1153 47K +5V
START/STOP MEM.
SK
SK111 4
BU108 4 6 2 3
RESET PRESCALER TB2 TB1

IC 120 (75107) +5V -5.2V
IC 121 (7451)
IC 122 (7403A)
IC 123 (7400)
IC 126 (7402)
IC 178 (7402)
IC 182 (34001)
IC 183 (74S74)
IC 184 (7400)
IC 185 (7402)
+5V

TOP VIEW +10.6V
IC 124 (6ZF 1201)
IC 125 (6ZF 1201)
IC 177 (4049) (Selected) +5V

SK105

MODE		PINS CONNECTED WAFER 2	PINS CONNECTED WAFER 3
COUNT A		1-2	1-3-10
FREQ A MHz	100 Hz	1-2-4	2-3-4-10-12
	10 Hz	1-4-5; 3-6	1-4-5-10
KHz	1 Hz	1-4-5; 3-6-7	2-5-6-10
	0.1 Hz	1-5; 3-6-7	6-10
PERIOD A µs	n = 1	1-8; 3-7	8-10
	n = 10^2	1-8-9; 3-10	7-8-9-10
	n = 10^4	1-8-9; 3-10	9-10
RATIO A/B or B/C	n = 10^2	1-9-11; 3-10	7-10-11
	n = 10^4	1-11-12	10-11

SK105			
. MODE		PINS CONNECTED	
		WAFER 2	WAFER 3
COUNT A		1-2	1-3-10
FREQ A	MHz 100 Hz	1-2-4	2-3-4-10-12
	MHz 10 Hz	1-4-5; 3-6	1-4-5-10
	KHz 1 Hz	1-4-5; 3-6-7	2-5-6-10
	KHz 0.1 Hz	1-5; 3-6-7	6-10
PERIOD A µs	n = 1	1-8; 3-7	8-10
	n = 10^2	1-8-9; 3-10	7-8-9-10
	n = 10^4	1-8-9; 3-10	9-10
RATIO A/B or B/C	n = 10^2	1-9-11; 3-10	7-10-11
	n = 10^6	1-11-12	10-11

Figure XIII-4. Circuit diagram, time base divider

BU105
BATTERY LOW
3
+5V
C177 10n
C140 2n2
TS139 BC557
Tp20
+120V
101
R1175 2K2
C189 330n
R189 470
R190 4K7
R191 22K
R192 6K8
DATA
A B C D
BU106
7 9 6 8
DISPL. CLOCK
DEC. POINT
ADDRESS D
BU106
4 14 3
-50V
Tp17
IC174
Tp16
Latch FF IC173
Decoder 1/4 IC178
IC181
A B C D DP
R1143 10K
C176 100n
+5V
R1167 1K8
R1168 1K8
R1169 1K8
R1170 1K8
C170 100p
R1144 820K
1/6 IC177
IC179
IC180
Main Gate IC172
From 80 MHz Input Ampl.
A1
Tp14
+5V
C178 10n
R1140 10K
+5.7V
Tp15
Tp21
-2.1V
IC 175 GZF 1201
IC 176 GZF 1201
R1145 10 K
R1146 10 K
1/4 IC182
R1165 10K
R1166 10K
1/2 IC170
1/2 IC171
1/2 IC171
1/2 IC170
80 MHz Decode
TO IC183: 10
TIME BASE REFERENCE
PERIOD
PERIOD
TIME BASE
MAIN GATE
RESET
IC 170 (74S74)
IC 172 (74S64)
IC 174 (7403)
IC 178 (7402)
IC 182 (34001)
IC 171 (74S112)
IC 180 (7442A)
IC 173 (7475)
IC 177 (4049) (Select)
TRANSFER
RESET
IC 179 (74.90)
IC 181 (8884)

BU105
BATTERY LOW
+5V
C177 10n
C140 2n2
TS139 BC537
Tp20
R190 4K7
R191 22K
R192 6K8
+120V
101
C189 330n
R1175 2K2
R189 470
GR180 BAV20
GR181 BAV20
GR182 BAV20
GR183 BAV20
GR184 BAV20
GR185 BAV20
GR186 BAV20
GR187 BAV20
GR188 BAV20
TS180 BS568
TS181 BS568
TS182 BS568
TS183 BS568
TS184 BS568
TS185 BS568
TS186 BS568
TS187 BS568
TS188 BS568
Tp19
C180 68n
C181 68n
C182 68n
C183 68n
C184 68n
C185 68n
C186 68n
C187 68n
C188 68n
R180 15K
R181 15K
R182 15K
R183 15K
R184 15K
R185 15K
R186 15K
R187 15K
R188 15K
-50V
B101 BR09253
Tp18
R194 2K2
R195 2K2
R198 2K2
R1130 2K2
R199 2K2
R196 2K2
R197 2K2
R193 2K2
IC90 8×470K
GR179 BZX79-C5V1
DATA
BU106
A
B
C
D
DISPL. CLOCK
DEC. POINT
ADDRESS D
BU106
Tp16
Tp17
IC181
IC170
R1143 10K
C176 100n
+5V
+5.7V
R1167 1K8
R1168 1K8
R1169 1K8
R1170 1K8
R1144 820K
C170 100p
1/6 IC177
1/6 IC177
1/6 IC177
IC179
IC180
R1145 10K
R1146 10K
Tp15
Tp21
-2.1V
IC 175 GZF 1201
IC 176 GZF 1201
1/4 IC182
≥1
R1165 10K
R1166 10K
+5V
R136 47K
5K105 WAFER 1
COUNT A
TRANSFER
RESET

5K105		
MODE		PINS CONNECTED ON WAFER 1
Count. A		1 - 2
Freq. A MHz	100 Hz	3 - 4
	10 Hz	3 - 5
	1 Hz	3 - 6
KHz	0,1 Hz	3 - 7
Period A µs	n = 1	3 - 8
	n = 10²	3 - 9
	n = 10⁴	3 - 10
Ratio A/B, B/C	n = 10²	3 - 11
	n = 10⁴	3 - 12

IC 173 (7475)
IC 177 (4049) (Select.)
IC 179 (7490)
IC 181 (8884)

Figure XIII-5. Circuit diagram, decimal counting unit and display

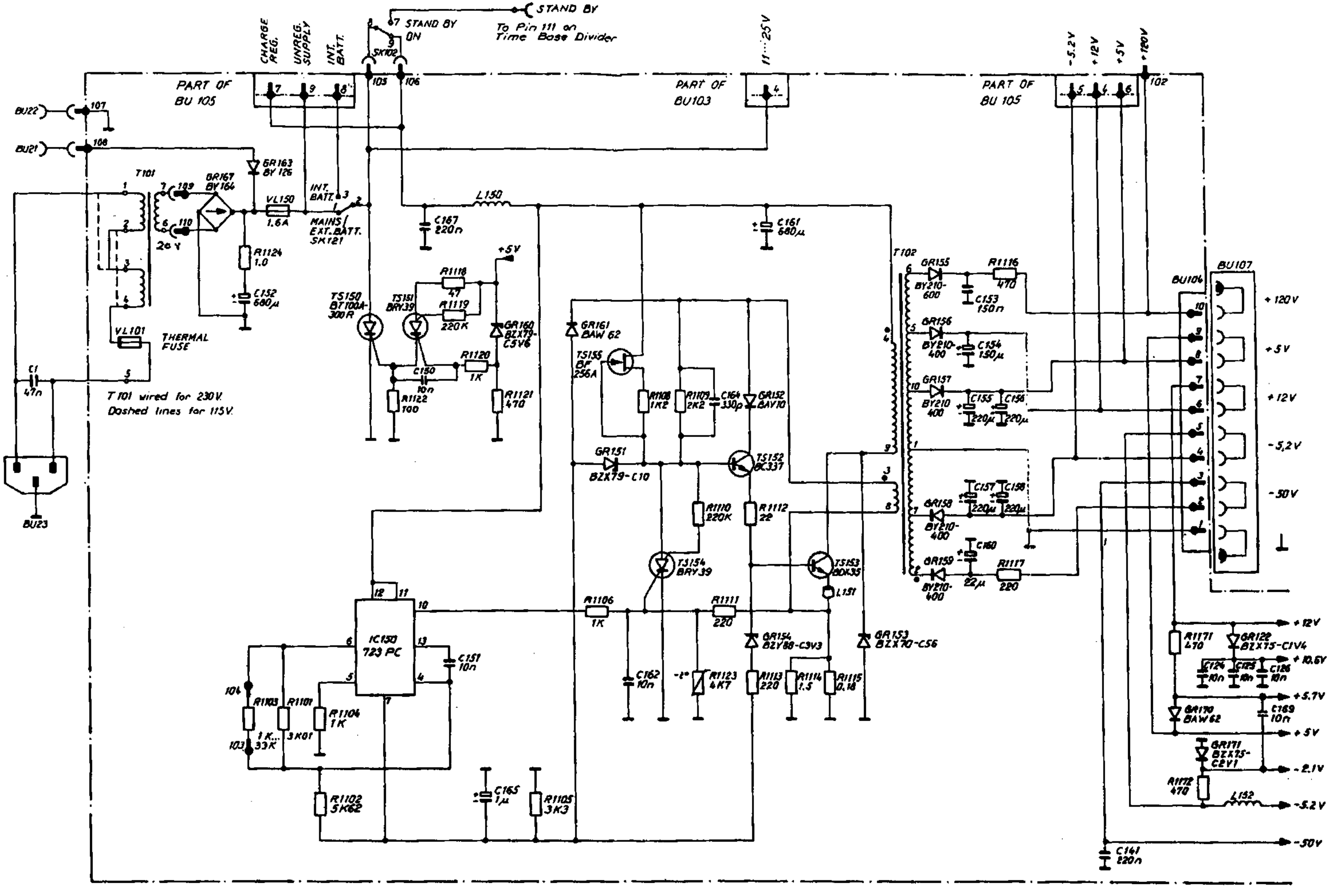


Figure XIII-6. Circuit diagram, power supply

Input B

Input Voltage at BU2	Input Freq at BU2	Measured Voltage
-40 dBm	200 MHz	-3 V
-20 dBm	200 MHz	+0.5 V
-10 dBm	200 MHz	+2 V

* measurable input signal at BU2

Figure XIII-14. Circuit diagram, unit 2 PM 6615