ROHDE&SCHWARZ

Instruments
Division

Service Manual

LEVEL METER
NRVD

857.8008.02

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Supplement to Service Manual
Power Meter
NRVD

Page 6.8, line 7: Replace line **12450** by line **12350**.

Page 6.12, first paragraph after Fig. 6-8 , add the following text:
"In the case of power meter <1> (NRVD), the correction factor at 50 MHz can be entered subsequently.

Page 6.10, add the following section:

6.3.4.3.1 Error Messages after Power-up of the NRVD

The selection of the desired test section (menu, Fig. 6-3) is followed by the request to enter the IEC-address of the NRVD, which is then checked. Should error messages result from the NRVD power-up sequence (missing RAM- or calibration data), the program suggests an appropriate remedy (restoring the RAM data or calibration).
The suggestions need not be followed even when calibration data are missing. Instead, verify the characteristics of the uncalibrated NRVD.

In the case of instruments not fitted with the NRVD-B2 option and missing calibration data it is also necessary to calibrate the DC(FREQ) input.

To this end, connect the calibrator to the three-contact connector X103 on the analog board (prompt). Selection of "Complete NRVD <7>" (menu, Fig. 6-10) causes the DC(FREQ) input to be verified or calibrated automatically.

In already calibrated instruments with NRVD-B2 option (no error message DEVICE ERROR *008 after execution of the power-up sequence), the DC(FREQ) input is not verified in automatic test runs ("Complete NRVD <7>" (menu, Fig. 6-10). The verification report reads "Option not included" as is stated after the DC output.

By a subsequent, selective verification "DC(FREQ) Input <4>" (menu, Fig. 6-10), the DC(FREQ) input can be checked and calibrated without the NRVD-B2 option fitted. The results are entered correspondingly in the report.

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6 Complete Instrument

This service manual for the power meter NRVD is included in the service kit NRVD-S1. The main section 6 - Repair of the Complete Instrument - focusses on the calibration of the power meter NRVD and on checking the instrument features including a list of the test instruments and utilities required. Section 7 describes the functions of the analog components of the analog board A2 and the filter board A4 and explains in detail the utilities provided for diagnostic and service purposes. Removal of boards or measures to be taken with replacement are finally treated.

Execution of the service works mentioned in Section 6 is supported by the calibration software supplied.

Contents of the service kit NRVD-S1 (order No.: 1029.2802.02):

- Service Manual (order No.: 0857.8895.24) including layouts of the individual boards, circuit diagrams, description of the implemented service functions and diagnostic means including hints for troubleshooting as well as explanation of the calibration procedures.
- Cal adapter (order No.: 0350.7818.02) for calibration of the NRVD via the interfaces of the power sensors.
- 5.25" floppy disk (1.2 MB) + 3.5" floppy disk (1.44 MB) (order No.: 1029.2850.00) for PAT/PSA (R&S) and IBM-AT controllers and compatibles. The floppy disks contain the subsequent software:

INST_D.BAT	Installation program
R&S BASIC	BASIC interpreter with BASIC drivers
CAL_D.BAS	Calibration program (cf. 6.3.4.3)

Installation of the above-mentioned programs is described in Section 6.3.4.3.

6.1 Function Description of Complete Instrument

(cf. circuit diagram 857.8150.01, block diagram 857.8008.01)

The power meter NRVD is designed as dual-channel power meter. The two test channels are completely independent of each other. The NRVD, in conjunction with a variety of probes and insertion units which can be connected, allows for precise evaluation of the signals applied from the kHz range up to the GHz range. The DC probe URV5-Z1 is provided for DC voltage measurements.

Realization of the measuring functions has been distributed on various boards, as shown by the block diagram of the complete instrument (cf. 857.8008.01).

Since the two test channels -A- and -B- are nearly identical, only the signal routing in channel A is described in detail. What is valid for measuring channel A analogously applies for channel B.

The measuring signal is received by the power sensor and converted into a DC voltage which is proportional to the measuring signal. The square-law region of the diode characteristic of the power sensor is used with small signals, the rectified output voltage is proportional to the applied measuring power. With large measuring signals, the power sensor diode works in the linear range and the output voltage is proportional to the applied measuring voltage. High accuracy across the entire dynamic range (nW to W) is achieved by storing all diode-specific data concerning transfer function, frequency response and temperature dependence in a non-volatile memory. This memory is part of the power sensor. All power sensors are provided with a temperature sensor for correction of the temperature dependence of the measuring diode. The current temperature of the power sensor is taken into account with evaluation of the measured values in the basic unit. The features of the temperature sensor are also stored in the non-volatile memory of the power sensor.

The output voltage of the thermal power sensors is always proportional to the power of the measuring signal applied due to the function of the instrument transformer. It depends on the type of power sensor whether the DC voltage supplied at its output is provided bipolar or unipolar referred to the ground reference of the instrument amplifier in the basic unit.

Evaluation of the output voltage of the power sensor is performed in the basic unit NRVD. The input interface of the basic unit is designed as easy-to-handle pin connection and allows for fast adaptation to the measuring task by simply replacing the power sensors. It depends on the type of probe, whether the DC measuring voltage is further amplified by the AC amplifier (all RF probes) or by the DC amplifier (DC-probe URV5-Z1). Subsequently, the amplified voltage is routed via an analog multiplexer to the integrated A/D converter. The A/D converter has been realized to a great extent as customer-specific circuit. Besides, this circuit contains further circuits for monitoring the input interface of the NRVD as well as bi-directional serial multiplexers. These multiplexers are used for data transfer between the controller board A1 and the analog board (A2) as well as for data exchange between the analog board and the power sensors connected. This procedure allows for transferring the calibration data of the active power sensors into the non-volatile memory of the power sensor and store them without using any special programming devices, only by means of the basic unit NRVD and a controller (cf. 7.1.3.4.4). The monitoring logic realizes changes of power sensor and adapts the power supply from the NRVD to the respective power sensor.

All power sensors connectable are supplied with + 5 V for reading of the power sensor data. The power supply is subsequently switched off with passive power sensors, with active ones, the voltage supply is switched to + 12 V/-12 V. With each replacement of a power sensor, the monitoring logic switches off all voltages for the channel concerned.

The basic unit NRVD is equipped with a test generator for testing the RF probes. The 50-MHz sinewave signal is provided with a power calibrated at 1 mW at the generator output (N-socket on the front panel) for test purposes. The test generator is switched on and off via menu keys.

The frequency information for frequency correction of the RF probes used can be transmitted to the basic unit as frequency-proportional DC voltage via the BNC socket "DC(FREQ)" (I/O Option NRVD-B2) or as numeric data via the IEEE-488 interface. Both connections are provided on the rear panel of the basic unit. The IEEE-488 interface also allows for remote control of the NRVD. The kind of communication can be switched over according to SCPI or IEEE488-1 (IEC 625-1) recommendations [SCPI/URV]. Thus, problem-free operation of the NRVD is possible even in earlier test systems without considerably modifying already existing operator routines.

If the input/output option NRVD-B2 is used, the test signal evaluated in the basic unit is provided as analog voltage at the output DC1 of test channel A and at the output DC2 of test channel B on the rear panel. The DC voltage provided is proportional to the bar graph indication. The left dead stop corresponds to 0 V, the right full-scale value on the bargraph scale is assigned 3 V. The analog outputs can also be shown on the scale by corresponding selection of the indication range (cf. operating manual, Section 3.3.2). The measuring start can be initiated also by external hardware via the trigger input. Performance of the triggered measurement is indicated by the TTL signal at the trigger output (both BNC sockets on the rear panel).

The controller module A1 controls the communication with the NRVD environment via the IEEE-488 interface, the control of the front panel, the communication with the analog board, non-volatile storage of the calibration data and the instrument settings, post-processing of the measured values as well as the power supply of the complete instrument (cf. description of the controller). The power connector of the NRVD is designed for all common voltages in the range from 90 to 264 V / 47 to 440 Hz.

Internal hardware tests of the digital and analog function groups are performed already with switching on the instrument and the results are displayed. Moreover, errors occurring during operation are displayed (cf. Section 4.3. about troubleshooting and diagnostic utilities in the operating manual).

The readout of measuring results, display of instrument state (operating mode, menu functions, IEEE state) as well as operating elements for manual operation have been concentrated on the display board A3 (cf. description of the board A3).

6.2 Required Test Instruments and Utilities

Table 6-1

Item	Type of instrument	Required specifications	Suitable R&S instrument	Order No.	Application
1	Cal-Adapter	special NRVD interface	Contained in service-kit NRVD-S1	0350.7818.02	6.3.4 6.3.5
2	DC-Calibrator [1]	±0.01/0.0195/.05 V ±0.1/0.195/0.5 V ±1/1.95/5/10/19.5 V; (0.005 %)	--	--	6.3.4 6.3.5
3	Digital multimeter [2]	Ohmmeter, meas range 1 MΩ, 0.015 % [3] DC; 0 to 10 V ±0.01 %	UDS5	349.1510.02	6.3.4 6.3.5
4	Power meter	1 mW ±0.4 % r<0.05 % (50 MHz)	NRVD + NRV-51, (-52) extra calibrated by R&S or PTP		6.3.4 6.3.5.4
5	DC probe	Special NRVD interface	URV5-Z1	395.0512.02	6.3.4 6.3.5.5
6	BNC cable				
7	Controller	IEC-625 interface, IBM compatible	PSA/PAT-fam.		6.3.4 6.3.5
8	Printer		PDN	351.4512	6.3.4
9	IEC-bus cable		PCK	292.2013	6.3.4
10	Centronics cable	Centronics interface			6.3.4

1) Further specifications of the calibrator and instructions for customization of the software of the calibration kit NRVD-S1 can be looked up in Sections 6.3.2 and 6.3.3.

2) The digital multimeter is required for adjustment of the resistor in the calibration adapter. If no UDS5 is available, adjustment, i.e. check of the 1-MΩ resistor can also be performed without CPU control (cf. 6.3.5.1). Adjustment accuracy, however, considerably influences calibration (verification) accuracy.

3) Within limited temperature range 23 ± 1°C

6.3 Calibration

The service kit NRVD-S1 contains the calibration adapter, the service manual and a floppy disc, which contains the calibration program among others. The calibration program in conjunction with a DC calibrator, a digital multimeter and a power meter allows for complete calibration of the basic unit NRVD or extensive testing of specifications with regard to compliance with specified data.

Calibration of the basic unit NRVD is performed via the IEEE-488 interface by means of a process controller compatible with IBM-AT (e.g. R&S controllers of the PSA family). The I/O option NRVD-B2 can be retrofitted and, therefore, calibration can also be performed via the front panel of the NRVD.

The calibration procedure can optionally be controlled automatically or interactively step by step. Selection of the functions (calibration/verification/single ranges etc.) is comprised in the menus. A report of the measuring or calibration tasks performed can be output by a printer (e.g. PDN).

A detailed description of the required specifications of the DC calibrator is given in Section 6.3.2. The use of other test instruments which comply with the required specifications (cf. Section 6.2) with regard to integration into the existing calibration program is explained in Section 6.3.3.
Fig. 6-1 Test setup for calibration (verification) of the NRVD

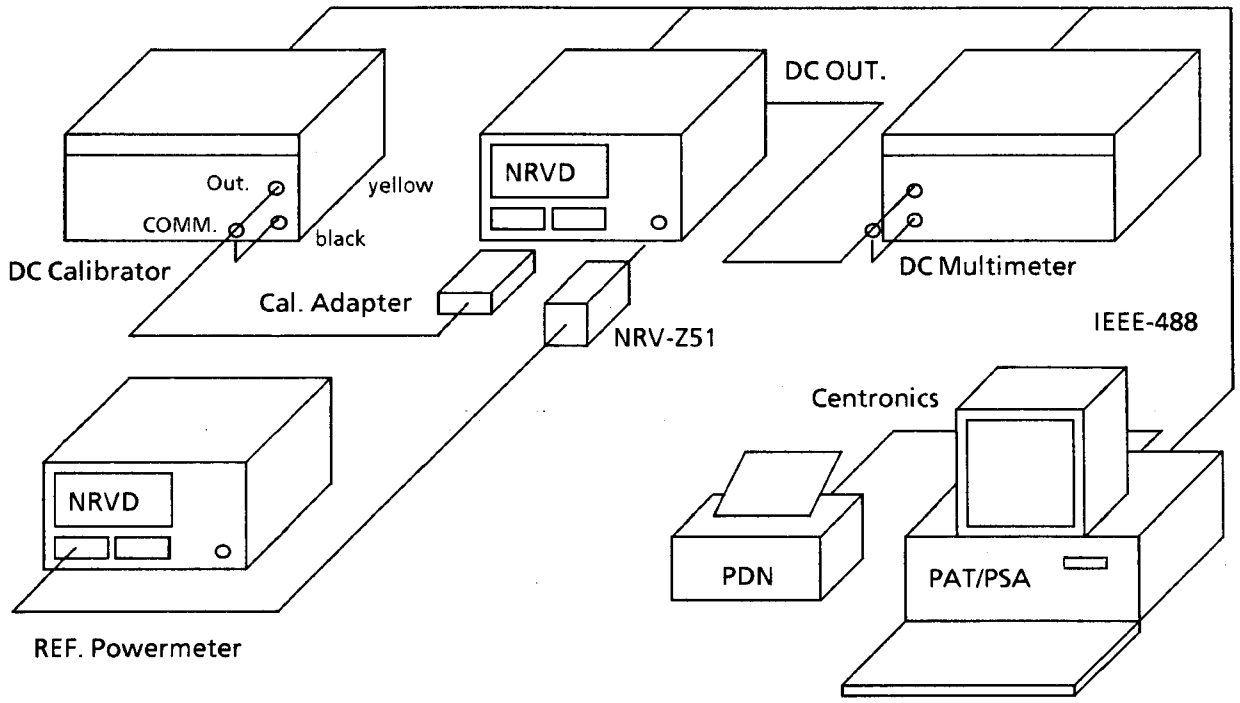


Fig. 6-1 Test setup to calibrate (test) the NRVD.

6.3.1 Calibration (Verification) of the NRVD

This section briefly illustrates the calibration and test procedure used for the NRVD.

Test probes of the NRVD convert the input parameter (RF power, voltage) into proportional voltages or currents and pass them on to the basic unit, which is why verification and calibration of the amplifiers in the basic unit is performed in analog form by means of DC voltages. Each of the two test channels (A, B) is provided with a DC amplifier with 11 measuring ranges for the RF probes. Both channels are provided with a common current-voltage converter with 4 measuring ranges and input selection in the basic unit for the DC probe URV5-Z1.

Each of the two test channels has a separate input for measuring the output voltages of the temperature sensors of the probes connected.

All function groups or specifications to be calibrated are listed in table 6-2.

Table 6-2 Survey of calibrated specifications

Calibrated specification (group)	Cal command
AC amplifier + 11 meas. ranges [1]	CAL:AMPL AC, U_i
AC amplifier - 11 meas. ranges [1]	CAL:AMPL AC, U_i
DC amplifier 4 meas. ranges	CAL:AMPL DC, U_i
Input temperature sensor 0.1 mA [1]	CAL:AMPL TEMP, -0,3
Input temperature sensor 1.0 mA [1]	CAL:AMPL TEMP, -3,0
DC (FREQ) input [2]	CAL:AMPL FREQ, U_i
Test generator 50 MHz 1 mW/50 Ω	CAL:ROSZ SET_50 MHz, P_i
DC output (Option NRVD-B2) [1] [3]	CAL:AMPL OUTP, 0 [4]

1) Calibrated (verified) separately in each channel (A, B)
2) BNC input DC (FREQ) on the rear panel is part of the I/O option NRVD-B2. If this option is not fitted, the input can be calibrated at the connector X103 (3 + 1 way) on the analog board A2.
3) I/O option NRVD-B2
4) The DC outputs are calibrated interactively with reference to the DC (FREQ) input directly from the frontpanel of the NRVD (cf. 6.3.5.5). Software version 1.30 and later versions also allow for calibration via IEEE bus. The parameters 0 or 1 can be input to start the calibration procedure which is equivalent to that from the front panel, entering "2" only calibrates the D2 output.

The calibration voltage of the calibrator is applied to the respective measuring inputs via the CAL adapter. The latter contains two relays, which are set automatically by the basic unit according to the function to be calibrated (cf. circuit diagram 350.7818.01 - Cal adapter). The required calibration voltages of the individual measuring ranges are listed in the table 6-3. The current source required for calibration of the DC amplifier is replaced by the calibrated 1-MΩ resistor of the CAL adapter.

Calibration voltages of opposite polarity are required for calibration of the AC amplifier (cf. table 6-3). The power sensors NRV-Z3, -Z4, -Z7 as well as the insertion units URV5-Z2, -Z4, -Z7 have balanced outputs, the others are unbalanced and supply a unipolar test voltage. The AC amplifiers are designed as instrument amplifiers with two separate inputs, which are used either both (symmetrical) or individually. Due to the wide dynamic range each of the two inputs is provided with a voltage divider. Since the dividing factors of the two voltage dividers are different due to the different tolerances of components, both inputs (+ and -) must be calibrated and tested separately.

Each calibration step consists of two stages to avoid errors caused by offset voltages:

- The output voltage of the calibrator is set to zero in the same range as the subsequent rated value, if possible. The sum of the inherent offset voltage and the offset voltage of the calibrator is measured in the basic unit.

- The rated value is set on the calibrator according to table 6-3. Subsequently, the actual value (rated value + offset) is measured in the basic unit. The calibration factor is calculated from the voltage deviation and stored in the basic unit.

Table 6-3 Measuring ranges and calibration values of the analog inputs, T_A = 23 ± 1 °C

Calibrated function [1] [CAL command]	Pol.	Rated value Ui [V]	Permitted tolerance [%]	Max. offset [mV]	Measuring range
AC amplifier [CAL:AMPL AC, U_i] [2]	±	0.01	0.12	0.05	1
		0.02	0.12	0.05	2
		0.05	0.12	0.05	3
		0,10	0.12	0.05	4
		0.20	0.12	0.05	5
		0.50	0.12	0.2	6
		1.0	0.12	0.2	7
		2.0	0.12	0.5	8
		5.0	0.12	1	9
		10.0	0.12	2	10
		20.0	0.12	5	11
DC probe amplifier [CAL:AMPL DC, U_i] [2]	+	0.1	0.12	0.5	1
		1.0	0.12	0.5	2
		10.0	0.12	5	3
		40.0	0.12	50	4
Temperature sensor [CAL:AMPL TEMP, U_i]	-	0.300	0.1	1.0	---
		3.0	0.1	5.0	---
DC-FREQ [CAL:AMPL FREQ, U_i]	+	10.0	0.12	50	---

1) The calibration date must be entered in the calibration mode (not prior to the previous date). The date is not required for reading the calibration data.

2) U_i is entered with the polarity sign! Rated values Ui < = 100 mV: DC calibrator about 100 mV

When the DC(FREQ) input is used, the measured offset voltage is stored for the internal correction in addition to the calibration factor.

The required measuring accuracy is ensured even without adjustment of components by the correction values determined by calibration together with continuous meas.-value correction. The entry of the date of calibration protects the calibration data against erroneous destruction. The new date entered must not be prior to the latest calibration date.

Check or readout of the NRVD calibration data is possible without entering the date. In this case, the date requested by the program is only used for printout of the report.

All function groups of the NRVD, except for the I/O option NRVD-B2, can only be calibrated via the IEEE bus. Calibration of the retrofitted option is performed interactively via the operating menu of the NRVD. The user is only requested to provide for the required external connection between the DC output to be calibrated and the DC(FREQ) input (cf. 6.3.5.5).

6.3.2 DC Calibrator

The calibration and test routine for the NRVD supports the calibrators listed below:

- Analogic (Data Precision)
- Datron 4000
- Fluke 5700

With Analogic 8200, voltages < 104 mV must be tapped at the 100-mV output on the rear. The user is informed thereof by a message on the display during the program-controlled test run. If another DC calibrator is used, the following requirements must be met:

- Voltages according to Section 6.2 must be settable with the required accuracy.
- It must be possible to set the output voltage to zero in the relevant output voltage range (offset handling, cf. Section 6.3.1).
- All output voltages, irrespective of their polarity, must be available at one pair of clamps without changing the connections of the Cal adapter.
- The calibrator must be a current sink with a capacity of at least 2 mA (see fig. 6-2 with explanation) for the output voltages -3 V, -0.3 V, 0 V.
- The calibrator must be controllable via IEEE bus.

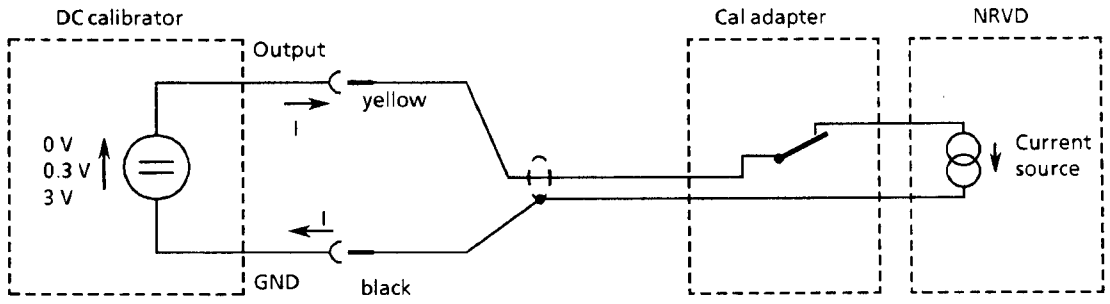


Fig. 6-2 Current conditions/ratio with calibration of the temperature sensor input

Except for calibration of the temperature sensor inputs, the Cal adapter connected to the basic unit represents a real load of 1 to 10 MΩ. With calibration or verification of the temperature sensor inputs, the measuring current supplied by the basic unit (cf. fig. 6-2, table 6-4) must be compensated without changing the output voltage of the calibrator.

With regard to this kind of load, it should be checked, whether the internal impedance of the calibrator used is low enough, such that the required voltage accuracy is still ensured.

Table 6-4 Calibrator load by the temperature sensor input

Calibr. range	Load current	
-0.3 V	100 µA	with offset determination (U_k = 0) in the calibration phase (U_k = -0,3 V)
-3.0 V	2 mA 1 mA	with offset determination (U_k = 0) in the calibration phase (U_k = -3 V)

6.3.3 Adapting the Software to Other Test Systems

DC calibrators:

Control variables of the three calibrators supported by the program are given in the control section 15420 to 15940 (variables for calibrator...). The control variables of another calibrator may replace one of these blocks.

The name of the calibrator should be entered in the lines 12270 to 12330, if required, and the address line of the modified block is to be entered in line 12450. The letter combination "An" is used in the program as identification for the output of notes about how to reverse the calibrator outputs with the type Analogic 8200.

If the IEEE address of the calibrator is different, it need not be corrected, since it is requested in the program run. Subsequently, it is checked, whether an instrument can be addressed at the given address.

Power meter:

The name of the power meter and the default IEEE-bus address are to be entered in the program lines 12730 to 12780. The IEEE bus address is offered in the program run and can be overwritten.

The destination address of the initialization routine is passed by means of the instruction ON Q GOSUB .. and must be entered in line 12920. The initialization routines provided are comprised in lines 11970 to 12120.

The test routine Pwmtr (12940 to 13020) contains the control commands of the power meter and is expanded analogously, if required.

6.3.3.1 Controller Requirements

- AT-compatible PSA/PAT controller (R&S) or IBM-PC
- IEEE-bus board and driver PAT-B1, order No.: 1007.1150.02
  (function-compatible with PCIIA/National)
- Parallel interface for connection of a printer (Centronics, LPT 1)
- Graphics card Herkules/EGA/VGA.
- Min. memory space: 250 kB RAM, 300 kB hard disk

6.3.4 Program-controlled Calibration/ Verification Measurement

6.3.4.1 General Remarks on Calibration

The test setup can be looked up in fig. 6-1. If a report of the test results is not requested, a printer is not required. The digital multimeter UDS5 is provided for adjustment of the CAL adapter. If a UDS5 is not available, the CAL adapter must be adjusted according to Section 6.3.5.1.

Note: *The ambient temperature during calibration should be 23 ± 1° C. The instruments used for calibration should be running for at least one hour. The power voltage must not deviate more than ± 10% from the rated value and relative humidity should not reach 80%.*

6.3.4.2 Installation and Start of the Programs Supplied

The calibration program CAL__D.BAS in the subdirectory \SER-D is written in R&S BASIC and is contained on the supplied floppy disk (service kit NRVD-S1) together with the required BASIC drivers and the installation program INST__D.BAT.

Started from the floppy disk, the program INST__D.BAT carries out the complete installation on the hard disk. First, all service programs are copied into the subdirectory C:\SER-D just created. The service programs only run in conjunction with the R&S BASIC interpreter. If the latter is not yet stored, it can now be installed. Therefore, the main program BASIC.COM is copied into the directory C:\RS-BASIC. All utility programs and drivers are stored in the subdirectory C:\SER-DRIV just created. The files AUTOEXEC:BAT and CONFIG.SYS are extended and the two original files are copied into the subdirectory "C:\RS-BASIC*.OLD".

Installation procedure:

- Insert floppy disk in drive A or B.
- Changeover to drive A or B: (C:\> A: (B:))
- Start the installation program: enter A:\>INST_D and press the ENTER key.
  The installation procedure is designed interactively.
- Remove the floppy disk from drive A (or B).
- Restart the controller system. (CTRL + ALT + DEL or STRG + ALT + ENTF).
  This action is indispensable, since it enables the computer to load all drivers required.
- Computer with Hercules graphics card installed:
  Prior to loading the BASIC interpreter the utility program HERCSUP.COM must be activated:
  enter C:\HERCSUP (from DOS level)
  or enter HERCSUP into the AUTOEXEC.BAT file.
- Change to the directory C:\SER-D and start R&S Basic (C:\> BASIC)
- Load the calibration program (LOAD "CAL_D").
  (Or press the function key F5 ("LOAD") and add CAL_D). The extension BAS is added automatically by Basic.

  Note: *Program names must be entered with the full pathname, if Basic was not started from C:\SER-D.*

- Start the program using the function key F2 or enter "RUN" and press the RETURN key.

6.3.4.3 Calibration program CAL__D.BAS

Program operation is mainly menu-controlled. The program continues with the next menu item by entering the identification character (letter or number) assigned to the desired program section. Letters can be uppercase or lowercase, pressing the RETURN key is only required with data entry.

Following program start (cf. 6.3.4.2), the program head with subsequent main menu is displayed for approx. 1.5 S:

Cal-Adapter Adjustment	<A>
Verification	<V>
Calibration	<C>
Calibration Faktors	<F>
Calibration Date	<D>
End of Programm	<E>

Fig. 6-3 NRVD calibration, menu 1

The sequence of sections in menu 1 is not a random sequence but corresponds to the usual calibration run.

- Before starting calibration or verification, the CAL adapter as test equipment should be checked with regard to accuracy of the 1MΩ resistor. Therefore, "Cal-Adapter Adjustment" →<A> is selected in menu 1. A detailed description of testing and adjustment is given in Section 6.3.4.4.
- The specifications of the EUT are determined by means of a verification measurement ("Verification" →<V>) prior to calibration. This allows for the user to decide, whether there is a fault or a drift within the permitted tolerance and whether the instrument will be subject to calibration. The procedure or special features of a verification measurement are described in Section 6.3.4.5.
- Calibration is initiated by entering C for "calibration". The procedure and differences compared to the verification measurement are explained in Section 6.3.4.7.
- The calibration factors substitute a hardware adjustment, which would be required otherwise and allow for a quick evaluation of the instrument state. Calibration factors determined with calibration are stored in a non-volatile memory in the NRVD and can be called under the menu item "Calibration Factors" <F>. The data are either displayed on the screen or output on a printer (Fig. 6-15). The sign ">" is used in the report to mark parameters which have been calibrated at the actual calibration date. Parameters calibrated prior to this date are not marked. The stored parameters of the manually calibrated DC outputs (from the frontpanel) are not provided with the mark (">").
- The menu item "Calibration Date" allows for calling the latest calibration date. It is absolutely required for calibration to enter the current date and this must be the latest calibration date.

6.3.4.4 Computer-controlled Adjustment of the Cal Adapter

The current source required for verification measurement and calibration of the DC amplifier is replaced by the calibrated 1-MΩ resistor of the Cal adapter in conjunction with the DC calibrator. The resistor data thus directly influences calibration accuracy. Its value (1000.0 ± 0.05 kΩ) must therefore be checked at regular intervals and readjusted, if necessary.

- Following program start, the option "Cal-Adapter Adjustment" <A> is selected in the main menu (cf. fig. 6-3).

  Subsequently, the required test setup is displayed (cf. fig. 6-4). After acknowledgement of the correct setup by <SPACE key> the program checks via the IEEE bus, whether the required instruments (NRVD + UDS5) are available and determines their IEEE-bus addresses for further program run. In case of an error (e.g., UDS5 was not found) the program waits until the error has been eliminated (UDS5 is identified after acknowledgement of performed test-setup correction by <Space key>.

Attention: The accuracy of the UDS5 considerably influences adjustment, which is why the calibration date of the UDS5 used should not be earlier than one year from the date of adjustment.

Note: *If two instruments with the same IEEE-bus address have been found, a message is output in the monitor line and the program waits until correction has been acknowledged.*

If the NRVD is identified more than once, a warning is read out in order to prevent the EUT to be confused with the calibrated power meter with calibration. With verification measurement or calibration, selection of the power meter is requested by the program in the first run.

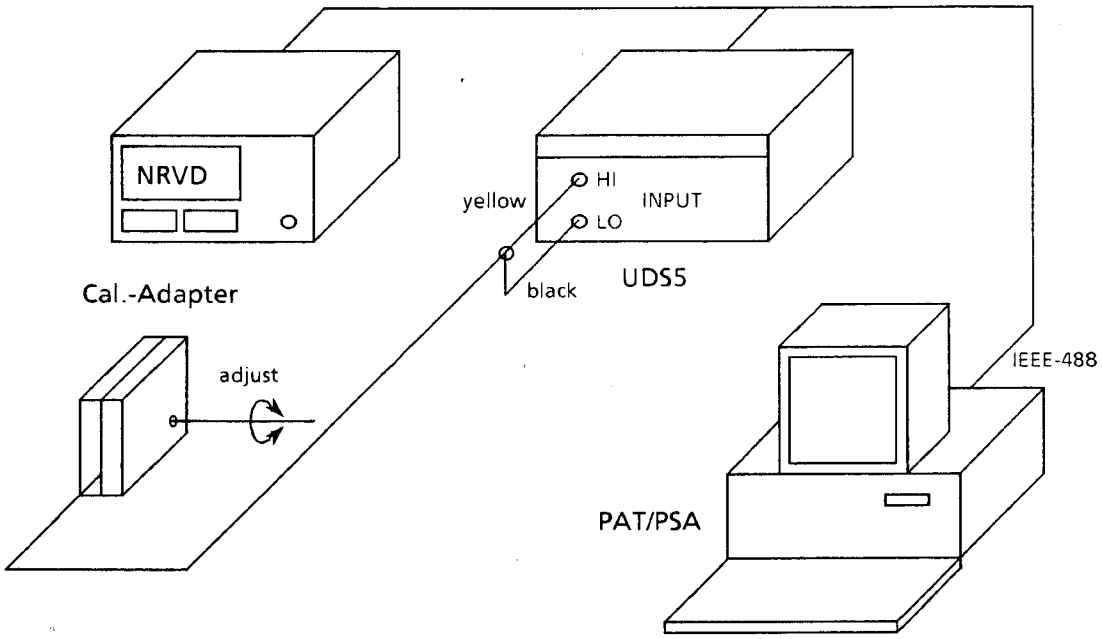


Fig. 6-4 Test setup for adjustment of the Cal adapter

Further operation depends on the test run and becomes a dialog:
Upon acknowledgement of the realized test setup displayed, the user is requested by the program to connect the Cal adapter to channel A of the NRVD[1]. The program automatically configures the Cal adapter for measurement of the 1-MΩ resistor/shunt and requests removal of the Cal adapter from the NRVD and connection of the Cal adapter inputs (yellow/black banana plugs) to the UDS5 [1]. Execution of the program instructions is checked and the resistance value is displayed. The measured value is marked, if the resistance value is beyond the tolerance (cf. fig. 6-5).

Cal-Adapter Adjustment
999.95 < 1000.01 < 1000.05 Return to Main-Menu with <R>

Fig. 6-5 Cal adapter adjustment

According to the display instructions, adjust the trimming resistor of the CAL adapter such that the resistance is within the tolerance range displayed. The potentiometer for adjustment of the 1000-kΩ resistor is accessible via a hole in the Cal adapter housing (cf. fig. 6-4).

Terminate adjustment by pressing the key → "R" for return to the main menu.

1) not applicable, if already performed

6.3.4.5 Verification

Upon selection of the option "NRVD Verification" by pressing the key "V" ("v"),
a verification run is initiated. All function blocks are measured by the verification measurements. However, the verification measurement does not influence the stored calibration data of the NRVD.

After selection of the verification measurement, the program determines addresses of available instruments with corresponding messages in the monitor range on the screen. First, the test setup (cf. fig. 6-1) is displayed. After acknowledgement of correct setup, the measuring instruments supported by the program are selected:

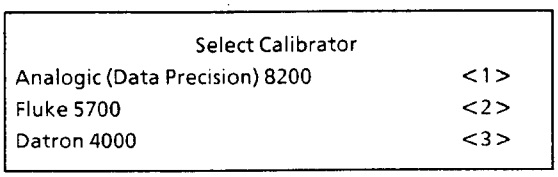


Fig. 6-6 NRVD calibration, selection of calibrator

In the next menu, the IEEE-bus address of the calibrator selected is recommended. The offer or a new entry (terminate by "Return") is accepted and, immediately following the entry, it is checked, whether an addressable instrument is available at the given address. If this is not the case, an error is signalled acoustically and correct entry is waited for.

Analogously, a power meter supported by the program is specified in the subsequent menu:

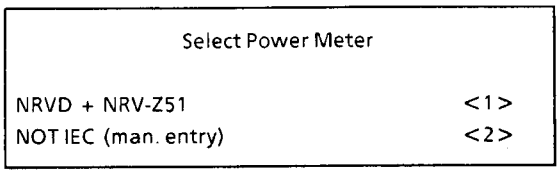


Fig. 6-7 NRVD calibration, selection of power meter

In the next menu, the IEEE-bus address of the power meter selected is proposed. The proposal or a new entry (terminate using "Return") is accepted and, immediately following the entry, it is checked, whether an addressable instrument is available at the given address. If this is not the case, an error is signalled acoustically and correct entry is waited for.

The instrument identification of the power meter (NRVD + NRV-Z51) is displayed, correct connection of the probe is checked and initialization is carried out (cf. fig. 6-8). If the result of the check is negative, the user is requested to correct, correct connection is acknowledged by "Sensor no error".

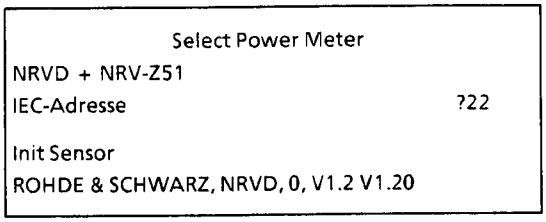


Fig. 6-8 NRVD calibration, selection of power meter

Analogously, the IEEE-bus address of the EUT is requested by the program.
The next menu offered by the program (cf. fig. 6-9) indicates the last calibration date of the EUT and requests for entry of the current test date, the name of the test engineer and information on the EUT (serial No., instrument version).

Starting with software version V1.30, the serial number of the instrument is contained in the instrument identification (cf. fig. 6-16). The entry is explained in Section 6.3.4.6.

The current test date is derived from the real-time clock of the controller, it can, however, be overwritten. The date is absolutely required for calibration and it must not precede the previous calibration date (otherwise, no calibration is possible, error messages). With verification measurement, the date is required only for the report.

NRVD Calibration (Last calibrated 1991, JUL, 31)	
Date (dd. mm. yy)	?21. 11. 92
Tested by (Name)	?Fuchs
NRVD Serial No.	?101324/001
NRVD Var.	857.8008.?02

Fig. 6-9 NRVD calibration, administration data

Subsequently, the user determines the extent of the verification measurement (cf. fig. 6-10). If the complete measurement <7> is selected, the verification procedure is only interrupted by requests for reconnecting the Cal adapter or for connecting the DC(FREQ) input to the current DC output. The procedure is continued after the execution of the respective request has been acknowledged and verified. In contrast to calibration, the DC amplifiers in both channels are checked.

When the verification measurements have been performed, the results can be either displayed or output on a printer in the form of a report (cf.6.3.4.8) or stored as ASCII file.

Note: *A verification measurement should be performed before the calibration measurement in order to store the actual state of the NRVD.*

The drift compared to the latest calibration can thus be evaluated and repair of a faulty instrument is not replaced by a calibration which could be avoided.

6.3.4.6 Entry of Serial No.

Starting with the software version 1.30, the serial No. of the NRVD is contained in the instrument identification (cf. figs. 6-8, 6-16). The entry of the serial number is made with first calibration of the NRVD and cannot be modified any more. The entry (starting with software version 1.30) can be made with a later calibration, if the serial number entered is 0. The serial number of the EUT is derived directly from the NRVD identification and entered in the menu 2 (administration data) by the calibration program, taking into account the software version. If the serial No. cannot be read from the identification, it must be entered. It consists of max. 11 characters, digits (0 to 9) and one special character ["/", "." and " " (space)] may be entered.

6.3.4.7 Calibration

The inherent calibration is initiated in the main menu (cf. fig. 6-3) by entering "C". The sequence of menus offered is similar to that of the verification measurement. If a calibrator or reference power meter has already been selected, the program checks whether it is correct and continues with the next step up to selection of the calibration extent (cf. fig. 6-10).

When entry of the administration data has been terminated, the required test setup for the test path selected in menu 1 (calibration or verification) is displayed (cf. fig. 6-1). If the verification measurement has already been performed, the calibration or the verification menu is displayed upon acknowledgement of the test setup, otherwise, the DC calibrator and the power meter are first selected.

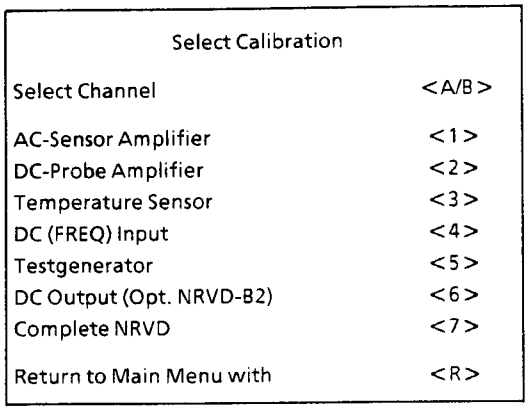


Fig. 6-10 Calibration and verification menu NRVD

Channel A is proposed as test channel by the program for calibration or verification of the individual blocks. The channel can be changed by a corresponding entry (B,A), if desired. The current channel is displayed in the "Select Channel" line. The type of test is selected by entry of the respective number. In contrast to the verification measurement, calibration of the DC-probe amplifier is only performed in test channel A (cf. 6.3.1). If the Cal adapter is not plugged in correctly, the user is requested to connect the Cal adapter to the selected channel on the NRVD.

Calibration of the DC outputs (DC1, DC2) is automatically offered by the program, depending on the NRVD configuration. It is only indicated in the menu, if the I/O option NRVD-B2 is fitted.

It depends on the software version of the EUT, how the test procedure is continued:
a) Calibration is performed directly from the front panel of the NRVD acc. to Section 6.3.5.5 and corresponding program instructions (software version of the controller prior to 1.30).
b) Starting with software version 1.30 (determined by the calibration program), the calibration is made directly by the controller.

The user is requested by the program to provide the external connection (BNC cable) between the output D1, which is to be calibrated, and the input DC(FREQ). The calibration procedure is started as soon as completion of the connection has been acknowledged. Subsequently, the DC2 output is calibrated analogously. If an error occurs, the type of error is indicated on the display and the user either repeats the calibration or continues with the next calibration item.

6.3.4.8 Test Reports

The subsequent possibilities of putting out the calibration and verification report are offered:

- Verification report optionally on screen, printer or as file
- Calibration report optionally on screen, printer or as file
- Error report on screen, printer or as file
- Output of calibration factors on screen, printer or as file.

The report is output to the printer via the first Centronics interface ("LPT1") of the controller. The calibration program does not contain any printer-specific sequences in order to ensure that any printer which contains the standard IBM character set can be used.
The reports can be filed sequentially as ASCII file. The file name is assigned the serial number (e.g., 101324.001 from fig. 6-9) and can be overwritten, if desired. Each modification of the name leads to creation of a new file. If the file name is deleted, the program returns to the menu selection of the kind of output.

The measured values determined during calibration or verification measurement are filed internally in a table. They can be called and are provided in the form of a report. The verification or calibration report contains the rated calibration values for each measuring range of a calibrated function group in the left column, permissible tolerances of the measured values, the measured values of the calibration voltage applied as well as the percentage of deviation from the rated value. This percentage is displayed in the next column for measuring results obtained in channel A followed by columns containing the measured values and percentage of deviation for measuring results obtained in channel B.

Both reports (cf. figs. 6-11, 6-13) contain information about the EUT, the calibration date and the overall evaluation of the measurement performed as well as space for signature of the test engineer.

The error report contains information about errors which may have occurred for each range of the tested function. The errors are documented by output of the concerned measuring range, rated value of the calibration voltage, measured values of the offset voltage and the rated voltage (cf. fig. 6-14). If the offset voltage exceeds the permitted value, it must be checked, whether the output zero voltage of the calibrator used is too high (perform adjustment, if required). The actual value (rated voltage) is provided with correction of the offset voltage and corresponds to the deviation of the applied calibrator voltage. If the calculated calibration factor is outside the range 0.95 to 1.05, an error is signalled and the actual value is entered in the column "Measured/V" in the error report.

Verification Report

POWER METER NRVD 857.8008.02 Serial No.: 101010/002
Last calibrated 1991,OKT,10

Funct.	Range	Nom./V	Tol./%	Measured/V - A -	Dev./%	Measured/V - B -	Dev./%
AC AMP							
	1	0.01	0.12	1.0001E-2	0.01	1.0003E-2	0.03
		- 0.01	0.12	-9.9980E-3	- 0.02	-9.9960E-3	- 0.04
	2	0.02	0.12	2.0001E-2	0.01	2.0002E-2	0.01
		- 0.02	0.12	-1.9997E-2	- 0.01	-1.9998E-2	- 0.01
	3	0.05	0.12	5.0001E-2	0.00	5.0006E-2	0.01
		- 0.05	0.12	-4.9998E-2	- 0.00	-5.0002E-2	0.00
	4	0.10	0.12	1.0000E-1	0.00	1.0001E-1	0.01
		- 0.10	0.12	-9.9999E-2	- 0.00	-1.0001E-1	0.01
	5	0.20	0.12	1.9996E-1	- 0.02	1.9996E-1	- 0.02
		- 0.20	0.12	-2.0004E-1	0.02	-2.0004E-1	0.02
	6	0.50	0.12	4.9994E-1	- 0.01	4.9996E-1	- 0.01
		- 0.50	0.12	-5.0002E-1	0.00	-5.0002E-1	0.00
	7	1.00	0.12	9.9994E-1	- 0.01	9.9997E-1	- 0.00
		- 1.00	0.12	-1.0000E0	0.00	-1.0000E0	0.00
	8	2.00	0.12	2.0000E0	0.00	2.0000E0	0.00
		- 2.00	0.12	-2.0001E0	0.00	-2.0000E0	0.00
	9	5.00	0.12	5.0001E0	0.00	5.0002E0	0.00
		- 5.00	0.12	-5.0002E0	0.00	-5.0001E0	0.00
	10	10.00	0.12	1.0000E1	0.00	1.0000E1	0.00
		-10.00	0.12	-1.0000E1	0.00	-1.0000E1	0.00
	11	20.00	0.12	2.0000E1	0.00	2.0001E1	0.01
		-20.00	0.12	-2.0001E1	0.01	-2.0001E1	0.00
DC AMP							
	1	0.10	0.12	1.0001E-1	0.01		
	2	1.00	0.12	9.9998E-1	- 0.00		
	3	10.00	0.12	1.0000E1	0.00		
	4	40.00	0.12	4.0000E1	- 0.00		
TEMP SENS							
		- 0.30	0.12	-2.9994E-1	- 0.02	-3.0006E-1	0.02
		- 3.00	0.12	-2.9998E0	- 0.01	-3.0001E0	0.00
Testgenerator							
		1.000mW	0.7	1.0004E-3	0.04		
DC (FREQ)							
		10.00	0.12	1.0000E1	0.00		
DC OUT							
		3.00	0.16	3.0005E0	0.02	3.0008E0	0.09

Result: No error

Tested by Date Signature

Beranek 11.08.92

Fig. 6-11 Verification report (NRVD without error)

Verification Report

POWER METER NRVD 857.8008.02 Serial No.: 101000/003
Last calibrated 1991,AUG,13

Funct.	Range	Nom./V	Tol./%	Measured/V	Dev./%	Measured/V	Dev./%
	Channel :			- A -		- B -	
AC AMP							
	1	0.01	0.12	9.9968E-3	- 0.03	1.0002E-2	0.02
		- 0.01	0.12	-9.9978E-3	- 0.02	-9.9986E-3	- 0.01
	2	0.02	0.12	1.9999E-2	- 0.01	1.9999E-2	- 0.00
		- 0.02	0.12	-1.9999E-2	- 0.01	-1.0137E-4*	-99.49
	3	0.05	0.12	4.9992E-2	- 0.02	4.9526E-2*	- 0.95
		- 0.05	0.12	-4.9988E-2	- 0.02	-4.9994E-2	- 0.01
	4	0.10	0.12	9.9978E-2	- 0.02	9.9990E-2	- 0.01
		- 0.10	0.12	-9.7089E-2*	- 2.91	-9.9990E-2	- 0.01
	5	0.20	0.12	1.9171E-1*	- 4.15	1.9999E-1	- 0.00
		- 0.20	0.12	-1.9998E-1	- 0.01	-2.0000E-1	- 0.00
	6	0.50	0.12	4.9986E-1	- 0.03	4.9983E-1	- 0.03
		- 0.50	0.12	-4.9986E-1	- 0.03	-4.9994E-1	- 0.01
	7	1.00	0.12	9.9985E-1	- 0.02	9.9966E-1	- 0.03
		- 1.00	0.12	-9.9987E-1	- 0.01	-9.9989E-1	- 0.01
	8	2.00	0.12	3.4299E-3*	-99.83	1.9992E0	- 0.04
		- 2.00	0.12	-1.9990E0	- 0.05	-1.9997E0	- 0.02
	9	5.00	0.12	4.9990E0	- 0.02	3.0193E0*	-39.61
		- 5.00	0.12	-4.9991E0	- 0.02	-4.9993E0	- 0.01
	10	10.00	0.12	9.9983E0	- 0.02	9.9970E0	- 0.03
		-10.00	0.12	6.4063E-2*	-99.99	-9.9991E0	- 0.01
	11	20.00	0.12	1.9995E1	- 0.02	1.9992E1	- 0.04
		-20.00	0.12	-1.9996E1	- 0.02	-1.9996E1	- 0.02
DC AMP							
	1	0.10	0.12	9.9944E-2	- 0.06	1.1925E-3*	-98.81
	2	1.00	0.12	9.9996E-1	- 0.00	9.9996E-1	- 0.00
	3	10.00	0.12	9.9982E0	- 0.02	9.9983E0	- 0.02
	4	40.00	0.12	6.3232E-3*	-99.98	3.9994E1	- 0.01
TEMP SENS							
		- 0.30	0.12	-2.9988E-1	- 0.04	-3.0000E-1	0.00
		- 3.00	0.12	-2.9994E0	- 0.02	-2.9998E0	- 0.01
Testgenerator							
		1.000mW	0.7	9.9970E-4	- 0.03		
DC (FREQ)							
		10.00	0.12	** Option NRVD-B2 not available			
DC OUT							
		3.00	0.16	** Option NRVD-B2 not available			

Result: ** NRVD exceeds limits **

Tested by Date Signature

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Fig. 6-12 Verification report (NRVD exceeds tolerance)

Calibration Report

POWER METER NRVD 857.8008.02 Serial No.: 101010/001
Next calibration: 8 - 94

Funct.	Range	Nom./V	Tol./%	Channel : - A - Measured/V	Dev./%	Channel : - B - Measured/V	Dev./%
AC AMP							
	1	0.01	0.12	1.0001E-2	0.01	1.0001E-2	0.01
		- 0.01	0.12	-9.9990E-3	- 0.01	-9.9990E-3	- 0.01
	2	0.02	0.12	2.0001E-2	0.01	2.0002E-2	0.01
		- 0.02	0.12	-1.9997E-2	- 0.01	-1.9998E-2	- 0.01
	3	0.05	0.12	5.0001E-2	0.00	5.0006E-2	0.01
		- 0.05	0.12	-4.9998E-2	- 0.00	-5.0002E-2	0.00
	4	0.10	0.12	1.0000E-1	0.00	1.0001E-1	0.01
		- 0.10	0.12	-9.9999E-2	- 0.00	-1.0001E-1	0.01
	5	0.20	0.12	2.0000E-1	- 0.00	1.9999E-1	- 0.00
		- 0.20	0.12	-2.0000E-1	0.00	-2.0000E-1	0.00
	6	0.50	0.12	4.9994E-1	- 0.01	4.9996E-1	- 0.01
		- 0.50	0.12	-5.0002E-1	0.00	-5.0002E-1	0.00
	7	1.00	0.12	9.9994E-1	- 0.01	9.9997E-1	- 0.00
		- 1.00	0.12	-1.0000E0	0.00	-1.0000E0	0.00
	8	2.00	0.12	2.0000E0	0.00	2.0000E0	0.00
		- 2.00	0.12	-2.0001E0	0.00	-2.0000E0	0.00
	9	5.00	0.12	5.0001E0	0.00	5.0002E0	0.00
		- 5.00	0.12	-5.0002E0	0.00	-5.0001E0	0.00
	10	10.00	0.12	1.0000E1	0.00	1.0000E1	0.00
		-10.00	0.12	-1.0000E1	0.00	-1.0000E1	0.00
	11	20.00	0.12	2.0000E1	0.00	2.0001E1	0.01
		-20.00	0.12	-2.0001E1	0.01	-2.0001E1	0.00
DC AMP							
	1	0.10	0.12	1.0001E-1	0.01		
	2	1.00	0.12	9.9998E-1	- 0.00		
	3	10.00	0.12	1.0000E1	0.00		
	4	40.00	0.12	4.0000E1	- 0.00		
TEMP SENS							
		- 0.30	0.12	-2.9997E-1	- 0.01	-3.0003E-1	0.01
		- 3.00	0.12	-2.9998E0	- 0.01	-3.0001E0	0.00
Testgenerator							
		1.000mW	0.7	1.0002E-3	0.02		
DC (FREQ)							
		10.00	0.12	1.0000E1	0.00		
DC OUT							
		3.00	0.16	3.0002E0	0.01	2.9999E0	-0.00

Result: No error

Tested by	Date	Signature
Beranek	11.08.92	

Fig. 6-13 Calibration report

Error Report

POWER METER NRVD 857.8008.02 Serial No.: 101010/003
Last calibrated 1992,AUG,13

Function	Chann:	- A -		- B -	
Range	Nom./V	Offset/V	Measured/V	Offset/V	Measured/V
AC AMP					
1	0.01				
	- 0.01				
2	0.02				
	- 0.02	. .	. .	. .	-1.014E-4
3	0.05	. .	. .	. .	4.953E-2
	- 0.05				
4	0.10				
	- 0.10	. .	-9.709E-2		
5	0.20	. .	1.917E-1		
	- 0.20				
6	0.50				
	- 0.50				
7	1.00				
	- 1.00				
8	2.00	. .	3.430E-3		
	- 2.00				
9	5.00	. .	. .	. .	3.019E0
	- 5.00				
10	10.00				
	-10.00	. .	6.406E-2		
11	20.00				
	-20.00				
DC AMP					
1	0.10	. .	. .	. .	1.192E-3
2	1.00				
3	10.00				
4	40.00	. .	6.323E-3		
TEMP SENS					
	- 0.30				
	- 3.00				
Testgenerator					
	1.00mW				
DC (FREQ)					
	10.00	** Option NRVD-B2 not available			
DC OUT					
	3.00	** Option NRVD-B2 not available			

Result: ** NRVD exceeds limits **

Tested by Date Signature

Beranek 14.08.92

Fig. 6-14 Error report

The calibration factors essentially replace the required hardware adjustment and are calculated as the ratio between the actual and rated values for each measuring range. The calculated amount is approx. 1 and is used for internal correction of the measured values.

The complete table of determined calibration factors (cf. fig. 6-15) can be called via the IEEE-interface using the following commands:

- "SYST:LANG 'TO_CAL'" (set calibration mode)
- "CAL:INFO?" (request Cal information)

```
-----------------------------------------------------------------
 NRVD-CAL-DATA                  last calibrated ('>')  1992,JUL,03
-----------------------------------------------------------------

>>>>>>    (AC+)    -CHN A-    (AC-)  |  (AC+)    -CHN B-    (AC-)
-----------------------------------------------------------------
AC[ .01] >  .991311     >  .991283     >  .989827     >  .989824
AC[ .02] >  .997952     >  .997945     >  .999277     >  .999278
AC[ .05] >  .993545     >  .993541     >  .992689     >  .992699
AC[ .10] >  .997853     >  .997854     >  .995071     >  .995067
AC[ .20] >  .994071     >  .994075     >  .994602     >  .994629
AC[ .50] >  .989028     >  .989415     >  .990648     >  .993396
AC[ 1.0] >  .994106     >  .994487     >  .998620     > 1.001287
AC[ 2.0] >  .989402     >  .989765     >  .991684     >  .994383
AC[ 5.0] >  .996736     >  .997119     >  .997110     >  .999858
AC[10.0] >  .992848     >  .993356     >  .996593     >  .999347
AC[20.0] >  .991364     >  .991546     >  .995412     >  .997288

>>>>>>   CF[-.30] -CHN A-  CF[-3.0] |  CF[-.30] -CHN B-  CF[-3.0]
-----------------------------------------------------------------
TEMP/UC  >  .997531     >  .997704     >  .997531     >  .997704

>>>>>>      CF[ .10] |     CF[ 1.0] |     CF[10.0] |     CF[40.0]
-----------------------------------------------------------------
  DC     > 1.003150     >  .997609     >  .991353     >  .995430

>>>>>>       OFFSET  |     CF[10.0]
-----------------------------------------------------------------
FREQ(DC) >  .002803     >  .995145

>>>>>>      CF[50MHz]
-----------------------------------------------------------------
 ROSZ    > 1.024200

>>>>>>     DC1(MIN)  |    DC1(MAX)  |    DC2(MIN)  |    DC2(MAX)
-----------------------------------------------------------------
OUTP(DC)    -.686573       3.985521       -.685852       3.988939

------------------------------------------------------------ END --
```

Fig. 6-15 NRVD, calibration data

Note: *Only the data marked ">" were calibrated on the date displayed. Data without this identification are of earlier date.*

6.3.5 Manual Calibration

Calibration of the option NRVD-B2 is implemented as semi-manual procedure, since it can be retrofitted. Calibration of the complete basic unit can also be performed in single steps by means of the calibration adapter; this procedure is explained in the next Section. The BASIC program (see 6.3.4) can thus be duplicated. The subsequent Section also allows for partial calibration, which is required, e.g., in case of repair or if no IEEE-bus compatible power meter of the required accuracy is available.

Note: *Prior to calibration, the thermal settling time of approx. 1 hour shall be adhered to, the ambient temperature shall be 23 ± 1° C and humidity shall not exceed 80%. Make sure that the power voltage does not deviate more than 10% from the rated value.*

6.3.5.1 Adjustment of the Cal Adapter

For verification and calibration of the DC amplifier, the Cal adapter is equipped with an adjustable resistor, which directly influences the measuring accuracy. Therefore, its value (1000.0 kΩ) should be checked regularly and readjusted, if necessary. The resistance can be measured with particular setting of the relays in the Cal adapter.

- Setting the Cal adapter (relays):
  Switch on NRVD and connect Cal adapter to channel A.
  NRVD display: `"READ SENSOR, CAL. ADAPTER"`
  Set calibration mode: `"SYST:LANG 'TO_CAL'"`
  Configure Cal adapter: `"CAL:SENS:NMOD 4"`

- How to determine the resistance:
  Remove Cal adapter from the NRVD and measure the input impedance of the Cal adapter (banana plug) and adjust, if necessary (R = 1000 ± 0.05 kΩ), fig. 6-4.

Attention: *The accuracy of the ohmmeter considerably influences the adjustment. The requested accuracy of the ohmmeter acc. to Section 6.2. has to be adhered to.*

6.3.5.2 Entry of Serial No.

Starting with software version 1.30, the serial No. of the NRVD is contained in the instrument identification (cf. fig. 6-16). With first calibration of the NRVD, the serial No. of the NRVD is entered subsequent to entry of the calibration date (cf. table 6-6) and cannot be modified any longer *). If the serial No. entered = 0, the entry (starting with software version 1.30) can be made with later calibration:

```
"SYST:LANG 'TO_CAL'"
"CAL:DATE yyyy,mm,dd"
"CAL:SER '0123745/019'"
```

The length of the serial No. may be max. 11 charaters. Entry of digits (0 to 9) and one special character ("/","." and " "(space)] is permitted.

*) Exception: Loss of the RAM data due to a faulty RAM back-up battery on the controller board implies loss of the serial No. information. The first calibration following repair is assumed by the firmware to be the very first calibration (cf. Section 7.3.2.1).

The instrument identification (fig. 6-16) including the serial No. and the software versions of the controller and the analog boards is output upon the addressed IEEE-bus query "*IDN".

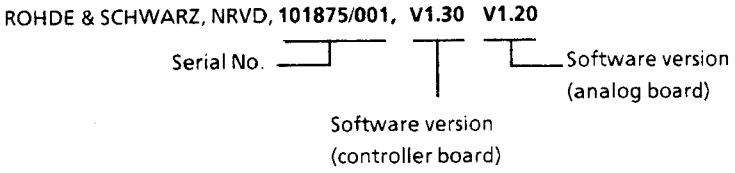


Fig. 6-16 NRVD identification

Calibration of the individual test functions is carried out according to the following scheme:

Table 6-5 Schedule of NRVD calibration procedure

User operation	NRVD
Call the desired calibr. function Input of rated value and polarity of the calibration voltage V_C	Hardware setting Setting of measuring range
Apply 0 V Initiate offset determination	--- Offset measurement ($\rightarrow V_0$) *)
Apply calibration voltage V_C Initiate calibration measurement	--- Measurement of actual value ($\rightarrow$Vm) Calculate and store calibration factor: $K = \frac{V_C}{Vm - V_0}$ *).

*) The offset voltage is only stored for the input DC(FREQ). For the other functions, adherence to the tolerances is checked only. The calibration factors are all stored.

The calibration data of the NRVD are protected against unintentional deletion by entry of the calibration date in the calibration mode implemented at the start of calibration. The individual calibration procedure is thus initiated, followed by selection of the individual calibration functions as shown in table 6-6. Calibration is terminated by entering `"CAL:END"`.

The query `"CAL:INFO?"` in the calibration mode without entering the date is sufficient for reading of the calibration data (verification) (cf. 6.3.4.8, Test Reports/calibration data), the data can, however, not be modified.

Table 6-6 NRVD calibration procedure

User operation	Entry on the controller: IECOUTadr.	NRVD display
Connect Cal adapter to NRVD (LOC-MODE)	--- 1)	READ SENSOR CAL-ADAPTER
Initiate calibration Enter calibration date Select measuring function	"SYST:LANG 'TO_CAL'" "CAL:DATE yyyy, mm, dd" "CAL:AMPL AC, U_C" 2)	CAL.-MODE AC U_C OFFS O.K
DC calibrator → 0 V (offset measurement) DC calibrator → +0,5 V DC calibrator → -0 V (offset measurement) DC calibrator → +10 V	"CAL:AMPL AC, 0.5" "CAL:TRIG" 3) "CAL:TRIG" "CAL:AMPL AC, -0.5" "CAL:TRIG" 3) "CAL:TRIG"	AC 0.50 OFFS O.K AC 0.50 run AC 0.50 AMPL O.K AC 0.50 run CAL-MODE O.K -AC 0.50 OFFS O.K -AC 0.50 run -AC 0.50 AMPL O.K -AC 0.50 run CAL-MODE
DC calibrator → 0 V (offset measurement) DC calibrator → +10 V	"CAL:AMPL DC, 10" "CAL:TRIG" 3) "CAL:TRIG" 3)	DC 10.0 OFFS O.K DC 10.0 run DC 10.0 AMPL O.K DC 10.0 run CAL-MODE O.K

1) The sensor connected is automatically initialized in the "Local Mode".
In the "Remote Mode", the reconnected sensor must be initialized:
"CAL:SENS:INIT(?)" (cf. Operating Manual, Section 3.8.1.7).

2) Calibration of further function blocks is initiated analogously using the following commands:

"CAL:AMPL DC, rated value"	for DC amplifier,
"CAL:AMPL TEMP,-0.3" (-3.0)	for temperature measuring input 0.1 (1)mA
"CAL:ROSZ SET_50 MHZ,POUT"	for test generator (cf. 6.3.5.4)
"CAL:AMPL FREQ, 10"	for DC (FREQ) input
"CAL:AMPL OUTP, 0 (1) or 2"	for DC outp. (0 (1) = sequential, DC1 to DC2; 2 = only DC2; cf. 6.3.5.5)
"CAL:END"	End of calibration

The rated values of the calibration voltages are listed in table 6-3.

3) The trigger command "CAL:TRIG" switches over to calibration of the rated value automatically following the offset measurement or terminates the calibration step.
During calibration, intermediate results (offset measurement, actual value measurement) can be inquired immediately upon the trigger command by entering: "CAL:INFO? MEAS" and be read, in order to find the causes of errors, which might occur.

Query for intermediate results "CAL:INFO? MEAS with calibration of the DC amplifier in the measuring range 10 V (cf. table 6-6) following a correctly performed offset measurement:

```
0;CAL:TRIG  O.K.  OFFS= 79.32E-06;AMPL=0,"not valid";CF=0,"not valid"
```

Upon correct measurement of rated value ("CAL:TRIG"):

```
0;CAL:TRIG  O.K.  OFFS= 71.39E-06;AMPL= 10.00024;CF=  .999164
```

The same inquiry for correct offset measurement and faulty calibration (amplitude of measured value and cal. factor faulty → error bit set):

```
0;CAL:TRIG  O.K.  OFFS=-19.83E-06;AMPL=0,"not valid";CF=0,"not valid"

1;CAL:TRIG   ER   OFFS=-19.83E-06;AMPL=  .000040;CF=  .000006
```

Note: *If offset measurement is faulty, measurement of the rated value is automatically indicated to be faulty, too.*

6.3.5.3 Calibration / Verification of DC(FREQ) Input

Calibration is performed according to the described schedule (cf. table 6-5) at 0 V and 10 V acc. to table 6-3. Verification is performed in Cal mode acc. to table 6-7 at the same voltages.

Table 6-7 Test schedule for DC(FREQ) input

Action	Entry on the controller: IECOUT Adr,	Reaction of NRVD
Switch on DC (FREQ) measurement	"CAL:AMPL FREQ, 10"	FREQ 10.0 OK
Apply 0 V from the calibrator to DC (FREQ)		
Measure the offset	"*TRG"	Displ. measured value
Apply 10 V from the calibrator to DC (FREQ)		
Measure the actual value	"*TRG"	Displ. measured value

The offset error may be ± 5 mV, the final value should amount to 10 ± 0.020 V.

6.3.5.4 Test Generator

The test setup acc. to fig. 6-17 illustrates how the current output power of the test generator is measured using a particularly calibrated power meter (see 6.2). The actual value of the power output is transferred to the NRVD via the controller, the NRVD calculates the calibration factor which was specified to be the ratio between the actual value and the rated value, and adjusts the test signal at the output (N-socket on the front panel) with corrected power. The signal is measured once again and the preceding step repeated, if required.

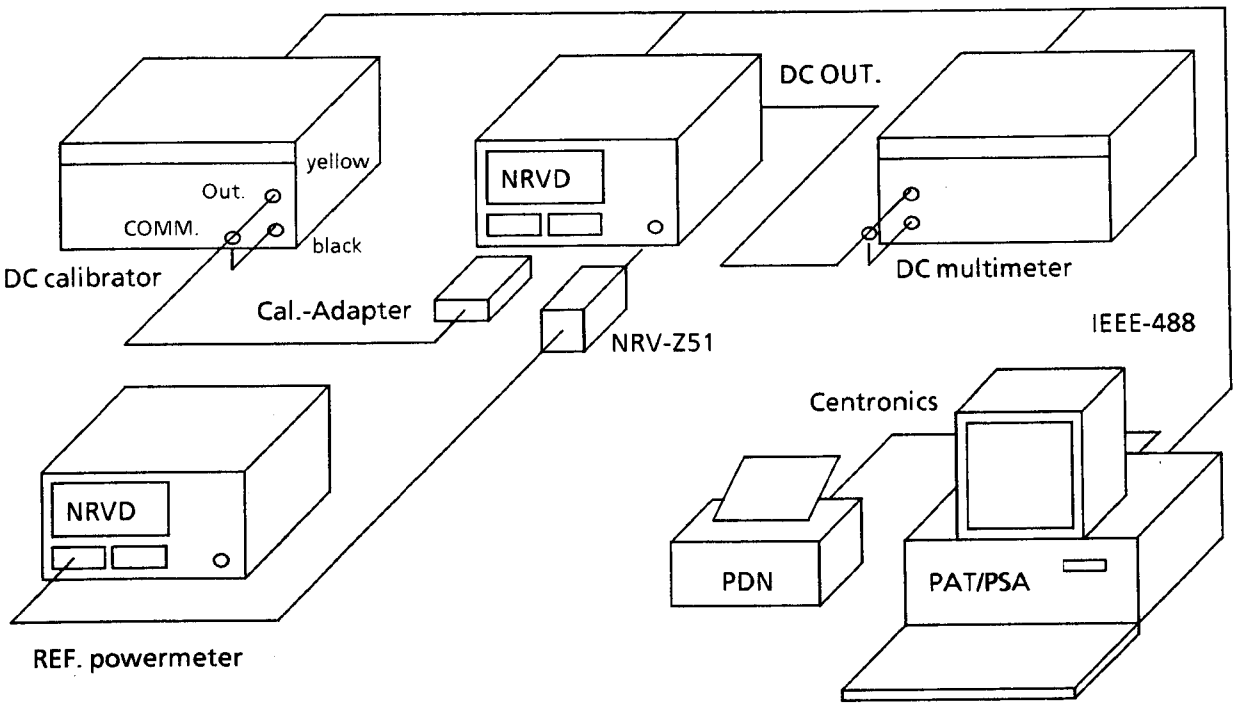


Fig. 6-17 Test setup for calibration of the test generator

Table 6-8 Calibration procedure - test generator

User operation	Entry on the controller: IECOUT Adr,	Reaction of NRVD
Initiate calibration	"SYST:LANG 'TO_CAL'" "CAL:DATE yyyy, mm, dd"	*CAL-MODE*
Switch off NRVD test generator	"CAL:ROSZ:STAT OFF"	LED "OUTPUT" →OFF
Reference power meter (NRVD) zero correction (A)	"SENS:CORR:STATE ON"	ZERO CHN.A
Switch on NRVD test generator	"CAL:ROSZ:STAT ON"	LED "OUTPUT" →ON
Transfer the measured power P_{out} to the NRVD	"CAL:ROSZ SET_50 MHz, P_{out}"	P_{out} corrected
Check the power output P_{out}: $0.999 \leq P_{out} \leq 1.001$ mW, repeat preceding step, if required	("CAL:ROSZ SET_50 MHz, P_{out}")	(P_{out} corrected)
Terminate calibration	"CAL:END"	Test mode, REM

Remark:
With software version V1.0, the output power must be determined in the test mode. Tranfer of the actual value is performed in the calibration mode.

6.3.5.5 DC Output (NRVD-B2 Option)

Verification

The two analog outputs DC1 and DC2 of the NRVD-B2 option supply a DC voltage in the range of approx. -0.6 V to 3.8 V which is proportional to the bargraph indication. Scaling of the two outputs is freely selectable due to free selection of the indication range. The left end of the bargraph scale is assigned the output voltage 0 V, the right full-scale value is assigned the output voltage + 3 V. If the test voltage is constant (calibrator) in the test setup acc. to fig. 6-18 the voltage values are both verified with corresponding scaling. Verification can be performed either from the front panel or via the IEEE-interface.

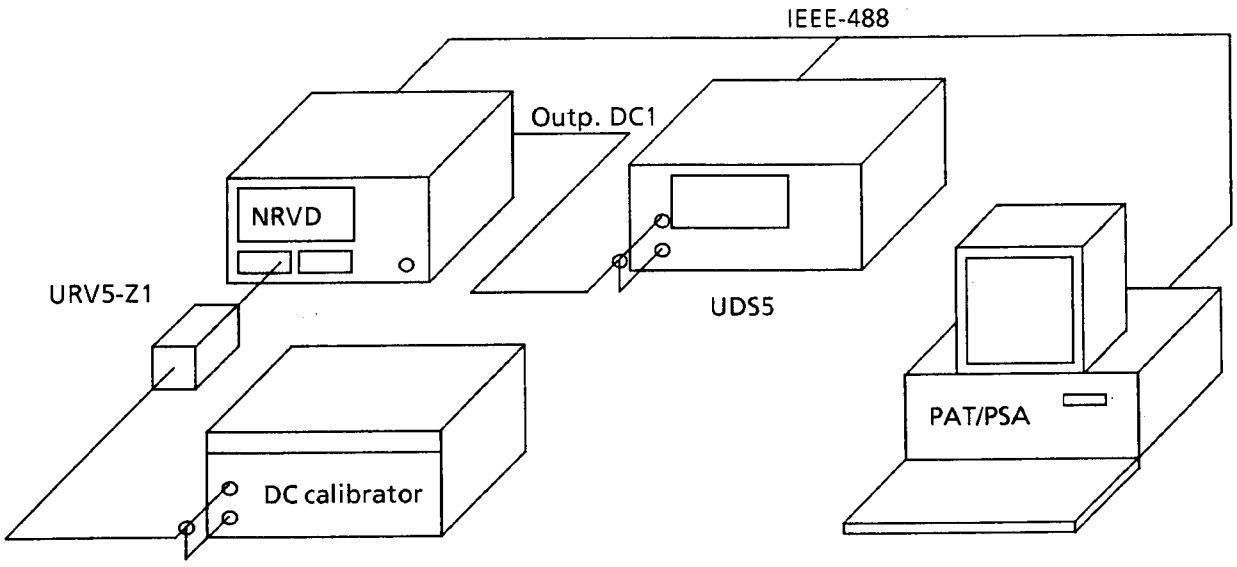


Fig. 6-18 Test setup for verification of the DC outputs of the NRVD-B2

Preparation

- Connect DC probe URV5-Z1 in test channel A and apply 1 V from the calibrator.
- Connect DC voltmeter to the analog output DC1.
- NRVD: → Store measured value as reference value: **MEAS → REF.**
  → Select display V/Vr: **"UNIT" → "REL → more → more → V/Vr"**
  → Define the left scale value of the bargraph to be 1, the right one to be 2:
  "DISP" → "BARGRPH → SCALE→ 1 → STO →2 → STO"
- The output voltage at DC1 must be 0.000 V ± 5 mV.
  → Define the left scale value of the bargraph to be 0, the right one to be 1.
- The output voltage at DC1 must be 3.000 V ± 5 mV.
- Verify test channel B and DC2 analogously.

Verification via IEEE bus and controller

Table 6-9 Verification schedule/analog outputs (NRVD-B2 option)

User operation	Entry on the controller: IECOUT Adr,	Reacion of NRVD
Calibrator → + 1 V		
Initialize probe	**"INP:SENS:INIT"**	READ SENSOR
Switch on DC1	**"OUTP:DC:STAT ON"**	
Switch on relative display	**"SENS:VOLT:UNIT REL"**	V/V_r
Measured input voltage (NRVD)	**"*TRG"**	Displ. measured value (e. g. 1.002 V)
Measured value →reference value	**"VOLT:REF:MVAL"**	Displ.: 1.000
Carry out scaling	**"DISP:ANN:BARG:SCAL:LOW 1; UPP 2"**	DC1 →0 V
Measure output voltage (Volt meter, V = 0 ±0.005 V)	**"*TRG"**	Displ.: 1.000
Carry out scaling	**"DISP:ANN:BARG:SCAL:LOW 0; UPP 1"**	Displ.: 1.000, DC1 →3 V
Measure output voltage (Volt meter; V = 3 ±0.005 V)	**"*TRG"**	Displ.: 1.000

▸ Plug DC probe URV-Z5 in test channel B, connect DC voltmeter to the output DC2. Verify channel B correspondingly.

Calibration

The analog outputs DC1 and DC2 of the NRVD-B2 option are calibrated via the DC(FREQ) input. The user is requested on the NRVD display to provide a connection between the output to be calibrated (DC1, DC2) and the DC(FREQ) input (BNC cable on the rear panel). Entry of the date with calibration of the NRVD-B2 option from the NRVD front panel is not required. The calibration procedure is shown in table 6-10.

Starting with software version 1.30 (controller board, see also 6.3.5.2), calibration of the analog outputs is also possible via the IEEE bus (additional identification of the cal. factors/cf. fig. 6-15) The procedure is shown in table 6-10.

Table 6-10 Calibration of the analog outputs (NRVD-B2 option, local mode)

User operation	NRVD display/reaction
Initiate calibration (**LOC-MODE**): Key →**"SPEC"** + Menu keys → **"more"** →**"DC-OUTP"**→**"DC-OUT *CAL"**	DC1-DC (FREQ) *EXEC
Connect output DC1 to the input DC (FREQ) via BNC cable	|
Press menu Key →**"*EXEC"**	DC1-CAL-RUNNING DC2-DC (FREQ) *EXEC ←
Connect output DC2 to the input DC (FREQ) via BNC cable	|
Press menu Key →**"*EXEC"**	DC2-CAL-RUNNING (WRNG. 20/CAL OUT O.T. *) DC-OUTP ON OFF
Remove connections on the rear panel, end of calibration.	

*) When an error occurs, the program returns to the beginning of the respective calibration step. Use the key "→ MEAS" to interrupt calibration.

Table 6-11 Calibration of the analog outputs (NRVD-B2 option, rem. mode)

User operation	Entry on the controller:IECOUTadr.	NRVD display
Connect Cal. adapter to NRVD (LOC-MODE)	--- 1)	READ SENSOR CAL-ADAPTER
Initiate calibration Enter calibration date Determine cal. function	**"SYST:LANG 'TO_CAL'"** **"CAL:DATE yyyy, mm, dd"** **"CAL:AMPL OUTP 0"** 2),3)	CAL.-MODE *OUTP.DC1 O.K.*
Connect DC1 to DC(FREQ)		
Trigger calibration	**"CAL:TRIG"**	DC1-CAL RUNNING *OUTP.DC2 O.K.*
Connect DC2 to DC(FREQ)		
Trigger calibration	**"CAL:TRIG"**	DC2-CAL RUNNING *CAL-MODE O.K.*

1) In REM mode, the sensor connected must be intialized (cf. table 6-6)

2) Starting with software version 1.30 (controller board)

3) The parameter 2 (instead of "0" or "1") calibrates only DC2.

6.3.5.6 Overview of the NRVD Calibration Commands

Table 6-12 Overview of the NRVD calibration commands

Cal command	Function/NRVD
"SYST:LANG'TO_CAL'"	Calibration mode set (inevitable for subsequent commands)
"CAL:INFO? (AC)"	Output of the cal. data for function given (AC ampl.; DC, TEMP, FREQ, ROSZ). If no function is entered, all calibration data are output.
"CAL:DATE YYYY,mm,dd"	Entry of calibration date; not required for reading old calibration data
"CAL:SER '"_NR"	Entry of serial No. "S_NR"; max. 11 characters (cf. 6.3.5.2)
"CAL:AMPL AC, rated value"	Sets required measuring range automatically and calibrates the AC amplifier with the rated value entered (cf. tables 6-3 and 6-6)
"CAL:AMPL DC, rated value"	DC amplifier like AC amplifier
"CAL:AMPL FREQ 10"	Calibrates DC(FREQ) input with 10 V
"CAL:AMPL TEMP,-0.3" (-3.0)	Calibrates input of temperature sensor for 0.1 (1) mA sensors (cf. 6.3.1)
"CAL:AMPL OUTP, Nr"	Calibrates DC outputs via IEEE bus (starting with software version1.30/controller) No = 0 (1) →Seq. calibration DC1,2 No = 2 →calibrates only DC2
"CAL:TRIG"	Performs a measurement in the selected measuring range: 1st output offset acquisition 2nd output Actual-value measurement (cf. table 6-6)
"CAL:INFO? MEAS"	Output of current measured value determined by "CAL:TRIG" (cf. table 6-6)
"CAL:ROSZ:STAT ON" (OFF)	Switches test generator on (off) (except software versions up to V1.20)
"CAL:ROSZ SET_50 MHz, P_{OUT}"	Corrects the output power upon indication of the actual value P_{out} on 1 mW
"CAL:END"	Terminates the calibration mode
"CAL:SENS:INIT (?)"	Initializes sensors connected (? → with ACTUAL-state output)
"CAL:INP:NSEL (1)"	Selects the current, i.e. the indicated (1,2) test channel
"CAL:SENS:NMOD 4"	Configures the Cal adapter connected for measurement or adjustment of the 1-MΩ resistor (see 6.3.5.1)

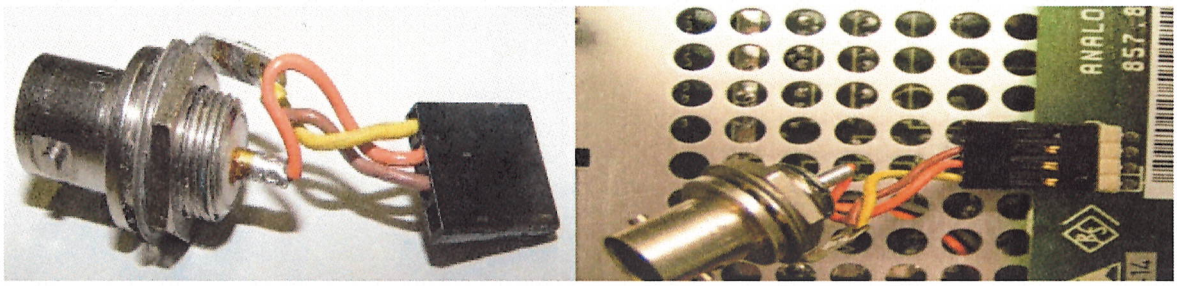
First Calibration of NRVD

If the calibration data are lost, a complete “first calibration” must be done.

The “first calibration” can be done with the normal NRVD calibration program G5.

The flag: “Option B2” must be seted.

Do cklick programmpoint "DC-Frequency-Adjustment"



For simulation of the option an adapter like on the picture is fitting on the analog board.

If this procedure is not carried out, despite complete calibration, the error message 008 (missing calibration data) appears.

ROHDE&SCHWARZ

Liste mechanischer Teile
Bilder und Erklärung zur Liste mechanischer Teile
List of mechanical parts
Figures and explanation pertaining to list of mechanical parts
Liste des pièces mécaniques
Figures et définitions pour liste des pièces mécaniques

(R 48 010 - 1)
095.1000 Bl. 13

Liste mechanischer Teile

Der NRVD ist in ***R&S-Kompaktbauweise 90*** aufgebaut.

Gehäusegröße:
2E, 1 /2, T350

Maße über alles:
220 × 103 × 355 (B × H × T)

Ergänzungen:
19"-Adapter ZZA-92
KS 396.4886.00

List of mechanical parts

The NRVD is designed in accordance with the ***R&S design 90***.

Cabinet size:
2E, 1 /2, T350

Overall dimensions:
220 × 103 × 355 (width × height × depth)

Accessories:
19"-Adapter ZZA-92
KS 396.4886.00

Lfd. Nr.	Kenn-zeichen	Menge	Benennung/Beschreibung	Sachnummer
No	Unit/ Comp.No	Qty	Designation	Stock No.
1		1	Haube, oben 2E, 1 /2, T350 Cover, top	350.6128
2		1	Haube, unten 2E, 1 /2, T350 Cover, bottom	350.6157
8		2	Gerätefuß, vorne Instrument foot, front	396.4534
9		2	Aufstellfuß, unten Foot, bottom	396.4540
11		2	Gerätefuß, hinten Instrument foot, rear	396.4586
12		8	Zapfen Pin	396.4634
15		2	Seitenleiste T350 Side strip	396.3073
16		4	M3 x 6 DIN965 A4	081.9378
17		1	Rückwandfuß, links 2E Rear-panel foot, left	396.4305
18		1	Rückwandfuß, rechts 2E Rear-panel foot, right	396.4092
21		1	Tragegriff T350 Carrying handle	396.3215
22		2	Griffbuchse DRM24 Washer	396.3367
23		2	M4 x 10 DIN965 A4	081.9478

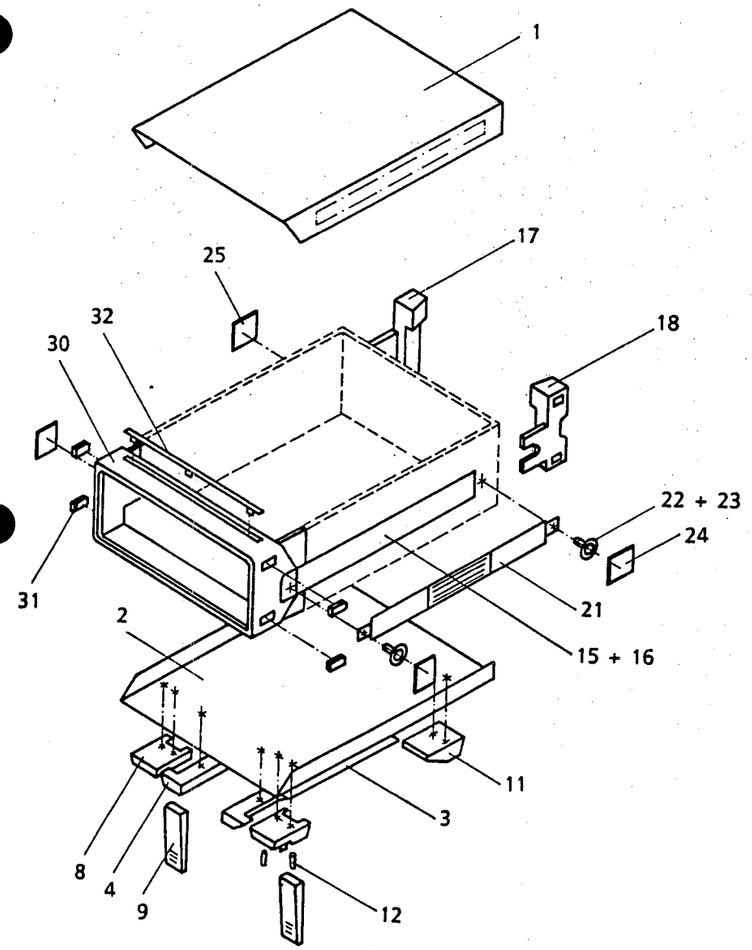
Lfd. Nr.	Kenn-zeichen	Menge	Benennung/Beschreibung	Sachnummer
No	Unit/ Comp.No	Qty	Designation	Stock No.
24		2	Abdeckung, Griffseite Cover, handle side	396.3350
25		2	Abdeckung, Leerseite Cover, blank side	396.3344
30		1	Frontrahmen 2E 1/2 Front frame	827.2382
31		4	Seitenfuß Side foot	396.4692
32		2	Stapelnutabdeckung 1/2 Cover for groove	827.5369
40		1,0 M	HF-Dichtschnur O-Prof. 2,0 SI RF seal	396.1035

Gehäuse

Aufbau

Der Aufbau besteht aus einer tragenden Aluminium-Druckguß-Rahmenkonstruktion mit gerätespezifischer Front-, Montage- und Rückplatte, die mit einer Ober- und Unterhaube (= Beplankung) ummantelt ist.

Rahmen und Beplankung:



Casing

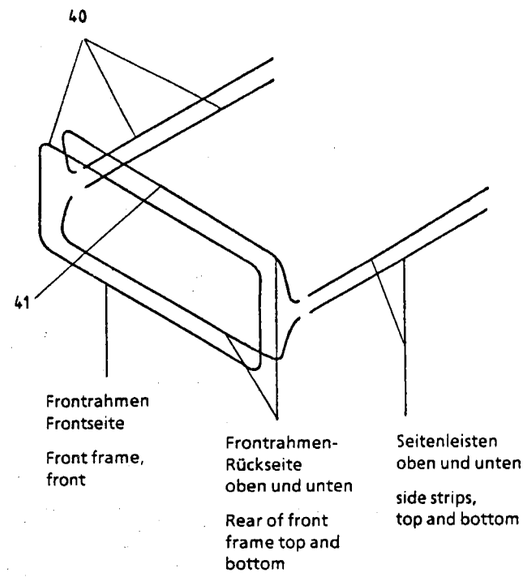
Construction

The construction consists of a self-supporting aluminium-cast frame with front, mounting and rear panel, top and bottom covers (= panelling).

Frame and panelling:

Dichtschnur (nur bei Geräten mit erhöhtem Schirmdämpfungsbedarf vorhanden) jeweils in die umlaufende Nut einlegen.

Insert the braided cord (provided only for instruments requiring a high degree of shielding) into the respective groove.



Die Dichtschnur in der Frontrahmen-Frontseite muß durch Klebepunkte in Abständen von ca. 80 mm fixiert werden. Dazu Klebepunkte mit ca. ø2 mm im Nutgrund anbringen und Dichtschnur aufdrücken.
Dauerhaft elastischen Kleber wie z.B. Si-Kautschuk 3145 RTV (R&S-Sachnr. WV 088.3152) verwenden.

The braided cord in the front of front frame must be fixed by glued joints approx. every 80 mm. Make joints (ø approx. 2 mm) on the bottom of the groove and press braided cord firmly on it.

Use a permanently elastic adhesive, such as Si-rubber 3145 RTV (R&S Part No. WV 088.3152).

Öffnen und Schließen des Gehäuses

Die gute Schirmdämpfung der Kompaktbauweise 90 erfordert häufige Kontaktstellen und hohe Paßgenauigkeit. In Verbindung mit einem leichten Anlagedruck, der mit dem Festziehen der Rückwandfußschrauben erreicht wird, erhält man einen straffen Sitz der Ober- und Unterhaube auf dem Rahmen.

Zum ***Öffnen*** muß man die Rückwandfußverschraubung lösen und die Füße nach rückwärts abziehen (Schrauben bleiben im Fuß haften). Je nach Bedarf läßt sich nun Ober- bzw. Unterhaube ebenfalls nach rückwärts abnehmen. Sitzen die Hauben sehr fest, erleichtert man das Abziehen durch abwechselndes Hebeln in Pfeilrichtung mit einem Schraubenzieher an beiden Geräteseiten (siehe Bild).

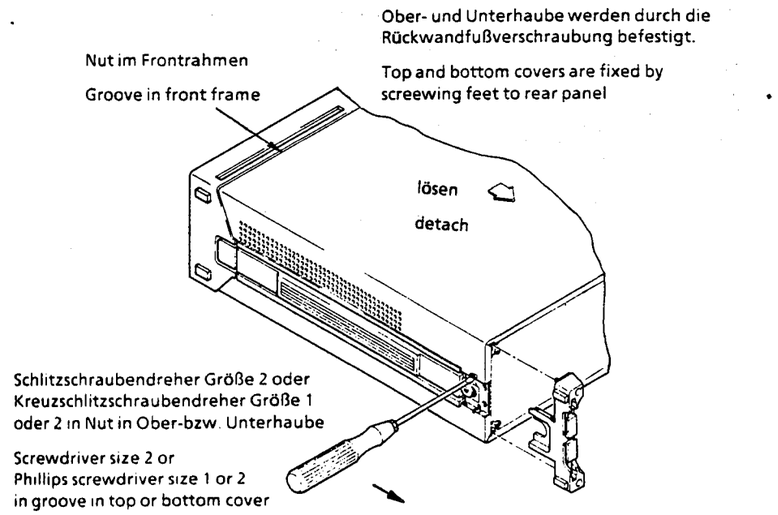
Zum ***Schließen*** des Gehäuses werden erst die Frontkanten der Hauben in die umlaufende Nut des Frontrahmens und der Seitenleisten eingeführt und dann in die Erhöhungen am Rückrahmen bis Anschlag eingerastet. Das Gerät ist wieder geschlossen, wenn die Rückwandfüße eingeschoben und die Schrauben festgezogen sind.

Opening and closing the cabinet

To obtain the high degree of shielding of design 90, many points of contact and accurate fitting are employed. When exerting a slight pressure by tightening the rear-panel feet, tight fitting of the top and bottom covers is ensured.

To ***open*** the cabinet, first undo the rear panel feet screws and withdraw the feet (captive screws). It is now possible to detach top and bottom cover if required. If the fitting of these cover plates is very tight, removal can be facilitated by alternately levering on both sides of the instrument using a screwdriver (see illustration).

To ***close*** the cabinet, insert the front edges of the covers into the groove of the front frame and the side strips and lock them into the catches on the rear frame into detent position. The cabinet is closed when the rear-panel feet are inserted and the screws tightened.



ER DIESE UNTERLAGE
BEHÄLTEN WIR UNS ALLE RECHTE VOR

IEC 625
IEEE448

A3
ANZEIGE
DISPLAY
857.8108.02
1
(X1)
34

(W1)

A1
RECHNER
PROCESSOR
350.5867.04
(X30) 12 24 1 13
(X40) 1 34
(X60) 1A 1B 25A 25B
(X50) 1 20
(X70) 6 5 4 3 2 1
(X80) 1 2

W150

OUTPUT
1.00MW
W10
X114

A4
FILTERPLATTE
FILTERBOARD
857.8308.02
A (X1) 1 12
B (X2) 1 12
(X3) 1 34
W4

A2
ANALOGPLATTE
ANALOGBOARD
857.8150.02
(X101) 1 34
(X102) 1 20
(X103) 1 4

(W3)

T1
(X70) 6 5 4 3 2 1
(X80) 1 2
NC
GE GN BL GR OR
X10 SW/GE
OR GE RT VI BR OR GR

S2
P2 2A GR
P1 1A
SW BL BR

S1
BL
GN/GE X10
SW
N E1 L G K H
F1 F2
N L

F1/F2:
100/120V
DIN41662 1500/250V
220/240V
DIN41662 1250/250V

04/00
03/00
ÄEND.
IND.

IEC 625
IEEE488

(W1)

(X30)

(X40)

(X50)

(X70)

(X80)

(X60)

(X10)

(W2)

A1
RECHNER
PROCESSOR
350.5867.04

OPTION
NRVD-B2
857.8908.02

I/O BOARD
351.1613.02

(X9)

(X8)

(W1)

(X10)

(W3)

BUCHSENPLATTE
CONNECTOR BOARD
857.8937.02

DC1 DC2 READY EXT. TRIG DC FREQ.

W150

T1

NC

GE GN BL GR RT

X10 SW/GE

OR GE RT VI BR OR GR

(X102)

(X103)

S2

P2 2A GR

P1 1A

SW BL BR

BL

GN/GE X10

SW

N E1 L I G K H B

F1 F2

S1

C D F B A I D E

(W3)

N L
47...440HZ

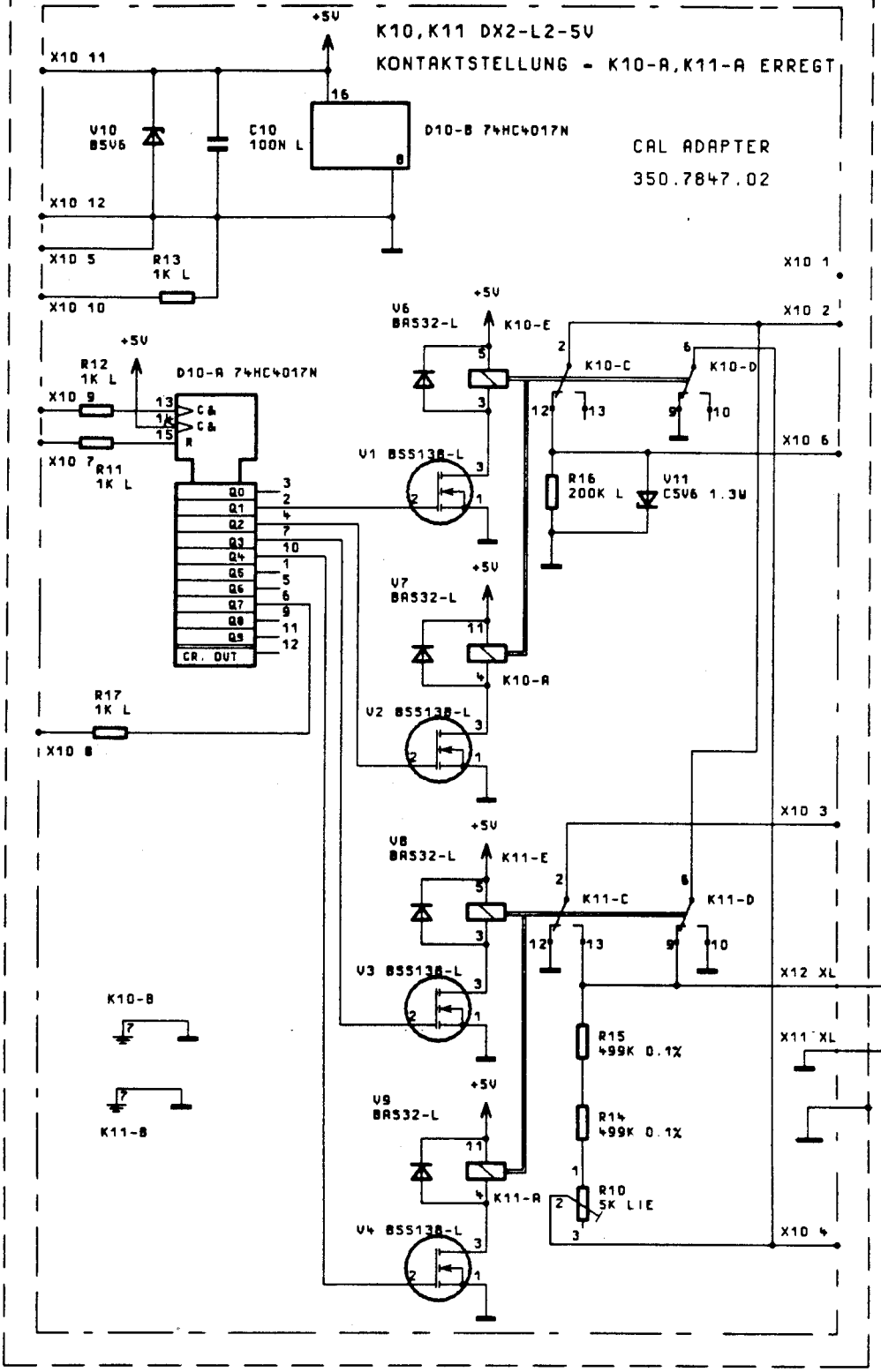
F1/F2:
100/120V
DIN41662-1500/250V
220/230V
DIN41662-1250/250V

ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING

CIRCUIT DIAGRAM IS VALID FOR MOD.02
STROMLAUF GILT FUER VAR.02

04/00	47627	11.02.92	SR	1KGU	TAG	NAME	BENENNUNG
				BEARB.		SR	NRVD LEISTUNGSMESSER
				GEPR.		SR	NRVD POWERMETER
				NORM			
				PLOTT	12.02.92		
03/00	45085	11.91	WR	ROHDE&SCHWARZ			ZEICHN. NR. 857.8008.01S
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET NRVD			BLATT-NR. 1 V. 1 BL.
				REG.I.V. 857.8008		ERSTE Z. 857.8008	

FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR



ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING

STROMLAUF GILT FUER VAR.02

CIRCUIT DIAGRAM IS VALID FOR MOD.02

01				1KGS	TAG	NAME	BENENNUNG
				BEARB.		SE	CALIBRATION ADAPTER
				GEPR.		REI	
				NORM			
				PLOTT	11.09.91		
REND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR. 350.7818.01S
				ZU GERAET NRVD-S1			REG.I.V. 1029.2808 V

BLATT-NR. 1 v. 1 * BL.

ERSTE Z.

ZEICHN.

ROHDE&SCHWARZ

SERVICE INSTRUCTIONS

Computer Board

350.5867

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Part lists
Circuit diagrams
Component plans

7 Checking and Repair of Computer Board A1

7.1 Function Description

(See circuit diagram 0350.5867.01S and block diagram 7-1)

The computer board A1 - designed in line with model 04 of the URE3 computer board - contains a microprocessor system with the 16-bit processor D4, which, as the main computer, performs the coordination and monitoring of all measurement sequences as well as control and computation tasks:

- Control and operation of inputs and outputs via keyboard, display, IEC-bus interface and of the In/Out Option NRVD-B2 including option identification.
- Communication with the coprocessor of the analog board A2 with handling of a bidirectional data transfer via the serial optocoupler interface.

The board also contains voltage supplies with rectifier and voltage controller for the digital section and the isolated analog section as well as a driver stage for the illumination control of the LCD.

When switching on the instrument, a comparator circuit provides a RESET signal for defined reset of the main processor and the peripheral circuits.

7.1.1 Clock Oscillator

The microprocessor D4 (80C186) is controlled by a 16-MHz clock. The oscillator circuit D3 provides a crystal-referenced TTL signal. The clock is derived from common gate D3 with ceramic resonator B1. The 16-MHz clock is applied to the microprocessor clock input D4.59 via jumper X1, X2.

7.1.2 Microprocessor

The processor system with D4 communicates with the peripheral units via an 18-bit address bus and a 16-bit data bus as well as via a control and interrupt bus. Registers D1, D2 and D45.B are used for temporary storing of addresses from the address/data lines AD0 to 16, A16 and A17 of D4. The ALE signal of the processor is used to differentiate between data and addresses (ALE → log. 1: addresses, ALE → log. 0: data)

The function sequence of the processor system is determined by the program stored in the two 64-kbyte EPROMs D5 and D6.

The main memory with 2 * 32 kbyte static RAM consists of the CMOS RAMs D7, D8 and permits non-volatile data storage due to battery backup (→ 7.1.4).

After switching on the operating voltage, a RESET signal (RESET 0) delayed by 100 ms is applied from comparator circuit N4 via X77,X87 to the processor at D4.24. A RESET-OUT signal (RESET 1) is then generated at D4.57 in order to reset the coprocessor of the analog board (→ 7.1.3 and A2 board).

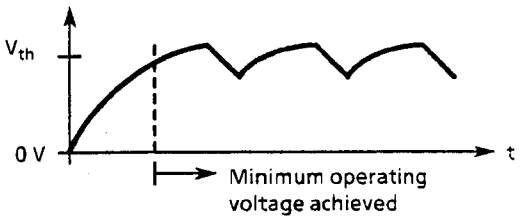
The function sequence is interrupt-controlled according to different priority levels, i.e. functional measures during instrument control lead to corresponding jumps in the program. Interrupt control is effected via INT0, INT1, INT2 and INT3 of processor D4.

Interrupt-controlled procedures include:

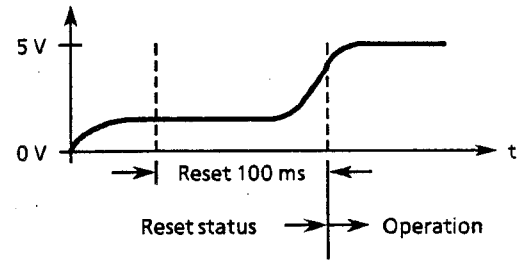
- Remote control via the IEC-bus controller D30 (INT0)
- Key operation and evaluation request via the key controller of the display board (INT1 from KEYINT, → A3 board, 7.1.3)
- External trigger signal from the In/Out Option NRVD-B2 (INT3, → In/Out Option 7.1.1)

7.1.3 RESET Generation

A delayed power-on signal is applied from the unregulated DC voltage of the 5-V computer supply to the comparators N4-A, B, D and timer C96, R86 at X77 (filter capacitor C98 and input 5-V controller N5.1) via an input voltage threshold (V79).



Switching on the operating voltage,
V_{th}: Threshold of reset circuit



RESET-0 signal at X77

Fig. 7-2 Timing of reset control

Function of RESET-0 signal:

- Reset of main processor D4.
- Reset of shift registers D51, D52 for serial interface to analog board.
- Reset of output port D40.
- Reset of key controller (→ A3 board, 7.1.1).
- Disabling of chip select inputs of RAMs D7, D8 during switch-on (→ 7.1.4).
- Switching through transistors V4, V5 (→ 7.1.4).

In the reset phase, processor D4 applies the output signal RESET 1 from RESET 0 to the optocoupler interface between computer and analog board in order to reset the coprocessor of the A2 board.

7.1.4 Battery Buffer and Data Preservation

The main memory with the CMOS RAMs D7, D8 is buffered via the lithium battery G1. The battery voltage and the 5-V supply are decoupled via diodes V2, V3 and transistor V4. When the instrument is switched off, the battery G1 supplies the CMOS RAMs and thus ensures non-volatile storage of calibration data, complete instrument setups, reference values for the measurement and the current IEC-bus address.

After switching on the power supply, the battery voltage is automatically replaced by the 5-V supply via V3 and V4.

During the RESET status (RESET 0 → active L), the CS inputs CS1 of the CMOS RAMs D7, D8 are applied to passive H via the NAND gates D12-A, B so as to prevent an undefined access to the stored data upon power-on.

Reset of the RESET 0 line to passive H causes transistor V4 to be switched through via V1 and V5. The voltage difference between the operating voltage V_{BUFF} of D7, D8 and the 5-V supply is thus very low.

Resistor divider R29, R37 and NAND gate D12-C permit course monitoring of the battery voltage.

With V_{batt} < 1,1 to 2,8 V, the output of D12-C is applied to H. The line PI 6 is also applied to H via R19.

After switching on, the processor reads the status via port D41 to data line D0 and outputs the message BATT LOW and the error message DEVICE ERROR * 000E on the display if D0 = 1 (status H) and RAM- and calibration data are simultaneously missing (→ Operating manual 4.1.2, Service manual 6.3).

7.1.5 Optocoupler Interface to Analog Section

Function of optocoupler interface:

- Electrical isolation between computer and analog board; this prevents hum and spurious signals from being picked up via the AC supply or IEC-bus connection during the measurement.
- Transfer of the Reset-Out signal to reset the coprocessor of the analog board when switching on (Signal RESET, → 7.1.3).
- Bidirectional serial data communication between the main computer and the coprocessor of the analog section for transmission of setting data, measurement commands or correction values to the coprocessor (signals INT, DATUM 1, CLOCK) and for data reception of the measurement results from the coprocessor (signals DATUM 2, CLOCK).

Data output to analog board:

- Parallel loading of shift registers D51, D52 via the 16-bit data bus of processor D4.
- The main processor D4 indicates to the coprocessor its readiness for data output via interface line INT at interrupt input INT0.
- The coprocessor switches to data reception (P1.7 → H).
- Serial output of the loaded data from shift register D52.17 via the optocoupler interface (DATUM1).
- The synchronous clock required is generated in groups of 8 clock pulses in the coprocessor of the analog board from the serial output port TXD and transferred via optocoupler U50-B to the shift registers of the computer board.
- In the analog board, the coprocessor synchronously reads in the data stream (DATUM 1) via the serial input port RXD.

Data reception from analog board:

- The coprocessor of the analog board indicates that it is ready for serial data transfer to the main processor D4 (INT2 via optocoupler U50-A).
- The coprocessor sends the data stream DATUM2 via the optocoupler interface using the clock signal CLOCK, thereby serially loading shift registers D51, D52 of the computer board.
- Dual-4-bit counter D56 counts the shift clock.
- After correct transfer of the data stream, the main processor reads the received data byte from shift registers D51, D52 via the 16-bit data bus.

Parity check:

The parity bit is checked for every transfer when transmitting or receiving data. In the event of faults caused e.g. by spurious pulses or hardware errors the transfer is repeated several times. Stationary parity errors are indicated on the display as DEVICE-ERROR * 0080 (→ 7.3 Troubleshooting).

Monitoring the time limit:

Every transmission or reception of data is monitored via a time limit. When the time limit is exceeded, this is indicated on the display as DEVICE-ERROR * 0010 or DEVICE-ERROR * 0020 (→ 7.3 Troubleshooting).

7.1.6 Peripheral Control of Display and Key Operation

(See function description and signal characteristics in display board A3, section 7.1)

Display control:

- Program-controlled reset for the LCD drivers from output port D46 (line PO12) when switching on
- Select lines CS1 to CS4 for the LCD drivers via inverter D43 from output port D40
- Conditioning of the clock (Serial Clock SCK), serial data stream (Serial Input SI) and control information (Command/Display C/D) for the LCD drivers via D40, D42, D44 and D45
- Interrogation of the acknowledgement signal (BUSY) of the LCD drivers via input port D41 on data line D0 of the microprocessor.

Key control:

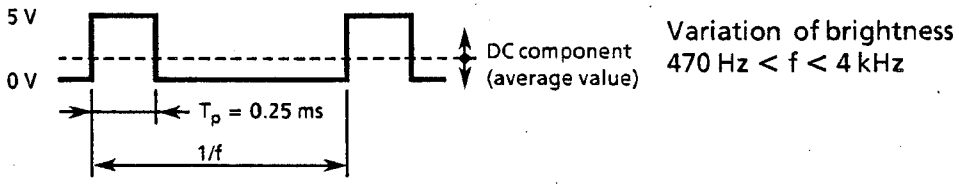
- Reset of key controller KEYINT when switching on via RESET 0* (line X40.A9)
- Interrupt signal INT1 applied to microprocessor during key operation
- Enable line PCS3, write/read selection WR*/RD* for initialization of the key controller and reading out of the key codes.

7.1.7 LCD Illumination Control

The buffer consisting of N4-C and driver transistor V80 provides a DC voltage of 0.7 to 5 V at X76 for the light bulbs of the LCD backlighting. V81 is used as short-circuit protection for V80.

A control signal with a constant pulse duration Tp = 0.25 ms and a pulse repetition rate depending on the selected brightness is output at TIMER-0 output D4.22 of the microprocessor.

Basic signal characteristic at D4.22:



The pulse control voltage is smoothed via RC network R76, C93.
The DC component provides the smallest output voltage at f = 470 Hz and the highest output voltage at f = 4 kHz.

7.1.8 IEC-bus Interface

The IEC-bus controller D30 performs all control tasks for the IEC-bus interface under processor control. The processor provides the system clock with the CLOCK-OUT square-wave signal 8 MHz (D4.56 → D30.3). The bidirectional drivers D31 and D32 provide for a standard termination of the 8 data lines, 5 control lines and 3 handshake lines at the 24-way IEC-bus connector X30.

7.1.9 Peripheral Control of the In/Out Option NRVD-B2

The input/output signals for the option are applied to connector X60 of the computer board (X60.A1 to B13, → In/Out-Option NRVD-B2, section 7.1).

Connector X60.B17 is used to indicate whether the option is installed in the instrument. After switching on the instrument, the processor reads in the current status:

PI1 → H: X60.B17 is open
→ Option is installed

PI1 → L: X60.B17 is short-circuited to ground via the connection to X60.B1
→ Option no installed

The remaining connections of X60 are provided for R&S-internal test purposes.

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Required characteristics	Appropriate R&S instrument	Order No.
1	Digital voltmeter	DC, 0 to 10 V, ± 0,5 %	UDS5	349.1510.02
2	Oscilloscope	DC to 100 MHz, 2 channels	BOL	374.2000.02
3	Frequency counter	10 Hz to 30 MHz, ± 0.0005%	NRVD	350.5315.03
4	IEC-bus controller		PSA5	1006.3008.04

7.3 Troubleshooting

For troubleshooting, use the following flow charts and internal diagnostic tools. The fault is then exactly located by means of the circuit diagram.

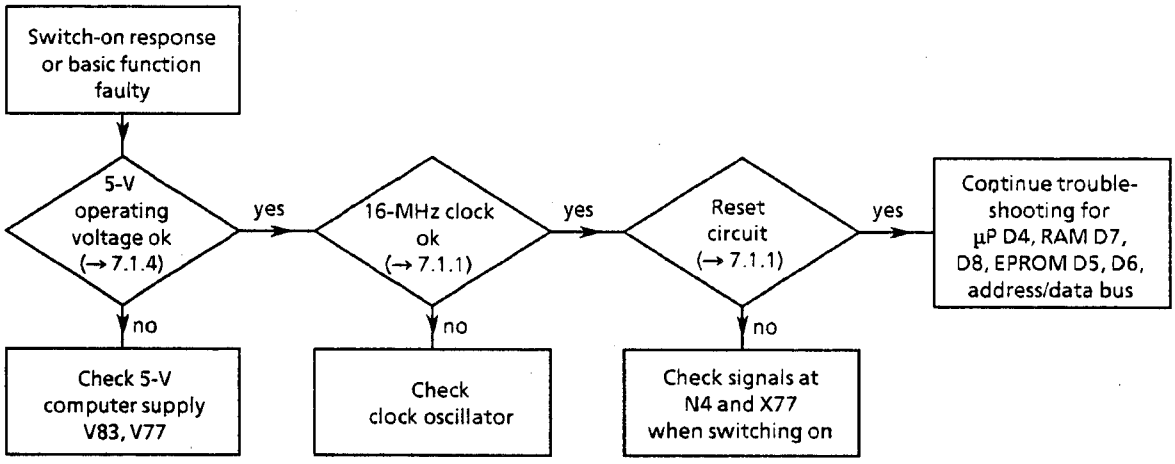
7.3.1 Switch-on Response or Basic Computer Function Faulty

Diagnostic tool:

Device-Err	Cause	Possible error and remedy
0001	Checksum error of EPROMs	Replace EPROMs D5, D6

Note: This error message assumes that the processor has been switched on properly; it can be output only in certain cases depending on the program run.

Troubleshooting flow chart:



7.3.2 Optocoupler Interface to Analog Board Faulty

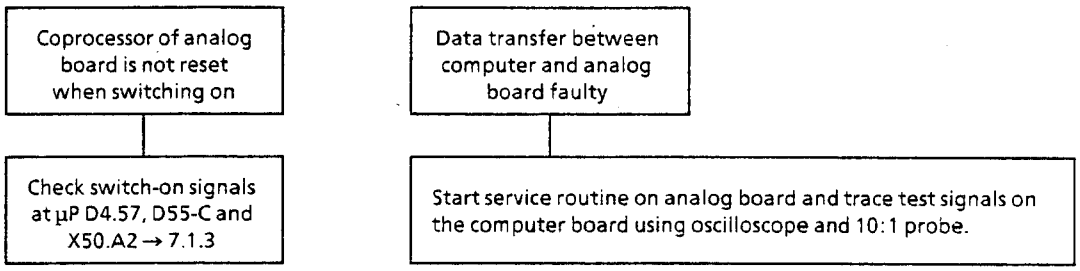
Diagnostic tools:

Automatic error indication on the display: DEVICE-ERROR *___

Device-Err	Cause	Possible fault and remedy
0010	Time exceeded when sending to analog board	Check data interface computer/analog board
0020	Time exceeded when receiving from analog board	Check data interface computer/analog board
0040	Error in data transfer from analog board to computer board	Data transfer disturbed, check ribbon cable connection X50, optocoupler U50-A and peripheral devices
0080	Parity error in data transfer from analog board to computer board	Check serial interface to analog board, trigger service routine (A2 analog board, see Section 7.3.2.2.2).
0100	Hardware error in analog board or interface to analog board	Further diagnosis via IEC-bus command "DIAG:AHAR?" → Operating manual 3.8.8.3.3, service manual 7.3/A2 Analog Board. If bit EH = 1 → hardware error on analog board. Check optocoupler interface.

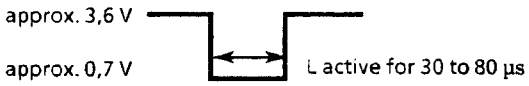
Service routine in µP program of analog board:

To start the service routine, connect shorting plug to service plug X710 of the analog board. Test signals are generated on the analog board and transferred to the computer board via the optocoupler (→ Analog board A2, section 7.3)



Enable single INT signal by pressing the →MEAS key:

Oscillogram at D55.6:
with DC coupling

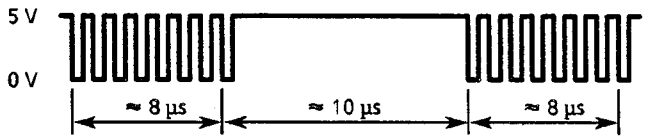


Oscillogram at X50.A3:
with AC coupling

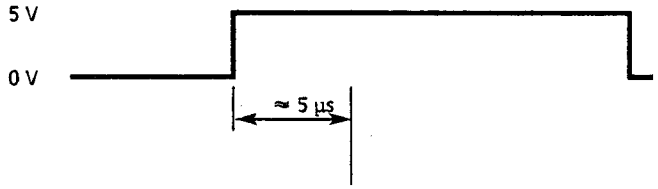


Troubleshooting at: Output port D40 and control,
driver D55-B, ribbon cable connection X50,
optocoupler U704 on analog board

Oscillogram at U50.6:
Period length approx. 82 µs



Oscillogram at D56.6:
Period length approx. 82 µs

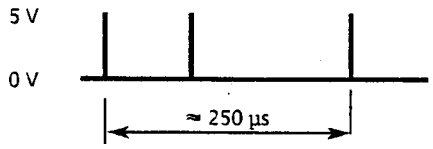


Oscillograms at U50.7:
Period length approx. 82 µs



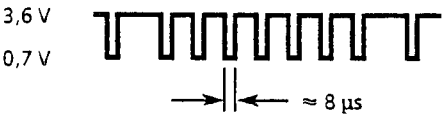


Oscillogram at D51.19, D52.19:
PCS2 signal



Oscillogram at D55.3:

Low level at D700.8 or U704.6 in analog board (short circuit to ⊥)



Troubleshooting at: optocoupler U50, gate function D33, D53, D54
driver D55-A, binary counter D56
shift registers D51, D52, ribbon cable connection X50, W150

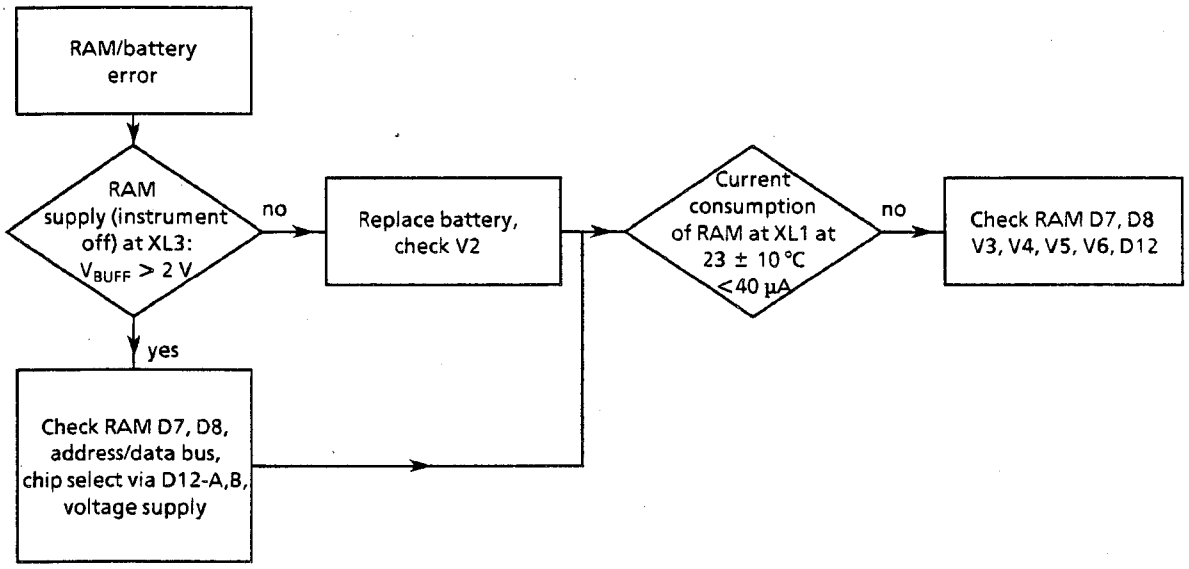
7.3.3 Fault in RAM, Buffer Battery and Voltage Supply Function

Diagnostic tools:

Automatic error indication on the display: DEVICE-ERROR * _ _ _ _

Device-Err	Cause	Calibration data missing
0002	Calibration data missing	RAM error Replace RAM D7, D8 recalibrate instrument → Service manual Kap. 6.3
000E	Battery defective ("BATT LOW" display) RAM and calibration data missing	Replace battery G1, recalibrate instrument → Operating manual, section 4.1.2 and Service manual Kap. 6.3 section 7.3.2.1 /A2 Analog board

Troubleshooting flow chart:



7.4 Checking and Adjustment

7.4.1 Checking the Operating Voltages

Test point - ref.	Voltage	Tolerance	Remark
X78 - ground X88	+ 5 V	± 0.15 V	Current supply digital section Reference potential: computer shielding panel and instrument case
X84 - ground X86	approx. 8 V	---	High-end voltage for 5-V digital section
X3 - ground	4.9 V 2.3 to 3.5 V	≤ 0.2 V to + 5 V (X78)	RAM supply, V_{BUFF} Instrument On Instrument Off
X76 - ground	0.7 to 5 V	---	for LCD illumination
X71 - GND1	U1 (+ 15 V)	± 0.75 V	Current supply analog section A2 board
X72 - GND1	U2 (- 15 V)	± 0.75 V	Reference: analog potential (outer conductor BNC input)
X73 - GND1	U3 (+ 5 V)	± 0.15 V	Isolated to computer

7.4.2 Checking the Clock Frequency for the Microprocessor

For the measurement, connect a frequency counter via a 10:1 probe to the output of the clock oscillator at test point X1.

Measure clock frequency: 16 MHz ± 1.6 kHz (0.01 %) *)

*) Component specification D3 - note additional measuring inaccuracy of the counter used!

7.5 Dismantling and Reassembling of the Computer Board

7.5.1 Removal and Replacement of the Computer Board

(See also exploded view)

Removal:

- Remove the two rear-panel feet and upper instrument cover (item 17 + 18, 4 scews and item 1)
- Remove the I/O board of the In/Out Option (section 7.5 of In/Out Option NRVD-B2).
- Remove cable plug from X40, X50, X70 and X80, swivel back the safety levers of X40.
- Remove the 2 screws of IEC-bus connector X30.
- Loosen and remove controller N5
- Remove the 5 screws with washers fastening the computer board; be careful not to short-circuit the battery with the screw in the vicinity of G1.
- Slightly lift the computer board at the front, push towards the front of the instrument and take out.

Caution when handling the board!

After removing the computer board, some circuit parts are still connected to the battery voltage.

Replacement:

To replace the computer board, proceed in the reverse order to removal.

7.5.2 Hints for Replacing Components

Voltage controller	N2:	Electrically isolated from shielding panel
Transistor	V80:	Electrically isolated from shielding panel
Voltage controller	N5:	Note original mounting height

7.6 Interfaces

Pin	Name	Input/ output	Origin/destination		Value range	Signal description
X30.1...24	IEEE 488 IEC bus	Input/ output	IEC-bus connection rear of instrument		TTL level ground 0 V	Signal acc. to IEEE 488 or DIN IEC 625 standard
X40.A16 X40.B16	+ 5 V	Output	A3, Display,	X1.32 X1.31	4.85 to 5.15 V	Supply voltage
X40.B15 X40.A17 X40.B17	GND		A3, Display,	X1.29 X1.34 X1.33	0 V	Ground
X40.A9	RESET 0*	Output	A3, Display,	X1.18	0.7 to 4.5 V	Reset for key contr. KEYINT.
X40.A3	PO12	Output	A3, Display,	X1.6	HCMOS level	Reset for LCD drivers
X40.B14 X40.A15	LCD-ILLUM	Output	A3, Display,	X1.27 X1.30	0.7 to 5 V	LCD illumination variable brightness
X40.B13	LED0/A3	Output	A3, Display,	X1.25	0/5 V	
X40.A14	LED1/A2	Output	A3, Display,	X1.28	0/5 V	Address 2
X40.A4	INT1	Output	A3, Display,	X1.8		Interrupt
X40.B2	A0*	Output	A3, Display,	X1.3		Address 0
X40.A2	A1*	Output	A3, Display,	X1.4		Address 1
X40.B1	RD*	Output	A3, Display,	X1.1		Read enable
X40.A1	WR*	Output	A3, Display,	X1.2		Write enable
X40.B8	PCS3	Output	A3, Display,	X1.15	Inputs: L = 0 to 0.8 V H = 2 to 5 V	Chip select
X40.A8	D0*	Inp./outp.	A3, Display,	X1.16		
X40.B7	D1*	Inp./outp.	A3, Display,	X1.13	Outputs: L = 0 to 0.4 V H = 4.6 V min.	
X40.A7	D2*	Inp./outp.	A3, Display,	X1.14		
X40.B6	D3*	Inp./outp.	A3, Display,	X1.11		
X40.A6	D4*	Inp./outp.	A3, Display,	X1.12		Data bus for key controller
X40.B5	D5*	Inp./outp.	A3, Display,	X1.9		
X40.A5	D6*	Inp./outp.	A3, Display,	X1.10		
X40.B4	D7*	Inp./outp.	A3, Display,	X1.7		
X40.A12	CS1	Output	A3, Display,	X1.24		
X40.B11	CS2	Output	A3, Display,	X1.21		Chip select for LCD drivers D1 to D4
X40.A13	CS3	Output	A3, Display,	X1.26		
X40.A11	CS4	Output	A3, Display,	X1.22		
X40.B10	SCK	Output	A3, Display,	X1.19	CMOS level	Serial Clock
X40.B12	BUSY	Input	A3, Display,	X1.23		Feedback
X40.B9	C/D	Output	A3, Display,	X1.17		Command/Data
X40.A10	SI	Output	A3, Display,	X1.20		Serial Input

Control lines for key controller

Control lines of 4 LCD drivers

Pin	Name	Input/ Output	Origin/destination	Value range	Signal description
X50.A10 X50.B6	GND1		A2, Anal.board, X102.20 X102.11	0 V	Analog ground 1
X50.B10	GND2		A2, Anal.board, X102.19	0 V	Analog ground 2, Power Return
X50.A9	+ 15 V	Output	A2, Anal.board, X102.18	14.25 to 15.75 V	Supply voltage, analog
X50.B9	-15 V	Output	A2, Anal.board, X102.17	-14.25 to -15.75V	Supply voltage, analog
X50.A8 X50.A7 X50.A6	+ 5 V VCC1 VCC2	Output Input Input	A2,Anal.board, X102.16 X102.14 X102.12	4.85 to 5.15 V	Supply voltage, analog + 5 V analog + 5 V analog
X50.A5 X50.B1	GND0		A2, Anal.board, X102.10 X102.1	0 V	Ground, casing
X50.B5 X50.B4 X50.B3 X50.B2	VCC3 VCC4 VCC5 VCC6	Output	A2, Anal.board, X102.9 X102.7 X102.5 X102.3	4.85 to 5.15 V	Supply voltage + 5 V digital
X50.B8	CLOCK	Output	A2, Anal.board, X102.15	┐ │ │	Clock signal for data interface analog board
X50.B7	DATUM2	Input	A2, Anal.board, X102.13	│ ┘	Data input
X50.A4	DATUM1	Output	A2, Anal.board, X102.8	L: 3 to 8 mA H: 0 to 0.5 mA	Data input
X50.A3	INT	Output	A2, Anal.board, X102.6	Level appr. 3.6 V	Interrupt
X50.A2	RESET	Output	A2, Anal.board, X102.4	│ │	Reset for D751
X50.A1	EXT FRQ	Output	A2, Anal.board, X102.2	┘	
X60.B2	+ 5 V	Output	In/Out Option NRVD-B2, X9.3	4.85 to 5.15 V	Supply voltage, digital
X60.A1 X60.A2 X60.B1	GND		In/Out Option, X9.2 In/Out Option, X9.4 In/Out Option, X9.1	0 V	Ground
X60.A4	PCS6	Output	In/Out Option, X9.8	┐ │	Chip select
X60.A5	WR	Output	In/Out Option, X9.10	HCMOS level │	Write enable
X60.B4	A1	Output	In/Out Option, X9.7	┘	Address line
X60.B8	D0	Output	In/Out Option, X9.15	┐	┐
X60.A8	D1	Output	In/Out Option, X9.16	│	│
X60.B9	D2	Output	In/Out Option, X9.17	│	│
X60.A9	D3	Output	In/Out Option, X9.18	│	│
X60.B10	D4	Output	In/Out Option, X9.19	│	│
X60.A10	D5	Output	In/Out Option, X9.20	HCMOS level	Data bus for DAC
X60.B11	D6	Output	In/Out Option, X9.21	│	│
X60.A11	D7	Output	In/Out Option, X9.22	│	│
X60.B12	D8	Output	In/Out Option, X9.23	│	│
X60.A12	D9	Output	In/Out Option, X9.24	│	│
X60.B13	D10	Output	In/Out Option, X9.25	│	│
X60.A13	D11	Output	In/Out Option, X9.26	┘	┘

Pin	Name	Input/ Output	Origin/destination	Value range	Signal description
X60.B5	INT3	Input	In/Out Option X9.9	┐	Interrupt from ext. trigger
X60.B6	FREQ IN	Input	In/Out Option, X9.11	¦	not connectet
X60.A6	PO8	Output	In/Out Option, X9.12	HCMOS level	Ready out
X60.A7	PO9	Output	In/Out Option, X9.14	¦	On/off frequency input
X60.B7	PO10	Output	In/Out Option, X9.13	┘	32:1 frequency divider
X60.A3	U0	Output		approx. 8 V	High-end voltage for 5 V digital
X60.B3	RESET0	Output		0 to 4.5 V	Reset line
X60.B14	D12	Inp./outp.		┐	┐
X60.A14	D13	Inp./outp.		¦	¦
X60.B15	D14	Inp./outp.		HCMOS level	Data bus
X60.A15	D15	Inp./outp.		¦	¦
				┘	┘
X60.A18	A0	Output		┐	┐
X60.A19	A2	Output		¦	¦
X60.B19	A3	Output		¦	¦
X60.A20	A4	Output		¦	¦
X60.B20	A5	Output		¦	¦
X60.A21	A6	Output		¦	¦
X60.B21	A7	Output		¦	¦
X60.A22	A8	Output		¦	Address bus
X60.B22	A9	Output		¦	¦
X60.A23	A10	Output		¦	¦
X60.B23	A11	Output		HCMOS level	¦
X60.A24	A12	Output		¦	¦
X60.B24	A13	Output		¦	¦
X60.A25	A14	Output		¦	¦
X60.B25	A15	Output		¦	┘
X60.A16	MCS0	Output		¦	┐
X60.B16	MCS1	Output		¦	¦
X60.A17	RD	Output		¦	Control signals
X60.B18	BHE	Output		¦	¦
				┘	┘
X60.B17	PI1 (DRQ1) (A16)	Input Input Output	Jumper ⊥ to X60.B1: Opt. not installed in NRVD	0/5 V	Option identification NRVD-B2
X70.6		Input	Power transformer, Low voltage, analog potential	V_{ac} approx. 18 V to GND2	┐ High-end voltage for
X70.4		Input		V_{ac} approx. 18 V I approx. 0.3 A	± 15 V analog supply ┘
X70.5	GND2	Input		0 V	
X70.2		Input		┐	High-end voltage for
X70.1		Input		V_{ac} approx. 8 V I approx. 0.2 A	5 V analog supply
X80.2		Input	Power transformer, Low voltage, computer potential	V_{ac} approx. 7 V I approx. 0.9 A	High-end voltage for
X80.1		Input		┘	5 V digital supply

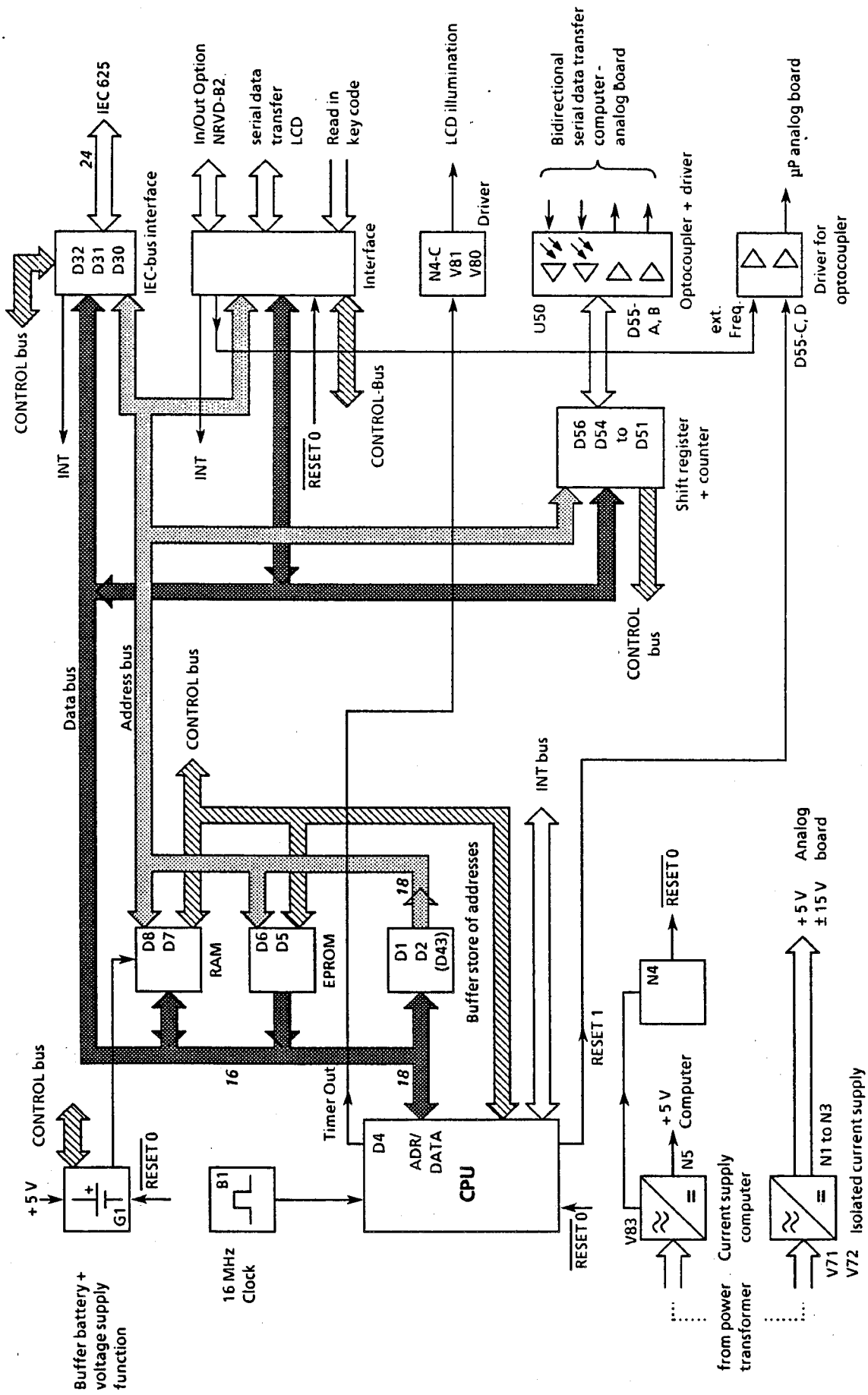


Fig. 7-1 Block diagram NRVD computer

FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR

D3-A 74HC04 OR CLOCK-GENERATOR

D4 80C186

D1-A 74HC573

D6-A D27256/512

D5-A D27256/512

D2-A 74HC373

D6-B 74HC75

D10-A 74HC10

D10-B 74HC10

D9-A 74HC27

D11-A 74HC32

D1-B D2-B D3-G D4-B D5-B D10-D D11-E D11-B D7-B D8-B D11-F D11-D

STROMLAUF

A	
REND. IND.	AI ND M111

D1-A 74HC573
R1 10K
X9 XL
R2 10K
D2-A 74HC573
R3 10K
D46-B 74HC75
R4-B
R5-B
R12-B 4K7 9XC
RESET1
D6-A D27256 /512
D5-A D27256 /512
R14 4K75
R13 0R
R18 4K75
R17 4K75
R15 0R
R16 0R
D10-A 74HC10
D10-B 74HC10
D9-A 74HC27
D11-A 74HC32
R24 0R
R23 0R
R22 4K75
V1 1N4448
C1 1N
V5 BCY59-9
R25 2K21
V4 BCY79-9
X3 XL
V BUFF
V3 5082-2800
V2 5082-2800
C2 10N
C3 1U
R21 4K75
R29 2M
R37 10M
X1 XL
G1 3V4
X2 XL
R20 4K75
D12-C 74HC132
V6 5082-2800
R19 10K
D8-A HM6264LP15
D7-A HM6264LP15
D9-B 74HC27
D9-C 74HC27
D12-B 74HC132
D12-A 74HC132
D10-C 74HC10
R28 10K
ADDR
DATA
INT
CONTROL
D10-D
C10 100N
D11-E
R69 10K
D11-D 74HC32
D7-D
D8-D
D11-F
V BUFF
D12-D 74HC132
R67 2K21

STROMLAUF GILT FUER VAR.02 CIRCUIT DIAGRAM IS VALID FOR MOD.02

A	---	03.88	LI	1KGU	TAG	NAME	BENENNUNG
				BEARB.		LI	RECHNER
				GEPR.		LI	PROCESSOR
				NORM			
				PLOTT	12.10.88	*	
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR. 350.5867.01S
				ZU GERRET	URE3		REG.I.V. 350.5315 ERSTE Z.

BLATT-NR. 1 V. 5 BL.

IEC BUS

DISPLAY/KEYBOARD

REAR PANEL
GERAETE RUECKWAND
SHIELD
X31 1
X30 12 18 19 20 21 22 23 24
X30 16 15 14 13 4 3 2 1
X30 10 11 5 6 7 8 9 17
D7 D6 D5 D4 D3 D2 D1 D0
SRQ ATN EOI DAV NRFD NDAC IFC REN

R31 1K
D30-A UPD7210C
CLK OUT
RES CLK CS RD WR A3 A2 A1 A0 INT REQ DMA REQ DMA ACK
INTO DRQ0
D0 D1 D2 D3 D4 D5 D6 D7
DIO8 DIO7 DIO6 DIO5 DIO4 DIO3 DIO2 DIO1
T/R3 T/R1 T/R2
SRQ ATN EOI DAV NRFD NDAC IFC REN

D31-A SN75160AN
TE PE D8 D7 D6 D5 D4 D3 D2 D1 B8 B7 B6 B5 B4 B3 B2 B1

D32-A SN75161AN
TE DC SRQ ATN EOI DAV NRFD NDAC IFC REN

D33-B 74HC132
D33-C 74HC132
D54-D 74HC32
R30 1K
V30 5082-2800
C30 150

ADDR
DATA
INT
CONTROL
PCS5

INT1
RESET 0S
X40A 4
X40A 9
X40B 2 X40A 2
X40A 1 X40B 1
X40B 8
X40B 4 X40A 5 X40A 6 X40A 7 X40B 7 X40A 8
X40A 10 X40B 9
X40B 10
X40A 12
X40B 11
A0* A1* WR* RD* D7* D6* D5* D4* D3* D2* D1* D0*

+5V
R46 4K75
R47 4K75

D47-A 74HC367
EN1 EN2

D11-D 74HC32
R48 10K
C48 10n

D48-A 74HC245
G3 3EN1 3EN2

D45-A 74HC75
1D C1 C2 2D
C/D SCK CS1 CS2

D44-B 74HC00
D44-A 74HC00
R40 10K

D42-D 74HC32
D43-A 74HC04
D42-C 74HC32
D42-B 74HC32
D43-F 74HC04
D43-E 74HC04

D40-A 74HC259
E CLR A0 A1 A2 D Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7

D40-B D31-B D32-B D41-F D40-E D41-E D40-A D47-F D43-G D44-F D46-G D47-A D48-A
C31 100N C32 100N C41 100N C42 100N C43 100N C44 100N C49 100N

R37 10K
D44-A D44-B D44-C D44-D

A
REND. IND.

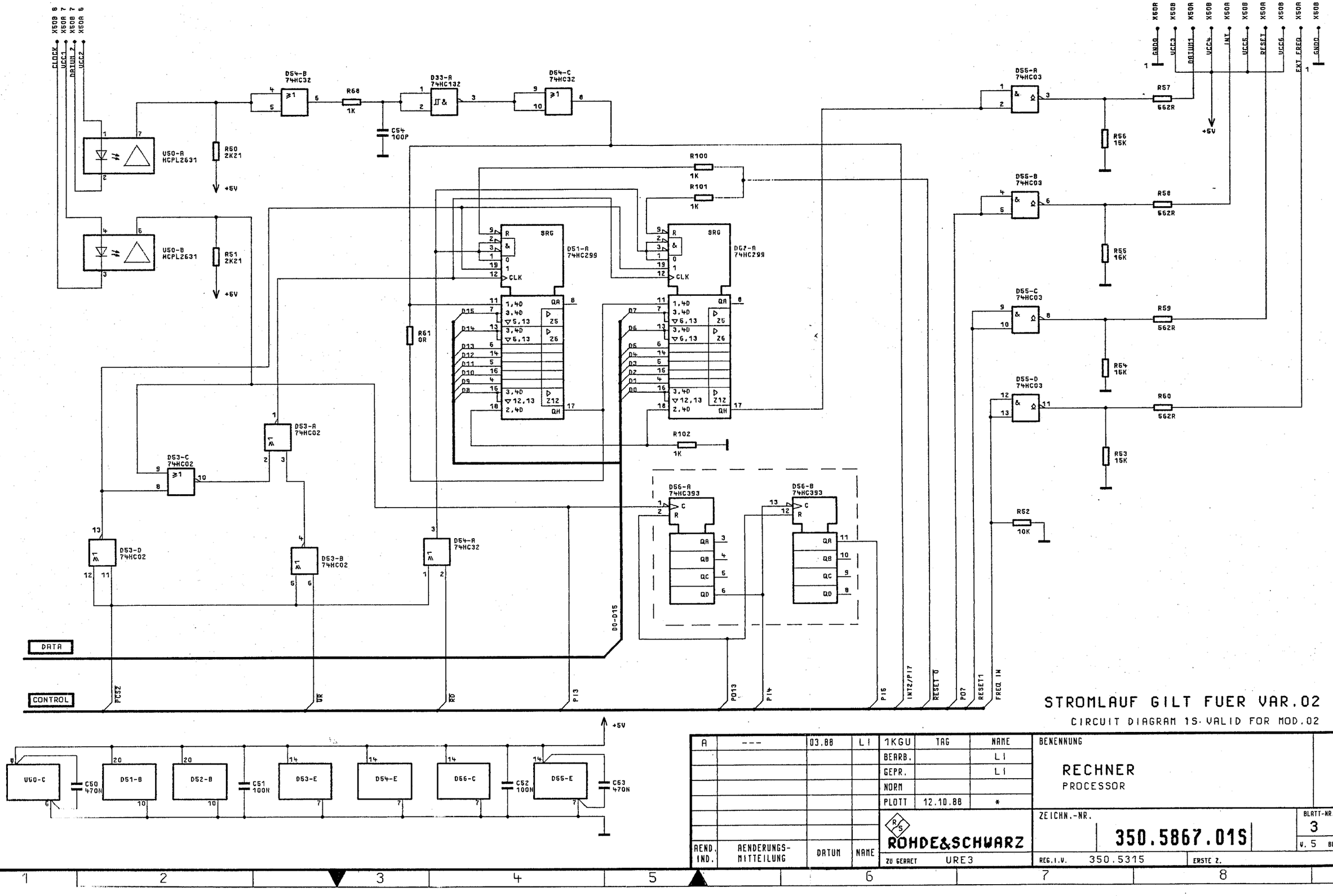
DISPLAY/KEYBOARD

STROMLAUF GILT FUER VAR.02 CIRCUIT DIAGRAM IS VALID FOR MOD.02

A	---	03.88	LI	1KGU	TAG	NAME	BENENNUNG
				BEARB.		LI	RECHNER
				GEPR.		LI	PROCESSOR
				NORM			
				PLOTT	12.10.88	*	
				R/S ROHDE&SCHWARZ			ZEICHN.-NR. 350.5867.01S
				ZU GERAET URE3			REG.I.V. 350.5315
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME				ERSTE Z.

BLATT-NR. 2 V. 5 BL.

INTERFACE ANALOGTEIL



STROMLAUF GILT FUER VAR.02

CIRCUIT DIAGRAM IS VALID FOR MOD.02

A	---	03.88	LI	TKGU	TAG	NAME	BENENNUNG
				BEARB.		LI	RECHNER
				GEPR.		LI	PROCESSOR
				NORM			
				PLOTT	12.10.88	*	
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR. 350.5867.01S
				ZU GERRET	URE3		REG.I.V. 350.5315

BLATT-NR. 3 v. 5 BL.

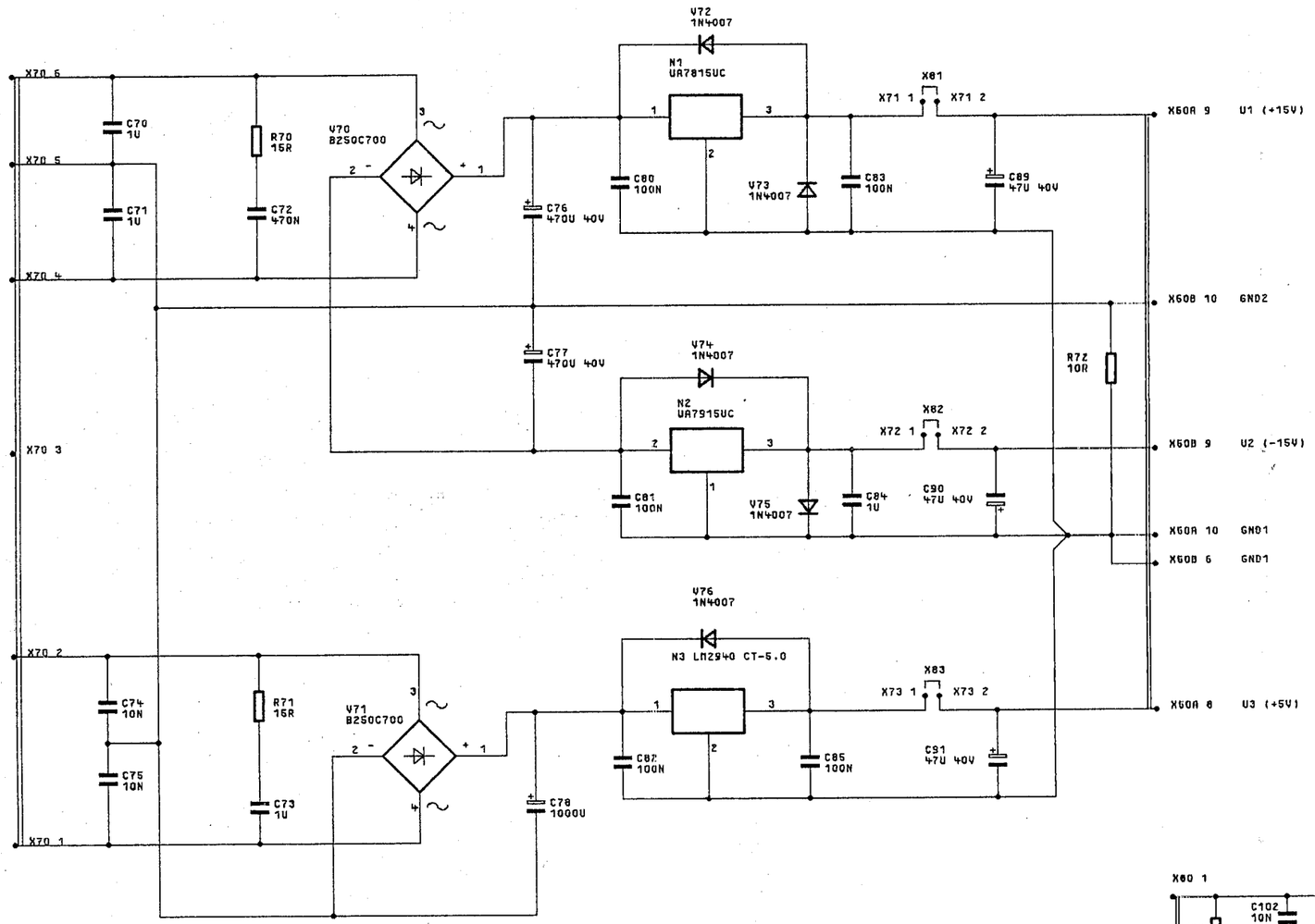
ERSTE Z.

FUER DIESE UNTERLAGE BEHALTEN WIR UNS ALLE RECHTE VOR

ZEICHN.-NR.

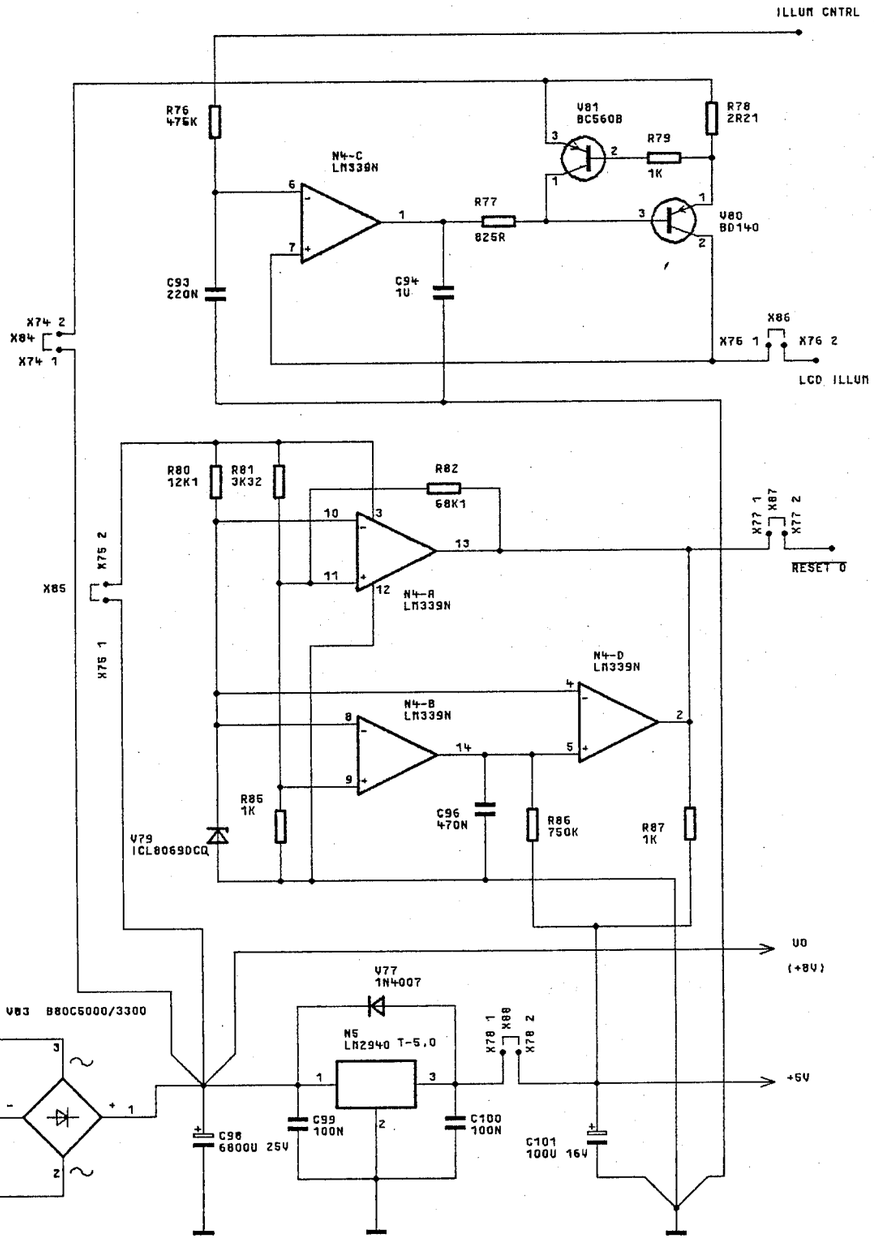
SPANNUNGSVERSORGUNG FUER ANALOGTEIL

POWER SUPPLY FOR ANALOG SECTION



SPANNUNGSVERSORGUNG FUER DIGITALTEIL

POWER SUPPLY FOR DIGITAL SECTION



FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR

ZEICHN.-NR.

ACHTUNG: EGB!

ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.

ATTENTION: ESD!

ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING.

STROMLAUF GILT FUER VAR.02

CIRCUIT DIAGRAM IS VALID FOR MOD.02

AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME
A	---	03.88	LI
B	—	4.89	Li

1KGU	TRG	NAME
BEARB.		LI
GEPR.		LI
NORM		
PLOTT	24. 4.89	*

ROHDE&SCHWARZ

ZU GERAET URE3

BENENNUNG

RECHNER
PROCESSOR

ZEICHN.-NR. 350.5867.01S

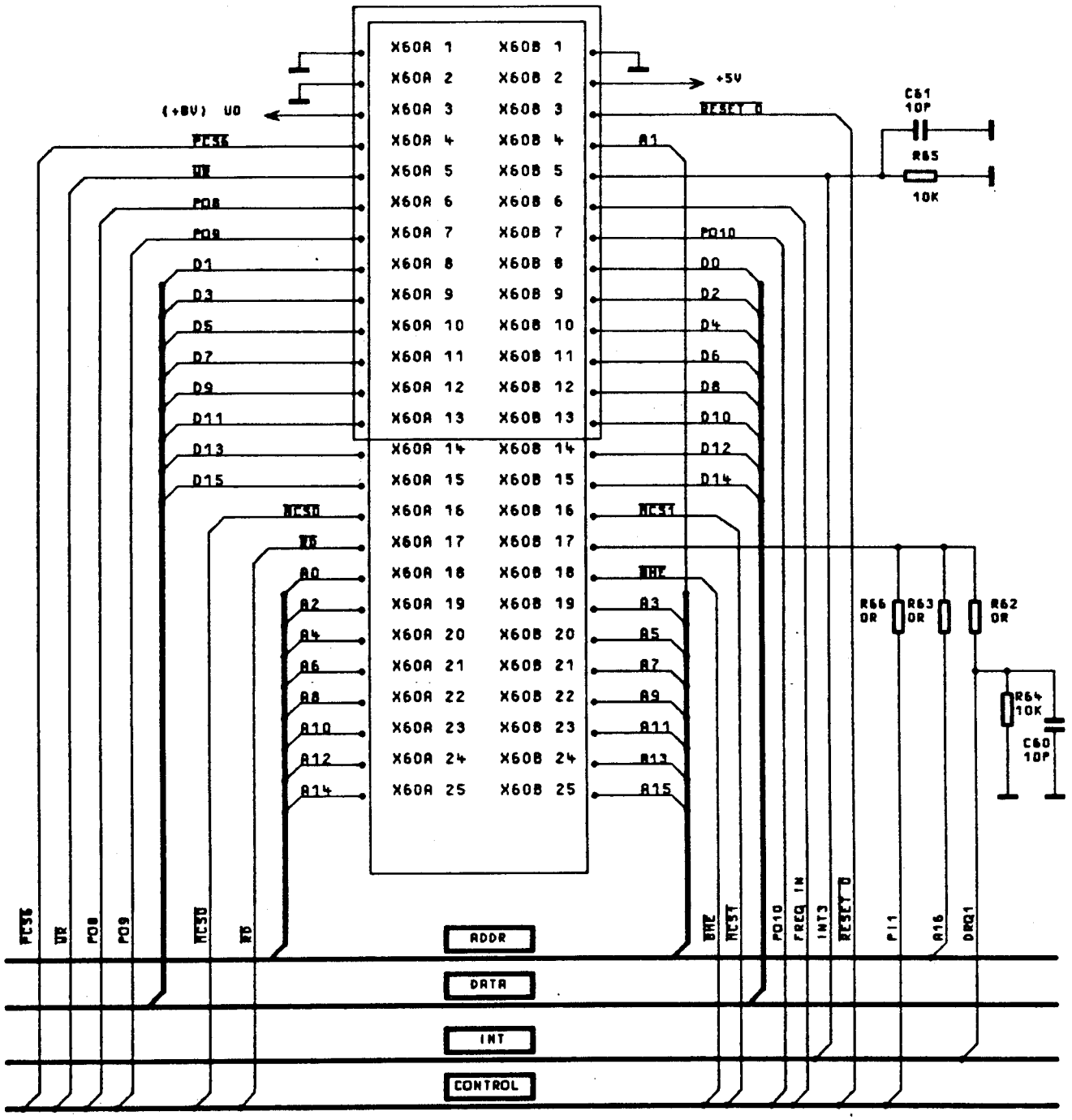
BLATT-NR. 4

REG.I.V. 350.5315

ERSTE Z.

FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR

INTERFACE - OPTION



STROMLAUF GILT FUER VAR.02 CIRCUIT DIAGRAM IS VALID FOR MOD.02

A	---	03.88	LI	1KGU	TAG	NAME	BENENNUNG
				BEARB.		LI	RECHNER
				GEPR.		LI	PROCESSOR
				NORM			
				PLOTT	12.10.88	*	
REND. IND.	RENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GEMAET	URE3		

ROHDE&SCHWARZ

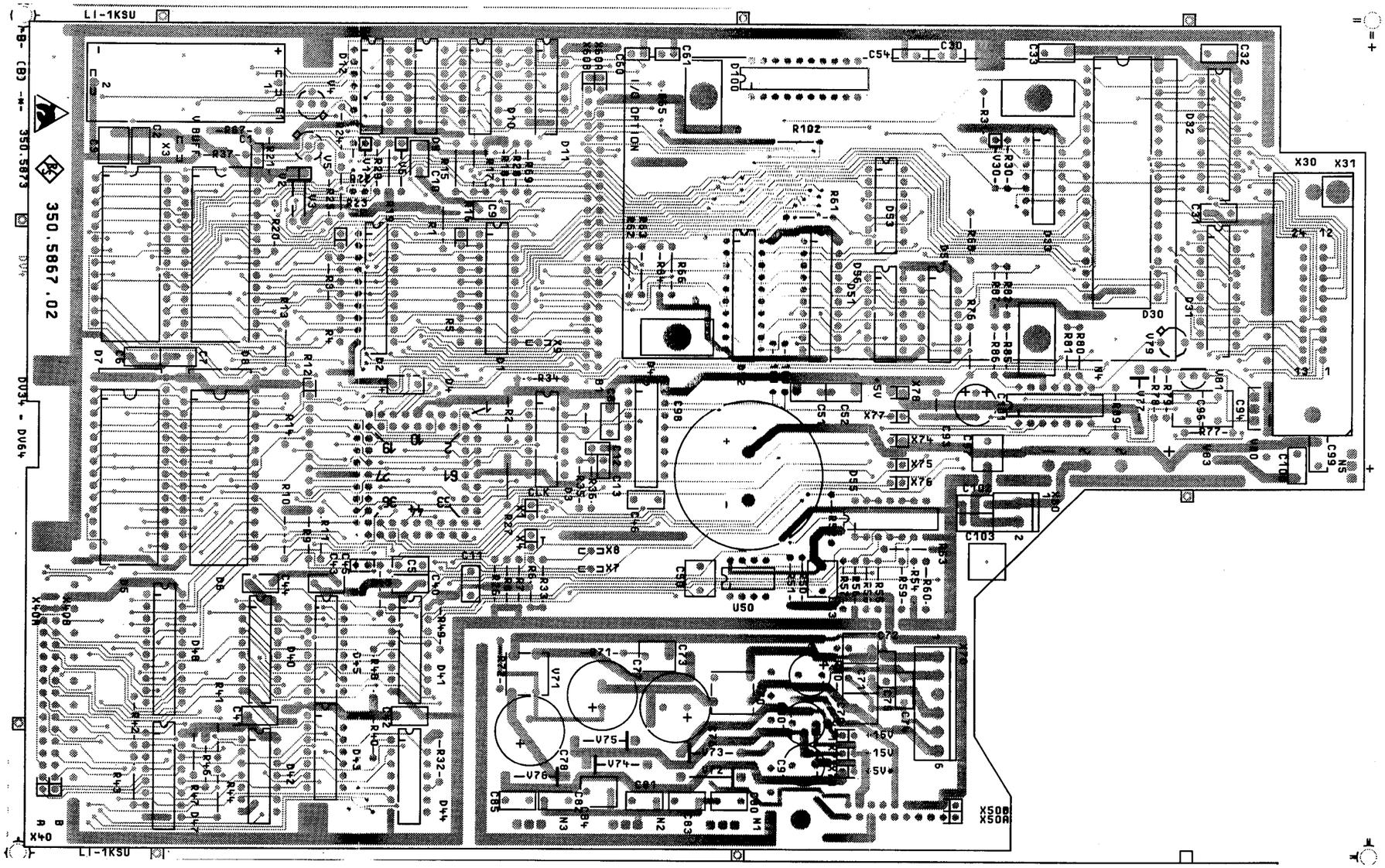
ZEICHN.-NR. 350.5867.01S

BLATT-NR. 5 V. 5 BL.

REG.I.V. 350.5315 ERSTE Z.

ZEICHN.-NR.

Ansicht und Leitungsführung Bauteilseite
View of tracks on component side



VARIANTENERKLÄRUNG/VERSION
VAR 02 – GRUNDAUSFÜHRUNG/BASIC MODEL

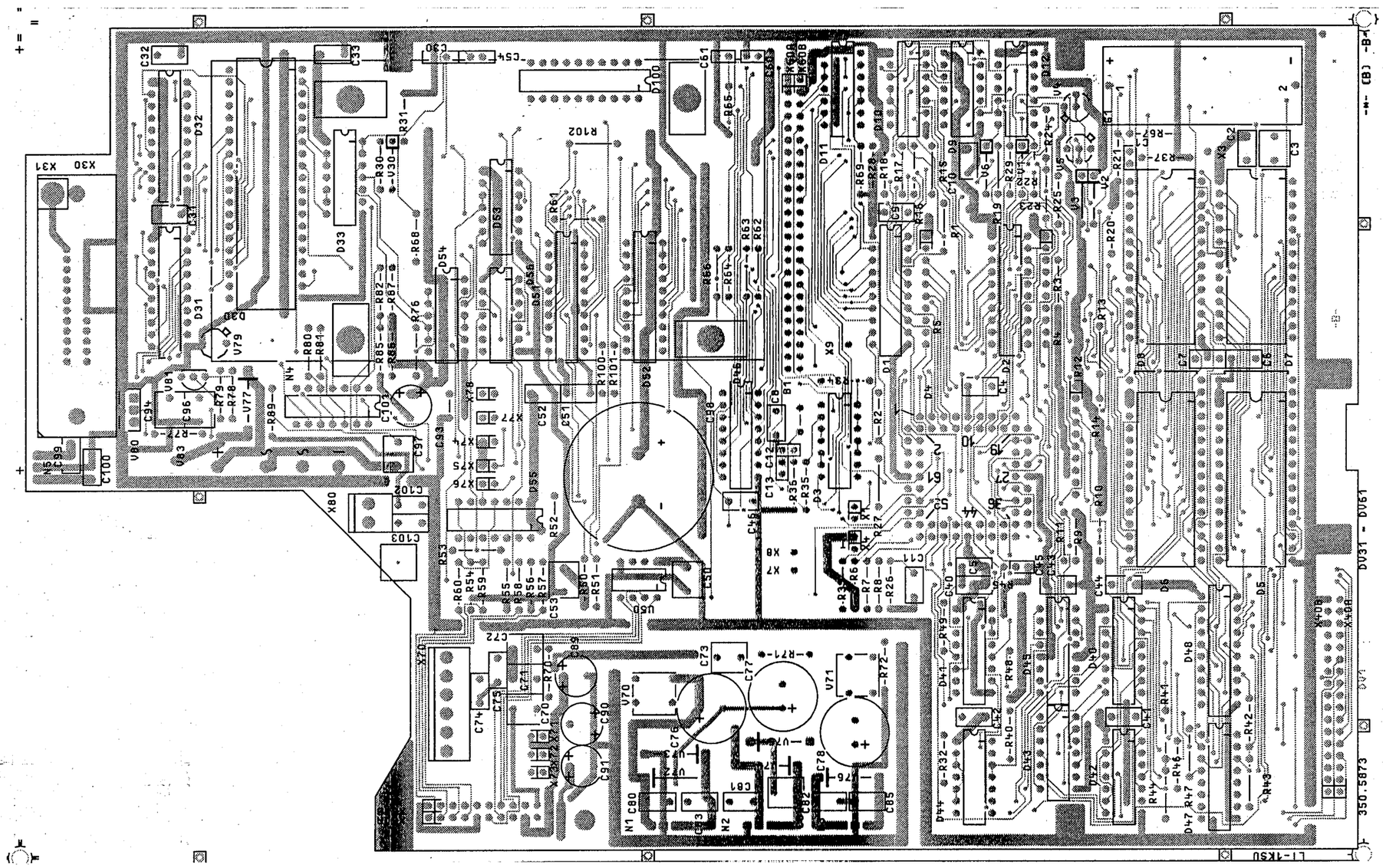
ACHTUNG: EGB!
Elektrostatisch gefährdete Bauelemente erfordern eine besondere Handhabung.
ATTENTION ESD!
Electrostatic sensitive devices require a special handling.
(hierzu HVC 250)

A		9.88	Li	Maße ohne Toleranzangabe		Maßstab 1 : 1	
						Halbzeug, Werkstoff	
				1KGU	Tag	Name	Benennung: RECHNER Processor — Z
				Bearb.	10.88	LI	
				Gepr.			
				Norm			
				ROHDE&SCHWARZ			Zeichn.-Nr. 350.5867.02 — Blatt-Nr. 2 v. Bl.
And Zust	Änderungs-Mitteilung	Tag	Name	zu Gerat URE 3		reg. i. V. 350.5315 V	erste Z.

Für diese Unterlage behalten wir uns alle Rechte vor.

11 6107 87

Ansicht und Leitungsführung Lötseite
View of tracks on solder side



VARIANTENERKLÄRUNG/VERSION
VAR 02 – GRUNDAUSFÜHRUNG/BASIC MODEL

A		9.88	Li	Maße ohne Toleranzangabe		Maßstab 1 : 1
						Halbzeug, Werkstoff
				1KGU	Tag	Name
				Bearb.	10.88	LI
				Gepr.		
				Norm		
				ROHDE&SCHWARZ		Benennung: RECHNER / Processor — Z
				zu Gerät URE 3		Zeichn Nr. 350.5867.02 — Blatt-Nr. 3 v. Bl.
And. Zust.	Änderungs-Mitteilung	Tag	Name			Ers. f. V 350.5315 V — erste Z.

(hierzu HVC 250)

ACHTUNG: EGB!
Elektrostatisch gefährdete Bauelemente erfordern eine besondere Handhabung.

ATTENTION ESD!
Electrostatic sensitive devices require a special handling.

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ROHDE&SCHWARZ

SERVICE INSTRUCTIONS

Analog Board

857.8150.02

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Part lists
Circuit diagrams
Component plans

7 Testing and Repair of the Analog Board A2

7.1 Function Description

(circuit diagram 857.8008.01, 0857.8150.01, sheet 1)

The analog unit contains two independent amplifiers for RF probes, one current-voltage converter for DC probes, which can be switched over at the input and one A/D converter with series-connected analog multiplexer. The plug-in probes are supplied by two independent voltage sources. The test generator with an output power calibrated to 1 mW with 50 MHz is provided for testing the RF probes.

Control of the hardware latches, the automatic offset adjustment of the amplifiers as well as communication with the controller board A1 and data transfer between the analog board and sensors connected is controlled by the onboard controller (D751, D707 to D709). Data transmission to the boards connected (controller, power sensors) is realized via a serial controller interface, the switchover is carried out by the programmable serial multiplexer of the customized circuit Volcon (D700). Programming is executed via the address bus and the parallel 8-bit data bus. Setting data are also transmitted via the parallel data bus controlled by the address decoder D705, the data are stored in the hardware latches of the analog function blocks. The block diagram of the Volcon circuit (fig. 7-2) illustrates that further functions are integrated apart from the multiplexer. The two independent monitoring logics of the sensor registrate each change of sensor and simultaneously switch off the voltage supply for the test channel concerned. When a sensor is reconnected, the sensor-specific voltage supply is switched on again according to the program. The voltage supply is set to 5 V for all measuring heads for readout of the data. Subsequently, the voltage for the passive sensors is switched off, the voltage for the active sensors is set to ± 12 V. The RST connector of the Volcon (D700.19) prevents unpermitted voltages for measuring heads which might be connected from being switched on with power-on of the instrument.

The oscillator of the Volcon provides the clock signal for the analog controller as well as for the counter chain and run control of the integrating A/D converter. The resolution and measuring time of the A/D converter (N602, U601, D601, D700) is optimally adapted to the measuring task due to the programmability of the sequence control and the cycle counter.

7.1.1 AC Amplifiers

(circuit diagram 857.8150.01, sheets 2,4)

The output signals of the RF power or voltage sensors connected are applied via the input filters to the respective AC amplifier of each channel (A or B). Since the two AC amplifiers are built up identically as instrument amplifiers (numbering of the components in channel A starting with 200 corresponds to the numbering in channel B starting with 400), which is why only the AC amplifier A is described in detail.

It depends on the type of measuring head whether the DC test signal supplied by the power sensor is unipolar or bipolar referred to the ground reference of the AC amplifier. This signal is routed via the input filters (filter board, circuit diagram 857.8308.01) and analog multiplexers (V228, V229, V237-V239, V243, V244) to the input of the amplifier (X211.1,2). The FET transistors V240 and V242 limit the input signal to approx. 2 V. The load of the diode measuring heads remains unchanged in case of limitation due to series-connection of the transistors.

The test signal which is amplified up to 5 V is applied to the A/D converter via the analog multiplexer. Overloads of the multiplexer and the converter are prevented by the DC clamp diodes (V231).

Amplification is divided into 11 ranges in order to cover the entire dynamic range from fractions of µV up to approx. 15 V. The test signal is passed via the analog multiplexer (V228, 229 / V243,244) directly to the inputs of the instrument amplifier (X211.1-2) in the 5 most sensitive measuring ranges. The polarity of the measuring signal is switched over periodically and the measured value is determined as the difference between two successive measurements. This simulation of a bridge-connected chopper amplifier eliminates the offset of the amplifier. In the other measuring ranges (6 to 11), the input signal is divided by approx. 34 dB (table 7-1, AC amplification ranges). The input dividers R291-R204 and R268-R202 essentially determine the input impedance of the AC amplifier. The input impedance can be reduced from approx. 10 MΩ to 0.5 MΩ via the FET transistors V234-V236. The measuring speed can thus be considerably increased, particularly with large measuring voltages, where the diode measuring heads act as peak-value meter. The charge dispenser is regularly actuated for a few ms in the measuring ranges with the input divider switched on (table 7-1). The inputs of the instrument amplifier are connected to ground potential periodically via V237 + V238 in order to obtain the offset.

Table 7-1 Amplification ranges of the AC amplifiers

Measuring range No.:	Amplification (AC amplifier)	Input divider	Total amplification
1	268	x1	268
2	122	x1	122
3	55.9	x1	55.9
4	25.9	x1	25.9
5	12.0	x1	12.0
6	268	x0.0216	5.79
7	122	x0.0216	2.64
8	55.9	x0.0216	1.21
9	25.9	x0.0216	0.559
10	12.0	x0.0216	0.259
11	5.64	x0.0216	0.122

The amplification changeover is effected by the analog multiplexers D201, D202 and the FET transistors V239 + V241.

The instrument amplifier consists of a high-amplification operational amplifier (N202) and a low-noise preamplifier stage with low offset current. The preamplifier stage is provided with a dual FET transistor V226A + B. The drain currents of the differential preamplifier stage remain constant due to N201A.

The maximumn control range of the AC amplifier is retained by means of periodical offset checks and a 7-bit automatic offset correction via the D/A converter D203 + N201B. The offset adjustment is carried out according to the successive approximation just upon switch-on of the instrument. The resolution is approx. 400 µV/digit. A correction is made, if the offset voltage exceeds a specified value.

7.1.2 DC Amplifier

(circuit diagram 857.8150.01, sheet 3)

This function group in conjunction with the sensor impedance (= 9 MΩ) acts as inverting amplifier. The amplification is divided into four ranges (cf. table 7-2), the changeover is effected via the analog multiplexer D323.

Table 7-2 Amplification ranges of the DC amplifier

Meas. range	1	2	3	4
Amplification	2.028	0.203	0.0203	0.00203

The function group DC amplifier is used for both test channels. Test channel A or test channel B are freely selectable as signal source via the multiplexers D321 + D322. The remaining two positions of the analog multiplexers allow for determination of the inherent offset voltage (the input of the amplifier is connected to ground via R315) and determination of the input offset current. In this case, the amplifier input is connected to ground potential via R308 + R309. Compensation of the input offset voltage of the operational amplifier is made via the D/A converter D324 with the associate resistor network such that the input offset current is maintained below 10 pA. The adjustment is performed according to the successive approximation procedure just upon switching on the instrument. Similar to the AC amplifier, the measured value is determined as the difference between the measured values of the test voltage applied and the offset value of the sensor-impedance equivalent /R308 + R309). During the measurement, the offset value is monitored and corrected correspondingly when the limit values are exceeded. Due to the low measuring currents, the arrangement of the individual switches of the input multiplexers D321 + D322 is selected such that the internal leakage currents are compensated as far as possible and maximum crosstalk attenuation is achieved.

7.1.3 MXADCTRL

This group shown on the block diagram consists of the input multiplexer of the A/D converter, the A/D converter, current sources for temperature sensors of the measuring heads, voltage supplies for measuring heads as well as the controller of the analog board with its monitoring and control logic.

7.1.3.1 Multiplexer

(circuit diagram 857.8150.01, sheet 6)

The analog multiplexer D601 + D610 allows for applying voltages of various test points of the instrument to the A/D converter. It is thus possible to check even internal test points for service purposes apart from determination of the current measured values in channel A and channel B, measurement of the frequency-proportional voltage at the DC(FREQ) input (conditioned by the amplifier N603B), determination of the temperature of the sensors via the inherent temperature sensors of the two test channels. The multiplexer D610 is mainly provided for selection of the service test points. The subsequent internal test points are evaluated one after the other:

- Control voltage of level control of the 50-MHz test generator -TPO-
- -6-V reference voltage for current sources of the temperature sensors.
- Current data of the voltage supply (V_{cc1}, V_{cc2}) to the measuring heads connected.
- Internal voltage supply ± 15 V
- Internal voltage supply ± 5 V

The desired test point is selected via the address and data bus <D7 to D4> and is stored in the latch D604 during the measurement (see division of address range, tables 7-3, 7-9).

7.1.3.2 A/D Converter

(circuit diagram 857.8150.01, sheets 6, 7)

The A/D converter circuit consists of the function group pulse-width modulator (N602B, D601A-C, U601) and the control and evaluation logic (D700). The DC input voltage of the A/D converter at X642.2 is converted into a square-wave signal (AMI), the duty cycle of which is proportional to the input voltage. The signal subject to pulse-width modulation is synchronized with the clock frequency and its pulse-width is determined in the counter of D700. The counting frequency is 12 MHz. The same clock frequency was used for the micrcoprocessor in order to avoid interferences.

The sychronized signal (SMOUT) is routed back via D601B + C and R630 and is used for compensation of the currents at the inverting input of the integrator N602B. The duration of a measuring cycle (= period of SMOUT) is also derived from the counting clock and is 1/6 ms. Thus, the shortest measuring time with optimum suppression of interferences with frequencies of 50 or 60 Hz (mains) was achieved. The resolution of approx. 11 bits/measuring cycle for the A/D measuring range can be increased to 19 bits for longer measuring times. Currents from three sources are summed up at the integrator input:

- Measuring current proportional to the input voltage via R631.
- 6-kHz rectangular driver current via R646 for generation of the delta signal (AC-coupled via C612).
- Compensation current, derived from the 5-V reference voltage (N601.6), proportional to the duty cycle of the synchronized, pulse-width-modulated square-wave signal (SMOUT).

The voltage characteristics at important knots of the A/D converter for an input voltage of 0 V are illustrated by fig. 7-1.

As long as the arithmetic means of the sum of currents at the integrator input unequals zero, the DC components of the delta signal at the integrator output is varied. Consequently, the time distance of the zero crossings which are registrated by the comparator U601 connected, varies and thus varies duty cycle of the signal supplied (AMI). Due to the superimposed 6-kHz driver current component, the zero crossing becomes considerably steeper and thus reduces undesired feedback effects.

The integration time can be selected in steps of 167 µs by programming the run control of the A/D converter (D700). Depending on the task (measuring speed, resolution) customization has been realized by the integrated microprocessor control via the address and the data bus. The end of a started conversion sequence is indicated to the microprocessor as hardware interrupt via the output "ZZOFL" (D700.39).

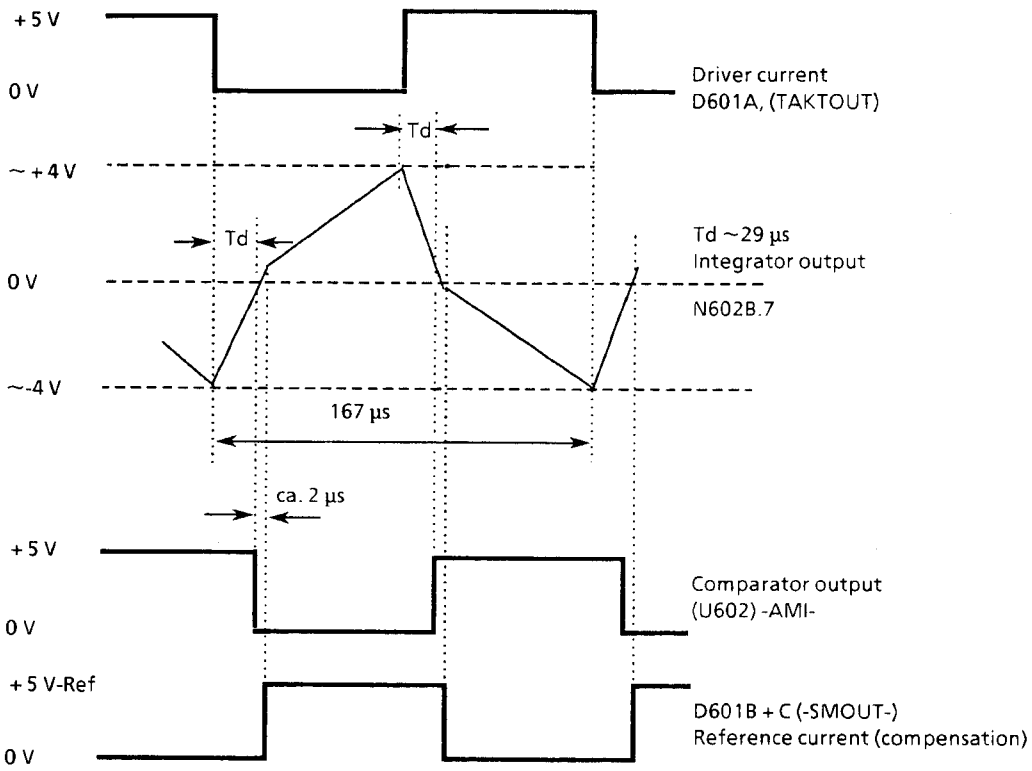


Fig. 7-1 Voltage shapes in the A/D converter

7.1.3.3 DC(FREQ) input

(circuit diagram 857.8908.01 / NRVD-B2; 857.8150.01, sheet 6 / analog board)

The frequency-proportional voltage of the external DC(FREQ) input is directly applied to the inverting amplifier N603B via the socket panel of the NRVD-B2 option via R645. The input impedance is determined to 1 MOhm by R645, the amplification is -1/3. The BNC socket DC(FREQ) on the rear panel is used as reference. The clamp diodes V623 prevent the analog multiplexer D602 from being overdriven.

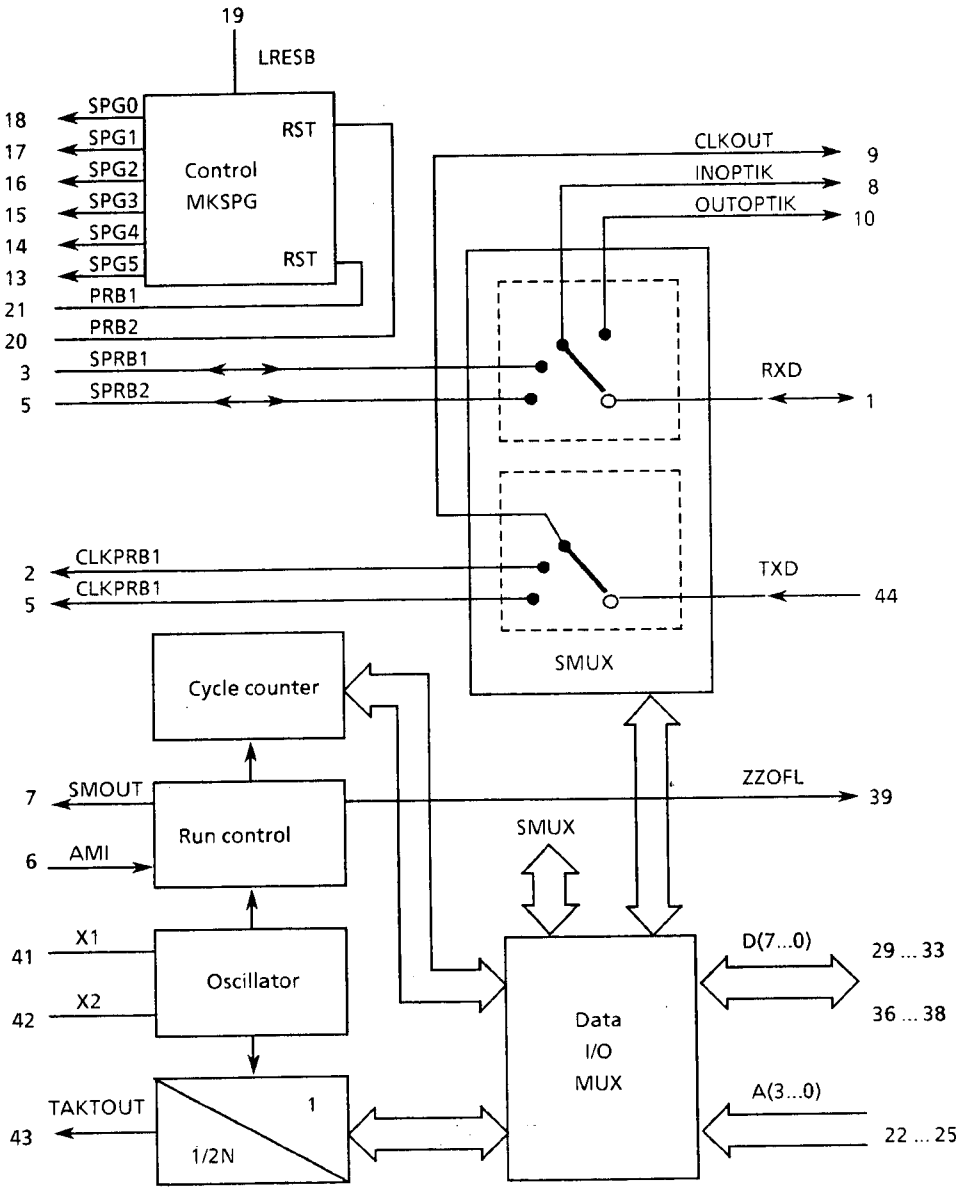


Fig. 7-2 Block diagram of D700 (Volcon)

7.1.3.4 Sensor Control

(circuit diagram 857.8308.01 / Filter board,
857.8150.01, sheets 1, 2, 4, 6, 7 / analog board)

7.1.3.4.1 Identification of Sensor

The connectors ID1 (channel A) or ID2 (channel B) and D700.21 or D700.20 are used to find out, whether a sensor is plugged in the test channel. If this is not the case (the identifier line assumes the logic "HIGH" state by means of internal pull-up resistors of D700, all voltages for the channel concerned are switched off by a hardware logic in D700 (outputs SPG0 to 2, or SPG3 to 5 /D700 are set to logic "L"). The identifier line assumes logic "LOW" level as soon as a sensor is connected. This state is realized by the processor by reading out the status register of D700 and the positive voltage supply of + 5 V is switched on. Subsequently, the sensor data are read by the processor via the serial data connection DATP1 + CLKP1 (DATP2 + CLKP2 in channel B). According to the information transmitted, the voltage supply can either be switched off, if the sensor connected is passive, or switched over to + 12 V/-12 V, if the sensor is an active one. If the type of sensor connected is not known, the voltage supply is switched off and a corresponding error message is displayed. The logic "HIGH" signal of the lines ID1 and ID2 is stored temporarily in D700 and can only be enabled again by the processor in order to ensure that short-term removals of sensor are realized correctly.

7.1.3.4.2 Voltage Supply

(circuit diagram 857.8150, sheets 2, 4, 7)

Each test channel of the NRVD contains two independent voltage sources, which are controlled by D700. Depending on the measuring head connected, the following voltage combinations can be set in each of the two channels:

1. V_{cc} = 0 V; V_{ee} = 0 V — Operation setting for a passive sensor or test channel without sensor
2. V_{cc} = 5 V; V_{ee} = 0 V — Basic setting upon connection of a sensor for readout of the sensor data.
3. V_{cc} = 12 V; V_{ee} = -12 V — Voltage supply for an active sensor in measurement mode.

The a.m. voltage combinations (except for 1) can only be set upon connection of an adequate sensor. The switch-on sequence is controlled by the controller of the analog board, the setting data transmitted via the data and address bus are stored in D700. The positive voltage supply for test channel A is programmed via the level converters V701 + V702 and the voltage regulator G701. The positive voltage for test channel B is set analogously via V707 + V706 and the voltage regulator G700. The voltages are switched on or off via D700.18 + V710 + V714 in channel A and via D700.15 + V709 + V712 in channel B.

The negative voltage sources are through-connected to the power sensors via the outputs D700.16 (SPG2), level converter V202 and the relay K200 (channel A) or via D700.13 (SPG5), level converter V402 and the relay K400 (channel B).

For safety reasons, all latches of the voltage setting are reset with switch-on via the RST connector D700.19 and thus all supply voltages of the sensors are switched off.

7.1.3.4.3 Temperature Sensors

The output voltage of the RF power and voltage sensors is temperature-dependent. It is absolutely necessary to determine the current temperature of the sensors and take it into account with evaluation of the measuring results in order to avoid errors which are caused by this temperature dependence. The temperature sensors fitted to the measuring heads supply a temperature-dependent voltage with a constant current flow. The measuring current is applied to the temperature sensor via the lines "TEMPA" (test channel A) or "TEMPB" (test channel B) and the voltage drop occurring is measured via the same line. The measuring current of 1 mA is switched on by V647 in channel A (V601 in channel B) depending on the measuring head connected. The voltage drop at the 1-mA sensor is approx. -3 V and the voltage at the 0.1-mA sensor is -0.3 V. The temperature-proportional voltages are measured via the multiplexer input D602.2 (test channel A) or D602.4 (test channel B). The current is only switched on for a few ms because of the heat due to the power loss at the sensor. The switching transistors are controlled by the data-bus latch D604 via the comparators V602 which are used as level converters. D604 simultaneously stores the measuring-path coding of the multiplexers D602 + D610.

7.1.3.4.4 Programming of the Sensor Memories

Calibration data of the measuring heads, which are provided with a reprogrammable data memory can be stored in a non-volatile memory without additional programming devices, only by means of a controller and NRVD.

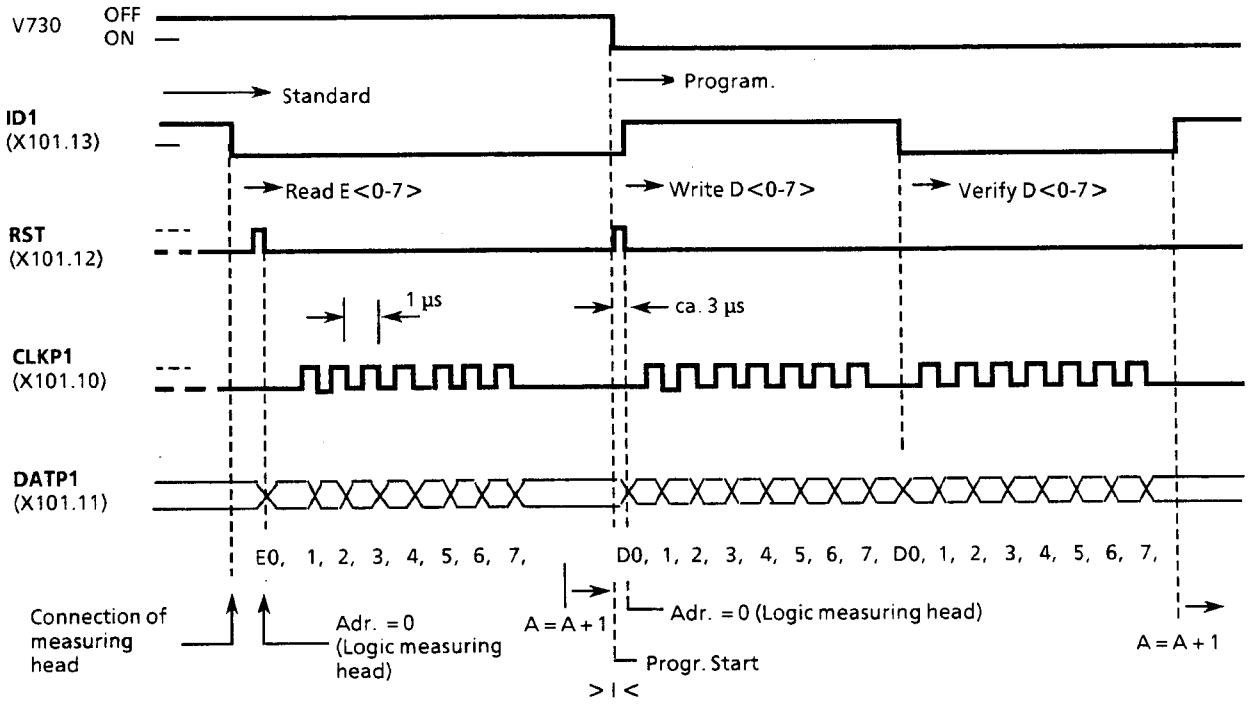


Fig. 7-3 Readout and programming of the sensor data

In normal operation, the sensor data are read out subsequent to connecting the sensor (line ID1 "LOW"/channel A, X101.13). The voltage supply of the measuring head (V_{cc1} = +5 V) is switched on for this purpose.

Reading of the first 8-bit data word is illustrated in the first section of fig. 7-3. The reset signal sets the address counter of the sensor logic to 0 and simultaneously provides the first bit of the data word at the output. The memory address is automatically incremented by the sensor logic upon output of the first data word and the following data word is transmitted with the next clock package.

The voltage supply of the sensor is switched over to + 12 V/-0 V in programming mode. The write or read signal (W; log. "H"; $\overline{R}$; log. "L") is transmitted via the line ID1, the $\overline{R/W}$ signal is applied to ID1 by the data bus via D710 and V732. During programming, the input D700.21 is supplied with the logic "L" level via V730, in order to prevent the voltage supply from being disconnected during the write cycle (ID1 = "H") which might be interpreted "Sensor not connected" (cf. 7.1.3.4.1)

Programming of a data word is shown in the second section of fig. 7-3. Subsequent to switch-over to the programming mode (V730 → conducting), a logic "H" level is provided at ID1 via the data bus and D710 + V732, thus initiating the write cycle. The reset signal resets the sensor logic (address → 0) to the original state. Subsequently, the logic level on line ID 1 becomes "LOW" (V732 → switched off) and the data word stored is verified. The memory address of the sensor logic is incremented with the next write pulse (ID1 → "H") and the next data word is stored and verified analogously. Transmission of the probe data from (to) the controller of the analog board is synchronous with the clock signal. The probe data to be stored are transferred from the controller via the IEEE-bus interface of the basic unit, the controller module A1, the serial interface to the analog module A2 and the controller of the analog board to the sensor interface of the respective test channel.

The functions of the transistors V732, V730 as well as of the input D700.21 are realized in channel B by V728, V729 and D700.20.

7.1.3.5 Onboard Controller of the Analog Board

(circuit diagram 857.8150.01 / analog board, sheet 7)

The controller is provided for control of the hardware of the analog board, for communication with the measuring heads connected and processing of the measuring data for the main controller of the NRVD. The CPU containing the 80C51FA (D751) is the nucleus of the controller. The latch D709 extracts the address information of the lower address-bus byte A<7...0> from the data stream of the multiplexed port P0. The main memory of the processor is provided with 256 kbits - RAM (D707), the program memory D708 comprises 512 kbits. The RAM D707 is selected via the address line A15, the program memory is addressed via $\overline{PSEN}$ of the CPU and the 16-bit address bus.

Table 7-3 Analog board of NRVD, address ranges and accessibility

Address	Access	Data	Meaning
000H-7FFFH	R/W	D<7:0>	Controller - RAM
000H-FFFFH	R	D<7:0>	Controller EPROM, firmware
Axx0H-AxxFH	W	D<7:0>	Hardwareoperation of the analog unit (cf. Table 7-9)
Cxx0H-CxxHF	R/W	D<7:0>	- Volcon, D700 - (ADC, serial multiplexer, monitoring of the sensor, supply to the sensor)

The hardware latches are addressed via the demultiplexer D705. D700 - Volcon - is addressed in the upper part of the address range (from 0C000H) via D706B and A<3...0> as RAM. Either write (setting of functions) or read access (measuring results, information on operation) to D700 is possible. The interrupt input INT1 of the CPU is controlled by the ZZOFL output of D700. The HIGH-level-to-LOW-level transition indicates to the processor, that the number of programmed integration cycles of the A/D converter has been reached and the measurement has been performed. The clock signal for the processor (12 MHz) has been derived from the clock signal for the A/D converter, in order to avoid interferences between different sources.

The reset signal for the processor is obtained from the module A1 (controller board) via the interface X102.4-X102.5 and the opto-coupler U703. The reset delay compared to the main controller (A1) causes the time constant R766 + C720 with D706-C.

The serial interface of the CPU (port 3) is used at a clock rate of 1 MHz for communication with the main controller of the NRVD (board A1) and the plug-in measuring heads of the two test channels. Selection of the sensors is program-controlled via the serial multiplexers of D700 (see block diagram 7-2). Communication with the main controller is realized via two unidirectional data lines isolated by opto-couplers and a separate clock line. A bidirectional data line and the associate clock line are provided for connection with the sensors (DATP1 + CLKP1/test channel A, or DATP2 + CLKP2 for test channel B). It is thus possible then to program the memories of the measuring heads in the NRVD without using additional programming devices (cf. 7.1.3.4.4).

7.1.4 Test Generator

(circuit diagram 857.8150, sheet 5)

The oscillator equipped with V524 is the nucleus of the test generator. The frequency-determining π element (C566-L503-C572 + 507,C571) is tuned to 50 MHz. The signal amplitude at the oscillator output (node L503-L504) is regulated to a constant value by means of a PLL. Consequently, the internal impedance at this point is 0 Ω. The 50-MHz sinewave signal is passed to the N-socket "TESTOUT" via the capacitive voltage divider C507 + C572-C571 and the output matching network L501 - R545 + R552 + R535. The power available at this socket (front panel) is calibrated to 1 mW and provided for the test of the RF measuring heads.

The actual value of the amplitude PLL is obtained by rectifying (V578) the oscillator output voltage at the node L504-L504. The amplifier/integrator N511B compares this value to the rated value. The control voltage from the output of the N511B is passed via the required time constants to the capacity diode V525, which is used as control-voltage-dependent voltage divider in the feedback path of the oscillator. The temperature dependence of the measuring diode V578 is compensated by V579 in the reference path of the PLL.

The rated value for the control loop is derived from the +6 V reference voltage via an A/D converter. The converter consists of D541 and the associate resistance network and allows for exact calibration of the output power of the test generator at the N-socket TESTOUT. The calibration value is stored in the non-volatile memory of the controller module A1.

7.2 Test Instruments and Utilities

Table 7-4 Required test instruments

Item	Type of instrument	Required specifications	Suitable R&S instrument	Order No.	Application
1	Digital multimeter	DC: 0 to 300 V +0.05 %, 0 to 2 A AC: 0 to 300 V	UDS 5	349.1510.02	7.4.1
2	Oscilloscope	DC to 100 MHz	BOS, BOL		7.3.2.2.2
3	Cal. adapter			350.7818.02	7.4.3
4	Resistor	3.01 kΩ ±0.1%			7.4.3
5	Frequency counter	10 Hz to >50 MHz, >0.1 % V_i<0.2 V			7.4.2 7.4.4
6	Directional coupler	Directivity >50 dB Z_0 = 50 Ω	URV5-Z9, selected	265.5315.02	7.4.4.2
7	Cable	Z_0 = 50 Ω, 2x N connector, el. length = 75 cm/50 MHz			7.4.4
8	Short-circuit	N connector			7.4.4
9	RF probe	Bandwith >100 MHz	URV-Z7	395.2615.02	7.4.4.2
10	Controller	IEEE448 interface	PSA family		

The following circuit diagrams are required for successful troubleshooting: basic unit NRVD 857.8008.01, 350.5867.04 - controller, 857.8108.01 - display, 857.8150.01 - analog board 857.8308.01 - filter board and I/O option NRVD-B2 (if fitted), 351.8908.01.

7.3 Troubleshooting

Rough classification of the error cause has been made considerably easier by means of the internal diagnostic utilities. In case of total failure it is generally advisable to first check the setting of the power voltage and the power fuses on the rear panel of the instrument.

7.3.1 General Remarks on Troubleshooting

Many function groups are centrally provided, e.g., with reference voltages +6 V (-6 V) or additionally stabilized +5 V/-5 V. If the central supply fails, various error messages are output, which are due to a common cause. If these error messages occur frequently, it is advisable to search for a common cause.

The sequence and extent of the internal selftest operations, which are performed just upon switch-on allow for error localization in a relatively small range of the circuitry. The error messages are coded hexadecimally (cf. table 7-5) and are summed up, if they occur several times.

The localization of faults on the analog board of the NRVD has further been facilitated by readout of the error bits (see 7.3.2.2 Service functions).

7.3.2 Diagnosis Utilities

7.3.2.1 Error Messages

The current state of the instrument is checked just upon switch-on and, with occurrence of an error, a hexadecimally coded error message (see table 7-5) is displayed. If more errors occur, the codings of the individual errors are summed up.

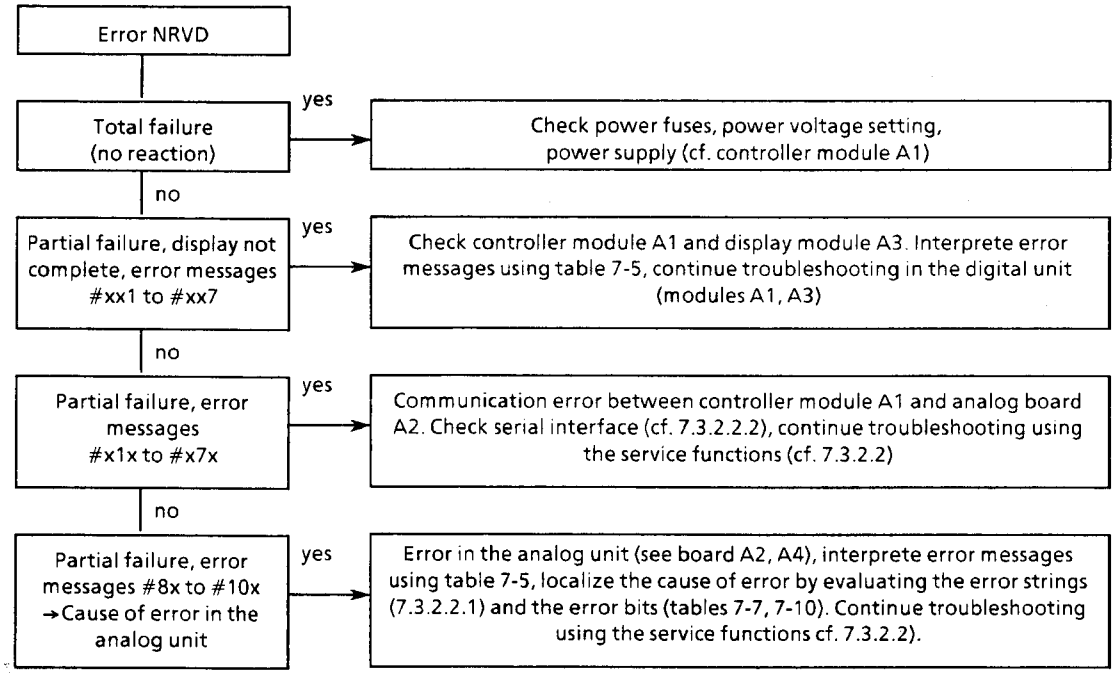
Example: A message "DEVICE-ERROR * 182" contains information about missing RAM data (* 2), hardware errors on the analog board (* 100) and errors with transmission (parity, * 80).

Table 7-5 Meaning of the NRVD error messages and remedies

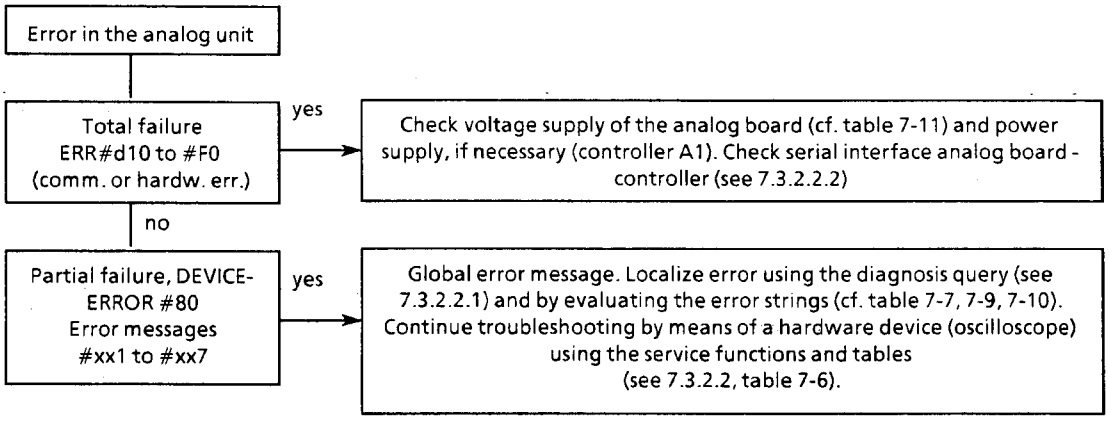
Error message	Cause	Possible error and remedy
DEVICE-ERROR * 1	Errors of the EPROMs summed up	Replace EPROMs D5, D6 (computer board)
DEVICE-ERROR * 2	RAM data missing	RAM error (replace D7, D8, computer board) Update RAM data, cf. 7.3.2.1
DEVICE-ERROR * 4	Lith. battery discharged (displ.: "BATT.LOW")	Replace battery, perform recalibration
DEVICE-ERROR * 8	Calibration data missing	Perform recalibration (cf. Service Manual 6.3.4)
DEVICE-ERROR * 10 DEVICE-ERROR 20	Time limit for transmission to analog board exceeded Time limit for receipt from analog board exceeded	Check serial interface to the analog board. Trigger service routine D700 (cf. 7.3.2.2.2)
DEVICE-ERROR * 40	Error in data transfer from analog board to computer board	Trigger service routine (analog board). Check test signals according to Fig. 7-7 (see 7.3.2.2.2).
DEVICE-ERROR * 80	Parity error in data transfer from computer to analog board	
DEVICE-ERROR * 100	Hardware error in analog board	Localize using the error string, see 7.3.2.2.1, Utilities for Hardware Diagnosis
DEVICE-ERROR * 400	SENSOR-FAILURE	Sensor faulty (external). Check power supply and serial interface to sensor (7.3.2.2.3)

Subsequent to display of the error message, it is possible in most cases to assign the causes of error either to the digital unit of the instrument (controller module A1, display module A3; - error messages in the range from # 001 to # 00F), or to the analog unit (module A2-analog board, A4-filter board; - error messages # 80, # 100). If no error message is output or if the instrument shows no reaction, the following troubleshooting flowcharts in conjunction with internal test routines can be used for troubleshooting.

Troubleshooting flowchart 1 for the complete instrument



Troubleshooting flowchart 2, analog unit



DEVICE ERR #002 - Loss of the RAM data together with ERR #004 (battery discharged) is indicated as ERR #006 or with change of software. The missing RAM data (preassignment of the instrument settings) can be assigned again from the firmware range (preset setup) by means of the following key sequence:

"SPEC" → "mre →mre →more →more →INIT → *EXEC"

7.3.2.2 Service Functions for Testing the Analog Hardware

The diagnostic commands (table 7-6) set the instrument into the service mode. The test run of the processor on the analog board is stopped and then measurement is performed acc. to the setting made via the service function. The instrument setting prior to switch-over to the service mode is stored and thus, the measurement can be continued without interferences after resetting the test mode.

Table 7-6 Diagnostic commands NRVD

Diagnostic command	Function within the analog board A2
DIAG:AHAR (?) Nr	Triggering of the internal calibration routines
DIAG:ATEST Nr	Periodical test routines (interface test, Switch-identify etc.)
DIAG:ACON? Nr	Triggering of A/D conversions
DIAG:ASET Nr	Setting of group functions (e. g. amplification multiplexer, offset, etc.)

If a sensor is to be operated in service mode, it must be connected and initialized in the test mode, already. The sensor is thus identified and all functions depending on the type of sensor connected can then be carried out.

7.3.2.2.1 Hardware Diagnosis Utilities

The display of a hardware-error message can be further specified using the diagnostic command "DIAG:AHAR?". The 64-bit reply string (cf. fig. 7-4) contains coded information on the current status at each test point on the analog board assigned to a bit. If the measured value at the test point concerned exceeds the tolerance, the corresponding bit is set. The meaning of the individual bits in the hardware-error string as well as measured-value ranges of the test points assigned can be looked up in the tables 7-7 and 7-10.

```
1,"00000001  10000100 00000000 00000000 00000000 00000100 00000000 00000000
```

or

```
0,"No error"
```

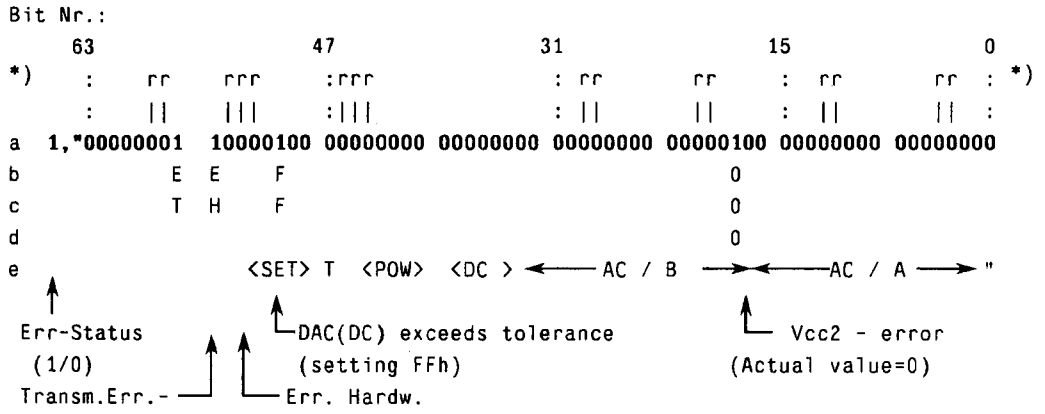
if no error was found.

Fig. 7-4 Diagnosis reply string, additional information is suppressed (DIAG:TEST1 OFF).

Further information on the error string can be requested using the preceding command

"DIAG:TEST ON"

(cf. fig. 7-5).
The measured values at the faulty test points are output together with the reply string.



*) r - reserved bits (see Tab. 7-7)

Fig. 7-5 Diagnosis reply string: extended information requested:
(DIAGN: TEST1 ON = > 5 lines with additional information in lines b to e).

The error status bit (global error bit) is separated by a comma. The additional information below the error bits set, evaluated column by column, indicate the current setting or measured value. The bit No. 18 and the bit No. 50 are set in fig. 7-5, by way of example. According to the tables 7-7 and 7-10 the voltage supply of the sensor V_{cc1} + 5 V in channel A is 0 V and thus below the tolerance (bit 17), the setting of the D/A converter for offset correction in the DC amplifier is "0FFH" and, is thus not permitted. Correct setting must be in the range <002h to 0FEh>. Consequently, the global hardware-error bit (55) is set. The bit No. 56 (transmission error) was set, too.

The measured value required is displayed together with its associate limits, if the parameter (number of error bit) is added to the diagnostic command "DIAG:AHAR? No" (cf. fig. 7-6, see also table 7-10).

```
1.00000E-01;1.88204E+00;5.00000E+00
-----------;-----------;-----------
   ( min.  ;  Actual value  ;   max.)
```

Fig. 7-6 Display of current measured value at the test point corresponding to the error bit (reply string to "DIAG:AHAR? 13").

7.3.2.2.2 Testing the Communication Interface A2/Analog Board ↔A1/Main Controller

The test routine is triggered by a short-circuit at X710.1-2 (shorting jumper). The routine is periodically processed until the short-circuit at X710 is removed again.

The processor periodically reads the information (8-bit word) at the output of the receive opto-coupler U704.6 and, in the next step, sends the received data word out via X102.13 (D700.10 - OUTOPTIK). The clock is passed from the output TXD of the micro-controller D751 via the serial multiplexer of D700 (Volcon, pin 9-CLKOUT) to the interface output X102.15 - CLOCK. The bidirectional data at the node D751.11-D700.1 (RXD) are switched by the serial data multiplexer of D700 (cf. block diagram 7-2) according to the direction of transmission.

Table 7-7 Error status, hardware-error bits

Error bit	Meaning	Test phase
0	V_{CC1} (0 V)	(Initialization), measurement
1	V_{CC1} (+5 V)	(Initialization), measurement
2	V_{CC1} (+12 V)	(Initialization), measurement
3, 4	reserved	
5 to 10	Offset voltage AC-A, Measuring voltage 6 to 11	(Initialization), measurement
11, 12	reserved	
13	Hub 0, 1-mA-Sensor	(Initialization), measurement
14	Offset 1-mA-Sensor	(Initialization), measurement
15	Temp. 0,1-mA-Sensor	(Initialization), measurement
16	Temp. 1-mA-Senosr	(Initialization), measurement
17	V_{CC2} (0 V)	(Initialization), measurement
18	V_{CC2} (+5 V)	(Initialization), measurement
19	V_{CC2} (+12 V)	(Initialization), measurement
20, 21	reserved	
22 to 27	Offset voltage AC-B, Measuring voltage 6 to 11	(Initialization), measurement
28, 29	reserved	
30	Hub 0,1-mA-Sensor	(Initialization), measurement
31	Offset 1-mA-Sensor	(Initialization), measurement
32	Temp. 0,1-mA-Senor	(Initialization), measurement
33	Temp. 1-mA-Sensor	(Initialization), measurement
34 to 37	Offset voltage DC Measuring voltage 1 to 4	(Initialization), measurement
38	Offsetstrom DC	(Initialization), measurement
39	Tuning voltage TPO	(Initialization)
40	-6 V	(Initialization)
41	-15 V	(Initialization)
42	-5 V	(Initialization)
43	Offset A/D converter	(Initialization), measurement
44	-6 V	(Initialization)
44 to 46	reserved	
47	Timeout ADC	Measurement
48	DAC - set AC-A	(Initialization), measurement
49	DAC - set AC-B	(Initialization), measurement
50	DAC - set DC	(Initialization), measurement
51	DAC - set 50 MHz	(Initialization), measurement
52 to 54	reserved	
55	Hardw. error	---
56	Transmission error	---
57 to 58	reserved	

X102.15, X102.8, X102.13 are interfaces with negligible voltage deviation, which are supplied with current. It is therefore recommended to check the voltage characteristics (oscilloscope) first at the driver outputs (D700.9, .10) and at the input D700.8.

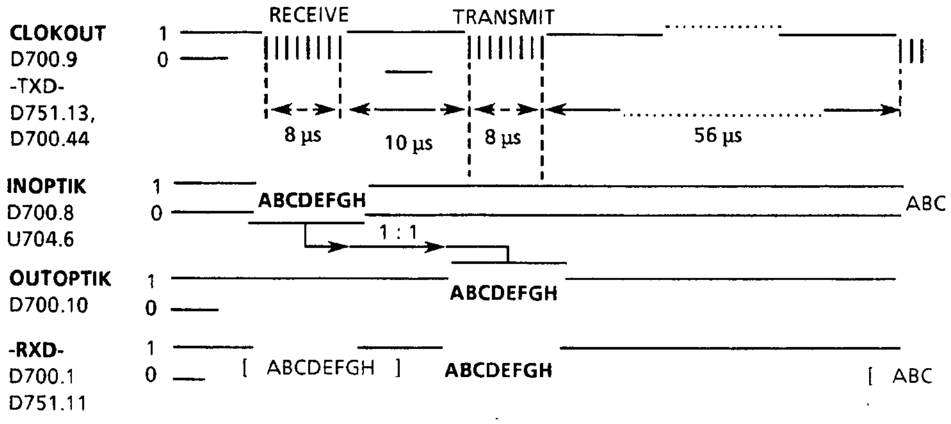


Fig. 7-7 Time frame of the interface test-routine

The switch-on frequency of the LED changes in order to mark the test routine optically. The LED H702 lights up at a clock of approx. 4 Hz during the test run. The LED H701 also assumes another function and signals the state of the interrupt input INT0 (= U704.7; INT0 = 0 → H701 lights up) during the test run.

7.3.2.2.3 Cyclic Test Functions

Two types of functions are available, which can be selected by input of the parameter (No.):

- Probe read: `"DIAG:ATEST No."` **(No = 0→test channel A, 1→test channel B)**

This function is used to check, if a sensor is connected. If so, the +5 V voltage supply is switched on and, subsequent to reset of the address counter, 16 bytes are read from the data memory of the sensor. Following read-out, the voltage supply is switched off again and the switch-off state is checked. If an error is found, the corresponding error bits are set.

- Switch identify: `"DIAG:ATEST 2"`

Proceeding from the current hardware setting, all bits of the latches 0 to 8 are periodically inverted for 0.1 ms. The cycle time for all latches is approx. 10 ms (see fig. 7-8). A trigger pulse for representation of the processes on an oscillograph can be obtained at X710.1. The state of the latches upon termination of this test routine is equivalent to that before calling the test routine.

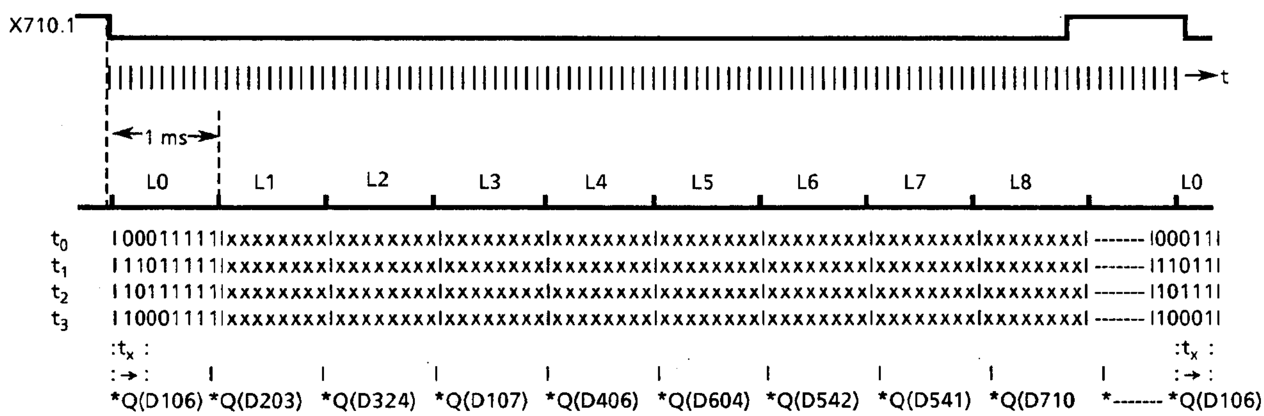


Fig. 7-8 Time frame "Switch identify"

The timing of the service function "Switch identify" (see fig. 7-8) shows that the distance tx between the falling edge of the trigger signal and the bit which changes the state (latch output) is only assigned one bit. This bit (output) can thus be identified uniquely. The test of the verify-function for reprogrammable data memories in channel A or B (transistors V730-732/ V728-729 with D710) can be used as application example. With correct function, the voltage shape at X101.13 (.29) must correspond to that illustrated in fig. 709, when a sensor is connected at X101.13 (.29) or is substituted by a pull-down resistor of 10 kΩ. When the a.m. functions are disabled, both transistors (V730 + V732) are disconnected, the level at the ID1 line is determined by the pull-down (X101.13) and the pull-up resistor (Volcon). The "Switch identify" routine sequentially switches on the two transistors, the voltage level must be "LOW" for approx. 1 ms with switch-on of V730, after 1 ms it will be approx. + 5 V for 1 ms (fig. 7-9).

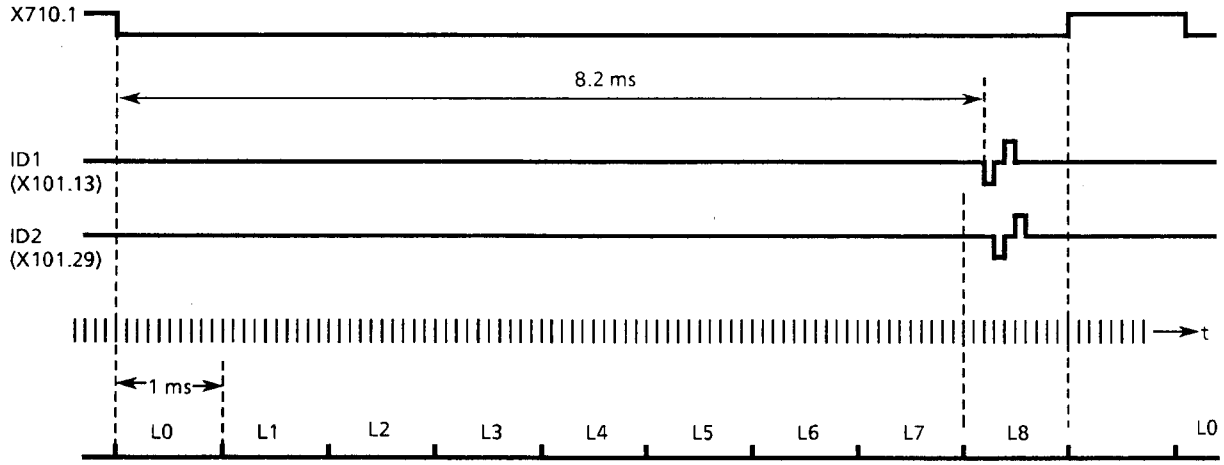


Fig. 7-9 Verify test, typ. voltage shape at X101.13 (X101.29)

7.3.2.2.4 Setting of Group Functions

The settings of hardware configurations listed below (tables 7-9 a to e) are carried out using the command "DIAG:ASET No". The parameter (No) depends on the desired setting and can be looked up in table 7-9. Tests are not performed in conjunction with these settings (comp. "DIAG:AHAR No). During the setting procedure, the port connection P1.1 (X710.1) assumes logic "L" level (0 V).

Each setting is acknowledged by the instrument by display of an error status. The global error bit is set to zero independent of the state of bits <54 to 0> (cf. figs. 7-4, 7-5).

In contrast to "Probe-read" or a test routine ("DIAG:AHAR No.), the hardware configuration set is not influenced by triggering of the cyclic functions "Switch identify" or A/D conversion.

7.3.2.2.5 Triggering of A/D Conversions

The voltage applied to the input of the A/D converter (X642; X641.9) can be measured using the service function "DIAG:ACON? No). The integration time is set by entry of the parameter (No.) (cf. table 7-8). The output of the measured value corresponds to that of a triggered measurement. During the measurement procedure, the port connection P1.1 of the processor D751 (X710.1) assumes logic "L" level (0 V). If the time limit is exceeded by the A/D converter, the error bit 47 as well as the global error bit 55 (hardware-error) are set.

Table 7-8 Coding of the integration times of the D/A converter

Integration time [ms]	0.5	1	2	5	10	16 2/3	20
Parameter No.:	0	1	2	3	4	5	6

The measured values output are completely corrected. The periodically measured offset voltage of the A/D converter referred to the reference ground (D602.1, error bit 43) is used for offset correction. The sensitivity of the A/D converter is corrected corresponding to the calibration factor of the temperature-sensor input (0.1 mA).

Table 7-9a Table 7-9a Schedule of parameters for service setting of the hardware configuration [DIAG:ASET NO)

:ASET No.	Meaning	Function	Data-Bit D76543210	Address LE Latch	Remark
0	AC amplifier A,	reserviert	xxxx0000	A00H LE 0 D106	1. 2)
1	Measuring range 1	x268	xxxx0001		1. 2)
2	Measuring range 2	x122	xxxx0010		1. 2)
3	Measuring range 3	x55.9	xxxx0011		1. 2)
4	Measuring range 4	x25.9	xxxx0100		1. 2)
5	Measuring range 5	x12.0	xxxx0101		1. 2)
6	Measuring range 6	x5.79	xxx11001		1. 2)
7	Measuring range 7	x2.64	xxx11010		1. 2)
8	Measuring range 8	x1.21	xxx11011		1. 2)
9	Measuring range 9	x0.559	xxx11100		1. 2)
10	Measuring range 10	x0.259	xxx11101		1. 2)
11	Measuring range 11	x0.122	xxx11110		1. 2)
12	Test mode AC - A	GND/INV	xxx01xxx		2)
13		NORMAL	xxx1xxxx		2)
14	Discharge circuit	OFF	xx0xxxxx		
15		ON	xx1xxxxx		
16	Meas. current (temp.) A	OFF	xxxxxx00	A005H LE5 D604	
17		0.1 mA	xxxxxx01		
18		1.0 mA	xxxxxx10		
19	AC amplifier B,	reserviert	xxxx0000	A003H LE 3 D107	1. 2)
20	Measuring range 1	X268	xxxx0001		1. 2)
21	Measuring range 2	x122	xxxx0010		1. 2)
22	Measuring range 3	x55.9	xxxx0011		1. 2)
23	Measuring range 4	x25.9	xxxx0100		1. 2)
24	Measuring range 5	x12.0	xxxx0101		1. 2)
25	Measuring range 6	x5.79	xxx11001		1. 2)
26	Measuring range 7	x2.64	xxx11010		1. 2)
27	Measuring range 8	x1.21	xxx11011		1. 2)
28	Measuring range 9	x0.559	xxx11100		1. 2)
29	Measuring range 10	x0.259	xxx11101		1. 2)
30	Measuring range 11	x0.122	xxx11110		1. 2)
31	Test mode AC - B	GND/INV	xxx01xxx		2)
32		NORMAL	xxx1xxxx		2)
33	Discharge circuit	OFF	xx0xxxxx		
34		ON	xx1xxxxx		
35	Meas. current (temp.) B	OFF	xxxx00xx	A005H LE5 D604	
36		0.1 mA	xxxx01xx		
37		1.0 mA	xxxx10xx		

1) The indication of the amplification means total amplification from the sensor interface to the output of the AC amplifier (X641.1, .3). The predivider has already been taken into account for the measuring ranges 6 to 11.

2) Test mode GND/INV: The input signal is inverted in the ranges 1 to 5 or directly applied to the amplifier (D106,7 = >xxx00xxx / xxx10xxx; chopper operation), the inputs are connected to the divider base in the remaining measuring ranges (bit configuration D106, D107 acc. to table 7-9a)
Test mode NORMAL: A signal applied to the sensor interface is amplified according to 1) and is available at the amplifier output (X641) in inverted form.

Table 7-9b Schedule of parameters for setting of the hardware configuration [DIAG:ASET No.]

:ASET No.	Meaning	Function	Data Bit D76543210	Address LE Latch	Remark
	DC amplifier				
38	Measuring range 1	x 2.00	00xxxxxx	A003H LE 3 D107	3)
39	Measuring range 2	x0.20	01xxxxxx		3)
40	Measuring range 3	x0.020	10xxxxxx		3)
41	Measuring range 4	x0.0020	11xxxxxx		3)
42	DC test mode	Channel -A-	00xxxxxx	A000H LE 0 D106	
43		Channel -B-	01xxxxxx		
44		GND	10xxxxxx		4)
45		OFFSET ADJ.	11xxxxxx		4)
46	ADC Multiplexer	AC - A	0000xxxx	A005H LE 5 D604	
47	(D 602)	DC	0001xxxx		
48	(D 602)	AC -B	0010xxxx		
49	(D 602)	(OSC)	0011xxxx		
50	(D 602)	GND	0100xxxx		
51	(D 602)	TEMP - A	0101xxxx		
52	(D 602)	TEMP - B	0110xxxx		
53	(D 602)	DC (FREQ)	0111xxxx		
54	(D 602)	TPO	1000xxxx		
55	(D 602)	-6 V	1001xxxx		
56	(D 602)	V_{CC1}	1010xxxx		
57	(D 602)	V_{CC2}	1011xxxx		
58	(D 602)	$\Sigma(\pm 15\ V)$	1100xxxx		
59	(D 602)	$\Sigma(\pm 5\ V)$	1101xxxx		
60	(D 602)	reserved	-----		
61	(D 602)	reserved	-----		
62	Test generator 50 MHz	OFF	0xxxxxxx	A006 H LE 6 D541	
63		ON	1xxxxxxx		
64	Data memory -A-	Reset: 0 V	xxxxxxx0	A008H LE 8 D710	
65		5 V	xxxxxxx1		
66	ID1 enable (A)	V730 OFF	xxx1x0xx		
67	ID1 disable	V730 ON	xxxxx1xx		
68	Read -A- (V730-ON)	V732 OFF	xxx1x1xx		5)
69	Write -A- (V730-ON)	V732 ON	xxx0x1xx		
70	Data memory -B-	Reset: 0 V	xxxxxx0x		
71		5 V	xxxxxx1x		
72	ID2 enable (B)	V729 OFF	xx1x0xxx		
73	ID2 disable	V729 ON	xxxx1xxx		
74	Read -B- (V729-ON)	V728 OFF	xx1x1xxx		5)
75	Write -B- (V729-ON)	V728 ON	xx0x1xxx		
76 to 79	reserved	reserved	---		

3) Amplification with a source impedance of 9 MΩ (DC probe). The amplification is 9 times as high, if the calibration adapter (Ri = 1 MΩ) is used.

4) The inverting input of N305 via R308 + R309 (= 9 MΩ) is grounded, if the setting "GND" is selected. Setting "OFFS ADJ." via R315 = 4.75 kΩ.

5) Reading of the sensor data is also possible, even if the bit No.2 (channel A) or No. 3 (channel B) is not set.

Table 7-9c S chedule of parameters for setting of the hardware configuration [DIAG:ASET No]

:ASET No.:	Meaning	Function	Data Bit D76543210	Address LE Latch	Remark
80 81 82	Offset DAC -A-	000h 080h 0FFh	00000000 10000000 11111111	A001H LE 1 D203	
83 84 85	Offset DAC -B-	000h 080h 0FFh	00000000 10000000 11111111	A004H LE 4 D403	
86 87 88	Offset DAC -DC-	000h 080h 0FFh	00000000 10000000 11111111	A002H LE 2 D324	
89 90 91	Test generator 50 MHz - P_{out} - (D542)	000h 080h 0FFh	00000000 10000000 11111111	A007H LE 7 D542	

Table 7-9d S chedule of parameters for setting of the hardware configuration [DIAG:ASET No]

:ASET No.:	Meaning	Function	D700, [6] SPG 543210	Address Latch	Remark
92	Voltage supply	0 V/0 V	xxxxx0	C001H D700	7)
93	Test channel A; V_{cc}/V_{ee}	+ 5 V/0 V	xxx001		7)
94	V_{CC1} (X101.14)	+ 12 V/0 V	xxx011		8)
95	V_{ee} = ARGND (X101.3)	+ 12 V/-12 V	xxx111		9)
96	Voltage supply	0 V/0 V	xx0xxx		7)
97	Test channel B; V_{CC}/V_{ee}	+ 5 V/0 V	001xxx		7)
98	V_{CC2} (X101.30)	+ 12 V/0 V	011xxx		8)
99	V_{ee} = BRGND (X101.19)	+ 12 V/-12 V	111xxx		9)

Table 7-9 e Schedule of parameters for setting of the hardware configuration [DIAG:ASET No]

:ASET No.:	Meaning	Function	D700, serielle MEX	Address Latch	Remark
100 101 102 103	100 to 103 Configuration of the Cal adapter for: (Chan. A)	Temp. Sensor AC - Adjust 1 MΩ AC + ; DC	Data transfer via serial interface →Cal. adapter	C005H D700	10)
104 105 106 107 108 to 255	104 to 107 Configuration of the Cal adapter for: (Chan. B) reserved	Temp. Sensor AC - Adjust 1 MΩ AC + ; DC reserved	Data transfer via serial interface →Cal. adapter	C005H D700 C005H D700	10)

6) SPG (voltage) <5...0> = >D700.13 to D700.18

7) Only with any identified sensor.

8) Only with reprogrammable sensor identified.

9) Only with identified active sensor.

10) Only with identified calibration adapter. The setting of the calibration adapter modifies the logic states of the control lines to the data memory and the sensor supply.

Table 7-10 Tolerance ranges of internal test routines with associate coding [DIAG:AHAR(?) No]

Error bit No.:	Meaning	Test channel	Specified range (Test)	Settings acc. to table 7-8	Funct. No.:	Remark
0	V_{CC1} (0 V)	A	-0.010 to 0.200	92, 56	0	1), 4)
1	V_{CC1} (+5 V)	A	+0.245 to +0.282	93, 56	1	1), 4)
2	V_{CC1} (+12 V)	A	+0.583 to +0.670	94, 56	2	2), 4)
3, 4	reserved					6)
5	Offset AC, Ran. 6	A	-0.480 to +0.480	6, 12, 14, 46	5	
6	Offset AC, Ran. 7	A	-0.230 to +0.230	7, 12, 14, 46	6	
7	Offset AC, Ran. 8	A	-0.075 to +0.075	8, 12, 14, 46	7	
8	Offset AC, Ran. 9	A	-0.064 to +0.064	9, 12, 14, 46	8	
9	Offset AC, Ran. 10	A	-0.040 to +0.040	10, 12, 14, 46	9	
10	Offset AC, Ran. 11	A	-0.030 to +0.030	11, 12, 14, 46	10	
11, 12	reserved					6)
13	Deviation 100-µA Senor	A	+0.100 to +5.000	16, 51/17, 51	13, 15	1), 5)
14	Offset 1-mA Sensor	A	-0.100 to +0.100	16, 51/18, 51	14, 15	1), 5)
15	Test voltage 100-A Senor	A	-0.410 to -0.190	16, 51/17, 51	13, 15	1), 5)
16	Test voltage 1 mA Senor	A	-3.540 to -2.420	16, 51/18, 51	14, 16	1), 5)
17	V_{CC2} (0 V)	B	-0.010 to 0.200	96, 57	17	1), 4)
18	V_{CC2} (+5 V)	B	+0.245 to +0.282	97, 57	18	1), 4)
19	V_{CC2} (+12 V)	B	+0.583 to +0.670	99, 57	19	2), 4)
20, 21	reserved					6)
22	Offset AC, Ran. 6	B	-0.480 to +0.480	25, 31, 33, 48	22	
23	Offset AC, Ran. 7	B	-0.230 to +0.230	26, 31, 33, 48	23	
24	Offset AC, Ran. 8	B	-0.075 to +0.075	27, 31, 33, 48	24	
25	Offset AC, Ran. 9	B	-0.064 to +0.064	28, 31, 33, 48	25	
26	Offset AC, Ran. 10	B	-0.040 to +0.040	29, 31, 33, 48	26	
27	Offset AC, Ran. 11	B	-0.030 to +0.030	30, 31, 33, 48	27	
28, 29	reserved					6)
30	Deviation 100-µA Senor	B	+0.100 to +5.00	35, 52/36, 52	30	1), 5)
31	Offset 1-mA Sensor	B	-0.100 to +0.100	35, 52/37, 52	31	1), 5)
32	Test voltage 100-A Senor	B	-0.410 to -0.190	35, 52/37, 52	32	1), 5)
33	Test voltage 1-mA Senor	B	-3.540 to -2.420	35, 52/37, 52	33	1), 5)
34	Offset AC, Ran. 1		-0.500 to +0.500	38, 44, 47	34	
35	Offset AC, Ran. 2		-0.050 to +0.050	39, 44, 47	35	
36	Offset AC, Ran. 3		-0.010 to +0.010	40, 44, 47	36	
37	Offset AC, Ran. 4		-0.010 to +0.010	41, 44, 47	37	
38	(I-Offset DC) * 3 GΩ		-0.075 to +0.075	39, 45, 47	38	
39	Tuning voltage [TPO]		-1.200 to -0.040	63, 54	39	
40	-6 V		-0.575 to -0.611	56	40	
41	Σ(±15 V)		-0.077 to +0.077	58	41	
42	Σ(±5 V)		-0.026 to +0.026	59	42	
43	Offset A/D converter		-0.250 to +0.250	50	43	
44-46	reserved					6)
47	Timeout A/D					
48	D/A set. AC	A	2 to 0FEh	8, 12, 14, 46	48	1), 3)
49	D/A set. AC	B	2 to 0FEh	27, 31, 33, 48	49	1), 3)
50	D/A set. DC		2 to 0FEh	39, 44, 47, 45	50	3)
51	D/A set. 50 MHz		2 to 0FEh	39, 44, 45, 47	51	
52-54	reserved					6)
55	Hardware error					
56	Transmission error					
57-58	reserved					6)

1) Only with identified sensor (connect sensor in the "LOCAL" mode before calling the function), any type.

2) Only with identified, active sensor. The two voltages (± 12 V) are switched on simultaneously during the test phase.

3) The number of offset-adjustment steps depends on the respective offset error (max. ± 14 mV permitted). Subsequent to adjustment, the offset voltage is measured and evaluated by calling the corresponding function (table 9).

4) When the test has been performed, the voltage supply to the sensor is switched off (independent of the setting prior to calling the test).

5) These test functions measure the voltage at the temperature sensor with and without current switched on and thus influence 2 error bits. The respective LSB is set, if errors are found with offset measurement (without current), the MSB is set, if the voltage applied to the sensor with current switched on, exceeds the permitted limit values. Both tests are always performed, independent of the No. (13; 15/0.1 mA or 14; 16/1 mA in channel A), the test function was called by.
Both test functions can be performed with any identified sensor. If error bits are set (e.g., active sensor tested by the test function 14 + 16 instead of 13 + 15), they remain set even upon return to the test mode.

6) Reserved bits are assigned the value 0. Bits 45, 46, 47 do not contain any significant information.

7.4 Testing and Adjustment

7.4.1 Checking the Operating Voltages

Table 7-11 Supply voltages for module A2/analog board

Test point	Rated value	Tolerance	Remark; Components supplied
X102.18	+ 15 V	± 0.75 V	Voltage supply from Module A1, reference X102.20,11; N201, N202, V202, N305, N401, N402, V402, N511, (N504, N512, N513, N514, S501) N601, N602, N603, N604, U601, U602, U603
X102.17	-15 V	± 0.75 V	Voltage supply from Module A1, reference X102.20,11; N201, N202, D201, N305, N401, N402, D401, N511, (N504, N512, N513, N514, S501) N602, N603, U601, U602, U603, V622
X102.16 X102.14 X102.12	+ 5 V	± 0.15 V	Voltage supply from module A1 for digital unit of the analog board, reference X102.20; D700, D705 to D710, D751, (S501), U703, U704, V728, V732
G104.1 (+C119)	+ 5 V	± 0.15 V	If the + 15-V supply works correctly; D106, D107, D201, D202, D204, D321, D322, D323, D401, D402, D404, D604
G105.1 (-C121)	-5 V	± 0.15 V	If the -15-V supply works correctly; D202, D204, D321, D322, D323, D402, D404
G600.6	+ 5 V	± 0.05V	If the + 15-V supply works correctly; reference voltage for ADC & + 6V D601 (via N601)
G104.1 (+C119)	+ 6 V	± 0.15 V	D203, D324, D403, D541, D542, D602, D610
G104.1 (+C119)	-6 V	± 0.15 V	D602, D610

7.4.2 Check of the Clock Signal for the Microprocessor and Volcon

- Connect a frequency counter via a 10:1 probe at D700.40 (42) to check the clock signal. The clock frequency should be 12 MHz ± 0.012 MHz (0.1%).

- Check the clock signal at D751.21 using an oscilloscope (C_{sensor} < 15 pF). The ampitude should be at least 3.5 V_{pp}.

7.4.3 Checking the Temperature Measuring Currents

It is required for checking the temperature measuring currents to connect the inputs of the calibration adapter (banana plug) via a 3.01-kΩ ±1% resistor. Calling the service function "DIAG:AHAR? No" shortly switches on the corresponding current (No) and the dropping voltage at the 3.01-kΩ resistor is measured. This voltage (V_r) should be within the following ranges:

Measuring current = 0.1 mA:	-0.297 V ≤ V_r ≤ -0.288 V	(for active sensors)
Measuring current = 1.0 mA:	-3.016 V ≤ V_r ≤ -2.919 V	(for passive sensors)

- Initialize calibration adapter in test channel A.
  (Connect in "LOCAL" mode or "INIT:SENS(?)" in REM mode)

- Set calibration adapter for measurement of the temperature sensor
  → **"DIAG:ASET 100"**

- Call test function **"DIAG:AHAR? 13"** (0.1 mA)
  or **"DIAG:AHAR? 14"** (1 mA).

- Read and evaluate the current voltage value V_r at the 3.01 kΩ resistor.

  Check the temperature measuring currents in test channel B correspondingly:

- Initialize calibration adapter in test channel B
  → **"INIT:SENS"**

- Initialize temperature measurement in channel B
  → **"DIAG:ASET 104"**

- Call test function **"DIAG:AHAR? 30"** (0.1 mA)
  or **"DIAG:AHAR? 31"** (1 mA)

- Read and evaluate the current voltage value V_r at the 3.01 kΩ resistor.

Note: *Cyclic measurements are nor performed when testing the temperature measuring currents by means of the calibration adapter. The measuring current is 0.1 mA for active sensors and 1 mA for passive sensors.*

7.4.4 Adjustment of the Test Generator

Preparation

- The analog board is installed in the basic unit NRVD, the cover ot the analog board is fixed by screwed and the coaxial cable W10 is connected to X114 (test generator output). The lower housing shell of the basic unit is not fitted.

- Connect a frequency counter with a 50-Ω termination to the output of the test generator (N-socket "TEST" on the front panel).

- Switch on the test generator in the NRVD operation menu.
  (Key sequence **"SPEC" → "TEST.GEN" → "ON/OFF"**)

7.4.4.1 Frequency Adjustment

Adjust the frequency of the test generator to 50 MHz ± 0.5 MHz using L 503 (accessible via hole in the cover of the analog board).

7.4.4.2 Checking the Reflection Coefficient

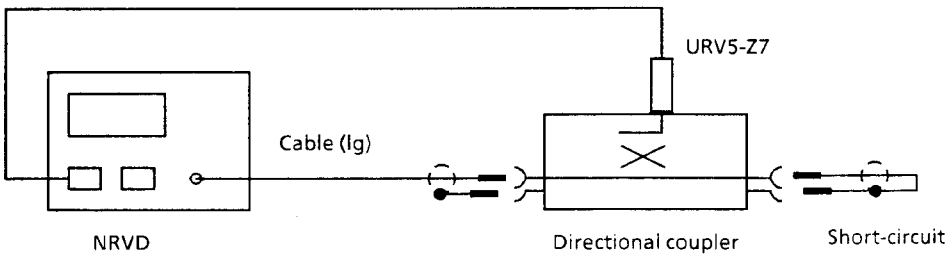


Fig. 7-10 Test setup for check of the reflection coefficient

- Connect directional coupler URV5-Z9 (selected acc. to table 7-4) to the output of the test generator (N-socket "TEST" on the front panel) via a low-loss 50-Ω line of 0.75 m electric length.
- Measure the amplitude of the reflected wave with open (V_1) and shortcut output (V_2).
- Calculating the reflection coefficient:
  When the measurement plane is shifted, the absolute value of the imaginary impedance-component directly leads to a change of the amplitude of the reflected wave with a changeover of the terminating impedance from short-circuit to idle state. The absolute reflection coefficient is thus

$$r = \left| \frac{V_1 - V_2}{V_1 + V_2} \right|$$

  which should be max. 0.01. If it exceeds 0.01, adjust L501 to the minimum of the voltage difference (V_1-V_2).

7.5 Removal and Assembly

7.5.1 Removal and Installation of the Analog Board

Removal:

- Take off both rear-panel feet after removing the four fixing screws and withdraw the lower shell of the housing to the rear (item 17 + 18, 4x item 19, it. 1).
- Remove cable W4 from the support on the analog board and withdraw at the connector X101 (analog board).
- Withdraw cables W150 and W3 from the analog board.
  Disconnect coaxial cable W10 from the analog board (key width #6) and remove.
- Remove the 5 combi screws from the analog-board fixing.
- Lift the analog board at the side of the voltage regulators and remove from the basic unit.
- Undo the fixing screws of the screening cover and take off cover.

Note: *If test measurements are only to be performed at the provided test points of the analog board, it is sufficient to remove the screening cover of the analog board. The cable W4 can be reconnected.*

Installation:

- Carefully mount the analog board again in the reverse order. It is advisable to insert the combi-screw on the edge below the filter panel into the respective hole before mounting the analog board.
- The connecting cable W150 to the module A1/controller board must be put together in the partition slot such that is does not touch the switch stick of the power switch.
- The RF screening on the rear panel must not be damaged.

7.5.2 Service Position of the Analog Board

The board can be inserted upend into the slots provided on the lower side panel of the basic unit for service purposes. This position allows for access to both sides of the board in operating mode.

For this purpose, remove the analog board from the basic unit NRVD according to 7.5.1 and insert into the guide slots (fig. 7-14). Take the connecting cable W150 to the controller board out of the slot in the partition and connect it to the analog board (connector X102). The cable W4 from the filter board is reconnected to X101.

7.6 Interfaces

Pin	Name	Input/ Output	Origin/ destination	Specified range	Signal description
X101.1, 2, 15 to 18, 31			A4, Filter board		Ground
X101.3, 6, 8	ARGND	Output		-11.58 to -13 V	Analog ground channel A - Power supply to test channel A
X101.4	- INPA	Input		max ± 22 V	- Test input of test channel A
X101.5	+ INPA	Input		max ± 22 V	+ Test input of test channel A
X101.7	DCINP1	Input		max. ± 0.17 mA	DC input of test channel A
X101.9	TEMPA	Output		I = 0.95 to 1.05 mA/ - 3 V I = 98 to 102 µA/ - 0.24 V	Connector for temperature measurement of test channel A
X101.10	CLKP1	Output		L < = 1 V, H > = 4 V	Clock signal of test channel A
X101.11	DATP1			L < = 1.5 V, H > = 3.5 V	Data line of test channel A
X101.12	RSTP1	Output		L < = 1.44 V, H > = 3.7 V	Reset test channel A
X101.13	ID1	Output		L < = 1.44 V, H > = 3.7 V	Identification test channel A Verify-program
X101.14	VCC1	Output		0 V; 4.8 to 5.3 V 11.4 to 12.6 V	Positive power supply (sensor A)
X101.19, 22, 24	BRGND	Output		-11.58 to -13 V	Analog ground channel B - Power supply to test channel B
X101.20	- INPB	Input		max ± 22 V	- Test input of test channel B
X101.21	+ INPB	Input		max ± 22 V	+ Test input of test channel B
X101.23	DCINP2	Input		max. ± 0.17 mA	DC input of test channel B
X101.25	TEMPB	Output		I = 0.95 to 1.05 mA/ - 3 V I = 98 to 102 µA/ - 0.24 V	Connector for temperature measurement of test channel B
X101.26	CLKP2	Output		L < = 1 V, H > = 4 V	Clock signal of test channel B
X101.27	DATP2			L < = 1.5 V, H > = 3,5 V	Data line of test channel B
X101.28	RSTP2	Output		"	Reset test channel B
X101.29	ID2	Output		" "	Identification test channel B verify program
X101.30	VCC2	Output		0 V; 4.8 to 5.3 V 11.4 to 12.6 V	Positive power supply (test channel B)
X102.5	VCC5	Input	A1, Processor	4.85 V to 5.15 V	Supply voltage
X102.7	VCC4	Input		4.85 V to 5.15 V	(+ 5 V Digital)
X102.9	VCC3	Input		4.85 V to 5.15 V	(+ 5 V Digital)
X102.11, 19, 20	GND				Digital ground

Pin	Name	Input/ Output	Origin destination	Specified range	Signal description
X102.12, 14, 16	+5VD	Input	A1, Processor	4.85 V to 5.15 V	Supply voltage
X102.4	RST	Input		L = 3 to 8 mA	Reset
X102.6	INT	Input		H = 0 to 0.5 mA	Interrupt
X102.8	Datum1	Input		(Voltage approx 3.6 V)	Data input
X102.13	Datum2	Output		(Voltage approx 3.6 V)	Data output
X102.15	Clock	Output		(Voltage approx 3.6 V)	Clock signal
X102.18	+15V	Input		14.25 to 15.75 V	Voltage supply
X102.17	-15V	Input		-14.25 to -15.75 V	Voltage supply
X103.2	DCINP	Input	NRVD-B2 Connector board	-15 V to 15 V	DC-Freq. input
X103.1, 3	RINP5	Input			Ref. GND
X114	TESTOUT	Output		50 MHz 0.9 to 1.1 mW	Test generator output
X641.1	INP0	Output		-5.5 to 5.5 V	AC amplifier A
X641.2	INP1	Output		-5.5 to 5.5 V	DC amplifier
X641.3	INP2	Output		-5.5 to 5.5 V	AC amplifier B
X641.4	INP3	Output		-5.5 to 5.5 V	DC output Cal generator
X641.5		Output		0 V	ADC reference point
X641.6		Output		-5.5 to 5.5 V	Temp. test channel A
X641.7		Output		-5.5 to 5.5 V	Temp. test channel B
X641.8		Output		-5.5 to 5.5 V	Ext. f-DC
X641.9		Output		-5.5 to 5.5 V	Analog. MUX-OUT
X642.1		Output		-5.5 to 5.5 V	Analog. MUX-OUT
X642.2		Output		-5.5 to 5.5 V	ADC input
X211.1		Input		-2 to 2 V	AC amplifier input
X211.2		Input		-2 to 2 V typ.	AC amplifier input
X212.1		Input		7.3 to 9.2 V	AC amplifier ref.
X212.2		Input		-11 to 11.2 V	AC amplifier offs.
X411.1		Input		-2 to 2 V	AC amplifier input
X411.2		Input		-2 to 2 V typ.	AC amplifier input
X412.1		Input		7.3 to 9.2 V	AC amplifier ref.
X412.2		Input		-11 to 11.2 V	AC amplifier offs.

FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR

ZEICHN.-NR.

X101 1
X101 2
X101 3
X101 4
X101 5
X101 6
X101 7
X101 8
X101 9
X101 10
X101 11
X101 12
X101 13
X101 14
X101 15
X101 16
X101 17
X101 18
X101 19
X101 20
X101 21
X101 22
X101 23
X101 24
X101 25
X101 26
X101 27
X101 28
X101 29
X101 30
X101 31
X101 32
X101 33
X101 34

C113 1N L
C114 1N L

TEMPA
CLKP1
DATP1
RSTP1
ID1
VCC1
TEMPB
CLKP2
DATP2
RSTP2
ID2
VCC2

+5V -5V +6V -6V +15V -15V

-INPA
+INPA
ARGND

AC AMPLIF A
ON SHEET2

ASELA BSELA BG-C BG-B BG-A
D7 D6 D5 D4 D3 D2 D1 D0 LE1

DISCHA
INP0
INP1

DCINP1
DCINP2

DC AMPLIF
ON SHEET3

D7 D6 D5 D4 D3 D2 D1 D0 LE2

SEL3 SEL2 G1 G0

-INPB
+INPB
BRGND

AC AMPLIF B
ON SHEET4

BSELA BSELB BG-C BG-B BG-A
D7 D6 D5 D4 D3 D2 D1 D0 LE4

D106-A
74HCT574T-B
LE0
D107-A
74HCT574T-L
LE3
EN C1 1D

R156 1K L
R155 1K L

C109 100P L
C108 100P L
C110 100P L
C112 100P L
C111 100P L

CDISB

X103 1
X103 2
X103 3
X103 4
COD.
DCINP
RINP5

MXADCTRL
ON SHEET6
ON SHEET7

RSTP1 RSTP2 TEMPA TEMPB ID2 DATP2 CLKP2 VCC2 ID1 DATP1 CLKP1 VCC1
CDISB LE7 LE6 LE5 LE4 LE3 LE2 LE1 LE0 CTRLH CTRLL D7 D6 D5 D4 D3 D2 D1 D0 A3 A2 A1 A0

DISCHB INP2 INP3 +REF TPO

+15V -15V +5VD

TESTGENERATOR
ON SHEET5

X114 1
X114 2
X114 3
X114 4
X114 5
TESTOUT

CTRLH CTRLL

HVC-WARN

+5V

D106-B
D107-B
C106 100N L
C107 100N L

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05/00	45084
AEND. IND.	AENDERUNG MITTEI

MXADCTRL

ON SHEET6

ON SHEET7

DC AMPLIF

ON SHEET3

AC AMPLIF B

ON SHEET4

TESTGENERATOR

ON SHEET5

COD.

X103 1
X103 2
X103 3
X103 4

DCINP
RINP5

DISCHA
INP0
INP1

RSIP1
RSIP2
TEMPA
TEMPB
ID2
DATP2
CLKP2
VCC2
ID1
DATP1
CLKP1
VCC1

+5V -5V +6V -6V +15V -15V

+5VD

C117 100N L
C116 100N L
C115 100N L

GND

CLOCK
DATUM2
VCC3
DATUM1
VCC4
INT
VCC5
RST

X102 20
X102 19
X102 18
X102 17
X102 16
X102 15
X102 14
X102 13
X102 12
X102 11
X102 10
X102 9
X102 8
X102 7
X102 6
X102 5
X102 4
X102 3
X102 2
X102 1

CDISB CDISA LE7 LE6 LE5 LE4 LE3 LE2 LE1 LE0 CTRLH CTRLL D7 D6 D5 D4 D3 D2 D1 D0 A3 A2 A1 A0

DISCHB INP2 INP3 +REF TPO

X114 1
X114 2
X114 3
X114 4
X114 5

TESTOUT

-INPB
+INPB
BRGND

SELB SELA G1 G0

BSELA BSELB BG-C BG-B BG-A

D107-A
74HCT574T-L

EN C1 1D

LE3

R155 1K L

C109 100P L
C108 100P L
C110 100P L
C112 100P L
C111 100P L

HVC-WAND
HVC
765 4 8 123
GND

ANALOG DIGITAL

G104
78L05-L

G105
79L05-L

C103 100N L
C118 100U 25V
C104 100N L
C123 100U 25V

R157 2K21 L
C119 100U 25V
C120 100N L
R154 2K21 L
C121 100U 25V
C122 100N L

+15V -15V +5V -5V

D106-B
D107-B
C106 100N L
C107 100N L

08/00	47627	03.92	SR	1KGU	TAG	NAME	BENENNUNG
				BEARB.		SR	ANALOGPLATTE
				GEPR.		SR	ANALOGBOARD
				NORM			
				PLOTT	17.03.92		
05/00	45085	01.92	SR	ROHDE&SCHWARZ			ZEICHN.-NR. 857.8150.01S
AEND. IND.	AENDERUNGS MITTEILUNG	DATUM	NAME	ZU GERAET NRVD			BLATT-NR. 1 V. 7 BL.
				REG.I.V. 857.8008		ERSTE Z. 857.8008	

FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR

ZEICHN.-NR.

+INPA
R215 5K62 L
V240 PN4118A
V244 PN4118A
R298 100K L
V243 PN4118A
R296 100K L
R291 475K L
R297 10M
V235 PN4118A
V239 PN4118A
R206 100K L
R204 221K
C232 82P L
V234 PN4118A
V238 PN4118A
R201 100K L
V236 SST177-L
R202 221K
V237 PN4118A
R200 100K L
R203 475K L
R268 10M
C226 68P L
V241 PN4118A
R205 100K L
-INPA
R216 5K62 L
R269 1G
R26 1G L
V24
V242 SST177-L
V229 PN4118A
R288 100K L
R289 121K L
R267 100K L
V228 PN4118A
R270 100K L
DISCHA (SH6/U602)
D201-A HEF4052BT-L
(SH1/D106) ASELA
(SH1/D106) ASELB
MUXDX
K200-B
K200-C
ARGND
N200 LM79L12ACD-B
IN OUT COMMON
-15V
C200 4N7 L
C202 100N L
R272 1K L
R273 121R L
V233 BAS32-L
V230 5V6 L
+5V
-15V
C241 10N L
R207 6K81 L
D201-B
+15V
K200-A
V201 BAS32-L
R240 1K5 L
C240 100U 16V TA
R241 22K1 L
SPG2
(SH7/D700)
V202 BC850B L
X211 1
X211 2
R208 33K2 0.1%
R212 33K2 0.1%
R263 4M7 L
V227 BAV99-L
V226-A SST404-L
V226-B SST404-L
C201 27P L
C236 27P L
X212 2
R213 4M7 L
AG-A
AG-B
AG-C
(SH1/D106)
R290 10K 0.1%
R264 10K 0.1%
N201-A TL072ACD-L
R250 10K L
V232 6V8 L
R299 15K L
R209 22K1 L
X212 1
* - NICHT BESTUECKT/
NOT IN PCB
D202-A 74HC4051T-L
* R220 5M6 L
R271 2M67
R204 1M21
R211 549K
R277 249K
R266 110K L
R265 46K4 L
* R221 10K2 L
R214 10K L

08/00	47621
05/00	45085
AEND. IND.	AENDE MITTE

V244
PN4118A
V243
PN4118A
V239
PN4118A
V238
PN4118A
V237
PN4118A
V241
PN4118A
V229
PN4118A
R298 100K L
R296 100K L
R206 100K L
R201 100K L
R200 100K L
R205 100K L
R288 100K L
R270 100K L
D201-A
HEF4052BT-L
MUXDX
R273 121R L
V230
5V6 L
C241 10N L
R287 6K81 L
D201-B
+5V
-15V
X211 1
X211 2
+15V
R208 33K2 0.1%
R212 33K2 0.1%
R263 4M7 L
V227 BAV99-L
V226-A SST404-L
V226-B SST404-L
R290 10K 0.1%
R264 10K 0.1%
R299 15K L
N201-A TL072ACD-L
V232 6V8 L
R209 22K1 L
X212 1
-15V
X212 2
N201-B TL072ACD-L
C230 680P L
R281 274K L
R213 4M7 L
C201 27P L
C235 27P L
N202 OP07CS8-L
R210 147K L
R292 294K
R293 590K
R207 1M21
R275 2M43
R294 4M75
R295 10M
R276 147K L
-6V
R274 1K L
LE1
(SH7/D705)
D0
D1
D2
D3
D4
D5
D6
D7
EN
C1
1D
D203-A
74HC574T-L
C228 1N L
R280 10K L
* R222 5M62
R283 2M67
C233 3P3 L
R282 1M21
C235 8P2 L
R285 549K
C231 15P L
R286 249K
C234 39P L
R278 110K
C229 82P L
R279 46K4
* C223 220P L
* R223 18K2
D204-A
74HC4051T-L
AG-A
AG-B
AG-C
(SH1/D106)
R250 10K L
+5V
V231 BAV99-L
INP0
(SH6/D602)
-5V
D202-A
74HC4051T-L
* R220 5M6 L
R271 2M67
R284 1M21
R211 549K
R277 249K
R266 110K L
R265 46K4 L
* R221 18K2 L
R214 10K L
* - NICHT BESTUECKT/
NOT IN PCB
+15V
C237 100N L
N201-C
C238 100N L
-15V
D204-B
D202-B
+6V
D203-B
C227 4N7 L

08/00	47627	03.92	SR	1KGU	TAG	NAME	BENENNUNG
				BEARB.		SR	AC AMPLIF A
				GEPR.		SR	**ANALOGPLATTE**
				NORM			ANALOGBOARD
				PLOTT	17.03.92		
05/00	45085	01.92	SR				ZEICHN.-NR. **857.8150.01S** BLATT-NR. 2 V. 7 BL.
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			
				ZU GERAET NRVD			REG.I.V. 857.8008 ERSTE Z. 857.8008

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BEHALTEN WIR UNS ALLE RECHTE VOR

G1 (SH1/D107)
G0 (SH1/D107)

D323-A
74HC4052T-L

SELB
R328 1K L
D321-A
SCL4052BE
R313 121R L
R314 121R L
MUXDX

DCINP2
DCINP1

D322-A
SCL4052BE
SELA
SELB
R318 121R L
MUXDX

R320 1K L
R321 147K
R315 4K75
R309 4M75
R308 4M32

C316 100N L
+15V
N305
LT1056S8-L
R322 10K L
C317 100N L
C308 1N L
-15V

R319 18K2
C309 4N7 L
R323 182K
C311 470P L
R324 1M82
C312 47P L
R326 10M
R325 8M25
R327 0R
C313 1P2 L
+5V
V301 BAV99-L
-5V
INP1 (SH6/D602)

R310 147K
R329 294K
R312 590K
R307 1M21
R330 2M43
R317 4M75
R316 10M
R311 90R9
-6V

R300 1K B
LE2
EN
C1
D324-A
74HC574T-B
(SH2/D203)

+5V
R306 10K L
C315 100N L
-5V
D321-B
D322-B
D323-B
+6V
C310 100N B
D324-B

00/00	47627	03.92	SR	TKGU	TAG	NAME	BENENNUNG
				BEARB.		SR	ANALOGPLATTE
				GEPR.		SR	ANALOGBOARD
				NORM			
				PLOTT	17.03.92		
00/00	45085	01.92	SR	ROHDE&SCHWARZ			ZEICHN.-NR. 857.8150.01S
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU ERSETZ.	NRVD		BLATT-NR. 3 v. 7 BL.
				REG I.V.	857.8008	ERSTE Z.	857.8008

FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR

+INPB
R415 5K62 L
-INPB
R416 5K62 L
V435 PN4118A
V434 PN4118A
V436 SST177-L
R491 475K L
R403 475K L
R489 121K L
R467 100K L
DISCHB (SH6/U602)
R497 10M
R404 221K
R402 221K
R468 10M
C432 82P L
C426 68P L
R469 1G
R46 1G L
V440 PN4118A
V44*
V442 SST177-L
V428 PN4118A
V444 PN4118A
V443 PN4118A
V439 PN4118A
V438 PN4118A
V437 PN4118A
V441 PN4118A
V429 PN4118A
R498 100K L
R496 100K L
R406 100K L
R401 100K L
R400 100K L
R405 100K L
R488 100K L
R470 100K L
D401-A HEF4052BT-L
(SH1/D107) BSELA
(SH1/D107) BSELB
MUXDX
R472 1K L
R473 121R 1
V433 BAS32-L
V430 5V6 1
C441 10N L
R407 6K81 1
D401 B
+5V
-15V
* - NICHT BESTUECKT/
NOT IN PCB
K400-B
K400-C
BRGND
N400 LM79L12ACD-L
IN OUT
COMMON
-15V
C400 4N7 L
C402 100N L
+15V
K400 B
V401 BAS32-L
R440 1K5 1
C440 10U 16V TA
R441 22K1 L
SPGS
V440 BC858B 1
X411 1
X411 2
X412 2
X412 1
+15V
-15V
R408 33K2 0.1%
R412 33K2 0.1%
R413 4M7 L
R463 4M7 L
V427 BAV99-L
V426-A SST404-L
V426-B SST404-L
C401 27P L
C436 27P L
BG-A
BG-B
BG-C
(SH1/D107)
R464 10K 0.1%
R490 10K 0.1%
N401-A TL072ACD-L
V432 6V8 L
R409 22K1 L
R499 15K L
D402-A 74HC4051T-L
R471 2M67
R484 1M21
R411 549K
R477 249K
R466 110K L
R465 46K4 L
* R421 18K2 L
R414 10K L
* R420 5M6 L

08/00
05/00
AEND. IND.

V444 PN4118A
V443 PN4118A
V439 PN4118A
V438 PN4118A
V437 PN4118A
V441 PN4118A
V429 PN4118A
R498 100K L
R496 100K L
R406 100K L
R401 100K L
R400 100K L
R405 100K L
R488 100K L
R470 100K L
D401-A HEF4052BT-L
MUXDX
R473 121R L
C441 10N L
R447 6KM1 L
D401-B
* - NICHT BESTUECKT/ NOT IN PCB
X411 1
X411 2
R463 4M7 L
V427 BAV99-L
V426-A SST404-L
V426-B SST404-L
R408 33K2 0.1%
R412 33K2 0.1%
+15V
R490 10K 0.1%
R464 10K 0.1%
R499 15K L
V432 6V8 L
R409 22K1 L
N401-A TL072ACD-L
X412 1
-15V
X412 2
R413 4M7 L
C401 27P L
C436 27P L
N401-B TL072ACD-L
C430 680P L
R481 274K L
R410 147K L
R492 294K
R493 590K
R407 1M21
R475 2M43
R494 4M75
R495 10M
R476 147K L
-6V
N402 OP07CS8-L
R450 10K L
C428 1N L
R480 10K L
* R422 5M62
R483 2M67
C433 3P3 L
R482 1M21
C435 8P2 L
R485 549K
C431 15P L
R486 249K
C434 39P L
R478 110K
C429 82P L
R479 46K4
* C423 220P L
* R423 18K2
D404-A 74HC4051T-L
BG-A
BG-B
BG-C
(SH1/D107)
R474 1K L
LE4 (SH7/D705)
EN
C1
D403-A 74HC574T-L
+5V
-5V
V431 BAV99-L
INP2
(SH6/D602)
D402-A 74HC4051T-L
* R420 5M6 L
R471 2M67
R404 1M21
R411 549K
R477 249K
R466 110K L
R465 46K4 L
* R421 10K2 L
R414 10K L
C437 100N L
N401-C
C438 100N L
D404-B
D402-B
D403-B
+6V
C427 4N7 L

08/00	47627	03.92	SR	1KGU	TAG	NAME	BENENNUNG
				BEARB.		SR	AC AMPLIF B
				GEPR.		SR	ANALOGPLATTE
				NORM			ANALOGBOARD
				PLOTT	17.03.92		
05/00	45085	01.92	SR				ZEICHN.-NR. 857.8150.01S
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET	NRVD		REG.I.V. 857.8008 ERSTE Z. 857.8008

ROHDE&SCHWARZ

BLATT-NR. 4 V. 7 BL.

FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR

TPD

+6V

R560 10K 0.1%

R558 27K1 0.1%

N511-A TL072ACD-L

R579 82K5 L

R580 18K2 L

V579 HSMS2800-L

R581 18K2 L

R547 82K5 L

R546 10K L

N511-B TL072ACD-L

V578 HSMS2800-L

C567 4N7 L

C570 10N L

R543 100K L

R550 100K L

R548 10K L

R561 1K L

R549 1K L

C568 1U 25V TA L

C524 5P6 L

C525 1N L

V525 BB620-L

R585 10K L

R586 5K62 L

L504 4U7H

C572 33P 1% CG L

C563 5P6 L

L503 530NH

C566 33P 1% CG L

C507 6P8 L

V524 BC850B-L

R587 33R2 L

C565 10N L

R588 1K21 L

C573 1N L

R574 8M25

R584 10M

R554 1M21

R559 4M75

R582 300K 0.1%

R526 300K 0.1%

R589 10M

R571 56K2 L

R575 300K 0.1%

D541-A 74HCT574T-L

LE7

R555 1M2 L

R572 2M43

R552 300K 0.1%

R583 300K 0.1%

D0 D1 D2 D3 D4 D5 D6 D7

R556 10K L

U603-C LM339D-L

+2.5V

R538 18K2 L

V577 BC850B-L

-15V

R530 221R L

L501 30NH

R545 100R 0.1%

TESTOUT

C571 220P-L

R552 100R 0.1%

R535 2K74 L

R533 10R L

R534 1R

R539 1K5

C562 33P L

R541 221R L

R537 10K 0.1%

S501-A DG413DY-L

S501-B DG413DY-L

C564 10N L

R540 1K5 L

N512 LT1028CJ8

+15V

-15V

R506 47K5 L

N504 OP07CS8-L

INP3

(SH6/D602)

R505 47K5 L

* - NICHT BESTUECKT/
NOT IN PCB

+6V

+15V

R563 1K8 0.1%

N514 OP07CS8-L

R544 100R L

R568 1K84 0.1%

R565 10K 0.1%

R536 100R L

R542 10K 0.1%

N513 OP07CS8-L

R553 8M25

R567 4M75

R576 2M43

R557 300K 0.1%

R573 1M2 L

R566 56K2 L

R564 1M21

R570 300K 0.1%

R590 300K 0.1%

R591 300K 0.1%

R569 300K 0.1%

D542-A 74HCT574T-L

LE6

R551 10K L

CTRLH

CTRLL

R501 10K L

S501-C

S501-D

S501-E

+5VD

D541-B

D542-B

C574 4N7 L

N511-C

00/00	47627	03.92	SR	1KGU	TAG	NAME	BENENNUNG
				DEARB.		SR	ANALOGPLATTE
				GEPR.		SR	ANALOGBOARD
				NORM			
				PLOTT	17.03.92		
09/00	45085	01.92	SR	ROHDE&SCHWARZ			ZEICHN.-NR. 857.8150.01S
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET NRVD			BLATT-NR. 5 v. 7 BL.
				REG.I.V. 857.8008		ERSTE Z. 857.8008	

ZEICHN.-NR.

ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING

STROMLAUF GILT FUER VAR.02

CIRCUIT DIAGRAM IS VALID FOR MOD.02

* = NICHT BESTUECKT/NOT IN PCB

FUER DIESE UNTERLAGE BEHALTEN WIR UNS ALLE RECHTE VOR

ZEICHN.-NR.

DCINP
RINP5 (SH1/X103)
R645 1M
C633 470P L
R633 332K
R634 10K
R635 3K01 L
* V625 BAV99-L
R632 4K75 L
V623 BAV99-L
N603-B TL072ACD-L
+5V
-5V

N602-A TL072ACD-L

X641 9
X641 8
X641 7
X641 6
X641 5
X641 4 (SH5/N504) INP3
X641 3 (SH4/V431) INP2
X641 2 (SH3/V301) INP1
X641 1 (SH2/V231) INP0

D602-A HEF4051BT-L
MUXDX

TEMPA
TEMPB
V649 BAV99-L
V602 BAV99-L
R649 57K6 0.1%
R636 3K01
R602 57K6 0.1%
R603 3K01
R637 27K4 L
R647 27K4 L
R600 27K4 L
R601 27K4 L
V637 BSS123-L
V647 BSS123-L
V600 BSS123-L
V601 BSS123-L
-6V

U602-A LM339D-L
U602-B LM339D-L
U602-C LM339D-L
U602-D LM339D-L
R639 10K L
R638 10K L
+2.5V

U603-D LM339D-L
R666 10K L
U603-A LM339D-L
U603-B LM339D-L
(SH1/D106) CD1SN
(SH1/D107) CD1SB
(SH2/V289) D1SCHN
(SH4/V489) D1SCHB

D604-A 74HCT574T-L
R699 10K L
EN
C1
D0
D1
D2
D3
D4
D5
D6
D7

D601-D HEF4070BT-L
R643 1K L
VC (D601.14)

D610-A HEF4051BT-L

TPO (SH5/N511)
R604 11K L
R610 100K L
-6V
R605 11K L
R611 200K L
VCC1
* R612 200K L
ARGND
R606 11K L
R613 200K L
VCC2
* R614 200K L
BRGND
R607 11K L
R615 200K L
+15V
R616 200K L
-15V
R608 11K L
R617 200K L
+5V
R618 200K L
0V
R609 11K L

D601-C HEF4070BT-L
R629 1K L
D601-B HEF4070BT-L
D601-A HEF4070BT-L
R628 1K L
X642 1
X642 2
R646 33K2 L
R630 98K
C612 100N 50V
R631 274K

+15V
C601 100N L
R640 47K5
R648 27K4
G600 REF02CP
N601 LF411CN
R650 22R1 L
C613 100N L
R624 5K62

08/00
05/00
IND.
IND.

ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING

STROMLAUF GILT FUER VAR.02

CIRCUIT DIAGRAM IS VALID FOR MOD.02

* = NICHT BESTUECKT/NOT IN PCB

D601-C HEF4070BT-L
D601-B HEF4070BT-L
D601-A HEF4070BT-L
R629 1K L
R628 1K L
SMOUT (SH7/D700)
TAKTOUT (SH7/D700)
V623 BAV99-L
N602-A TL072ACD-L
X642 1
X642 2
R646 33K2 L
R630 98K8 0.1%
C612 100N 50V
R631 274K
C611 1N 100V
D602-A HEF4051BT-L
MUXDX
+15V
+5V
GND
R627 2K21 L
N602-B TL072ACD-L
U601 LM211D-L
AMI (SH7/D700)
R640 47K5
R648 27K4
C601 100N L
-15V
VC (R643)
D601-E
N602-C
N603-C
U602-E
U603-E
TPO (SH5/N511)
R604 11K L
R610 100K L
-6V
R605 11K L
R611 200K L
VCC1
* R617 200K L
ARGND
R606 11K L
R611 200K L
VCC2
* R619 200K L
ARGND
R607 11K L
R603 3K01
D610-A HEF4051BT-L
D601-D HEF4070BT-L
R643 1K L
VC (D601.14)
G600 REF02CP
N601 LF411CN
C613 100N L
N604 OP07CS8-L
R641 100R L
V622 BC850B-L
C610 1N L
R651 100R L
R626 1K1 0.1%
+6V
R624 5K62 0.1%
R625 6K81 0.1%
N603-A TL072ACD-L
D602-B
D610-B
D604-A 74HCT574T-L
D604-B
C614 100N L

08/00	47627	03.92	SR	1KGU	TAG	NAME	BENENNUNG
				BEARB.		SR	ANALOGPLATTE
				GEPR.		SR	ANALOGBOARD
				NORM			
				PLOTT	17.03.92		
05/00	45005	01.92	SR	ROHDE&SCHWARZ			ZEICHN.-NR. 857.8150.01S
AEND. IND.	AENDERUNGS MITTEILUNG	DATUM	NAME	ZU GERAET	NRVD		BLATT-NR. 6 V. 7 BL.
				REG.I.V.	857.8008	ERSTE Z.	857.8008

FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR

V712 BCP69-16-L
R703 47R 2.4W
V703 BAS32-L
+15V
VCC2 (SH1/X101)
R711 10K L
G700 LM340T
R705 5K62 L
R707 15K L
C702 100N L
R702 1K L
V709 BC850B-L
V705 B6V8
*V70
V706 BC850B-L
V707 BC850B-L
R712 12R1 L
GND
R720 22K1 L
R716 22K1 L

V714 BCP69-16-L
R704 47R 2.4W
V704 BAS32-L
VCC1 (SH1/X101)
R721 10K L
G701 LM340T
R709 5K62 L
R708 150K L
R701 15K L
C701 100N L
R713 1K L
V710 BC850B-L
V713 B6V8
*V71
V702 BC850B-L
V711 BAS32-L
V701 BC850B-L
R706 12R1 L
GND
R710 22K1 L
R715 22K1 L

V731 HSMS2800-L
+5VD
C724 100N L
C721 100N L
GND
19
35
11

CLOCK
DATUM2
VCC3 DATUM1
INT VCC4
(SH1/X102)
+5VD
+5VD
V704 HCPL2631
R776 2K21 L
R757 2K21 L
R756 15K L
R764 15K L
GND
R771 562R L
R755 562R L
R782 475R L
GND

(SH4/R441) SPG5
)SH2/R241) SPG2
(SH1/X101) ID2
(SH1/X101) ID1
R761 10K L
R779 10K L
V730 BC850B-L
V729 BC850B-L
R763 22K1 L
R762 22K1 L
GND

(SH1/X101) DATP1
(SH1/X101) CLKP1
(SH1/X101) DATP2
(SH1/X101) CLKP2
(SH6/D601) TAKTOUT
(SH6/D601) SMOUT
(SH6/U601) AMI
R795 825R L
R796 475R L
R797 825R L
R798 475R L

R760 150R L
R765 1M L
X715 1
X715 2
B700 12MHZ
C722 100P L
C715 47P L
GND
+5VD
V732 BC860B-L
V728 BC860B-L

D710-A 74HCT574T-L
R767 10K L
GND
EN
C1
R754 22K1 L
R758 22K1 L

(SH1/X101) RSTP2
(SH1/X101) RSTP1

LRESB VDD VDD
SPG6 SPG4 SPG3 SPG2 SPG1 SPG0
PRB2 PRB1
SPRB1 CLKPRB1 SPRB2 CLKPRB2
X2 X1 TAKTOUT SMOUT AMI
CSB WRB RDB
A3 A2 A1 A0
PORT0 PORT1 PORT2 PORT3 PORT4 PORT5 PORT6 PORT7
CLKOUT
OUTOPTIK
INOPTIK
OSZOUT
RXD TXD
ZZOFL
VSS VSS
D700 VOLCON-B

* = NICHT BESTUECKT/NOT IN PCB

+5VD
C723 100N L
GND
R778 100K L
R759 100K L
R775 100K L
R774 100K L
R777 100K L
R769 100K L
R773 100K L
R772 100K L
D0 D1 D2 D3 D4 D5 D6 D7

WR
RD
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
A15

D706-B 74HCT132T-L
D706-A 74HCT132T-L
D705-A 74HCT154T-L
LE0 LE1 LE2 LE3 LE4 LE5 LE6 LE7

D707-A N84256-B
OE WE CS
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7

R753 1K L
GND

08/00 47627
05/00 450[illegible]
AEND. IND. AENDERUNG MITTEILUNG

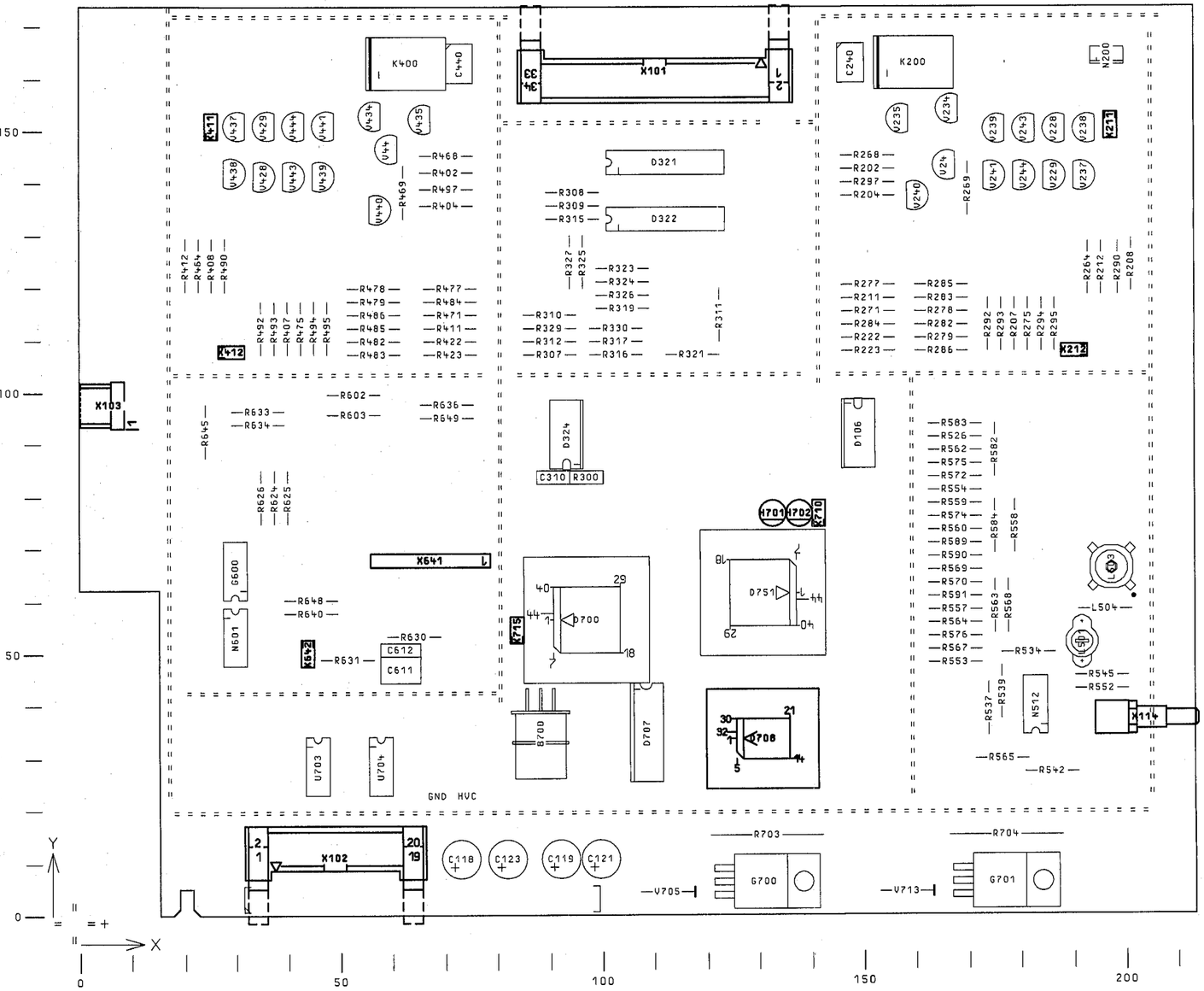
ZEICHN.-NR

* = NICHT BESTUECKT/NOT IN PCB

(SH1/X102)

08/00	47627	03.92	SR	1KGU	TAG	NAME	BENENNUNG
				BEARB.		SR	ANALOGPLATTE
				GEPR.		SR	ANALOGBOARD
				NORM			MXADCTRL
				PLOTT	17.03.92		
05/00	45085	01.92	SR	ROHDE&SCHWARZ			ZEICHN.-NR. 857.8150.01S
AEND. IND.	AENDERUNGS MITTEILUNG	DATUM	NAME	ZU GERAET NRVD			REG.I.V. 857.8008 ERSTE Z. 857.8008

BLATT-NR. 7 V. 7 BL.



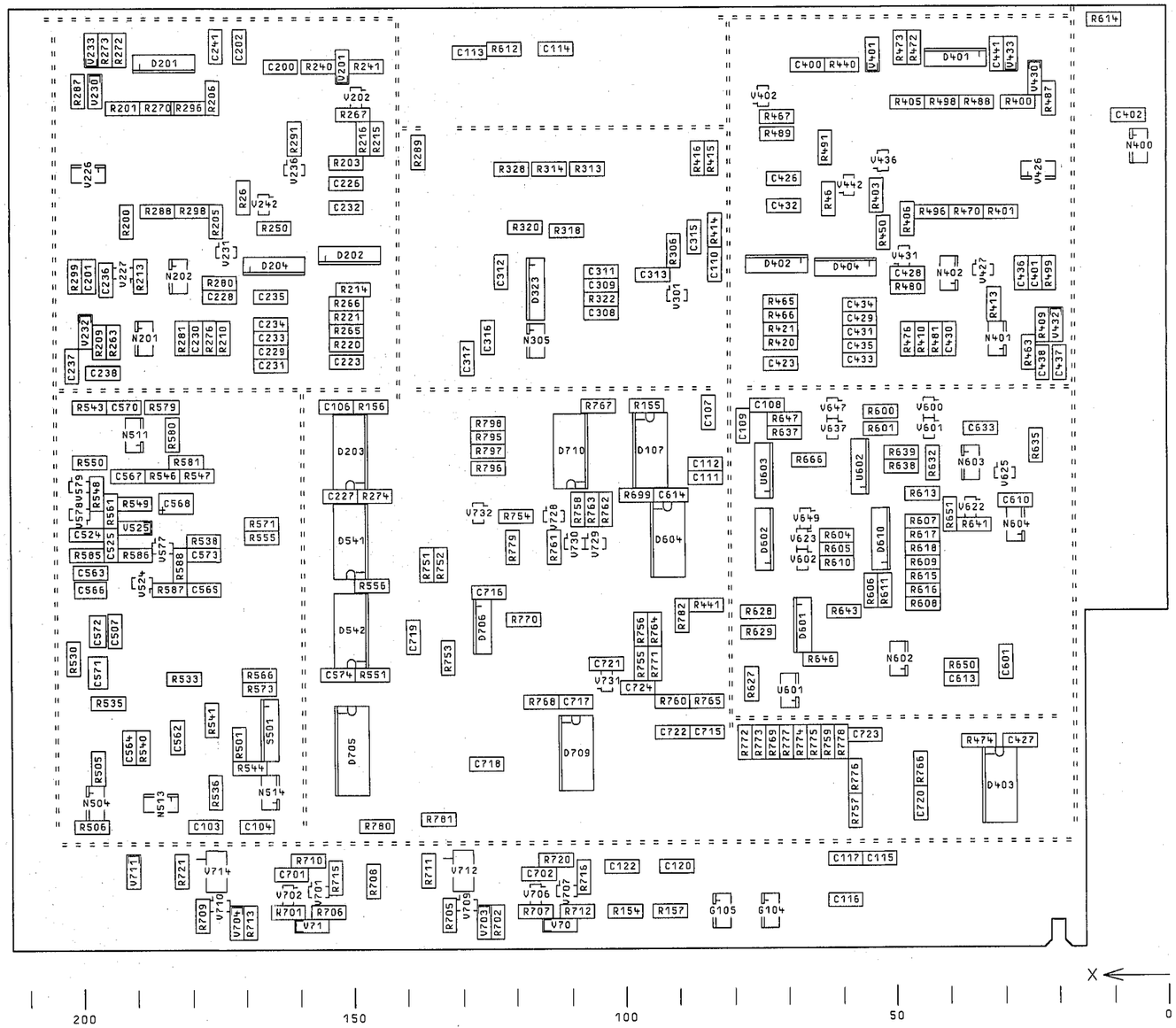
DARSTELLUNG SEITE B

VIEW ON SIDE B

09/00	47627	03.92	SR	?KGU	TAG	NAME	BENENNUNG
				BEARB.		SR	ANALOGPLATTE
				GEPR.		SR	ANALOGBOARD
				NORM			Z
				PLOTT	18 03 92		
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR 857.8150.01 ED
				ZU GERAET NRVD			REG.I.V. 857.8008 BLATT 2 BLATTZAHL 11

DIESE ZEICHNUNG IST EIN RECHNERAUSDRUCK. AENDERUNGEN NUR DURCH AENDERN DES DATENSATZES ERFOLGEN
FUER DIESE ZEICHNUNG BEHALTEN WIR UNS ALLE RECHTE VOR.

FUER DIESE ZEICHNUNG BEHALTEN WIR UNS ALLE RECHTE VOR.
DIESE ZEICHNUNG IST EIN RECHNERAUSDRUCK. AENDERUNGEN AN IHR NUR DURCH AENDERN DES DATENSATZES ERLAUBT



DARSTELLUNG SEITE A
VIEW ON SIDE A

09/00	47627	01.97	RG	GEZ.	TAG	NAME	BENENNUNG: ANALOGPLATTE / ANALOGBOARD — Z
				BEARB.			
				GEPR.			
				NORM.			
				PLOTT	18.03.97		ZEICHN.-NR. 857.8150.01 ED — BLATT-NR. 2-
BLOCK IND	BENENNUNG AENDERUNG	DATUM	NAME				ERSATZ F. 857.8008 — ERSETZT 857.8008

ROHDE&SCHWARZ

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Part lists

Circuit diagrams

Component plans

7 Checking and Repair of Display Board A3

7.1 Function Description

(see circuit diagram 857.8108.01S)

The display board A3 contains an LCD panel, 20 operating keys as well as LEDs for display of the current setting. In addition to these functions, the associated control and evaluation circuits are also accommodated on the board.

7.1.1 Liquid Cristal Display

The LCD panel H1 is a device-specific display designed in super-twisted-nematic technology, featuring a high contrast and a wide viewing angle. Four LCD controllers D1 to D4 control the LCD with 4 x 128 display segments in 4-fold multiplex operation. For this purpose, a voltage supply in 4 stages is provided.

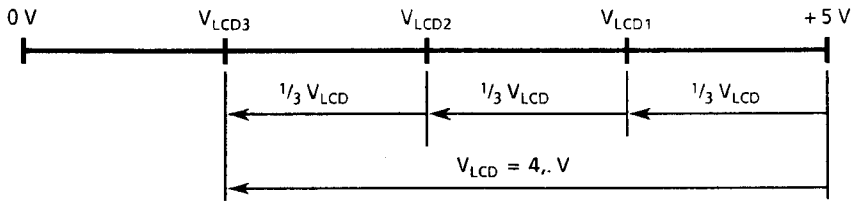


Fig. 7-1 LCD voltage supply

The optimum operating voltage V_{LCD} is fed in via amplifier N1-A, set using R24 and changed according to the temperature with approx. -14 mV/K via V3. The LCD drivers D1 to D4 are synchronously driven using a 125-kHz clock from key controller D5. After switching on the instrument, the reset status necessary for proper functioning of the LCD drivers is obtained with a stable clock signal via program control at port line PO12 (X1.6) from the computer board.

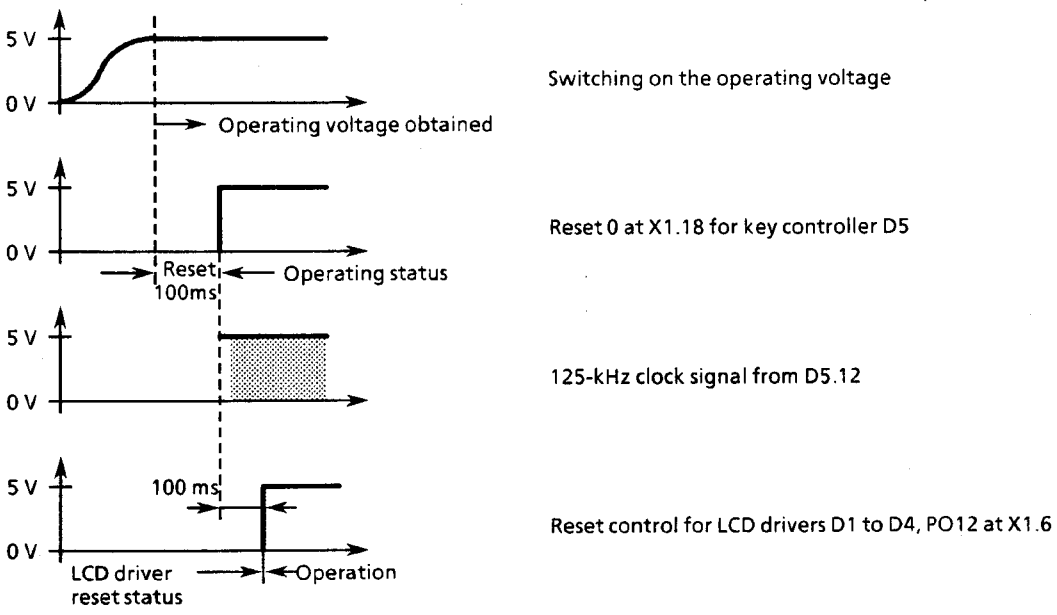


Fig. 7-2 Timing of reset control

The display data are transferred byte by byte via the serial interface X1.20 (SI = Serial Input) and X1.19 (SCK = Serial Clock). Control line X1.17 (C/D = Command/Display) is used to differentiate between command and display bytes. Chip select lines X1.24/21/26/22 (CS 1 to 4) are used for selection of an LCD driver for data transfer. Each time a byte has been transferred, the BUSY line (X1.23) is set to logic 0 = 0 V as the common output of all drivers and permits time-optimized data transfer as an acknowledgement signal.

Basic time diagrams for data transfer:

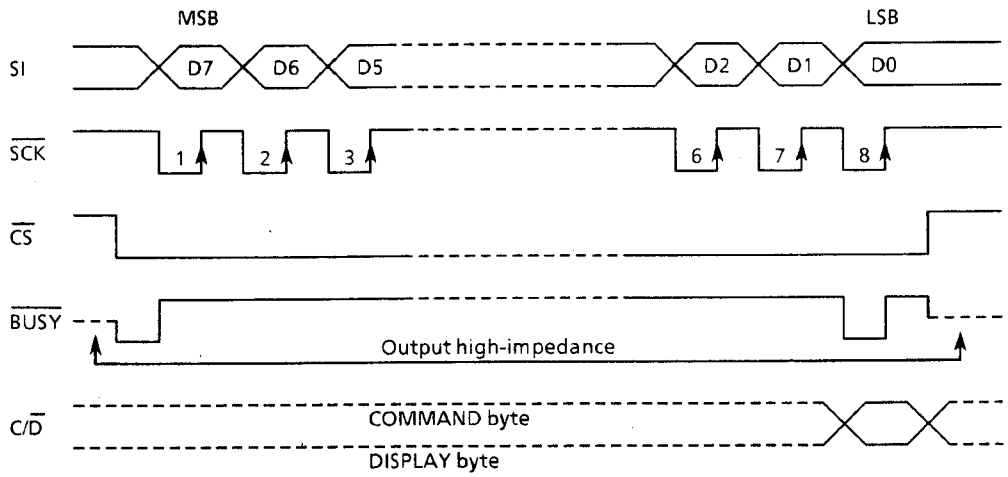


Fig. 7-3 Signal characteristic for one data byte

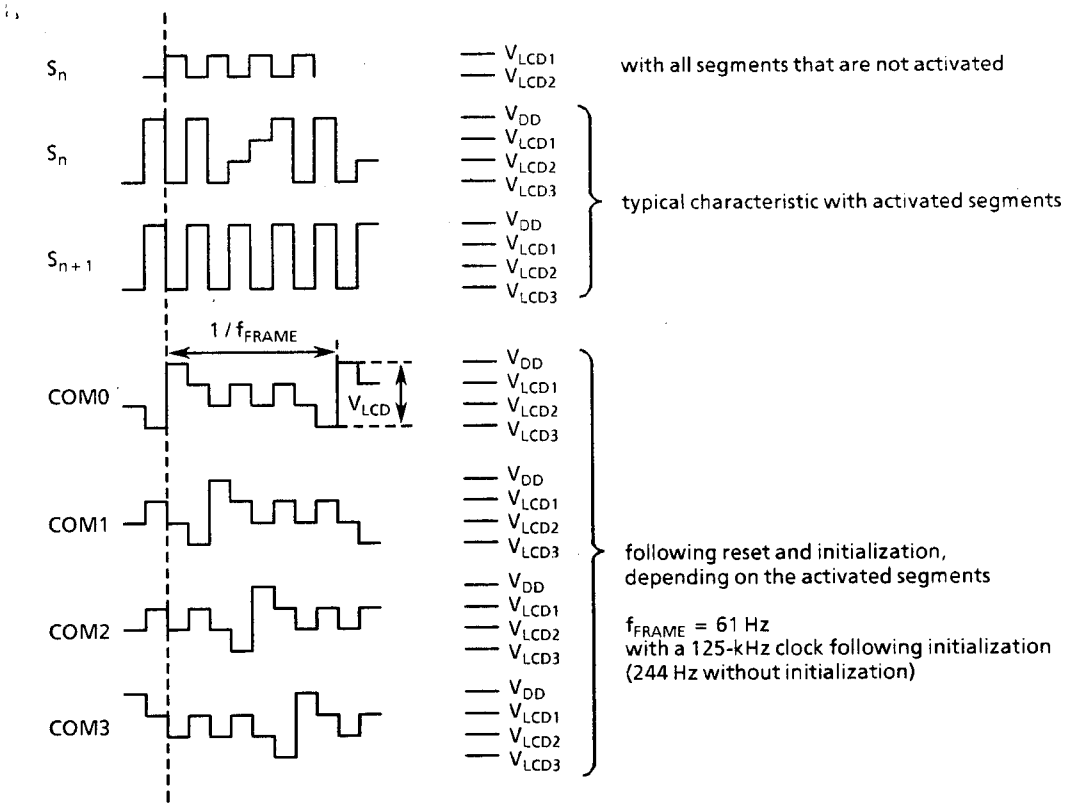
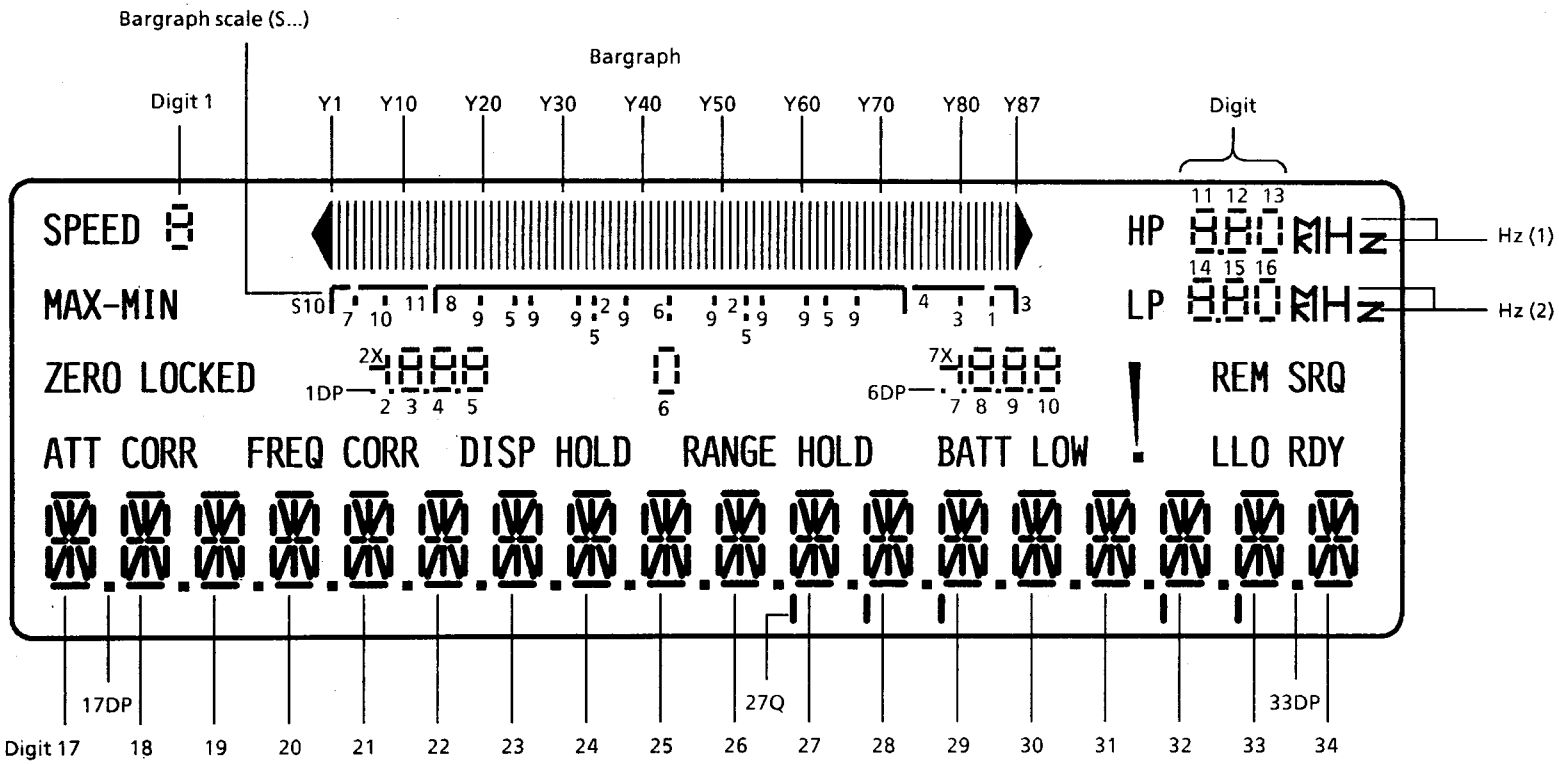
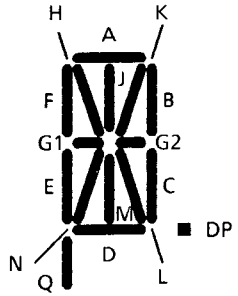


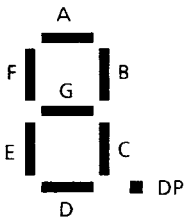
Fig. 7-4 Basic signal characteristic at LCD drivers and display



14-segment digit:



7-segment digit:



Unit:

MHz
kHz

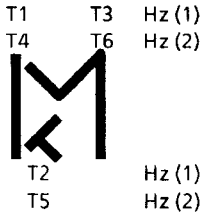


Fig. 7-5 LCD panel

Contact and segment assignment of LCD display H1 and LCD drivers:

Units	7-segment digit no.							Messages		
	11	12	2	3	4	5	1			
Hz (1)	F A	F A	X	F A	F A	F A	F A	–	SPEED	COM 0
T3	G B	G B	B, C	G B	G B	G B	G B	MIN	MAX	COM 1
T1	E C	E C	1DP	E C	E C	E C	E C	LOCKED	ZERO	COM 2
T2	D DP	D 13 A...F	2DP	D DP	D DP	D DISP HOLD	D	FREQ CORR	ATT CORR	COM 3

H1.	99	103	102	101	100	161	162	163	164	165	166	167	169	168	170	171
D1.	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36

14-segment digit no.				
20	19	18	17	
B K H A	B K H A	B K H A	B K H A	COM 0
G2 J G1 F	G2 J G1 F	G2 J G1 F	G2 J G1 F	COM 1
C L N E	C L N E	C L N E	C L N E	COM 2
DP M D	DP M D	DP M D	DP M D	COM 3

H1.	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5
D1.	35	34	32	31	30	29	28	27	26	25	24	23	22	21	20	19

14-segment digit no.				
28	27	26	25	
B K H A	B K H A	B K H A	B K H A	COM 0
G2 J G1 F	G2 J G1 F	G2 J G1 F	G2 J G1 F	COM 1
C L N E	C L N E	C L N E	C L N E	COM 2
DP M D Q	DP M D Q	DP M D	DP M D	COM 3

H1.	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41
D2.	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36

14-segment digit no.				
24	23	22	21	
B K H A	B K H A	B K H A	B K H A	COM 0
G2 J G1 F	G2 J G1 F	G2 J G1 F	G2 J G1 F	COM 1
C L N E	C L N E	C L N E	C L N E	COM 2
DP M D	DP M D	DP M D	DP M D	COM 3

H1.	40	39	38	37	32	31	30	29	28	27	26	25	24	23	22	21
D2.	35	34	32	31	30	29	28	27	26	25	24	23	22	21	20	19

7-segment digit no.				Bargraph scale S...			
7	8	9	10	6			
X	F A	F A	F A	S1	S7	S10	COM 0
B, C	G B	G B	G B	S2	S5	S9	COM 1
6DP	E C	E C	E C	6 A...F	S6	S11	COM 2
7DP	D DP	D DP	D	S3	S4	S8	COM 3

H1.	106	107	108	109	110	111	112	113	114	160
D3.	51	50	49	48	47	46	45	44	43	19

Bargraph Y1 to Y87																						
87	80	79	72	71	64	63	56	55	48	47	40	39	32	31	24	23	16	15	8	7		COM 0
86	81	78	73	70	65	62	57	54	49	46	41	38	33	30	25	22	17	14	9	6	1	COM 1
85	82	77	74	69	66	61	58	53	50	45	42	37	34	29	26	21	18	13	10	5	2	COM 2
84	83	76	75	68	67	60	59	52	51	44	43	36	35	28	27	20	19	12	11	4	3	COM 3

H1.	115	116	117	119	120	123	124	128	129	133	134	138	139	143	144	147	148	150	151	152	153	154
D3.	42	41	40	39	38	37	36	35	34	32	31	30	29	28	27	26	25	24	23	22	21	20

Message	7-segment digit no.				Units, messages			14-segment digit no.				
	14		15					22				
	F	A	F	A	Hz (2)	LP	HP	B	K	H	A	COM 0
	G	B	G	B	T6	!	REM	G2	J	G1	F	COM 1
	E	C	E	C	T4	BATT LOW	LLO	C	L	N	E	COM 2
SRQ	D	DP	D	16 A...F	T5	RANGE HOLD	RDY		M	D		COM 3

H1.	81	82	83	84	85	94	105	104	80	79	78	77
D4.	51	50	49	48	47	46	45	44	43	42	41	40

14-segment digit no.																				
33				32				31				30				29				
B	K	H	A	B	K	H	A	B	K	H	A	B	K	H	A	B	K	H	A	COM 0
G2	J	G1	F	G2	J	G1	F	G2	J	G1	F	G2	J	G1	F	G2	J	G1	F	COM 1
C	L	N	E	C	L	N	E	C	L	N	E	C	L	N	E	C	L	N	E	COM 2
DP	M	D	Q	DP	M	D	Q	DP	M	D		DP	M	D		DP	M	D	Q	COM 3

H1.	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57
D4.	39	38	37	36	35	34	32	31	30	29	28	27	26	25	24	23	22	21	20	19

7.1.2 LCD Backlighting

The light bulbs E1 to E4 for the LCD illumination are operated with a DC voltage of 0.7 to 5 V. With the instrument set appropriately, the brightness can continuously be varied via microprocessor control (→ A1 computer board).

7.1.2.1 Operating State Indication

Additional information on the current test channel, on/off state of the test generator and state of the keyboard which has a double key assignment (Data with digital input) is indicated optically via LEDs H2 to H5. The LEDs are addressed via latch D6. The necessary data are provided via data bus D<3...0>*, addressing is effected via lines $\overline{PCS3}$, A2* and is evident from table 7-1.

Table 7-1 Addressing of the LEDs at the front panel

Log. state of the line			Function
A2* X1.28	$\overline{PCS3}$ X1.15	$\overline{CS}$ D5.9	
L	L	L	Keyboard entry (via D5-KEYINT)
H	L	H	Data at the data bus D<3....0>* are accepted in D6 with the positive edge -WR* (X1.2) (log. state "L" switches on H2 to H5)
L	H	H	No response
H	H	H	No response

7.1.3 Key Decoding

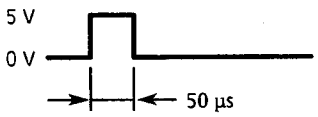
The operating keys S1 to S19 are directly connected with key controller D5 in a field of 4 row and 6 column lines. By pressing a key, a connection between a row and a column is produced. Keyboard enquiry is effected with the R&S-specific device KEYINT according to a new static method, which dispenses with keyboard scanning even upon key actuation.

The row lines R0 to R7 and column lines C0 to C7 of D5 are equipped with bidirectional drivers. This permits to clearly identify a pressed key in two steps (bidirectional transmission).

When no keys are pressed in the idle state, the column drivers are actively switched to 0, the row lines as the receivers are applied to 1 via pull-up resistors. When a key is pressed, the row line involved is applied to logic 0 via the contact by the respective column driver. Following internal debouncing, the control enters the code of the row information into the keyboard register. Then, the column drivers are switched off (tristate) and the row drivers then switched on (row drivers to logic 1). The row lines now operate as transmitters, the columns as receivers (reply mode).

The column inputs provide a 1 on the activated column and a 0 on all other ones. Thus, the column information is also available to be entered into the keyboard register. Then the idle state is resumed again. Finally an interrupt is set, reporting to the processor via line INT1 that a key information is available.

Interrupt signal after pressing a key:
at D5.11, X1.8



The processor reads the 8-bit key information at address 0 via data bus D0 to D7 and acknowledges the interrupt by writing a 0 to address 0; the interrupt is thus reset.

Keyboard controller D5 is reset via the reset line at X1.18 after switching on the instrument. The internal clock oscillator with ceramic resonator B1 then operates at 250 kHz. D5 internally operates at 125 kHz. This clock is also available at output D5.12 for controlling the LCD drivers (→ diagrams in section 7.1.1).

7.2 Measuring Instruments and Auxiliary Equipment

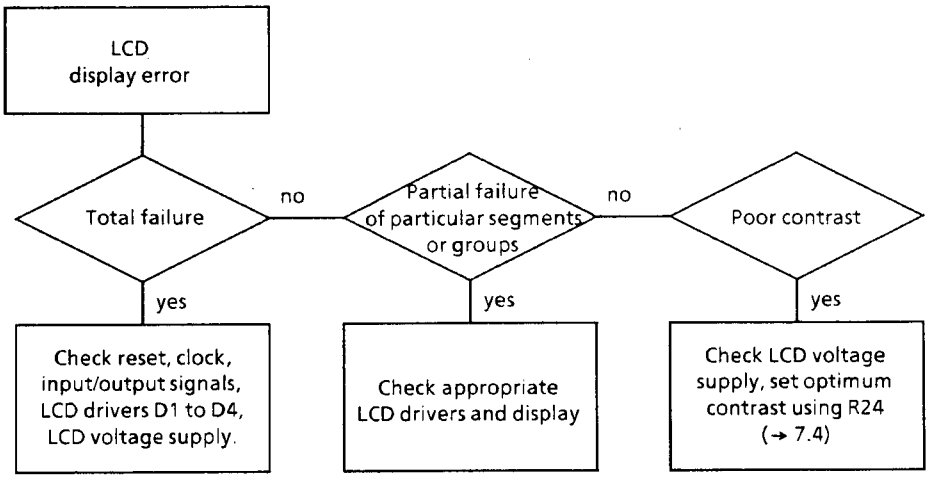
Item	Type of instrument	Required characteristics	Appropriate R&S instrument	Order No.
1	Digital voltmeter	DC, 0 to 10 V ±0.25 %	URE3	350.5315.03
2	Oscilloscope	DC to 10 MHz, 2 channels	BOL	374.2000.02
3	Frequency counter	50 Hz to 1 MHz, ±0.1 %	URE3	350.5315.03

7.3 Troubleshooting

For troubleshooting, use the auxiliary routines in the instrument and the following flow charts. Exact fault location is then possible using the circuit diagram.

7.3.1 LCD Faulty

Call up LCD test routine via the SPEC key. All LCD segments must be displayed → compare with Fig. 7-5.



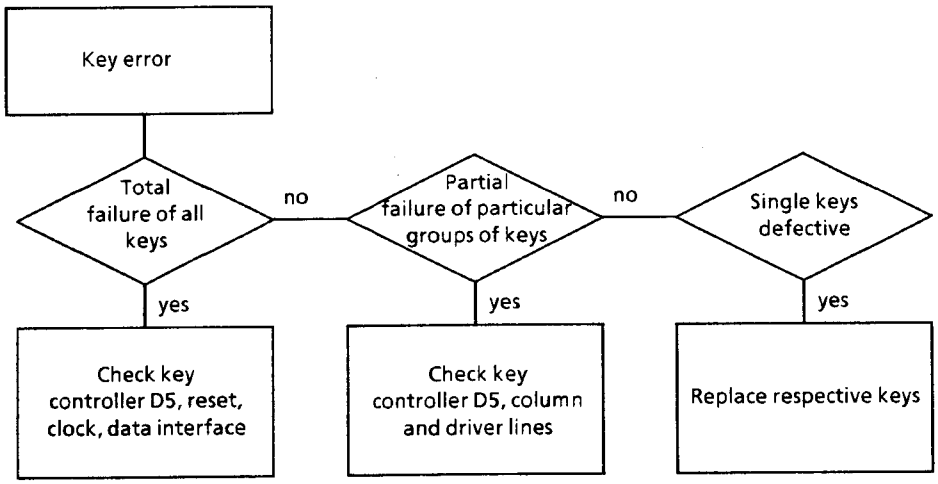
7.3.2 Keyboard Faulty

Call up test routine for keys via

"SPEC" + menu keys "mre + mre + FRONTPANEL + CHECK + KEY".

Press the keys one after the other; each time a key is pressed, a reading corresponding to the inscription must be shown on the display. The test routine can be abandoned by pressing the MEAS key twice.

Start troubleshooting in the analog board, in the case of a total failure of the keys also check the computer board.

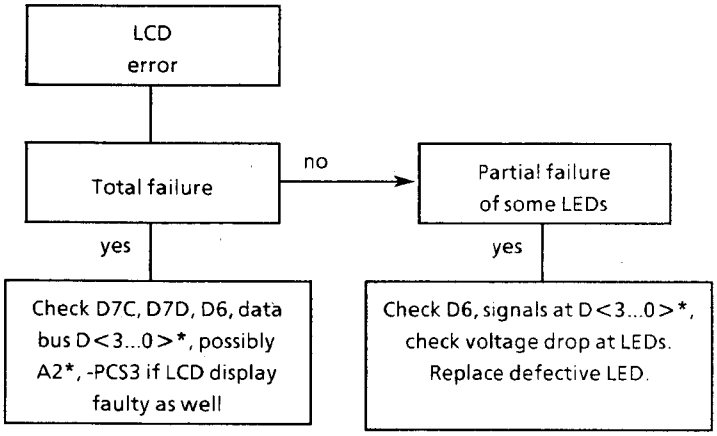


7.3.3 Error of the State Indication

Call the LED test routine via

"SPEC" + menu keys "mre + mre + FRONTPANEL + CHECK + LCD/LED"

All four LEDs must light up. If otherwise, locate error according to the following troubleshooting flowchart.



7.3.4 LCD Illumination Faulty

- Check voltage at X76 of computer board A1:
  rated value + 0.7 to 5 V depending on brightness setting
- Continue troubleshooting in A1 board
- Replace light bulb according to section 7.5.1, 7.5.2

7.4 Checking and Adjustment

7.4.1 Checking the Supply Voltages

Test point - Reference			Voltage	Tolerance	Remark
X2	-	X3	0.7 to 5 V	----	Depending on backlighting
X1.31 X1.32	-	X1.29 X1.33 X1.34	5 V	±0.15 V	
X1.31	-	N1.1	4.3 V typ.	±0.2 V typ.	Depending on contrast setting and temperature
N1.1	-	X1.29	0.7 V typ.	----	
D4.4	-	X1.29	2.13 V typ.	----	
D4.3	-	X1.29	3.57 V typ.	----	
D1.4	-	X1.29	2.13 V typ.	----	
D1.3	-	X1.29	3.57 V typ.	----	

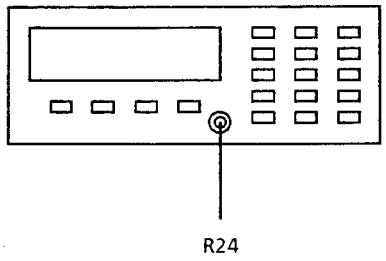
7.4.2 Checking the Clock Frequency for Key Controller and LCD Drivers

Measure the clock frequency by applying a frequency counter or oscilloscope to D5.12 via probe tip. The clock frequency at the output of the key controller must be 125 kHz ± 0.5 %.

Note: A missing clock in the normal operating state of the LCD drivers may cause damage to the LCD.

7.4.3 Setting the LCD Contrast

The contrast of the liquid crystal display can be varied using R24. For this purpose, remove the labelling strip (see also exploded view). R24 can be adjusted via the opening in the base plate.



To ensure an optimum setting, lift the instrument on the front feet so that you can look at the display at an angle slightly from below.

Further presetting on the instrument:

- Select analog display (keys, DISP, BARGRAPH-VOL)
- Maintain the display value (key MEAS→REF)

Use R24 to set the optimum visual contrast; make sure that ***only*** the currently activated segments are displayed. All others must remain invisible.

7.5 Dismantling and Reassembly

7.5.1 Removal and Replacement of the Display Board

See also exploded view.

Removal:

- Remove the 2 rear-panel feet and the upper instrument cover (item 17 + 18, 4 screws and item 1).
- Remove the labelling strip (item 45, 4 screws with washers, item 46 + 47).
- Swivel out the display board A3 together with the front mounting panel (item 50, item 48).
- Withdraw ribbon cable W1 from plug X40 of the computer board.
- Take the cable socket through the opening of the metal frame.
- Remove front mounting panel (item 48, 4 screws item 49).

> ***Only remove the screws marked by hatching; the other screws fasten the key switching panel (→ 7.5.3).***

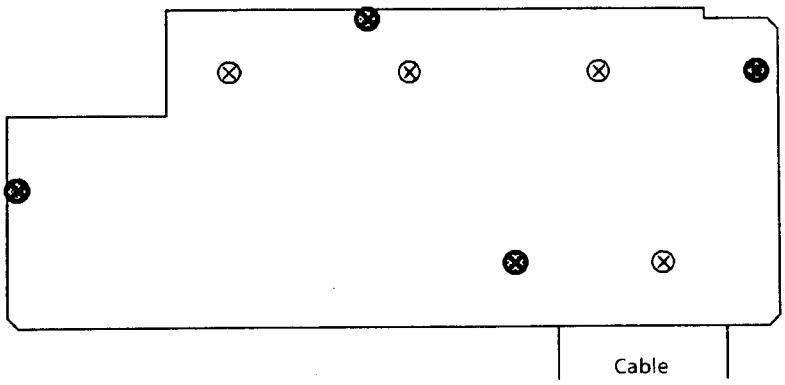


Fig. 7-6 Display board with fixing screws

- For troubleshooting, it is recommended to reconnect the completely removed display board to the computer board via the cable socket.

Replacement:

The procedure for reassembling has to be carried out in the reverse order to that of dismantling.

7.5.2 Removal and Replacement of LCD and Light Bulbs

- Put the display board with the LCD pointing downwards to a clean and flat surface.
- Bend the 8 bender strips of the metal frame straight.
- Hold the metal frame and pull the display board out of the bender strips - the LCD with the metal frame, lighting unit and the conductive rubber strips remains a complete unit.
- Leave this unit like this if only the light bulbs are to be replaced.
- Dismantle the LCD unit if the display is to be replaced.

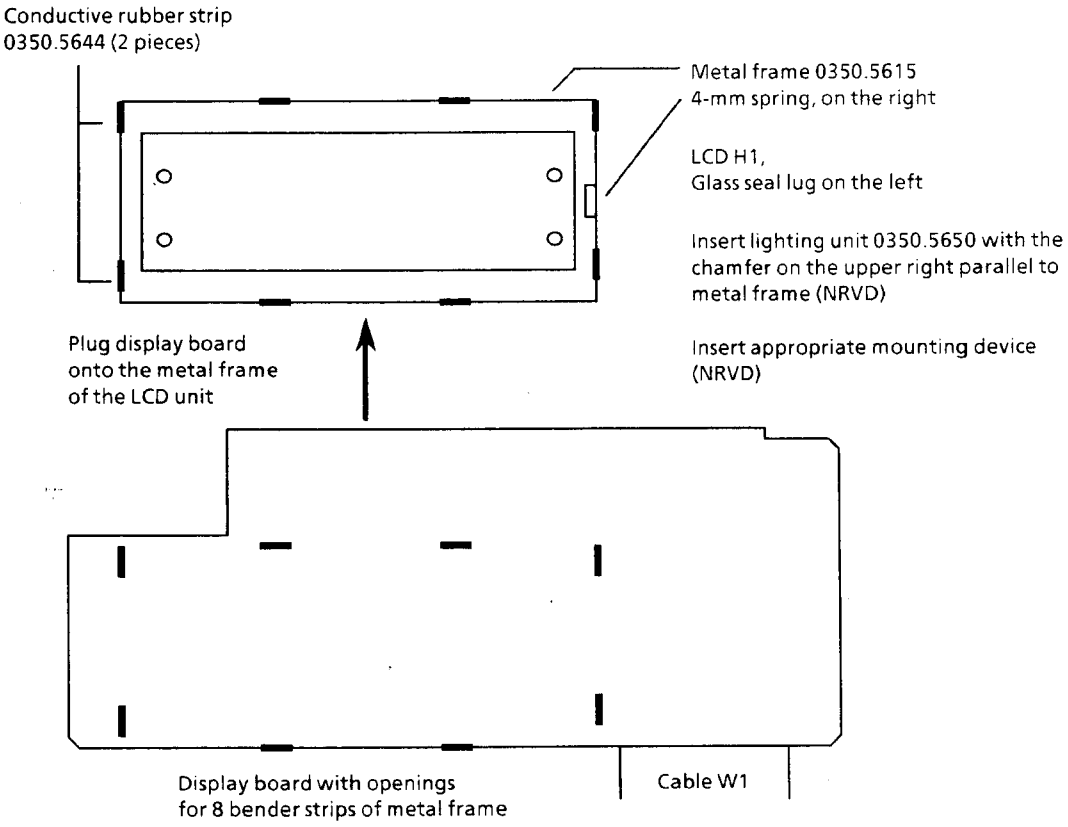


Fig. 7-7 Installation of LCD

- Solder in light bulbs E1 to E4 with a maximum mounting height of 6.8 mm.
- Put the metal frame to a flat surface with the bender strips pointing to the top and the springs to the right!
- Insert LCD, glass seal lug on the left, in the case of a new display attach 2 plastic labels with stock number 0350.57909 on the side.
- Insert the lighting unit with the chamfer on the upper right and the conductive rubber strip, making sure that they are free from dust.
- Replace the display board, making sure that the light bulbs fit exactly into the openings of the lighting unit.
- Firmly press the display board against the frame and traverse the 8 bender strips by approx. 15 degrees.

7.5.3 Removal and Replacement of Keytops and Key Switching Panel

Replacing the keytops:

The keytops can be removed and replaced without removing the display board.

The following parts are required:

- for S1 to S12, S18, S19, colour light-grey (17 pieces), stock no. SB 0396.0116
- for S13 to S17, colour dark-grey (5 pieces), stock no. 0396.0039

Removing the key switching panel:

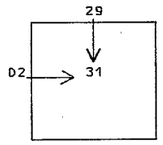
- Remove screws according to Fig. 7-6 in 7.5.1
- Remove key switching panels with pressure panel.

Replace the parts, making sure that they are free from dust, and tighten the 4 fixing screws with a torque of 0.1 to 0.2 Nm and lock them using screw locking varnish WV 0087.5818.

7.6 Interfaces

Pin	Name	Input/ Output	Origin/destination	Value range	Signal description	
X1.31 X1.32	+ 5 V	Input	A1, Computer, X40.AB16	4.75 to 5.25 V	Supply voltage	
X1.29 X1.33 X1.34	GND	Input	A1, Computer, X40.AB17 X40.B16	0 V	Ground (casing potential)	
X1.18	RESET0*	Inp./Outp.	A1, Computer, X40.A99	0.7 to 4.5 V	Reset for key controller D5	
X1.6	PO12	Input	A1, Computer, X40.A3	HCMOS level	Reset for DCD drivers	
X1.27 X1.30	LCD-ILLUM	Input	A1, Computer, X40.A16 X40.B14	0.7 to 5 V	LCD illumination (only URE3) variable brightness	
X1.28	A2*	Input	A1, Computer, X40.A14	0/5 V ± 5 %	Adress 2	
X1.8	INT1	Output	A1, Computer, X40.A4	┐	Interrupt	┐
X1.3	A0	Input	A1, Computer, X40.B2	Inputs: L = 0 to 0.8 V	Address 0	Control lines for key controller D5
X1.4	A1	Input	A1, Computer, X40.A2	H = 2 to 5 V	Address 1	
X1.1	RD*	Inp./Outp.	A1, Computer, X40.B1	Outputs: L = 0 to 0.4 V	Read	
X1.2	WR*	Inp./Outp.	A1, Computer, X40.A1	H = 4.6 V min.	Write	
X1.15	PCS3	Input	A1, Computer, X40.B8	┘	Chip select	┘
X1.16	D0*	Inp./Outp.	A1, Computer, X40.A8	┐	┐	
X1.13	D1*	Inp./Outp.	A1, Computer, X40.B7			
X1.14	D2*	Inp./Outp.	A1, Computer, X40.A7	Inputs: L = 0 to 0.8 V	Data bus for key controller D5	
X1.11	D3*	Inp./Outp.	A1, Computer, X40.B6	H = 2 to 5 V		
X1.12	D4*	Inp./Outp.	A1, Computer, X40.A6	Outputs: L = 0 to 0.4 V		
X1.9	D5*	Inp./Outp.	A1, Computer, X40.B5	H = 4.6 V min.		
X1.10	D6*	Inp./Outp.	A1, Computer, X40.A6			
X1.7	D7*	Inp./Outp.	A1, Computer, X40.B4	┘	┘	
X1.24	CS1	Input	A1, Computer, X40.A12	┐	┐	
X1.21	CS2	Input	A1, Computer, X40.B11		Chip select for LCD drivers D1 to D4	
X1.26	CS3	Input	A1, Computer, X40.A13			
X1.22	CS4	Input	A1, Computer, X40.A11	┘	┘	
X1.19	SCK	Input	A1, Computer, X40.B10	CMOS level	Serial clock	┐
X1.23	BUSY	Output	A1, Computer, X40.B12		Feedback	Control lines of 4 LCD drivers
X1.17	C/D	Input	A1, Computer, X40.B9		Command/Data	
X1.20	SI	Input	A1, Computer, X40.A10	┘	Serial input	┘

BEISPIEL:
EXAMPLE:



BEDEUTUNG: H1.31 - D2.29
SIGNIFICANCE: H1.31 - D2.29

VERBINDUNGSLISTE LCD H1 - TREIBER D1...D4 LIST OF CONNECTIONS LCD H1 - DRIVERS D1...D4

PINS D1...D4		19	20	21	22	23	24	25	26	27	28	29	30	31	32	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
H1 - P I N S	ZU D1	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	171	170	168	169	167	166	165	164	163	162	161	100	101	102	103	99
	ZU D2	21	22	23	24	25	26	27	28	29	30	31	32	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	ZU D3	160	154	153	152	151	150	148	147	144	143	139	138	134	133	129	128	124	123	120	119	117	116	115	114	113	112	111	110	109	108	107	106
	ZU D4	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	104	105	94	85	84	83	82	81

SIEHE ANSCHLUSSLISTE COMMONLEITUNGEN
SEE LIST OF CONNECTIONS FOR COMMON LINES

FUER DIESE UNTERLAGE BEHALTEN WIR UNS ALLE RECHTE VOR

ZEICHN.-NR.

CIRCUIT DIA

NDUNGSLISTE LCD H1 - TREIBER D1...D4 LIST OF CONNECTIONS LCD H1 - DRIVERS D1...D4

28	29	30	31	32	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
14	15	16	17	18	19	20	171	170	168	169	167	166	165	164	163	162	161	100	101	102	103	99
30	31	32	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
143	139	138	134	133	129	128	124	123	120	119	117	116	115	114	113	112	111	110	109	108	107	106
66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	104	105	94	85	84	83	82	81

SIEHE ANSCHLUSSLISTE COMMONLEITUNGEN

SEE LIST OF CONNECTIONS FOR COMMON LINES

H1

D2-A UPD7225G-00 L

D3-A UPD7225G-00 L

D4-A UPD7225G-00 L

+5V

R17 47K5 L, C5 1N L, R18 47K5 L, C6 1N L, R19 47K5 L, R23 47K5 L, R24 5K, R25 5K62 L, C8 100N L, V3 BC550, R22 22K1 L, C7 100N L, V_LCD ADJUST, N1-A CA3240AE, R21 100K L, R20 681K L, N1-B CA3240AE

R14 47K5 L, C3 1N L, R15 47K5 L, C4 1N L, R16 47K5 L

R3 27K4, R4 27K4, R5 27K4, R6 27K4 L, R7 27K4 L, R8 27K4 L, R9 27K4 L, R10 27K4 L, R11 27K4 L, R12 27K4 L

S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16 S17 S19 S18

C1 220P, R28 100K L, B1 250KHZ, C2 470P

DS KEYINT

TASTEN KEYS

CHANEL 7	W ⟷ DBM 8	ZERO 9
MODE 4	UNIT 5	RANGE 6
MEAS →REF 1	REF 2	DISP 3
FILTER 0	FREQ .	SPEC +/-
MENU		
1	2	3	4
→MEAS		SETUP CLR	LOCAL/ TALK EXP

ANSCHLUSSLISTE COMMONLEITUNGEN

FOR COMMON LINES
LIST OF CONNECTIONS

	C0	C1	C2	C3
PINS D4	15	16	17	18
PINS H1	1	2	3	4
	89	88	87	86
	93	92	91	90
	98	97	96	95
	155	156	157	158
	172	173	159	174
	175	176	177	178

ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.

ATTENTION: ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING.

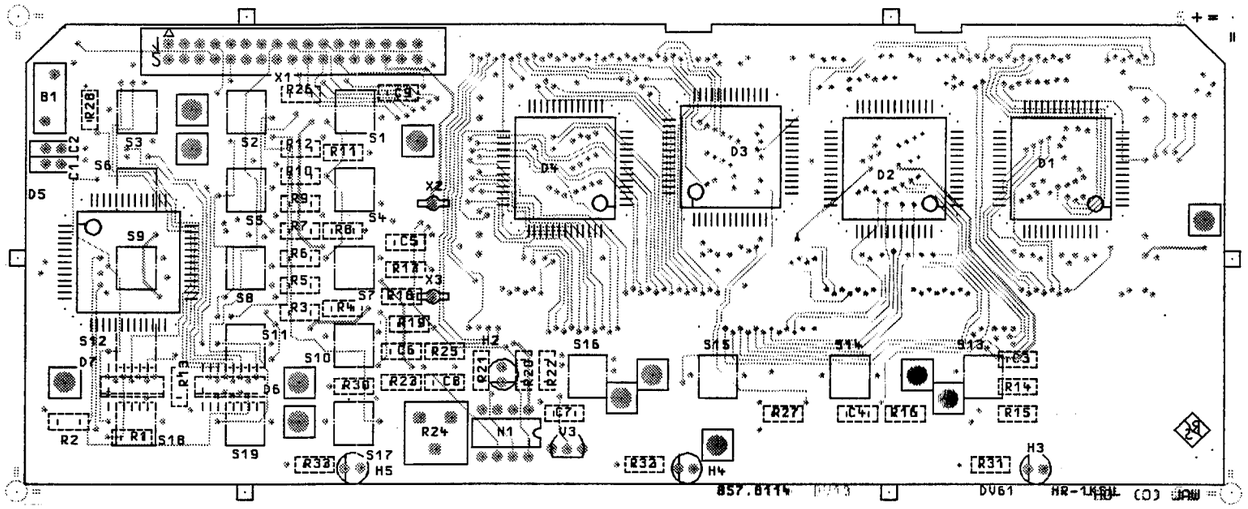
CIRCUIT DIAGRAM IS VALID FOR MOD.02

STROMLAUF GILT FUER VAR.02

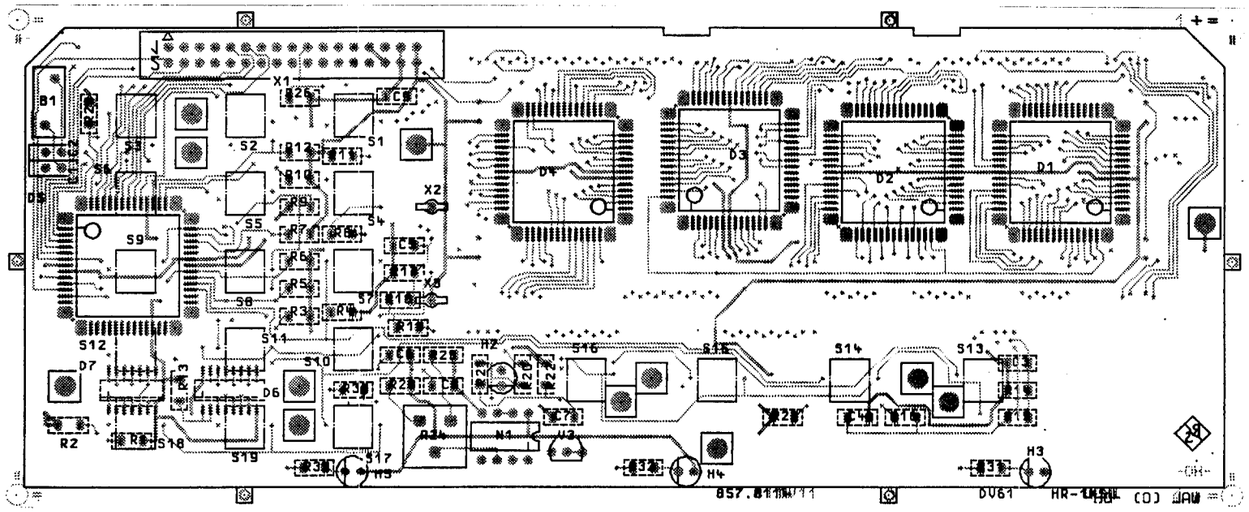
				1KGU	TAG	NAME	BENENNUNG
				BEARB.		MK	ANZEIGEPLATTE
				GEPR.		MK	DISPLAY BOARD
				NORM			
				PLOTT	15. 6.90	WAL	
AEND. IND.	AENDERUNGS MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN. NR. 857.8108.01S
				ZU GERAET NRVD			REG.I.V. 857.8008 ERSTE Z.

BLATT-NR. 1 V. 1 BL.

Ansicht und Leitungsfuehrung Loetseite
View of tracks on solder side



DV13

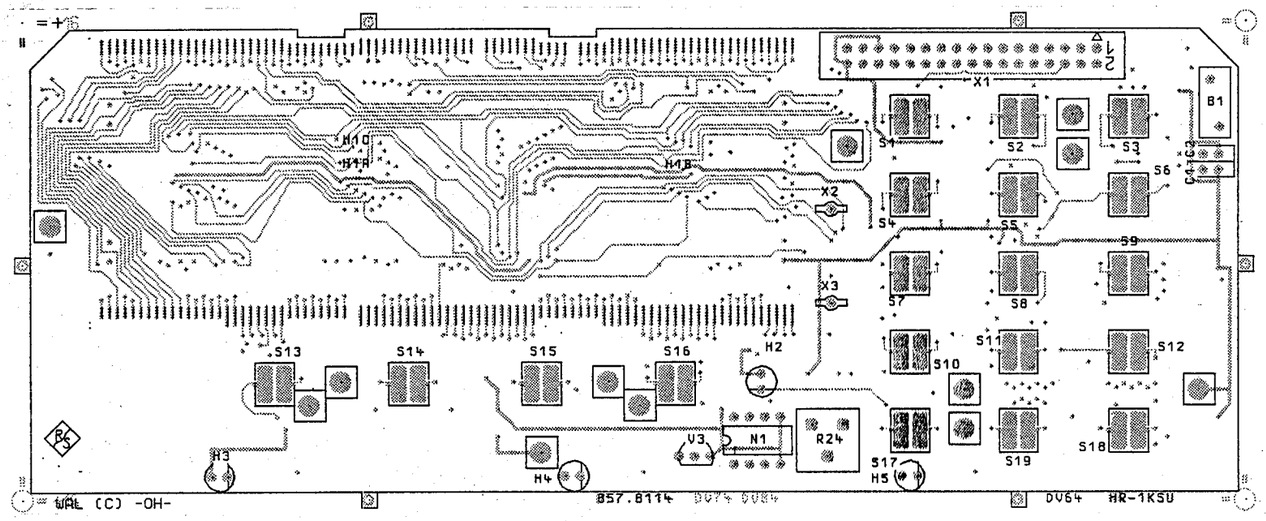


DV11

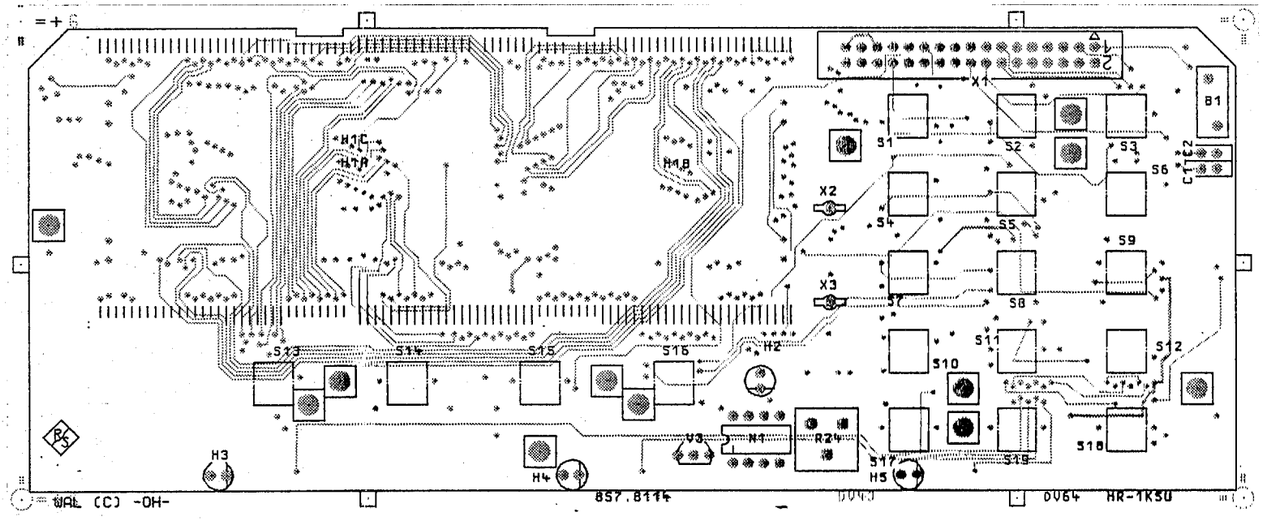
				Maße ohne Toleranzangabe		Maßstab 1 : 1	
						Halbzeug, Werkstoff	
				1KGU	Tag / Name	Benennung ANZEIGEPLATTE	Z
				Bearb.	06.90 MK		
				Gepr.			
				Norm			
And. Zust.	Anderungs-Mitteilung	Tag	Name	ROHDE&SCHWARZ		Zeichn.-Nr. 857.8108	Blatt-Nr. 3 v. 4 Bl.
				zu Gerat NRVD		reg. i. V 857.8008 V	erste Z.

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Ansicht und Leitungsfuehrung Bauteilseite
View of tracks on component side



DV41



DV43

				Maße ohne Toleranzangabe		Maßstab 1 : 1	
						Halbzeug, Werkstoff	
				1KGU	Tag	Name	Benennung ANZEIGEPLATTE Z
				Bearb.	06.90	MK	
				Gepr.			
				Norm			
				ROHDE & SCHWARZ			Zeichn.-Nr. 857.8108 Blatt-Nr. 4 v. 4 Bl.
Änd. Zust.	Änderungs-Mitteilung	Tag	Name	zu Gerät NRVD		reg. i. V. 857.8008 V	erste Z.

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ISO-Projektion Methode E

ROHDE&SCHWARZ

SERVICE INSTRUCTIONS

Filter Board

857.8308.02

Contents

		Page
7	**Testing and Repair of the Module A4 Filter Board**	7.1
7.1	**Function Description of the Board**	7.1
7.2	**Test Instruments and Utilities**	7.1
7.3	**Troubleshooting**	7.1
7.4	**Removal and Assembly**	7.2
7.4.1	Removal of the Module A4, Filter Board	7.2
7.4.1.1	Filter Board on the Front Panel	7.2
7.4.1.2	Filter Board on the Rear Panel	7.2
7.4.1.3	Removal of the Board	7.2
7.5	**Interfaces**	7.3

Part lists

Circuit diagrams

Component plans

7 Testing and Repair of the Module A4 Filter Board

7.1 Function Description of the Board

(circuit diagram 857.8308.01)

The filter board is the input interface of the NRVD. The two input sockets X1, X2 are provided for reception of the measuring heads, separately for test channel A and B. The filter board is connected to the front panel of the NRVD at minimum RF leakage, the electrical connection to the analog board is realized via the plug-in flat cable W4. The signal lines from the two input sockets X1, X2 on the filter board to the interface X3 (connection of cable W4 to the analog board) are provided with a lowpass filter for suppression of RF interferences. Thus, RF interferences, which might occur at the test site, hardly influence the test results. Due to the relativly small bandwidth of the test signal and high impedances, RC lowpass filters have been used for the test-signal connections X1.2, X1.3 and X1.4. LC filters have been used for the digital signal lines X1.8 (DATP1) and X1.7 (CLKP1). The temperature-measuring line X1.6 and the voltage supply (X1.11) are also provided with LC lowpass filters. The lines of channel B are filtered identically.

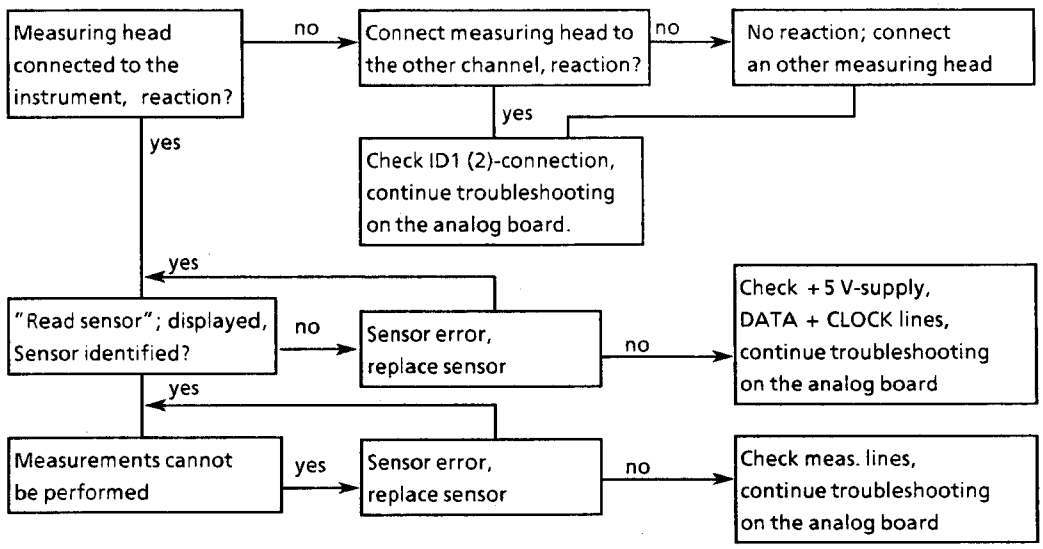
The board does not contain any adjustable components, which is why no adjustment is required.

For rack-mounting, the board can also be fitted to the rear panel of the NRVD instead of the front panel (cf. Section 7.5, Assembly).

7.2 Test Instruments and Utilities

Item	Type of instrument	Required specifications	Suitable R&S instrument	Order No.	Application
1	Ohmmeter	Ω: 0 to 10 MΩ	UDS 5	349.1510.02	7.3

7.3 Troubleshooting



The filter board does not accomodate any active components; therefore, a test of the connections (ohmmeter) acc. to the circuit diagram or interface description is sufficient. The troubleshooting diagram can be used analogously.

7.4 Removal and Assembly

7.4.1 Removal of the Module A4, Filter Board

- Remove the two rear-panel feet upon loosening the four Phillips screws and withdraw the lower housing shell to the rear (be careful not to damage the RF screening strips on the rear panel).

7.4.1.1 Filter Board on the Front Panel

- Remove four fixing screws on the cover of the front panel and remove the front panel.
- Loosen the cable W4 from the support at the analog board and disconnect from X101.
- Remove three screws fixing the filter board and take off the filter board with the two sockets for connecting the sensor and the cable W4 to the rear.

7.4.1.2 Filter Board on the Rear Panel

- Loosen the cable W4 at the analog board from its support and disconnect from X101.
- Remove three Phillips screws fixing the filter board and take out the filter board with the two sockets and the cable W4 facing to the front panel.

7.4.1.3 Removal of the Board

Undo the fixing screws of the screening cover at the removed filter board and withdraw the filter board from the housing and the two input sockets (be careful not to damge the earthing spring).

Installation:

- Reassemble the pieces in the reverse order, fix the cover to the position which is not occupied on the filter board.

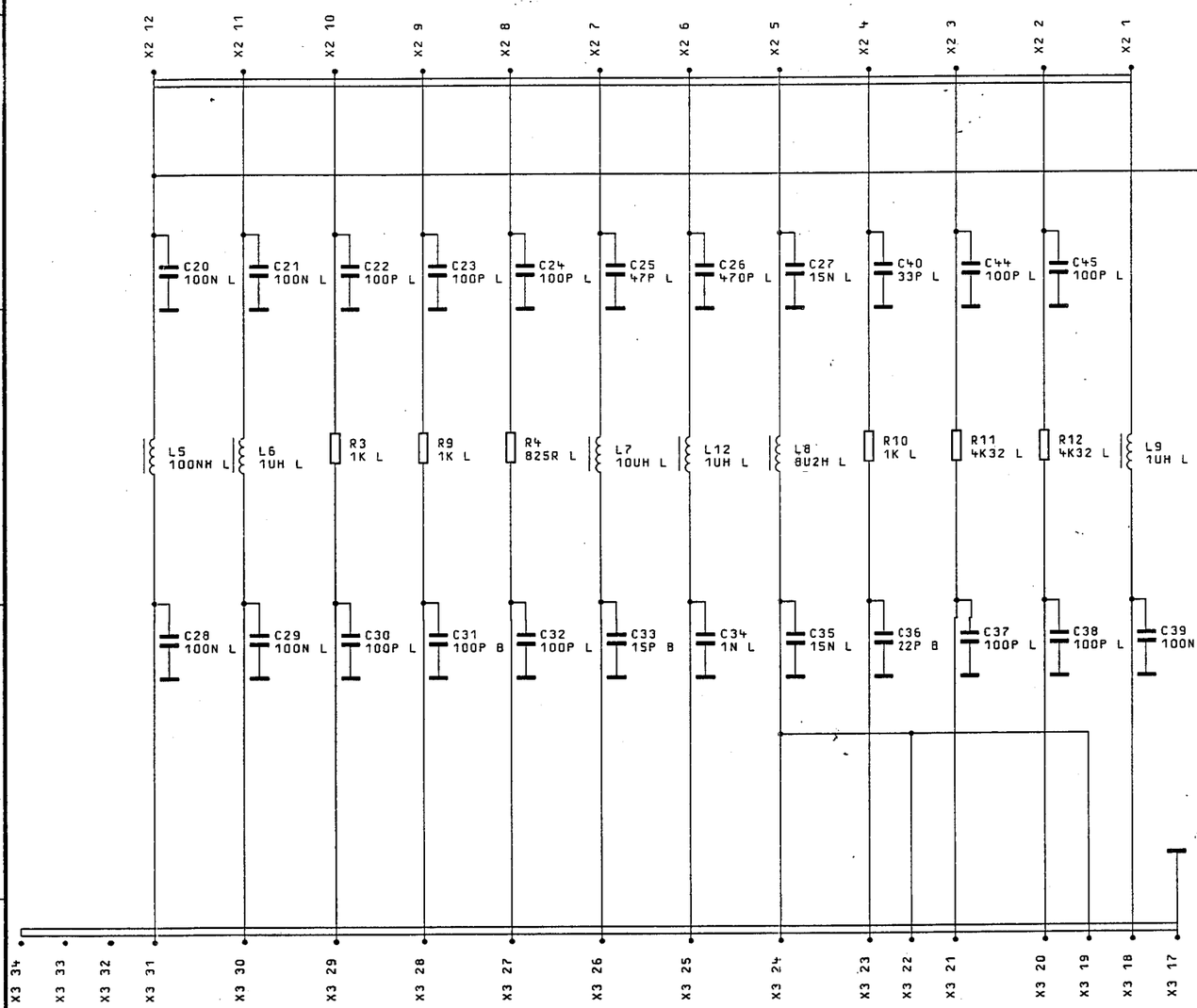
  Hinweis: *When mounting, make sure that the cable W4 and the flat cable 150 do not touch (interferences)!*
  Be careful not to bend the earthing spring when reassembling the filter board. The spring must be visible in the connection cartridge for the measuring heads.

7.5 Interfaces

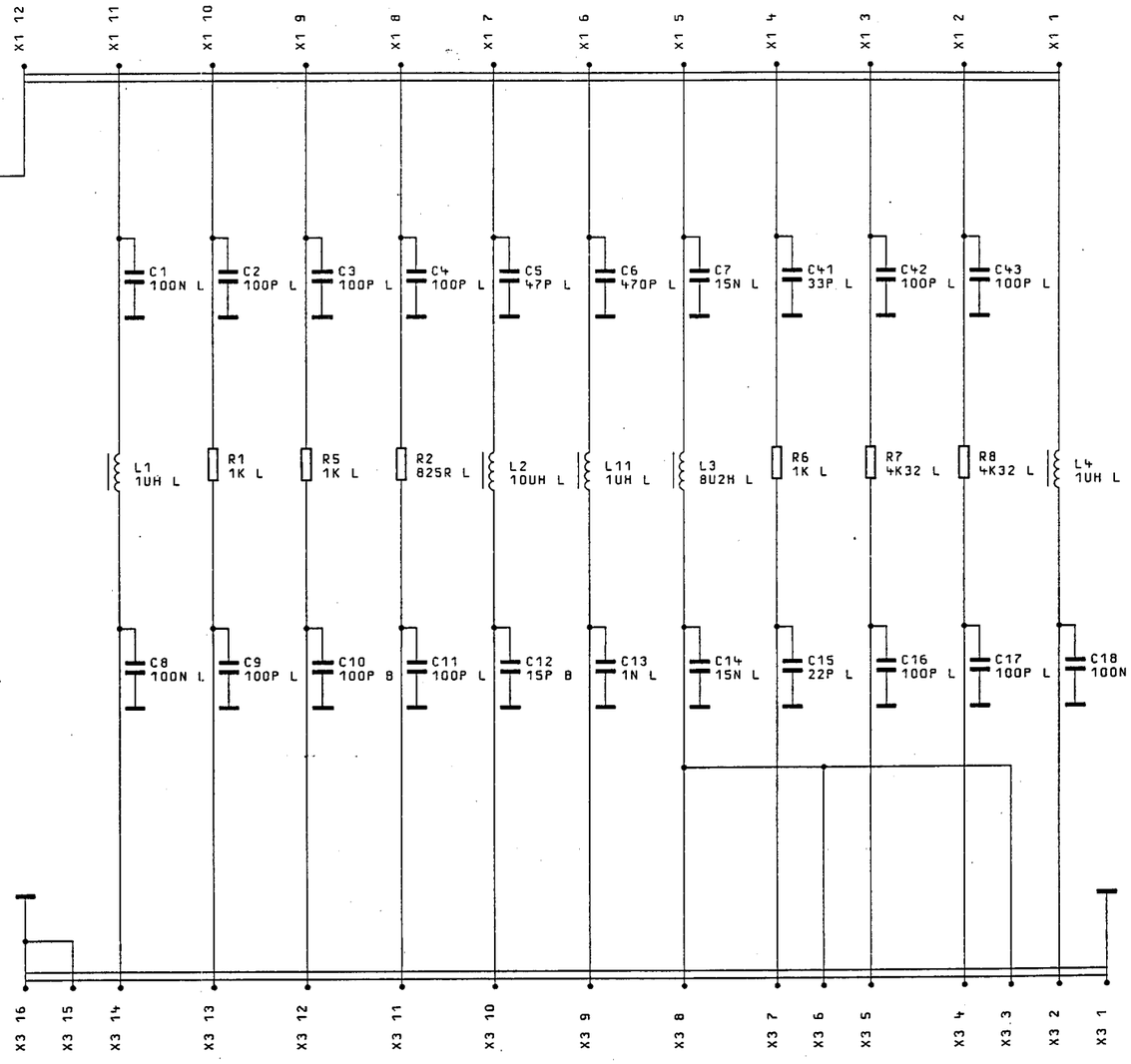
Pin	Name	Input/ Output	Origin	Specified range	Signaldescription
X3.1, 15-17			A2, Analog board		Ground
X3.2, X1.1					Ground
X3.3, 6, 8, X1.5	ARGND				Ref. ground test channel A
X3.4, X1.2	-INPA				AC test input A
X3.5, X1.3	+ INPA				AC test input A
X3.7, X1.4	DCINP1				DC test input A
X3.9, X1.6	TEMPA				Temp. test connector A
X3.10, X1.7	CLKP1				CLK test channel A
X3.11, X1.8	DATP1				Data test channel A
X3.12, X1.9	RSTP1				RST/CE test channel A
X3.13, X1.10	ID1				Identification of sensor A
X3.14, X1.11	VCC1				Vcc test channel A
X3.18, X2.1					Ground
X3.19, 22, 24, X2.5	BRGND				Ref. ground test channel B
X3.20, X2.2	-INPB				AC test input B
X3.21, X2.3	+ INPB				AC test input B
X3.23, X2.4	DCINP2				DC test input B
X3.25, X2.6	TEMPB				Temp. test connector B
X3.26, X2.7	CLKP2				CLK test channel B
X3.27, X2.8	DATP2				Data test channel B
X3.28, X2.9	RSTP2				RST/CE test channel B
X3.29, X2.10	ID2				Identification of sensor B
X3.30, X2.11	VCC2				Vcc test channel B
X3.31, X2.12, X1.12	GND				Ground

BEHALTEN WIR UNS ALLE RECHTE VOR

PROBE B



PROBE A



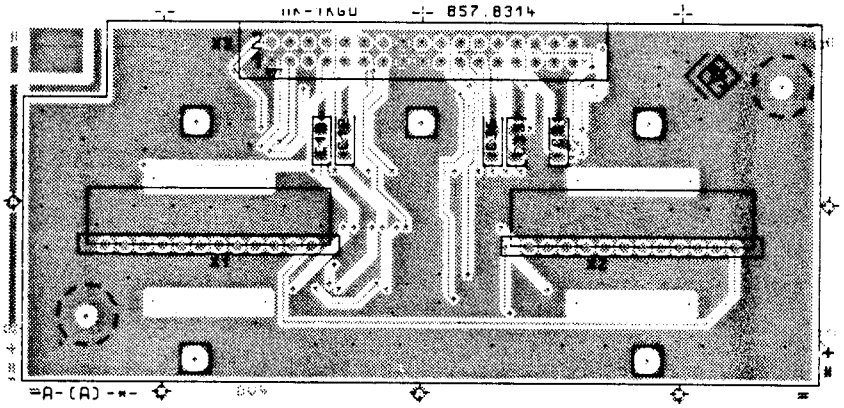
STROMLAUF GILT FUER VAR.02

CIRCUIT DIAGRAM IS VALID FOR MOD.02

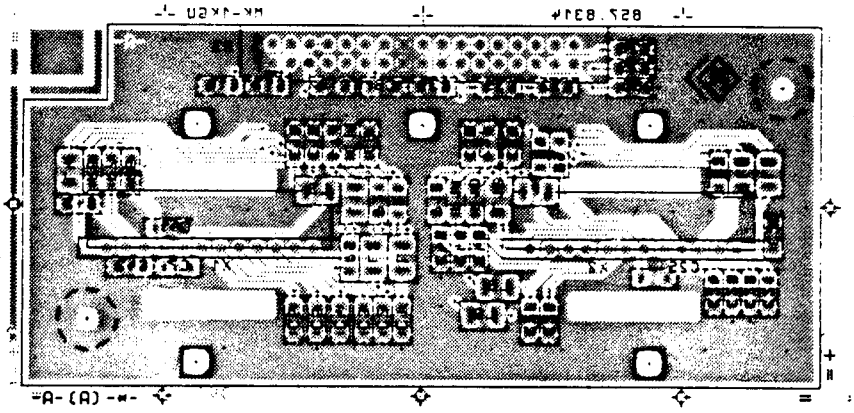
03/00	47627	02.92	MK	1GPK	TAG	NAME	BENENNUNG
				BEARB.		SR	FILTERPLATTE
				GEPR.		MK	FILTERBOARD
				NORM			
				PLOTT	17.03.93		
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR. 857.8308.01S
				ZU GERAET NRVD			REG.I.V. 857.8008 ERSTE Z. 857.8008

BLATT-NR. 1 V. BL.

Ansicht und Leitungsfuehrung Bauteilseite
View of tracks on component side



Ansicht und Leitungsfuehrung Loetseite
View of tracks on solder side



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				Maße ohne Toleranzangabe		Maßstab 1 : 1	
						Halbzeug, Werkstoff	
				1KGU	Tag	Name	Benennung FILTERPLATTE Z
				Bearb	12.90	MK	
				Gepr			
				Norm			
				ROHDE&SCHWARZ		Zeichn.-Nr 857.8308	Blatt-Nr 2 v 4 Bl
And Zust	Anderungs-Mitteilung	Tag	Name	zu Gerat NRVD		reg. V 857.8008 V	erste Z

ROHDE&SCHWARZ

SERVICE INSTRUCTIONS

In/Out Option NRVD-B2

857.8908.02

Contents

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7.1.1	Trigger Input TRIG	7.2
7.1.2	Ready Output RDY	7.2
7.1.3	Analog Outputs DC1 and DC2	7.2
7.2	**Measuring Instruments and Auxiliary Equipment**	7.3
7.3	**Troubleshooting**	7.4
7.3.1	Analog Outputs DC1 and DC2 Faulty	7.4
7.4	**Checking and Adjustment**	7.5
7.4.1	Checking the Operating Voltages	7.5
7.4.2	Calibration of Analog Outputs	7.5
7.5	**Removal and Replacement of In/Out Option**	7.5
7.6	**Interfaces**	7.6

Part lists
Circuit diagrams
Component plans

7 Checking and Repair of In/Out Option NRVD-B2

7.1 Function Description

(See circuit diagram 857.8908.01S and block diagram)

This board is included as an option in the NRVD. It enables the following functions via five BNC sockets at the rear of the instrument:

- Frequency test input for control signals (**DC(FREQ)**
- Trigger input for triggering measured values using a control signal (**TRIG**)
- Ready output to indicate that valid measurement results are available (**RDY**)
- Two analog outputs (**DC1** and **DC2**) for output of DC voltages for level and frequency proportional to the measured value.

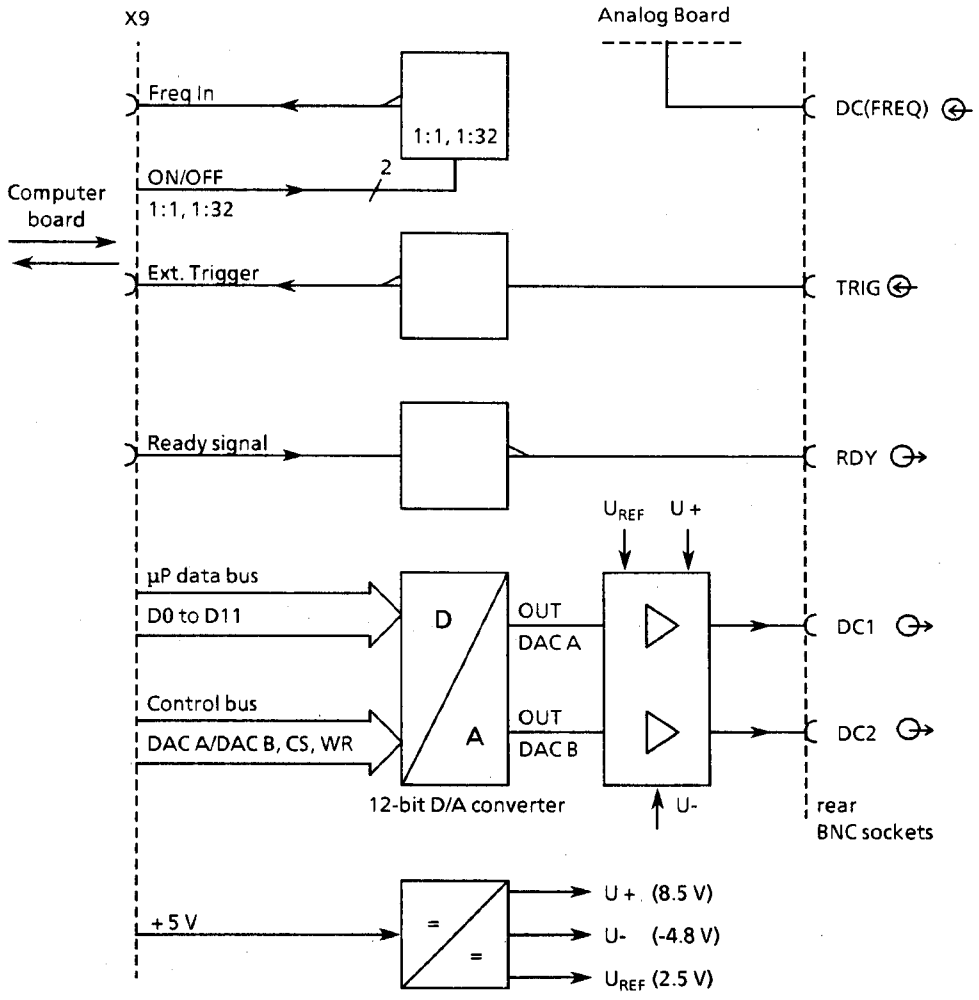


Fig. 7-1 Block diagram In/Out Option NRVD-B2

7.1.1 Trigger Input TRIG

The trigger input uses an external trigger source to provide an interrupt to the processor of the computer board A1. A signal change from H to L causes a measured value to be triggered if the input is activated.

Idle state: Signal at High level (+ 5 V or TTL High) or TRIG input open
Active: Signal at Low level (0 V or TTL Low) or TRIG input short-circuited

The trigger signal at X2 is applied in inverted state via D1-C to the computer board A1 and processor D4.

7.1.2 Ready Output RDY

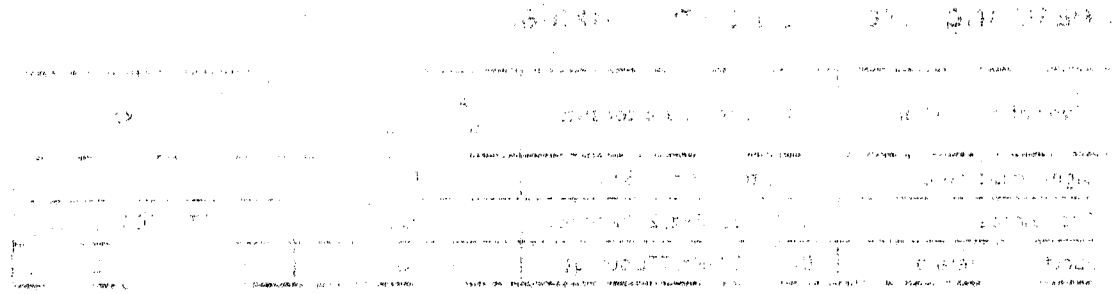
Parallel to the ready display RDY, the RDY output X3 provides a logic signal from the computer board A1 via X9.12 and inverter/buffer D1-D.

At X3: active High ≡ + 5 V with no load or TTL level with LS TTL load.

7.1.3 Analog Outputs DC1 and DC2

Depending on the instrument setting, appropriate DC voltages are applied to analog outputs X4 and X5 with each display cycle.

The display values conditioned in the computer board A1 are transferred in binary format in groups of 12 bits each via the data bus to the dual DAC U1. The D/A converter or analog output to be driven is selected via line X9.7 DAC A/DAC B. An analog voltage ranging from -0.6 V to + 3.6 V is output via N1, N2 and the reference voltage V_{REF} with calibrated analog outputs.



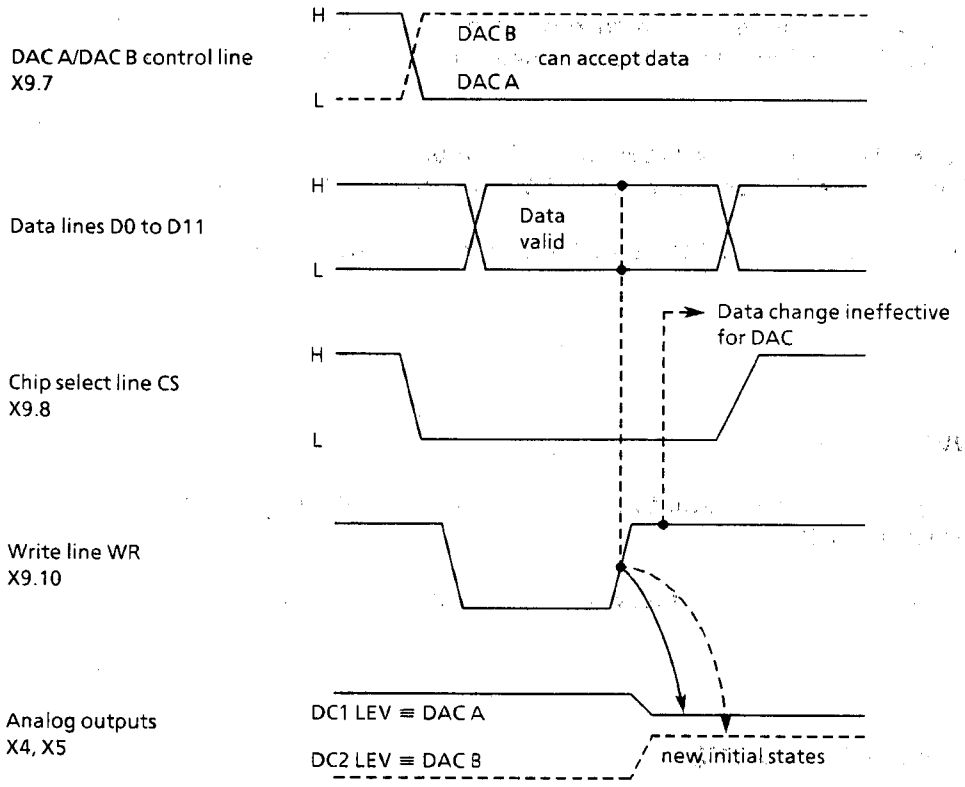


Fig. 7-2 Control signals for D/A converters U1-A,B

The I/O board also contains a voltage supply V+, V- for operational amplifiers N1 and N2 and a reference diode V8 for the +2.5-V reference voltage of the DAC and the precision op amps. Switching converter N3 provides the voltages V+ = +8.5 V and V- = -4.8 V from +5 V at X9.3.

The analog outputs of the In/Out Option can be calibrated ***in conjunction with the basic instrument NRVD*** using calibration routines without external measuring equipment (→ Operating manual, appendix A, 1.10).

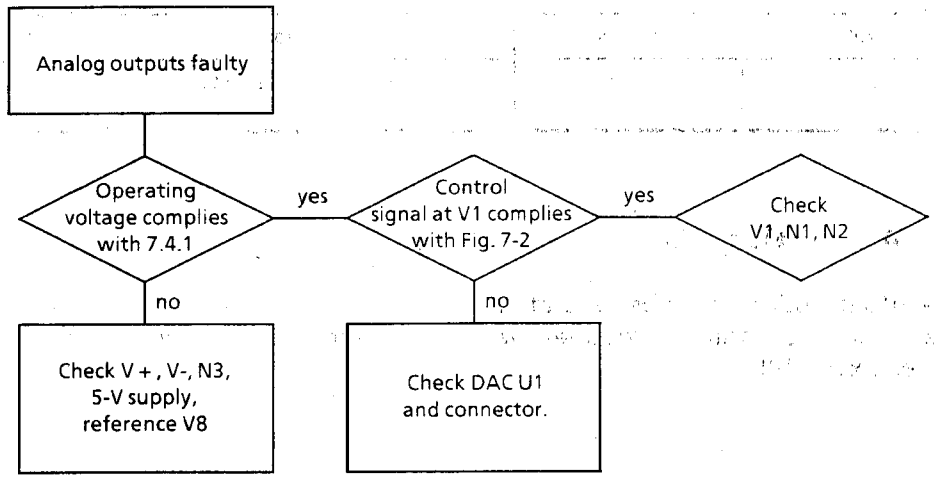
7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Required characteristics	Appropriate R&S instrument	Order No.
1	Digital multimeter	DC, 0 to 10 V ±0.05 %	UDS5	349.1510.02
2	Oscilloscope	DC to 100 MHz, 2 channels	BOL	374.2000.02
3	Function generator	DC to 30 MHz, TTL output	AFGU	377.5000.02

7.3 Troubleshooting

For troubleshooting, proceed according to the following flow charts. Use the circuit diagram for exact fault location.

7.3.2 Analog Outputs DC1 and DC2 Faulty



7.4 Checking and Adjustment

7.4.1 Checking the Operating Voltages

Test point - reference	Voltage	Tolerance	Remark
X9.3 - X9.2 N3.8 - X9.1	5 V	±0.15 V	
N1,8 - N3.3	8.5 V	±0.5 V	with properly working 5-V supply
N1.4 - N3.3	-4.8 V	±0.4 V	with properly working 5-V supply
U1.4 - U1.5 U1.22 - X9.1	2.5 V	±5 mV	Precision reference voltage

7.4.2 Calibration of Analog Outputs

The analog outputs of the In/Out Option are to be calibrated in conjunction with the basic instrument NRVD using program-controlled calibration routines without external measuring equipment (→ Operating manual, appendix A 1.10).

Conditions of calibration:

- Calibrated basic instrument
- Warm-up time 30 minutes
- Ambient temperature 23 ±3 °C
- AC supply voltage, rated value ±5 %

7.5 Removal and Replacement of In/Out Option

(See also exploded view)

Removal:

- Remove the 2 rear-panel feet and both instrument covers (item 17 + 18 and item 1 + 2).
- Pull out the 2 ribbon cable sockets (I/O board).
- Press the 4 plastic supports at the top of the I/O board together and lift off the board.
- Remove the 2 screws at the rear of the instrument and take out the connection plate towards the bottom (item 85 + 86).

Replacement:

For replacement, proceed in the reverse order to removal; see also operating manual section 2.2.

When replacing the lower instrument cover (item 2) make sure not to catch the user's guide in the front frame and damage it. As a precaution, first remove the plastic support first by slightly pressing it together at the sides.

7.6 Interfaces

Pin	Name	Input/ output	Origin/destination	Value range	Signal description
X9.3	VCC	Input	A1, Computer, X60.B2	4.85 V to 5.15 V	Supply voltage digital
X9.1	DGND		A1, Computer, X60.B1	0 V	Digital ground
X9.2			A1, Computer, X60.A1		
X9.4	AGND		A1, Computer, X60.A2	0 V	Analog ground
X9.8	CS	Input	A1, Computer, X60.A4	┐	Chip select
X9.10	WR	Input	A1, Computer, X60.A5	HCMOS level	Write enable
X9.7	DAC A/ DAC B	Input	A1, Computer, X60.B4	┘	Address line
X9,15	D0	Input	A1, Computer, X60.B8	┐	┐
X9.16	D1	Input	A1, Computer, X60.A8	┆	┆
X9.17	D2	Input	A1, Computer, X60.B9	┆	┆
X9.18	D3	Input	A1, Computer, X60.A9	┆	┆
X9.19	D4	Input	A1, Computer, X60.B10	┆	┆
X9.20	D5	Input	A1, Computer, X60.A10	HCMOS level	Data bus for DAC
X9.21	D6	Input	A1, Computer, X60.B11	┆	┆
X9.22	D7	Input	A1, Computer, X60.A11	┆	┆
X9.23	D8	Input	A1, Computer, X60.B12	┆	┆
X9.24	D9	Input	A1, Computer, X60.A12	┆	┆
X9.25	D10	Input	A1, Computer, X60.B13	┆	┆
X9.26	D11	Input	A1, Computer, X60.A13	┘	┘
X9.9	EXT TRIG	Output	A1, Computer, X60.B5	┐	ext. trigger
X9.11	FREQ IN	Output	A1, Computer, X60.B6	┆	Frequency input
X9.12	READY	Input	A1, Computer, X60.A6	HCMOS level	Ready signal
X9.14	ON/OFF	Input	A1, Computer, X60.A7	┆	On/off Frequency input (not conn)
X9.13	:1/:32	Input	A1, Computer, X60.B7	┘	32:1 frequency divider
X8.5	FREQ IN	Input	Connect. plate, X7.B3		Control signals
X8.3	GND		Connect. plate, X7.A2	0 V	Ground
X8.4			X7.B2		
X8.6			X7.A3		
X8.9			X7.B5		
X8.7	EXT. TRIG	Input	Connect. plate, X7.B4	TTL level	External trigger input
X8.8	READY	Output	Connect. plate, X7.A4	TTL level	Ready output
X8.1	DC1	Output	Connect. plate, X7.B1	-0.68 V ± 5 % to 3.98 V ± 3 %	DC output 1
X8.2	DC2	Output	Connect. plate, X7.A1	-0.68 V ± 5 % to 3.98 V ± 3 %	DC output 2

Pin	Name	Input/ Output	Origin/destination	Value range	Signal description
X1	DC(FREQ)	Input	BNC socket rear, X103.2	0 V to 10 V	Rear input frequency proportional voltage
X2	TRIG	Input	BNC socket rear, X7.B4	TTL-Pegel	External trigger input
X3	RDY	Output	BNC socket rear, X7.A4	TTL-Pegel	Ready output
X4	DC1 LEV	Output	BNC socket rear, X7.B1	-0,68 V ± 5 % to 3,98 V ± 3 %	Analog output 1 for level
X5	DC2 LEV	Output	BNC socket rear, X7.A1	-0,68 V ± 5 % to 3,98 V ± 3 %	Analog output 2 for level

CONNECTOR BOARD

I/O BOARD

FREQ IN

EXT. TRIG

READY

DC 1

DC 2

NICHT BESTUECKT
NOT IN PCB

ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.

ATTENTION: ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING.

CIRCUIT DIAGRAM IS VALID FOR MOD.02

STROMLAUF GILT FUER VAR.02

	1KGU	TAG	NAME
	BEARB.		MK
	GEPR.		MK
	NORM		
	PLOTT	11.5.90	MK

BENENNUNG: NRVD-B2 I/O OPTION

ZEICHN.-NR.: 857.8908.01S

BLATT-NR.: 1

V. 1 BL.

ROHDE&SCHWARZ

ZU GERÄT NRVD

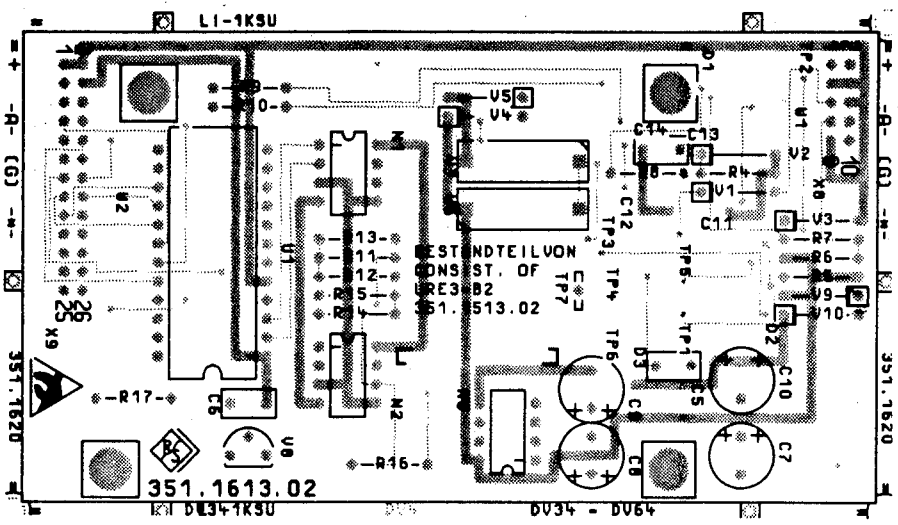
REG.I.V. 857.8008

ERSTE Z.

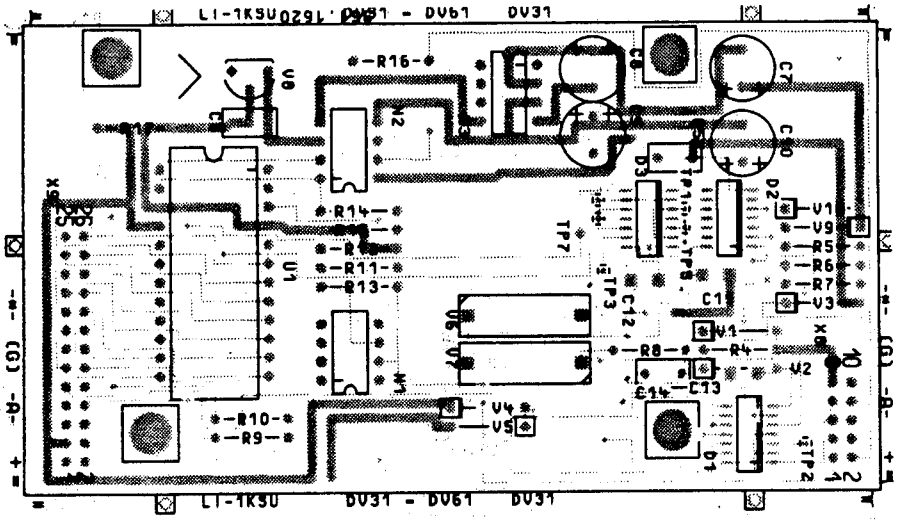
BEND. IND. | AENDERUNGS-MITTEILUNG | DATUM | NAME

FUER DIESE UNTERLAGE BEHALTEN WIR UNS ALLE RECHTE VOR

ZEICHN.-NR.



Ansicht und Leitungsführung Bauteilseite
View of tracks on component side



Ansicht und Leitungsführung Lötseite
View of tracks on solder side

(hierzu HVC 250)

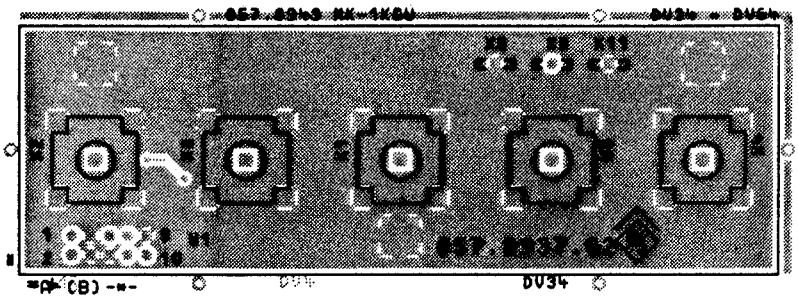
ACHTUNG: EGB!
Elektrostatisch gefährdete Bauelemente erfordern eine besondere Handhabung

ATTENTION ESD!
Electrostatic sensitive devices require a special handling

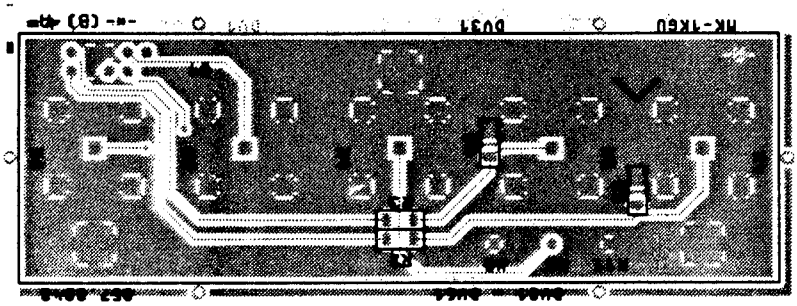
B 42766	5.90 Li	Maße ohne Toleranzangabe		Maßstab 1 : 1	
				Halbzeug, Werkstoff	
		1KGU	Tag	Name	Benennung: I/O-BOARD — Z
		Bearb	5.89	LI	
		Gepr			
		Norm			
		ROHDE & SCHWARZ		Zeichn.-Nr 351.1613.02	Blatt-Nr 3
And Zust	Änderungs-Mitteilung	Tag	Name	zu Gerät URE3-B2	reg. V 351.1513V — erste Z

Für diese Unterlage behalten wir uns alle Rechte vor

Ansicht und Leitungsfuehrung Bauteilseite
View of tracks on component side



Ansicht und Leitungsfuehrung Loetseite
View of tracks on solder side



Für diese Unterlage behalten
wir uns alle Rechte vor

			Maße ohne Toleranzangabe		Maßstab 1 : 1
					Halbzeug, Werkstoff
			1KGU	Tag	Name
			Bearb	10.90	MK
			Gepr		
			Norm		
			ROHDE&SCHWARZ		Zeichn.-Nr 857.8937
			zu Gerat NRVD		reg. i V 857.8908 V
And Zust	Anderungs-Mitteilung	Tag	Name		

Benennung
BUCHSENPLATTE
CONNECTORBOARD

Z

Blatt-Nr 2

v Bl

erste Z