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1991 AND 1992 NANOSECOND UNIVERSAL COUNTERS

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RACAL

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LETHAL VOLTAGE WARNING

VOLTAGES WITHIN THIS EQUIPMENT ARE SUFFICIENTLY HIGH TO ENDANGER LIFE.

COVERS MUST NOT BE REMOVED EXCEPT BY PERSONS QUALIFIED AND AUTHORISED TO DO SO AND THESE PERSONS SHOULD ALWAYS TAKE EXTREME CARE ONCE THE COVERS HAVE BEEN REMOVED.

RESUSCITATION

TREATMENT OF THE NON-BREATHING CASUALTY

1 SHOUT FOR HELP. TURN OFF WATER, GAS OR SWITCH OFF ELECTRICITY IF POSSIBLE

Do this immediately. If not possible don't waste time searching for a tap or switch.

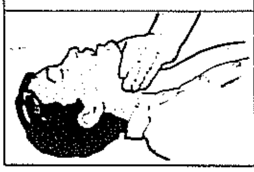
2 REMOVE FROM DANGER: WATER, GAS, ELECTRICITY, FUMES, ETC.

Safeguard yourself when removing casualty from hazard. If casualty still in contact with electricity, and the supply cannot be isolated, stand on dry non-conducting material (rubber mat, wood, linoleum).
Use rubber gloves, dry clothing, length of dry rope or wood to pull or push casualty away from the hazard.

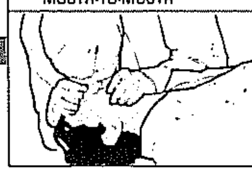
3 REMOVE OBVIOUS OBSTRUCTION TO BREATHING

If casualty is not breathing start ventilation at once.

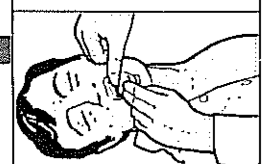
LOOSEN NECKWEAR
TILT HEAD BACKWARDS
AND PUSH CHIN UPWARDS



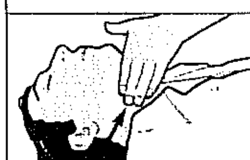
PINCH THE NOSE
COMMENCE VENTILATION
FOUR GOOD INFLATIONS
MOUTH-TO-MOUTH



IF CHEST DOES NOT RISE
RE-CHECK AIRWAY, REMOVE
OBSTRUCTION AND RE-INFLATE



CHECK PULSE



POSITION OF PULSE

PULSE PRESENT

PULSE ABSENT

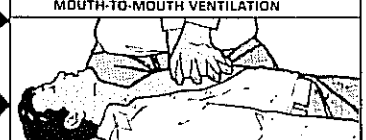
HEART HAS STOPPED BEATING
LAY ON BACK ON FIRM SURFACE (eg FLOOR).
COMMENCE EXTERNAL CHEST COMPRESSION AND CONTINUE MOUTH-TO-MOUTH VENTILATION

ONE FIRST AIDER

15 Compressions at 80 per minute followed by 2 Inflations

TWO FIRST AIDERS

One conducts chest compressions, without pause at 60 per minute. The other administers mouth-to-mouth ventilation — after each 5th compression.

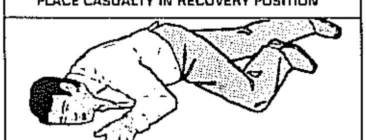


Check heart beat after first minute and then after every three minutes. Continue external chest compression and mouth-to-mouth ventilation until a normal pulse is felt and colour improves.

CONTINUE INFLATIONS
UNTIL RECOVERY OF
NORMAL BREATHING

CONTINUE INFLATIONS
UNTIL RECOVERY OF
NORMAL BREATHING

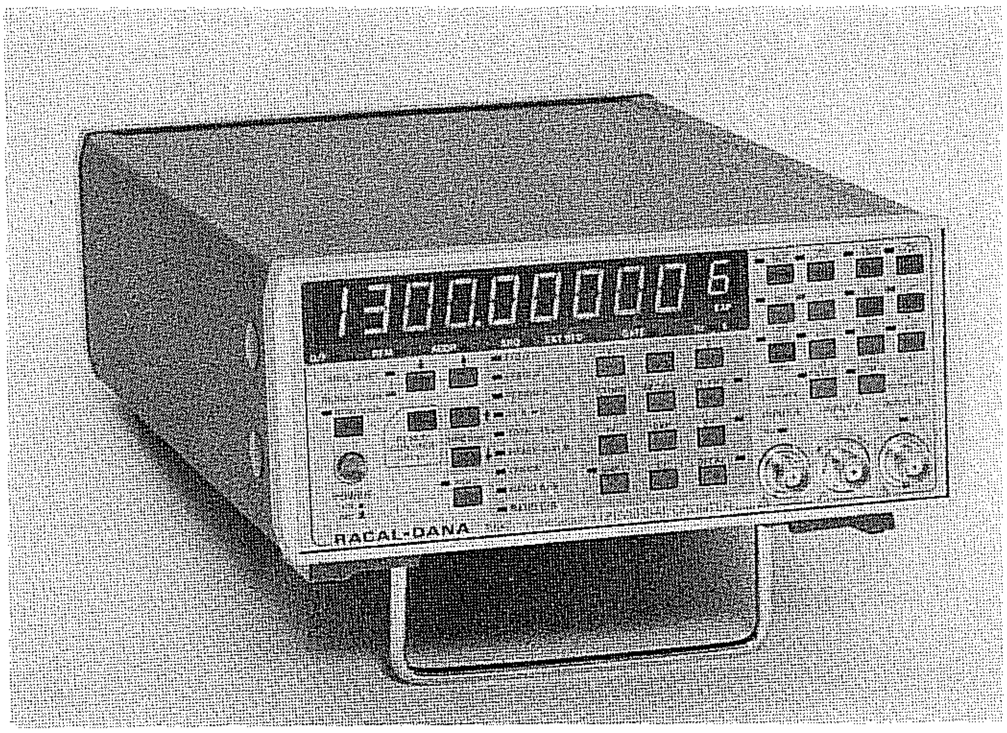
WHEN NORMAL BREATHING COMMENCES
PLACE CASUALTY IN RECOVERY POSITION



Keep casualty at rest. Remove on a stretcher. Watch closely, particularly for difficulty in breathing. Lightly cover with blankets or other materials.

SEND FOR DOCTOR AND AMBULANCE

DOCTOR	AMBULANCE	HOSPITAL	Nearest First Aid Post
TELEPHONE	TELEPHONE	TELEPHONE	



Universal Counter 1992

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of indentification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

POZIDRIV SCREWS

The metric thread cross-head screws fitted to RACAL equipment are of the POZIDRIV type. Phillips and POZIDRIV screwdrivers are not interchangeable, and use of the wrong type of screwdriver may cause damage. POZIDRIV is a registered trade mark of G.K.N. Screws and Fasteners Ltd. POZIDRIV screwdrivers are manufactured by Stanley Tools Ltd.

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Model 1991

Input Characteristics

Inputs A and B

Frequency Range	
Input A	DC to 160MHz DC coupled 10Hz to 160MHz AC coupled
Input B	DC to 100MHz DC coupled 10Hz to 100MHz AC coupled
Sensitivity	
Sine Wave	25mVrms DC to 100MHz 50mVrms to 160MHz
Pulse	75mV p-p, 5nS min. width
Dynamic Range (× 1 attenuation)	75mV to 5V p-p to 50MHz 75mV to 2.5V p-p to 100MHz 150mV to 2.5V p-p to 160MHz
Signal Operating Range	
× 1 attenuation	± 5.1V
× 10 attenuation	± 51V
Input Impedance (nominal) (× 1 and × 10 atten.)	
Separate Mode	50ohms or 1 Megohm //≤45pf
Common Mode	50ohms or 1 Megohm //≤55pf
Maximum Input (without damage)	
50 ohms	5V(DC + ACrms)
1 Megohm (× 1 attenuation)	260V(DC + ACrms), DC to 2kHz Decreasing to 5V rms, at 100kHz and above.
1 Megohm (× 10 attenuation)	260V(DC + ACrms), DC to 20kHz Decreasing to 50Vrms at 100kHz and above.
Coupling	AC or DC.
Low Pass Filter	50kHz nominal (Input A selectable).
Trigger Slope	+ve or −ve
Attenuator	×1 or ×10. In Auto Trigger mode, attenuator selected automatically if necessary.
Trigger Level Range	
Manual	
× 1 attenuation	± 5.1V in 20mV steps.
× 10 attenuation	± 51V in 200mV steps.
Automatic	± 51V.
Trigger Level Accuracy	
Manual and Automatic	
× 1 attenuation	± 30mV ± 1% of trigger level reading.
× 10 attenuation	± 300mV ± 1% of trigger level reading.
Auto Trigger	
Frequency Range	DC and 50Hz to 100MHz (Typically 160MHz)
Min. Amplitude (AC)	Typically 150mV p-p*
× 10 attenuator	Automatically selected if input signal exceeds ±5.1V or 5.1V p-p*.

Trigger Level Outputs (Rear Panel)	
Range	± 5.1V
Accuracy (Relative to true trigger level)	
× 1 attenuation	± 1% V output ± 10mV
× 10 attenuation	± 1% V output ± 100mV
Impedance	10 kohm nominal.

External Arming

A comprehensive external arming capability to determine the START and/or STOP point of a measurement. Available on all measurement functions except phase.

Input Signal (via Rear Panel)	TTL compatible (min. pulse width 200ns).
Slope	+ve or −ve independently selectable on START or STOP arm.
Impedance	1kohm nominal.

Measurement Modes

Frequency A

Range	DC to 160MHz.
Digits Displayed	3 to 9 digits plus overflow
LSD Displayed (Hz)	$F \times 10^{-D}$ (D = No. of digits, F = Freq. rounded up to next decade)*.
Resolution *(Hz)	± LSD† ± (Trig. Error* × Freq.) /Gate Time.
Accuracy *(Hz)	± Resolution ± (Timebase Error × Frequency)

Time Interval

Range	
Separate Mode	0 to 8 × 10^5 sec. Typically −2nS to +8 × 10^5 Sec.
Common Mode	5nS to 8 × 10^5 Sec.
Input	
Common	Input A START and STOP
Separate	Input A START Input B STOP
Trigger Slopes	+ve or −ve Selectable START and STOP.
LSD Displayed	1nS min.
Resolution *(Sec)	± LSD ± 1nS ± Trig Error*
Accuracy *(Sec)	± Resolution ± (Timebase Error × TI). ± Trigger Level Timing Error* ± 2nS**

Time Delay

Available on Time Interval and Totalize.

Range	200 µS to 800 mS nominal.
Step Size	25 µS nominal.
Accuracy	± 0.1% Rdg. ± 50µS

** A differential delay which may be reduced by numerical offset or external compensation.
† 2LSD for 6–9 digits displayed.
* See Definitions.

Period A

Range	6.25nS to 1.7 $\times 10^3$ Sec
Digits Displayed	3 to 9 digits plus overflow.
LSD Displayed (Sec)	P $\times 10^{-D}$ (D = No. of digits, P = Period rounded up to next decade)*.
Resolution *(Sec)	± LSD† ± (Trig. Error* × Period) /Gate Time.
Accuracy *(Sec)	± Resolution ± (Timebase Error × Period).

Ratio A/B

Specified for higher frequency applied to Input A.

Range	DC to 100MHz on both inputs.
LSD Displayed (for 6–9 digits selected)	$\left(\frac{10}{\text{Freq. B} \times \text{Gate Time}}\right)$, rounded to nearest decade*.
Resolution*	± LSD ± (Trig. Error B */Gate Time) × Ratio.
Accuracy*	± Resolution.

Totalize A by B

Accumulative or single totalize.

Input	Input A.
Range	$10^{18}-1$ (Max. 9 most significant digits displayed).
Maximum Rate	10^8 events/Sec.
Minimum Pulse Width	5nS min. at trigger points.
Accuracy	±1 count.
Start/Stop	Electrical (Input B) or Manual.

Phase (A rel. to B)

Range	0.1° to 360°.
LSD Displayed	0.1° to 1MHz. 1.0° to 10MHz. 10° to 100MHz.
Resolution *(degrees)	± LSD ± (TI Resolution/Period A) × 360°
Accuracy *(degrees)	± LSD ± (TI Accuracy/Period A) × 360°

Amplitude Measurement

Peak*

Frequency Range	50Hz to 20MHz.
Amplitude Range	160mV p-p to 51V p-p.
Resolution	
× 1 attenuation	20mV
× 10 attenuation	200mV
Accuracy	
× 1 attenuation	± 50mV ± 6% V p-p. (Typically ± 40mV ± 2% V p-p.)
× 10 attenuation	± 500mV ± 10% V p-p. (Typically ± 400mV ± 3% V p-p.)

DC (<15mV p-p AC)

Amplitude Range	±51V.
Resolution	
× 1 attenuation	20mV
× 10 attenuation	200mV
Accuracy	
× 1 attenuation	± 40mV ± 1% Rdg.
× 10 attenuation	± 400mV ± 1% Rdg.

Math

Available on all measurements except Phase and Check.

Function	(Result −X)/Z.
Entry Range	$\pm 1 \times 10^{-10}$ to $\pm 1 \times 10^{10}$ to 9 significant figures.

General

Internal Timebase

Crystal Controlled

Frequency	10MHz.
Aging	2×10^{-6} in the first year.
Temperature Stability	1×10^{-5} over the range 0 to +50°C.
Adjustment	Via rear panel.

Frequency Standard Output

Frequency	10MHz.
Amplitude	>600mV p-p into 50 ohms.
Impedance	250 ohms nominal.

External Standard Input

Frequency	10MHz (see also Option 10 for other frequencies).
Signal Amplitude (Sine Wave)	Min. 100mV rms Max. 10V rms
Impedance	1 kohm nominal at 1V p-p 500 ohms nominal at 10V p-p

Gate Time

(Frequency, Period and Ratio modes). Automatically determined by resolution selected (Range 1 msec –10sec)*.

Resolution Selected	Gate Time (seconds)
9 + overflow	10
9	1
8	0.1
7	0.01
6,5,4,3	0.001

Single Cycle (Hold)	Enables a single measurement to be initiated and held.
Display	9-digit, high brightness, 14mm LED display in engineering format with exponent digit.

† 2LSD for 6–9 digits displayed.
* See Definitions.

Power Requirements

Voltage	90–110 103–127 193–237 207–253 VAC
Frequency	45–450Hz
Rating	35VA Max.
Operating Temperature Range	0° to + 50°C. (0° to + 40°C with battery pack).
Storage Temperature Range	−40°C to +70°C (−40°C to +60°C with battery pack).
Safety	Designed to meet the requirements of IEC348 and follow the guidelines of UL1244.
Weight	Net 3.63kg (8lb.) excl. battery 6.8kg (15lb.) inc. battery Shipping 5.5kg (11lb.) excl. battery 8.75kg (19.3lb.) inc. battery
Shipping Dimensions	430 × 360 × 280mm (16.91 × 14.2 × 11.0 ins.)

Model 1992

Specification identical to that for Model 1991 with the addition of the following:-

Input Characteristics

Input C

Frequency Range	40MHz to 1.3GHz.
Sensitivity	
Sine Wave	<10mV rms, 40MHz to 1GHz <75mV rms to 1.3GHz.
Dynamic Range	10mV rms to 5V rms to 1GHz. 75mV rms to 5V rms to 1.3GHz.
Input Impedance	50 ohms nominal AC coupled.
VSWR	≤ 2:1 at 1GHz.
Maximum Input	7V rms (fuse protected). Fuse located in BNC connector.
Damage Level	25W.

Measurement Modes

Frequency C

Range	40MHz to 1.3GHz.
LSD	As for Frequency A*.
Resolution* and Accuracy*	As for Frequency A.

Ratio C/B

Specified for higher frequency applied to Input C.

Range	Input C 40MHz to 1.3GHz. Input B DC to 100MHz.
LSD Displayed (for 6–9 digits selected)	$\left(\frac{640}{\text{Freq. B} \times \text{Gate Time}}\right)$, rounded to nearest decade*.
Resolution* and Accuracy*	As for Ratio A/B.

Options

Option 01 Rear Panel Inputs

A rear panel input, factory fitted option, is available for ATE applications. Inputs A and B are in parallel with those on the front panel while input C (Model 1992 only) is fitted in place of the front panel input.

Option 04T

Temperature Controlled Crystal Oscillator

Frequency	10MHz.
Aging Rate	3×10^{-7}/month. 1×10^{-6} in the first year.
Temperature Stability	1×10^{-6} over the range 0 to +40°C (operable to +50°C).
Adjustment	Via rear panel.

Option 04A

Ovened Oscillator

Frequency	10MHz
Aging Rate	3×10^{-9}/day averaged over 10 days after 3 months continuous operation.
Temperature Stability	$\pm 3 \times 10^{-9}$/°C averaged over range 0° to +45°C (operable to +50°C).
Warm Up	Typically $\pm 1 \times 10^{-7}$ within 6 minutes.
Adjustment	Via rear panel.

Option 04B

High Stability Ovened Oscillator

Frequency	10MHz
Aging Rate	5×10^{-10}/day averaged over 10 days after 3 months continuous operation.
Temperature Stability	$\pm 6 \times 10^{-10}$/°C averaged over range 0° to +45°C (operable to +50°C).
Warm Up	$\pm 1 \times 10^{-7}$ within 20 minutes.
Adjustment	Via rear panel.

Option 07

Rechargeable Battery Pack and External DC Operation.

Battery Type	Sealed lead-acid cells.
Battery Life	Typically 4 hours at +25°C (10 hrs on standby).
Battery Condition	Display indicates battery low.
External DC	11–16V via socket on rear panel (−ve ground, not isolated).

Option 10

Reference Frequency Multiplier

Input Frequency	1, 2, 5 or 10MHz ($\pm 1 \times 10^{-5}$).
Input Amplitude and Impedance	As for external standard input.

Option 55

GPIB Interface	Designed to comply with IEEE-STD-488 (1978) and to conform with the guidelines of IEEE-STD-728 (1982).
Control Capability	All functions and controls programmable except power on/off and standby charge.
Output	Engineering format (11 digits and exponent).

* See Definitions.

IEEE-STD-488 Subsets	SH1, AH1, T5, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C0, E2.
Handshake Time	250μS to 1mS/character dependent on message content.
Read Rate	Typically 20/sec dependent upon measurement function.

Definitions

LSD (Least Significant Digit).
In Frequency and Period modes display automatically upranges at 1.1 × decade and downranges at 1.05 × decade, except on Input C for input frequency > 1GHz.

Accuracy and Resolution Expressed as an RMS value.

Trigger Error RMS.

$$\text{Trigger Error (seconds)} = \sqrt{\frac{(e_{i1}^2 + e_{n1}^2)}{S1^2} + \frac{(e_{i2}^2 + e_{n2}^2)}{S2^2}}$$

where e_i = input amplifier RMS noise (typically 150μV RMS in 160MHz bandwidth).
e_n = input signal RMS noise in 160MHz bandwidth.
S = Slew rate at trigger point V/Sec.
Suffix 1 denotes START edge
Suffix 2 denotes STOP edge
In Frequency A, Period A, Frequency B and Period B modes triggering is always on positive going edge.

Trigger Level Timing Error

$$\text{Trigger Level Timing Error (Seconds)} = 0.035 \left(\frac{1}{S1} - \frac{1}{S2}\right)$$

$$\text{typically} = 0.018 \left(\frac{1}{S1} - \frac{1}{S2}\right)$$

S1 = Slew rate on START edge V/Sec.
S2 = Slew rate on STOP edge V/Sec.

Gate Time

The nominal gate time indicated is set by the resolution selected in Frequency Period Ratio and Check modes. It is the value which is used in the calculation of LSD and Resolution. The true gate time will be extended from this value by up to:

(a) One period of the input signal(s) on Frequency B, Period B and Ratio A/B.
(b) Two periods of the input signal on Frequency A and Period A.
(c) One period of input signal B on Ratio C/B.

Peak and Peak-to-Peak Amplitudes

Peak is defined as being the highest or lowest point at which the signal width is 5nS. Similarly, Peak-to-Peak is the difference between the highest and lowest points at which the signal width is 5nS.

Supplied Accessories

Power Cord
Spare Fuse
Operator's Manual
Spare 1.3GHz Fuse (Model 1992 only).

Ordering Information

1991	160MHz Universal Counter
1992	1300MHz Universal Counter

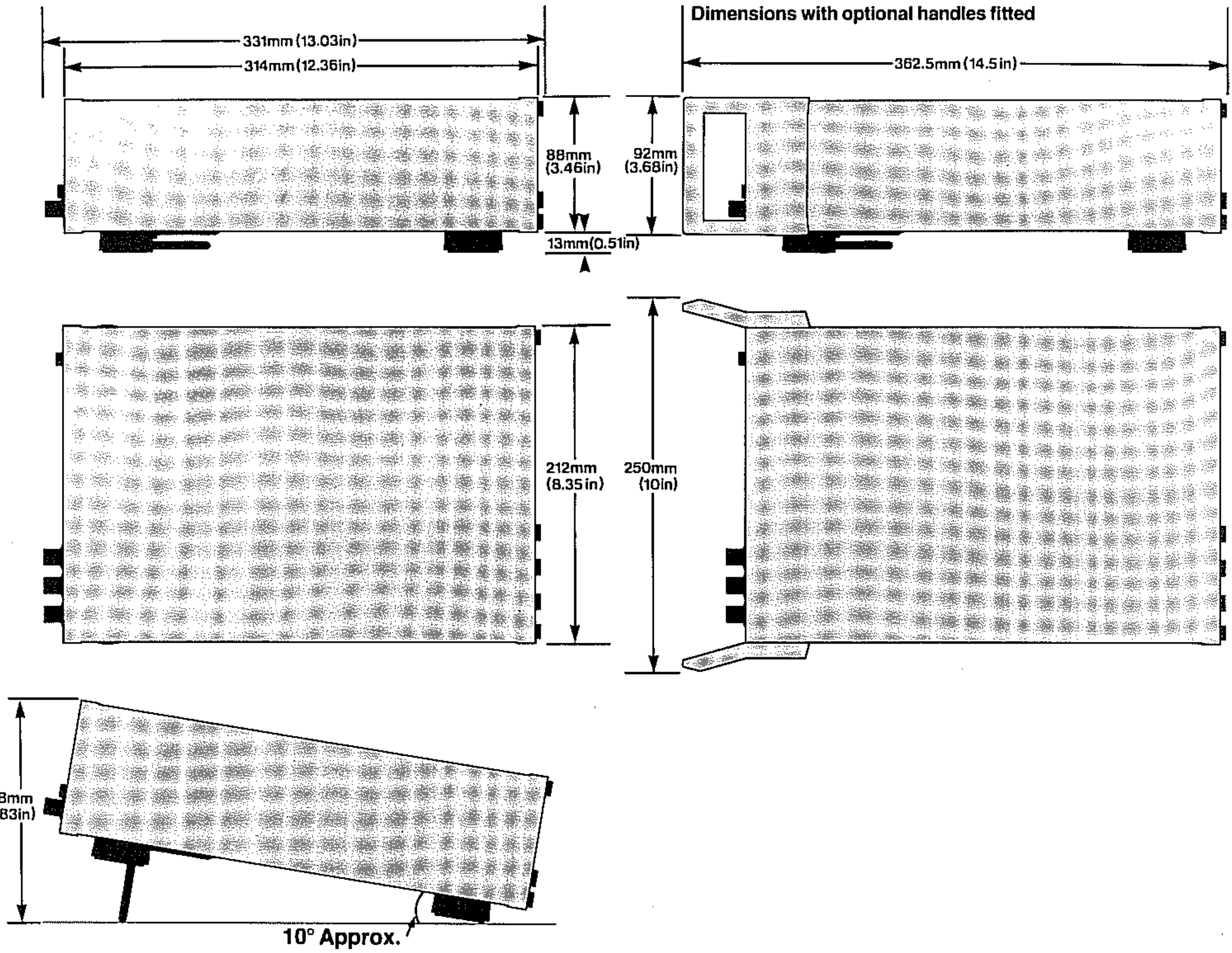
Options and Accessories

01*	Rear Panel Inputs	11–1709 (Model 1991)
01*	Rear Panel Inputs	11–1732 (Model 1992)
04T**	TCXO	11–1713
04A**	Oven Oscillator	11–1710
04B**	High Stability Oven Oscillator	11–1711
07†	Battery Pack	11–1625
10	Reference Frequency Multiplier	11–1645
55†	GPIB Interface	11–1626
60	Handles	11–1730
60A	Rack Mounting Kit (Fixed, Single)	11–1648
60B	Rack Mounting Kit (Fixed, Double)	11–1649
61	Carrying Case	15–0773
61M	Protectomuff Case	15–0736
65	Chassis Slides (incl. Rack Mounts)	11–1716
	Thru-line Connector	11–0167
	Telescopic Antenna	23–9020
	High Impedance Probe	23–9104
	1.3GHz Fuse (Pkt. 5)	11–1718

** Fitting Option 01 may affect certain specification parameters.*

*** Only one frequency standard may be fitted at any one time. The standard reference will be supplied unless option 04T, 04A or 04B is specified.*

† The battery pack and GPIB options cannot both be fitted.


Dimensions with optional handles fitted
331mm (13.03in)
314mm (12.36in)
362.5mm (14.5in)
88mm (3.46in)
92mm (3.68in)
13mm (0.51in)
212mm (8.35in)
250mm (10in)
148mm (5.83in)
10° Approx.

INTRODUCTION

1 The Racal-Dana universal counters, Models 1991 and 1992, are microprocessor controlled instruments offering high accuracy measurements with a comprehensive range of facilities. The Model 1992 is provided with an additional C channel which extends the frequency measuring range from 160 MHz to 1.3 GHz.

MEASUREMENT FUNCTIONS

Frequency A Function

2 The Frequency A function is used to measure the frequency of the signal applied to the channel A input. A resolution of nine digits is available with a one-second gate time.

Frequency C Function

3 The Frequency C function is available on Model 1992 only. It is used to measure the frequency of the signal applied to the channel C input. A resolution of nine digits is available with a one-second gate time.

Period A Function

4 The Period A function is used to measure the period of the waveform applied to the A channel input. A number of periods, depending upon the resolution (and therefore the gate time) selected, are measured, and the average value is displayed.

Time Interval Function

5 The Time Interval function is used to make single-shot measurements of the time interval between:

(1) An event occurring at the channel A input and a later event at the channel B input (using separate input channels).

(2) Two events occurring at the channel A input (using a common input channel).

6 The arming of the stop circuit can be delayed for a time set by the operator. This prevents the measurement interval being stopped prematurely by spurious pulses, such as those caused by contact bounce.

Total A Function

7 The Total A function permits events occurring at the channel A input to be totalized. The counting interval can be controlled by:

(1) Electrical start and stop signals applied to the channel B input (Total A by B).

(2) Successive operations of a front panel key (Manual Totalize).

8 Delayed arming of the stop circuit, to prevent spurious triggering, is available in the Total A by B mode. The Manual Totalize mode provides the facility for totalizing cumulatively over a number of periods.

Phase A rel B Function

9 The Phase A rel B function is used to measure the phase difference between the waveform applied to the A channel input and that applied to the channel B input. The phase difference is displayed in degrees, and indicates the phase lead at the channel A input.

Ratio A/B Function

10 The Ratio A/B function is used to measure the ratio of the frequency applied to the channel A input to that applied to the channel B input.

Ratio C/B Function

11 The Ratio C/B function is available on Model 1992 only. It is used to measure the ratio of the frequency applied to the channel C input to that applied to the channel B input.

CHECK FUNCTION

12 With the Check function selected a number of functional tests of the instrument's circuits can be made without the use of additional test equipment. Although these tests do not check the instrument's performance to its published specification, they can be used to verify that the equipment is operating correctly following receipt or transportation to a new location. A suitable functional check procedure is given in Section 3.

SIGNAL INPUT CHANNELS

13 Signal input channels A and B are fully independent, but provision is made for connection of the signal at the channel A input into both channels. When this is done, the channel B input socket is isolated from channel B.

14 Each channel is provided with independent controls to permit the selection of:

(1) AC or DC input coupling.

(2) 1 MΩ or 50 Ω input impedance.

(3) X1 or X10 input attenuation.

(4) Positive- or negative-slope trigger.

(5) Manually-set or automatically-set input trigger level.

The manually-set trigger level is entered into an internal store.

The auto trigger level is derived by measuring the positive and negative peaks of the input signal. If the peak-to-peak value exceeds 5.1 V, or if either peak is outside the range ±5.1 V, the X10 attenuator is switched in. The trigger level is then set to the arithmetic mean of the measured value.

When operating on auto trigger with the X10 attenuator in circuit, the attenuator will be switched out if the peak-to-peak value is less than 4.6 V and both peak values are within the range ±4.6 V.

The trigger levels in use are available at pins mounted on the rear panel of the instrument. The voltage range is ±5.1 V regardless of whether the attenuator is switched in or not, so the voltage should be multiplied by 10 when the attenuator is in circuit.

15 Signal input channel C is available on Model 1992 only. This input has a nominal input impedance of 50 Ω and is AC coupled. Protection against excessive signal levels is provided by a fuse in the input socket.

LOW-PASS FILTER

16 An internal low-pass filter can be introduced to reduce the bandwidth of channel A to 50 kHz (nominal).

MATH FUNCTION

17 When the math function is active, the displayed value is

$$\frac{\text{Measurement result} - X}{Z}$$

where X and Z are values entered into stores within the instrument by the operator. X is set to 0 and Z to 1 when the instrument is first switched on. By suitable choice of values for X and Z, ratio, offset (null) and percentage-difference displays can be obtained.

SPECIAL FUNCTIONS

18 A number of special functions are available to the operator. These provide test procedures and operating facilities additional to those available by operation of the front panel controls. Details are given in Section 4 of this manual.

ERROR INDICATION

19 Certain errors in the operation of the instrument will result in the generation of error codes, which will be displayed. Details are given in Section 4 of this manual.

EXTERNAL ARMING

20 External arming of the start and stop circuits for the measurement interval can be carried out by means of signals connected to a socket mounted on the rear panel. Any combination of internal and external arming can be selected by use of the appropriate special function.

DISPLAY FORMAT

21 The display uses an engineering format, with a nine digit mantissa and one exponent digit. Overflow of the most significant digits can be used to increase the display resolution.

HOLD FEATURE

22 The hold feature allows readings to be held indefinitely. A new measurement cycle is initiated using the RESET key.

RESOLUTION AND GATE TIME

23 In the Total A by B and Manual Totalize modes, the counting interval (gate time) is controlled by the time interval between the start and stop signals at the channel B input, or between successive operations of the HOLD key. In the Frequency A, Frequency C, Period A, Ratio A/B and Ratio C/B modes, the gate time is determined by the display resolution selected. In Phase mode, the gate time is fixed and the display resolution is determined by the input signal frequency. Details of the relationship between gate time and resolution for each measurement mode are given in Section 4 of this manual.

EXTERNAL FREQUENCY STANDARD INPUT

24 The instrument may be operated using an external frequency standard. The instrument will operate from the external standard, in preference to the internal standard, whenever the signal at the EXT STD INPUT socket is of sufficient amplitude. It will revert to operation from the internal standard automatically if the input from the external standard is removed.

STANDBY MODE

25 When the instrument is switched to standby, the internal frequency standard continues to operate but the measuring circuits are switched off. If the battery pack option is fitted and an external power supply is connected, the battery is charged at the full rate.

INITIALIZATION

26 When the instrument is first switched on, or when it is initialized via the GPIB, it is set to the following conditions:

Measurement Function	FREQ A
Display Resolution	8 digits
Channel A and B Inputs	Manual trigger AC coupling Negative-slope trigger 1 MΩ input impedance LF filter disabled Common input disabled
Delay	Disabled
Delay Store	200 μs

Math Function	Disabled
X Store	0
Z Store	1
Hold	Disabled
Special Functions	Functions 10, 20, 30, 40, 50, 60, 70 enabled.

OPTIONS AVAILABLE

Frequency Standards (04X Options)

27 A wide range of internal frequency standard options is available. The technical specifications are given in Section 1 of this manual. The frequency standard can be changed, if required, by the customer: instructions are given in Section 3.

Reference Frequency Multiplier (Option 10)

28 The reference frequency multiplier is an internally-mounted, phase-locked multiplier, which permits the use of external frequency standard signals at 1 MHz, 2 MHz, 5 MHz or 10 MHz. The multiplier can be fitted by the customer: instructions are given in Section 3.

GPIB Interface (Option 55)

29 An internally mounted interface to the IEEE-488-GPIB is available. This permits remote control of all the instrument's functions except the power ON/OFF and standby switching. The interface can be fitted by the customer: instructions are given in Section 3. The GPIB interface cannot be fitted to an instrument already fitted with the battery pack option. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an accessory.

Battery Pack (Option 07)

30 Fitting the internal battery permits the instrument to be used in locations where no suitable AC supply is available. The option also allows operation from an external DC supply.

31 The battery is trickle-charged whenever the instrument is operated from an AC supply. Charging at the full rate is carried out when the instrument is switched to the standby mode. A full charge requires approximately 14 hours.

32 The instrument will operate continuously for approximately 4 hours from a fully-charged battery. It will switch off automatically when the battery approaches the discharged condition. The STBY/CHRG indicator starts to flash approximately 15 minutes before this occurs. The battery life can be extended by use of the Battery-Save facility.

33 The battery pack can be fitted by the customer. Instructions are given in Section 3. The battery pack cannot be fitted to an instrument already fitted with the GPIB interface option.

Rack Mounting Kits

34 The following kits, permitting the instrument to be mounted in a standard 19-inch rack are available:

(1) Single instrument, fixed-mount kit (Option 60A).
(Racal-Dana part number 11-1648).
The mounted instrument occupies half the rack width and is two rack units (3.5 inches) in height. The instrument is mounted offset in the rack and may be at either side.

(2) Double instrument, fixed-mount kit (Option 60B).
(Racal-Dana part number 11-1649).
The panel of the mounting kit occupies the full rack width and is two rack units (3.5 inches) in height. Two instruments can be mounted side-by-side.

35 All the kits can be fitted by the customer. Instructions are given in Section 3.

UNPACKING

1 Unpack the instrument carefully to avoid unnecessary damage to the factory packaging.

2 If it becomes necessary to return the instrument to Racal-Dana Instruments for calibration or repair, the original packaging should be used. If this is not possible, a strong shipping container should be used. Ensure that sufficient internal packing is used to prevent movement of the instrument within the container during transit.

POWER SUPPLY

AC Line Voltage Setting

3 Before use, check that the AC voltage selector is set correctly for the local AC supply. The voltage range already set can be seen through a window in the selector board retaining clamp to the left of the AC power plug.

4 If it is necessary to change the setting, proceed as follows:

(1) Undo the selector board retaining clamp on the rear panel.

(2) Withdraw the board.

(3) Replace the board with the required voltage setting positioned so that it will show through the window in the retaining clamp.

(4) Replace the retaining clamp.

Line Fuse

5 Check that the rating of the line fuse is suitable for the AC voltage range in use. The fuse should be of the ¼ in x 1¼ in, glass cartridge, surge-resisting type. The required rating is:

90 V to 127 V: 500 mAT (Racal-Dana part number 23-0052).
193 V to 253 V: 250 mAT (Racal-Dana part number 23-0056).

Power Cord

6 The 1991 and 1992 are Safety Class 1 instruments, and are designed to meet international safety standards. A protective ground terminal, which forms part of the power-input connector on the rear panel, is provided. Each instrument is supplied with a 3-core power cord. Only the power cord supplied should be used to make electrical connection to the power-input connector.

7 AC power for the instrument must be taken from a power outlet incorporating a protective ground connector. When the green/yellow conductor of the power cord is joined to this connector, the exposed metalwork of the instrument is grounded. The continuity of the protective ground connection must not be broken by the use of 2-core extension cords or 3-prong to 2-prong adapters.

8 Connection of the power cord to the power outlet must be made in accordance with the standard color code.

	European	American
Line	Brown	Black
Neutral	Blue	White
Ground (Earth)	Green/Yellow	Green

FUNCTIONAL CHECK

9 The check given in paragraph 11 tests the operation of most of the instrument's circuits to establish whether the instrument is functioning correctly. The procedure should be followed when the instrument is first taken into use, and after transportation to a new location. It does not check that the instrument is operating to the published specification. Detailed specification tests are given in Section 7 of the maintenance manual.

10 A 50Ω coaxial test lead, fitted with BNC connectors is required. This lead must be at least 60 cm, but not more than 1 m long.

11 (1) Connect the instrument to a suitable AC supply.

(2) Switch the instrument on. Check that the instrument type-number appears in the display for approximately two seconds, followed by a number which indicates the software version and issue numbers.

(3) Press the FUNCTION ↓ key until the CHECK indicator lights. Check that the display shows 10.0000000 6 and that the GATE indicator is flashing.

(4) Verify that the RESOLUTION indicator is lit. Press the RESOLUTION ↓ key five times, ensuring that the resolution of the display is decreased by one digit each time.

(5) Press the RESOLUTION ↑ key to increase the resolution to nine digits.

12 If required, the following additional checks may also be performed, using the instrument's special functions.

(1) Press

[7] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF] .

Check that all LEDs, with the exception of TRIG A, TRIG B, GATE and STBY/CHRG flash on and off every two seconds. If the GPIB option is installed, the REM, ADDR and SRQ indicators should be lit.

(2) Connect the 10 MHz STD OUTPUT socket on the rear panel to the front panel INPUT A connector, using the coaxial test lead.

(3) Press

[7] [7] [SHIFT] [STORE] [SF].

Verify that the display shows *0.******* 0 Hz where * indicates a blanked digit. The X10, 50Ω, DC, FILTER and COM A indicators for channel A should light in turn.

(4) Disconnect the coaxial lead from the INPUT A connector. The display should show an error number after a few seconds.

(5) Connect the coaxial lead to the INPUT B connector.

(6) Press

[7] [8] [SHIFT] [STORE] [SF].

Check that the display shows *0.******* 0 Hz. The X10, 50Ω and DC indicators for channel B should light in turn.

(7) Disconnect the coaxial lead from the INPUT B connector and the 10 MHz STD OUT connector. The display should show Er 56.

(8) Switch the instrument off.

FREQUENCY STANDARD

13 If it is intended to use an external frequency standard, the output of the frequency standard should be connected to the EXT STD INPUT connector on the rear panel of the instrument. The connection should be made using coaxial cable. Switch on the frequency standard and the instrument: check that the EXT STD indicator on the front panel of the instrument lights.

14 A 10 MHz signal, derived from the frequency standard in use, is available at the 10 MHz STD OUT connector on the rear panel of the instrument. If this signal is used, the connection should be made using coaxial cable.

EXTERNAL ARMING

15 If external arming is to be used, the arming signal should be connected to the EXT ARM INPUT connector on the rear panel.

TRIGGER LEVEL OUTPUT

16 The trigger levels in use on channels A and B are available via pins on the instrument rear panel. If required, connection to the pins should be made using a clip-on probe or small crocodile clip.

PREPARATION FOR USE WITH THE GPIB

Introduction

17 The instrument must be prepared for use in accordance with the instructions given in Paragraphs 3 to 8 before the instructions given in this section are implemented.

Connection to the GPIB

18 Connection to the GPIB is made via a standard IEEE-488 connector, mounted on the rear panel. The pin assignment is given in Table 3.1. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an optional accessory.

TABLE 3.1

GPIB Connector Pin Assignment

Pin	Signal Line	Pin	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd (6)
7	NRFD	19	Gnd (7)
8	NDAC	20	Gnd (8)
9	IFC	21	Gnd (9)
10	SRQ	22	Gnd (10)
11	ATN	23	Gnd (11)
12	SHIELD	24	Gnd (5 and 17)

Address Setting and Display

19 The interface address is set using five switches, A1 to A5, which are mounted on the rear panel. The permitted address settings, in binary, decimal and ASCII character form, are given in Table 3.2. The GPIB address set can be displayed, in decimal form, by pressing

[SHIFT] [RECALL] [LOCAL] .

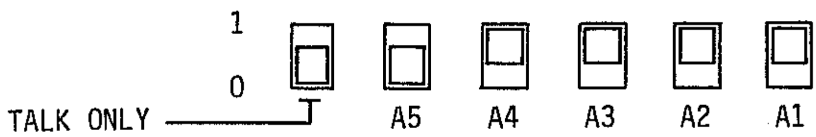
If the address is changed, this key sequence must be repeated to display the new address. The instrument is returned to the measurement mode by pressing

[CONTINUE] .

20 For addressed operation, the TALK ONLY switch must be in the logic '0' position (down). When this switch is in the logic '1' position, the interface is switched to the talk-only mode. The settings of switches A1 to A5 are then irrelevant.

TABLE 3.2

Address Switch Settings



SWITCH SETTINGS					ADDRESS CODES		
A5	A4	A3	A2	A1	DECIMAL	ASCII LISTEN ADDRESS	ASCII TALK ADDRESS
0	0	0	0	0	0	SP	@
0	0	0	0	1	1	!	A
0	0	0	1	0	2	"	B
0	0	0	1	1	3	#	C
0	0	1	0	0	4	$	D
0	0	1	0	1	5	%	E
0	0	1	1	0	6	&	F
0	0	1	1	1	7	'	G
0	1	0	0	0	8	(	H
0	1	0	0	1	9	)	I
0	1	0	1	0	10	*	J
0	1	0	1	1	11	+	K
0	1	1	0	0	12	,	L
0	1	1	0	1	13	-	M
0	1	1	1	0	14	.	N
0	1	1	1	1	15	/	O
1	0	0	0	0	16	Ø	P
1	0	0	0	1	17	1	Q
1	0	0	1	0	18	2	R
1	0	0	1	1	19	3	S
1	0	1	0	0	20	4	T
1	0	1	0	1	21	5	U
1	0	1	1	0	22	6	V
1	0	1	1	1	23	7	W
1	1	0	0	0	24	8	X
1	1	0	0	1	25	9	Y
1	1	0	1	0	26	:	Z
1	1	0	1	1	27	;	[
1	1	1	0	0	28	<	\
1	1	1	0	1	29	=	]
1	1	1	1	0	30	>	^

GPIB CHECK

21 The procedure which follows checks the ability of the instrument to accept, process and send GPIB messages. The correct functioning of the instrument under local control should be verified before the procedure is attempted.

22 The recommended test equipment is the Hewlett-Packard HP-85 GPIB controller, with the I/O ROM in the drawer. It is assumed that the select code of the controller I/O port is 7, and that the address of the instrument is 15 (to change the address, see Paragraph 19). If any other controller or select code/address combination is used, the GPIB commands given in the following paragraphs will require modification. The controller should be connected to the GPIB interface of the instrument via a GPIB cable. No connection should be made to the channel A, B or C inputs.

23 Successful completion of the GPIB check proves that the instrument's GPIB interface is operating correctly. The procedure does not check that all the device-dependent commands can be executed. However, if the GPIB interface works correctly and the instrument operates correctly under local control, there is a high probability that it will respond to all device-dependent commands.

Remote and Local Message Check

24 Switch the instrument on. Check that the REM, ADDR and SRQ indicators flash on and off once. If the indicators do not flash, or if they flash continuously, there is a fault on the GPIB board.

25 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 715	

Check that the REM indicator lights.

26 Test as follows:

Action	HP-85 Code	Your Controller
Send the device-dependent command CK	OUTPUT 715; "CK"	

Check that the ADDR indicator lights and that the Check mode is selected.

27 Test as follows:

Action	HP-85 Code	Your Controller
Send the instrument's listen address followed by the GTL message	LOCAL 715	

Check that the REM indicator is off. The ADDR indicator will also be off if the controller used sends the unlisten message (UNL) true automatically. This is the case when using the HP-85.

Local Lockout and Clear Lockout Check

28 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 715	
Send the LLO message	LOCAL LOCKOUT 7	

Check that the REM indicator lights. Operate the LOCAL key on the front panel and verify that the REM indicator remains lit.

29 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message false	LOCAL 7	

Check that the REM indicator is off.

30 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 715	

Check that the REM indicator lights. Press the LOCAL key and verify that the REM indicator turns off.

Data Output Check

31 Test as follows:

Action	HP-85 Code	Your Controller
Set the instrument to the check mode by sending the listen address, followed by the device-dependent command CK	OUTPUT 715; "CK"	
Prepare a store to receive a 21-byte data string	DIM Z$ [21]	
Send the instrument's talk address. Store the 21-byte data string in the prepared store	ENTER 715; Z$	
Display the contents of the store	DISP Z$	

Check that the display reads CK+0010.0000000E+06 with the cursor moved to the next line, indicating that carriage return (CR) and line feed (LF) have been accepted.

SRQ and Status Byte Check

32 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true	REMOTE 7	
Set the instrument to send the SRQ message when an error is detected, and force the generation of error code 05 by sending the device-dependent commmand XXX	OUTPUT 715;"IPXXX"	
Store the status of the GPIB interface of the controller, in binary form, as variable T	STATUS 7, 2; T	
Display the status of the SRQ line	DISP"SRQ=";BIT(T,5)	

Check that the HP-85 displays SRQ=1, the SRQ status bit is at logic '1' or the SRQ line is $\leqslant$0.8 V. Check that the SRQ indicator on the instrument is lit.

33 Test as follows:

Action	HP-85 Code	Your Controller
Conduct a serial poll and store the status byte as variable R	R = SPOLL (715)	
Display variable R	DISP "R="; R	

Check that the SRQ indicator is turned off when the serial poll is made. The value of R should be 101 (in binary form, R should be 0000000001100101). If using an HP-85 controller, check that the ADDR indicator is turned off.

Device Clear and Selected Device Clear Check

34 Test as follows:

Action	HP-85 Code	Your Controller
Set the instrument to the Total A by B mode by sending the listen address, followed by the device-dependent command TA	OUTPUT 715;"TA"	
Send the DCL message true	CLEAR 7	

Check that the function indicated on the instrument front panel changes to FREQ A.

35 Test as follows:

Action	HP-85 Code	Your Controller
Reset the instrument to the Total A by B mode by sending the listen address, followed by the device-dependent command TA	OUTPUT 715;"TA"	
Send the SDC message true	CLEAR 715	

Check that the function indicated on the instrument front panel changes to FREQ A.

IFC Check

36 Test as follows:

Action	HP-85 Code	Your Controller
Send the ATN message false Send the IFC message true	RESUME 7 ABORTIO 7	

Check that the ADDR indicator is turned off.

TALK ONLY Selector Test

37 (1) Set the TALK ONLY switch in the instrument rear panel to '1'. Check that the REMOTE indicator is turned off and the ADDR indicator lights.

(2) Set the TALK ONLY switch to '0'. Check that the ADDR indicator turned is off.

OPTION FITTING INSTRUCTIONS

Single-Instrument Fixed Rack Mounting Kit 11-1648 (Option 60A)

38 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	1	16-0643
Long mounting bracket	1	16-0644
Screw, M4 x 16	4	24-7733
Crinkle washer M4	4	24-2802
Spacer, plain M4x5	4	24-4112
Screw, M6 x 16	4	24-7995
Cup washer, M6	4	24-2809
Caged nut, M6	4	24-2240

39 Assemble the kit to the instrument as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the bottom cover by sliding it towards the rear of the instrument.

(4) Remove the instrument's feet from the bottom cover.

(5) Replace the bottom cover. Replace and secure the bezel.

(6) Remove the four blind grommets from the sides of the instrument. This will reveal two threaded holes in each side frame.

(7) At one side of the instrument, secure a mounting bracket to the side frame, using two spacers, M4 screws and crinkle washers. Position the spacers between the mounting bracket and the side frame.

(8) Repeat step (7) at the other side of the instrument.

(9) Fit the cup washers to the M6 screws. Offer the instrument up to the rack in the required position, and secure the brackets to the rack using the M6 screws and nuts.

Double-Instrument Fixed Rack Mounting Kit 11-1649 (Option 60B)

40 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	2	16-0643
Screw, M4 x 16	4	24-7733
Crinkle washer, M4	4	24-2802
Spacer, plain, M4 x 5	4	24-4112
Spacer, female	2	14-1583
Spacer, male	2	14-1584
Mating plate	1	13-2000
Rivet, plastic	4	24-3211
Screw, M6 x 16	4	24-7995
Cup washer, M6	4	24-2809
Caged nut, M6	4	24-2240

41 Prepare both instruments as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the bottom cover by sliding it towards the rear of the instrument.

(4) Remove the instrument's feet from the bottom cover.

(5) Replace the bottom cover. Replace and secure the bezel.

(6) Remove the four blind grommets from the sides of the instrument. This will reveal two threaded holes in each side frame.

(7) Remove two buffers from the bezel at the side which is to be at the centre of the rack.

42 Assemble the kit to the instruments as follows:

(1) At the sides which are to be at the centre of the rack, secure the female spacers to one instrument and the male spacers to the other. The spacers screw into the threaded holes in the side frames.

(2) At the other side of each instrument, secure a mounting bracket to the side frame, using two plain spacers, M4 screws and crinkle washers. Position the spacers between the mounting bracket and the side frame.

(3) Fit the male spacers on one instrument into the female spacers on the other.

(4) Position the mating plate to bridge the gap between the bezels. Secure it by pushing the plastic rivets through the plate into the buffer holes.

(5) Fit the cup washers to the M6 screws. Offer the two instruments up to the rack in the required position, and secure the brackets to the rack using the M6 screws and nuts.

PCB-Mounted Frequency Standard, 11-1713 (Option 04T)

43 The kit comprises:

Item	Qty	Racal-Dana Part Number
Plate assembly	1	11-1610
Oscillator PCB	1	19-1208
Crinkle washer M3	3	24-2801
Screw, M3 x 6	3	24-7721

Installation

44 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the frequency standard already fitted. Instructions are given in Paragraph 45 or Paragraph 48, according to type.

(5) Secure the PCB to the plate assembly, using an M3 screw and washer from the kit. The screw should be passed through the mounting hole in the board and screwed into the threaded spacer of the plate assembly. The component side of the board should be towards the plate assembly.

(6) Connect the PCB to the motherboard at PL14, with the plate assembly towards the rear panel of the instrument.

(7) Secure the plate assembly to the rear panel, using two M3 screws and washers. The screws pass through the holes adjacent to the FREQ STD ADJUST aperture and screw into the plate assembly.

(8) Replace the top cover. Replace and secure the bezel.

Removal

45 (1) Remove the two screws adjacent to the FREQ STD ADJUST aperture in the rear panel.

(2) Pull the PCB and plate assembly upwards until the board is disconnected from the motherboard.

Ovened Frequency Standards 11-1710 and 11-1711 (Options 04A and 04B)

46 The kit comprises:

Item	Qty	Racal-Dana Part Number
Oscillator assembly	1	9444 for 11-1710 9423 for 11-1711
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

Installation

47 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the frequency standard already fitted. Instructions are given in Paragraph 45 or Paragraph 48, according to type.

(5) Connect the flying lead on the oscillator assembly to SK14 on the motherboard.

(6) Secure the oscillator assembly to the rear panel of the instrument, using the M3 screws and washers. The screws pass through the holes adjacent to the FREQ STD ADJUST aperture and screw into the oscillator assembly.

(7) Replace the top cover. Replace and secure the bezel.

Removal

48 (1) Remove the two screws adjacent to the FREQ STD ADJUST aperture in the rear panel.

(2) Lift the oscillator assembly out of the chassis and disconnect the flying lead from the motherboard at PL14.

Reference Frequency Multiplier Option 11-1645 (Option 10)

49 The kit comprises:

Item	Qty	Racal-Dana Part Number
Frequency multiplier	1	19-1164
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

50 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the frequency standard if an ovened type is fitted.

(5) Remove the shorting link from between pins 8 and 9 on PL16.

NOTE: This link should be stored in a safe place. It must be replaced if Option 10 is removed from the instrument.

(6) Connect the frequency multiplier PCB to the motherboard at PL16 and PL17, with the threaded spacers towards the right-hand side frame.

(7) Secure the PCB to the side frame, using the M3 screws and washers.

(8) Replace and secure the frequency standard if it was removed in (5).

(9) Replace the top cover. Replace and secure the bezel.

GPIB Option 11-1626 (Option 55)

51 The kit comprises:

Item	Qty	Racal-Dana Part Number
GPIB board assembly	1	19-1146
Shakeproof washer, M3	2	24-2813
Screw, M3 x 6	2	24-7721

NOTE 1:
This option cannot be fitted to an instrument already fitted with the battery pack option.

NOTE 2:
The software version number (the first part of the decimalised number) on the GPIB ROM (IC10) must be the same as that for the main instrument ROM (IC22 on the motherboard).

52 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the blanking plate from the rear panel by pushing out the plastic rivets from the inside of the instrument.

(5) Hold the GPIB board, component side down, with the GPIB connector towards the rear panel. Connect the ribbon cable to the motherboard at SK4.

(6) Tilt the board, and lower it into the instrument. Position it with the support brackets just below the top flanges of the side frames.

(7) Slide the board towards the rear panel so that the support brackets enter the grooves immediately below the top flanges of the side frames.

(8) Secure the bracket which carries the GPIB connector to the rear panel using the M3 screws and washers.

NOTE:
The screws and washers provide the ground connection between the GPIB connector and the instrument chassis. Tighten the screws firmly to ensure that a good connection is obtained.

(9) Replace the top cover. Replace and secure the bezel.

Battery Pack Option 11-1625 (Option 07)

53 The kit comprises:

Item	Qty	Racal-Dana Part Number
PCB assembly	1	11-1722
Mounting bracket	1	11-1599
Battery pack	1	11-1723
Cover plate	1	13-2040
Crinkle washers, M3	2	24-2801
Screws, M3	2	24-7721
Crinkle washers, M4	6	24-2802
Plain washers, M4	2	24-2705
Screws, M4	6	24-7730
Spare fuse, 3AT	1	23-0069

NOTE:
This option cannot be fitted to an instrument already fitted with the GPIB interface option.

54 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the blanking plate from the rear panel by pushing out the plastic rivets from the inside of the instrument.

(5) If a PCB-mounted frequency standard is fitted, remove the two screws adjacent to the FREQ STD ADJUST aperture.

(6) Remove the four screws which secure the rear panel to the side frames.

(7) Ease the rear panel away from the instrument until it disconnects from the motherboard at PL19 and PL20.

(8) Hold the PCB assembly with the switches towards the rear of the instrument and the PCB connector pointing downwards.

(9) Lower the assembly into the chassis and connect the PCB to the motherboard at PL21, taking care that it mates correctly.

(10) Replace and secure the rear panel.

(11) If a PCB-mounted frequency standard is fitted, secure it to the rear panel with the screws removed in (5).

(12) Position the cover plate over the switches protruding through the rear panel. Secure the cover plate and the rear panel to the PCB assembly, using the M3 screws and washers.

(13) Secure the mounting bracket to the right-hand side frame, using two M4 screws and washers. The horizontal flange should be towards the top of the instrument.

(14) Position the battery pack within the chassis, with the supporting lugs resting on the mounting bracket. Secure the battery pack to the left-hand side frame, using two M4 screws and washers.

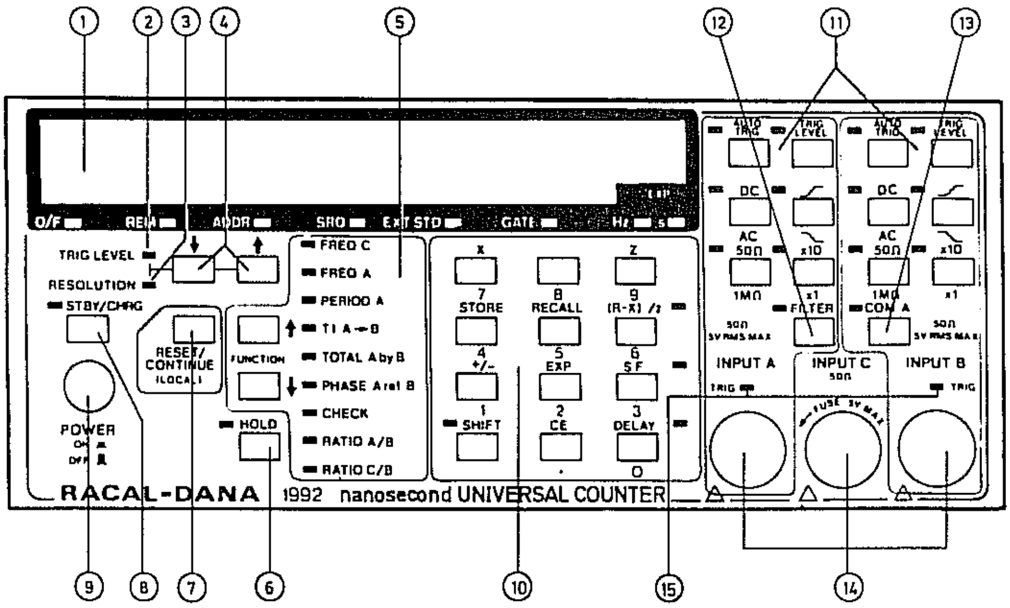
(15) Secure the supporting lugs to the mounting bracket, using M4 screws and washers.

(16) Connect the flying lead on the battery pack to the connector on the PCB assembly.

(17) Replace the top cover. Replace and secure the bezel.

INTRODUCTION

1 The instrument should be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the AC voltage selector.



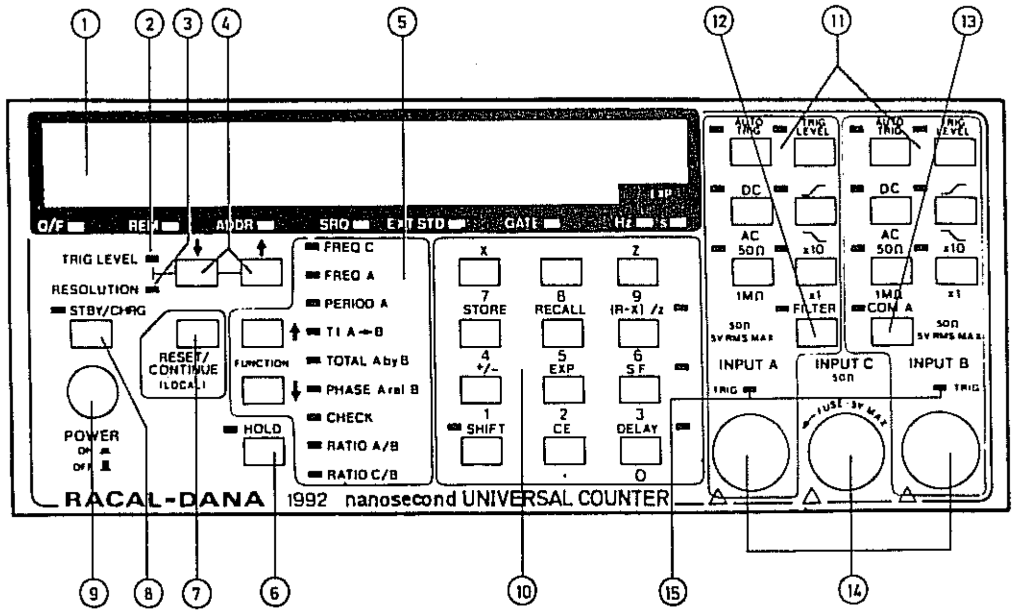
DESCRIPTION OF CONTROLS, INDICATORS AND CONNECTORS

Front Panel Items

2

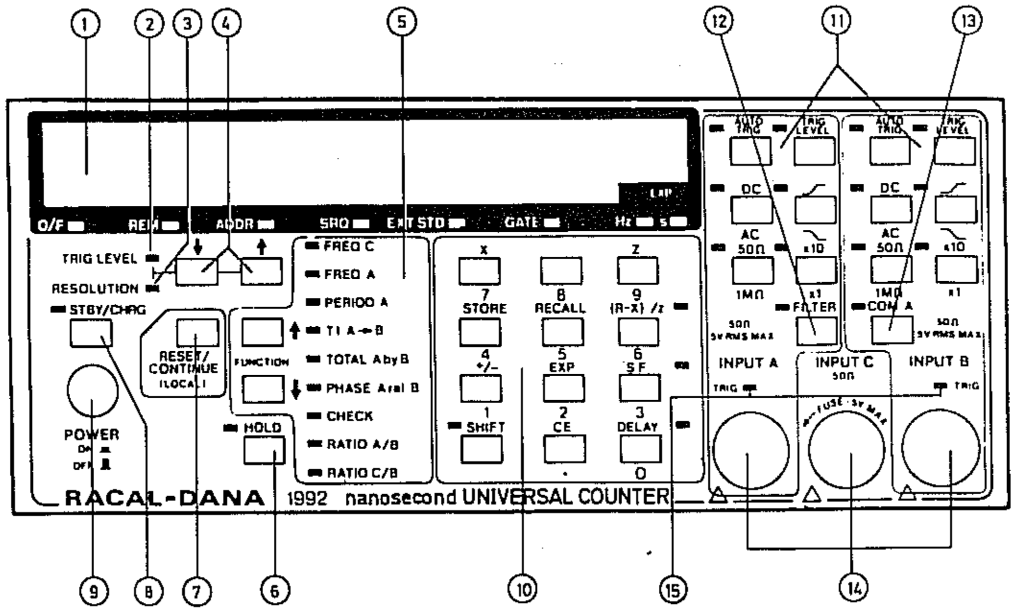
Reference	Item	Description
①	Display	A 7-segment, LED, digital display, used to display: (1) The result of a measurement. (2) A number awaiting entry into an internal store. (3) A number recalled from an internal store. (4) Error indications.

Reference	Item	Description
		The display format is in engineering format, with a 9-digit mantissa and a 1-digit exponent. The exponent is normally a multiple of three. The exponent digit is blanked, and should be assumed to be zero, for: (1) Display of phase mode measurement results. (2) Totalize measurement results having less than ten digits. (3) Numbers not involving an exponent which have been entered using the numeric keypad.
	O/F Indicator	Lights when the measurement result has overflowed the ninth digit of the display.
	REM Indicator	Lights when the instrument is operating under remote control.
	ADDR Indicator	Lights when the instrument is acting as a listener or as a talker.
	SRQ Indicator	Lights when the instrument generates a service request.
	EXT STD Indicator	Lights when the instrument is operating from an external frequency standard.
	GATE Indicator	Lights while a measurement cycle is in progress.
	Display Units Indicators	The Hz indicator lights for a frequency display. The s indicator lights for a time display. Neither indicator lights for a display of phase angle, ratio, total, trigger level or a number.
(2)	TRIG LEVEL Control Indicator	Lights when a trigger level is being displayed. The displayed trigger level can be stepped up or down using the ↑ and ↓ keys, or can be changed using the numeric keyboard.



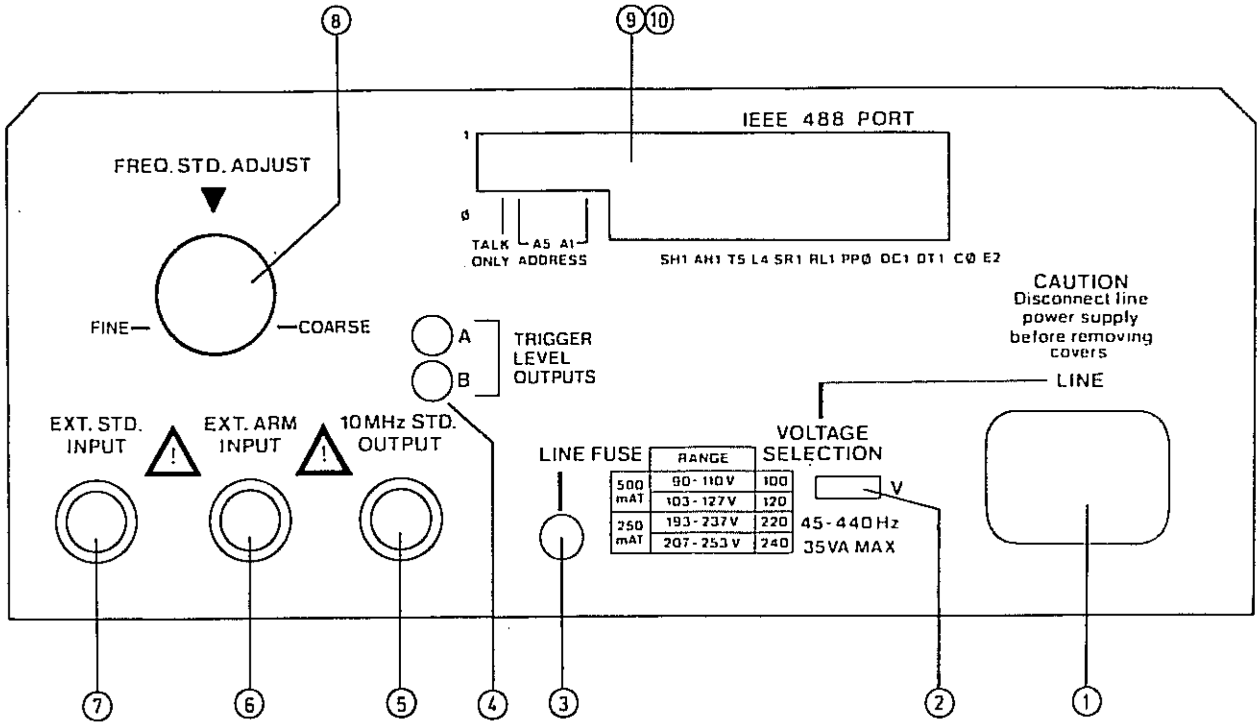
Reference	Item	Description
(3)	RESOLUTION Control Indicator	Lights to show that the resolution of the display, and, therefore, the measurement period (gate time) can be changed by means of the ↑ or ↓ control keys.
(4)	Step-Up ↑ and Step-Down ↓ Keys	Used to step the display resolution or the displayed value of trigger level up or down.
(5)	Function Selector	The functions can be selected in turn using the FUNCTION ↑ and ↓ keys. The function selection 'wraps round' at both ends.
(6)	HOLD Key	Successive operations put the instrument into and out of the Hold (single-shot measurement) mode. The indicator lights when the instrument is in the Hold mode. Readings are triggered using the RESET key. When the instrument is in the Manual Totalize mode (using special function 61) successive operations of the key start and stop the measurement cycle.

Reference	Item	Description
(7)	RESET/CONTINUE (LOCAL) Key	This key has three functions. RESET Clears the display and triggers a new measurement cycle when the instrument is in the measurement mode. CONTINUE Returns the instrument to the measurement mode and triggers a measurement cycle, following the display of a number recalled from store. It can also be used to clear the OP Er indication. LOCAL Returns the instrument to local control from remote GPIB control provided local lockout is not set.
(8)	STBY/CHRG Key	Successive operations switch the instrument into and out of the standby state. The indicator lights when the instrument is in the standby state. If the battery pack option is installed the indicator flashes when the battery approaches the discharged state. The battery is charged at the full rate when the instrument is in standby and external power is applied.
(9)	POWER Switch	Controls the AC or DC power to the instrument.
(10)	Numeric Keypad	Used to enter numbers into, and recall numbers from, the instrument's internal stores. Also used to enable and disable the math function, the special functions and the stop circuit arming delay (hold off).



Reference	Item	Description
(11)	Measurement Channel Controls	The A and B channels have identical control keys.
	AUTO TRIG Key	Used to select auto-trigger level or manual trigger level. The indicator lights when auto-trigger level is selected.
	TRIG LEVEL Key	Successive operations display the trigger level in use and store the displayed trigger level. The indicator flashes when the trigger level is being displayed. (The trigger level control indicator (2) will also light).
	AC/DC Key	Used to select AC or DC coupling of the input signal. The indicator lights when DC coupling is selected.
	Trigger Slope Key	Used to select the positive-going, ⁄ or negative-going, \ , edge of the input waveform for triggering. The indicator lights when the positive-going edge is selected.
	50 Ω/1 MΩ Key	Used to select 50 Ω or 1 MΩ input impedance. The indicator lights when 50 Ω is selected.

Reference	Item	Description
	X10/X1 Key	Used to select attenuation of the input signal. With X10 selected the input is attenuated by a factor of 10. The indicator lights when X10 is selected.
(12)	FILTER Key	Successive operations enable and disable the channel A input filter. The indicator lights when the filter is enabled.
(13)	COM A Key	Used to connect the channel A input to channels A and B in parallel (common configuration). The indicator lights when the common configuration is selected. The channel A AUTO TRIG key controls both channels, the channel B AUTO TRIG key being rendered inoperative. The channel B AUTO TRIG indicator follows the state of the channel A indicator. Both channels adopt the same trigger level with auto-trigger level selected. Different trigger levels can be set in the two channels when manual trigger level is selected. The channel A 50 Ω/1 MΩ, X10/X1 and DC/AC keys control both channels. The channel B X10/X1 and DC/AC indicators follow the state of the channel A indicators. The channel B 50 Ω/1 MΩ indicator continues to show the impedance of the channel B input.
(14)	Input Connectors	All inputs are BNC connectors.
(15)	TRIG Indicators	Channels A and B are provided with trigger indicators. (1) Indicator permanently lit. Trigger level too low or signal input held in high state. (2) Indicator flashing. Channel being triggered. (3) Indicator permanently off. Trigger level too high or signal input held in low state.

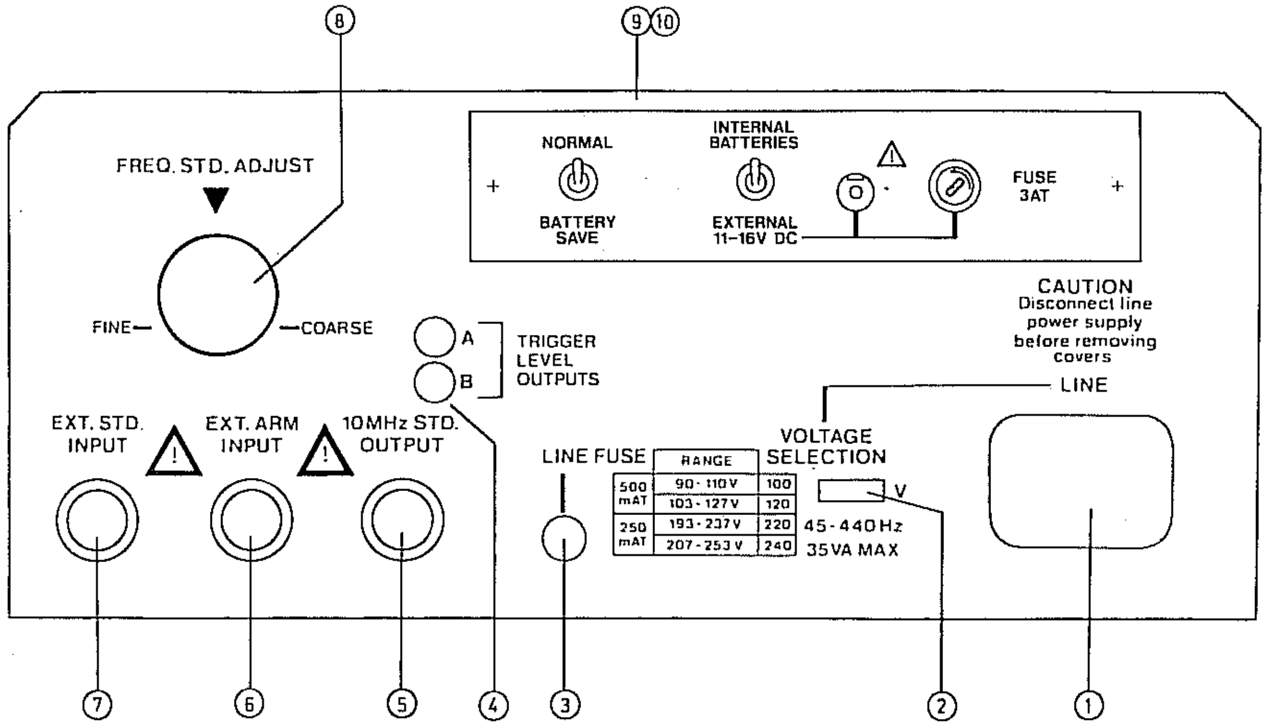


Rear Panel Items

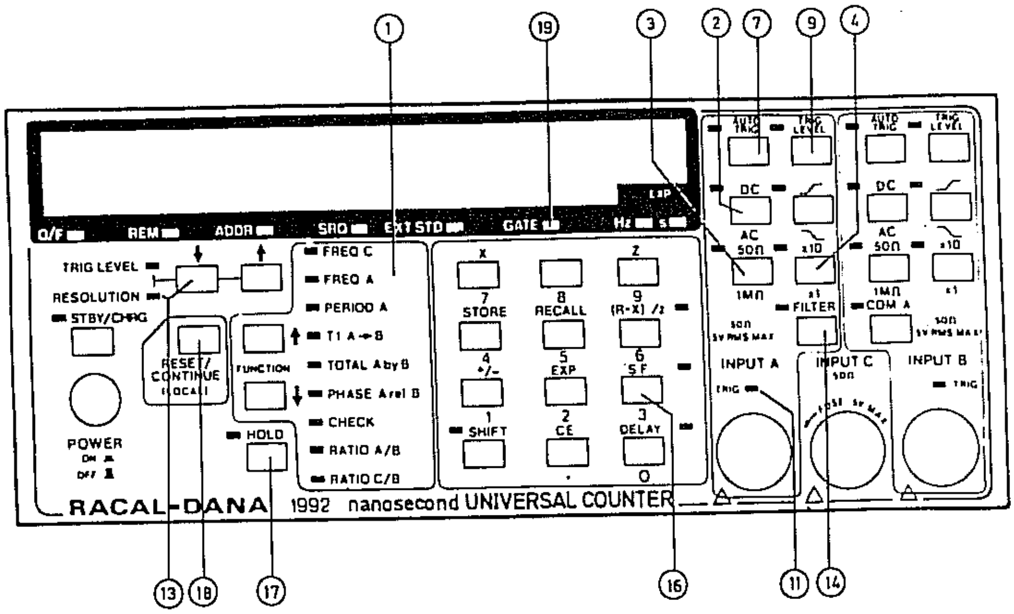
3

Reference	Item	Description
①	AC Power Input Plug	A standard connector for the AC power supply. A RFI filter is incorporated.
②	Line Voltage Selector	Voltage selection is changed by repositioning a printed circuit board inside the instrument. The voltage selected can be seen through the window.
③	Line Fuse	A $\frac{1}{4}$ in x 1$\frac{1}{4}$ in, anti-surge, glass cartridge fuse. The required fuse ratings for different line voltage ranges are shown on the panel and in Section 3 of this manual.
④	Trigger Level Output	The trigger levels in use on the channels A and B are available at two pins. The voltage range is ±5.1 V, regardless of whether or not the X10 attenuator is selected.

Reference	Item	Description
5	10 MHz STD OUTPUT	A BNC connector, providing a 10MHz signal locked to the frequency standard in use.
6	EXT ARM INPUT	A BNC connector for accepting external arming signals.
7	EXT STD INPUT	A BNC connector for connecting an external frequency standard. The instrument will operate from the external frequency standard whenever a signal of suitable frequency and amplitude is applied. The frequency required is 10 MHz unless the reference frequency multiplier option is fitted. With this option, frequencies of 1 MHz, 2 MHz, 5 MHz and 10 MHz are acceptable.
8	FREQ. STD. ADJUST	This aperture provides access to allow adjustment of the internal frequency standard.
9	GPIB Option	
	GPIB Address Switches	Switches A1 to A5 define the listen and talk addresses for GPIB operation in the addressed mode. The talk-only switch must be in the 'Ø' position. With the talk-only switch in the '1' position the instrument is set to the talk-only condition. The positions of switches A1 to A5 are then irrelevant.
	GPIB Connector	An IEEE-488-1978 standard connector used to connect the instrument to the GPIB. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an accessory.



Reference	Item	Description
(10)	Battery-Pack Option	
	DC Power Input Plug	Permits the instrument power to be derived from an external DC supply.
	Battery NORMAL/SAVE Switch	Used to select the Battery-Save facility.
	INTERNAL/EXTERNAL DC Supply Switch	Used to select operation from the internal battery or an external DC supply
	DC Supply Fuse	A ¼ in x 1¼ in glass cartridge fuse of the anti-surge type. The required rating is 3 AT.



FREQUENCY MEASUREMENT

4 (1) Switch the power on.

(2) Select the FREQ A or FREQ C (Model 1992 only) measurement mode, using the function selector (1) .

(3) If channel A is to be used, set the AC/DC coupling (2) , input impedance (3) , and attenuator (4) as required.

(4) Connect the signal to be measured to the channel A or C input.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) If channel A is used, select auto-trigger (7), or set the manual trigger level to the required value (9) . Check that the channel A TRIG indicator (11) flashes.

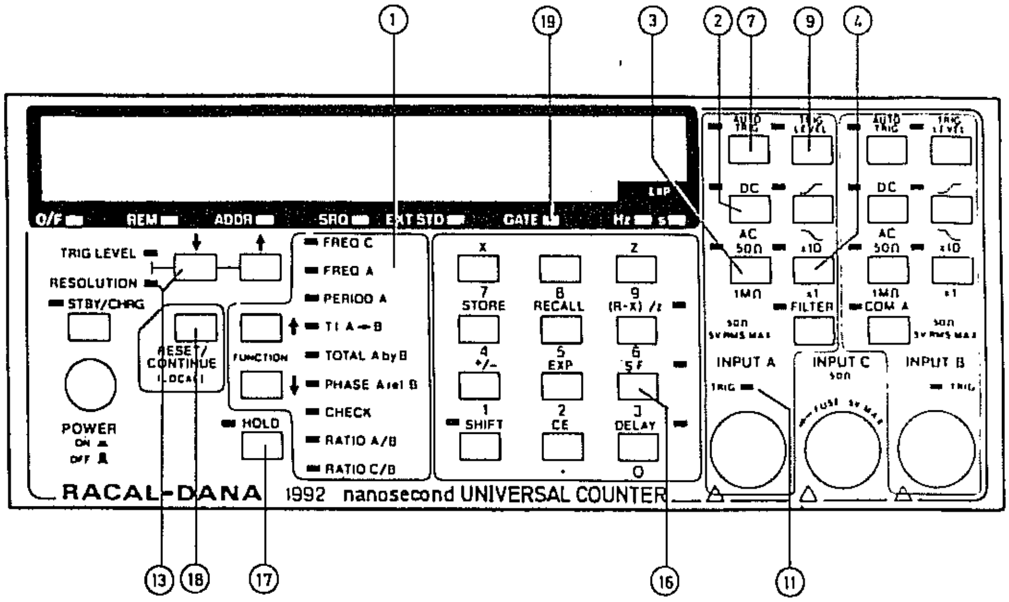
(6) Select the required display resolution (13) .

(7) If a frequency below 50 kHz is to be measured in the presence of noise, enable the filter (14) .

(8) If external arming is to be used, connect the arming signal and enter the required special function number. Enable the special functions (16) .

(9) If operation in the hold mode is required, select HOLD (17) and press the RESET key (18) .

(10) Check that the GATE indicator (19) flashes on during the measurement period.



PERIOD MEASUREMENT

5 (1) Switch the power on.

(2) Select the PERIOD A measurement mode, using the function selector (1).

(3) Set the AC/DC coupling (2), input impedance (3), and attenuator (4) for channel A, as required.

(4) Connect the signal to be measured to the channel A input.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

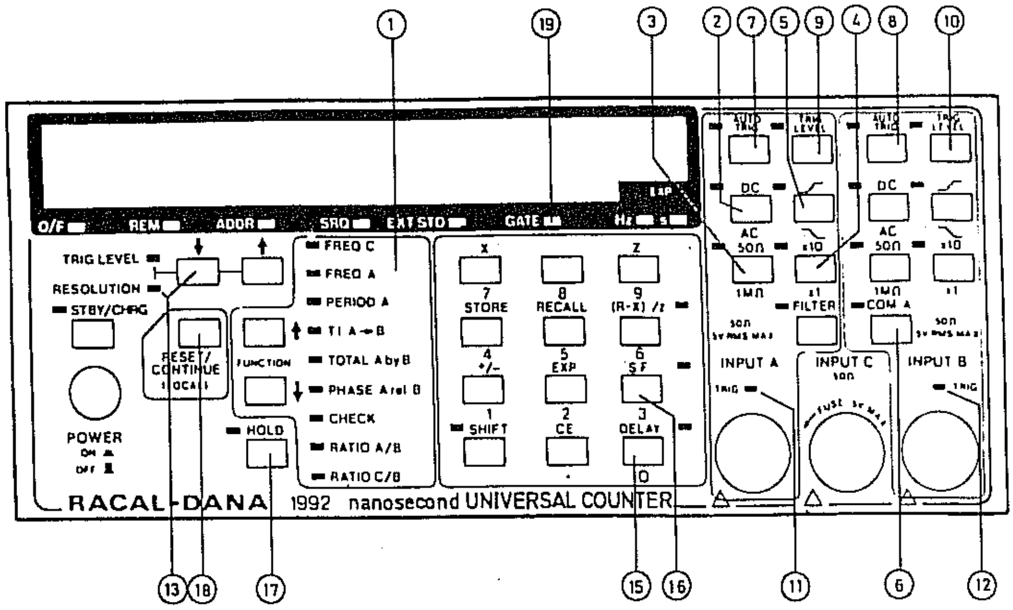
(5) Select auto-trigger (7), or set the manual trigger level to the required value (9). Check that the channel A TRIG indicator 11 flashes.

(6) Select the required display resolution (13).

(7) If external arming is to be used, connect the arming signal and enter the required special function number. Enable the special functions (16).

(8) If hold mode operation is required, select HOLD (17) and press the RESET key (18).

(9) Check that the GATE indicator (19) flashes on during the measurement period.



TIME INTERVAL MEASUREMENT

6 (1) Switch the power on.

(2) Select the T.I. A → B measurement mode, using the function selector ①.

(3) Set the AC/DC coupling ②, input impedance ③, attenuator ④, and slope ⑤, as required. If the start and stop signals are from the same source, select COM A ⑥.

(4) Connect the start signal to the channel A input. If a separate stop-signal source is used, connect the stop signal to the channel B input and set the associated input controls.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNALS DO NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Select auto-trigger ⑦ ⑧, or set the manual trigger levels to the required values ⑨ ⑩. Check that the TRIG indicators ⑪ ⑫ flash.

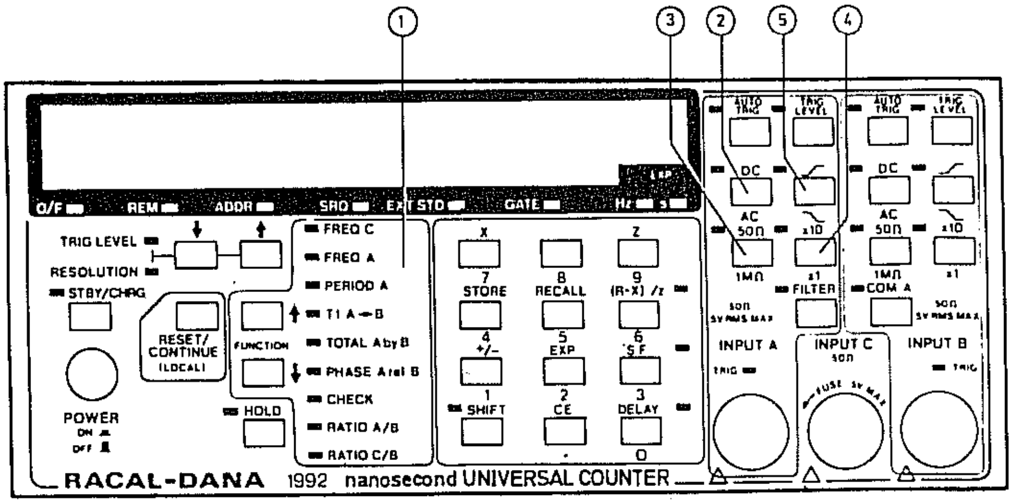
(6) Select the required display resolution ⑬.

(7) If a delay to the stop circuit is required, enter the required delay in the delay store and enable the delay ⑮.

(8) If external arming is be used, connect the arming signal and enter the required special function number. Enable the special functions ⑯.

(9) If hold mode operation is required, select HOLD ⑰ and press the RESET key ⑱.

(10) Check that the GATE indicator ⑲ flashes on during the measurment period.



TOTALIZE MEASUREMENT

Total A by B

7 (1) Switch the power on.

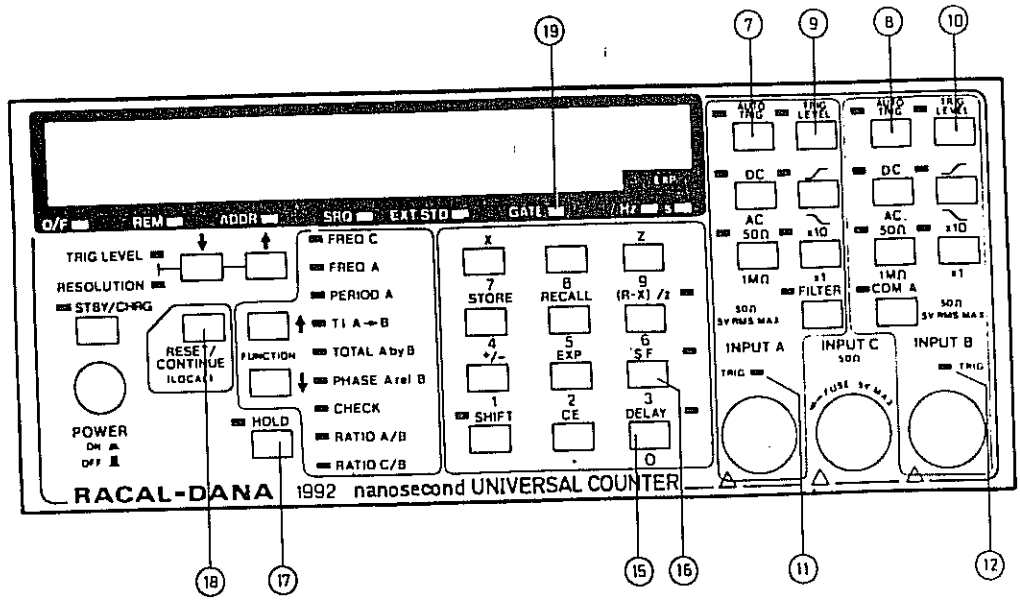
(2) Select the TOTAL A by B measurement mode using the function selector ① .

(3) Set the AC/DC coupling ② , input impedance ③ , attenuator ④ and slope ⑤ as required for both channels.

NOTE:
The channel A slope switch selects the slope of the events which are counted. The measurement period starts on the slope of the B channel signal selected by the channel B slope switch, and stops on the opposite slope.

(4) Connect the signal to be totalized to the channel A input and the control signal to the channel B input.

CAUTION: SIGNAL LEVELS
ENSURE THAT THE SIGNAL LEVELS DO NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.



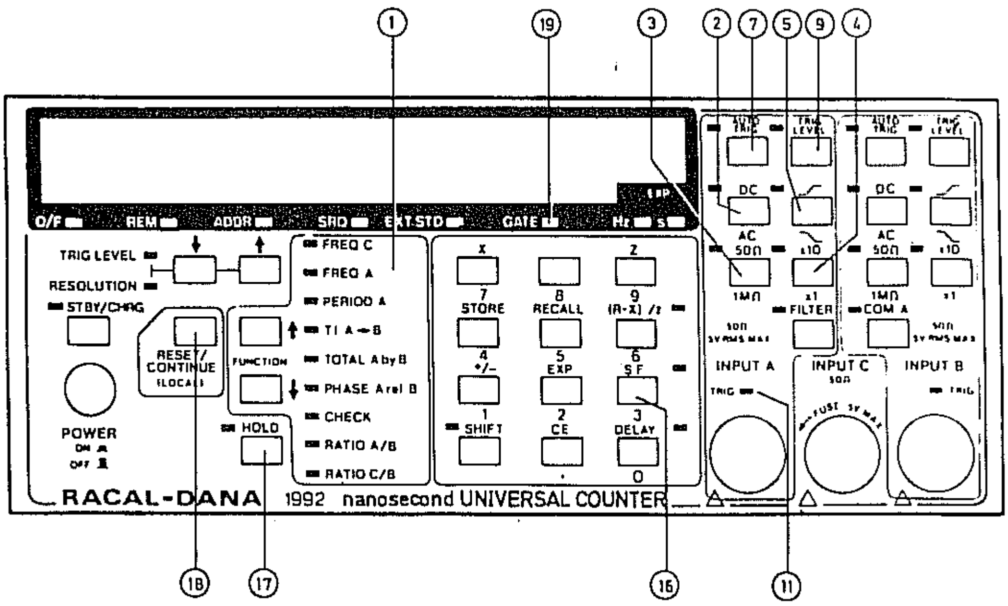
(5) Select auto-trigger ⑦ ⑧ , or set the manual trigger levels to the required values ⑨ ⑩. Check that the TRIG indicators ⑪ ⑫ flash.

(6) If a delay to the stop circuit is to be used, enter the required delay into the delay store and enable the delay ⑮ .

(7) If external arming is to be used, connect the arming signal and enter the required special function number. Enable the special functions ⑯ .

(8) If hold mode operation is required, select HOLD ⑰ and RESET ⑱ .

(9) Trigger a measurement cycle. Check that the GATE indicator ⑲ flashes on during the measurement period.



Manual Totalize

8 (1) Switch the power on.

(2) Select the TOTAL A by B measurement mode, using the function selector (1) .

(3) Set the AC/DC coupling (2) , input impedance (3) , attenuator (4) and slope (5) of channel A as required.

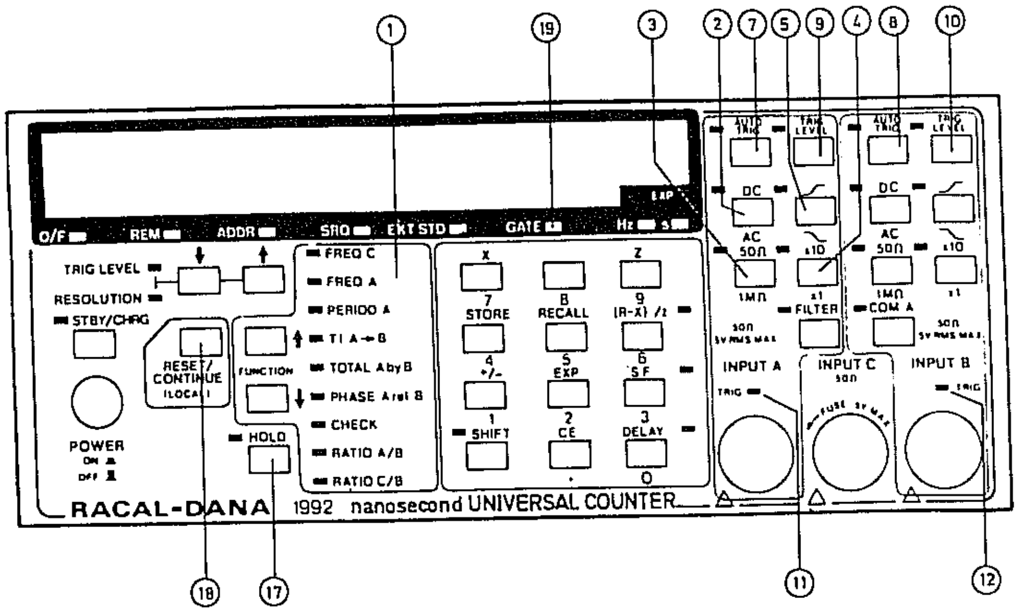
(4) Enter 61 in the special function register and enable the special functions (16) . The HOLD indicator (17) will light.

(5) Connect the signal to be totalized to the channel A input.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(6) Select auto-trigger (7) , or set the manual trigger level to the required value (9). Check that the TRIG indicator (11) flashes.

(7) Start and stop a measurement using the HOLD key (17) . The HOLD indicator will be turned off and the GATE indicator (19) will light during the measurement period. The displayed result is cumulative over successive measurement cycles. If required, clear the display after a measurement cycle by pressing the RESET key (18) .



PHASE MEASUREMENT

9 (1) Switch the power on.

(2) Select the PHASE A rel B measurement mode, using the function selector (1) .

(3) Set the AC/DC coupling (2) , input impedance (3) , attenuator (4) and slope (5) as required.

(4) Connect the signals to be compared to the channel A and B inputs (the larger and cleaner signal to channel A for maximum accuracy).

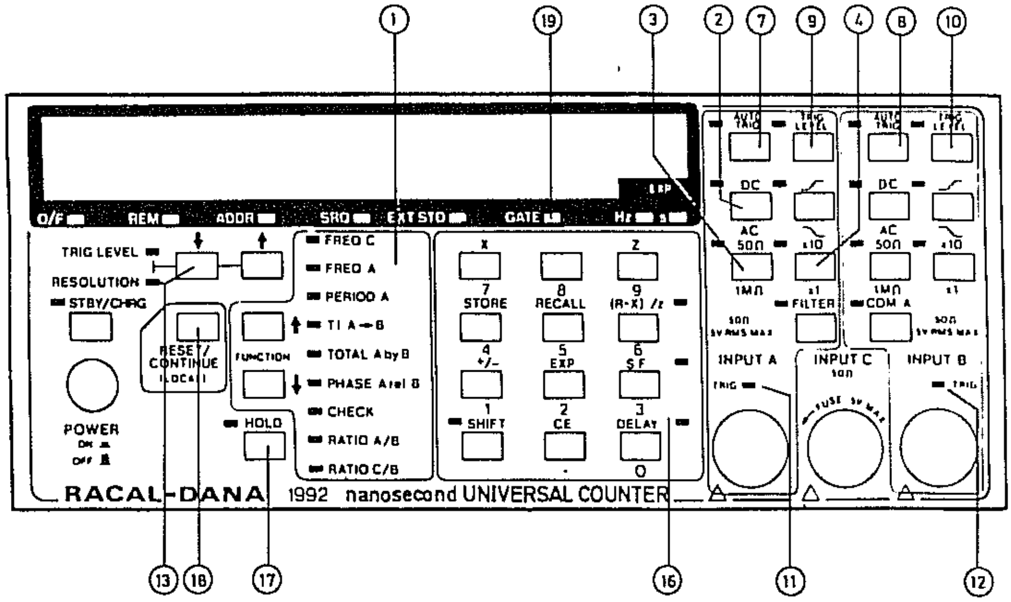
CAUTION SIGNAL LEVELS
ENSURE THAT THE INPUT SIGNALS DO NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Select auto-trigger (7) (8) , or set the manual trigger levels to the required values (9) (10) . Check that the TRIG indicators (11) (12) flash.

(6) If hold mode operation is required, select HOLD (17) and press the RESET key (18) .

(7) Check that the GATE indicator (19) flashes on during the measurement cycle.

NOTE:
The phase measurement is always positive, and is the angle by which the signal applied to channel A leads that applied to channel B.



RATIO MEASUREMENT

10 (1) Switch the power on.

(2) Select the RATIO A/B or RATIO C/B (1992 only) measurement mode, using the function selector ① .

(3) Set the AC/DC coupling ② , input impedance ③ , and attenuator ④ as required.

(4) Connect one of the signals to channel B and the other to channel A or C. The lower frequency signal should be connected to channel B.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNALS DO NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

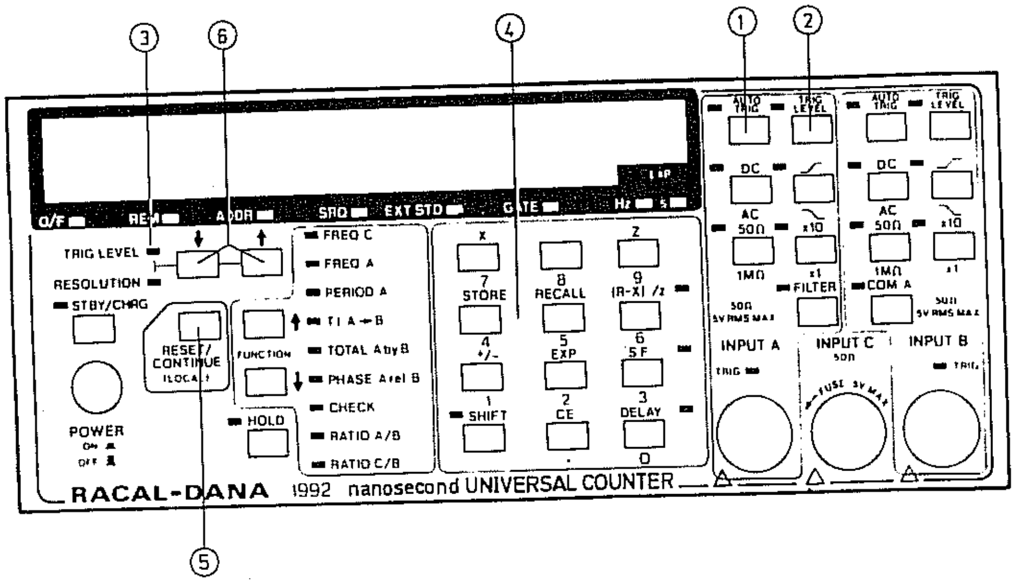
(5) Select auto-trigger ⑦ ⑧, or set the manual trigger levels to the required values ⑨ ⑩. Check that the TRIG indicators ⑪ ⑫ flash.

(6) Select the required display resolution ⑬ .

(7) If external arming is to be used, connect the arming signal and enter the required special function number. Enable the special functions ⑯ .

(8) If hold mode operation is required, select HOLD ⑰ and press the RESET key ⑱ .

(9) Check that the GATE indicator ⑲ flashes on during the measurement period.



TRIGGER LEVEL

Trigger Level Modes

11 The trigger level may be set by the operator (manual trigger level) or determined automatically by the instrument (auto-trigger level). The auto-trigger level is the arithmetic mean of the positive and negative-peak values of the input signal. The two modes are enabled alternately by successive operations of the AUTO TRIG key (1) . The indicator lights when the auto-trigger mode is selected.

Displaying and Setting the Manual Trigger Level

12 (1) Select the manual trigger mode using the AUTO TRIG key (1) .

(2) Display the trigger level by pressing the TRIG LEVEL key (2) . The associated indicator will flash and the trigger level control indicator (3) will light.

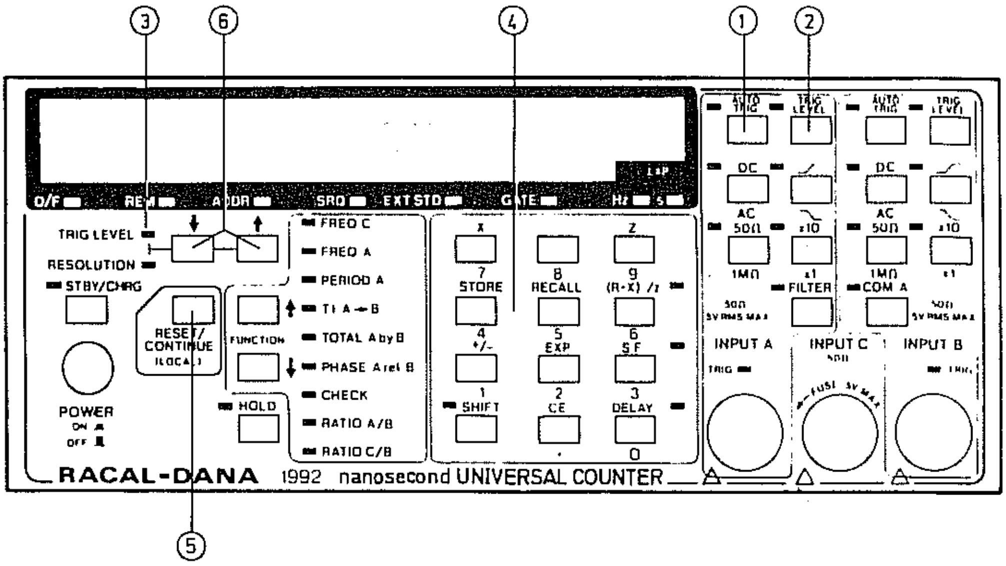
(3) To change the trigger level:

(a) Enter the required value, using the numeric keypad (4)

NOTE:
Up to this point the instrument can be returned to the measurement mode with the trigger level unchanged by pressing the CONTINUE key (5),

or

(b) Use the step up ↑ or step down ↓ control key (6) .



(4) Return the instrument to the measurement mode by pressing the TRIG LEVEL key (2) The TRIG LEVEL indicator and the trigger level control indicator (3) will go out.

NOTE:
There is only one trigger level store for each channel. Use of the auto-trigger mode will result in the manual trigger level being overwritten.

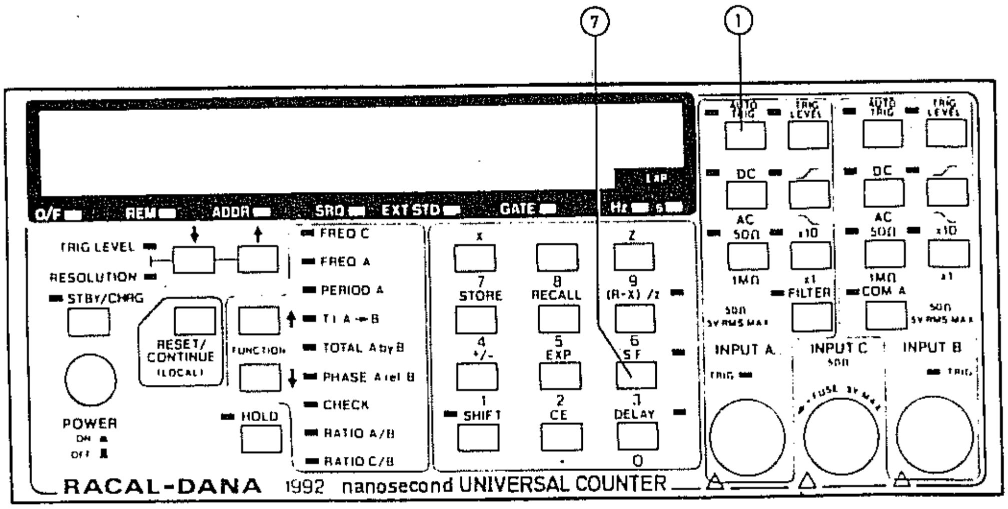
Displaying the Auto-Trigger Level

13 (1) Select the auto-trigger mode, using the AUTO TRIG key (1) .

(2) Display the auto-trigger level by pressing the TRIG LEVEL key (2) . The associated indicator will flash and the trigger level control indicator (3) will light.

NOTE:
Any attempt to make a numerical entry while the auto-trigger level is being displayed will cause the OP Er message to be displayed.

(3) Return the instrument to the measurement mode by pressing the TRIG LEVEL key (2) or the CONTINUE key (5) . The TRIG LEVEL indicator and the trigger level control indicator (3) will go out.



Single-Shot Auto-Trigger Level

14 The auto-trigger level is normally measured continuously, and varies if the peak levels of the signal change. A single-shot measurement of auto-trigger level can be made using special function 31. This value remains stored as a manual trigger level until:

(1) Another single-shot measurement is made, or

(2) A new manual trigger level is entered.

15 To make a single-shot measurement of auto-trigger level:

(1) Enter 31 in the special function register (7).

(2) Enable the special functions (7).

(3) Select AUTO TRIG (1). The associated indicator lights while the level is calculated and stored, and is then turned off.

Further one-shot measurements are made by selecting AUTO TRIG with special function 31 active.

Automatic Attenuation Setting

16 When operating in the auto-trigger mode, automatic switching of the X10 attenuator occurs as follows:

(1) The attenuator is switched in if the peak-to-peak value of the measured signal exceeds 5.1 V or if either peak is outside the range ±5.1 V.

(2) The attenuator is switched out if the peak-to-peak value of the measured signal is less than 4.6 V and both peaks are within the range ±4.6 V.

DISPLAY RESOLUTION

17 For all measurement functions other than TOTAL A by B and PHASE A rel B, the resolution refers to the number of zeros displayed when no signal is applied at the input. The resolution can be set to display 3 to 10 digits. (For a resolution of 10, the most significant digit overflows the display). A 10% overrange of the display is permitted without a change of range. Because of this, an additional digit with a value of 1 may appear at the more significant end of the display when measurements are made.

18 With some measurement functions, the number of digits appearing may be less than the selected resolution to ensure they are rounded to meaningful values.

19 When ratio measurements are made, no more than eight digits are displayed, regardless of the resolution selected.

20 For the TOTAL A by B measurement function the display shows the true total of events counted from 1 to 999 999 999. For higher totals the exponent is used.

21 For the PHASE A rel B measurement, up to four digits may be displayed for frequencies up to 1 MHz and up to three digits for higher frequencies. Leading zeros are suppressed. For frequencies above 10 MHz the resolution of the display is 10^{o}, and a place-holding zero is displayed as the least-significant digit.

Setting the Display Resolution

22 Whenever the resolution control indicator is lit, the resolution can be changed using the step-up ↑ and step-down ↓ keys. To step up from nine to ten digits, the step up key must be held for approximately two seconds.

Resolution With External Stop Circuit Arming

23 When external arming of the stop circuit is used, the minimum display resolution is governed by the arming period, as shown in Table 4.1.

TABLE 4.1

Resolution With External Arming

Arming Period	Minimum Resolution
Less than 100μs	4
100μs to 1 ms	5
1 ms to 10 ms	6
10 ms to 100 ms	7
100 ms to 1 s	8
1 s to 10 s	9

GATE TIME

24 For the frequency, period and ratio measurement functions, the gate time is related to the resolution selected, as shown in Table 4.2.

TABLE 4.2

Resolution and Gate Time

Resolution	Gate Time
10 (9 digits + overflow)	10 s
9	1 s
8	100 ms (see NOTE 2)
7	10 ms
6	1 ms
5	1 ms (see NOTE 3)
4	1 ms (see NOTE 3)
3	1 ms (see NOTE 3)

NOTE 1:
The gate times shown are nominal. Due to the use of the recipromatic counting technique the gate time may be extended by:

(a) Up to one period of the input signal on FREQ B and RATIO A/B.

(b) Up to two periods of the input signal on FREQ A and PERIOD A.

(c) Up to 64 periods of the input signal on FREQ C and RATIO C/B.

NOTE 2:
A resolution of 8 is selected when the instrument is first switched on.

NOTE 3:
With resolutions of 3, 4 and 5 selected, measurements are averaged.

25 For the PHASE A rel B measurement function the gate time depends upon the signal frequency. The gate time is approximately 25 ms for frequencies above 200 Hz, but will be increased at lower frequencies.

STOP CIRCUIT DELAY (HOLD OFF)

Use of the Delay

26 The stop circuit can be delayed when the T.I. A → B or the TOTAL A by B measurement function is selected. The required delay is entered into an internal store by the operator. The delay function can then be enabled and disabled as required. The delay is set to 204.8 µs (minimum delay) when the instrument is first switched on.

27 The delay can be used to prevent the stop circuit being triggered prematurely by spurious signals, such as those resulting from contact bounce. The principle is shown in Fig 4.1.

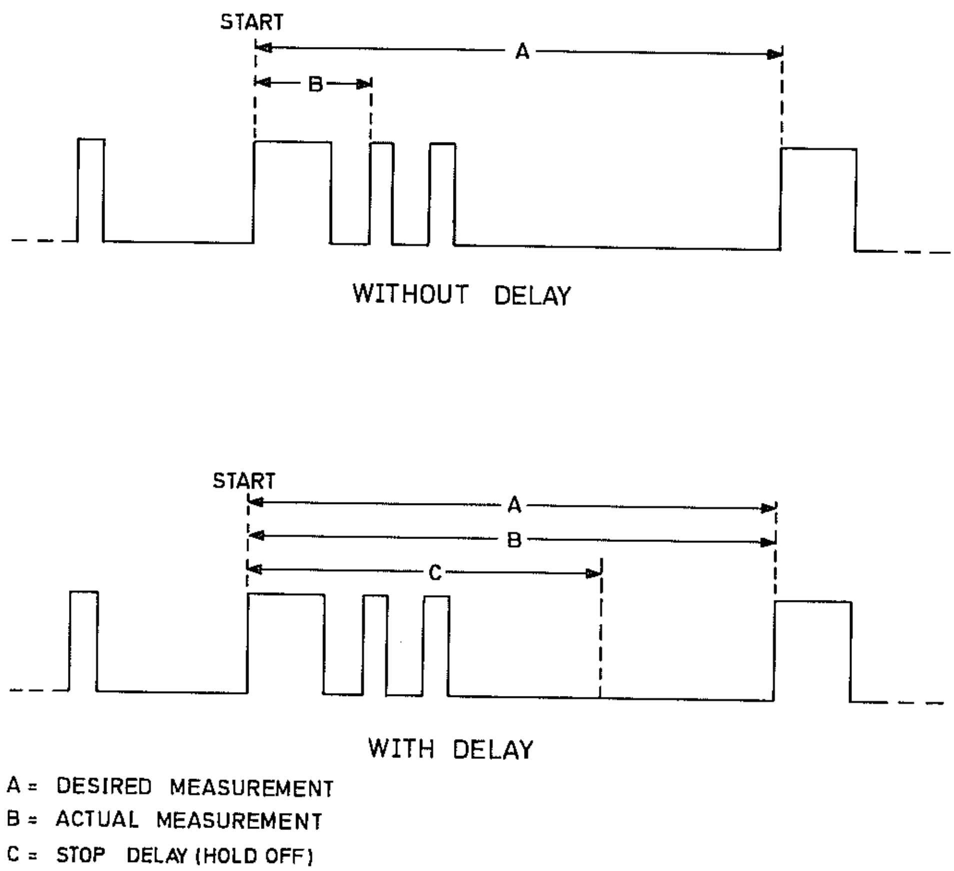


Fig 4.1 Use of Stop Circuit Delay

Displaying the Delay

28 The value of delay held in the store can be displayed by pressing

[SHIFT] [RECALL] [DELAY] .

Changing the Delay

29 A new value is entered into the delay store using the numeric keypad. Either direct decimal or exponential format may be used. For example, a delay of 305 μs may be entered using

[.] [0] [0] [0] [3] [0] [5] [SHIFT] [STORE] [DELAY]

or [3][0][5] [SHIFT] [EXP] [6] [SHIFT] [+/-] [SHIFT] [STORE] [DELAY] .

The instrument returns to the measurement mode automatically once the new delay value is stored.

30 The value of delay entered is rounded to the nearest 25.6 μs before it is stored. The permitted range of delay is from 204.8 μs to 800 ms. Attempted entry of an out-of-range value will result in the display of OP Er (operator error). The number in the delay store is retained when the instrument is switched to standby.

Enabling and Disabling the Delay

31 The stop delay is enabled and disabled by means of the key sequence

[SHIFT] [DELAY] .

The DELAY indicator lights when the delay is enabled.

SPECIAL FUNCTIONS

Special Function Numbering

32 The special functions provided for use by the operator are listed in Table 4.3. Each special function is defined by a two-digit number.

Special Function Register

33 One special function from each decade is entered into a special function register. Only the second digit is stored: the decade is indicated by the position of the digit in the register. The default state is with 0 entered in each position. The contents of the register can be displayed by pressing

[SHIFT] [RECALL] [SF] .

A typical display is illustrated in Fig 4.2.

TABLE 4.3

Special Functions

Function Number	Function		
		Start	Stop
10	Arming	Internal	Internal
11	Arming	External +ve	Internal
12	Arming	External -ve	Internal
13	Arming	Internal	External +ve
14	Arming	Internal	External -ve
15	Arming	External +ve	External +ve
16	Arming	External +ve	External -ve
17	Arming	External -ve	External +ve
18	Arming	External -ve	External -ve
20	Normal operation		
21	Channels A and B interchanged (see NOTE 1)		
30	Continuous measurement of auto-trigger level		
31	One-shot measurement of auto-trigger level		
40	Display time between measurement cycles	150ms	(see NOTE 2)
41	Display time between measurement cycles	0	(see NOTE 2)
42	Display time between measurement cycles	1s	(see NOTE 2)
43	Display time between measurement cycles	10s	(see NOTE 2)
44	Display time between measurement cycles	300s	(see NOTE 2)
50	Value displayed by operation of TRIG LEVEL	Trigger level	
51	Value displayed by operation of TRIG LEVEL	Signal positive peak	
52	Value displayed by operation of TRIG LEVEL	Signal negative peak	
60	Measurement made with TOTAL A by B selected	Normal TOTAL A by B	
61	Measurement made with TOTAL A by B selected	Manual Totalize	
70	Function with CHECK selected	10 MHz check	
71	Function with CHECK selected	LED check	
72-76	Reserved for diagnostic testing		
77	Channel A relay check		
78	Channel B relay check		

NOTE 1:
Special function 21 permits FREQ B, PERIOD B, T.I. B → A, TOTAL B by A and Phase B rel A. For these functions:
(1) FREQ B is specified to 100 MHz only.
(2) PERIOD B is specified down to 10 ns
(3) TOTAL B by A operates for one complete cycle of the channel A signal. The stop circuit delay is available on channel A.

NOTE 2:
Special functions 40, 42, 43 and 44 are only available when in local control. Special function 41 is selected automatically when in remote control.

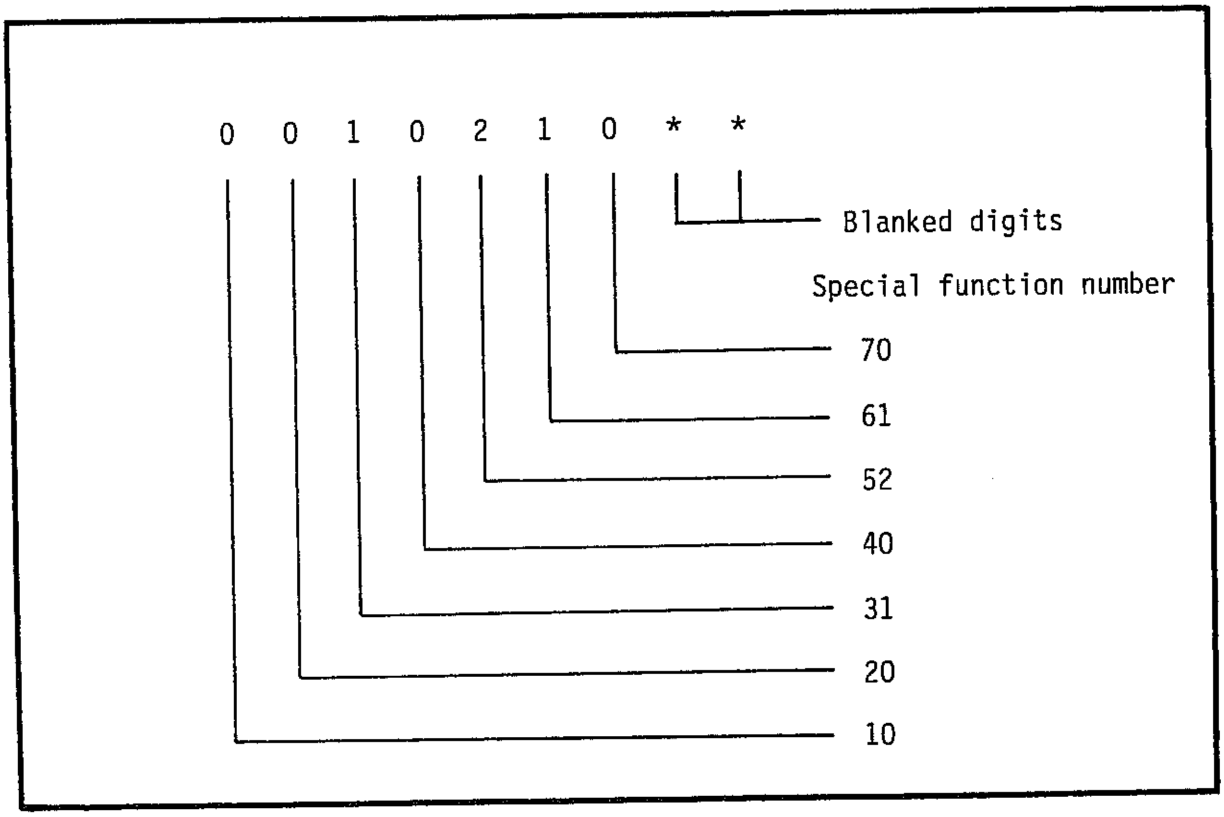


Fig 4.2 Special Function Register Display

Setting the Special Function Register

34 When a special function is to be used, its number must first be entered into the register. This is done by pressing

[N] [N] [SHIFT] [STORE] [SF] .

where NN is the special function number to be entered. The digits enter the display as the keys are pressed. The instrument returns to the measurement mode automatically once the number is stored.

35 When a number is stored it overwrites the number stored in the same decade. To remove a number from the register, another number from the same decade must be stored.

36 The numbers stored in the register are retained while the instrument is switched to the standby mode.

Enabling and Disabling the Special Functions

37 The default state corresponds to the default state of the special function register, i.e., with special functions 10, 20, 30, 40, 50, 60 and 70 enabled. The group of special functions whose numbers are entered in the special function register are enabled and disabled by means of the key sequence

[SHIFT] [SF] .

The SF indicator lights when this group of special functions is enabled.

NOTE:
A special function entered in the register while the special functions are enabled will be enabled immediately.

ERROR CODES

38 The instrument is able to detect a number of error states, which are indicated on the display. The meanings of the error codes are shown in Table 4.4

TABLE 4.4

Error Codes

Display	Error
Er 01	Phase measurement attempted on signals of different frequencies.
Er 02	Measurement result too large for the display.
Er 03	Overflow of internal counters.
OP Er	Error in numerical entry.
Er 50	Incorrect result obtained when in check mode.
Er 51	Relay or amplifier failure – Channel A – X10/X1
Er 52	Relay or amplifier failure – Channel A – 50 Ω/1 MΩ
Er 53	Relay or amplifier failure – Channel A – DC/AC
Er 54	Relay or amplifier failure – Channel A – FILTER
Er 55	Relay or amplifier failure – COM A
Er 56	Relay or amplifier failure – Channel B – X10/X1
Er 57	Relay or amplifier failure – Channel B – 50 Ω/1 MΩ
Er 58	Relay or amplifier failure – Channel B – DC/AC

NOTE:
Error codes Er 51 to Er 55 will only be generated with special function 77 active.
Error codes Er 56 to Er 58 will only be generated with special function 78 active.

Clearing the Error Codes

39 Error code Er 01 is cleared by:

(1) Making a phase measurement on signals of equal frequency.

(2) Selecting another measurement function.

Error codes Er 02 and Er 03 are cleared by:

(1) Obtaining a measurement result that is within range.

(2) Selecting another measurement function

OP Er is cleared by pressing [RESET].

MATH FUNCTION

40 The math function may be used with all measurement functions except Phase A rel B and CHECK. Its use permits the measured value to be offset and/or scaled before being displayed.

41 When the maths function is active the display indicates

$$\frac{\text{Measurement result} - X}{Z}$$

where X and Z are values entered into stores within the instrument by the operator. When the instrument is first switched on, X is set to 0 and Z to 1.

NOTE:
It is possible to set the constant Z to zero. However, any attempt to use the math function with this value set will cause an error code to be generated.

42 Displays of ratio, offset (null) and percentage difference can be obtained by setting X and Z as shown in Table 4.5.

TABLE 4.5

Uses of Math Function

Function Displayed	X	Z
Ratio: Measurement/N	0	N
Offset: Measurement - N	N	1
Percentage difference: 100 (Measurement-N)/N	N	N/100

Displaying the Math Constants

43 The values held in the X and Z stores can be displayed by pressing

[SHIFT] [RECALL] [X] or

[SHIFT] [RECALL] [Z] .

Changing the Constants

44 New values are entered into the math-constant stores using the numeric keypad. Either direct decimal or exponential format may be used. For example, a value for X of 0.0231 may be entered using

[.] [0] [2] [3] [1] [SHIFT] [STORE] [X]

or [2] [3] [1] [SHIFT] [EXP] [4] [SHIFT] [+/-] [SHIFT] [STORE] [X].

The instrument returns to the measurement mode automatically once the new value is stored.

45 The ranges of permissible values are:

(1) $1 \times 10^{-9} \leqslant Z < 1 \times 10^{10}$

(2) 0

(3) $-1 \times 10^{10} < Z \leqslant -1 \times 10^{-9}$

For negative numbers the ninth digit is available, but not displayed.

Enabling and Disabling the Math Function

46 The math function is enabled and disabled by means of the key sequence

[SHIFT] [(R-X)/Z] .

The (R-X)/Z indicator lights when the function is enabled.

EXTERNAL ARMING

47 This feature allows the start and/or stop point to be synchronized to a real time event or complex signal. Arming signal is connected to rear panel input and the relevant special function selected (Table 4.3). The measurement gate opening and closing are still determined by the input signal but can be conditioned (armed) by the external arming signal. Minimum start to stop external arming period is 50 µs (80 µs for RATIO A/B).

USING THE BATTERY PACK OPTION

Power Supply Changeover

48 When the battery pack option is installed, the instrument can be powered from the internal battery, an external DC supply of 11V to 16V, or an external AC supply. If the instrument is operating from either the DC supply or the battery, it will automatically change to operation from the AC supply when this is connected. The battery will not take over from either the AC or the DC supply if the supply fails. An external DC supply will not take over from the AC supply if the AC supply fails.

Battery-Low Indication

49 When the instrument is operating from the internal battery, or from an external DC supply, the STBY/CHRG indicator will start to flash as the supply voltage approaches the minimum permissible level. This occurs regardless of whether the instrument is in the standby mode or not. When operating from the battery, the instrument can be used in the measurement mode for approximately 15 minutes after the indicator commences flashing.

50 When the voltage of the battery or the external DC supply reaches the minimum permissible level, the instrument shuts down completely.

Operating Instructions

51 Instructions for preparing the instrument to make measurements are given in the following paragraphs. No other change in the operating procedure is required.

Operation From the Battery

52 (1) Set the INT/EXT switch on the rear panel to INT.

(2) Set the BATTERY SAVE/NORMAL switch to NORMAL.

(3) Switch the instrument on.

(4) Check that the instrument goes through the normal switch-on sequence. If the STBY indicator is flashing, or if there is no display, charge the battery.

53 If the battery-save facility is to be used, set the BATTERY SAVE/NORMAL switch to BATTERY SAVE. The instrument will remain in the measurement mode for approximately one minute and will then switch to standby. It can be returned to the measurement mode for a further period of one minute by pressing the STBY/CHRG key.

Operation From an External DC Supply

54 (1) Ensure that the instrument is switched off.

(2) Connect the DC supply to the DC power-input plug on the rear panel. The mating connector is a 2.1 mm coaxial socket.

CAUTION: SUPPLY POLARITY
THE POSITIVE SIDE OF THE SUPPLY MUST BE CONNECTED TO THE CENTER CONDUCTOR.

(3) Set the INT/EXT switch on the rear panel to EXT.

(4) Switch the instrument on. Check that the instrument goes through the normal switch-on sequence.

Battery Charging

55 The battery is trickle-charged whenever the instrument is operated from an A.C. supply and INT/EXT switch set to INT position. To charge the battery at the full rate, connect the instrument to an external AC or DC supply and switch to the standby mode.

INTRODUCTION

1 The instrument must be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the AC line voltage selector.

GPIB OPERATING MODES

2 The instrument can be operated via the GPIB in either the addressed mode or the talk-only mode.

TALK-ONLY MODE

3 The talk-only mode may be used in systems which do not include a controller. Such a system permits remote reading of the instrument's measurement data, but the instrument is operated by means of the front-panel controls as described in Section 4.

4 The rate at which measurements are made is determined by the instrument. The output buffer is updated at the end of each measurement cycle, overwriting the previous measurement data if this has not been transferred to the listener.

5 The transfer of data from the instrument to the listener is triggered by the listener. The instrument's output buffer is cleared when the data transfer is complete. Problems arising from the differences between the measurement rate and data transfer trigger rate are resolved according to the following protocol:

(1) If data transfer is in progress at the end of a measurement cycle, the updating of the output buffer is delayed. The data transferred will relate to the previous measurement cycle.

(2) If the data transfer trigger occurs during a measurement cycle and the output buffer is empty, data transfer will be delayed until the buffer is updated. The data transferred will then relate to the latest measurement cycle.

(3) If a measurement cycle is completed before the results of the previous cycle have been transferred to the listener, the buffer will be updated. The data for the previous cycle will be overwritten and lost.

6 The rate at which measurements are made can be controlled in the following ways:

(1) The gate time of the instrument (duration of the measurement cycle) can be controlled by choosing an appropriate display resolution.

(2) A time interval can be introduced between measurement cycles by using special functions 40 to 44.

(3) The instrument can be operated in the hold mode. Single measurement cycles can be triggered, when required, by means of the RESET key.

7 The format of the data output is described in Table 5.1.

ADDRESSED MODE

8 In addressed-mode operation, all the instrument's functions, except the power ON/OFF and standby switching, can be controlled by means of device-dependent commands, sent via the bus, when the instrument is addressed to listen. The measurements made, and data regarding the instrument's status, can be read via the bus when the instrument is addressed to talk. If the instrument is addressed to talk when the output buffer is empty, no data transfer can take place and bus activity will cease. Data transfer will commence when the output buffer is updated at the end of the next measurement cycle.

DATA OUTPUT FORMAT

9 The same output message format is used for the transmission of measured values and numbers recalled from the instrument's internal stores. The message consists of a string of 21 ASCII characters for each value transmitted. These are to be interpreted as shown in Table 5.1. The units should be assumed to be Hz, seconds, degrees or a ratio, depending upon the commands previously given to the instrument.

TABLE 5.1

Output Message Format

Byte No	Interpretation	Permitted ASCII Characters
1	Function letter	See Table 5.2
2	Function letter	
3	Sign of measurement	+ or -
4	Most significant digit	0 to 9
5	Digit	0 to 9 or .
6	Digit	0 to 9 or .
7	Digit	0 to 9 or .
8	Digit	0 to 9 or .
9	Digit	0 to 9 or .
10	Digit	0 to 9 or .
11	Digit	0 to 9 or .
12	Digit	0 to 9 or .
13	Digit	0 to 9 or .
14	Digit	0 to 9 or .
15	Least significant digit	0 to 9 or .
16	Exponent indicator	E
17	Sign of exponent	+ or -
18	More significant digit	0 to 9
19	Less significant digit	0 to 9
20	Carriage return	CR
21	Line Feed	LF

NOTE 1:
Bytes 4 to 15 will always include 11 digits and a decimal point. Zeros will be added, where necessary, in the more significant digit positions.

NOTE 2:
The exponent indicated by bytes 18 and 19 will always be a multiple of three.

TABLE 5.2

Function Letters

Function	Function Letters
Frequency A	FA
Frequency C	FC
Ratio A/B	RA
Ratio C/B	RC
Time interval	TI
Total A by B	TA
Phase	PH
Period A	PA
Check	CK
Recalled Data	**Function Letters**
Unit type	UT
Resolution	RS
Trigger level, A channel	LA
Trigger level, B channel	LB
Math constant X	MX
Math constant Z	MZ
Delay time	DT
Special function	SF
Master software issue number	MS
GPIB software issue number	GS

NOTE:
Spaces are substituted for the function letters when special function 81 is active.

SERVICE REQUEST

10 The instrument can be set, by means of device-dependent commands, to generate the service request message (SRQ) when:

(1) A measurement cycle is completed
(2) A change of frequency standard occurs
(3) An error state is detected
(4) Any combination of (1), (2) and (3).

11 The generation of the SRQ may also be inhibited. The necessary commands are given in Table 5.14. Option (3) of Paragraph 10 is selected when the instrument is first switched on.

STATUS BYTE

12 The format of the status byte, generated in response to a serial poll, is given in Table 5.3.

TABLE 5.3

Status Byte Format

DIO Line	Function
1	LSB ⎤
2	⎬ Number of error detected (binary)
3	MSB ⎦ (See NOTE 1)
4	'1' = frequency standard changed
5	'1' = reading ready (See NOTE 2)
6	'1' = error detected
7	'1' = service requested
8	'1' = gate open

NOTE 1:
The error code numbers which can occur are:

1 Phase measurement attempted on waveforms of differing frequency.
2 Result out of range of the display
3 Overflow of internal counters
4 Error in numerical entry
5 Syntax error in GPIB command

No measurement data string is available if error code 1, 2 or 3 is generated.

NOTE 2:
Regardless of the SRQ mode in use, the SRQ message that a reading is ready is not generated following a data-recall operation.

NOTE 3:
The errors are cleared as follows:

Error 1: Correct the difference in input frequencies or change the measurement mode in use.

Error 2: The error is cleared when an in-range measurement is completed.

Error 3: The error is cleared when an in-range measurement is completed.

Error 4: The error is cleared when a valid numerical entry is made.

Error 5: The command string will be correctly executed up to the point at which the error occurs. The remainder of the string will be hand-shaken, but not executed. The error is cleared when the next valid command is received.

EXPLANATION OF RESPONSE TO INTERFACE MESSAGES

13 The instrument will respond to all valid device-dependent commands which are received after it has been addressed to listen. Device-dependent commands are recognized as such because they are transmitted with the attention (ATN) message false.

14 The instrument also responds to a number of multi-line interface messages. These are recognized because they are transmitted with the ATN message true. Refer to Table 5.4, which gives the instrument's response to different bus messages. The following paragraphs detail the instrument's response to these messages. Any multi-line message not specifically mentioned is hand-shaken, but is otherwise ignored.

Address Messages

15 The instrument responds to address messages defined by the setting of the address switches, A1 to A5, on the rear panel.

16 On receipt of its listen address, the instrument becomes a listener. If it has previously been addressed to talk it ceases to act as a talker. If in the local control state when the address is received, the instrument goes to the remote control state provided that the REN message is true.

17 On receipt of its talk address, the instrument becomes a talker. If it has previously been addressed to listen it ceases to act as a listener. If in the local control state when the address is received, it will remain under local control.

18 If the instrument has been addressed to talk, and then receives the talk address of another device, it ceases to act as a talker.

Local Lockout

19 The instrument will respond to the local lockout (LLO) message regardless of its addressed state. The return-to-local function of the LOCAL key on the front panel is disabled (the RESET/CONTINUE function remains enabled when in local control).

20 Local lockout is cleared by sending the remote enable (REN) message false. This returns all devices on the bus to the local control state.

Device Clear and Selected Device Clear

21 The instrument only responds to the device clear (DCL) message and the selected device clear (SDC) message when it is in the remote control state. It will only respond to the SDC message if it is a listener, but will respond to the DCL message regardless of its addressed state.

22 The instrument responds to either message by reverting to the functions and settings of the power-up state. No change is made to the condition of the GPIB interface.

TABLE 5.4

Response to Bus Messages

Message	Addressed State	Instrument Response
Address	Any	For listen address: Becomes a listener and goes to the remote control state. If previously addressed to talk, ceases to act as a talker. For talk address: Becomes a talker. If previously addressed to listen, ceases to be a listener. For talk address of another device: If previously addressed to talk, ceases to be a talker.
Local Lockout (LLO)	Any	LOCAL key disabled. (Cleared by sending the REN message false).
Device Clear (DCL) Selected Device Clear (SDC)	Any, but must be in remote control. Listen, and in remote control	Reverts to power-up state.
Serial Poll Enable (SPE) Serial Poll Disable (SPD)	Any Any	Enters the serial poll mode state (SPMS). If addressed to talk while in this state, sends the status byte. Enters the serial poll idle state (SPIS). If addressed to talk while in this state, sends data in the output message format.
Group Execute Trigger (GET)	Listen, and no measurement cycle in progress	Takes a measurement.
Go to Local (GTL)	Listen	Reverts to local control.
Untalk Unlisten	Talk Listen	Ceases to be a talker. Ceases to be a listener. The ADDR indicator is turned off.

Serial Poll Enable and Serial Poll Disable

23 The instrument responds to both the serial poll enable (SPE) message and the serial poll disable (SPD) message regardless of its addressed state.

24 The instrument responds to the SPE message by entering the serial poll mode state (SPMS). If the instrument is addressed to talk while in this state, it will put its status byte onto the bus instead of its normal data output string.

25 The instrument responds to the SPD message by leaving the SPMS and entering the serial poll idle state (SPIS). If the instrument is addressed to talk while in this state, it will put its data output string onto the bus provided data is available in the output buffer.

Group Execute Trigger

26 The instrument responds to the group execute trigger (GET) message provided that it is a listener and no measurement cycle is in progress. Except for the inability to retrigger during a measurement cycle, the response to the GET message is the same as to the device-dependent command T2.

Go to Local

27 The instrument responds to the go to local (GTL) message provided that it is a listener. The instrument reverts to the local control state, but remains addressed to listen. It will return to remote control on receipt of the first byte of a device-dependent command.

Untalk and Unlisten

28 If addressed to talk, the instrument will go to the talker idle state (TIDS) on receipt of the untalk message. If addressed to listen, it will go to the listener idle state (LIDS) on receipt of the unlisten message. The ADDR indicator will be turned off.

INPUT COMMAND CODES

29 When the instrument is addressed to listen it can be controlled by means of device-dependent commands given in the following tables:

Table 5.6 Instrument Preset Code
Table 5.7 Measurement Function Codes
Table 5.8 Input Control Codes
Table 5.9 Measurement Control Codes
Table 5.10 Store and Recall Codes
Table 5.11 Numerical Input Format
Table 5.12 Numerical Input Ranges
Table 5.13 Resolution Selection
Table 5.14 Special Function Codes
Table 5.15 Service Request Codes

30 If more than one command is to be sent, no delimiters are required. If necessary, commas, spaces and semicolons may be included in command strings as an aid to clarity without affecting the operation of the instrument. Each command string must be followed by an end-of-string terminating group. The permitted terminating groups are shown in Table 5.5.

TABLE 5.5

Permitted Terminators

1	2	3	4	5	6
LF	LF EOI true	CR EOI true	CR LF	CR LF EOI true	Last Character EOI true

TABLE 5.6

Instrument Preset Code

Function	Code
Set instrument functions and settings to the power-up state	IP

TABLE 5.7

Measurement Function Codes

Function	Code
Frequency A	FA
Frequency C	FC
Period A	PA
Time interval	TI
Total A by B	TA
Phase of A relative to B	PH
Ratio A/B	RA
Ratio C/B	RC
Check	CK

NOTE:
The 1991 does not accept FC and RC as valid commands.

TABLE 5.8

Input Control Codes

Function	Code	
	A Channel	B Channel
AC coupling selected	AAC	BAC
DC coupling selected	ADC	BDC
1 MΩ input impedance selected	AHI	BHI
50 Ω input impedance selected	ALI	BLI
Positive slope trigger selected	APS	BPS
Negative slope trigger selected	ANS	BNS
X10 attenuator disabled	AAD	BAD
X10 attenuator enabled	AAE	BAE
Manual trigger level selected	AMN	BMN
Auto trigger level selected	AAU	BAU
A channel filtering enabled	AFE	
A channel filtering disabled	AFD	
A and B channels separate	BCS	
A and B channels common	BCC	

TABLE 5.9

Measurement Control Codes

Function	Code
Select continuous measurement mode	TØ (see NOTE 1)
Select one-shot measurement mode	T1 (see NOTE 2)
Take one measurement or start totalize measurement	T2 (see NOTE 3)
Stop totalize measurement	T3 (see NOTE 3)
Read present value without stopping totalize measurement	RF (see NOTE 4)
Delay disabled	DD
Delay enabled	DE
Reset (Stop measurement cycle and clear output buffer)	RE
Math function disabled	MD
Math function enabled	ME

NOTE 1:
When making continuous measurements the output buffer is updated at the end of each gate period. If the buffer is being read via the GPIB when the gate period ends, updating is delayed until reading is complete.

NOTE 2:
When one-shot measurements are being made, the output buffer is cleared each time command T2 is received. The measurement made must, therefore, be read before a further measurement cycle is triggered.

NOTE 3:
When making totalize measurements, commands T2 and T3 are used with TA and special function 61. In this mode the readings made in successive totalize periods are cumulative. The RE command is used to reset the count to zero when required.

NOTE 4:
The RF command (reading on the fly) must be sent each time a reading is required. The reading is obtained when the instrument is made a talker.

TABLE 5.10

Store and Recall Codes

Function	Code
Recall unit type	RUT
Store display resolution number	SRS
Recall display resolution number	RRS
Store A channel manual trigger level	SLA (see NOTE 1)
Recall A channel manual trigger level or peak level	RLA (see NOTES 1 and 2)
Store B channel manual trigger level	SLB (see NOTE 1)
Recall B channel manual trigger level or peak level	RLB (see NOTES 1 and 2)
Store maths constant X	SMX
Recall maths constant X	RMX
Store maths constant Z	SMZ
Recall maths constant Z	RMZ
Store arming delay value	SDT
Recall arming delay value	RDT
Recall special function register	RSF
Recall master software issue number	RMS
Recall GPIB software issue number	RGS

NOTE 1:
The manual trigger level is automatically scaled by a factor of 10 when the X10 attenuator is switched in or out of circuit. Ensure that the correct input attenuation is selected before storing or recalling the trigger level.

NOTE 2:
The levels recalled by commands RLA and RLB depend upon the enablement of special functions 50, 51 and 52.

NOTE 3:
Numbers to be stored should follow the store command. The format to be used for numerical entry is given in Table 5.11. The limiting values for numerical entries are given in Table 5.12.

NOTE 4:
The instrument returns to the measurement mode automatically at the completion of a store or recall operation.

NOTE 5:
No SRQ message is generated for recalled data.

TABLE 5.11

Numerical Input Format

Byte	Interpretation	Permitted ASCII Characters
1	Sign of mantissa	+ or -
2	Most significant digit	0 to 9 or .
3	Digit	0 to 9 or .
4	Digit	0 to 9 or .
5	Digit	0 to 9 or .
6	Digit	0 to 9 or .
7	Digit	0 to 9 or .
8	Digit	0 to 9 or .
9	Digit	0 to 9 or .
10	Digit	0 to 9 or .
11	Least significant digit	0 to 9 or .
12	Exponent indicator	E or e
13	Sign of exponent	Space, + or -
14	More significant digit	0 to 9
15	Less significant digit	0 to 9

NOTE 1:
Spaces, nulls or zeros occurring immediately before byte 1 will be ignored.

NOTE 2:
Byte 1 may be omitted. A positive mantissa will then be assumed.

NOTE 3:
Bytes 2 to 11 may contain up to nine digits and a decimal point. If more than nine digits are entered without a decimal point, excess digits will be truncated. The excess digits will, however, increase the power of ten stored.

If fewer than nine digits are required the unused bytes may be omitted.

NOTE 4:
Spaces or nulls entered between bytes 11 and 12 will be ignored.

NOTE 5:
The exponent group, bytes 12 to 15, may be omitted.

NOTE 6:
Byte 13 may be omitted or transmitted as a space. In either case a positive exponent will be assumed.

NOTE 7:
Byte 15 may be omitted for a single-digit exponent.

NOTE 8:
Units are assumed to be volts for trigger level and seconds for delay time.

TABLE 5.12

Numerical Input Ranges

Function	Command Code	Numerical Limits	
		Low	High
Resolution	SRS	3	10
Trigger Level (X1)	SLA, SLB	-5.1	+5.1
Trigger Level X10	SLA, SLB	-51	+51
Math constant	SMX, SMZ	$\geq 1 \times 10^{-9}$	$< 1 \times 10^{10}$
		0	
		$> -1 \times 10^{10}$	$\leq -1 \times 10^{-9}$
Delay time	SDT	200×10^{-6}	0.8

NOTE 1:
Numbers entered will be rounded up before storage, as follows:

(1) Trigger level (X1) to next multiple of 20 mV
(2) Trigger level (X10) to next multiple of 200 mV
(3) Delay time to next multiple of 25.6 μs

NOTE 2:
Resolution entries will be rounded down to the next integer. The related gate times are shown in Table 5.13.

NOTE 3:
The math constant Z can be set to zero. However, any attempt to use the math function with this value set will cause an error code to be generated.

TABLE 5.13

Gate Times

Number of digits in Freq. Period and Check	Gate Time	Resolution number
10	10 s	10
9	1 s	9
8	100 ms	8
7	10 ms	7
6	1 ms	6
5	1 ms	5
4	1 ms	4
3	1 ms	3

TABLE 5.14

Special Function Codes

Function	Code
Special functions disabled	SFD
Special functions enabled	SFE
Enter special function nn in special function register	Snn

NOTE 1:
The list of special functions is given in Section 4 Table 4.3.

NOTE 2:
A special function entered in the register while the special functions are enabled will be enabled immediately.

TABLE 5.15

Service Request Codes

Function	Code
Inhibit generation of SRQ	Q0
SRQ generated when error is detected	Q1
SRQ generated for measurement ready	Q2
SRQ generated for measurement ready or error detected	Q3
SRQ generated for frequency standard changeover	Q4
SRQ generated for frequency standard changeover or error detected	Q5
SRQ generated for measurement ready or frequency standard changeover	Q6
SRQ generated for measurement ready, error detected or frequency standard changeover	Q7

NOTE:
SRQ is not generated by data recalled from store.

TABLE 5.16

Alphabetic List of Command Codes

Code		Code	
AAC	A channel, AC coupling	ME	Maths function enabled
AAD	A channel X10 attenuator disabled	PA	Period A
AAE	A channel X10 attenuator enabled	PH	Phase A relative to B
AAU	A channel autotrigger	Qn	SRQ mode
ADC	A channel, DC coupling	RA	Ratio A/B
AFD	A channel filtering disabled	RC	Ratio C/B (1992 only)
AFE	A channel filtering enabled	RDT	Recall delay time
AHI	A channel, 1 MΩ	RE	Reset measurement
ALI	A channel, 50 Ω	RF	Read total so far
AMN	A channel manual trigger	RGS	Recall GPIB software issue
ANS	A channel, -ve slope	RLA	Recall A channel trigger or peak level
APS	A channel, +ve slope	RLB	Recall B channel trigger or peak level
BAC	B channel, AC coupling	RMS	Recall master software issue number
BAD	B channel X10 attenuator disabled	RMX	Recall math constant X
BAE	B channel X10 attenuator enabled	RMZ	Recall math constant Z
BAU	B channel autotrigger	RRS	Recall resolution
BCC	A and B channels common	RSF	Recall special function
BCS	A and B channel separate	RUT	Recall unit type
BDC	B channel, DC coupling	Snn	Special function
BHI	B channel, 1 MΩ	SDT	Store delay time
BLI	B channel, 50 Ω	SFD	Special function disabled
BMN	B channel manual trigger	SFE	Special function enabled
BNS	B channel, -ve slope	SLA	Store A channel trigger level
BPS	B channel, +ve slope	SLB	Store B channel trigger level
CK	Check	SMX	Store math constant X
DD	Delay disabled	SMZ	Store math constant Z
DE	Delay enabled	SRS	Store resolution
FA	Frequency A	Tn	Measurement mode or Start/Stop reading
FC	Frequency C (1992 only)	TI	Time interval
IP	Instrument preset	TA	Total A by B
MD	Math function disabled		

NOTE:
n represents a single digit.

INTRODUCTION

1 This section describes the principles of operation of the instrument, with respect to a number of block diagrams in the text, and describes the significant features of the circuits used with respect to the circuit diagrams given in Section 8. The block diagrams are annotated with the main circuit references to simplify cross referencing between the block diagram and circuit diagram.

2 In the circuit descriptions the integrated circuits are referred to by the circuit reference given on the appropriate circuit diagram. Note that a separate series of numbers, starting at IC1, is allocated to each assembly. Where an integrated circuit package contains more than one circuit, suffix letters are used to distinguish between them. Where it is required to identify a particular pin of an integrated circuit, the circuit reference, with suffix letter if appropriate, is followed by an oblique stroke and the required pin number.

FUNCTIONAL SYSTEMS

3 The instrument contains nine functional systems. These are:

(1) The channel A and channel B system.

(2) The channel C system (1992 only).

(3) The measurement system.

(4) The display system.

(5) The keyboard system.

(6) The microprocessor system.

(7) The standby and IRQ system.

(8) The power supply system.

(9) The internal frequency standard system.

4 The functional relationship between the systems is illustrated in Fig 6.1. The measurement system is internally configured by the microprocessor system according to the instructions entered via the keyboard or GPIB system. The signal to be measured and the signal from the frequency standard are fed to the measurement system. The measured result is passed to the microprocessor system. If mathematical manipulation of the result is required, this is performed by the microprocessor before the final output is passed to the display or GPIB system.

5 The standby and IRQ system handles instructions to switch to standby, received from the keyboard system or the battery pack option, and interrupt requests made by other systems.

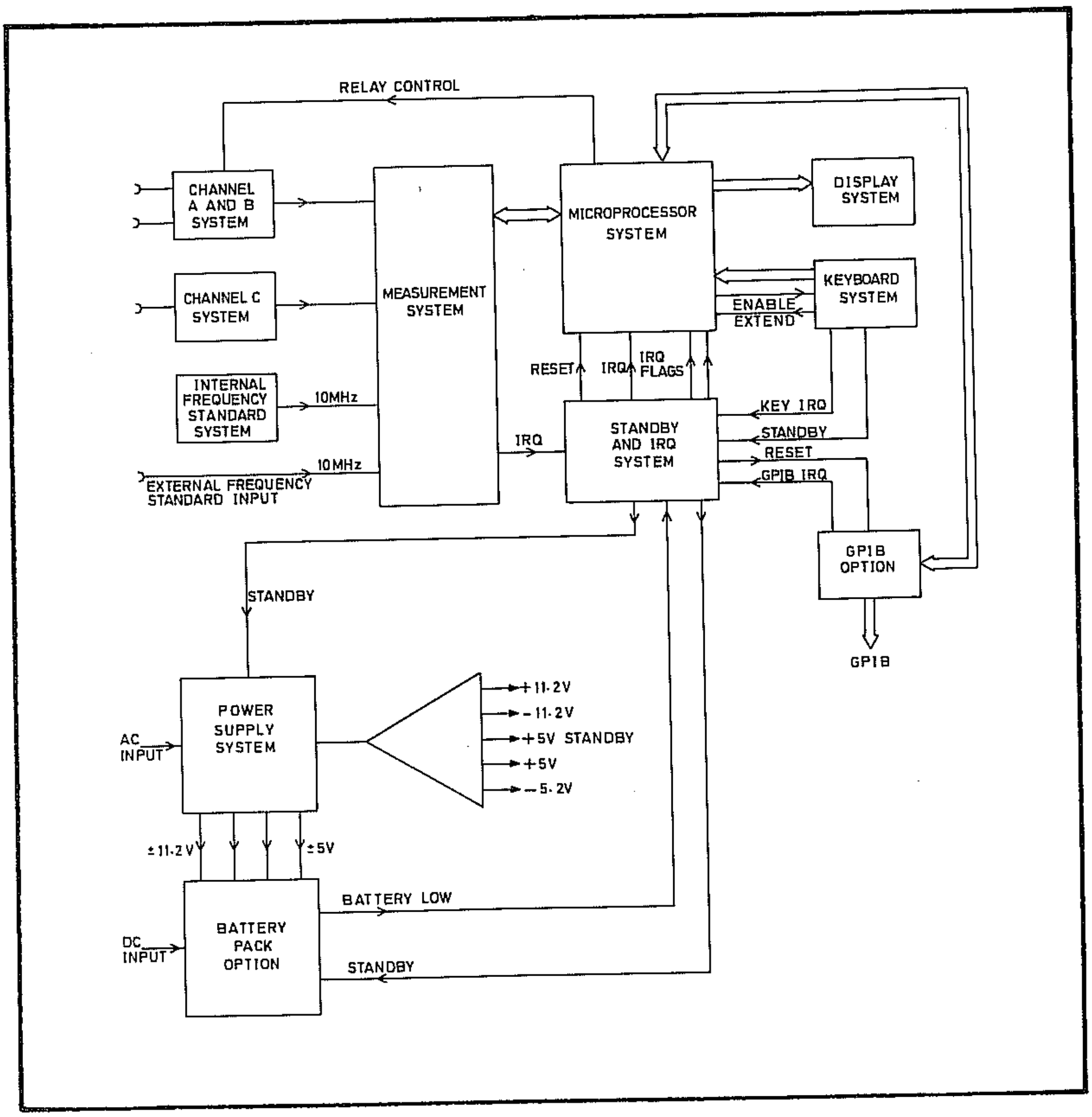


Fig 6.1 Functional Block Diagram

THE CHANNEL A AND CHANNEL B SYSTEM

Functional Description

6 The channel A and channel B system processes the signals applied at the channel A and channel B inputs to produce differential pairs of signals which are fed to the measurement system. A block diagram is given in Fig 6.2.

7 Each channel includes relay-controlled circuits which allow selection of 50 Ω/1 MΩ input impedance, AC/DC coupling and X1/X10 attenuation. The common A configuration (channel B signal disconnected and channel A signal connected to both amplifiers in parallel) can be selected.

8 The channel amplifiers feature separate high frequency and low frequency paths. The crossover frequency is nominally 5 kHz. Signal filtering can be introduced, in channel A only, by disconnecting the high frequency amplifier path and increasing the bandwidth of the low frequency path to 50 kHz nominal. The signals from the high and low frequency paths are combined, and drive a Schmitt trigger output stage.

9 The trigger levels for the two channels are derived independently in the digital-to-analog converter (DAC) using data supplied from the microprocessor system.

10 Control signals for the system relays are supplied from the microprocessor system.

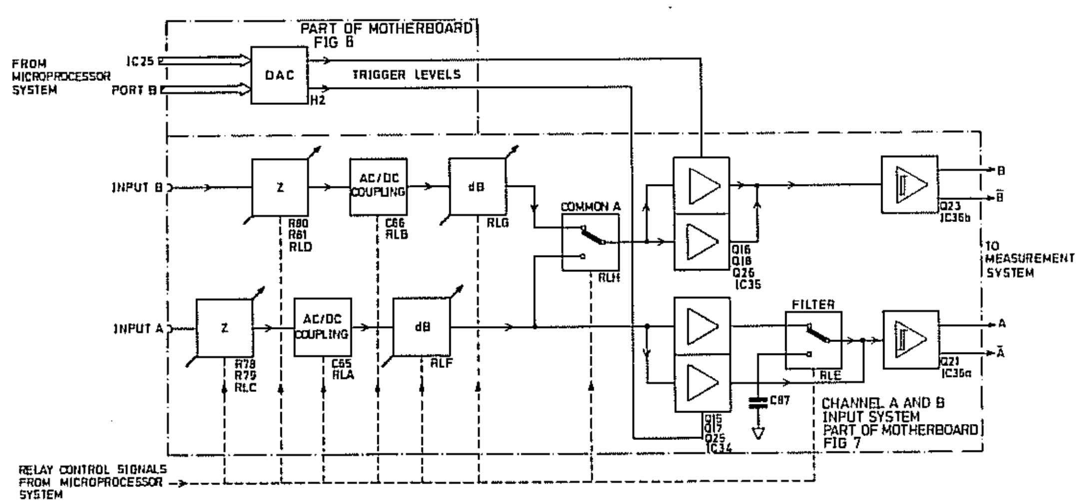


Fig 6.2 The Channel A and Channel B System

Circuit Description

11 The circuit diagram is shown in Fig 7 in Section 8. When relay RLC is energised the input impedance seen at SK5 (INPUT A) is 50Ω, given by resistors R78/R79 in parallel.

12 When energised, RLA gives DC coupling of the input signal. With RLA deenergised the signal is AC coupled via C65. R165 limits the current surge which occurs if DC coupling is selected while C65 is in the charged state.

13 The X1/X10 attenuator is formed by R82, R83, R87 and RLF. With RLF deenergised, the attenuator has a series element R82 and a shunt element formed by R83 and R87 in parallel. The attenuation is 20 dB (nominal). With RLF energised R82 is short circuited, giving 0 dB attenuation.

14 The attenuator output is fed to the high frequency channel buffer, Q15 and Q17, via R160 and C73. The gate of Q15 is protected against excessive negative voltage swings by D5. The gain from the attenuator output to the emitter of Q17 is approximately 0.94.

15 The buffer of the low frequency channel, IC34 and Q25, receives its input from the potential divider R87. The gain from R87 pin 1 to the emitter of Q25 is approximately 0.94. Any offset in the system can be nulled by adjusting R192.

16 When RLE is deenergised (channel A filter not selected) the signals from the two buffers are combined at the base of Q21 by the network C79 and R107. These components act as a low-pass filter to the output of the low frequency buffer, and as a high-pass filter to the output of the high frequency buffer. The crossover frequency is 5 kHz.

17 The signal at Q21 emitter is fed to the Schmitt trigger, IC36a, via the diode bridge formed by D18, D19, D20 and D21. This protects the input of IC36a by limiting the signal swing to approximately ±1 V.

18 The differential output of IC36 forms the input to the measuring system. The hysteresis of IC36, and therefore the channel sensitivity, can be set by adjusting R149.

19 The trigger level is set by the DAC, H2, shown in Fig 8, and is fed to IC34/2 via R202 and one section of R89. Feedback, taken from the emitter of Q21 to IC34/2 via R89 pins 5 and 3, makes R89 pin 3 a virtual earth point, and the gain from the R136/R202 junction to the emitter of Q21 is -0.94. A 1 V DC level at the channel A input and a 1 V trigger level therefore combine to give 0 V at Q21 emitter. Thus the selected trigger point on the input signal is always brought to 0 V at Q21 emitter.

20 When the channel A low-pass filter is selected, RLE is energised. This open circuits the high frequency channel, and connects C87 across the low frequency channel. The low frequency channel bandwidth is then nominally 50 kHz.

21 The circuit of channel B is similar to that of channel A, but is not provided with a low-pass filter. Energizing RLH connects the signal applied at the channel A input to both channel amplifiers.

22 The relays are controlled by the microprocessor system. The voltage levels on the control lines are latched in IC24, shown in Fig 8 in Section 8.

THE CHANNEL C SYSTEM

Functional Description

23 The channel C system is provided on Model 1992 only. A block diagram is given in Fig 6.3. The system processes the signal applied at the channel C input and feeds it to the measurement system.

24 The channel input is protected by a fuse, mounted in the input connector, and by a signal limiting circuit. This is followed by an automatic level control circuit, which reduces the range of signal level applied to the amplifier.

25 After amplification the signal is prescaled by 64 before being passed via a buffer and a signal gate to the measurement system.

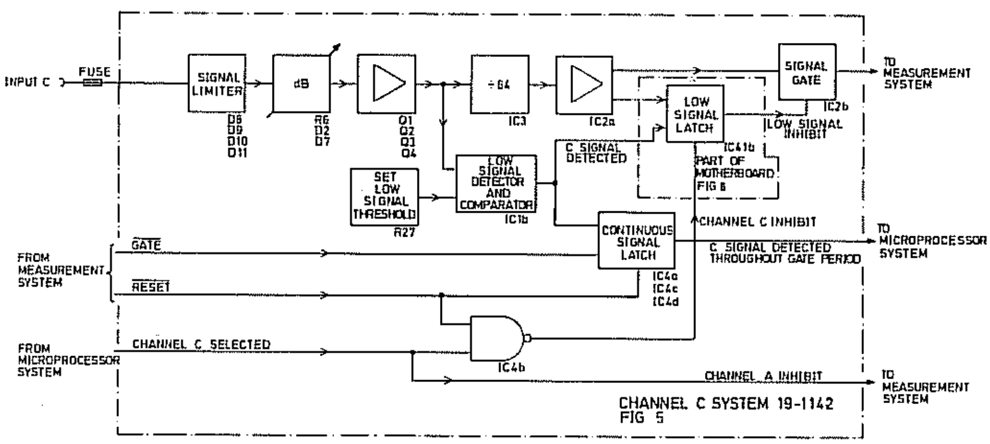


Fig 6.3 The Channel C System

26 The amplitude of the signal at the amplifier output is monitored by a detector and comparator. The comparator output controls the low-signal latch. If the detector output is below the threshold, the latch is set and the channel output is inhibited by the signal gate. When the detector output goes above the threshold the low-signal latch is armed, and opens the signal gate on the next signal edge from the prescaler. This enables the instrument to make measurements on bursts of signal.

27 The detector output is also applied to the continuous signal latch. This latch is reset at the beginning of each gate period, and is set if the detector output falls below the threshold level. The microprocessor system samples the latch output throughout the gate period. If the measured signal falls below the threshold level during this period, the measured result is set to zero.

28 If channel C is not selected, the low-signal latch is held reset by a control signal from the microprocessor system and the output to the measurement system is inhibited. The same control signal is used to enable channel A, so that the two channels cannot be enabled at the same time.

Circuit Description

29 The circuit diagram is shown in Fig 5 in Section 8. The signal to be measured is connected via SK13 (INPUT C). The circuit is protected by the fuse, which is mounted within SK13. The signal amplitude is limited by the diode clamp comprising D8, D9, D10 and D11.

30 A measure of automatic gain control is achieved by means of an attenuator, formed by R6 and the impedance of the PIN diodes, D2 and D7. The peak-to-peak detector, D1, D3, R7 and C48, produces a negative voltage proportional to the signal amplitude. A direct current proportional to this voltage flows through the PIN diodes via L1. The impedance of the diodes decreases if the current increases, so that changes in signal amplitude are offset by changes in attenuation.

31 The signal passes through four amplifier stages, incorporating Q1, Q2, Q3 and Q4. The amplified signal is fed to the counter, IC3, via the shaping circuit formed by R37, C46 and R36.

32 The signal frequency is prescaled by 64 in IC3 and buffered in IC2a. Provided that channel C is selected and the amplitude of the signal is adequate, the output at IC2a/2 passes to the measurement system via the gate, IC2b, and SK7 pin 5.

33 The signal at the output of Q4 is fed to the low-signal detector, D5 and C23. The comparator, IC1b, compares the detector output with a threshold voltage, set by R27. The comparator output is at logic '1' if the detector output is below the threshold (channel C signal amplitude too low for accurate counting).

34 The logic level at the comparator output is inverted in IC1a, and is fed via SK7 pin 14 to the D input of the low-signal latch, IC41b, shown in Fig 8. IC41b is clocked by the output of IC2a via SK7 pin 8. If the signal from Q4 is below the threshold, IC41b/14 goes to logic '1'. This level is fed back via SK7 pin 7 to disable the gate, IC2b, and inhibit the output to the measurement system.

35 The $\overline{\text{GATE}}$ signal enters the system at SK7 pin 17 and is inverted in IC1c. The resulting signal and the output of the comparator, IC1b, are fed to IC4a. If both inputs are at logic '1', indicating that the channel C signal level is too low while the gate is open, the continuous signal latch, IC4c and d, is set. The latch output is fed to the microprocessor system via SK7 pin 11, and prevents the result of any measurement made during that gate period from being displayed.

36 The U signal at SK7 pin 16 is at logic '1' when channel C is selected. A buffered version of this signal is fed to SK7 pin 1 via IC2c, and disables channel A at IC41a, shown in Fig 8. When channel C is not selected, SK17 pin 16 is at logic '0'. This level is inverted and buffered in IC4b and IC1d, and is fed to IC41b, shown in Fig 8, via SK7 pin 13. IC41b is held reset, inhibiting the channel C signal at IC2b via SK7 pin 7.

THE MEASUREMENT SYSTEM

Functional Description

37 The measurement circuits of the instrument are provided by three custom-built integrated circuits. These are the two Multiple Counter and Control (MCC) circuits, MCC1 and MCC2, and the Timing Error Correction (TEC) circuit. A block diagram is shown in Fig 6.4.

38 The circuits within MCC1 and MCC2 are configured by the microprocessor according to the measurement function in use. The recipromatic counting technique is used. With this technique the measured signal, not the counter clock pulses, controls the start and stop of the measurement period (gate time) as shown in Fig 6.5. The gate time therefore extends over an integral number of cycles of the measured waveform. The gate time is measured by counting the clock pulses which occur while the gate is open. This leads to timing errors at both ends of the gate time, as shown. The TEC circuit enhances the measurement accuracy by compensating for these errors.

39 For all measurement functions except FREQ A and PERIOD A the signals to be measured are fed directly to MCC2. For FREQ A and PERIOD A the channel A signal is scaled by two and fed to the $\overline{\text{C}}$ input of MCC2. When FREQ C is selected, the prescaler is disabled by the CHANNEL A INHIBIT signal from the channel C system.

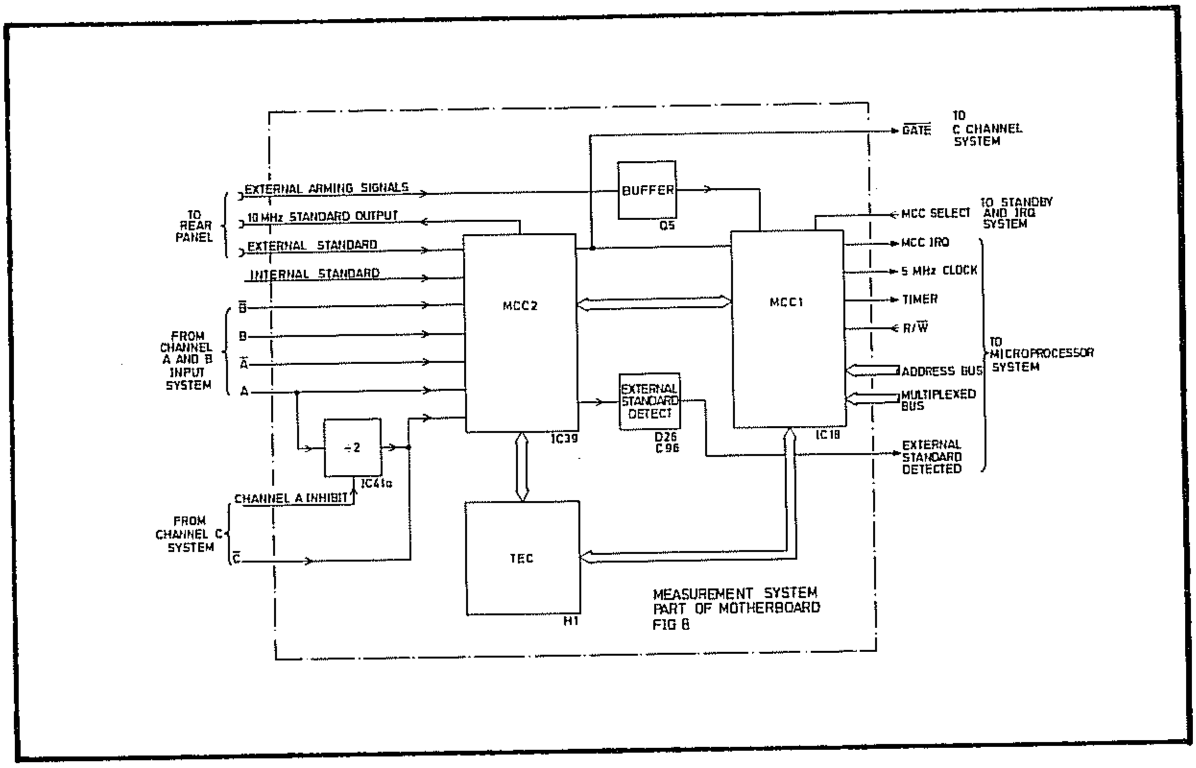


Fig 6.4 The Measurement System

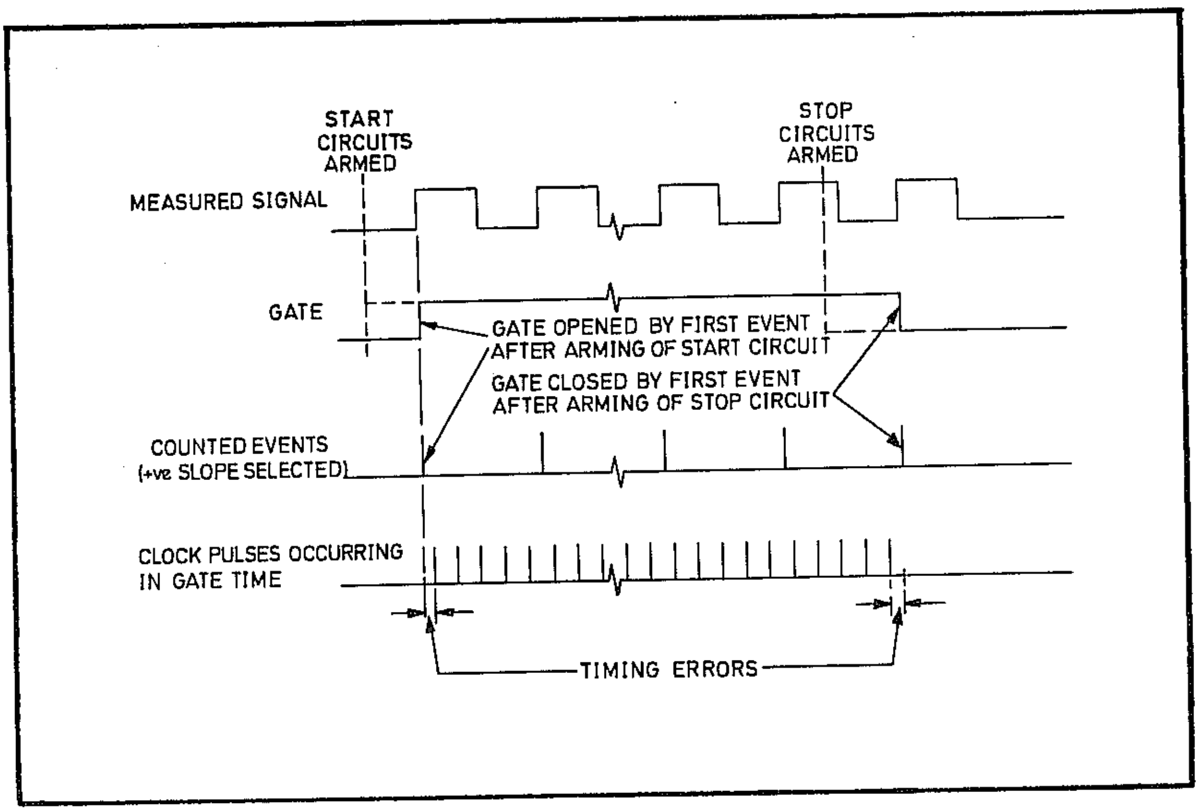


Fig 6.5 Basic Recipromatic Counting Technique

40 At the end of each measurement period MCC1 generates an interrupt request for the microprocessor system. The registers within MCC1 are addressed using the address bus and the MCC SELECT line. The measured value is transferred to the microprocessor system via the multiplexed bus.

41 The internal and external frequency standard inputs are both fed to MCC2. The system will operate from the external standard provided that the input is of sufficient amplitude. A 10 MHz output, derived from the frequency standard in use, is made available at a socket on the rear panel.

Circuit Description

42 The circuit diagram is shown in Fig 8 in Section 8.

Measured Signal Input

43 For all measurement functions other than FREQ A and PERIOD A, the differential outputs from channel A and channel B are applied to the measuring circuit at IC39/15, 16, 17 and 18. For the FREQ A and PERIOD A functions, the A signal frequency is divided by two in IC41a and fed to IC39/19.

44 For the FREQ C and RATIO C/B functions (1992 only) the $\overline{C}$ signal is fed to IC39/19. For these functions IC41a/5 is held at logic '1' by the PST1 control line (CHANNEL A INHIBIT) from the channel C system. As a result, IC41a is held set and the A signal is inhibited from reaching IC39/19.

Reference Frequency

45 The internal reference signal is applied to IC39/2 and the external reference signal, if present, to IC39/3. A buffered version of the external reference is present at IC39/24, and is applied to the detector D26/C96/R129. The detector output is fed to IC23/6, and is read periodically by the microprocessor. If the level is above the TTL logic '1' threshold, the microprocessor sets IC39/38 to logic '0' and the measurement system switches to use the external reference.

46 A 10 MHz signal, derived from the frequency standard in use, is present at IC39/37, and is fed to the 10 MHz STD OUTPUT socket on the rear panel via PL19 pin 2.

47 A 10 MHz reference signal, derived from the frequency standard in use is present at IC39/36. This signal is applied to the TEC, H1, at pin 6, and, after inversion in IC29e, to IC18/24.

Microprocessor Clock and Timer

48 A 5 MHz clock signal for the microprocessor (and the GPIB microprocessor if fitted) is taken from IC18/2. A 39.0625 kHz clock signal for the microprocessor timer is taken from IC18/4.

Channel C Gate and Reset

49 A $\overline{GATE}$ signal (logic '0' during the measurement period) and a $\overline{RESET}$ signal (negative going pulse at the end of each measurement period) are taken from IC39/27 and IC18/40 and fed to the channel C system via PL7 pins 17 and 15.

External Arming Input

50 Signals connected to the EXT ARM INPUT socket on the rear panel are fed to IC18/27 via PL19 pin 1 and the amplifier stage, Q5.

Control Signals

51 The logic levels on lines Q0 to Q4, between IC18 and IC39 are shown in Table 6.1. These levels are stable if:

(1) No signals are applied to any of the channel inputs
(2) Auto-trigger is disabled on channels A and B.

TABLE 6.1

Control Signals

Measurement	Control Line				
Function	Q0	Q1	Q2	Q3	Q4
FREQ A	1	1	0	1	0
PERIOD A	1	1	0	1	0
FREQ B	1	0	0	1	0
PERIOD B	1	0	0	1	0
FREQ C	1	1	0	1	0
T.I. A→B	0	0	1	1	0
T.I. B→A	0	0	0	1	0
TOTAL A by B	1	0	0	1	1
TOTAL B by A	1	0	1	1	1
RATIO C/B	1	1	0	1	1
RATIO A/B	1	0	1	1	1
Special function 72	1	1	1	0	1
Special function 73	1	1	1	0	0
Special function 74	1	1	1	0	1
Special function 75	1	1	1	0	0

NOTE (1) The FREQ B, PERIOD B and T.I. B→A functions are obtained with special function 21 active.

(2) Special functions 72 to 75 can only be active when CHECK is selected.

THE DISPLAY SYSTEM

Functional Description

52 A block diagram of the system is given in Fig 6.6. The GPIB indicators, the GATE indicator, the channel A and channel B TRIGGER indicators and the STANDBY indicator are held on or off by control signals from other systems. The remainder of the display is multiplexed under the control of the display drivers.

53 To update the display, the microprocessor selects the appropriate display driver, using the MODE 1 and MODE 2 control lines. A string of nine 8-bit words (a control word and eight data words) is then put onto the bus. Each word is entered into a memory within the display driver under the control of the STROBE signal.

54 The display driver puts the data words onto its output bus in turn. For each data word, the appropriate numeric indicator or group of LEDs is enabled by a signal on its control line.

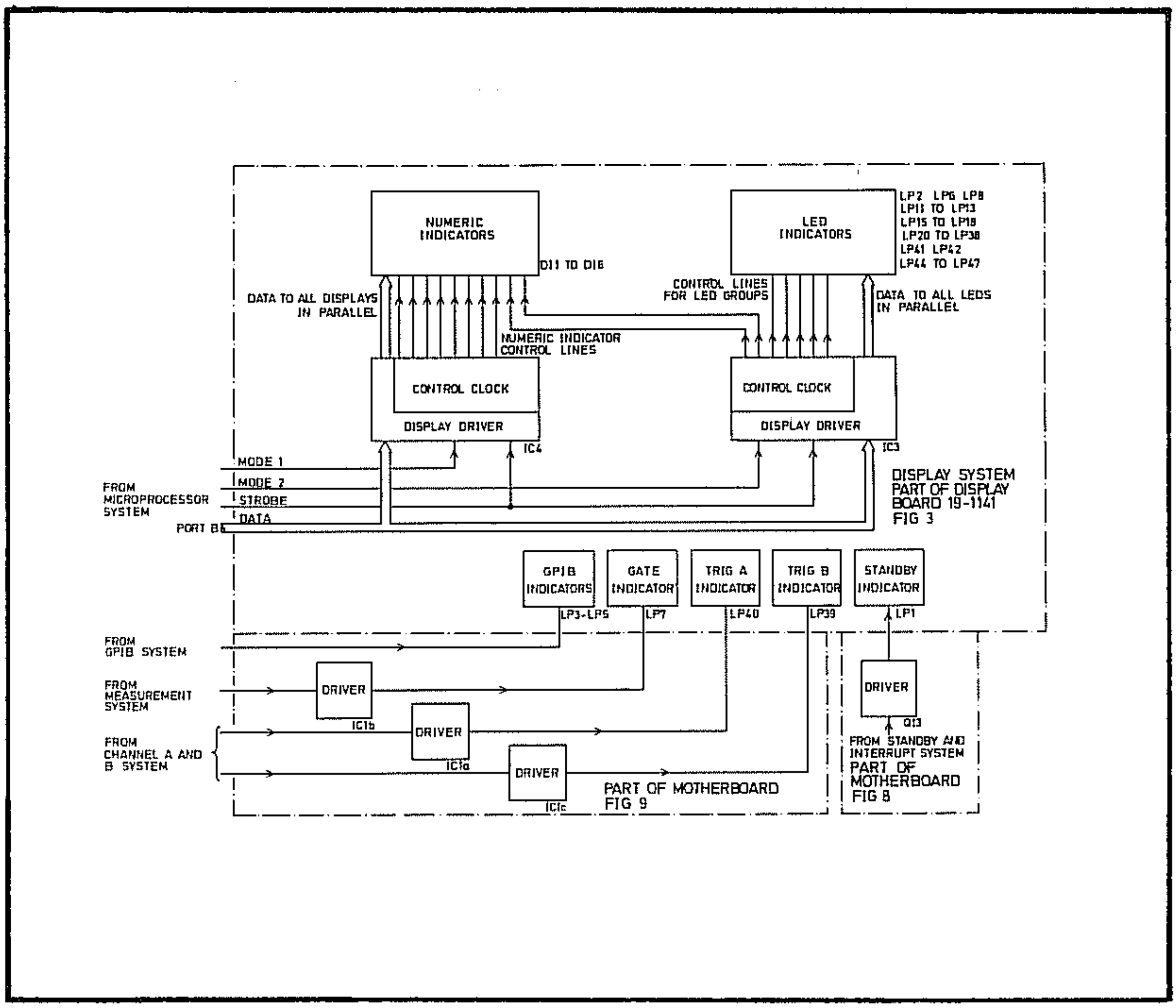


Fig 6.6 The Display System

Circuit Description

55 The circuit diagram is shown in Fig 3 in Section 8. The GPIB indicators, LP3, LP4 and LP5, are driven via SK1 from the GPIB system. The GATE indicator, LP7, is driven from the measurement system via a driver stage, shown in Fig 9, and SK2 pin 11. The TRIG indicators, LP39 and LP40, are driven from the channel A and B system via driver stages, shown in Fig 9, and SK2 pins 7 and 3. The STANDBY indicator, LP1, is driven via SK1 pin 8 from the standby and interrupt system. The remaining LED indicators and the numeric indicators DI5 and DI6 are controlled by the display driver, IC3. Numeric indicators DI1 to DI4 are controlled by IC4.

56 Display data are stored in memory within IC3 and IC4. To change the data, the microprocessor puts a control word on the port B bus. The microprocessor writes this word into the display drivers by means of a negative pulse applied to the DISPLAY STROBE line at SK1 pin 4. The control word determines the operating mode of the display drivers.

57 The microprocessor then selects the display driver required by setting a logic '0' on the appropriate MODE line, at SK1 pin 3 or 6. Eight words containing display data are written into the selected display driver via the port B bus, controlled by eight negative-going pulses on the DISPLAY STROBE line.

58 The output of each display driver is multiplexed, under the control of an internal clock. Eight-bit display data (for seven segments + decimal point or eight LED indicators) are put onto the device output bus (pins 1 to 4 and 24 to 27). A positive pulse is then applied to the enablement line of the device or group of indicators which is to display the data. The enablement line waveforms consist of 500µs positive-going pulses at approximately 250 pps.

THE KEYBOARD SYSTEM

Functional Description

59 A block diagram of the system is given in Fig 6.7. The encoding of the keyboard data is performed within the system without microprocessor action. An interrupt request (IRQ) is made to the microprocessor when encoding is complete. Data transfer is initiated by the KEYBOARD ENABLE signal from the microprocessor.

60 The 32 keys are divided into two 16-key matrices. When a key is pressed, its position is encoded into a 5-bit word. One bit, carried on the KEYBOARD EXTEND line, indicates the matrix in which the key is located. The remaining bits indicate the position of the key within the matrix.

61 When a key is pressed, the encoder examines both matrices simultaneously, and generates a 4-bit code representing the key position. The same four bits are generated regardless of the matrix in which the key is located.

62 If the key pressed is in the extended key matrix, one of the inputs to the NAND gate is pulled low. The KEYBOARD EXTEND line is then set to logic '0'. If the key is in the non-extended matrix the inputs to the NAND gate are isolated from the key line by one of the diodes, and the KEYBOARD EXTEND line remains at logic '1'.

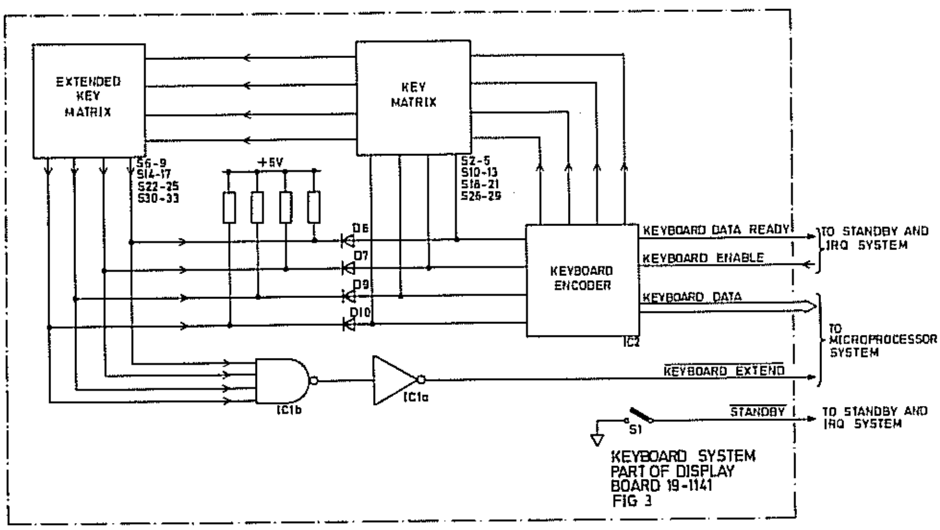


Fig. 6.7 The Keyboard System

Circuit Description

63 The circuit diagram is given in Fig 3 in Section 8. The keys are divided into two 16-key matrices, having common row lines connected to the encoder at IC2/7, 8, 10 and 11. The matrices have separate column lines, connected in pairs to IC2/1, 2, 3 and 4.

64 The encoder normally holds the row lines at logic '0'. When a key is pressed the corresponding column line is pulled to logic '0'. The encoder then scans the keyboard and stores a 4-bit code, corresponding to the row and column of the key, in an internal register. Because the column lines are connected to the encoder in pairs, it cannot find which matrix contains the key.

65 The KEYBOARD EXTEND line indicates which matrix contains the key that is pressed. The inputs to IC2 are normally held at logic '1', so that SK2 pin 9 is at logic '1'. If a key in the extended matrix (column lines connected directly to the inputs of IC1b) is pressed,

one input of IC1b is pulled to logic '0' and SK2 pin 9 will go to logic '0'. The column lines of the other matrix are isolated from the inputs of IC2 by D6, D7, D9 and D10, so that the logic level at SK2 pin 9 is not changed when a key in this matrix is pressed.

66 When the key-position code has been stored, the encoder sets the KEYBOARD DATA READY line, at SK2 pin 4, to logic '1' giving a microprocessor interrupt. The microprocessor sets IC2/13 to logic '0', using the KEYBOARD ENABLE line, and the encoder puts the 4-bit code onto the bus. The microprocessor reads the code and the state of the KEYBOARD EXTEND line to find which key has been pressed.

THE MICROPROCESSOR SYSTEM

Functional Description

67 A block diagram of the system is given in Fig 6.8. The microprocessor used has a 5-bit bus for the high-order address bits and an 8-bit multiplexed bus which is used for the low-order address bits and for data. The low-order address bits are strobed into the address latch, which holds them on an 8-bit address bus, to free the multiplexed bus for data.

68 Two latches, fed from port B of the microprocessor, are used to maintain voltage levels on the instrument control lines. A third latch is used to read the status of the instrument flags via port B. The latches and registers for the connection of the multiplexed bus to the measurement system are in the measurement system, and are controlled by the MCC SELECT signal. The display data latches are in the display system, and are controlled by strobe and chip select signals obtained from port A.

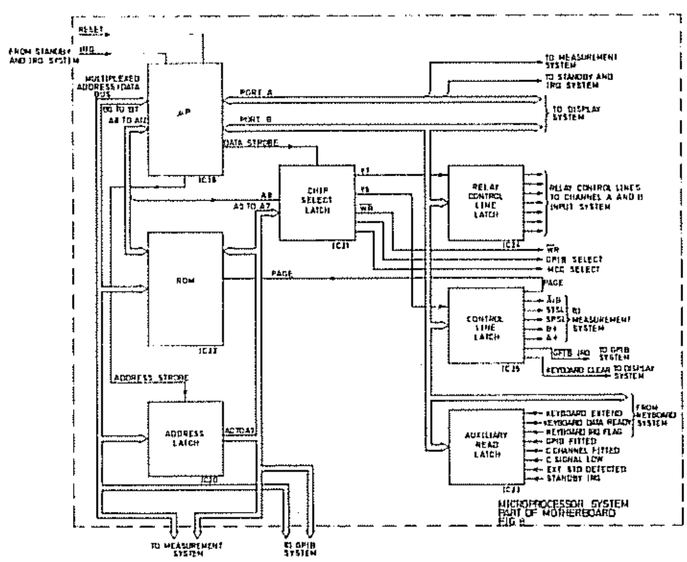


Fig 6.8 The Microprocessor System

Circuit Description

69 The circuit diagram is given in Fig 8 in Section 8. The microprocessor clock and timer signals are generated in the measurement system, and are fed to IC19/39 and IC19/37. A $\overline{\text{RESET}}$ signal is generated in the standby and IRQ system when the instrument is switched on or off, and is fed to IC19/1.

70 The microprocessor bus for the high-order address bits is designated A8 to A12. The multiplexed bus, used for the low-order address bits and for data is designated B0 to B7. The microprocessor also has two input/output ports PA0 to PA7 and PB0 to PB7.

Multiplexed Bus Operation

71 The microprocessor puts IC19/6 (ADDRESS STROBE) to logic '1' and IC19/4 (DATA STROBE) to logic '0'. This enables the address latch, IC20 (IC20/11 at logic '1') disables the ROM, IC22 (IC22/20 at logic '1') and disables the address decoder, IC21 (IC21/6 at logic '0').

72 The address is put onto lines B0 to B7 and A8 to A12. When the lines have settled the ADDRESS STROBE line is taken to logic '0'. The low-order bits of the address are latched into IC20, and are held on address lines A0 to A7. Lines B0 to B7 are now free for use as a data bus.

Address Decoding

73 The levels on address lines A6 to A12 are decoded in IC21 to provide the following outputs:

(1) $\overline{\text{MCC SEL}}$, the chip-select signal for IC18.
(2) $\overline{\text{GPIB SEL}}$, the chip-select signal for the GPIB address decoder.
(3) $\overline{\text{WR}}$, the write control signal for H2.
(4) Y6, the chip select signal for output latch IC25.
(5) Y7, the chip select signal for output latch IC24.

74 These outputs are only available when IC21 is enabled by a logic '1' at IC21/6 and a logic '0' at IC21/4 and 5. The level at IC21/6 is set by the DATA STROBE output at IC19/4, which is at logic '1' when the multiplexed bus is available for data transfer. All outputs from IC21 are decoded from addresses with lines A9 to A12 at logic '0', when IC21/4 and 5 are held at logic '0' by the output from IC27a, b and d.

Input and Output Latches

75 The logic levels required on the instrument control lines and on the PAGE line (most significant bit of RAM address) are set into the output latches, IC24 and IC25, from data port B of the microprocessor. The latch strobe signals are decoded in IC21. Data may be read by the microprocessor from the input latch, IC23. The latch strobe signal is provided via data port A of the microprocessor.

THE STANDBY AND IRQ SYSTEM

Functional Description

76 The system generates reset signals for the microprocessor and GPIB interface, and the standby switching signal for the power supply system. It also combines the IRQ signals from the GPIB interface, the measurement system and the keyboard system for connection to the microprocessor. A block diagram is given in Fig 6.9.

77 Reset signals for the microprocessor and the GPIB interface are generated whenever power is applied to or removed from the instrument's power supply system.

78 On switching to standby, the standby signal from the keyboard system sets the standby IRQ latch. The latch outputs provide the standby IRQ and a standby flag for the microprocessor system. The standby IRQ output also clocks the standby ON/OFF latch to the set state. This provides signals to switch the power supply to standby, light the STANDBY indicator and disable IC30b, so inhibiting the other IRQs. At the end of the microprocessor interrupt routine the standby IRQ latch is reset, removing the standby IRQ. The state of the standby ON/OFF latch is not changed.

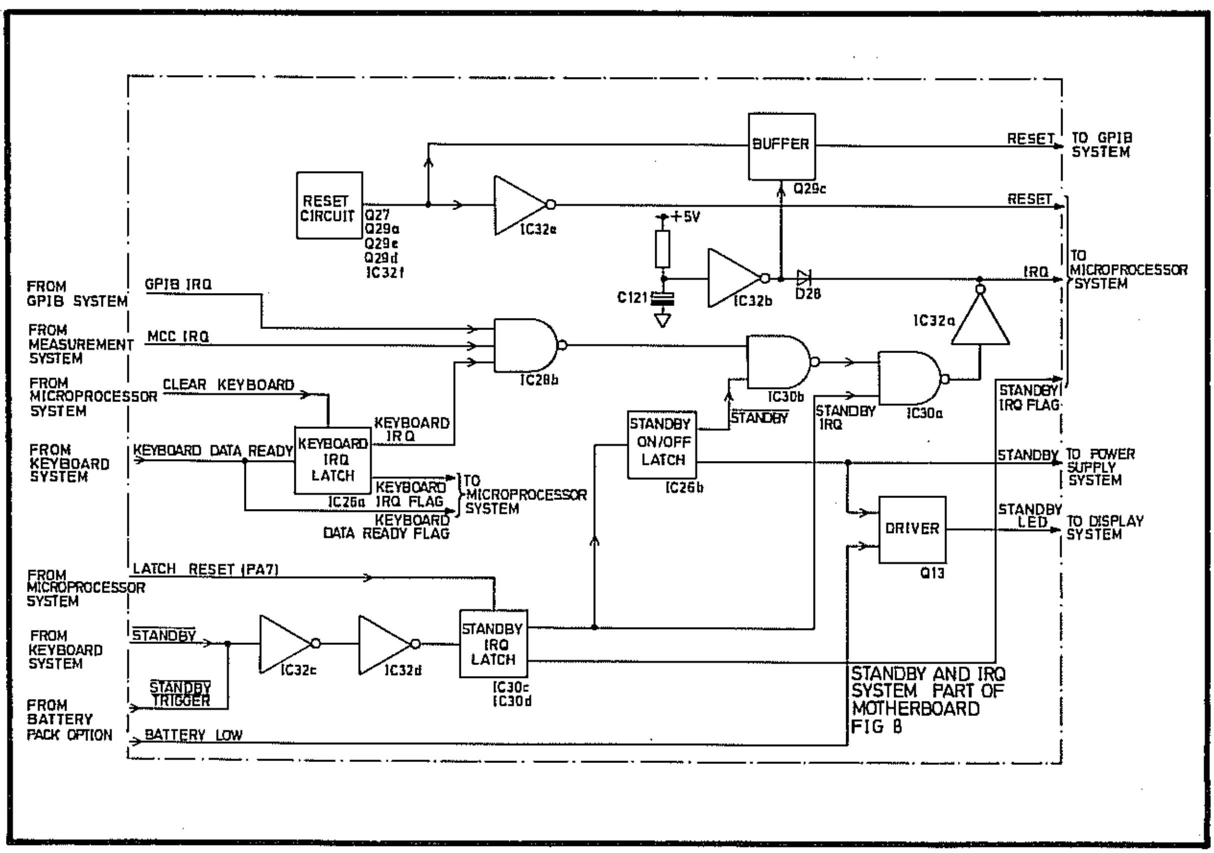


Fig 6.9 The Standby and IRQ System

79 While the instrument is in standby, the input to IC32b is held low and the IRQ input to the microprocessor is held high via D28. This inhibits all IRQs. The output from IC32b also holds the GPIB interface reset via Q29c.

80 On return from standby, the standby IRQ latch is again set by the standby signal from the keyboard system. The standby ON/OFF latch is clocked to the reset state, the power supply is returned to normal operation and IC30b is enabled. The input to IC32b rises as C121 charges, removing the reset signal from the GPIB interface and enabling the microprocessor IRQ input. The microprocessor is now able to accept the IRQ from IC30a. At the end of the restart sequence the standby IRQ latch is reset.

81 When the encoder in the keyboard system has data ready to be read by the microprocessor, the keyboard IRQ latch is clocked via the KEYBOARD DATA READY line. The latch outputs provide the keyboard IRQ and a keyboard IRQ flag. Once the keyboard has been identified as the source of the interrupt, the latch is reset by the microprocessor.

Circuit Description

82 The circuit diagram is shown in Fig 8 in Section 8.

Reset Circuit

83 The $\overline{\text{RESET}}$ signal is generated in the circuit containing Q27, Q29a, d and e, and C125. When the instrument is switched on, the input to IC32f is held low until C125 charges through R215, Q29a and R216. The output at IC32f/12 goes to logic '1' when power is applied, but drops to logic '0' after approximately 300 ms. This output is inverted by IC32e to provide the microprocessor reset and by Q29c to provide the GPIB reset.

84 If there is a reduction in the +5 V STANDBY supply, due to the instrument being switched off or to power failure, the potential across R217 falls. The potential at Q27 emitter is maintained by the charge in C125, so Q27 conducts. The current in R218 makes the base of Q29d positive, so the transistor conducts and holds the base of Q27 low until C125 is completely discharged. This ensures that a good reset action is obtained, even if the power is quickly restored.

Standby Operation

85 On switching to standby, PL1 pin 14 is taken to 0 V by the STANDBY key. Debouncing is provided by R158 and C126. The leading edge of the signal is sharpened in IC32c, C118, R151 and IC32d, and sets the standby IRQ latch, IC30c and d.

86 The negative-going output from IC30c/10 is passed via IC30a, IC32a and R152 to IC19/2, to provide a microprocessor interrupt. The positive-going output from IC30d/11 forms the standby IRQ flag (read by the microprocessor via IC23 during the interrupt routine) and clocks the standby latch, IC26b, to the set state.

87 The logic '0' level at IC26b/8 switches on Q13, and provides power for the STANDBY indicator via PL1 pin 8. The same output is applied to IC30b/5, and disables the other interrupts, which are connected to IC30b/6.

88 The logic '1' level at IC26b/9 shuts down the power supplies except the +5 V STANDBY supply.

89 At the end of the interrupt routine the microprocessor resets the standby IRQ latch by applying logic '1' to IC30c/8 from IC19/7.

90 On return from standby, the standby IRQ latch is again set. This provides a microprocessor interrupt and sets the standby IRQ flag, as before. The positive-going output from IC30d/11 clocks the standby latch back to the reset state, so that the STANDBY indicator is turned off and the power supplies are restored. The microprocessor resets the standby IRQ latch at the end of the interrupt routine.

91 When the instrument is operating from the battery pack in the battery-save mode, the STANDBY TRIGGER control line (PL21 Pin 9 on Fig. 9) is taken to logic '0' after approximately one minute by the battery pack. This switches the instrument to the standby mode. The instrument is returned to the measurement mode by operation of the STANDBY key.

The IRQ Circuits

92 The KEYBOARD DATA READY line, at PL2 pin 4, goes to logic '1' when the keyboard encoder has data available. This clocks IC26a to the set state to provide a keyboard IRQ flag at IC23/11 and an interrupt signal at IC28b/9. Interrupts from the measurement system (MCC IRQ) and the GPIB interface (GPIB IRQ) are connected to IC28b/12 and IC28b/10 and 13.

93 If any of these interrupts occurs, IC28b/8 and IC30b/6 will go to logic '1'. Provided the standby latch, IC26b, is not set, IC30b/5 will be at logic '1' and the interrupt signal passes via IC30a and IC32a to IC19/2.

94 When the instrument is switched into or out of the standby state, the standby IRQ latch, IC30c and d, is set. The standby IRQ from IC30c/10 is fed to IC19/2 via IC30a and IC32a.

95 The circuit comprising R220, C121, IC32b and D28 disables the microprocessor interrupt input and holds the GPIB microprocessor reset line low (via Q29c) while the +5 V power supply to R220 is switched off. On return from standby, C121 charges and IC32b/4 goes to logic '0'. The microprocessor interrupt input is enabled and the GPIB microprocessor is reset. The delay in enabling the interrupts prevents the standby IRQ which occurs on return from standby from being acted upon before the power supplies are fully restored.

Functional Description

96 A block diagram of the system is given in Fig 6.11. The AC supply enters at a plug mounted on the rear panel, and passes via a fuse and RFI filter, mounted on the motherboard, to the line switch.

97 The switched supply is connected to the primary winding of the power transformer via the operating voltage range selector. This has the form of a plug-in printed circuit board, which is positioned according to the line voltage.

98 The transformer has a tapped secondary winding, which supplies two rectifiers.

99 The rectifiers feed regulators providing +11.2 V, -11.2 V, +5 V, +5 V and -5.2 V. Alternatively the raw supplies can be supplied by the Battery Pack Option, if fitted. The -5.2 V regulator and one of the +5 V regulators, which supply most of the instrument's circuits, are shut down by a signal from the microprocessor system when the instrument is switched to standby.

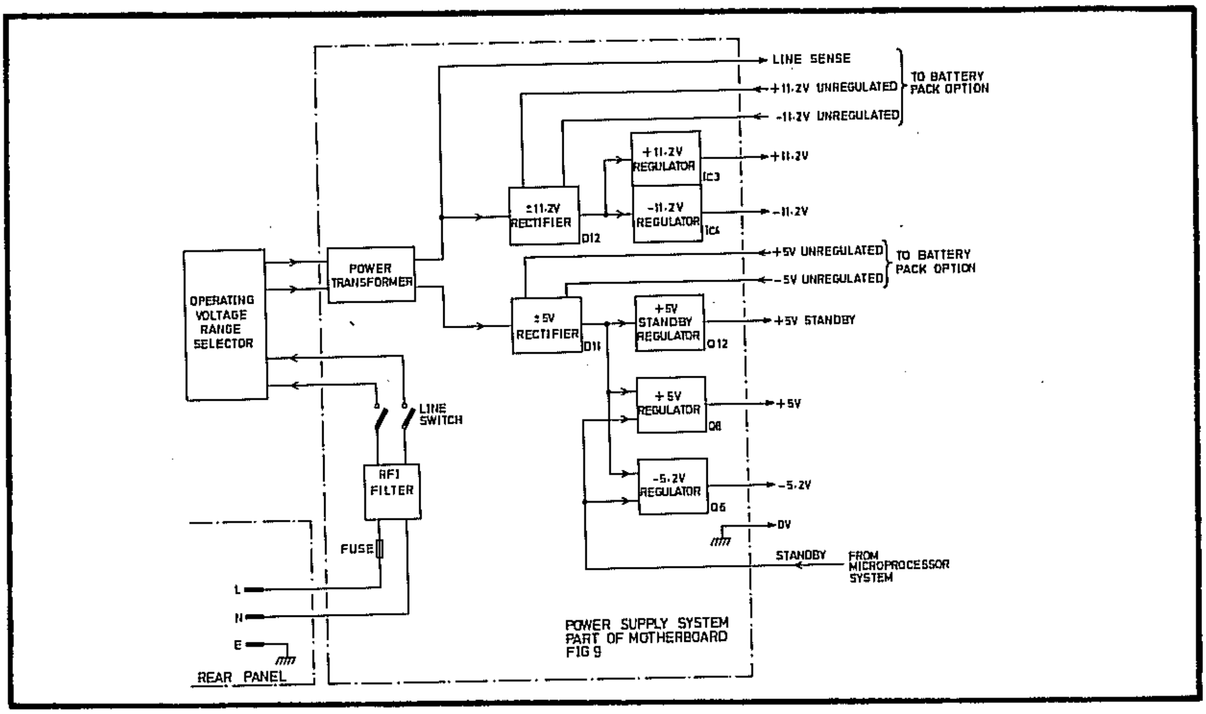


Fig 6.10 The Power Supply System

Circuit Description

100 The circuit diagram is shown in Fig 9 in Section 8. AC power connected at the power input plug passes via fuse FS1 and the RF filter, formed by L1, L2, C46, C47 and C48, to the POWER switch, S1b. The switched supply is connected to the primary windings of T1 via the tracks of a printed circuit board, which is inserted in SK8.

101 The secondary windings of T1 supply the ±5 V rectifier, D11, C49 and C50, and the ±11 V rectifier, D12, C52 and C59. When the battery pack is in use, raw DC supplies at ±5 V and ±11 V are provided via PL21.

102 Regulated supplies at ±11.2 V are provided by the integrated circuit regulators, IC3 and IC4. The common terminals of these regulators are held at approximately -0.7 V and +0.7 V by diodes D13 and D14.

103 Regulated supplies at +5 V are provided by two discrete component regulators having series elements Q8 and Q12. The non-inverting inputs to the comparators, IC31a and IC31c, are connected to a +2.5 V reference voltage, derived in the hybrid circuit H2 in Fig 8. Potential dividers formed by elements of R49 hold each inverting input at half the output voltage of the assocated regulator.

104 A regulated supply at -5.2 V is provided by a discrete component regulator having Q6 as its series element. The comparator inputs are held at approximately 0 V. The potential divider controlling the inverting input is connected across the +5 V and -5.2 V rails.

Standby Mode

105 When the instrument is switched to standby, the standby latch, IC26b on Fig 8, is clocked to the set state. The base of Q11 is pulled high, and IC31a/3 is pulled low. The base of Q9 is pulled low by IC31a, the base current of Q8 is cut off and the regulator is shut down. When the voltage of the +5 V rail falls IC31b/6 goes more negative. The base of Q7 is taken towards 0 V by IC31b, so that the base current of Q6 is cut off and the -5.2 V regulator is shut down.

THE FREQUENCY STANDARD SYSTEM

Functional Description

106 The internal frequency standards 19-1147 and 19-1208 are 10 MHz oscillators. Frequency standards 9423 and 9444 each comprise a 5 MHz oscillator and a frequency doubler. A block diagram of the 9423 and 9444 oscillators is shown in Fig 6.11.

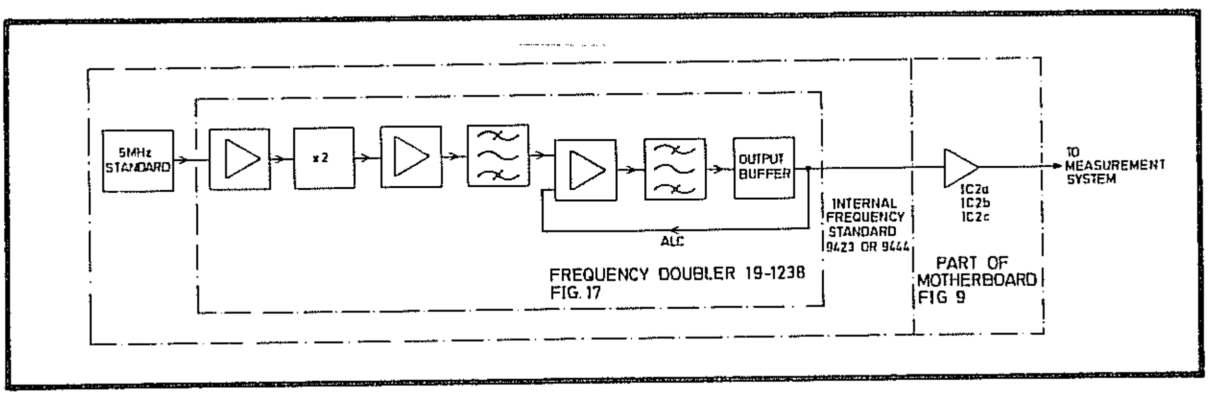


Fig 6.11 9423 and 9444 Oscillators

107 For all oscillator types the 10 MHz signal is passed to the measurement system via a buffer on the motherboard.

108 Signals from an external frequency standard are applied to a signal conditioning circuit on the motherboard. If a 10 MHz external frequency standard is used, the output of this circuit may be connected directly to the measurement system. For external frequency standards at sub-multiples of 10 MHz, the external frequency multiplier option is fitted between the conditioning circuit and the measurement system.

Circuit Description

Frequency Doubler

109 The circuit diagram of the frequency doubler, used with frequency standards 9423 and 9444, is given in Fig 17 in Section 8. The 5 MHz input is applied to the balanced amplifier containing Q1 and Q2. The base of Q3 is driven by the differential outputs from the amplifier, via D1 and D2, so that the frequency here is 10 MHz.

110 The 10 MHz signal is amplified and filtered in the two stages containing Q3 and Q5, and fed to pin 3 via the buffer, Q6.

111 The output signal is fed back via C6 to switch Q4 on during the positive peaks of the signal. The gain of Q5 is controlled by the potential across C3, which charges via R12 and discharges via Q4. If the output signal increases, the time for which Q4 conducts increases so that the mean potential across C3 decreases. The resulting decrease in gain of Q5 provides automatic level control.

Internal Frequency Standard Buffer

112 The buffer circuit is shown in Fig 9 in Section 8. The 10 MHz input at PL14 pin 4 is shaped and buffered in IC2a, IC2b and IC2c before being fed to the measurement system at IC39/2. The inverting inputs of IC2 are connected to the bias voltage at IC2/11.

External Frequency Standard Buffer

113 The buffer circuit is shown in Fig 9 in Section 8. The signal connected to the EXT. STD. INPUT socket on the rear panel is fed to PL20 pin 4. Protection against excessive signal amplitude is provided by D6, D7 and R32.

114 The buffer comprises IC14a, IC14b and IC14c. The inverting inputs are connected to the bias voltage at IC14/11. The final stage has feedback connected via R11 to give a Schmitt trigger action.

115 The differential output of the final stage is fed to PL16 pins 6 and 9 for use in the reference frequency multiplier option. If the option is not fitted, LK1 is fitted between pins 8 and 9 of PL16 to connect the signal to the measurement system at IC39 pin 3.

THE REFERENCE FREQUENCY MULTIPLIER (OPTION 10)

Functional Description

116 The block diagram of the multiplier is given in Fig. 6.12. The input to the circuit is taken from the EXT STD INPUT socket on the rear panel, via a signal conditioning circuit on the motherboard. The output of the circuit is passed to the measurement system. The $\overline{\text{BYPASS}}$ control line is held at logic '1' by the +5 V STANDBY supply.

117 The circuit contains a 10 MHz oscillator operating in a phase-locked loop. If an external reference signal of suitable amplitude is present at the EXT. STD. INPUT socket, a rectangular waveform at the reference frequency is fed to the external reference detector. The detector output triggers the switching signal generator. The oscillator is then enabled and the bypass logic connects the 10 MHz from the buffer and splitter to the output.

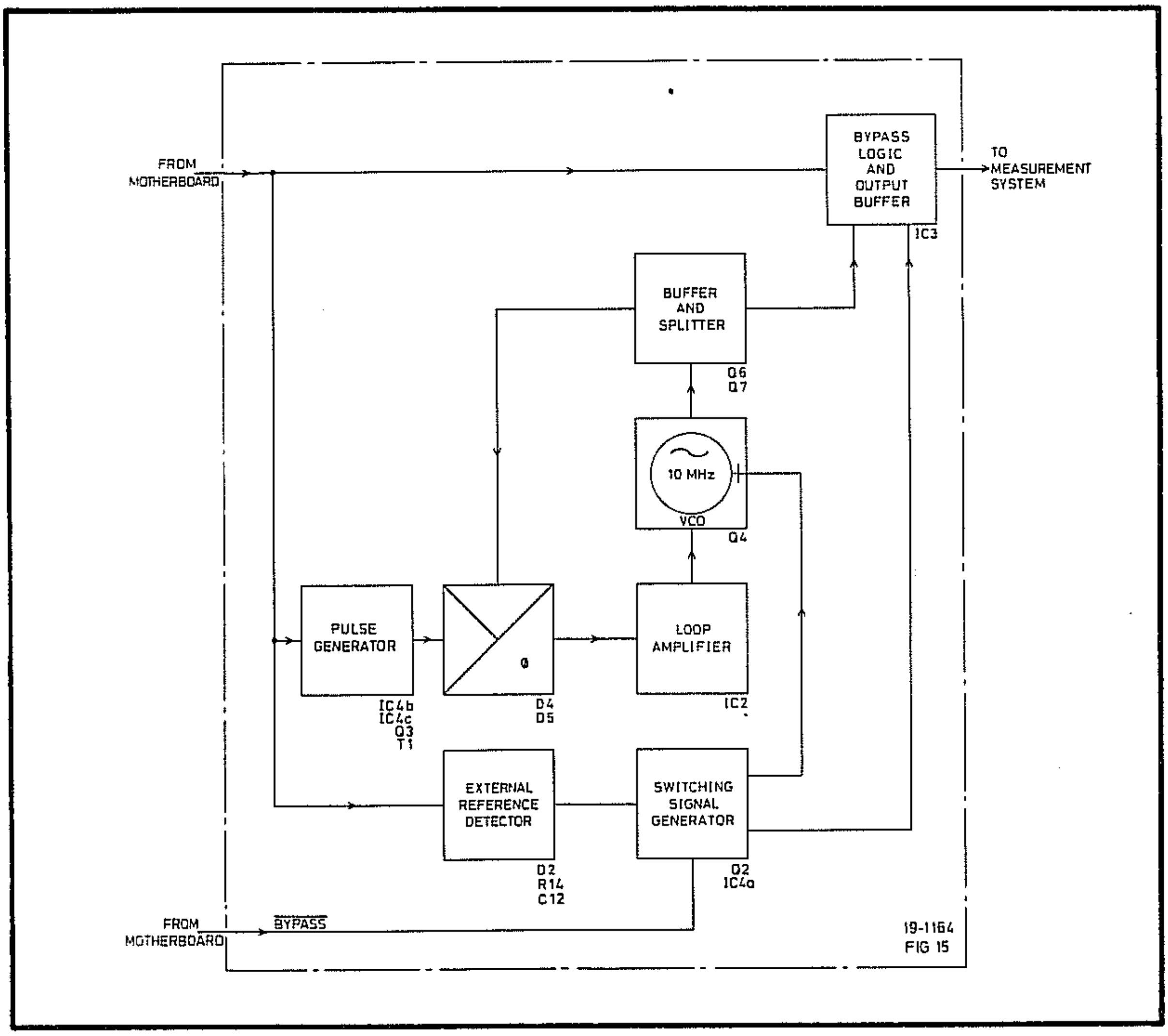


Fig. 6.12 The Reference Frequency Multiplier

118 The pulse generator output is fed to the phase detector, and forms the reference signal for the phase-locked loop. The phase detector is of the sampling type, allowing the oscillator to be phase-locked to a reference signal of 10 MHz or any sub-multiple of 10 MHz.

119 If no external reference signal of suitable amplitude is present at the EXT. STD. INPUT socket, the reference detector output does not trigger the switching signal generator. The oscillator is disabled and the bypass logic connects the circuit input to the output.

Circuit Description

120 The circuit diagram is given in Fig. 15 in Section 8.

Input Circuit and Pulse Generator

121 Two antiphase waveforms derived from the external reference signal enter the system at SK16 pins 6 and 9. The waveform from pin 9 is converted from ECL to TTL levels in Q1 and squared in IC4d before being applied to the pulse generator, IC4b and IC4c. The operation of this circuit is illustrated in Fig. 6.13.

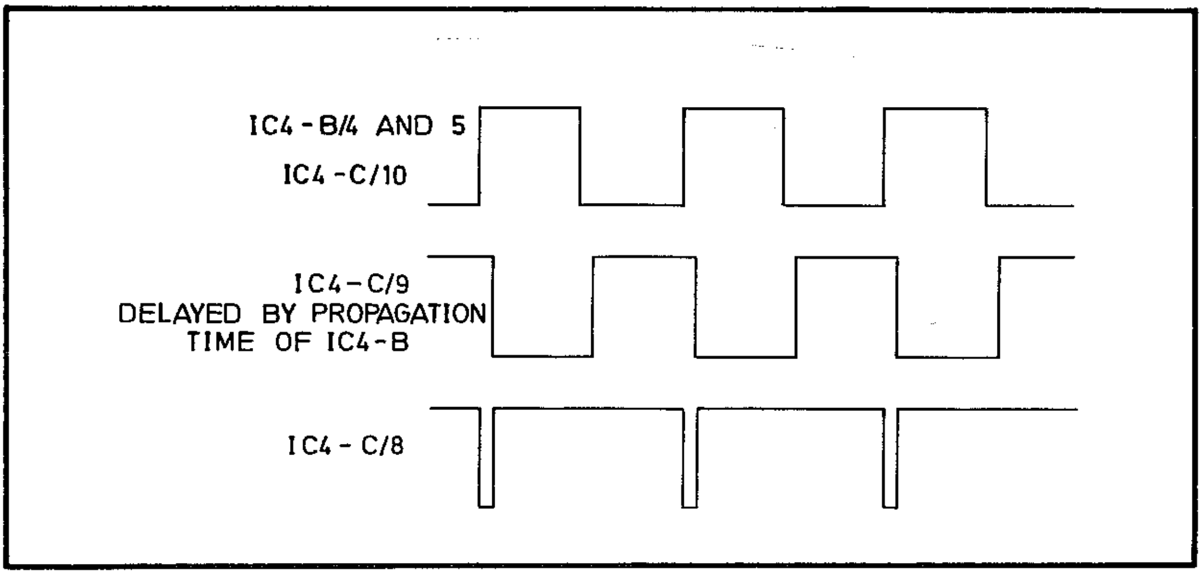


Fig. 6.13 Pulse Generator Waveforms

122 The negative-going pulses at IC4c/8 are used to switch Q3, which drives the transmission-line type transformer, T1. The transformer acts as a phase splitter, so that, for the duration of each pulse from IC4c/8, the sampling bridge of the phase detector is held forward biased, with the D4A/D5A and D4B/D5B junctions symmetrical about 0 V.

The Phase-Locked Loop

123 The loop oscillator active element is Q4. The oscillator frequency is controlled by the crystal XL1 and the varactor diode D1. The trimming capacitor C2 can be adjusted to compensate for a range of crystal and varactor tolerances.

124 The oscillator output drives a unity-gain cascode buffer, Q6/Q7. The buffered signal from the collector of Q7 forms the RF input to the phase detector.

125 When the sampling bridge of the phase detector is forward biased by the pulses from T1, the D5A/D5B junction adopts the same potential as the D4A/D4B junction. At other times the junctions are isolated from each other by the high impedance of the non-conducting diodes. The bridge output is therefore a series of samples of the loop oscillator waveform, taken at the frequency of the external frequency standard.

126 The phase detector output depends upon the relative frequency of the loop oscillator and the frequency standard, and upon the phase of the loop oscillator waveform at the instant of sampling. If the standard frequency is 10 MHz every cycle of the loop oscillator output is sampled, but if it is a sub-multiple of 10 MHz only every second, fourth, fifth or tenth cycle will be sampled. In all cases, however, provided the standard frequency is an exact sub-multiple of the loop oscillator frequency, the samples will be of constant amplitude. If the standard frequency is not an exact sub-multiple of the loop oscillator frequency the output pulses will be amplitude modulated.

127 The amplitude of each phase detector output pulse depends upon the instantaneous value of the loop oscillator waveform at the instant of sampling. The pulses are integrated in C7 to form the input to the loop amplifier IC2. When the loop is in lock the voltage across C7 maintains the voltage at IC2/6, and therefore across the varactor, at the level needed to maintain the loop oscillator at the lock frequency.

External Reference Detector and Bypass Switching

128 The output from IC4d/11 is fed to a detector formed by D2, C12 and R14. If no external reference signal is present at the EXT. STD. INPUT socket, SK16 pin 9 is held low, Q1 conducts and IC4d/11 is at logic '1'. The detector output, and therefore the base of Q2, is at +5 V and Q2 is switched off. A logic '0' level is applied to IC4a/2, giving a logic '1' at IC4a/3 and the base of Q5. The zener diode, D3, converts the logic levels from TTL to the level required to switch Q5. R8 and R9 provide ECL logic levels for IC3b and c.

129 With Q5 switched on the voltage across R4 holds the emitter of Q4 positive with respect to its base, disabling the oscillator. At the same time a logic '1' level taken from the junction of R8 and R9 is applied to IC3b/7 and IC3c/11. This disables IC3c and enables IC3a, so that the oscillator output line is open circuited and SK16 pin 6 is connected to SK16 pin 5 and 8 via IC3a and IC3d.

130 When an external reference signal is present at SK16 pin 9 the output from IC4d/11 is a TTL square wave at the external reference frequency. The detector output holds the base of Q2 negative, so that Q2 conducts and IC4a/2 is at logic '1'. Since IC4a/1 is held at logic '1' by +5 V at SK17 pin 4, IC4a/3 is at logic '0'. Under

these conditions Q5 is cut off and the loop oscillator is enabled. A logic '0' is applied to IC3b/7 and IC3c/11 from the junction of R8 and R9. This disables IC3a and enables IC3c, so that the oscillator output is connected to SK16 pins 5 and 8 via IC3c and IC3d.

THE GPIB INTERFACE (OPTION 55)

Introduction

131 The GPIB interface is a self-contained, microprocessor controlled system. It handles the transfer of data between its internal memory and the GPIB without involvement of the main instrument microprocessor. Data transfer is made one byte at a time, each transfer being controlled by the IEEE-488 handshake protocol. The circuit diagram is given in Fig 11 in Section 8.

132 The microprocessor $\overline{\text{RESET}}$ signal is derived from the standby and IRQ system. The clock signal is derived from MCC1, IC18, shown in Fig 8 in Section 8.

133 The microprocessor uses a multiplexed bus, the eight low-order bits being used for both address and data. The low-order address bits are put onto the bus first, and are latched into IC11 by the address strobe. The bus is then free for data use.

134 Data transfer between the microprocessors is initiated by an interrupt, and is controlled by a 3-wire handshake protocol. The transfer is in the form of a data string, the number of bytes in the string being indicated by the first byte.

Address Setting and Recognition

135 The microprocessor reads the settings of the address switches in switchbank S1, via its port B inputs, approximately every 1 ms and writes the settings into an address register within the general purpose interface adapter (GPIA) IC12.

136 When the interface address is set on the bus by the controller, it is recognised by the GPIA by comparison with the contents of the internal address register.

Reading From the Bus

137 When the interface is addressed to listen, the GPIA conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point IC12/27 is at logic '0', givng a logic '1' level at IC18d/11. This puts three of the bilateral switches in IC13 to the conducting state, so completing the RFD line. The logic '0' at IC12/27 also puts the buffers in IC14 and IC15 to the receive condition. Data from the bus enters the GPIA data-in register, and IC12/40 goes to logic '0' to provide an interrupt request to the microprocessor, IC9.

138 The microprocessor interrupt routine establishes the reason for the interrupt. The address decoder, IC8, is enabled via IC6c, IC6d, IC7a, IC7b and IC7c, using address lines GA7, 9, 10, 11 and 12. The decoder is addressed using lines GA4, 5 and 6, and gives the GPIA enable signal at IC8/15. The data-in register of the GPIA is addressed using the $R/\overline{W}$ line and lines GA0, 1 and 2. The microprocessor then reads the contents of the data-in register and transfers the data to memory.

139 When the data-in register has been read, the GPIA cancels the interrupt request and allows the data accepted (DAC) line to go high. The handshake routine then continues, and a further byte, if available is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

Writing to the Bus

140 When the GPIA is addressed to talk its internal data-out register will normally be empty. Under these conditions IC12/40 goes to logic '0' and provides an interrupt request to the microprocessor.

141 IC17a is in the reset state, giving a logic '1' at IC18d/12. Since IC12/27 is at logic '1' when the GPIA is addressed to talk, IC18d/13 is also at logic '1'. The resulting logic '0' at IC18d/11 open circuits three of the bilateral switches in IC13 to break the RFD line. The fourth bilateral switch conducts, due to the logic '1' at IC19c/10, and holds IC12/18 at 0 V. Even if the listening device asserts that it is ready for data, IC12 will not attempt to load the contents of the data-out register onto the bus.

142 The microprocessor interrupt routine establishes the reason for the interrupt. The microprocessor then enables the address decoder, IC8, via IC6c, IC6d, IC7a, IC7b and IC7c, using address lines GA7, 9, 10, 11 and 12. The decoder is addressed using lines GA4, 5 and 6, and gives the GPIA enable signal at IC8/15. The data-out register of the GPIA is addressed using the $R/\overline{W}$ line and lines GA0, 1 and 2, and a data byte is written into the register. The GPIA then cancels the interrupt request.

143 Following the data transfer, the microprocessor sets IC17a, using line PB7, to give a logic '0' at IC18d/12. This gives a logic '1' at IC18d/11, which enables three bilateral switches in IC13 and connects the RFD line. The fourth switch in IC13 is disabled, so releasing IC12/18 from 0 V. When the listening device asserts that is is ready for data, the GPIA loads the contents of the data-out register onto the bus and continues with the handshake routine.

144 When the data-out register has been read, the GPIA generates a further interrupt request. The microprocessor resets IC17a, using line PB6, giving a logic '1' at IC18d/12, so that the RFD line is again broken at IC13. The data transfer and data transmission sequence is then repeated.

Serial Poll

145 The status byte register of the GPIA is normally updated approximately every 1 ms by the microprocessor. When the interface is addressed to talk following the receipt of the serial poll enable (SPE) message, the GPIA puts the status byte onto the bus without further action by the microprocessor.

146 When the serial poll is completed, the controller sends the serial poll disable (SPD) message, which is detected by IC6a, IC6b, IC7d, IC18a and IC19b. The resulting logic '1' at IC17a/3 clocks IC17a to the reset condition, and gives a logic '1' at IC18d/12.

Data Transfer Between Microprocessors

147 Data transfer between microprocessors is made using the multiplexed data bus on both devices. Connection between the buses is made by means of a D-type latch, IC1 or IC2, depending on the direction of data transfer. All data transfers are initiated by the sending device. The first byte indicates the number of bytes to be transferred.

148 For data transfer to the GPIB microprocessor, the instrument microprocessor sets PL4 pin 22 ($\overline{\text{GPIB DATA IRQ}}$) low. This provides an interrupt request (IRQ) to the GPIB microprocessor via IC4d. As part of the interrupt routine, IC8 is enabled and addressed to give an enabling signal for IC5d. The microprocessor reads the IRQ flag via IC5d and data bus line 7 to establish that the IRQ is from the instrument and not the GPIA.

149 The GPIB microprocessor prepares to receive data, and then enables and addresses IC8 to give a signal which clocks IC16a via IC20b. The level set on line 0 of the data bus is transferred to IC16/5, and forms the ready for data (RFD) signal to the instrument microprocessor.

150 The instrument microprocessor enables and addresses IC3 to give an enabling signal to IC5c, reads the RFD signal, puts the first data byte on the bus and readdresses IC3 to give a clock signal which latches the data into IC1. It then addresses IC3 to give a clock signal for IC16b, so that the logic level set at IC16b/12 is transferred to IC16b/9 to form the data valid (DAV) signal to the GPIB microprocessor.

151 The GPIB microprocessor addresses IC8 to give a signal to enable IC5a, and reads the DAV signal via data bus line 6. It then cancels its RFD signal, addresses IC8 to give an output enable signal for IC1 (via IC20c) and reads the data. A data accepted (DAC) signal is sent via IC2 and the RFD signal is reset. The instrument microprocessor responds by cancelling its DAV signal and entering the next data byte into IC1. Data transfer continues in this manner until the required number of bytes have been received.

152 Data transfer from the GPIB microprocessor to the instrument processor follows a similar pattern. The IRQ signal is passed from port A line 0 via IC18b and IC4c. The IRQ flag is read by the instrument microprocessor during its interrupt routine, via IC5b (enabled by an output from IC3). The IRQ signal is cancelled by the instrument microprocessor setting data bus line 0 to logic '0' and then addressing IC3 to clock IC17b. The resulting logic '0' at IC17b/9 disables IC18b.

153 During data transfer from the GPIB interface to the instrument, the RFD signal is passed via IC16b and IC5a, the DAV signal via IC16b and IC5c, the DAC signal via IC1 and the data via IC2.

INTRODUCTION

1 This section is written in six parts, which relate to:

(1) Test equipment required.

(2) Dismantling and reassembly.

(3) Special functions for diagnostic purposes.

(4) Fault finding.

(5) Setting up instructions for use after repair, or if the instrument fails the overall performance verification.

(6) Overall performance verification procedure.

TEST EQUIPMENT REQUIRED

2 A complete list of the test equipment required to carry out the procedures described in this section is given in Table 7.1. The items required for each operation are listed at the start of the relevant instructions.

3 A particular model of test equipment is recommended in some cases, but other equipment having the required parameters given in Table 7.1 may be used. Although the procedures to be followed are given in general terms, they are based on the use of the recommended test equipment. Some modification to the procedure may be necessary if other test equipment is used.

DISMANTLING AND REASSEMBLY

Introduction

4 Instructions for dismantling and reassembling the instrument are limited to those areas where special care is needed or difficulty may be experienced.

WARNING: LETHAL VOLTAGE
DANGEROUS AC VOLTAGES ARE EXPOSED WHEN THE INSTRUMENT IS CONNECTED TO THE AC SUPPLY WITH THE COVERS REMOVED. SWITCH THE INSTRUMENT OFF AND DISCONNECT THE SUPPLY SOCKET FROM THE REAR PANEL BEFORE CARRYING OUT ANY DISMANTLING OR REASSEMBLY OPERATION.

TABLE 7.1

Test Equipment Required

Item	Description Recommended Model	Required Parameters
1	Signal Generator Racal-Dana 9087	Low phase noise. Jitter<0.5 ns Frequency range 10 kHz to 1.3 GHz Output level 1 mV to 1 V 10 MHz INT STD OUTPUT.
2	Oscilloscope with 1:1 Probe	Bandwidth 50 MHz
3	Digital Multimeter Racal Dana 4002A	Frequency range: DC to 10 MHz Level: 20 mV to 20 V
4	Frequency Standard Racal-Dana 9475	10 MHz Accuracy better than ±3 parts in 10^{10}.
5	Audio Oscillator Racal-Dana 9083	Frequency range: 10 Hz to 5 kHz Level: 30 mV into 50 Ω
6	Pulse Generator Phillips PM5771	To provide a single positive-going pulse with a low level of +0.4 V and a high level of +2.4 V (TTL output limit levels)
7	Connecting Lead	50 Ω coaxial cable with BNC connectors. Length between 80 cm and 1 m.
8	T-piece	BNC, 50 Ω
9	Coaxial Load	BNC, 50 Ω
10	GPIB Controller HP-85	
11	GPIB Analyzer Racal Dana 488	

Instrument Covers

5 (1) Disconnect the power input socket from the rear panel.

(2) Remove the two screws securing the rear panel bezel: remove the bezel.

(3) If the handles are fitted, peel off the adhesive trim patch from both handles. Remove the two screws securing each handle: remove the handles and spacers.

(4) Remove the top cover by sliding it to the rear of the instrument.

(5) Remove the bottom cover by sliding it to the rear of the instrument.

6 To replace the covers, follow the reverse of the above procedure. Ensure that the top cover is fitted with the access holes towards the front of the instrument, and that the tongues on the ends of the covers are fitted under the edges of the front panel and rear bezel.

Front Panel

7 (1) Remove the instrument covers.

(2) Remove the clamping collars from the channel A and channel B inputs. A suitable slotted screwdriver is included in the Customer Service Support Kit.

(3) Remove the two screws securing the front panel to the side frame at both sides of the instrument.

(4) Ease the front panel forward until the display board disconnects from the motherboard at PL1 and PL2.

(5) Disconnect the coaxial lead from the back of the channel C input.

8 To replace the panel, follow the reverse procedure. Pass the POWER switch button through the aperture in the panel and reconnect the channel C amplifier before securing the panel.

Rear Panel

9 (1) Remove the instrument covers.

(2) If a PCB-mounted frequency standard is fitted, remove the screws securing it to the rear panel. Pull the PCB assembly upwards until the board disconnects from the motherboard at PL14.

(3) Remove the two screws securing the rear panel to the side frame at both sides of the instrument.

(4) Ease the panel away from the instrument to disconnect assembly 19-1206 from the motherboard at PL19 and PL20.

(5) If an ovened frequency standard is fitted, disconnect the flying lead from PL14.

(6) Remove the nut and crinkle washer securing the rectifier bridge, D11, to the panel.

(7) Disconnect the green/yellow lead connecting the rear panel stud to the power input plug.

10 To replace the panel follow the reverse of the above procedure.

WARNING: LETHAL VOLTAGE
THE GROUNDING OF EXTERNAL METALWORK OF THE INSTRUMENT DEPENDS UPON THE CONNECTION BETWEEN THE REAR PANEL STUD AND THE POWER INPUT PLUG. ENSURE THAT THE GREEN/YELLOW LEAD IS CORRECTLY CONNECTED DURING REASSEMBLY.

Channel C Amplifier

11 (1) Remove the top cover.

(2) Remove the two screws securing the board to the right-hand side frame.

(3) Pull the board upwards to disconnect it from the motherboard at SK7. This allows access to both sides of the board for servicing.

12 To remove the board completely:

(1) Remove the front panel.

(2) Disconnect the coaxial lead from the back of channel C input.

13 To replace the amplifier follow the reverse of the above procedure.

Display Board

14 (1) Remove the instrument covers.

(2) Remove the front panel.

(3) Remove the three screws securing the display board to the front panel and remove the board.

15 To replace the display board, follow the reverse of the above procedure.

SPECIAL FUNCTIONS FOR DIAGNOSTIC PURPOSES

16 The special functions listed in Table 7.2 are provided for use during maintenance. The functions are used in conjunction with the CHECK mode. They are entered in the special function register by pressing:

[N] [N] [SHIFT] [STORE] [SF]

and are enabled and disabled by pressing

[SHIFT] [SF]

TABLE 7.2

Additional Special Functions

Function Number	Function With CHECK Mode Selected
70	10 MHz check
71	LED check
72	Measurement of short start TEC count
73	Measurement of long start TEC count
74	Measurement of short stop TEC count
75	Measurement of long stop TEC count
76	D-to-A converter check
77	Channel A relay check
78	Channel B relay check

Special Function 70

17 Special function 70 is the default state of its decade. It provides measurement of the 10 MHz internal frequency standard, and verifies operation of the microprocessor system, MCC1, MCC2 and the TEC.

Special Function 71

18 Special function 71 exercises all the LEDs, except STANDBY, GATE, TRIG A, TRIG B, REM, ADDR and SRQ, at approximately 0.5 Hz. If the GPIB interface is fitted, the REM, ADDR and SRQ indicators light.

Special Functions 72, 73, 74 and 75

19 Special functions 72, 73, 74 and 75 should only be used for diagnostic purposes at an ambient temperature of $23^{\circ}C \pm 2^{\circ}C$.

20 The long counts must be 800 ± 220. The short counts must be in the range (0.5 x long count) $^{+20}_{-40}$. Counts outside these ranges indicate that the TEC has failed.

Special Function 76

21 With special function 76 active, the microprocessor continuously exercises the D-to-A converters in both channel A and channel B through the range -5.1 V to +5.1 V. The waveform (511 levels spaced by 0.2 V) can be monitored at the trigger output pins on the rear panel.

Special Function 77

22 With the 10 MHz STD OUTPUT socket on the rear panel connected to the channel A input, activating special function 77 causes the microprocessor to exercise the channel A relays for X10/X1, 50 Ω/1 MΩ, DC/AC, FILTER and COM A.

Special Function 78

23 With the 10 MHz STD OUTPUT socket on the rear panel connected to the channel B input, activating special function 78 causes the microprocessor to exercise the channel B relays for X10/X1, 50 Ω/1 MΩ and DC/AC.

FAULT FINDING

24 A guide to fault location is given in the flow charts of Fig 7.1 to Fig 7.8. The charts provide a logical procedure for localising the fault to an area of circuit. When using the charts it is essential to begin at the start point in Fig 7.1 or Fig 7.6 and act according to the results of each decision box met in turn. Starting part way through any chart is unlikely to lead to satisfactory fault location.

25 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	2
Digital Multimeter	3
Coaxial Lead	7
GPIB Controller	10
GPIB Analyzer	11

SETTING UP AFTER REPAIR

Introduction

26 After repair, the relevant setting-up procedures from those given in the following paragraphs should be implemented before carrying out the overall specification check. The procedures should also be used if the instrument fails a routine specification check.

27 The ambient temperature must be maintained at 23 °C ± 2 °C throughout the procedures. The instrument should be powered from an AC supply, not a battery pack.

WARNING: LETHAL VOLTAGE
THESE PROCEDURES REQUIRE THE INSTRUMENT TO BE OPERATED WITH THE COVERS REMOVED. LETHAL VOLTAGE LEVELS ARE EXPOSED UNDER THESE CONDITIONS.

Channel A Input System

28 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1

29 Set R149 fully counter-clockwise and R192 to its mid-position. R192 is located inside the screened module, as shown in Fig 7.9.

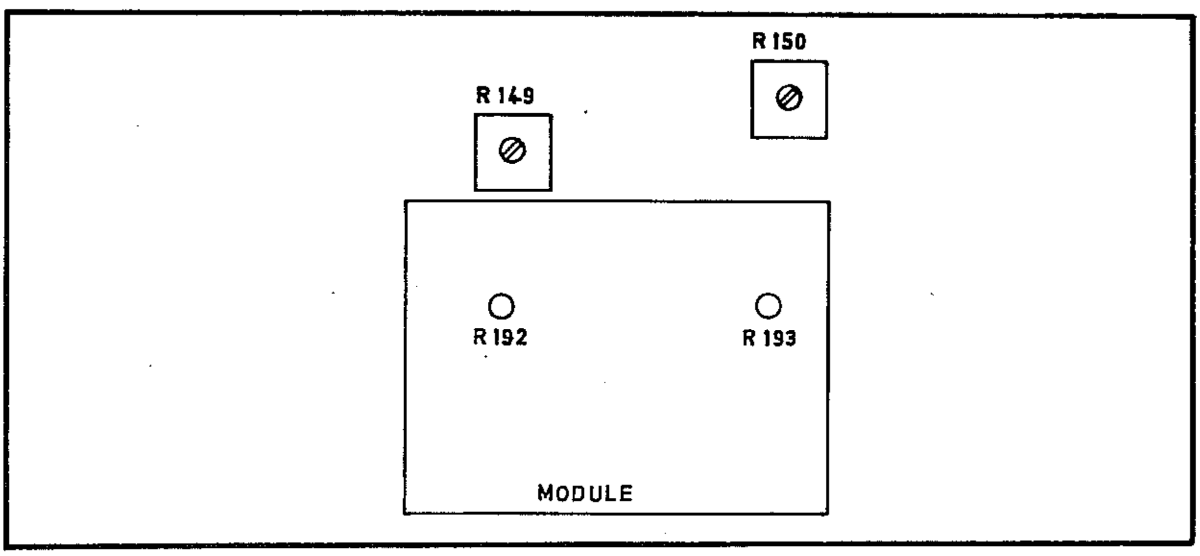


Fig 7.9 Location of R149 and R192

30 (1) Switch the 1991/92 on. Select FREQ A.

(2) Select 50 Ω impedance for channel A.

(3) Press the RESOLUTION ↓ key five times, until 000 is displayed.

(4) Connect the test equipment as shown in Fig 7.10.

(5) Set the signal generator output to 100 MHz at a level of 3.0 mV r.m.s.

(6) Verify that the EXT STD indicator is lit, and that the channel A TRIG indicator is flashing.

(7) Adjust R192 to obtain the most stable display indication of 100.0 6 ± 0.1 6, with the GATE indicator flashing.

NOTE: Care is needed when adjusting R192. The display indication is random with R192 set to either side of the correct position.

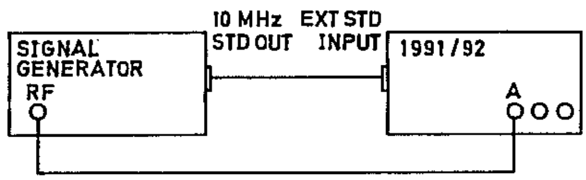


Fig 7.10 Connections for Channel A Input System Adjustment

31 (1) Switch off the RF output of the signal generator.

(2) Press the RESOLUTION ↑ key five times, until 00000000 is displayed.

(3) Switch on the RF output of the signal generator.

(4) Increase the signal generator output to 13 mV r.m.s.

(5) Adjust R149 slowly clockwise until the display just becomes unstable. Turn back until the display is just stable, and indicates 100.000000 6 ± 0.000001 6.

(6) Reduce the signal generator output to 7 mV r.m.s. Verify that the GATE indicator stops flashing. If it does not, repeat steps (4) to (6).

(7) Switch off the 1991/92. Disconnect the test equipment.

Channel B Input System

32 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1

33 Set R150 fully counter-clockwise and R193 to its mid-position. R193 is located inside the screened module, as shown in Fig 7.11.

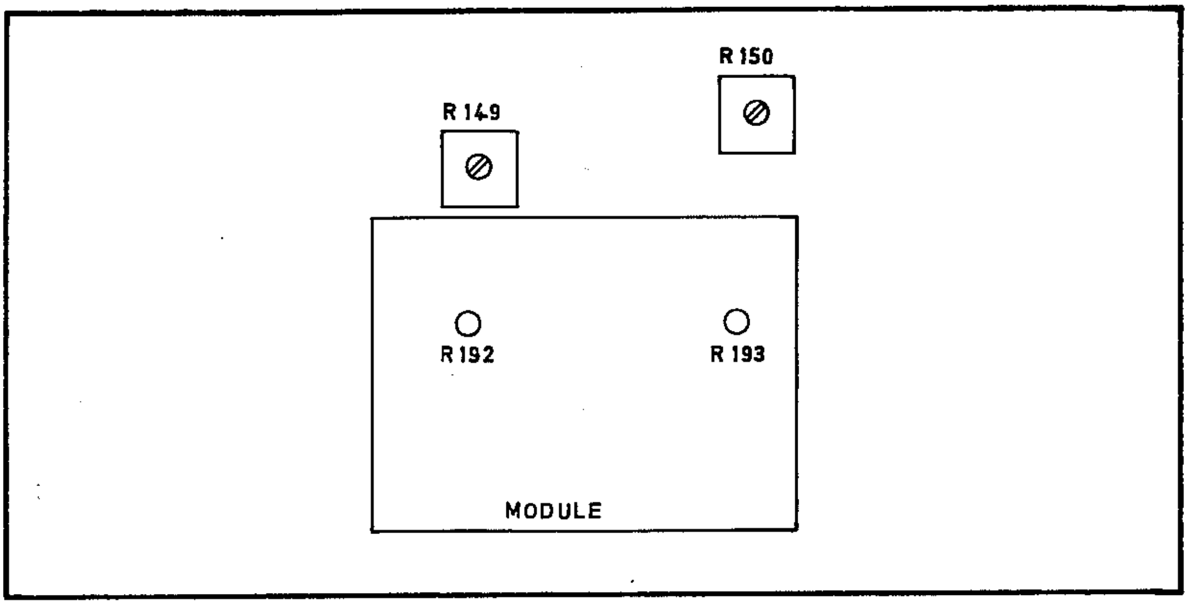


Fig 7.11 Location of R150 and R193

34 (1) Switch the 1991/92 on. Select FREQ A.

(2) Select 50 Ω impedance for channel B, and press

[2] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF]

(3) Press the RESOLUTION ↓ key five times, until 000 is displayed.

(4) Connect the test equipment as shown in Fig 7.12.

(5) Set the signal generator output to 100 MHz at a level of 3.0 mV r.m.s.

(6) Verify that the EXT STD indicator is lit, and that the channel B TRIG indicator is flashing.

(7) Adjust R193 to obtain the most stable display indication of 100.0 6 ± 0.1 6, with the GATE indicator flashing.

NOTE: Care is needed when adjusting R193. The display indication is random with R193 set to either side of the correct position.

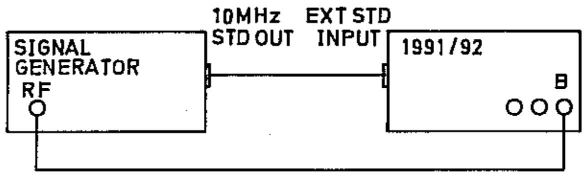


Fig 7.12 Connections for Channel B Input System Adjustment

35 (1) Switch off the RF output of the signal generator.

(2) Press the RESOLUTION ↑ key five times, until 00000000 is displayed.

(3) Switch on the RF output of the signal generator.

(4) Increase the signal generator output to 13 mV r.m.s.

(5) Adjust R150 slowly clockwise until the display just becomes unstable. Turn back until the display is just stable, and indicates 100.000000 6 ± 0.000001 6.

(6) Reduce the signal generator output to 7 mV r.m.s. Verify that the GATE indicator stops flashing. If it does not, repeat steps (4) to (6).

(7) Switch off the 1991/92. Disconnect the test equipment.

Channel C Assembly 19-1142 (Model 1992 only)

36 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Connecting Lead	7

37 Connect the test equipment as shown in Fig 7.13.

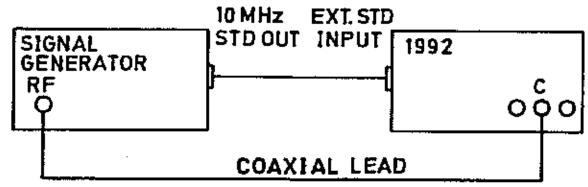


Fig 7.13 Connections for Channel C Input System Adjustment

38 (1) Set R27 on assembly 19-1142 fully clockwise.

(2) Switch the 1992 on. Select FREQ C. Verify that the EXT STD indicator is lit.

(3) Set the signal generator output to 1 GHz at a level of 5.0 mV r.m.s.

(4) Adjust R27 until the gate indicator just starts flashing and the 1992 display indicates 1000.00000 6 ± 0.00001 6.

(5) Switch the output of the signal generator off. Reduce the output level to 4.5 mV r.m.s.

(6) Switch the output of the signal generator on. Verify that the 1992 is not counting. If it is, repeat steps (3) to (6).

(7) Switch off the 1992. Disconnect the test equipment.

INTERNAL FREQUENCY STANDARD, ROUTINE CALIBRATION

39 Test equipment required:

Item	Table 7.1 Item No
Frequency Standard	4

NOTE: If an Option 04A (9444) or Option 04B (9423) frequency standard is fitted, allow the instrument to warm up for one hour (switched to standby, if required) before making any adjustment.

40 (1) Switch on the 1991/92. Select FREQ A and verify that 00000000 is displayed. If the Option 04B (9423) frequency standard is fitted, press the RESOLUTION ↑ key until 000000000 is displayed.

(2) Connect the test equipment as shown in Fig 7.14.

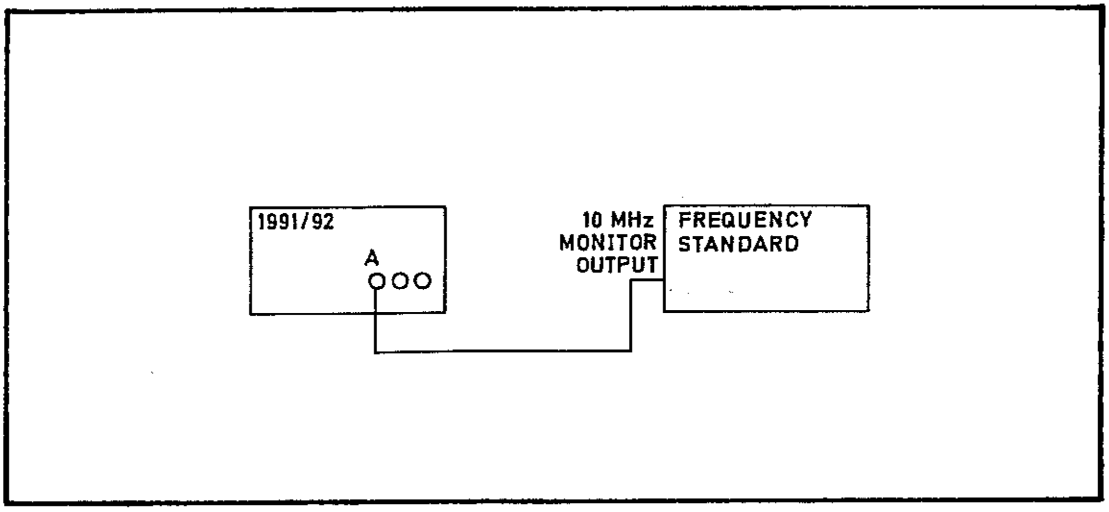


Fig 7.14 Connections for Internal Frequency Standard Adjustment

(3) Press [1] [0] [SHIFT] [EXP] [6] [SHIFT] [STORE] [X]

(4) Press [SHIFT] [RECALL] [X]

Verify that 10.000000 6 is displayed

(5) Press [CONTINUE] and [SHIFT] [R-X/Z]

(6) Adjust the internal frequency standard, via the aperture in the rear panel, to be as near to 10 MHz as possible. The display limits are shown in Table 7.3.

(7) Switch off the 1991/92. Switch off and disconnect the test equipment.

TABLE 7.3

Internal Frequency Standard Accuracy

Frequency Standard	Display	Accuracy
Standard Oscillator	±5 0	5 parts in 10^7
Option 04T	±1 0	1 part in 10^7
Option 04A (9444)	±100 -3	1 part in 10^8
Option 04B (9423)	±10 -3	1 part in 10^9

OVERALL SPECIFICATION CHECK

Introduction

41 Satisfactory completion of the following performance verification procedures (PVPs) will confirm that the instrument is functional and meets its specification. Before commencing the specification check ensure that the instrument passes the test given in Section 3 Paragraphs 9 to 12. The PVPs should be carried out in the order given.

42 The following conditions must be maintained throughout the specification check:

(1) The instrument must be operated from an AC supply.

(2) The line voltage must be within the range indicated by the line voltage selector.

(3) The instrument covers must be fitted.

(4) The ambient temperature must be 23 $^{0}C \pm 2\ ^{0}C$.

(5) The power supply to the frequency standard must be uninterrupted.

43 The instrument should be allowed to warm up for one hour (switched to standby, if required) before commencing the specification check.

Channel A Sensitivity PVP

44 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Digital Multimeter	3
Audio Oscillator	5
T-piece	8

45 (1) Switch on the 1991/92. Select 50 Ω on channel A.

(2) Connect the test equipment as shown in Fig 7.15. Check that the EXT STD indicator lights.

(3) Set the signal generator output to the frequencies shown in Table 7.4 in turn. Set the 1991/92 resolution to the corresponding value.

(4) At each frequency, determine the minimum input level to the 1991/92 which gives stable counting. Verify that this is not more than the level shown in the table.

(5) Disconnect the test equipment.

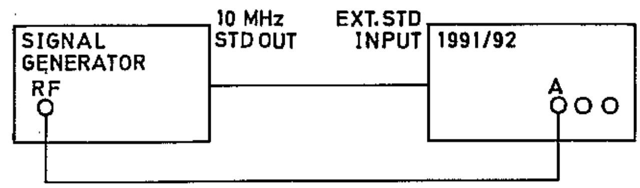


Fig 7.15 Connections for Channel A Sensitivity PVP

TABLE 7.4

Channel A Sensitivity

Frequency	1991/92 Resolution	Signal Level
160 MHz	8 digits	40 mV
100 MHz	8 digits	20 mV
10 MHz	7 digits	20 mV
100 kHz	5 digits	20 mV

46 (1) Connect the test equipment as shown in Fig 7.16.

(2) Set the signal generator output to the frequencies shown in Table 7.5 in turn. Set the 1991/92 resolution to the corresponding value. Enable the 50 kHz filter.

(3) At each frequency, determine the minimum input level to the 1991/92 which gives stable counting. Verify that this is not more than the level shown in the table.

(4) Disable the 50 kHz filter. Disconnect the test equipment.

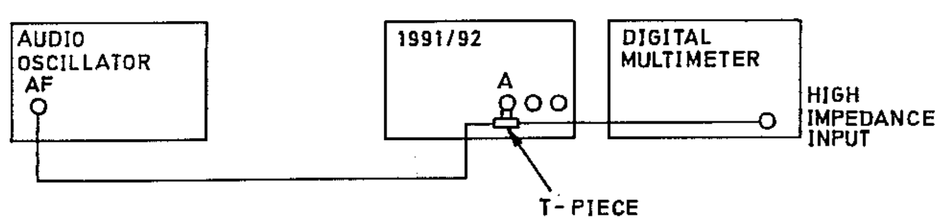


Fig 7.16 Connections for Channel A Sensitivity PVP

TABLE 7.5

Channel A Sensitivity

Frequency	1991/92 Resolution	Signal Level
5 kHz	3	20 mV
10 Hz	3	20 mV

Channel B Sensitivity PVP

47 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Digital Multimeter	3
Audio Oscillator	5
T-piece	8

48 (1) Select 50 Ω on channel B.

(2) Connect the test equipment as shown in Fig 7.17. Check that the EXT STD indicator lights.

(3) Press [2] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF]

(4) Set the signal generator output to the frequencies shown in Table 7.6 in turn. Set the 1991/92 resolution to the corresponding value.

(5) At each frequency, determine the minimum input level to the 1991/92 which gives stable counting. Verify that this is not more than the level shown in the table.

(6) Disconnect the test equipment.

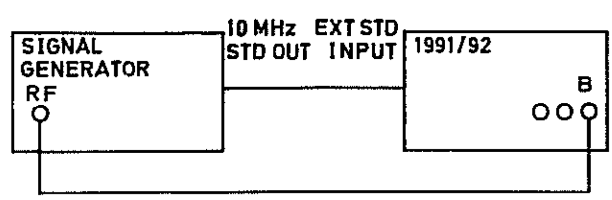


Fig 7.17 Connections for Channel B Sensitivity PVP

TABLE 7.6

Channel B Sensitivity

Frequency	1991/92 Resolution	Signal Level
100 MHz 10 MHz 100 kHz	8 digits 7 digits 5 digits	20 mV 20 mV 20 mV

49 (1) Connect the test equipment as shown in Fig 7.18.

(2) Set the signal generator output to the frequencies shown in Table 7.7 in turn. Set the 1991/92 resolution to the corresponding value. Enable the 50 kHz filter.

(3) At each frequency, determine the minimum input level to the 1991/92 which gives stable counting. Verify that this is not more than the level shown in the table.

(4) Press [2] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

(5) Disable the 50 kHz filter. Disconnect the test equipment.

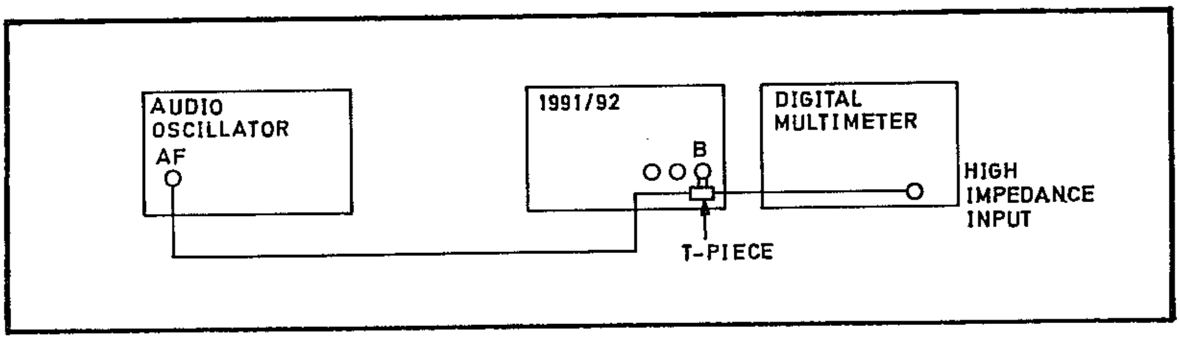


Fig 7.18 Connections for Channel B Sensitivity PVP

TABLE 7.7

Channel B Sensitivity

Frequency	1991/92 Resolution	Signal Level
5 kHz 10 Hz	3 3	20 mV 20 mV

Channel C Sensitivity PVP (1992 Only)

50 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Connecting Lead	7

51 (1) Connect the test equipment as shown in Fig 7.19.

(2) Select FREQ C.

(3) Set the signal generator output to the frequencies shown in Table 7.8 in turn. Set the 1991/92 resolution to the corresponding value.

(4) At each frequency, determine the minimum input level to the 1991/92 which gives stable counting. Verify that this is not more than the level shown in the table.

(5) Disconnect the test equipment.

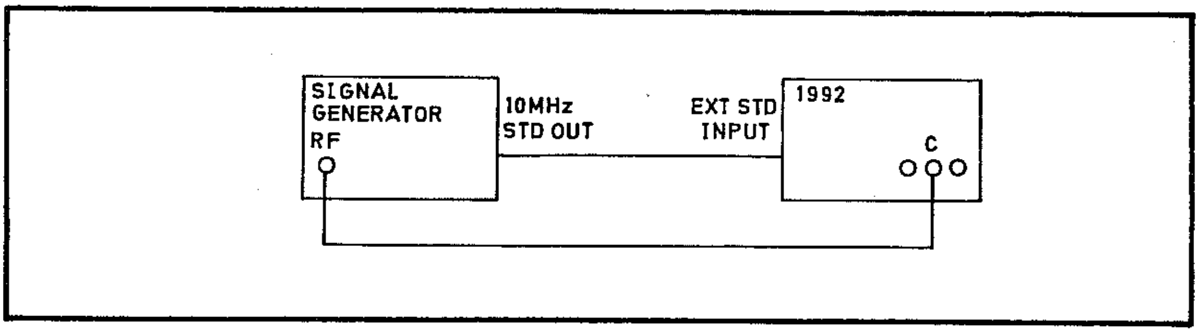


Fig 7.19 Connections for Channel C Sensitivity PVP

TABLE 7.8

Channel C Sensitivity

Frequency	1991/92 Resolution	Signal Level
40 MHz	8 digits	8.5 mV
100 MHz	8 digits	8.5 mV
500 MHz	8 digits	8.5 mV
1000 MHz	9 digits	8.5 mV
1300 MHz	9 digits	70 mV

External Standard Input Sensitivity PVP

52 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1

53 (1) Connect the signal generator output to the EXT STD INPUT socket on the rear panel of the 1991/92.

(2) Set the signal generator output to 10 MHz at a level of 10 mV.

(3) Slowly increase the signal level until the 1991/92 EXT STD indicator lights steadily.

(4) Verify that the signal level is not more than 75 mV r.m.s.

(5) Disconnect the test equipment.

10 MHz Standard Output Level PVP

54 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	2
T-piece	8
Load	9

55 (1) Connect the test equipment as shown in Fig 7.20.

(2) Verify that the peak-to-peak amplitude of the displayed waveform is 1.0 V ±0.4 V. Verify that the mark/space ratio is between 30:70 and 70:30.

(3) Disconnect the test equipment.

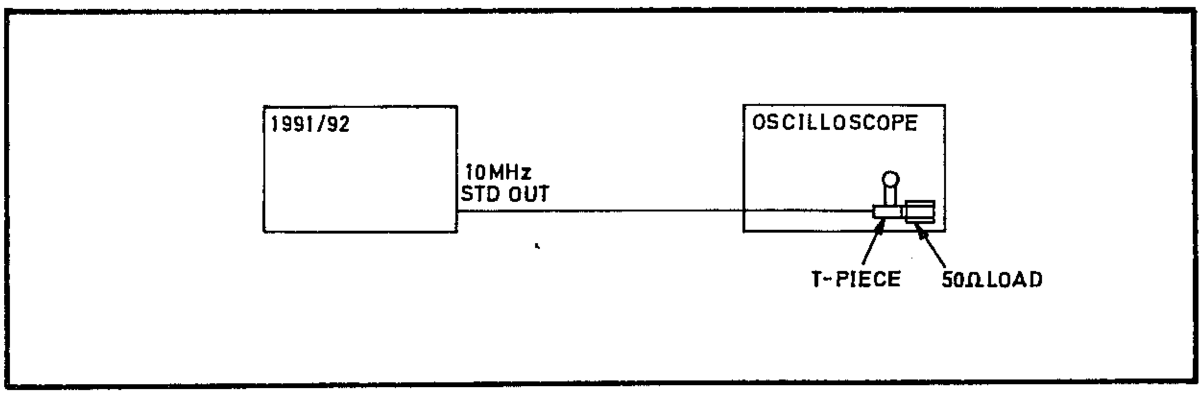


Fig 7.20 Connections for 10 MHz Standard Output Level PVP

Minimum Time Interval PVP

56 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1

57 (1) Connect the test equipment as shown in Fig 7.21.

(2) Select 50 Ω on channel A, T.I. A B and COM A.

(3) Set the signal generator output to 100 MHz at a level of 1 V.

(4) Verify that a display of 0 ± 2ns is obtained.

(5) Disconnect the test equipment.

Fig 7.21 Connections for Minimum Time Interval PVP

External Arming PVP

58 Test equipment required

Item	Table 7.1 Item No
Signal Generator	1
Pulse Generator	6

59 (1) Select 50 Ω on channel A and FREQ A. Press the RESOLUTION key three times until 00000 is displayed.

(2) Connect the test equipment as shown in Fig 7.22.

(3) Set the signal generator output to 10 MHz at a level of 200 mV r.m.s.

(4) Prepare the pulse generator to give a single, 300 μs, positive-going pulse with a low level of +0.4 V and a high level of +2.4 V (TTL limit levels).

(5) Press [1] [6] [SHIFT] [STORE] [SF] [SHIFT] [SF]

(6) Verify that the instrument is not counting.

(7) Trigger the pulse generator to obtain a single pulse output.

(8) Verify that the display indicates 10.0000 6 Hz ± 1 count and that the instrument is not continuously gating.

(9) Press [1] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

(10) Disconnect the test equipment.

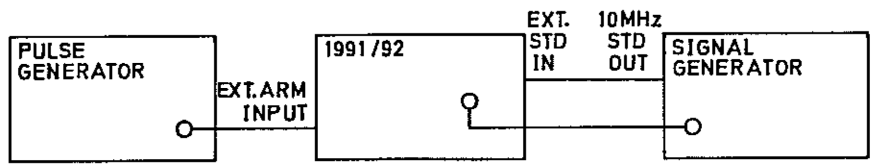


Fig 7.22 Connections for External Arming PVP

Trigger Level PVP

60 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope with Probe	2
Digital Multimeter	3

61 (1) Connect the test equipment as shown in Fig 7.23.

(2) Select DC coupling of the oscilloscope input.

(3) Set the oscilloscope to monitor a waveform of approximately 12 V peak-to-peak with a frequency of approximately 2 Hz.

(4) Select CHECK.

(5) Press [7] [6] [SHIFT] [STORE] [SF] [SHIFT] [SF]

(6) Verify that the channel A and B TRIG indicators are flashing, and that the displayed waveform is as shown in Fig 7.24.

(7) Transfer the oscilloscope probe to the channel B TRIG LEVEL OUTPUT pin and verify that the same waveform is displayed.

(8) Press [7] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

(9) Disconnect the test equipment.

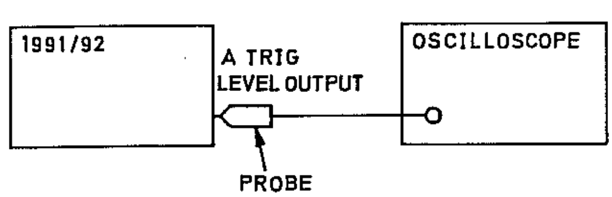


Fig 7.23 Connections for Trigger Level PVP

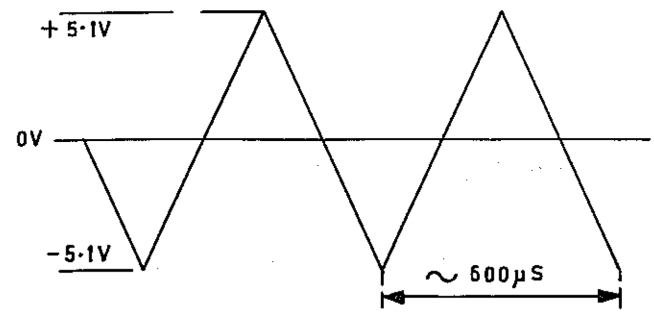


Fig 7.24 Trigger level Waveform

62 (1) Connect the test equipment as shown in Fig 7.25.

(2) Set the multimeter to measure DC volts.

(3) Press [TRIG LEVEL] [5] [TRIG LEVEL] on channels A and B.

(4) Verify that the multimeter indicates +5 V ± 60 mV.

(5) Transfer the probe to the channel B TRIG LEVEL OUTPUT pin and verify that the multimeter indicates +5 V ± 60 mV.

(6) Press [TRIG LEVEL] [0] [TRIG LEVEL] on channels A and B.

(7) Verify that the multimeter indicates 0 V ± 10 mV.

(8) Transfer the probe to the channel A TRIG LEVEL OUTPUT pin and verify that the multimeter indicates 0 V ± 10 mV.

(9) Press [TRIG LEVEL] [5] [SHIFT] [±] [TRIG LEVEL]

(10) Verify that the multimeter indicates -5 V ± 60 mV.

(11) Transfer the probe to the channel B TRIG LEVEL OUTPUT pin and verify that the multimeter indicates -5 V ± 60 mV.

(12) Disconnect the test equipment.

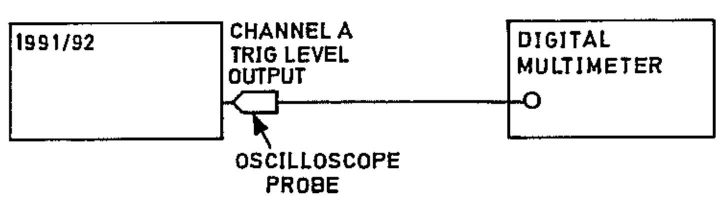


Fig 7.25 Connections for Trigger Level PVP

Internal Frequency Standard PVP

63 Test equipment required:

Item	Table 7.1 Item No
Frequency Standard	4

64 (1) Switch on the 1991/92. Select FREQ A and verify that 00000000 is displayed. If the Option 04B (9423) frequency standard is fitted, press the RESOLUTION ↑ key until 000000000 is displayed.

(2) Connect the test equipment as shown in Fig 7.26.

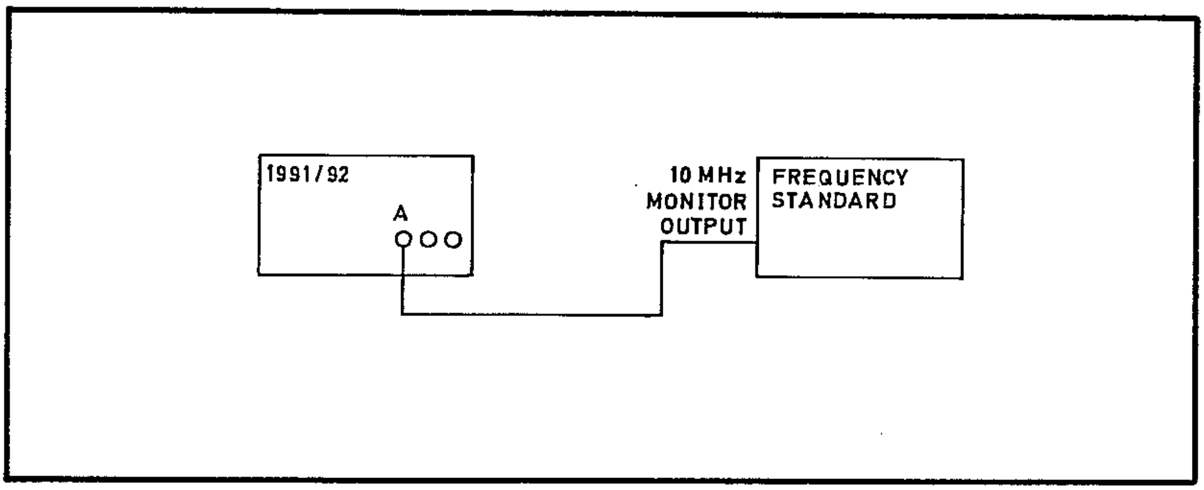


Fig 7.26 Connections for Internal Frequency Standard Adjustment

(3) Press [1] [0] [SHIFT] [EXP] [6] [SHIFT] [STORE] [X]

(4) Press [SHIFT] [RECALL] [X]

Verify that 10.000000 6 is displayed.

(5) Press [CONTINUE] and [SHIFT] [R-X/Z]

(6) Verify that the value displayed is within the limits shown in Table 7.9.

TABLE 7.9

Internal Frequency Standard Accuracy

Frequency Standard	Display	Accuracy
Standard Oscillator	±5 0	5 parts in 10^7
Option 04T	±1 0	1 part in 10^7
Option 04A (9444)	±100 -3	1 part in 10^8
Option 04B (9423)	±10 -3	1 part in 10^9

65 Switch off the 1991/92. Switch off and disconnect the test equipment.

SECTION 8 — PARTS LIST AND CIRCUIT DIAGRAMS

PARTS LIST

FRONT AND REAR PANEL ASSEMBLIES

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
REAR PANEL ASSEMBLY					
		Feedthrough terminals for trigger levels			24-3547
FRONT PANEL ASSEMBLY					
INPUT C		BNC to SMA socket, fused			17-1038
(1992 only)		Fuselink for 17-1038 (pack of 5)			11-1718

PARTS LIST

BNC MOUNTING BOARD 19-1206

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Sockets					
EXT STD INPUT		BNC socket, PCB mounting			23-3421
EXT ARM INPUT		BNC socket, PCB mounting			23-3421
10MHz STD OUTPUT		BNC socket, PCB mounting			23-3421
SK19		Connector 2 x 2 way			23-5159
SK20		Connector 2 x 2 way			23-5159

PARTS LIST

DISPLAY ASSEMBLY 19-1141

Fig 3

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistor					
	Ω		W		
R1	10k	Carbon Film	¼	5	20-2103
R2	10k	Carbon Film	¼	5	20-2103
R3	9X10k	SIL Array			20-5521
R4	10k	Carbon Film	¼	5	20-2103
R5	10k	Carbon Film	¼	5	20-2103
Capacitors					
	F		V		
C1	100n	Ceramic	50	20	21-1708
C2	4.7µ	Electrolytic	50	20	21-0785
C3	100n	Ceramic	50	20	21-1708
C4	100n	Ceramic	50	20	21-1708
C5	100n	Ceramic	50	20	21-1708
Diodes					
D1		Not Used			
D2		Not Used			
D3		Not Used			
D4		Not Used			
D5		Not Used			
D6		Silicon (1N4149)			22-1029
D7		Silicon (1N4149)			22-1029
D8		Not Used			
D9		Silicon (1N4149			22-1029
D10		Silicon (1N4149)			22-1029
LP1		LED, red			26-5026
LP2		LED, red			26-5026
LP3		LED, red			26-5026
LP4		LED, red			26-5026
LP5		LED, red			26-5026
LP6		LED, red			26-5026
LP7		LED, red			26-5026
LP8		LED, red			26-5026
LP9		Not Used			
LP10		Not Used			

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
LP11		LED, red			26-5026
LP12		LED, red			26-5026
LP13		LED, red			26-5026
LP14		Not Used			
LP15		LED, red			26-5026
LP16		LED, red			26-5026
LP17		LED, red			26-5026
LP18		LED, red			26-5026
LP19		Not Used			
LP20		LED, red			26-5026
LP21		LED, red			26-5026
LP22		LED, red			26-5026
LP23		LED, red			26-5026
LP24		LED, red			26-5026
LP25		LED, red			26-5026
LP26		LED, red			26-5026
LP27		LED, red			26-5026
LP28		LED, red			26-5026
LP29		LED, red			26-5026
LP30		LED, red			26-5026
LP31		LED, red			26-5026
LP32		LED, red			26-5026
LP33		LED, orange			26-5027
LP34		LED, red			26-5026
LP35		LED, red			26-5026
LP36		LED, red			26-5026
LP37		LED, red			26-5026
LP38		LED, red			26-5026
LP39		LED, red			26-5026
LP40		LED, red			26-5026
LP41		LED, red			26-5026
LP42		LED, red			26-5026
LP43		Not Used			
LP44		LED, red			26-5026
LP45		LED, red			26-5026
LP46		LED, red			26-5026
LP47		LED, red			26-5026

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Integrated Circuits					
IC1		4012			22-4754
IC2		74C922			22-4779
IC3		7218AIJI			22-4778
IC4		7218AIJI			22-4778
Displays					
DI1		Seven-segment display; double digit			26-1512
DI2		Seven-segment display; double digit			26-1512
DI3		Seven-segment display; double digit			26-1512
DI4		Seven-segment display; double digit			26-1512
DI5		Seven-segment display			26-1513
DI6		Seven-segment display			26-1511
Miscellaneous					
S1-S33		Keyswitch, single-pole			23-4125
		Button, blue			15-0705
		Button, grey			15-0703
		Button, grey, 1			16-0651
		Button, grey, 2			16-0652
		Button, grey, 3			16-0653
		Button, grey, 4			16-0654
		Button, grey, 5			16-0655
		Button, grey, 6 or 9			16-0656
		Button, grey, 7			16-0657
		Button, grey, 8			16-0658
		Button, grey, 0			16-0659
		Button, grey, decimal point			16-0660
SK1		Socket, 14-way			23-5160
SK2		Socket, 14-way			23-5160

PARTS LIST

1.3 GHz PRESCALER ASSEMBLY 19-1142 (1992 Only)

Fig 5

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
	Ω		W		
R1		Not Used			
R2		Not Used			
R3	10k	Chip	0.125	5	20-5768
R4	10k	Chip	0.125	5	20-5768
R5	150	Chip	1	5	20-5841
R6	39	Chip	1	5	20-5837
R7	330	Chip	0.125	5	20-5787
R8	150	Chip	0.125	5	20-5783
R9	270	Chip	0.125	5	20-5786
R10	100	Chip	0.125	5	20-5764
R11	270	Chip	0.125	5	20-5786
R12	10	Chip	0.125	5	20-5771
R13	33	Chip	0.125	5	20-5776
R14	330	Chip	0.125	5	20-5787
R15	270	Chip	0.125	5	20-5786
R16	390	Chip	0.125	5	20-5788
R17		Not Used			
R18	10	Chip	0.125	5	20-5771
R19	33	Chip	0.125	5	20-5776
R20	330	Chip	0.125	5	20-5787
R21	180	Chip	0.125	5	20-5784
R22	180	Chip	0.125	5	20-5784
R23	390	Chip	0.125	5	20-5788
R24	10	Chip	0.125	5	20-5771
R25	33	Chip	0.125	5	20-5776
R26	330	Chip	0.125	5	20-5787
R27	20k	Variable			20-7049
R28	390	Chip	0.125	5	20-5788
R29	100k	Chip	0.125	5	20-5813
R30	10	Chip	0.125	5	20-5771
R31	22	Chip	0.125	5	20-5774
R32	220	Chip	0.125	5	20-5785
R33	1.5k	Chip	0.125	5	20-5794
R34	1.5k	Chip	0.125	5	20-5794
R35	56k	Chip	0.125	5	20-5810

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	10	Chip	0.125	5	20-5771
R37	56	Chip	0.125	5	20-5779
R38	56k	Chip	0.125	5	20-5810
R39	1M	Chip	0.125	5	20-5770
R40		Not Used			
R41	4.7k	Chip	0.125	5	20-5799
R42	4.7k	Chip	0.125	5	20-5799
R43		Not Used			
R44	1k	Chip	0.125	5	20-5792
R45	150	Chip	0.125	5	20-5783
R46	27	Chip	0.125	5	20-5775
R47	27	Chip	0.125	5	20-5775
R48	27	Chip	0.125	5	20-5775
R49	27	Chip	0.125	5	20-5775
R50	470	Chip	0.125	5	20-5765
R51		Not Used			
R52	6.8k	Chip	0.125	5	20-5801
R53	3.3k	Chip	0.125	5	20-5797
R54	1k	Chip	0.125	5	20-5792
R55	1k	Chip	0.125	5	20-5792
R56	680	Chip	0.125	5	20-5790
R57	2.7k	Chip	0.125	5	20-5766
R58	3.3k	Chip	0.125	5	20-5797
R59	1k	Chip	0.125	5	20-5792
R60	1k	Chip	0.125	5	20-5792
R61	1k	Chip	0.125	5	20-5792
R62	1k	Chip	0.125	5	20-5792
R63		Not Used			
R64		Not Used			
R65		Not Used			
R66	150	Chip	0.125	5	20-5783
R67		Not Used			
R68	1M	Chip	0.125	5	20-5770
R69	1M	Chip	0.125	5	20-5770
R70	10	Chip	0.125	5	20-5771
R71	10	Chip	0.125	5	20-5771

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	10n	Chip	50	20	21-1801
C2	10n	Chip	50	20	21-1801
C3	10n	Chip	50	20	21-1801
C4	10n	Chip	50	20	21-1801
C5	10n	Chip	50	20	21-1801
C6	10n	Chip	50	20	21-1801
C7	3.3p	Chip	50	0.25p	21-1781
C8	10n	Chip	50	20	21-1801
C9	10n	Chip	50	20	21-1801
C10	10n	Chip	50	20	21-1801
C11	3.3p	Chip	50	0.25p	21-1781
C12	10n	Chip	50	20	21-1801
C13	10n	Chip	50	20	21-1801
C14	3.3p	Chip	50	0.25p	21-1781
C15	10n	Chip	50	20	21-1801
C16	47µ	Electrolytic	25	-10+50	21-0795
C17	10n	Chip	50	20	21-1801
C18	10n	Chip	50	20	21-1801
C19	4.7p	Chip	50	0.25p	21-1783
C20		Not Used			
C21	10n	Chip	50	20	21-1801
C22	3.3p	Chip	50	0.25p	21-1781
C23	12p	Chip	50	5	21-1799
C24	10n	Chip	50	20	21-1801
C25	10n	Chip	50	20	21-1801
C26	1n	Chip	50	20	21-1800
C27	47µ	Electrolytic	25	-10+50	21-0795
C28	10n	Chip	50	20	21-1801
C29	10n	Chip	50	20	21-1801
C30	10n	Chip	50	20	21-1801
C31	10n	Chip	50	20	21-1801
C32	10n	Chip	50	20	21-1801
C33	5.6p	Chip	50	0.25p	21-1784
C34	6.8p	Chip	50	0.25p	21-1785
C35	6.8p	Chip	50	0.25p	21-1785

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C36	6.8p	Chip	50	0.25p	21-1785
C37	47p	Chip	50	5	21-1795
C38	10n	Chip	50	20	21-1801
C39	10n	Chip	50	20	21-1801
C40	3.3p	Chip	50	0.25p	21-1781
C41	3.3p	Chip	50	0.25p	21-1781
C42	5.6p	Chip	50	0.25p	21-1784
C43	10n	Chip	50	20	21-1801
C44	47µ	Electrolytic	25	-10+50	21-0795
C45	47µ	Electrolytic	6.3	20	21-0704
C46	3.9p	Chip	50	0.25	21-1782
C47	10n	Chip	50	20	21-1801
C48	10n	Chip	50	20	21-1801
C49	3.3p	Chip	50	0.25p	21-1781
C50	3.3p	Chip	50	0.25p	21-1781
C51	15p	Chip	50	5	21-1789
C52	15p	Chip	50	5	21-1789
C53	100n	Ceramic	50	20	21-1708

Diodes

Cct. Ref.	Description	Racal Part Number
D1	Schottky (5082.2835)	22-1086
D2	PIN (5082.3379)	22-1058
D3	Schottky (5082.2835)	22-1086
D4	Not Used	
D5	Schottky (5082.2835)	22-1086
D6	Schottky (5082.2835)	22-1086
D7	PIN (5082.3379)	22-1058
D8	Hot Carrier (5082.2800)	22-1068
D9	Hot Carrier (5082.2800)	22-1068
D10	Voltage Regulator (BZX79C9V1)	22-1814
D11	Voltage Regulator (BZX79C9V1)	22-1814
D12	Silicon (IN4149)	22-1029

Transistors

Cct. Ref.	Description	Racal Part Number
Q1	BFR90	22-6123
Q2	BFR90	22-6123
Q3	BFR90	22-6123
Q4	HXTR3101	22-6155

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Integrated Circuits					
IC1		LM339			22-4249
IC2		MC10116			22-4528
IC3		SP4730			22-4694
IC4		74LS00			22-4531
Inductors					
L1		Coil Assembly			17-3240
Connectors					
SK7		Connector, 30-way			23-5173
		Coaxial Cable Assembly			10-2891

PARTS LIST

MOTHERBOARD ASSEMBLY 19-1145

Figs 7, 8 and 9

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
	Ω		W		
R1	1k	Chip	0.125	5	20-5792
R2	9x1k	SIL Array			20-5541
R3	330	Chip	0.125	5	20-5787
R4	330	Chip	0.125	5	20-5787
R5	1k	Chip	0.125	5	20-5792
R6	330	Chip	0.125	5	20-5787
R7	1k	Chip	0.125	5	20-5792
R8	10	Chip	0.125	5	20-5771
R9		Not Used			
R10		Not Used			
R11	470	Chip	0.125	5	20-5765
R12		Not Used			
R13		Not Used			
R14		Not Used			
R15		Not Used			
R16	470	Chip	0.125	5	20-5765
R17		Not Used			
R18	1k	Chip	0.125	5	20-5792
R19		Not Used			
R20		Not Used			
R21		Not Used			
R22		Not Used			
R23		Not Used			
R24		Not Used			
R25	10k	Chip	0.125	5	20-5768
R26		Not Used			
R27		Not Used			
R28	1k	Chip	0.125	5	20-5792
R29		Not Used			
R30		Not Used			
R31		Not Used			
R32	1k	Chip	0.125	5	20-5792
R33	1k	Chip	0.125	5	20-5792
R34		Not Used			
R35	4.7k	Chip	0.125	5	20-5799

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36		Not Used			
R37		Not Used			
R38		Not Used			
R39		Not Used			
R40	4.7k	Chip	0.125	5	20-5799
R41		Not Used			
R42		Not Used			
R43		Not Used			
R44		Not Used			
R45	390	Carbon Film	¼	5	20-2391
R46	5x10k	SIL Array			20-5562
R47	1k	Chip	0.125	5	20-5792
R48	120	Carbon Film	¼	5	20-2121
R49		SIL Array (Custom Built)			20-5556
R50		Not Used			
R51		Not Used			
R52		Not Used			
R53		Not Used			
R54	1k	Chip	0.125	5	20-5792
R55		Not Used			
R56		Not Used			
R57		Not Used			
R58		Not Used			
R59		Not Used			
R60	1k	Chip	0.125	5	20-5792
R61		Not Used			
R62		Not Used			
R63	390	Carbon Film	¼	5	20-2391
R64		Not Used			
R65	1k	Chip	0.125	5	20-5792
R66		Not Used			
R67	330	Chip	0.125	5	20-5787
R68	100k	Chip	0.125	5	20-5813
R69	390	Carbon Film	¼	5	20-2391
R70		Not Used			
R71		Not Used			
R72		Not Used			
R73		Not Used			
R74		Not Used			
R75	10k	Chip	0.125	5	20-5768

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R76	100k	Chip	0.125	5	20-5813
R77	330	Chip	0.125	5	20-5787
R78	100	Metal Oxide	1	5	20-4673
R79	100	Metal Oxide	1	5	20-4673
R80	100	Metal Oxide	1	5	20-4673
R81	100	Metal Oxide	1	5	20-4673
R82	900k	Carbon Film	½	0.25	20-7523
R83	111k	Metal Film	0.125	0.25	20-7522
R84	900k	Carbon Film	½	0.25	20-7523
R85	111k	Metal Film	0.125	0.25	20-7522
R86		Not Used			
R87		SIL Array (Custom Built)			20-5554
R88		SIL Array (Custom Built)			20-5554
R89		SIL Array (Custom Built)			20-5554
R90		Not Used			
R91		SIL Array (Custom Built)			20-5554
R92		Not Used			
R93		Not Used			
R94	180	Chip	0.125	5	20-5784
R95		Not Used			
R96	180	Chip	0.125	5	20-5784
R97		Not Used			
R98	470	Chip	0.125	5	20-5765
R99		Not Used			
R100	1.2k	Chip	0.125	5	20-5793
R101	330	Chip	0.125	5	20-5787
R102	470	Chip	0.125	5	20-5765
R103		Not Used			
R104	1.2k	Chip	0.125	5	20-5794
R105		Not Used			
R106		Not Used			
R107	1k	Chip	0.125	5	20-5792
R108		Not Used			
R109		Not Used			
R110	1k	Chip	0.125	5	20-5792
R111	10	Chip	0.125	5	20-5771
R112	10	Chip	0.125	5	20-5771
R113	10k	Chip	0.125	5	20-5764
R114		Not Used			
R115	1k	Chip	0.125	5	20-5792

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R116	470	Chip	0.125	5	20-5765
R117	10k	Chip	0.125	5	20-5764
R118		Not Used			
R119	1k	Chip	0.125	5	20-5792
R120	470	Chip	0.125	5	20-5765
R121	2.2k	Chip	0.125	5	20-5796
R122	2.2k	Chip	0.125	5	20-5796
R123	2.2k	Chip	0.125	5	20-5796
R124	2.2k	Chip	0.125	5	20-5796
R125	680	Chip	0.125	5	20-5790
R126	680	Chip	0.125	5	20-5790
R127		Not Used			
R128	220	Chip	0.125	5	20-5785
R129	1.5k	Chip	0.125	5	20-5794
R130		Not Used			
R131		Not Used			
R132		Not Used			
R133		Not Used			
R134		Not Used			
R135	100k	Chip	0.125	5	20-5813
R136	10k	Chip	0.125	5	20-5768
R137	10k	Chip	0.125	5	20-5768
R138		Not Used			
R139	10	Carbon Film	¼	5	20-2100
R140	100	Chip	0.125	5	20-5764
R141	10k	Chip	0.125	5	20-5768
R142	68	Chip	0.125	5	20-5780
R143	10	Carbon Film	¼	5	20-2100
R144		Not Used			
R145	10k	Chip	0.125	5	20-5768
R146	10	Chip	0.125	5	20-5771
R147	1k	Chip	0.125	5	20-5792
R148	3.3k	Chip	0.125	5	20-5797
R149	10k	Variable			20-7071
R150	10k	Variable			20-7071
R151	10k	Chip	0.125	5	20-5768
R152	10k	Chip	0.125	5	20-5768
R153		Not Used			
R154		Not Used			
R155	4.7k	Chip	0.125	5	20-5799

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R156	4.7k	Chip	0.125	5	20-5797
R157	100k	Chip	0.125	5	20-5813
R158	4.7k	Chip	0.125	5	20-5799
R159	18	Chip	0.125	5	20-5763
R160	100	Chip	0.125	5	20-5764
R161	68	Chip	0.125	5	20-5780
R162		Not Used			
R163	100	Chip	0.125	5	20-5764
R164	68	Chip	0.125	5	20-5780
R165	100	Chip	0.125	5	20-5764
R166	100	Chip	0.125	5	20-5764
R165	3.3k	Chip	0.125	5	20-5797
R168	3.3k	Chip	0.125	5	20-5797
R169	47	Chip	0.125	5	20-5778
R170	120	Carbon Film	$\frac{1}{4}$	5	20-2121
R171	120	Carbon Film	$\frac{1}{4}$	5	20-2121
R177		Not Used			
R173		Not Used			
R174	1k	Chip	0.125	5	20-5792
R175	1k	Chip	0.125	5	20-5792
R176		Not Used			
R177	1k	Chip	0.125	5	20-5792
R178	3.3k	Chip	0.125	5	20-5797
R179	1k	Chip	0.125	5	20-5792
R180	10k	Chip	0.125	5	20-5768
R181	470	Chip	0.125	5	20-5765
R182		Not Used			
R183		Not Used			
R184		Not Used			
R185		Not Used			
R186		Not Used			
R187		Not Used			
R188	1k	Chip	0.125	5	20-5792
R189	27k	Chip	0.125	5	20-5806
R190	1k	Chip	0.125	5	20-5792
R191	27k	Chip	0.125	5	20-5806
R192	10k	Variable			20-7071
R193	10k	Variable			20-7071
R194	10	Chip	0.125	5	20-5771
R195	20	Chip	0.125	5	20-5774

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R196	180	Chip	0.125	5	20-5784
R197		Not Used			
R198	10	Chip	0.125	5	20-5771
R199	20	Chip	0.125	5	20-5774
R200	180	Chip	0.125	5	20-5784
R201		Not Used			
R202	1k	Chip	0.125	5	20-5792
R203	1k	Chip	0.125	5	20-5792
R204	4.7k	Chip	0.125	5	20-5799
R205	330	Chip	0.125	5	20-5787
R206	330	Chip	0.125	5	20-5787
R207	330	Chip	0.125	5	20-5787
R208	330	Chip	0.125	5	20-5787
R209	330	Chip	0.125	5	20-5787
R210	330	Chip	0.125	5	20-5787
R211	1k	Chip	0.125	5	20-5792
R212	1k	Chip	0.125	5	20-5792
R213	1k	Chip	0.125	5	20-5792
R214	2.2k	Chip	0.125	5	20-5796
R215	6.8k	Chip	0.125	5	20-5801
R216	68	Chip	0.125	5	20-5780
R217	100k	Chip	0.125	5	20-5813
R218	10k	Chip	0.125	5	20-5768
R219	10k	Chip	0.125	5	20-5768
R220	10k	Chip	0.125	5	20-5768
R221	10k	Chip	0.125	5	20-5768
R222	10k	Chip	0.125	5	20-5768
R223	10k	Chip	0.125	5	20-5768
R224	10k	Chip	0.125	5	20-5768
R225	10k	Chip	0.125	5	20-5768
R226	68	Chip	0.125	5	20-5780
R227	10	Chip	0.125	5	20-5771
R228	1k	Chip	0.125	5	20-5792
R229	2.2k	Chip	0.125	5	20-5796
Capacitors	F		V		
C1	47µ	Electrolytic	25	20	21-0789
C2	10n	Chip	50	10	21-1801
C3	47µ	Electrolytic	25	20	21-0789
C4	10n	Chip	50	10	21-1801
C5	10n	Chip	50	10	21-1801

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C6	10n	Chip	50	10	21-1801
C7	10n	Chip	50	10	21-1801
C8	10n	Chip	50	10	21-1801
C9	10n	Chip	50	10	21-1801
C10	10n	Chip	50	10	21-1801
C11	10n	Chip	50	10	21-1801
C12	10n	Chip	50	10	21-1801
C13	1n	Chip	50	10	21-1800
C14	1n	Chip	50	10	21-1800
C15		Not Used			
C16		Not Used			
C17		Not Used			
C18		Not Used			
C19		Not Used			
C20		Not Used			
C21		Not Used			
C22	10n	Chip	50	10	21-1801
C23	47µ	Electrolytic	25	20	21-0789
C24	47µ	Electrolytic	25	20	21-0789
C25	47µ	Electrolytic	25	20	21-0789
C26	10n	Chip	50	10	21-1801
C27		Not Used			
C28	47µ	Electrolytic	25	20	21-0789
C29		Not Used			
C30		Not Used			
C31		Not Used			
C32		Not Used			
C33		Not Used			
C34		Not Used			
C35	1n	Chip	50	10	21-1800
C36	20n	Chip	400	10	21-1847
C37	33n	Chip	50	20	21-1808
C38		Not Used			
C39		Not Used			
C40	10n	Chip	50	10	21-1801
C41	33n	Chip	50	20	21-1808
C42	33n	Chip	50	20	21-1808
C43	33n	Chip	50	20	21-1808
C44	33n	Chip	50	20	21-1808
C45	33n	Chip	50	20	21-1808

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C46	47n	Chip	400	20	21-1859
C47	2.5n	Polypropylene	250	20	21-7002
C48	2.5n	Polypropylene	250	20	21-7002
C49	10000μ	Electrolytic	16		21-0683
C50	4700μ	Electrolytic	16	-10+30	21-0667
C51		Not Used			
C52	680μ	Electrolytic	25	20	21-0797
C53	47μ	Electrolytic	25	20	21-0789
C54	47μ	Electrolytic	25	20	21-0789
C55	47μ	Electrolytic	25	20	21-0789
C56	220p	Chip	50	5	21-1838
C57	220p	Chip	50	5	21-1838
C58	220p	Chip	50	5	21-1838
C59	680μ	Electrolytic	25	20	21-0797
C60		Not Used			
C61		Not Used			
C62		Not Used			
C63		Not Used			
C64		Not Used			
C65	20n	Chip	400	10	21-1847
C66	20n	Chip	400	10	21-1847
C67	6.8p	Chip	400	10	21-1859
C68	47p	Chip	50	2	21-1862
C69	6.8p	Chip	400	10	21-1859
C70	47p	Chip	50	2	21-1862
C71	2.7p	Chip	50	0.25p	21-1780
C72	3.9p	Chip	50	0.25p	21-1780
C73	100p	Chip	400	10	21-1857
C74	100p	Chip	400	10	21-1857
C75	10μ	Chip	50	10	21-1801
C76	10n	Chip	50	10	21-1801
C77	10n	Chip	50	10	21-1801
C78	10n	Chip	50	10	21-1801
C79	33n	Chip	50	10	21-1808
C80	100n	Chip	50	10	21-1802
C81	10n	Chip	50	10	21-1801
C82	33n	Chip	50	10	21-1808
C83	100n	Ceramic	50	20	21-1647
C84	10n	Chip	50	10	21-1801
C85	10n	Chip	50	10	21-1801

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C86	47µ	Electrolytic	25	20	21-0789
C87	3.3n	Chip	400	10	21-1858
C88	10n	Chip	50	10	21-1801
C89	47µ	Electrolytic	25	20	21-0789
C90	10n	Chip	50	10	21-1801
C91	10n	Chip	50	10	21-1801
C92	47µ	Electrolytic	25	20	21-0789
C93	10n	Chip	50	10	21-1801
C94	47µ	Electrolytic	25	20	21-0789
C95	47µ	Electrolytic	25	20	21-0789
C96	10n	Chip	50	10	21-1801
C97	10n	Chip	50	10	21-1801
C98	10n	Chip	50	10	21-1801
C99	10n	Chip	50	10	21-1801
C100	10n	Chip	50	10	21-1801
C101	10n	Chip	50	10	21-1801
C102	10n	Chip	50	10	21-1801
C103	10n	Chip	50	10	21-1801
C104	47µ	Electrolytic	25	20	21-0789
C105	47µ	Electrolytic	25	20	21-0789
C106	10n	Chip	50	10	21-1801
C107	33n	Chip	50	10	21-1808
C108	33n	Chip	50	10	21-1808
C109	10n	Chip	50	10	21-1801
C110	10n	Chip	50	10	21-1801
C111	47µ	Electrolytic	25	20	21-0789
C112	47µ	Electrolytic	25	20	21-0789
C113	47µ	Electrolytic	25	20	21-0789
C114	1µ	Electrolytic	50	20	21-0779
C115	10n	Chip	50	10	21-1801
C116	47µ	Electrolytic	25	20	21-0789
C117	10n	Chip	50	10	21-1801
C118	1n	Chip	50	10	21-1800
C119	10n	Chip	50	10	21-1801
C120	47µ	Electrolytic	25	20	21-0789
C121	1µ	Electrolytic	50	20	21-0779
C122		Not Used			
C123		Not Used			
C124		Not Used			
C125	47µ	Electrolytic	25	20	21-0789

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C126	1µ	Electrolytic	5	20	21-0779
C127	10n	Chip	50	10	21-1801
C128	1n	Chip	50	10	21-1800
C129	10n	Chip	50	10	21-1801
C130	10n	Chip	50	10	21-1801
C131	10n	Chip	50	10	21-1801
C132	33n	Chip	50	10	21-1808
C133	33n	Chip	50	10	21-1808
C225	47µ	Electrolytic	25	20	21-0789
C226	47µ	Electrolytic	25	20	21-0789

Diodes

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
D3		Silicon (1N4149)			22-1029
D4		Silicon (1N4149)			22-1029
D5		Silicon (1PAD50)			22-1099
D6		Silicon (1N4149)			22-1029
D7		Silicon (1N4149)			22-1029
D8		Silicon (JPAD50)			22-1099
D9		Not Used			
D10		Not Used			
D11		Bridge Rectifier (VH248)			22-1662
D12		Bridge (B40C800)			22-1664
D13		Silicon (1N4149)			22-1029
D14		Silicon (1N4149)			22-1029
D15		Silicon (1N4149)			22-1029
D16		Not Used			
D17		Not Used			
D18		Hot Carrier (5082.2835)			22-1086
D19		Hot Carrier (5082.2835)			22-1086
D20		Hot Carrier (5082.2835)			22-1086
D21		Hot Carrier (5082.2835)			22-1086
D22		Hot Carrier (5082.2835)			22-1086
D23		Hot Carrier (5082.2835)			22-1086
D24		Hot Carrier (5082.2835)			22-1086
D25		Hot Carrier (5082.2835)			22-1086

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
D26		Silicon (1N4149)			22-1029
D27		Not Used			
D28		Silicon (1N4149)			22-1029
D29		Not Used			
D30		BZX 79C2V7			22-1801
D31		BZX 79C2V7			22-1801
D32		BZX 79CC5V6			22-1809
D33		BZX 79CC5V6			22-1809
Transistors					
Q1		MPS 3640			22-6018
Q2		MPS 3640			22-6018
Q3		MPS 3640			22-6018
Q4		2N3904			22-6007
Q5		2N3904			22-6007
Q6		BDT 91			22-6152
Q7		ZTX550			22-6113
Q8		BDT92			22-6153
Q9		ZTX450			22-6112
Q10		ZTX450			22-6112
Q11		2N3904			22-6007
Q12		BDT92			22-6153
Q13		ZTX550			22-6113
Q14		2N3904			22-6007
Q15		BF256A			22-6163
Q16		BF256A			22-6163
Q17		BFS17			22-6206
Q18		BFS17			22-6206
Q19		Not Used			
Q20		Not Used			
Q21		BFS17			22-6206
Q22		2N3904			22-6007
Q23		BFS17			22-6206
Q24		2N3904			22-6007
Q25		2N3906			22-6008
Q26		2N3906			22-6008
Q27		2N3906			22-6008
Q28		ZTX550			22-6113
Q29		CA3083			22-4216

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Integrated Circuits					
IC1		10216			22-4590
IC2		10116			22-4528
IC3		7812 CT			22-4219
IC4		7912 CT			22-4294
IC5		Not Used			
IC6		Not Used			
IC7		Not Used			
IC8		Not Used			
IC9		Not Used			
IC10		Not Used			
IC11		Not Used			
IC12		Not Used			
IC13		Not Used			
IC14		10116			22-4528
IC15		Not Used			
IC16		Not Used			
IC17		Not Used			
IC18		MCC 1 (Custom Built)			22-8403
IC19		MC 146805E2			22-8307
IC20		74HCT373			22-4808
IC21		74LS138			22-4587
IC22		27128 (Programmed)			22-8572
IC23		74HCT224			22-4807
IC24		74LS373			22-4585
IC25		74HCT373			22-4808

NOTE: When ordering a replacement for IC22, it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
IC26		74LS74			22-4534
IC27		74LS32			22-4578
IC28		74LS10			22-4557
IC29		74LS04			22-4533
IC30		4011			22-4700

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
IC31		MC3403			22-4262
IC32		40106			22-4756
IC33		Not Used			
IC34		CA3140E			22-4269
IC35		CA3140E			22-4269
IC36		SP9687			22-4686
IC37		Not Used			
IC38		Not Used			
IC39		MCC2 (Custom Built)			22-840~~2~~4
IC40		Not Used			
IC41		MC10231			22-4542
H1		TEC (Custom Built)			17-1034
H2		DAC (Custom Built)			17-1035
<u>Inductors</u>	<u>H</u>				
L1	40µ	Choke			23-7217
L2	40µ	Choke			23-7217
L3		Not Used			
L4		Not Used			
L5	100µ	Choke			23-7213
L6	100µ	Choke			23-7213
L7	100µ	Choke			23-7213
L8	100µ	Choke			23-7213
L9	100µ	Choke			23-7213
L10	100µ	Choke			23-7213
L11	100µ	Choke			23-7213
L12		Not Used			
L13		Not Used			
L14		Choke			17-3166
L15		Choke			17-3166
L16		Not Used			
L17		Not Used			
L18		Not Used			
L19		Not Used			
L20	100µ	Choke			23-7213

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
PL1		Plug, 2x7-way			23-5162
PL2		Plug, 2x7-way			23-5162
PL3		Not Used			
PL4		Not Used			
PL5		Not Used			
PL6		Not Used			
PL7		Plug, 30-way			23-5174
PL8		Not Used			
PL9		Not Used			
PL10		Not Used			
PL11		Not Used			
PL12		Not Used			
PL13		Not Used			
PL14		Plug, 5-way			23-5164
PL15		Plug, 3-way			23-5175
PL16		Plug, 10-way			23-5165
PL17		Plug, 5-way			23-5164
PL18		Not Used			
PL19		Plug 2x3-way			23-5176
PL20		Plug, 2x2-way			23-5161
PL21		Plug, 2x10-way			23-5168
SK1		Not Used			
SK2		Not Used			
SK3		Not Used			
SK4		IC Socket, 28-way			23-3290
SK5		Socket, BNC			17-1039
SK6		Socket, BNC			17-1039
SK7		Not Used			
SK8		Socket, 6-way			23-5177
		AC Power Plug, PCB mounting			23-3429

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number

<u>Miscellaneous</u>

FS1		Fuselink 250mAT (193V to 253V)			23-0056
		Fuselink 500mAT (90V to 127V)			23-0052
		Fuseholder for FS1			23-0062
		Top for 23-0062			23-0063
		IC Socket, 28-way			23-3290
		IC Socket- 40-way			23-3297
S1		Mains Switch			23-4124
		Button for 23-4124			15-0674
		Control Rod for 23-4124			15-0693
T1		Mains Transformer			17-4102
RLA		Relay, Reed			23-7529
RLB		Relay, Reed			23-7529
RLC		Relay, Reed			23-7529
RLD		Relay, Reed			23-7529
RLE		Relay, DIL			23-7530
RLF		Relay, Reed			23-7528
RLG		Relay, Reed			23-7528
RLH		Relay, DPDT			23-7527

PARTS LIST

GPIB ASSEMBLY 19-1146

Fig 11

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
	Ω		W		
R1	9x3.3k	SIL Array			20-5532
R2	56	Carbon Film	¼	5	20-2560
R3	9x3.3k	SIL Array			20-5532
R4	330	Carbon Film	¼	5	20-2331
R5	330	Carbon Film	¼	5	20-2331
R6	330	Carbon Film	¼	5	20-2331
R7	5x3.3k	SIL Array			20-5531
R8	18	Carbon Film	¼	5	20-2180
R9	56	Carbon Film	¼	5	20-2560
R10	9x100k	SIL Array			20-5522
R11	5x100k	SIL Array			20-5558
Capacitors					
	F		V		
C1	47µ	Electrolytic	25	20	21-0789
C2	100n	Ceramic	50	20	21-1708
C3	100n	Ceramic	50	20	21-1708
C4	100n	Ceramic	50	20	21-1708
C5	100n	Ceramic	50	20	21-1708
C6	100n	Ceramic	50	20	21-1708
C7	100n	Ceramic	50	20	21-1708
C8	100n	Ceramic	50	20	21-1708
C9	10n	Ceramic	25	-20+80	21-1545
C10	10n	Ceramic	25	-20+80	21-1545
Integrated Circuits					
IC1		74HCT374			22-4809
IC2		74HCT374			22-4809
IC3		74HCT138			22-4806
IC4		7407			22-4063
IC5		74LS125			22-4657

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
IC6		74HCT02			22-4801
IC7		74HCT00			22-4800
IC8		74HCT138			22-4806
IC9		MC14805			22-8307
IC10		Programmed ROM			22-8009

NOTE: When ordering a replacement for IC10, it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
IC11		74HCT373			22-4808
IC12		68488			22-8305
IC13		4066			22-4761
IC14		75161			22-4284
IC15		75160			22-4283
IC16		74HCT74			22-4805
IC17		74HCT74			22-4805
IC18		74HCT00			22-4800
IC19		74HCT02			22-4801
IC20		74HCT32			22-4804
Miscellaneous					
		IC Socket, 28-way			23-3290
		IC Socket, 40-way			23-3297
		IC Socket, 14-way			23-3309
SK3		Connector, 24-way			23-3434
S1		Switch, 6-way, DIL			23-4102

PARTS LIST

OSCILLATOR ASSEMBLY 19-1147

Fig 13

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	100n	Ceramic	50	-20+80	21-1708
Connector					
SK14		Connector, 5-way			23-5166
Oscillator					
	10MHz	Crystal oscillator			23-9134

PARTS LIST

REFERENCE FREQUENCY MULTIPLIER ASSEMBLY 19-1164

Fig 15

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
	Ω		W		
R1	220	Chip	0.125	5	20-5785
R2	10k	Chip	0.125	5	20-5768
R3	12k	Chip	0.125	5	20-5802
R4	1.8k	Chip	0.125	5	20-5795
R5	100k	Chip	0.125	5	20-5813
R6	560k	Chip	0.125	5	20-5817
R7	10k	Chip	0.125	5	20-5768
R8	2.2k	Chip	0.125	5	20-5796
R9	2.2k	Chip	0.125	5	20-5796
R10	560	Chip	0.125	5	20-5789
R11	1.8k	Chip	0.125	5	20-5795
R12	330	Chip	0.125	5	20-5787
R13	2.2k	Chip	0.125	5	20-5796
R14	10k	Chip	0.125	5	20-5768
R15	10k	Chip	0.125	5	20-5768
R16	820	Chip	0.125	5	20-5791
R17	56	Chip	0.125	5	20-5779
R18	330	Chip	0.125	5	20-5787
R19	1.8k	Chip	0.125	5	20-5795
R20	56	Chip	0.125	5	20-5779
R21	56	Chip	0.125	5	20-5779
R22	820	Chip	0.125	5	20-5791
R23	1.8k	Chip	0.125	5	20-5795
R24	1.8k	Chip	0.125	5	20-5795
R25	1.8k	Chip	0.125	5	20-5795
R26	1.8k	Chip	0.125	5	20-5795
R27	220	Chip	0.125	5	20-5785
R28	220	Chip	0.125	5	20-5785
R29	220	Chip	0.125	5	20-5785
R30	220	Chip	0.125	5	20-5785
R31	220	Chip	0.125	5	20-5785

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors	F		V		
C1	33n	Chip	50	10	21-1808
C2	2-15p	Variable			21-6043
C3	220p	Chip	50	5	21-1838
C4	220p	Chip	50	5	21-1838
C5	33n	Chip	50	10	21-1808
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	10n	Chip	50	20	21-1801
C9	10n	Chip	50	20	21-1801
C10	10n	Chip	50	20	21-1801
C11	10n	Chip	50	20	21-1801
C12	10n	Chip	50	20	21-1801
C13	33n	Chip	50	10	21-1808
C14	33n	Chip	50	10	21-1808
C15	10n	Chip	50	20	21-1801
Diodes					
D1		Varactor (MV1640)			22-1097
D2		Silicon (BAS16)			22-1093
D3		Voltage regulator (BZX84C4V7)			22-1882
D4		Silicon (BAV99)			22-1096
D5		Silicon (BAV99)			22-1096
Transistor					
Q1		3904			22-6197
Q2		3906			22-6199
Q3		3906			22-6199
Q4		3904			22-6197
Q5		3904			22-6197
Q6		3904			22-6197
Q7		3904			22-6197
Integrated Circuits					
IC1		Not Used			
IC2		741			22-4292
IC3		MC10102			22-4514
IC4		74LS132			22-4582

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
SK16		Socket, 5-way			23-5166
SK17		Socket, 10-way			23-5167
Transformer					
T1		Transformer to Racal-Dana specification			17-3226

PARTS LIST

OSCILLATOR ASSEMBLY 19-1208

Fig 17

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	100n	Ceramic	50	20	21-1708
Connector					
SK14		Connector, 5-way			23-5166
Oscillator					
	10MHz	Oscillator, temperature compensated			23-9135

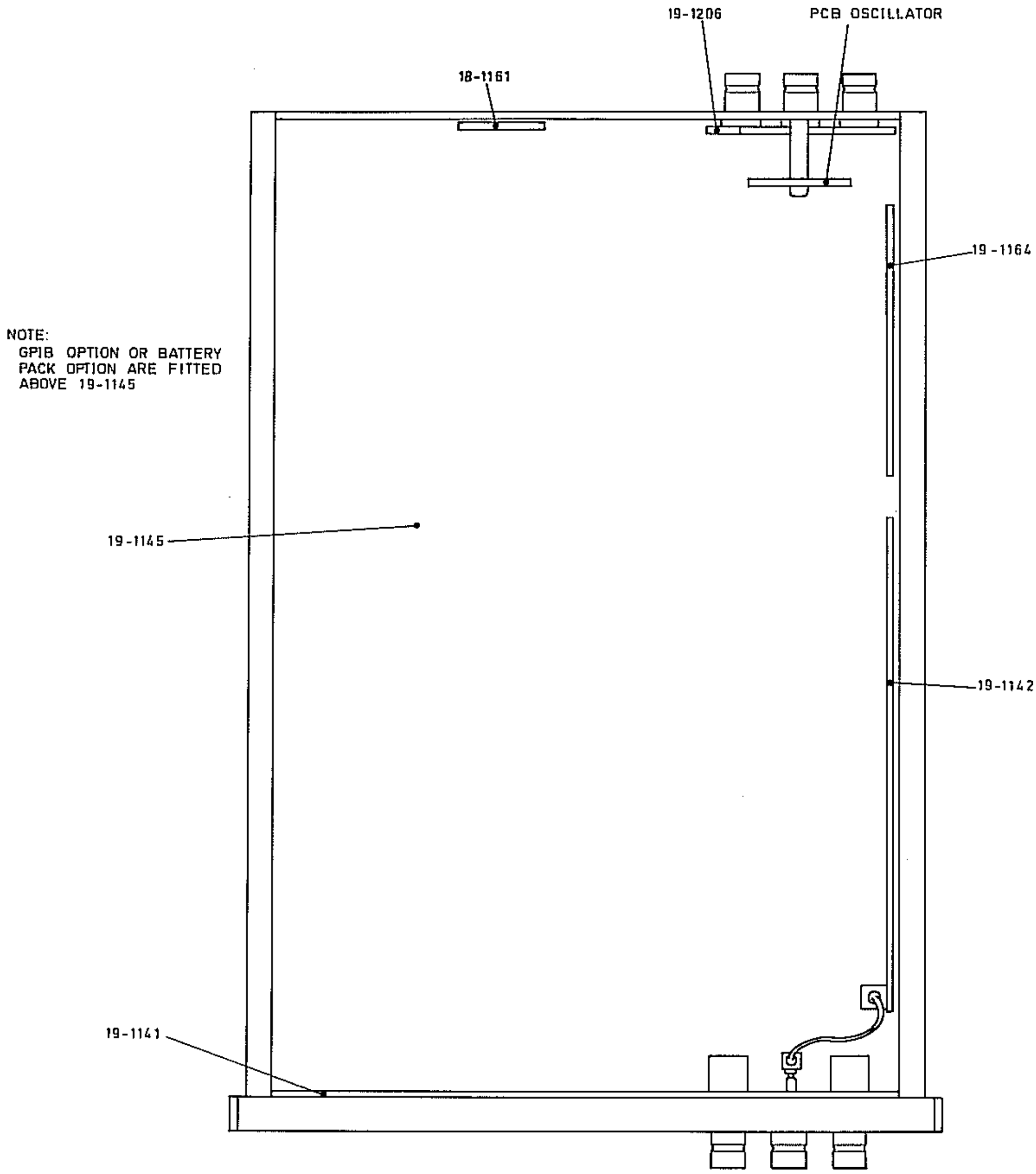
PARTS LIST

REFERENCE FREQUENCY DOUBLER ASSEMBLY 19-1238

Fig 17

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
	Ω		W		
R1	33	Chip	0.125	5	20-5776
R2	100	Chip	0.125	5	20-5764
R3	100	Chip	0.125	5	20-5764
R4	1k	Chip	0.125	5	20-5792
R5	470	Chip	0.125	5	20-5765
R6	470	Chip	0.125	5	20-5765
R7	1.5k	Chip	0.125	5	20.5794
R8	3.9k	Chip	0.125	5	20-5798
R9	3.9k	Chip	0.125	5	20-5798
R10	1.5k	Chip	0.125	5	20-5794
R11	1k	Chip	0.125	5	20-5792
R12	39k	Chip	0.125	5	20-5808
R13	15k	Chip	0.125	5	20-5803
R14	330k	Chip	0.125	5	20-5816
R15	10k	Chip	0.125	5	20-5768
R16	1k	Chip	0.125	5	20-5792
R17	3.9k	Chip	0.125	5	20-5798
R18	3.9k	Chip	0.125	5	20-5798
R19	100	Chip	0.125	5	20-5764
R20	1k	Chip	0.125	5	20-5792
Capacitors					
	F		V		
C1	10n	Chip	50	20	21-1801
C2	10n	Chip	50	20	21-1801
C3	10n	Chip	50	20	21-1801
C4	10n	Chip	50	20	21-1801
C5	10n	Chip	50	20	21-1801
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	10n	Chip	50	20	21-1801

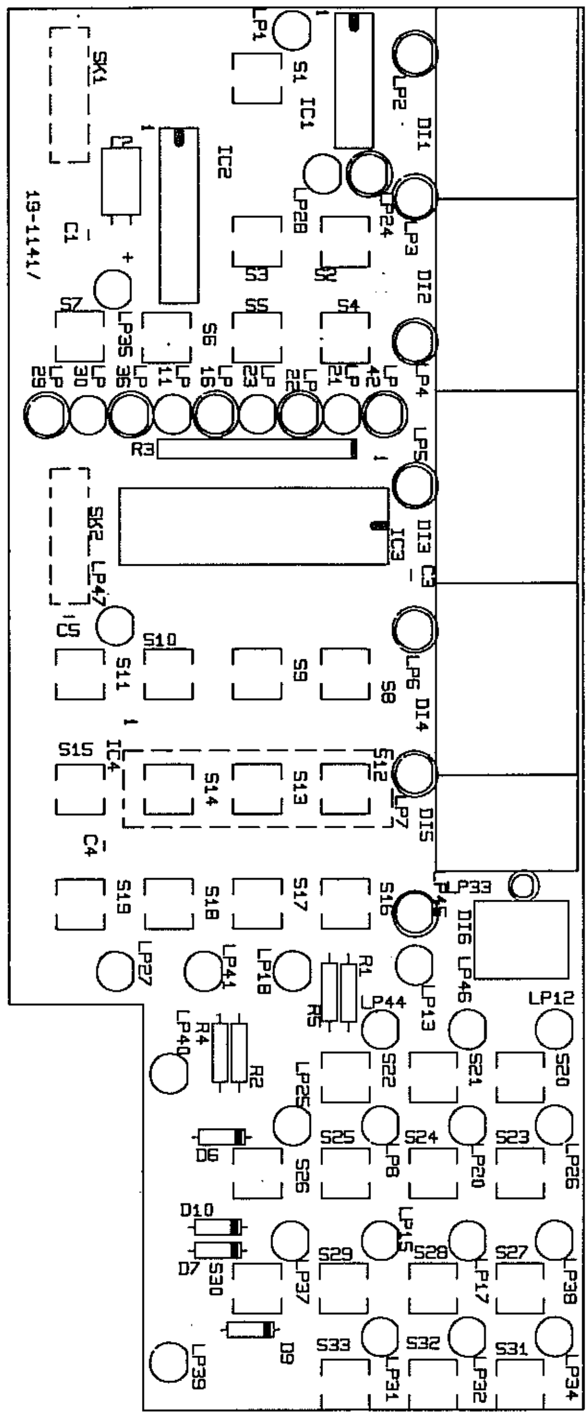
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Diodes					
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
Transistors					
Q1		2N3906			22-6008
Q2		2N3906			22-6008
Q3		2N3904			22-6007
Q4		2N3904			22-6007
Q5		2N3904			22-6007
Q6		2N3904			22-6007
Inductors					
	H				
L1	100μ	Choke		10	23-7213
T1		10.7 MHz IF Transformer			23-7149
T2		10.7 MHz IF Transforemer			23-7149



RACAL
TH 6428

Internal Layout

Fig.1



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Component Layout:
Display Assembly 19-1141

Fig. 2