1990

Service Manual

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MAINTENANCE MANUAL

1990

UNIVERSAL COUNTER

RACAL-DANA

RACAL

The Electronics Group

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1990

UNIVERSAL COUNTER

RACAL-DANA

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RACAL

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LETHAL VOLTAGE WARNING

VOLTAGES WITHIN THIS EQUIPMENT ARE SUFFICIENTLY HIGH TO ENDANGER LIFE.

COVERS MUST NOT BE REMOVED EXCEPT BY PERSONS QUALIFIED AND AUTHORISED TO DO SO AND THESE PERSONS SHOULD ALWAYS TAKE EXTREME CARE ONCE THE COVERS HAVE BEEN REMOVED.

RESUSCITATION

TREATMENT OF THE NON-BREATHING CASUALTY

1 SHOUT FOR HELP. TURN OFF WATER, GAS OR SWITCH OFF ELECTRICITY IF POSSIBLE

Do this immediately. If not possible don't waste time searching for a tap or switch.

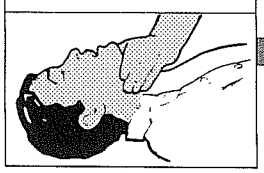
2 REMOVE FROM DANGER: WATER, GAS, ELECTRICITY, FUMES, ETC.

Safeguard yourself when removing casualty from hazard. If casualty still in contact with electricity, and the supply cannot be isolated, stand on dry non-conducting material (rubber mat, wood, linoleum).
Use rubber gloves, dry clothing, length of dry rope or wood to pull or push casualty away from the hazard.

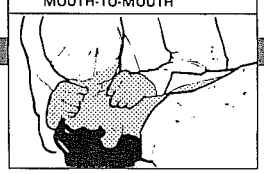
3 REMOVE OBVIOUS OBSTRUCTION TO BREATHING

If casualty is not breathing start ventilation at once.

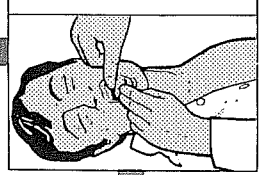
LOOSEN NECKWEAR
TILT HEAD BACKWARDS
AND PUSH CHIN UPWARDS



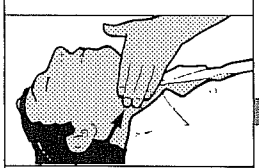
PINCH THE NOSE
COMMENCE VENTILATION
FOUR GOOD INFLATIONS
MOUTH-TO-MOUTH



IF CHEST DOES NOT RISE
RE-CHECK AIRWAY, REMOVE
OBSTRUCTION AND RE-INFLATE



CHECK PULSE



POSITION OF PULSE

PULSE PRESENT

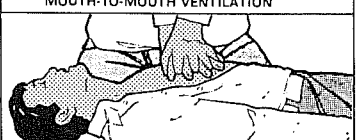
PULSE ABSENT

CONTINUE INFLATIONS
UNTIL RECOVERY OF
NORMAL BREATHING

HEART HAS STOPPED BEATING
LAY ON BACK ON FIRM SURFACE
(eg FLOOR).
COMMENCE EXTERNAL CHEST
COMPRESSION AND CONTINUE
MOUTH-TO-MOUTH VENTILATION

ONE FIRST AIDER
15 Compressions at 80 per minute followed by 2 Inflations

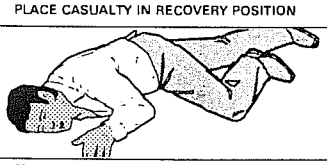
TWO FIRST AIDERS
One conducts chest compressions, without pause at 60 per minute. The other administers mouth-to-mouth ventilation – after each 5th compression.



Check heart beat after first minute and then after every three minutes. Continue external chest compression and mouth-to-mouth ventilation until a normal pulse is felt and colour improves.

CONTINUE INFLATIONS
UNTIL RECOVERY OF
NORMAL BREATHING

WHEN NORMAL BREATHING COMMENCES
PLACE CASUALTY IN RECOVERY POSITION



Keep casualty at rest. Remove on a stretcher. Watch closely, particularly for difficulty in breathing. Lightly cover with blankets or other materials.

SEND FOR DOCTOR AND AMBULANCE

DOCTOR	AMBULANCE	HOSPITAL	Nearest First Aid Post
TELEPHONE	TELEPHONE	TELEPHONE	

Universal Counter 1990

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of identification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

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SECTION 1 TECHNICAL SPECIFICATION

Input Characteristics

Frequency Range

Input A	DC to 120MHz DC coupled 10Hz to 120MHz AC coupled
Input B	DC to 100MHz DC coupled 10Hz to 100MHz AC coupled

Sensitivity

Sine Wave	25mVrms DC to 100MHz 50mVrms to 120MHz
Pulse	75mV p-p, 5ns min. width

Dynamic Range (x 1 attenuation)	75mV to 5V p-p to 50MHz 75mV to 2.5V p-p to 100MHz 150mV to 2.5V p-p to 120MHz

Signal Operating Range

x 1 attenuation	±2.5V
x 10 attenuation	±25V

Input Impedance (nominal)

Separate Mode (x1/x10)	1 Mohm //≤45pF
Common Mode (x1)	500kohm //≤55pF
Common Mode (x10)	1 Mohm //≤55pF

Maximum Input (without damage)

x1 attenuation	260V(DC + ACrms), DC to 2kHz Decreasing to 5Vrms, at 100kHz and above
x10 attenuation	260V(DC + ACrms), DC to 20kHz Decreasing to 50Vrms at 100 kHz and above
Coupling	AC or DC
Low Pass Filter	50kHz nominal (Input A selectable)
Trigger Slope	+ve or –ve
Attenuator	x1 or x10 nominal

Trigger Level Range

Manual

x1 attenuation	±2.8V typical
x10 attenuation	±28V typical

Trigger Level Output

Range	±2.8V typical
Accuracy*	
x1 (sep/common)	±10mV ± 5% of V output
x10 (separate mode)	±100mV ± 7% of V output
Impedance	10kohm nominal

Measurement Modes

Frequency A

Range	DC to 120MHz
Digits Displayed	3 to 8 digits plus overflow
LSD Displayed (Hz)	$F \times 10^{-D}$ (D = No. of digits, F = Freq. rounded up to next decade)*
Resolution *(Hz)	± LSD ± (Trig. Error* x Freq.)/Gate Time
Accuracy *(Hz)	± Resolution ± (Timebase Error x Freq.)

Time Interval

Range

Single	100ns to 8×10^5 sec
Averaged	10ns to 8×10^5 sec

Input

Common	Input A START and STOP
Separate	Input A START Input B STOP

Trigger Slopes	+ve or –ve Selectable START and STOP
LSD Displayed	100ns min. (10ns with averaging)
Resolution* (sec)	± LSD ± 5ns rms ± Trig Error*
Accuracy* (sec)	± Resolution ± (Timebase Error x TI) ± Trigger Level Timing Error* ± 2ns**

Time Delay

Available on Time Interval and Totalise

Range	200μs to 800ms nominal
Step Size	1ms nominal. (Extra step to 200μs)
Accuracy	± 0.1% setting ± 50μs

Period A

Range	8.3ns to 1.7×10^3 sec
Digits Displayed	3 to 8 digits plus overflow
LSD Displayed (sec)	$P \times 10^{-D}$ (D = No. of digits, P = Period rounded up to next decade)*
Resolution* (sec)	± LSD ± (Trig. Error* x Period)/Gate Time
Accuracy* (sec)	± Resolution ± (Timebase Error x Period)

Ratio A/B

Specified for higher frequency applied to Input A

Range	DC to 100MHz on both inputs
LSD Displayed (for 4-8 digits selected)	$\left(\frac{10}{\text{Freq. B} \times \text{Gate Time}}\right)$, rounded to nearest decade*
Resolution*	± LSD ± (Trig. Error B*/Gate Time) x Ratio
Accuracy*	± Resolution

*see definitions **A differential delay between amplifiers

Totalise A by B and Total A

Input	Input A
Start/Stop	Electrical (Input B) or Manual
Range	10^{12} - 1 (8 most significant digits displayed)
Maximum Rate	10^{8} events/sec.
Minimum Pulse Width	5ns min. at trigger points
Accuracy	±1 count

Phase (A rel. to B)

Range	0.1° to 360°
LSD Displayed	Normal (averaged) 1° (0.1°) to 100kHz 10° (1°) to 1MHz 100° (10°) to 5MHz
Resolution* (degrees)	± LSD ± (TI Resolution/Period A) x 360°
Accuracy* (degrees)	± LSD ± (TI Accuracy/Period A) x 360°

Time

Start/Stop	Manual
Range	40ms to 8 x 10^{5} sec.
Resolution	± 40ms
Accuracy	± Resolution ± (Timebase Error x Time)

100 Average

Function	Displays average value of 100 measurements
Averaging Time	2.5 sec. + (100 x single measurement time)

Null

Available on all measurements except Phase and Check

Function	Displays (Result – Null)
Entry Range	± 1 x 10^{-9} to ± 1 x 10^{10} to 8 significant figures

Single Cycle (Hold)
Enables a single measurement to be initiated and held

General

Internal Timebase
Crystal Controlled

Frequency	10MHz
Aging	2 x 10^{-6} in the first year
Temperature Stability	± 1 x 10^{-5} over the range 0 to +50°C
Adjustment	Internal

Gate Time

(Frequency, Period and Ratio modes)	Automatically determined by resolution selected. (Range 1msec-10sec)

Resolution Selected (Digits) / Gate Time*(s)

8	10
7	1
6	0.1
5	0.01
4,3	0.001

Display	8 – digit, high brightness, 14mm LED display in engineering format with exponent digit
Power Requirements	
Voltage (AC)	90–110V 103-127V 193-237V 207-253V } externally selectable
Frequency	45-440Hz
Rating	35VA Max
Operating Temperature Range	0° to +50°C (0° to +40°C with battery pack)
Storage Temperature Range	–40°C to +70°C (–40°C to +60°C with battery pack)
Environmental	Designed to meet MIL-T-28800, DEF-STD 66/31 and IEC 68
Safety	Designed to meet the requirements of IEC348 and follow the guidelines of UL1244
RFI/EMC	MIL-STD-461B
Weight	Net 3.6kg (8lb) excl. battery 6.8kg (15lb) incl. battery Shipping 5.5kg (12lb) excl. battery 8.75kg (19.3lb) incl. battery
Dimensions	331 x 218 x 101mm (13.03 x 8.58 x 3.98 ins)
Shipping Dimensions	430 x 360 x 280mm (16.9 x 14.2 x 11.0 ins)

Options

Option 02

Frequency Standard Input/Output

Frequency Standard Output

Frequency	10MHz
Amplitude	TTL levels giving approx. 1Vp-p into 50 ohms
Impedance	90 ohms nominal
Reverse Input	±15V max

*see definitions

External Standard Input

Frequency	10MHz (see also Option 10 for other frequencies)
Single Amplitude (Sine Wave)	300mVrms min. 10Vrms max.
Impedance	1 kohm nominal at 1V p-p

Option 04T

Temperature Compensated Crystal Oscillator

Frequency	10MHz
Aging Rate	3×10^{-7}/month 1×10^{-6} in the first year
Temperature Stability	$\pm 1 \times 10^{-6}$ over the range 0 to 40°C (operable to +50°C)
Adjustment	Via rear panel

Option 04A

Ovened Oscillator

Frequency	10MHz
Aging Rate	3×10^{-9}/day averaged over 10 days after 3 months continuous operation
Temperature Stability	$\pm 3 \times 10^{-9}$/°C averaged over range 0° to +45°C (operable to +50°C)
Warm Up	Typically $\pm 1 \times 10^{-7}$ within 6 minutes
Adjustment	Via rear panel

Option 04B

High Stability Ovened Oscillator

Frequency	10MHz
Aging Rate	5×10^{-10}/day averaged over 10 days after 3 months continuous operation
Temperature Stability	$\pm 6 \times 10^{-10}$/°C averaged over range 0° to 50°C
Warm Up	$\pm 1 \times 10^{-7}$ within 20 minutes
Adjustment	Via rear panel

Option 07

Rechargeable Battery Pack and External DC Operation

Battery Type	Sealed lead-acid cells
Battery Life	Typically 5.75 hours at +25°C (24 hrs on standby)
Battery Condition	Display indicates battery low
External DC	11-16V via socket on rear panel (–ve ground, not isolated)

Option 10

Reference Frequency Multiplier

Input Frequency	1,2,5 or 10MHz ($\pm 1 \times 10^{-5}$)
Input Amplitude and Impedance	As for external standard input

Option 55

GPIB Interface	Designed to comply with IEEE-STD-488 (1978) and to conform with the guidelines of IEEE-STD-728 (1982)
Control Capability	All functions and controls programmable except power on/off, trigger levels and standby/charge
Output	Engineering format (11 digits and exponent)
IEEE-STD-488 Subsets	SH1, AH1, T5, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C0, E2
Handshake Time	250μs to 1ms/character dependent on message content.
Read Rate	Typically 22/sec dependent upon measurement function

Definitions

LSD
(Least Significant Digit) — In Frequency and Period modes display automatically upranges at 1.1 x decade and downranges at 1.05 x decade

Accuracy and Resolution — Expressed as an rms value,

Trigger Error = (seconds)

$$\sqrt{\left(\frac{(e_i^2 + e_n^2)}{S^2}\right)_1 + \left(\frac{(e_i^2 + e_n^2)}{S^2}\right)_2} \text{ (rms)}$$

where e_i = input amplifier rms noise (typically 200μVrms in 120MHz bandwidth)
e_n = input signal rms noise in 120MHz bandwidth
S = Slew rate at trigger point V/sec
Suffix 1 denotes START edge
Suffix 2 denotes STOP edge
In Frequency A and Period A, triggering is always on positive going edge

Trigger Level Timing Error

$$\text{Trigger Level Timing Error (Seconds)} = 0.035 \left(\frac{1}{S1} - \frac{1}{S2}\right)$$

$$\text{typically} = 0.018 \left(\frac{1}{S1} - \frac{1}{S2}\right)$$

S1 = Slew rate on START edge V/sec.
S2 = Slew rate on STOP edge V/sec.

Trigger level output accuracy is referenced to the centre of the hysteresis band.

Gate Time
The nominal gate time indicated is set by the resolution selected in Frequency, Period, Ratio and Check modes. It is the value which is used in the calculation of LSD and Resolution. The true gate time will be extended from this value by up to one period of the input signal(s) on Frequency A, Period A and Ratio A/B.

Supplied Accessories

Power Cord
Spare Fuse
Operator's Manual

Ordering Information

1990	120MHz Universal Counter

Options and Accessories

02	Frequency Standard Input/Output	11-9000
04T**	TCXO	11-1713
04A*	Oven Oscillator	11-1710
04B*	High Stability Oven Oscillator	11-1711
07†	Battery Pack	11-1625
***10**	Reference Frequency Multiplier	11-1645
55†	GPIB Interface	11-9001
60	Handles	11-1730
60A	Rack Mounting Kit (Fixed, Single)	11-1648
60B	Rack Mounting Kit (Fixed, Double)	11-1649
61	Hard Carrying Case	15-0773
61M	Protectomuff Case	15-0736
65	Chassis Slides (incl. Rack Mounts)	11-1716
	Telescopic Antenna	23-9020
	High Impedance Probe (1MΩ)	23-9104

* Option 02 must also be purchased with these options

** Only one frequency standard may be fitted at any one time. The standard reference will be supplied unless option 04T, 04A or 04B is specified

† The battery pack and GPIB options cannot both be fitted

INTRODUCTION

1 The Racal-Dana universal counter Model 1990 is a microprocessor controlled instrument using recipromatic measurement techniques. The instrument offers a comprehensive range of functions and easy to use controls.

MEASUREMENT FUNCTIONS

Frequency A Function

2 The Frequency A function is used to measure the frequency of the signal applied to the channel A input. A resolution of seven digits is available with a one-second gate time.

Period A Function

3 The Period A function is used to measure the period of the waveform applied to the A channel input. A number of periods, depending upon the resolution (and therefore the gate time) selected, are measured, and the average value is displayed.

Time Interval Function

4 The Time Interval function is used to make single-shot measurements of the time interval between:

(1) An event occurring at the channel A input and a later event at the channel B input (using separate input channels).

(2) Two events occurring at the channel A input (using a common input channel).

5 The arming of the stop circuit can be delayed for a time set by the operator. This prevents the measurement interval being stopped prematurely by spurious pulses, such as those caused by contact bounce.

Total A by B Function

6 The Total A by B function permits events occurring at the channel A input to be totalized. The counting interval is controlled by electrical start and stop signals applied to the channel B input, where alternate edges start and stop the measurement.

7 Delayed arming of the stop circuit is available in the Total A by B mode to prevent spurious triggering.

Phase A rel B Function

8 The Phase A rel B function is used to measure the phase difference between the waveform applied to the A channel input and that applied to the channel B input. The phase difference is displayed in degrees, and indicates the phase lead at the channel A input.

Ratio A/B Function

9 The Ratio A/B function is used to measure the ratio of the frequency applied to the channel A input to that applied to the channel B input.

Total A Function

10 The Total A function totalizes events occurring at the Channel A input. The counting interval is controlled by successive operations of the front panel HOLD (start/stop) key.

Time Function

11 The time function is used to measure the time interval between successive operations of the front panel HOLD (start/stop) key, ie. stop watch.

CHECK FUNCTION

12 With the Check function selected a number of functional tests of the instrument's circuits can be made without the use of additional test equipment. Although these tests do not check the instrument's performance to its published specification, they can be used to verify that the equipment is operating correctly following receipt or transportation to a new location. A suitable functional check procedure is given in Section 3.

SIGNAL INPUT CHANNELS

13 Signal input channels A and B are fully independent, but provision is made for connection of the signal at the channel A input into both channels. When this is done, the channel B input socket is isolated from channel B.

14 Each channel is provided with independent controls to permit the selection of:

(1) AC or DC input coupling.

(2) X1 or X10 input attenuation.

(3) Positive- or negative-slope trigger.

(4) Manually-set input trigger level.

The trigger levels are set by the front panel potentiometers which also have a set zero position.

The trigger voltage levels in use are also available at pins mounted on the front panel of the instrument. The input trigger voltage range is typically ±2.8 V. The voltage should be multiplied by 10 when the attenuator is selected.

LOW-PASS FILTER

15 An internal low-pass filter can be introduced to reduce the bandwidth of channel A to 50 kHz (nominal).

NULL FUNCTION

16 With the NULL function active the instrument displays the difference between the measured value and the value held in the internal NULL store.

DELAY FUNCTION

17 In Time Interval and Total A by B, the stop circuit can be delayed. With the delay function active, the stop circuit is prevented from being triggered prematurely by spurious signals.

100 AVERAGE FUNCTION

18 Enabling this function increases the resolution by taking 100 measurements and displaying the averaged value. The signal must be repetitive and asynchronous with the counter standard.

SPECIAL FUNCTIONS

19 A number of special functions are available to the operator. These provide test procedures and operating facilities additional to those available by operation of the front panel controls. Details are given in Section 4 of this manual.

ERROR INDICATION

20 Certain errors in the operation of the instrument will result in the generation of error codes, which will be displayed. Details are given in Section 4 of this manual.

DISPLAY FORMAT

21 The display uses an engineering format, with an eight digit mantissa and one exponent digit. Overflow of the most significant digits can be used to increase the display resolution.

HOLD FEATURE

22 The hold feature allows readings to be held indefinitely. A new measurement cycle is initiated using the RESET key.

RESOLUTION AND GATE TIME

23 In the Total A by B, Total A and Time modes, the counting interval (gate time) is controlled by the time interval between the start and stop signals at the channel B input, or between successive operations of the HOLD key. In the Frequency A, Period A and Ratio A/B modes, the gate time is determined by the display resolution selected. In Phase mode, the gate time is fixed and the display resolution is determined by the input signal frequency. Details of the relationship between gate time and resolution for each measurement mode are given in Section 4 of this manual.

STANDBY MODE

24 When the instrument is switched to standby, the internal frequency standard continues to operate but the measuring circuits are switched off. If the battery pack option is fitted and an external power supply is connected, the battery is charged at the full rate.

INITIALIZATION

25 When the instrument is first switched on, or when it is initialized via the GPIB, it is set to the following conditions:

Measurement Function	FREQ A
Display Resolution	6 digits
Channel A and B Inputs	AC coupling Positive-slope trigger LF filter disabled Common input disabled
Delay Delay Store	Disabled 1 ms
Null Function Null Store	Disabled 0
100 Avg	Disabled
Hold	Disabled
Special Functions	Off

OPTIONS AVAILABLE

Frequency Standards (04X Options)

26 A wide range of internal frequency standard options is available. The technical specifications are given in Section 1 of this manual. The frequency standard can be changed, if required, by the customer: instructions are given in Section 3.

Reference Frequency Multiplier (Option 10)

27 The reference frequency multiplier is an internally-mounted, phase-locked multiplier, which permits the use of external frequency standard signals at 1 MHz, 2 MHz, 5 MHz or 10 MHz. The multiplier can be fitted by the customer: instructions are given in Section 3.

Reference Input and Output (Option 02)

28 The instrument may be operated using an external frequency standard. The instrument will operate from the external standard, in preference to the internal standard, whenever the signal at the EXT STD INPUT socket is of sufficient amplitude. It will revert to operation from the internal standard automatically if the external standard is removed. The 10 MHz STANDARD OUTPUT connector provides a signal derived from whichever standard is in use at the time.

GPIB Interface (Option 55)

29 An internally mounted IEEE-488-GPIB interface is available. This permits remote control of all the instrument's functions except the power ON/OFF, standby switching and trigger levels. The interface can be fitted by the customer: instructions are given in Section 3. The GPIB interface cannot be fitted to an instrument already fitted with the battery pack option. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an accessory.

Battery Pack (Option 07)

30 Fitting the internal battery permits the instrument to be used in locations where no suitable AC supply is available. The option also allows operation from an external DC supply with the internal/external switch set to EXTERNAL 11-16V DC position.

31 The battery is trickle-charged whenever the instrument is operated from an AC supply. Charging at the full rate is carried out when the instrument is switched to the standby mode. A full charge requires approximately 14 hours.

32 The instrument will operate continuously for approximately 5¾ hours from a fully-charged battery. It will switch off automatically when the battery approaches the discharged condition. The STBY/CHRG indicator starts to flash approximately 15 minutes before this occurs. The battery life can be extended by use of the Battery-Save facility.

33 The battery pack can be fitted by the customer. Instructions are given in Section 3. The battery pack cannot be fitted to an instrument already fitted with the GPIB interface option.

Rack Mounting Kits

34 The following kits, permitting the instrument to be mounted in a standard 19-inch rack are available:

(1) Single instrument, fixed-mount kit (Option 60A).
(Racal-Dana part number 11-1648).
The mounted instrument occupies half the rack width and is two rack units (3.5 inches) in height. The instrument is mounted offset in the rack and may be at either side.

(2) Double instrument, fixed-mount kit (Option 60B).
(Racal-Dana part number 11-1649).
The panel of the mounting kit occupies the full rack width and is two rack units (3.5 inches) in height. Two instruments can be mounted side-by-side.

35 All the kits can be fitted by the customer. Instructions are given in Section 3.

UNPACKING

1 Unpack the instrument carefully to avoid unnecessary damage to the factory packaging.

2 If it becomes necessary to return the instrument to Racal-Dana Instruments for calibration or repair, the original packaging should be used. If this is not possible, a strong shipping container should be used. Ensure that sufficient internal packing is used to prevent movement of the instrument within the container during transit.

POWER SUPPLY

AC Line Voltage Setting

3 Before use, check that the AC voltage selector is set correctly for the local AC supply. The voltage range already set can be seen through a window in the selector board retaining clamp to the left of the AC power plug.

4 If it is necessary to change the setting, proceed as follows:

(1) Undo the selector board retaining clamp on the rear panel.

(2) Withdraw the board.

(3) Replace the board with the required voltage setting positioned so that it will show through the window in the retaining clamp.

(4) Replace the retaining clamp.

Line Fuse

5 Check that the rating of the line fuse is suitable for the AC voltage range in use. The fuse should be of the $\frac{1}{4}$ in x $1\frac{1}{4}$ in, glass cartridge, surge-resisting type. The required rating is:

90 V to 127 V: 500 mAT (Racal-Dana part number 23-0052).
193 V to 253 V: 250 mAT (Racal-Dana part number 23-0056).

Power Cord

6 The 1990 is a Safety Class 1 instrument, which is designed to meet international safety standards. A protective ground terminal, which forms part of the power-input connector on the rear panel, is provided. Each instrument is supplied with a 3-core power cord. Only the power cord supplied should be used to make electrical connection to the power-input connector.

7 AC power for the instrument must be taken from a power outlet incorporating a protective ground connector. When the green/yellow conductor of the power cord is joined to this connector, the exposed metalwork of the instrument is grounded. The continuity of the protective ground connection must not be broken by the use of 2-core extension cords or 3-prong to 2-prong adapters.

8 Connection of the power cord to the power outlet must be made in accordance with the standard color code.

	European	American
Line	Brown	Black
Neutral	Blue	White
Ground (Earth)	Green/Yellow	Green

FUNCTIONAL CHECK

9 The check given in paragraph 10 tests the operation of most of the instrument's circuits to establish whether the instrument is functioning correctly. The procedure should be followed when the instrument is first taken into use, and after transportation to a new location. It does not check that the instrument is operating to the published specification. Detailed specification tests are given in Section 7 of the maintenance manual.

10 (1) Connect the instrument to a suitable AC supply.

(2) Switch the instrument on. Check that the instrument type-number appears in the display for approximately two seconds, followed by a number which indicates the software version and issue number.

(3) Press the FUNCTION ↓ key until the CHECK indicator lights. Check that the display shows 10.00000 E 6 Hz and that the GATE indicator is flashing.

(4) Verify that the RESOLUTION indicator is lit. Press the RESOLUTION ↓ key three times, ensuring that the resolution of the display is decreased by one digit each time.

(5) Press the RESOLUTION ↑ key four times to increase the resolution to seven digits, and check that the GATE indicator flashes about once a second.

(6) Press the RECALL key. Check that all LEDs, with the exception of REM, ADDR, SRQ, GATE, TRIG A, TRIG B and STBY/CHRG flash on and off every two seconds. If the GPIB option is installed, the REM, ADDR and SRQ indicators should be lit.

(7) Press the RESET/CONTINUE key to return to the check functions.

FREQUENCY STANDARD (Input/Output) Option 02)

11 If it is intended to use an external frequency standard, the output of the frequency standard should be connected to the EXT STD INPUT connector on the rear panel of the instrument. The connection should be made using coaxial cable. Switch on the frequency standard and the instrument: check that the EXT STD indicator on the front panel of the instrument lights.

12 A 10 MHz signal, derived from the frequency standard in use, is available at the 10 MHz STD OUT connector on the rear panel of the instrument. If this signal is used, the connection should be made using coaxial cable.

TRIGGER LEVEL OUTPUT

13 The trigger levels in use on channels A and B are available via pins on the instrument front panel. If required, connection to the pins should be made using a clip-on probe or small crocodile clip.

PREPARATION FOR USE WITH THE GPIB

Introduction

14 The instrument must be prepared for use in accordance with the instructions given in Paragraphs 3 to 8 before the instructions given in this section are implemented.

Connection to the GPIB

15 Connection to the GPIB is made via a standard IEEE-488 connector, mounted on the rear panel. The pin assignment is given in Table 3.1. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an optional accessory.

TABLE 3.1

GPIB Connector Pin Assignment

Pin	Signal Line	Pin	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd (6)
7	NRFD	19	Gnd (7)
8	NDAC	20	Gnd (8)
9	IFC	21	Gnd (9)
10	SRQ	22	Gnd (10)
11	ATN	23	Gnd (11)
12	SHIELD	24	Gnd (5 and 17)

Address Setting and Display

16 The interface address is set using five switches, A1 to A5, which are mounted on the rear panel. The permitted address settings, in binary, decimal and ASCII character form, are given in Table 3.2. The GPIB address set can be displayed, in decimal form, by pressing

[RECALL] [LOCAL]

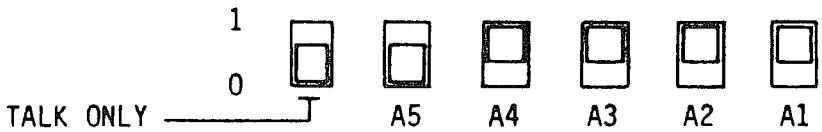
If the address is changed, this key sequence must be repeated to display the new address. The instrument is returned to the measurement mode by pressing

[CONTINUE]

17 For addressed operation, the TALK ONLY switch must be in the logic '0' position (down). When this switch is in the logic '1' position, the interface is switched to the talk-only mode. The settings of switches A1 to A5 are then irrelevant.

TABLE 3.2

Address Switch Settings



SWITCH SETTINGS					ADDRESS CODES		
A5	A4	A3	A2	A1	DECIMAL	ASCII LISTEN ADDRESS	ASCII TALK ADDRESS
0	0	0	0	0	0	SP	@
0	0	0	0	1	1	!	A
0	0	0	1	0	2	"	B
0	0	0	1	1	3	#	C
0	0	1	0	0	4	$	D
0	0	1	0	1	5	%	E
0	0	1	1	0	6	&	F
0	0	1	1	1	7	'	G
0	1	0	0	0	8	(	H
0	1	0	0	1	9	)	I
0	1	0	1	0	10	*	J
0	1	0	1	1	11	+	K
0	1	1	0	0	12	,	L
0	1	1	0	1	13	-	M
0	1	1	1	0	14	.	N
0	1	1	1	1	15	/	O
1	0	0	0	0	16	0	P
1	0	0	0	1	17	1	Q
1	0	0	1	0	18	2	R
1	0	0	1	1	19	3	S
1	0	1	0	0	20	4	T
1	0	1	0	1	21	5	U
1	0	1	1	0	22	6	V
1	0	1	1	1	23	7	W
1	1	0	0	0	24	8	X
1	1	0	0	1	25	9	Y
1	1	0	1	0	26	:	Z
1	1	0	1	1	27	;	[
1	1	1	0	0	28	<	\
1	1	1	0	1	29	=	]
1	1	1	1	0	30	>	^

GPIB CHECK

18 The procedure which follows checks the ability of the instrument to accept, process and send GPIB messages. The correct functioning of the instrument under local control should be verified before the procedure is attempted.

19 The recommended test equipment is the Hewlett-Packard HP-85 GPIB controller, with the I/O ROM in the drawer. It is assumed that the select code of the controller I/O port is 7, and that the address of the instrument is 15 (to change the address, see Paragraph 16). If any other controller or select code/address combination is used, the GPIB commands given in the following paragraphs will require modification. The controller should be connected to the GPIB interface of the instrument via a GPIB cable. No connection should be made to the channel A or B inputs.

20 Successful completion of the GPIB check proves that the instrument's GPIB interface is operating correctly. The procedure does not check that all the device-dependent commands can be executed. However, if the GPIB interface works correctly and the instrument operates correctly under local control, there is a high probability that it will respond to all device-dependent commands.

Remote and Local Message Check

21 Switch the instrument on. Check that the REM, ADDR and SRQ indicators flash on and off once. If the indicators do not flash, or if they flash continuously, there is a fault on the GPIB board.

22 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 715	

Check that the REM indicator lights.

23 Test as follows:

Action	HP-85 Code	Your Controller
Send the device-dependent command CK	OUTPUT 715; "CK"	

Check that the ADDR indicator lights and that the Check mode is selected.

24 Test as follows:

Action	HP-85 Code	Your Controller
Send the instrument's listen address followed by the GTL message	LOCAL 715	

Check that the REM indicator is off. The ADDR indicator will also be off if the controller used sends the unlisten message (UNL) true automatically. This is the case when using the HP-85.

Local Lockout and Clear Lockout Check

25 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 715	
Send the LLO message	LOCAL LOCKOUT 7	

Check that the REM indicator lights. Operate the LOCAL key on the front panel and verify that the REM indicator remains lit.

26 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message false	LOCAL 7	

Check that the REM indicator is off.

27 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 715	

Check that the REM indicator lights. Press the LOCAL key and verify that the REM indicator turns off.

Data Output Check

28 Test as follows:

Action	HP-85 Code	Your Controller
Set the instrument to the check mode by sending the listen address, followed by the device-dependent command CK	OUTPUT 715; "CK"	
Prepare a store to receive a 21-byte data string	DIM Z$ 21	
Send the instrument's talk address. Store the 21-byte data string in the prepared store	ENTER 715; Z$	
Display the contents of the store	DISP Z$	

Check that the display reads CK+000010.00000E+06 with the cursor moved to the next line, indicating that carriage return (CR) and line feed (LF) have been accepted.

SRQ and Status Byte Check

29 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true	REMOTE 7	
Set the instrument to send the SRQ message when an error is detected, and force the generation of error code 05 by sending the device-dependent commmand XXX	OUTPUT 715;"IPXXX"	
Store the status of the GPIB interface of the controller, in binary form, as variable T	STATUS 7, 2; T	
Display the status of the SRQ line	DISP"SRQ=";BIT(T,5)	

Check that the HP-85 displays SRQ=1, the SRQ status bit is at logic '1' or the SRQ line is < 0.8 V). Check that the SRQ indicator on the instrument is lit.

30 Test as follows:

Action	HP-85 Code	Your Controller
Conduct a serial poll and store the status byte as variable R	R = SPOLL (715)	
Display variable R	DISP "R="; R	

Check that the SRQ indicator is turned off when the serial poll is made. The value of R should be 101 (in binary form, R should be 0000000001100101). If using an HP-85 controller, check that the ADDR indicator is turned off.

Device Clear and Selected Device Clear Check

31 Test as follows:

Action	HP-85 Code	Your Controller
Set the instrument to the Total A by B mode by sending the listen address, followed by the device-dependent command TA	OUTPUT 715;"TA"	
Send the DCL message true	CLEAR 7	

Check that the function indicated on the instrument front panel changes to FREQ A.

32 Test as follows:

Action	HP-85 Code	Your Controller
Reset the instrument to the Total A by B mode by sending the listen address, followed by the device-dependent command TA	OUTPUT 715;"TA"	
Send the SDC message true	CLEAR 715	

Check that the function indicated on the instrument front panel changes to FREQ A.

IFC Check

33 Test as follows:

Action	HP-85 Code	Your Controller
Send the ATN message false Send the IFC message true	RESUME 7 ABORTIO 7	

Check that the ADDR indicator is turned off.

TALK ONLY Selector Test

34 (1) Set the TALK ONLY switch in the instrument rear panel to '1'. Check that the REMOTE indicator is turned off and the ADDR indicator lights.

(2) Set the TALK ONLY switch to '0'. Check that the ADDR indicator turned is off.

OPTION FITTING INSTRUCTIONS

Single-Instrument Fixed Rack Mounting Kit 11-1648 (Option 60A)

35 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	1	16-0643
Long mounting bracket	1	16-0644
Screw, M4 x 16	4	24-7733
Crinkle washer M4	4	24-2802
Spacer, plain M4x5	4	24-4112
Screw, M6 x 16	4	24-7995
Cup washer, M6	4	24-2809
Caged nut, M6	4	24-2240

36 Assemble the kit to the instrument as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the bottom cover by sliding it towards the rear of the instrument.

(4) Remove the instrument's feet from the bottom cover.

(5) Replace the bottom cover. Replace and secure the bezel.

(6) Remove the four blind grommets from the sides of the instrument. This will reveal two threaded holes in each side frame.

(7) At one side of the instrument, secure a mounting bracket to the side frame, using two spacers, M4 screws and crinkle washers. Position the spacers between the mounting bracket and the side frame.

(8) Repeat step (7) at the other side of the instrument.

(9) Fit the cup washers to the M6 screws. Offer the instrument up to the rack in the required position, and secure the brackets to the rack using the M6 screws and nuts.

Double-Instrument Fixed Rack Mounting Kit 11-1649 (Option 60B)

37 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	2	16-0643
Screw, M4 x 16	4	24-7733
Crinkle washer, M4	4	24-2802
Spacer, plain, M4 x 5	4	24-4112
Spacer, female	2	14-1583
Spacer, male	2	14-1584
Mating plate	1	13-2000
Rivet, plastic	4	24-3211
Screw, M6 x 16	4	24-7995
Cup washer, M6	4	24-2809
Caged nut, M6	4	24-2240

38 Prepare both instruments as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the bottom cover by sliding it towards the rear of the instrument.

(4) Remove the instrument's feet from the bottom cover.

(5) Replace the bottom cover. Replace and secure the bezel.

(6) Remove the four blind grommets from the sides of the instrument. This will reveal two threaded holes in each side frame.

(7) Remove two buffers from the bezel at the side which is to be at the centre of the rack.

39 Assemble the kit to the instruments as follows:

(1) At the sides which are to be at the centre of the rack, secure the female spacers to one instrument and the male spacers to the other. The spacers screw into the threaded holes in the side frames.

(2) At the other side of each instrument, secure a mounting bracket to the side frame, using two plain spacers, M4 screws and crinkle washers. Position the spacers between the mounting bracket and the side frame.

(3) Fit the male spacers on one instrument into the female spacers on the other.

(4) Position the mating plate to bridge the gap between the bezels. Secure it by pushing the plastic rivets through the plate into the buffer holes.

(5) Fit the cup washers to the M6 screws. Offer the two instruments up to the rack in the required position, and secure the brackets to the rack using the M6 screws and nuts.

TCXO Frequency Standard, 11-1713 (Option 04T)

40 The kit comprises:

Item	Qty	Racal-Dana Part Number
Plate assembly	1	11-1610
Oscillator PCB	1	19-1208
Crinkle washer M3	3	24-2801
Screw, M3 x 6	3	24-7721

Installation

41 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) If an ovened frequency standard is fitted, remove this. If the basic frequency standard is in use, remove link LK1 and the frequency controls blanking plate from the rear panel.

(5) Secure the PCB to the plate assembly, using an M3 screw and washer from the kit. The screw should be passed through the mounting hole in the board and screwed into the threaded spacer of the plate assembly. The component side of the board should be towards the plate assembly.

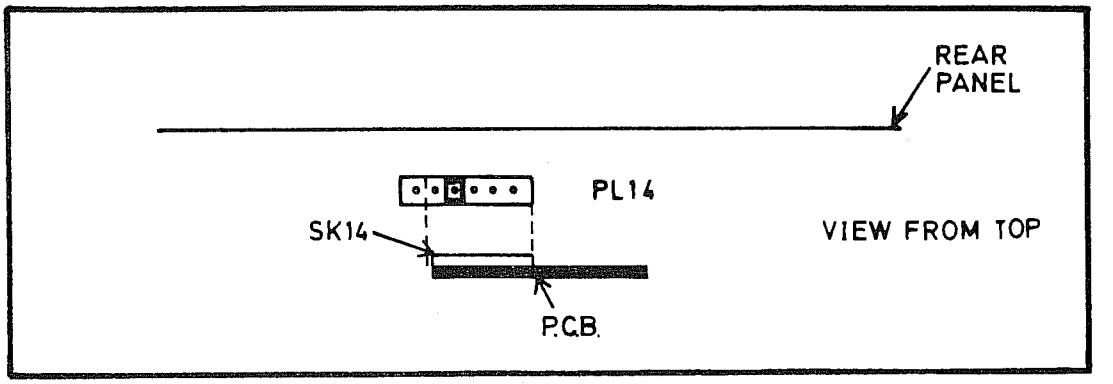


Fig 3.1 PCB to Motherboard Connection

(6) Connect the PCB to the motherboard at PL14, ensuring that the socket fits over the portion of PL14 indicated in Fig 3.1.

(7) Secure the plate assembly to the rear panel, using two M3 screws and washers. The screws pass through the holes adjacent to the FREQ STD ADJUST aperture and screw into the plate assembly.

(8) Replace the top cover. Replace and secure the bezel.

Removal

42 (1) Remove the two screws adjacent to the FREQ STD ADJUST aperture in the rear panel.

(2) Pull the PCB and plate assembly upwards until the board is disconnected from the motherboard.

Ovened Frequency Standards 11-1710 and 11-1711 (Options 04A and 04B)

43 The kit comprises:

Item	Qty	Racal-Dana Part Number
Oscillator assembly	1	9444 for 11-1710 9423 for 11-1711
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

Installation

44 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) If an ovened frequency standard is fitted, remove this as in para. 41. If the basic frequency standard is in use, remove link LK1 and the frequency controls blanking plate from the rear panel.

(5) Connect the frequency standard into the motherboard at PL14, ensuring that the socket fits over the portion of PL14 indicated (see illustration in para. 41).

(6) Secure the oscillator assembly to the rear panel of the instrument, using the M3 screws and washers. The screws pass through the holes adjacent to the FREQ STD ADJUST aperture and screw into the oscillator assembly.

(7) Replace the top cover. Replace and secure the bezel.

NOTE: When either of the ovened frequency standard options is fitted, the ref. input and output option should also be fitted.

Removal

45 (1) Remove the two screws adjacent to the FREQ STD ADJUST aperture in the rear panel.

(2) Lift the oscillator assembly out of the chassis and disconnect the flying lead from the motherboard at PL14.

Reference Frequency Multiplier Option 11-1645 (Option 10)

46 The kit comprises:

Item	Qty	Racal-Dana Part Number
Frequency multiplier	1	19-1164
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

47 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the frequency standard, if it is an ovened type.

(5) Remove the shorting link from between pins 8 and 9 on PL16.

NOTE: This link should be stored in a safe place. It must be replaced if Option 10 is removed from the instrument.

(6) Connect the frequency multiplier PCB to the motherboard at PL16 and PL17, with the threaded spacers towards the right-hand side frame.

(7) Secure the PCB to the side frame, using the M3 screws and washers.

(8) Replace and secure the frequency standard if it was removed in (5).

(9) Replace the top cover. Replace and secure the bezel.

NOTE: Where this option is fitted, the ref. input and output option must also be fitted.

Reference Input/Output Option 11-9000 (Option 02)

48 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws securing the board to the rear panel, and remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument. If the temperature compensated crystal oscillator (TCXO) is fitted, remove the screws holding this to the rear panel.

(4) Remove the four screws securing the rear panel to the side members and ease the rear panel back from the chassis. Take care not to strain the connecting wires.

(5) Remove the two plastic plugs covering the EXT STD INPUT and 10 MHz STD OUTPUT connector holes.

(6) Remove the nuts from the BNC connectors. Pass the connectors through the rear panel and secure the BNCs with the nuts on the outside.

(7) Replace the rear panel, taking care to align the connectors PL20/SK20. Note that the connectors PL19/SK19 are staggered when fitted correctly, see Fig 3.2:

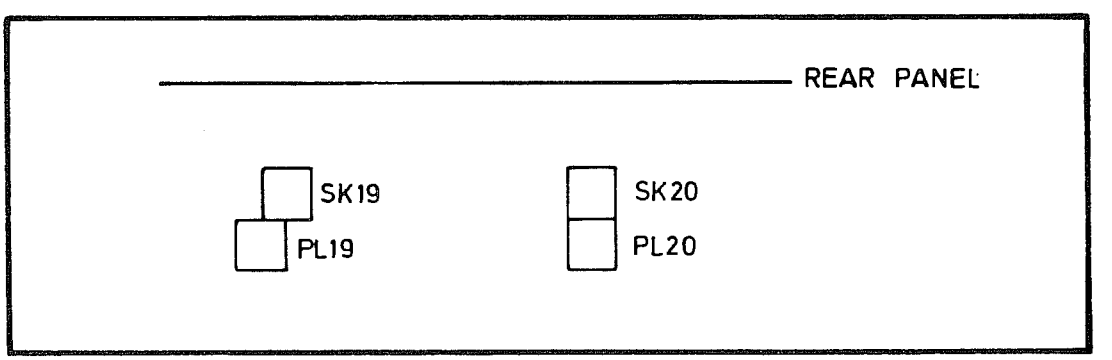


Fig 3.2 Connector Alignment

(8) Replace the screws holding the rear panel.

(9) Replace the top cover. Replace and secure the bezel.

GPIB Option 11-9001 (Option 55)

49 The kit comprises:

Item	Qty	Racal-Dana Part Number
GPIB board assembly	1	19-1146
Bracket	2	11-1728
Speednut	2	24-0146
Shakeproof washer, M3	2	24-2813
Screw, M3 x 6	2	24-7721
Washer, M4	2	24-2802
Screw, M3 x 6	2	24-7721
Screw, M4 x 8	4	24-7730

NOTE:
This option cannot be fitted to an instrument already fitted with the battery pack option.

50 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the blanking plate from the rear panel by pushing out the plastic rivets from the inside of the instrument.

(5) Slide a speednut onto each of the two brackets. Ensure that the flat non-threaded face of the speednut is uppermost.

(6) Secure one bracket to each sideframe of the instrument using the M4 screws and crinkle washers supplied. Ignore the two holes near the rear of the instrument in the RH sideframe.

(7) Hold the GPIB board, component side down, with the GPIB connector towards the rear panel. Connect the ribbon-cable to the motherboard at SK4.

(8) Tilt the GPIB board, and lower it into the instrument, easing the GPIB connector into the shaped cut-out in the rear panel of the instrument.

(9) Line-up the holes in the GPIB board with the speednuts (move the speednuts slightly if necessary). Secure the board with the two self-tapping screws.

(10) Secure the bracket which carries the GPIB connector to the rear panel, using the two M3 screws and shakeproof washers.

NOTE:
The screws and washers provide the ground connection between the GPIB connector and the instrument chassis. Tighten the screws firmly to ensure that a good connection is obtained.

(11) Replace the top cover. Replace and secure the bezel.

Battery Pack Option 11-1625 (Option 07)

51 The kit comprises:

Item	Qty	Racal-Dana Part Number
PCB assembly	1	11-1722
Mounting bracket	1	11-1599
Battery pack	1	11-1723
Cover plate	1	13-2040
Crinkle washers, M3	2	24-2801
Screws, M3	2	24-7721
Crinkle washers, M4	6	24-2802
Plain washers, M4	2	24-2705
Screws, M4	6	24-7730
Spare fuse, 3AT	1	23-0069
Plastic rivet	1	24-0252

NOTE:
This option cannot be fitted to an instrument already fitted with the GPIB interface option without first removing that option.

52 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the blanking plate from the rear panel by pushing out the plastic rivets from the inside of the instrument.

(5) If a PCB-mounted frequency standard is fitted, remove the two screws adjacent to the FREQ STD ADJUST aperture.

(6) Remove the four screws which secure the rear panel to the side frames.

(7) Ease the rear panel away from the instrument until it disconnects from the motherboard at PL19 and PL20.

(8) Hold the PCB assembly with the switches towards the rear of the instrument and the PCB connector pointing downwards.

(9) Lower the assembly into the chassis and connect the PCB to the motherboard at PL21, taking care that it mates correctly.

(10) Replace and secure the rear panel.

(11) If a PCB-mounted frequency standard is fitted, secure it to the rear panel with the screws removed in (5).

(12) Position the cover plate over the switches protruding through the rear panel. Secure the cover plate and the rear panel to the PCB assembly, using the M3 screws and washers.

(13) Secure the mounting bracket to the right-hand side frame, using two M4 screws and washers. The horizontal flange should be towards the top of the instrument.

(14) Position the battery pack within the chassis, with the supporting lugs resting on the mounting bracket. Secure the battery pack to the left-hand side frame, using two M4 screws and washers.

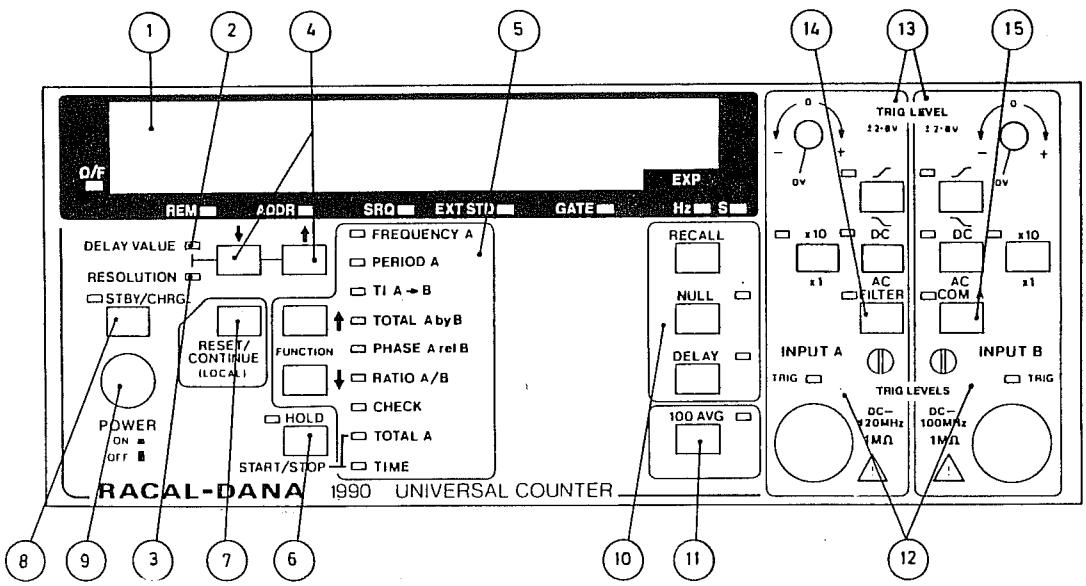
(15) Secure the supporting lugs to the mounting bracket, using M4 screws and washers.

(16) Connect the flying lead on the battery pack to the connector on the PCB assembly.

(17) Replace the top cover. Replace and secure the bezel.

INTRODUCTION

1 The instrument should be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the AC voltage selector.



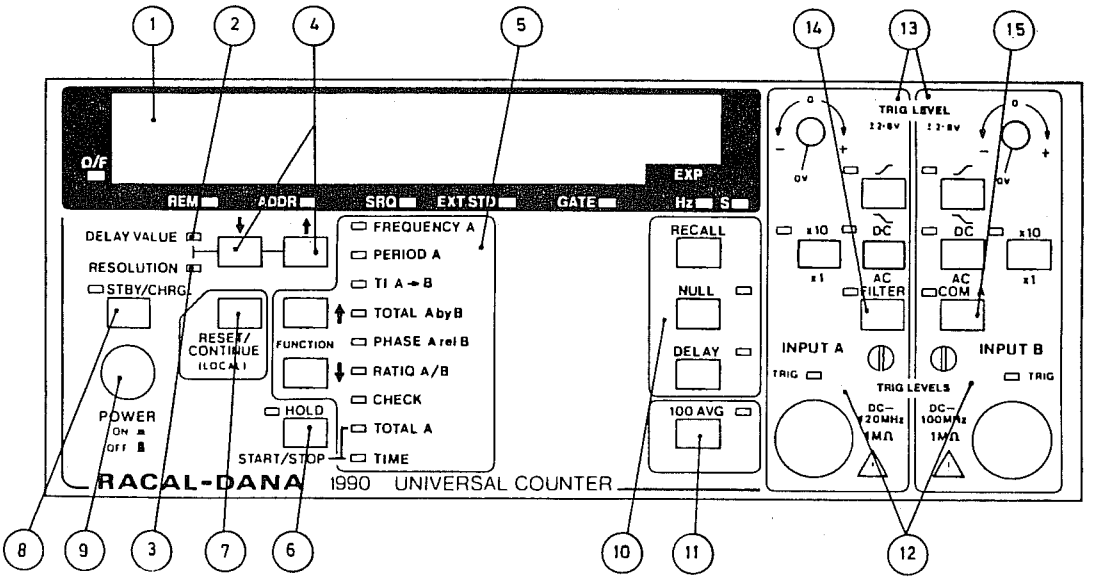
DESCRIPTION OF CONTROLS, INDICATORS AND CONNECTORS

Front Panel Items

2

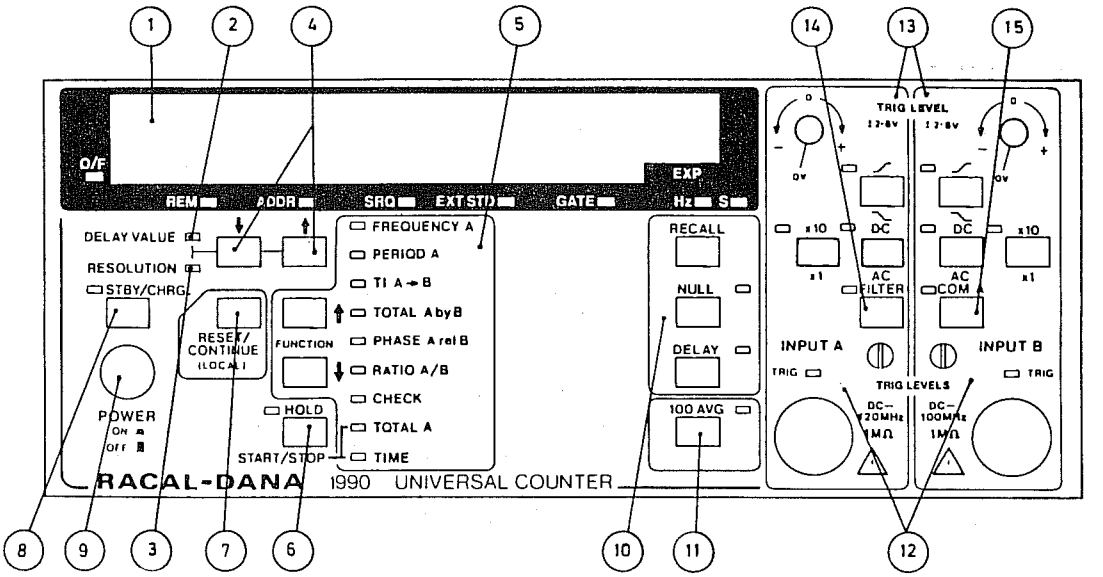
Reference	Item	Description
1	Display	A 7-segment, LED, digital display, used to display: (1) The result of a measurement. (2) A number awaiting entry into an internal store. (3) A number recalled from an internal store. (4) Error indications.

Reference	Item	Description
		The display format is in engineering format, with an 8-digit mantissa and a 1-digit exponent. The exponent is normally a multiple of three. The exponent digit is blanked, and should be assumed to be zero, for: (1) Display of phase mode measurement results. (2) Totalize measurement results having less than nine digits.
	O/F Indicator	Lights when the measurement result has overflowed the eighth digit of the display.
	REM Indicator	Lights when the instrument is operating under remote control.
	ADDR Indicator	Lights when the instrument is acting as a listener or as a talker.
	SRQ Indicator	Lights when the instrument generates a service request.
	EXT STD Indicator	Lights when the instrument is operating from an external frequency standard.
	GATE Indicator	Lights while a measurement cycle is in progress.
	Display Units Indicators	The Hz indicator lights for a frequency display. The S indicator lights for a time display. Neither indicator lights for a display of phase angle, ratio, total, or a number.
2	DELAY VALUE Control Indicator	Lights when a delay value is being displayed. The displayed delay value can be stepped up or down using the ↑ and ↓ keys.



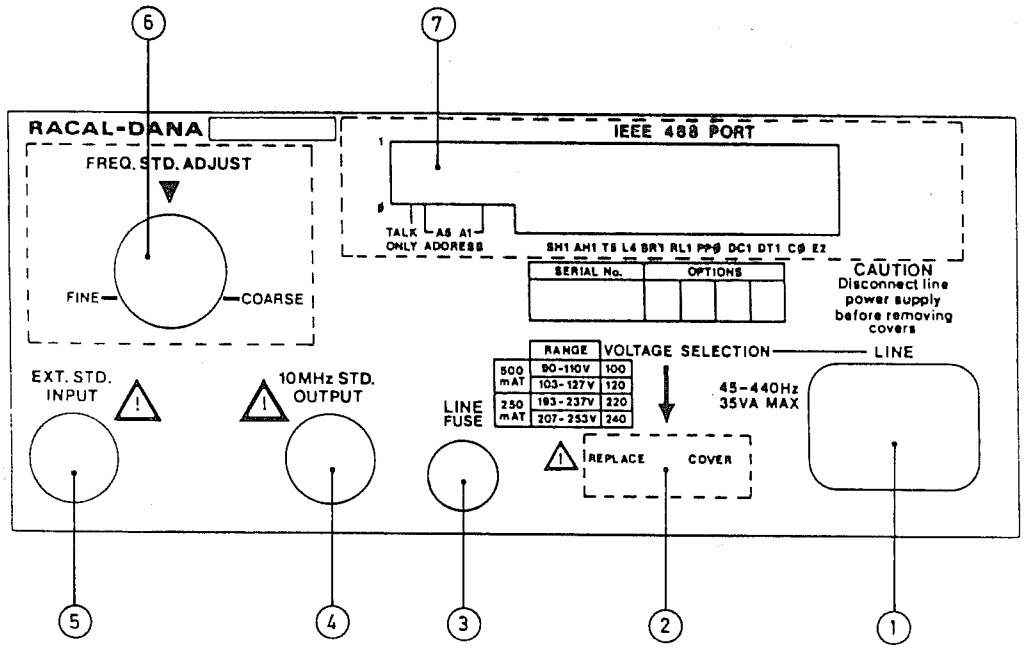
Reference	Item	Description
3	RESOLUTION Control Indicator	Lights to show that the resolution of the display, and, therefore, the measurement period (gate time) can be changed by means of the ↑ or ↓ control keys.
4	Step-Up ↑ and Step-Down ↓ Keys	Used to step the display resolution or the displayed delay value up or down.
5	Function Selector	The functions can be selected in turn using the FUNCTION ↑ and ↓ keys. The function selection 'wraps round' at both ends.
6	HOLD (Start/Stop) Key	Successive operations select or de-select the Hold (single-shot measurement) mode. The indicator lights when the instrument is in the Hold mode. Readings are triggered using the RESET key. When the instrument is in the Total A or Time modes, successive operations of the key start and stop the measurement cycle.

Reference	Item	Description
7	RESET/CONTINUE (LOCAL) Key	This key has three functions. RESET Clears the display and triggers a new measurement cycle when the instrument is in the measurement mode. CONTINUE Returns the instrument to the measurement mode and triggers a measurement cycle, following the display of a number recalled from store. LOCAL Returns the instrument to local control from remote GPIB control provided local lockout is not set.
8	STBY/CHRG Key	Successive operations switch the instrument into and out of the standby state. The indicator lights when the instrument is in the standby state. If the battery pack option is installed the indicator flashes when the battery approaches the discharged state. The battery is charged at the full rate when the instrument is in standby and external power is applied.
9	POWER Switch	Controls the AC or DC power to the instrument.
10	RECALL Key	Used in conjunction with NULL, DELAY and RESET keys. RECALL NULL displays the value in the Null store. RECALL DELAY displays the delay value and lights the DELAY VALUE indicator. The delay value can be changed using the Delay value ↑ and ↓ keys. RECALL RESET displays the GPIB address when this option is fitted.



Reference	Item	Description
	NULL Key and indicator	Key enables and disables the NULL function. At the time that the NULL function is enabled, the currently-displayed value is stored in the Null register. The indicator lights when NULL is selected.
	DELAY Key and indicator	Key enables and disables the DELAY function. The delay used is that currently in the delay value store. The indicator lights when DELAY is selected.
11	100 AVG Key and indicator	Key enables and disables the 100 AVG function. The indicator lights when 100 AVG is selected.
12	Measurement Channel Controls	The A and B channels have almost identical controls.
	TRIG LEVEL Controls	Used to set the trigger level, which can be continuously adjusted over the range -2.8 V to +2.8 V min. A switched 0 V position is also available, giving maximum sensitivity for frequency measurements.

Reference	Item	Description
	TRIG LEVEL Outputs	The trigger levels in use on the A and B channels are available at two terminals. The voltage range is typically ± 2.8 V , regardless of whether or not the X10 attenuator is selected.
	AC/DC Key	Used to select AC or DC coupling of the input signal. The indicator lights when DC coupling is selected.
	Trigger Slope Key	Used to select the positive-going, ⎍ or negative-going, ⎍ , edge of the input waveform for triggering. The indicator lights when the positive-going edge is selected.
	X10/X1 Key	Used to select attenuation of the input signal. With X10 selected the input is attenuated by a factor of 10. The indicator lights when X10 is selected.
13	TRIG Indicators	Channels A and B are provided with trigger indicators. (1) Indicator permanently lit. Trigger level too low or signal input held in high state. (2) Indicator flashing. Channel being triggered. (3) Indicator permanently off. Trigger level too high or signal input held in low state.
14	FILTER Key	Successive operations enable and disable the channel A input filter. The indicator lights when the filter is enabled.
15	COM A Key	Used to connect the channel A input to channels A and B in parallel (common configuration). The indicator lights when the common configuration is selected.
	Input Connectors	All inputs are BNC connectors.

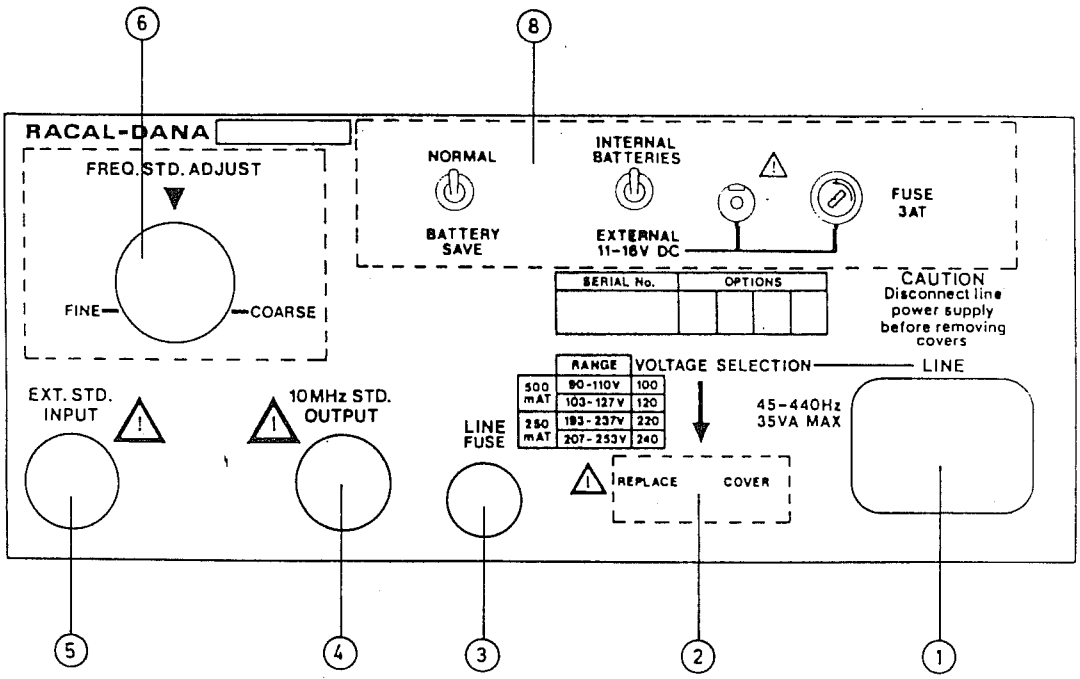


Rear Panel Items

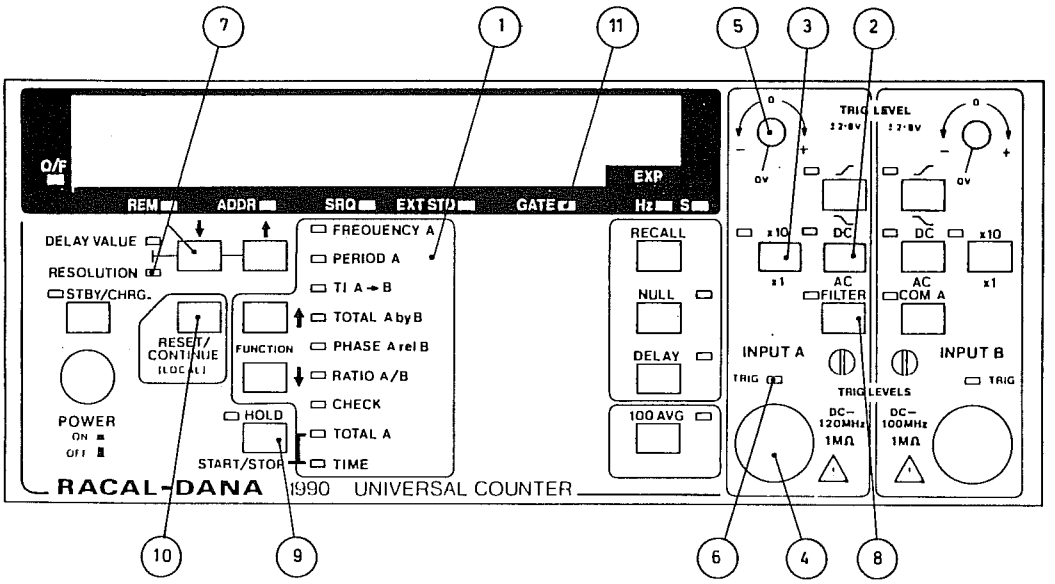
3

Reference	Item	Description
1	AC Power Input Plug	A standard connector for the AC power supply. An RFI filter is incorporated.
2	Line Voltage Selector	Voltage selection is changed by externally repositioning a printed circuit board. The voltage selected can be seen through a window in its retaining clamp.
3	Line Fuse	A $\frac{1}{4}$ in x $1\frac{1}{4}$ in, anti-surge, glass cartridge fuse. The required fuse ratings for different line voltage ranges are shown on the panel and in Section 3 of this manual.
4	10 MHz STD OUTPUT option 02 only	A BNC connector, providing a 10MHz output signal locked to the frequency standard in use.

Reference	Item	Description
5	EXT STD INPUT option 02 only	A BNC connector for connecting an external frequency standard. The instrument will operate from the external frequency standard whenever a signal of suitable frequency and amplitude is applied. The frequency required is 10 MHz unless the reference frequency multiplier option is fitted. With this option, frequencies of 1 MHz, 2 MHz, 5 MHz and 10 MHz are acceptable.
6	FREQ. STD. ADJUST	This aperture provides access to allow adjustment of the optional internal frequency standards.
7	GPIB Option	
	GPIB Address Switches	Switches A1 to A5 define the listen and talk addresses for GPIB operation in the addressed mode. The talk-only switch must be in the 'Ø' position. With the talk-only switch in the '1' position the instrument is set to the talk-only condition. The positions of switches A1 to A5 are then irrelevant.
	GPIB Connector	An IEEE-488-1978 standard connector used to connect the instrument to the GPIB. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an accessory.



Reference	Item	Description
8	Battery-Pack Option	
	DC Power Input Plug	Permits the instrument power to be derived from an external DC supply.
	Battery NORMAL/SAVE Switch	Used to select the Battery-Save facility.
	INTERNAL/EXTERNAL DC Supply Switch	Used to select operation from the internal battery or an external DC supply
	DC Supply Fuse	A $\frac{1}{4}$ in x $1\frac{1}{4}$ in glass cartridge fuse of the anti-surge type. The required rating is 3 AT.



FREQUENCY MEASUREMENT

4 (1) Switch the power on.

(2) Select the FREQ A measurement mode, using the function selector ① .

(3) Set the AC/DC coupling ② and attenuator ③ as required.

(4) Connect the signal to be measured to the channel A input ④ .

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Set the manual trigger level to the required value ⑤. Check that the channel A TRIG indicator ⑥ flashes.

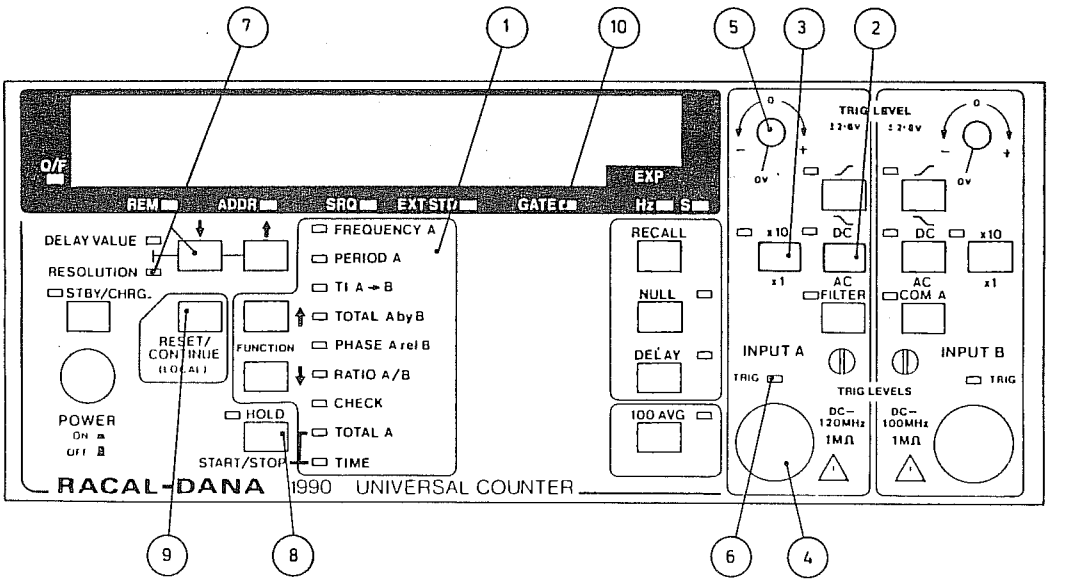
NOTE: Put the trigger control ⑤ to 0 V for maximum sensitivity. Any other position sets a trigger level between ±2.8 V.

(6) Select the required display resolution ⑦ .

(7) If a frequency below 50 kHz is to be measured in the presence of noise, enable the filter ⑧ .

(8) If operation in the hold mode is required, select HOLD ⑨ and press the RESET key ⑩ .

(9) Check that the GATE indicator ⑪ flashes on during the measurement period.



PERIOD MEASUREMENT

5 (1) Switch the power on.

(2) Select the PERIOD A measurement mode, using the function selector ① .

(3) Set the AC/DC coupling ② and attenuator ③ for channel A, as required.

(4) Connect the signal to be measured to the channel A input ④ .

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

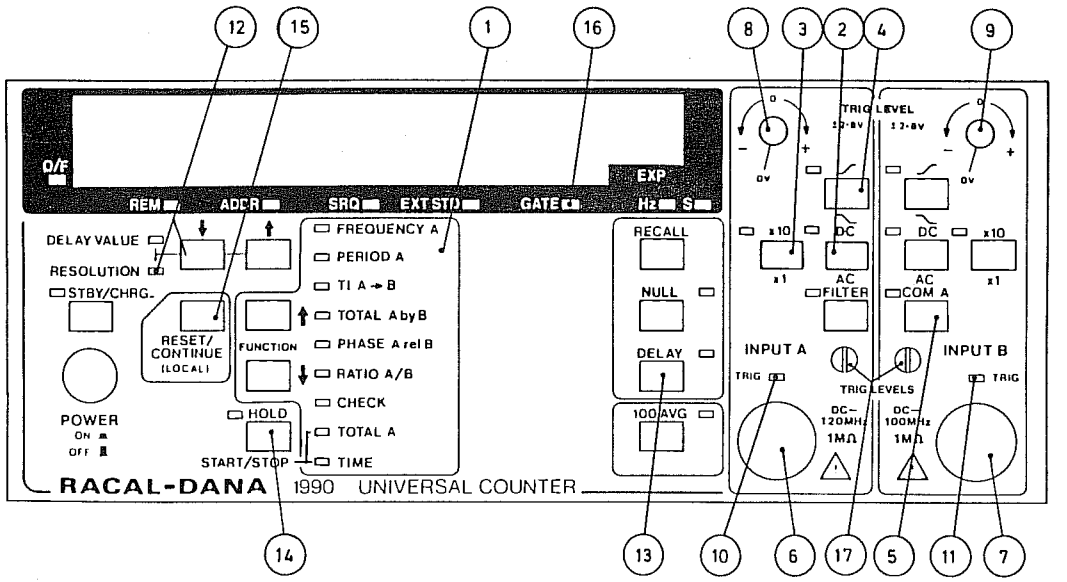
(5) Set the manual trigger level to the required value ⑤ . Check that the channel A TRIG indicator ⑥ flashes.

NOTE: Put the trigger control ⑤ to 0 V for maximum sensitivity. Any other position sets a trigger level between ±2.8 V.

(6) Select the required display resolution ⑦ .

(7) If hold mode operation is required, select HOLD ⑧ and press the RESET key ⑨ .

(8) Check that the GATE indicator ⑩ flashes on during the measurement period.



TIME INTERVAL MEASUREMENT

6 (1) Switch the power on.

(2) Select the T.I. A → B measurement mode, using the function selector (1) .

(3) Set the AC/DC coupling (2) , attenuator (3) , and slope (4) , as required. If the start and stop signals are from the same source, select COM A (5) .

(4) Connect the start signal to the channel A input (6) . If a separate stop-signal source is used, connect the stop signal to the channel B input (7) and set the associated input controls.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNALS DO NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Set the manual trigger levels to the required values (8) (9). Check that the TRIG indicators (10) (11) flash.

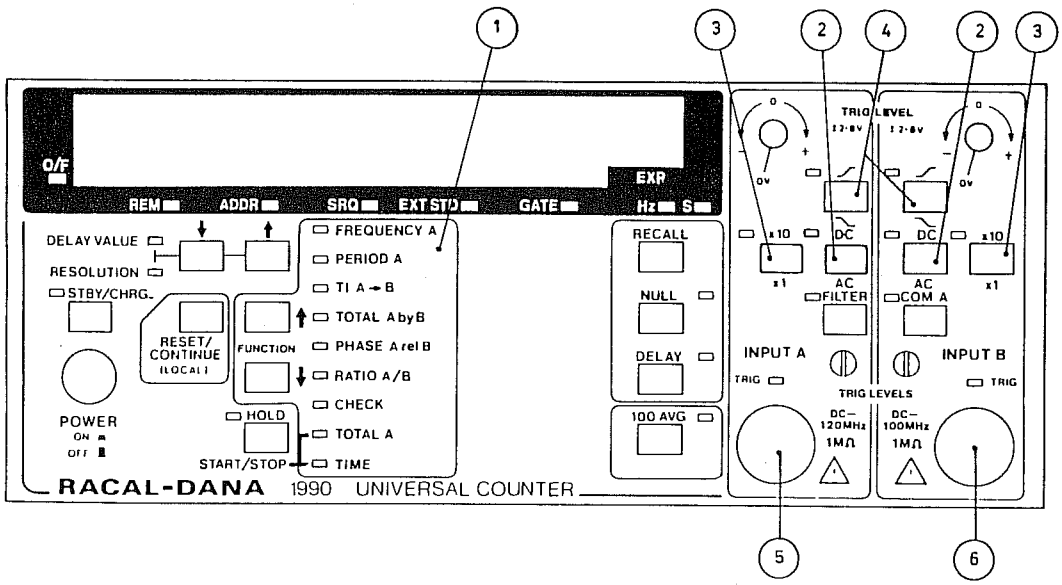
NOTE: If required, monitor the trigger output terminals (17) and set the trigger to a specific voltage level.

(6) Select the required display resolution (12) .

(7) If a delay to the stop circuit is required, set the required delay value and enable the delay (13) .

(8) If hold mode operation is required, select HOLD (14) and press the RESET key (15) .

(9) Check that the GATE indicator (16) flashes on during the measurment period.



TOTALIZE MEASUREMENT

Total A by B (Electrical)

7 A procedure for Total A (Manual) totalize is given in para. 8.

(1) Switch the power on.

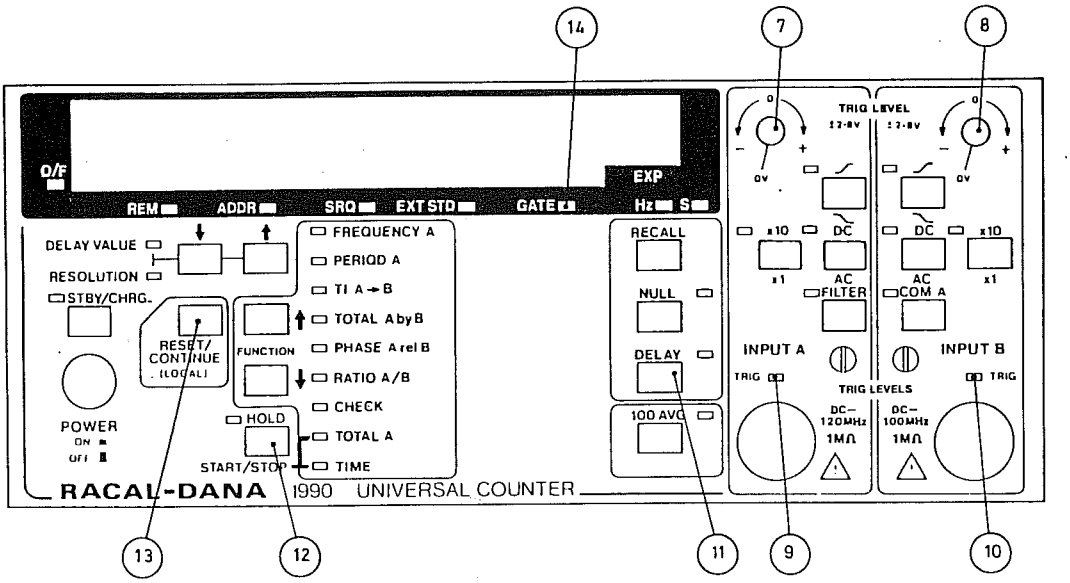
(2) Select the TOTAL A by B measurement mode using the function selector (1) .

(3) Set the AC/DC coupling (2) , attenuator (3) and slope (4) as required for both channels.

NOTE:
The channel A slope switch selects the slope of the events which are counted. The measurement period starts on the slope of the B channel signal selected by the channel B slope switch, and stops on the opposite slope.

(4) Connect the signal to be totalized to the channel A input (5) and the control signal to the channel B (6) input.

CAUTION: SIGNAL LEVELS
ENSURE THAT THE SIGNAL LEVELS DO NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

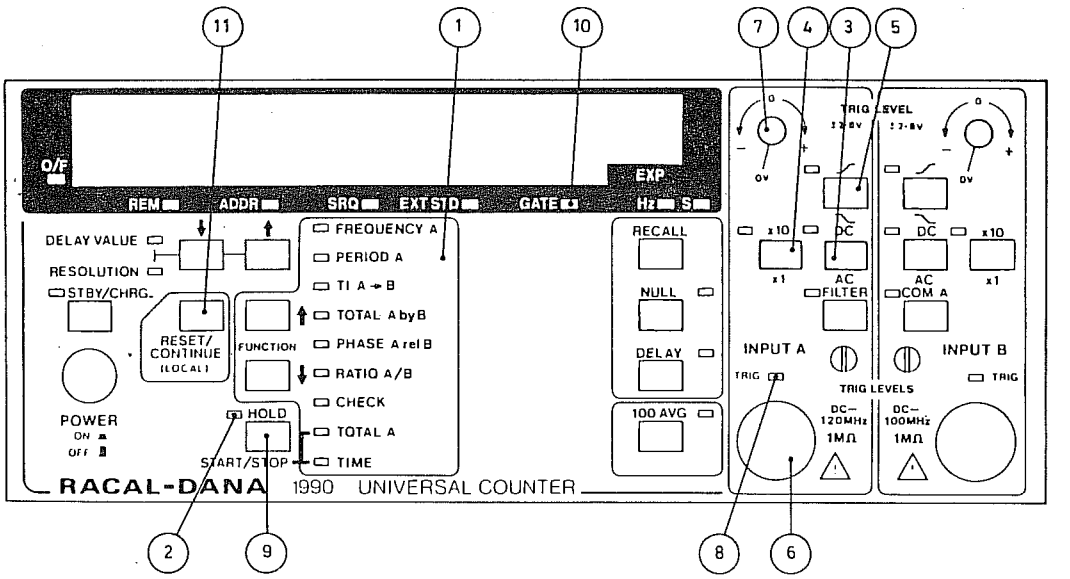


(5) Set the manual trigger levels to the required values (7) (8) Check that the TRIG indicators (9) (10) flash.

(6) If a delay to the stop circuit is to be used, set the required delay value and enable the delay (11).

(7) If hold mode operation is required, select HOLD (12) and RESET (13).

(8) Check that the GATE indicator (14) flashes on during the measurement period.



Total A (Manual)

8 (1) Switch the power on.

(2) Select the TOTAL A measurement mode, using the function selector (1) . The HOLD indicator (2) will light.

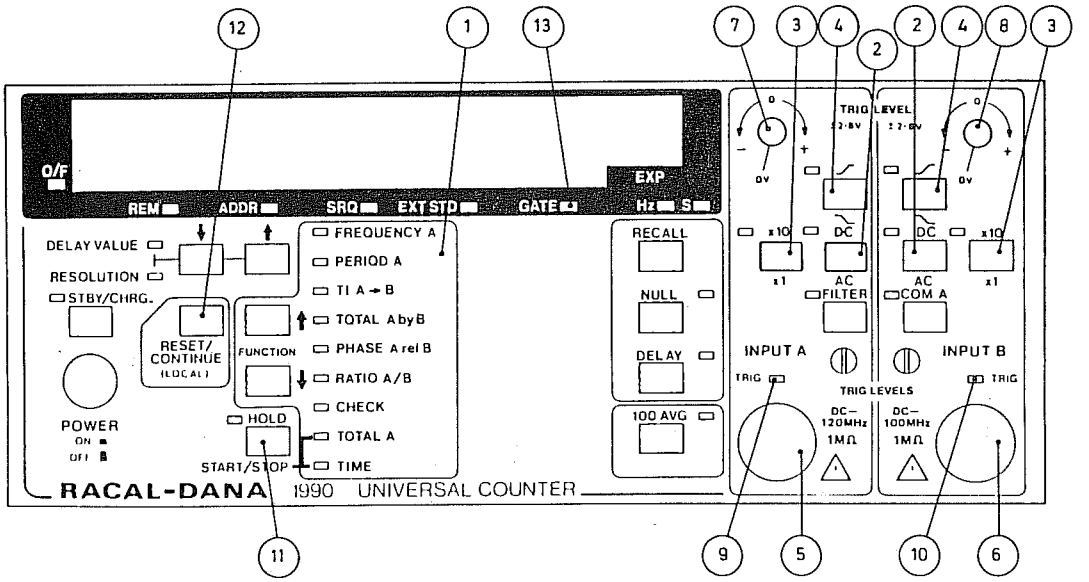
(3) Set the AC/DC coupling (3) , attenuator (4) and slope (5) of channel A as required.

(4) Connect the signal to be totalized to the channel A input (6).

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Set the manual trigger level (7) to the required value. Check that the TRIG indicator (8) flashes.

(6) Start and stop a measurement using the HOLD key (9) . The HOLD indicator (2) will be turned off and the GATE indicator (10) will light during the measurement period. The displayed result is cumulative over successive measurement cycles. If required, clear the display after a measurement cycle by pressing the RESET key (11) .



PHASE MEASUREMENT

9 (1) Switch the power on.

(2) Select the PHASE A rel B measurement mode, using the function selector (1) .

(3) Set the AC/DC coupling (2) , attenuator (3) and slope (4) as required.

(4) Connect the signals to be compared to the channel A (5) and B (6) inputs (the larger and cleaner signal to channel A for maximum accuracy).

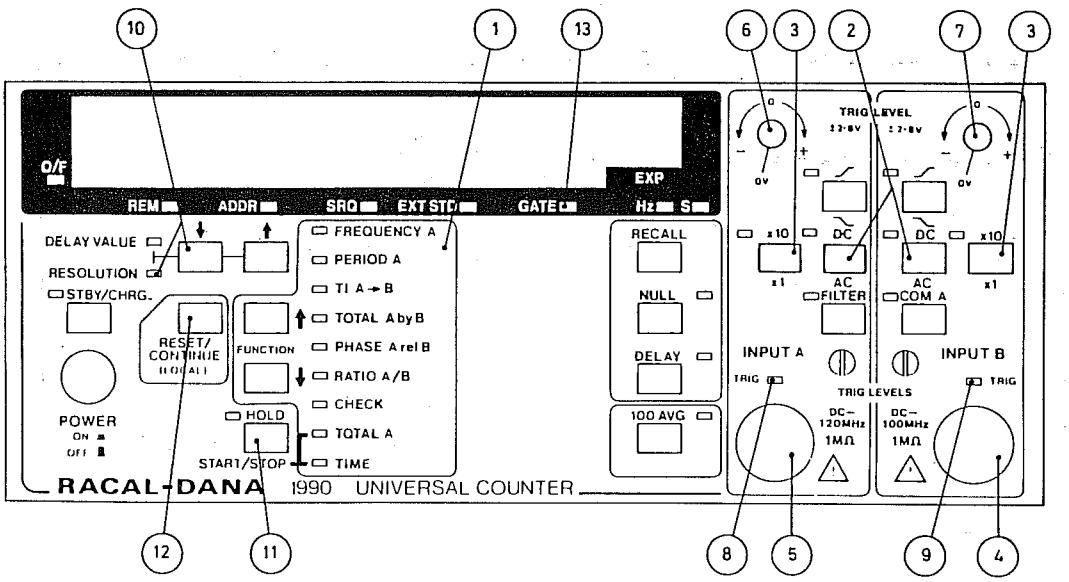
CAUTION SIGNAL LEVELS
ENSURE THAT THE INPUT SIGNALS DO NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Set the manual trigger levels to the required values (7)(8) . Check that the TRIG indicators (9) (10) flash.

(6) If hold mode operation is required, select HOLD (11) and press the RESET key (12) .

(7) Check that the GATE indicator (13) flashes on during the measurement cycle.

NOTE:
The phase measurement is always positive, and is the angle by which the signal applied to channel A leads that applied to channel B.



RATIO MEASUREMENT

10 (1) Switch the power on.

(2) Select the RATIO A/B measurement mode, using the function selector (1) .

(3) Set the AC/DC coupling (2) and attenuator (3) as required.

(4) Connect one of the signals to channel B (4) and the other to channel A (5) . The lower frequency signal should be connected to channel B.

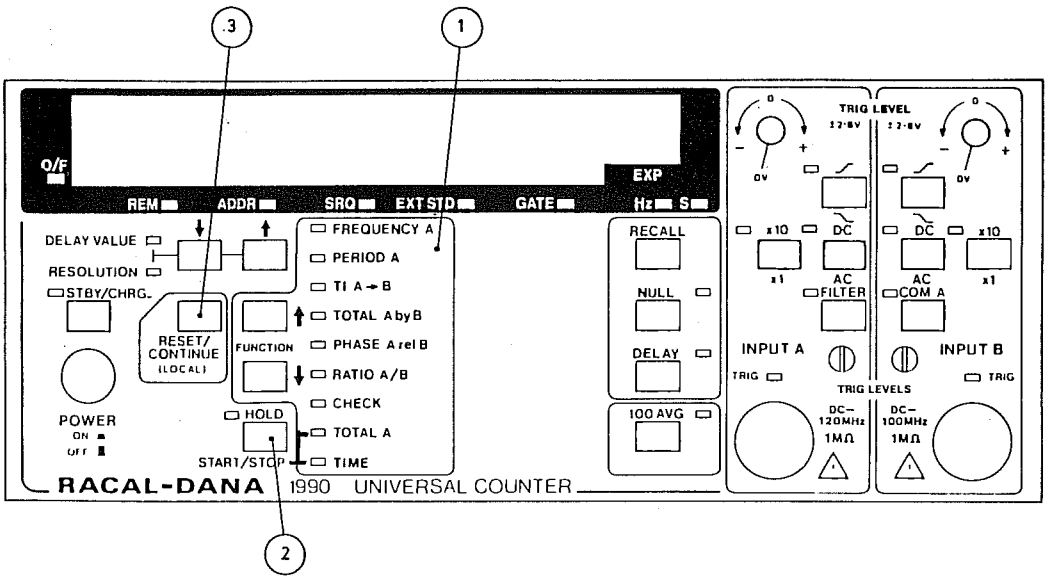
CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNALS DO NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Set the manual trigger levels to the required values (6) (7) . Check that the TRIG indicators (8) (9) flash.

(6) Select the required display resolution (10) .

(7) If hold mode operation is required, select HOLD (11) and press the RESET key (12) .

(8) Check that the GATE indicator (13) flashes on during the measurement period.



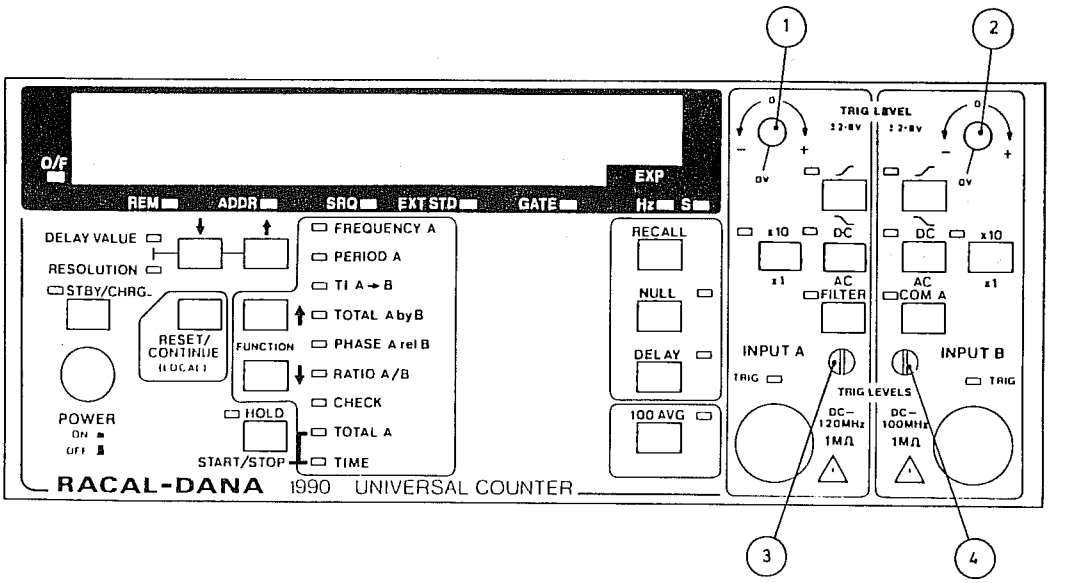
TIME MEASUREMENT

11 (1) Switch the power on.

(2) Select the TIME measurement mode using the function selector (1) .

(3) Start and stop the time measurement using the HOLD (start/stop) key (2) .

12 The HOLD indicator is turned off and the GATE indicator lit during the measurement period. The displayed result is cumulative over successive measurement cycles. If required, the display can be cleared, after a measurement cycle, by pressing RESET (3) .

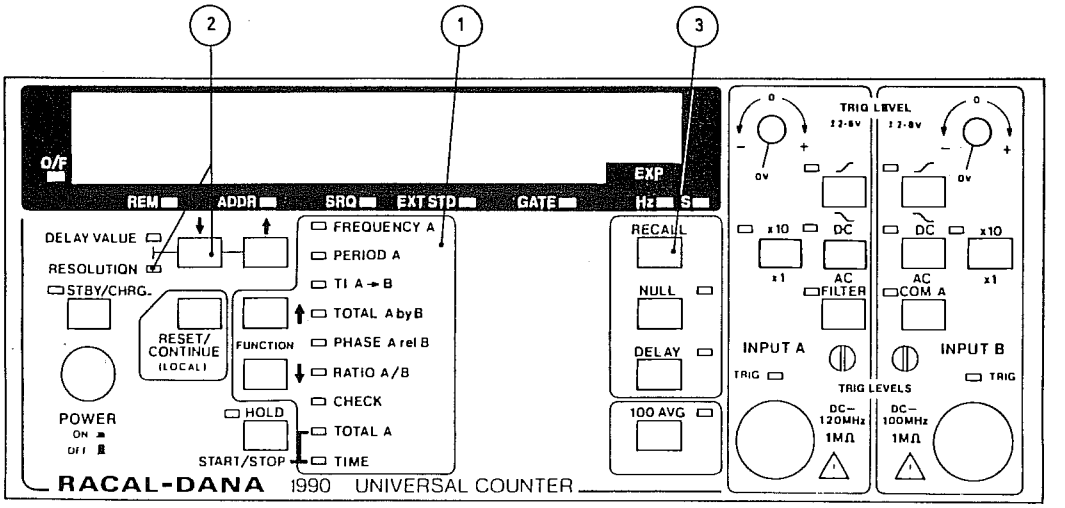


SETTING AND MEASURING THE TRIGGER LEVEL

13 (1) The trigger level is set using the rotary controls for channel A (1) and channel B (2) . Each control can be set independently for positive or negative levels typically between +2.8 V and -2.8 V with centre 0 V. Rotating the control clockwise gives a positive trigger level and anti-clockwise gives a negative trigger level.

(2) For maximum sensitivity on small signals a switched 0 V position is available by turning the appropriate control (1) or (2) fully anti-clockwise until the control clicks.

(3) The trigger voltage set can be measured at the output terminals (3) (4) , using a DVM, oscilloscope or other high input impedance instrument.



INSTRUMENT CHECKS

14 (1) Switch power on.

(2) Select the CHECK mode, using the function selector (1) . Check that 10 MHz is displayed. Resolution can be changed using the RESOLUTION key (2) .

(3) To check the front panel LEDs press RECALL (3) . All LEDs, with the exception of REM, ADDR, SRQ, GATE, TRIG A, TRIG B and STBY/CHRG, will flash on and off every two seconds. If the GPIB option is fitted, the REM, ADDR and SRQ will flash in time with the other LEDs.

DISPLAY RESOLUTION

15 For all measurement functions other than TOTAL A by B, TOTAL A and PHASE A rel B, the resolution refers to the number of zeros displayed when no signal is applied at the input. The resolution can be set to display 3 to 8 digits. A 10% overrange of the display is permitted without a change of range. Because of this, an additional digit with a value of 1 may appear at the more significant end of the display when measurements are made. If the 10% display overrange is exceeded, with eight digits selected, the overflow LED will light. An overflow can also occur when NULL or 100 AVG is enabled. The overflow digit can be displayed by decreasing the resolution.

16 With some measurement functions, the number of digits appearing may be less than the selected resolution to ensure that they are rounded to meaningful values.

17 When RATIO measurements are made, no more than eight digits are displayed, regardless of the resolution selected.

18 For the TOTAL A by B and TOTAL A measurement functions the display shows the true total of events counted from 1 to 99999999. For higher totals the exponent is used.

19 For the PHASE A rel B measurement, up to four digits may be displayed for frequencies up to 100 kHz and up to three digits for higher frequencies. Leading zeros are suppressed. For frequencies above 100 kHz the resolution of the display is reduced, and place-holding (half size) zeros are displayed as the least-significant digits.

Setting the Display Resolution

20 Whenever the resolution control indicator is lit, the resolution can be changed using the step-up and step-down keys.

GATE TIME

21 For the frequency, period and ratio measurement functions, the gate time is related to the resolution selected, as shown in Table 4.1.

TABLE 4.1

Resolution and Gate Time

Resolution	Gate Time
8	10 s
7	1 s
6	100 ms (see NOTE 2)
5	10 ms
4	1 ms
3	1 ms (see NOTE 3)

NOTE 1:
The gate times shown are nominal. Due to the use of the reciprocatic counting technique the gate time may be extended by up to one period of the input signal on FREQ A, PERIOD A and RATIO A/B.

NOTE 2:
A resolution of 6 is selected when the instrument is first switched on.

NOTE 3:
With a resolution of 3 selected, measurements are averaged.

22 For the PHASE A rel B measurement function the gate time depends upon the signal frequency. The gate time is approximately 50 ms for frequencies above 200 Hz, but will be increased at lower frequencies.

NULL FEATURE

23 The null feature allows a displayed value to be entered into the internal NULL store. When the null feature is enabled (NULL indicator lit) the display indicates

(measured value minus the value held in the NULL store).

24 The null feature is avilable with all functions except phase and check.

25 (1) Use the procedures given in paragraphs 4 to 12 to set up the instrument to display the measurement required. If nulling from a value already in the NULL store, press

[RECALL] [NULL] .

The value in the NULL store will be displayed.

(2) To enable NULL, press

[NULL] .

The NULL indicator will light. The displayed value will be entered into the NULL store. When a new measurement is made the display indicates the difference between the measured value and the value in the NULL store.

(3) To disable the null facility, press

[NULL] .

The NULL indicator will go out and the display will indicate the measured value. The value in the NULL store is unchanged.

26 The value held in the NULL store can be displayed at any time by pressing

[RECALL] [NULL] .

To return the instrument to the status existing before the NULL store contents were displayed press

[CONTINUE] .

STOP CIRCUIT DELAY (HOLD OFF)

Use of the Delay

27 The stop circuit can be delayed when the T.I. A→B or the TOTAL A by B measurement function is selected. The required delay is entered into an internal store by the operator. The delay function can then be enabled and disabled as required. The delay is set to 10 ms when the instrument is first switched on.

28 The delay can be used to prevent the stop circuit being triggered prematurely by spurious signals, such as those resulting from contact bounce. The principle is shown in Fig 4.1.

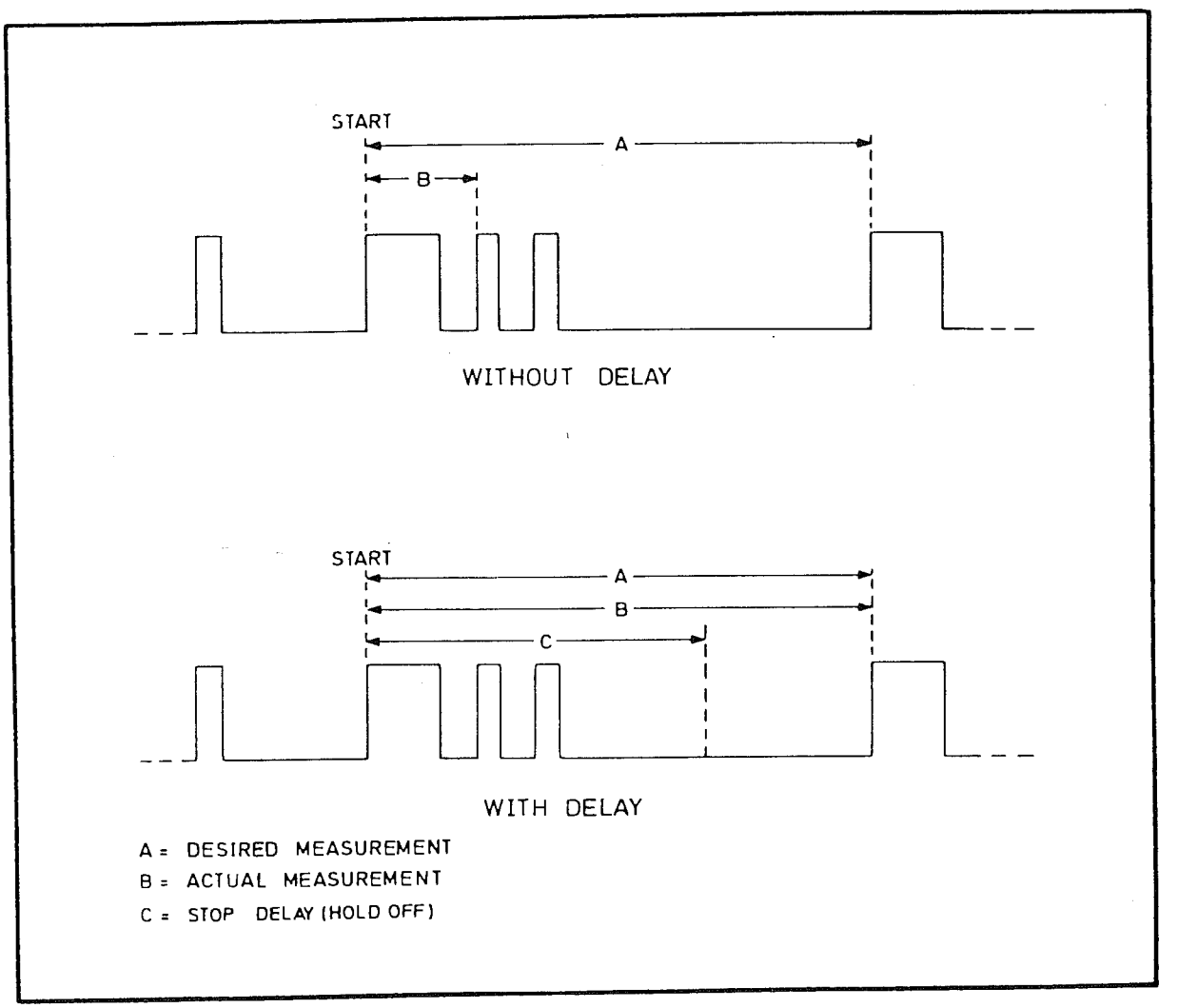


Fig 4.1 Use of Stop Circuit Delay

Displaying the Delay

29 The value of delay held in the store can be displayed by pressing

RECALL DELAY

Changing the Delay

30 The delay value stored is changed using the DELAY VALUE ↑ or ↓ keys. Pressing RESET/CONTINUE or DELAY stores the new delay value and returns the instrument to measurement mode. If DELAY has been pressed, the newly entered delay value is also enabled.

31 The permitted range of delay is from 200 µs to 800 ms. The value in the delay store is retained when the instrument is switched to standby.

Enabling and Disabling the Delay

32 The stop delay is enabled and disabled by means of the DELAY key. The DELAY indicator lights when the delay is enabled.

AVERAGE OF 100 READINGS

33 This feature allows one extra digit of resolution to be obtained by taking 100 readings into store and displaying the software average value. The average of 100 readings can be used with the Time Interval, Phase Measurement, Frequency A, Period A and Ratio A/B.

34 To enable the averaging facility press the 100 AVG key. The 100 AVG indicator will light.

35 With the appropriate signals connected the instrument will take 100 measurements, during which time the gate indicator will flash 100 times. The average value is then displayed. For reliable operation the signal must be constant during the measurement period and asynchronous (not related) to the counters frequency standard.

36 A new sequence can be started at any time by pressing

RESET / CONTINUE

37 To disable the averaging feature press 100 AVG . The 100 AVG indicator will go out.

SPECIAL FUNCTIONS

Frequency B

38 This function can be activated in FREQUENCY A mode only, by pressing:

DELAY

and holding the key down for three seconds. The DELAY indicator will then light and the counter will measure frequency B to the resolution selected.

39 To disable Frequency B press:

DELAY or RESET / CONTINUE .

The DELAY indicator will go out. Note that normal delay mode is not available in Frequency.

LED Check

40 When in CHECK mode this function is activated by pressing:

RECALL .

The LED Check causes the display and single LEDs to be alternately on and then off at a 3-second rate. All LEDs are checked, including the GPIB LEDs (if GPIB is fitted), except the STBY/CHRG, GATE and TRIG LEDs. To revert to the CHECK function press

RESET / CONTINUE .

ERROR CODES

41 The instrument is able to detect a number of error states, which are indicated on the display. The meanings of the error codes are shown in Table 4.2

TABLE 4.2

Error Codes

Display	Error
Er 01	Phase measurement attempted on signals of different frequencies.
Er 02	Measurement result too large or too small for the display.
Er 03	Overflow of internal counters.
Er 04	Number entry error (GPIB only).
Er 05	GPIB programming error (GPIB only).
Er 06	Phase inputs greater than 5 MHz.
Er 50	Basic check function error.

Clearing the Error Codes

42 Error code Er 01 is cleared by:

(1) Making a phase measurement on signals of equal frequency.

(2) Selecting another measurement function.

Error codes Er 02 and Er 03 are cleared by:

(1) Obtaining a measurement result that is within range.

(2) Selecting another measurement function

Error code Er 06 is cleared by:

(1) Reducing the input frequency to less than 5 MHz.

(2) Selecting another measurement function.

USING THE BATTERY PACK OPTION

Power Supply Changeover

43 When the battery pack option is installed, the instrument can be powered from the internal battery, an external DC supply of 11V to 16V, or an external AC supply. If the instrument is operating from either the DC supply or the battery, it will automatically change to operation from the AC supply when this is connected. The battery will not take over from either the AC or the DC supply if the supply fails. An external DC supply will not take over from the AC supply if the AC supply fails.

Battery-Low Indication

44 When the instrument is operating from the internal battery, or from an external DC supply, the STBY/CHRG indicator will start to flash as the supply voltage approaches the minimum permissible level. This occurs regardless of whether the instrument is in the standby mode or not. When operating from the battery, the instrument can be used in the measurement mode for approximately 15 minutes after the indicator commences flashing.

45 When the voltage of the battery or the external DC supply reaches the minimum permissible level, the instrument shuts down completely.

Operating Instructions

46 Instructions for preparing the instrument to make measurements are given in the following paragraphs. No other change in the operating procedure is required.

Operation From the Battery

47 (1) Set the internal/external switch on the rear panel to INTERNAL BATTERIES.

(2) Set the BATTERY SAVE/NORMAL switch to NORMAL.

(3) Switch the instrument on.

(4) Check that the instrument goes through the normal switch-on sequence. If the STBY indicator is flashing, or if there is no display, charge the battery.

48 If the battery-save facility is to be used, set the BATTERY SAVE/NORMAL switch to BATTERY SAVE. The instrument will remain in the measurement mode for approximately one minute and will then switch to standby. It can be returned to the measurement mode for a further period of one minute by pressing the STBY/CHRG key.

Operation From an External DC Supply

49 (1) Ensure that the instrument is switched off.

(2) Connect the DC supply to the DC power-input plug on the rear panel. The mating connector is a 2.1 mm coaxial socket.

CAUTION: SUPPLY POLARITY
THE POSITIVE SIDE OF THE SUPPLY MUST BE CONNECTED TO THE CENTER CONDUCTOR.

(3) Set the internal/external switch on the rear panel to EXTERNAL 11-16V.

(4) Switch the instrument on. Check that the instrument goes through the normal switch-on sequence.

Battery Charging

50 The battery is trickle-charged whenever the instrument is operated from an AC supply and the internal/external switch is set to INTERNAL BATTERIES. To charge the battery at the full rate, connect the instrument to an external AC or DC supply, switch on and select the standby mode.

SECTION 5 OPERATING VIA THE GPIB

INTRODUCTION

1 The instrument must be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the AC line voltage selector.

GPIB OPERATING MODES

2 The instrument can be operated via the GPIB in either the addressed mode or the talk-only mode.

TALK-ONLY MODE

3 The talk-only mode may be used in systems which do not include a controller. Such a system permits remote reading of the instrument's measurement data, but the instrument is operated by means of the front-panel controls as described in Section 4.

4 The rate at which measurements are made is determined by the instrument. The output buffer is updated at the end of each measurement cycle, overwriting the previous measurement data if this has not been transferred to the listener.

5 The transfer of data from the instrument to the listener is triggered by the listener. The instrument's output buffer is cleared when the data transfer is complete. Problems arising from the differences between the measurement rate and data transfer trigger rate are resolved according to the following protocol:

(1) If data transfer is in progress at the end of a measurement cycle, the updating of the output buffer is delayed. The data transferred will relate to the previous measurement cycle.

(2) If the data transfer trigger occurs during a measurement cycle and the output buffer is empty, data transfer will be delayed until the buffer is updated. The data transferred will then relate to the latest measurement cycle.

(3) If a measurement cycle is completed before the results of the previous cycle have been transferred to the listener, the buffer will be updated. The data for the previous cycle will be overwritten and lost.

6 The rate at which measurements are made can be controlled in the following ways:

(1) The gate time of the instrument (duration of the measurement cycle) can be controlled by choosing an appropriate display resolution.

(2) The instrument can be operated in the hold mode. Single measurement cycles can be triggered, when required, by means of the RESET key.

7 The format of the data output is described in Table 5.1.

ADDRESSED MODE

8 In addressed-mode operation, all the instrument's functions, except the power ON/OFF, standby switching and trigger levels, can be controlled by means of device-dependent commands, sent via the bus, when the instrument is addressed to listen. The measurements made, and data regarding the instrument's status, can be read via the bus when the instrument is addressed to talk. If the instrument is addressed to talk when the output buffer is empty, no data transfer can take place and bus activity will cease. Data transfer will commence when the output buffer is updated at the end of the next measurement cycle.

DATA OUTPUT FORMAT

9 The same output message format is used for the transmission of measured values and numbers recalled from the instrument's internal stores. The message consists of a string of 21 ASCII characters for each value transmitted. These are to be interpreted as shown in Table 5.1. The units should be assumed to be Hz, seconds, degrees or a ratio, depending upon the commands previously given to the instrument.

DEFERRED COMMANDS AND IMMEDIATE COMMANDS

10 Some commands (known as Deferred Commands) are accepted until a terminating character or message is received, see Table 5.5. The whole string will then be obeyed. Other commands (known as Immediate Commands) are obeyed as soon as they are received. These are indicated, in Table 5.18, by an asterisk.

EXAMPLE: OUTPUT 716; FA ANS SRS5 S81 CR LF

Because SRS is an immediate command, Frequency A, A Channel Negative Slope, and 5 Digit Resolution will all be set following receipt of SRS5.

TABLE 5.1

Output Message Format

Byte No	Interpretation	Permitted ASCII Characters
1	Function letter	See Table 5.2
2	Function letter	
3	Sign of measurement	+ or -
4	Most significant digit	0 to 9
5	Digit	0 to 9 or .
6	Digit	0 to 9 or .
7	Digit	0 to 9 or .
8	Digit	0 to 9 or .
9	Digit	0 to 9 or .
10	Digit	0 to 9 or .
11	Digit	0 to 9 or .
12	Digit	0 to 9 or .
13	Digit	0 to 9 or .
14	Digit	0 to 9 or .
15	Least significant digit	0 to 9 or .
16	Exponent indicator	E
17	Sign of exponent	+ or -
18	More significant digit	0 to 9
19	Less significant digit	0 to 9
20	Carriage return	CR
21	Line Feed	LF

NOTE 1:
Bytes 4 to 15 will always include 11 digits and a decimal point. Zeros will be added, where necessary, in the more significant digit positions.

NOTE 2:
The exponent indicated by bytes 18 and 19 will always be a multiple of three.

TABLE 5.2

Function Letters

Function	Function Letters
Frequency A	FA
Period A	PA
Time interval	TI
Total A by B	TA
Phase	PH
Ratio A/B	RA
Check	CK
Total A	TM
Time	TC
Recalled Data	**Function Letters**
Unit type	UT
Resolution	RS
Null store	NL
Delay time	DT
Special function	SF
Master software issue number	MS
GPIB software issue number	GS

NOTE:
Spaces are substituted for the function letters when special function 81 is active.

SERVICE REQUEST

11 The instrument can be set, by means of device-dependent commands, to generate the service request message (SRQ) when:

(1) A measurement cycle is completed
(2) A change of frequency standard occurs
(3) An error state is detected
(4) Any combination of (1), (2) and (3).

12 The generation of the SRQ may also be inhibited. The necessary commands are given in Table 5.17. Option (3) of Paragraph 10 is selected when the instrument is first switched on.

STATUS BYTE

13 The format of the status byte, generated in response to a serial poll, is given in Table 5.3.

TABLE 5.3

Status Byte Format

DIO Line	Function
1	LSB } Number of error detected (binary)
2	
3	MSB } (See NOTE 1)
4	'1' = frequency standard changed
5	'1' = reading ready (See NOTE 2)
6	'1' = error detected
7	'1' = service requested
8	'1' = gate open

NOTE 1:
The error code numbers which can occur are:

1 Phase measurement attempted on waveforms of differing frequency.
2 Result out of range of the display
3 Overflow of internal counters
4 Error in numerical entry
5 Syntax error in GPIB command
6 Phase measurement attempted on signal above 10 MHz.

No measurement data string is available if error code 1, 2 or 3 is generated.

NOTE 2:
Regardless of the SRQ mode in use, the SRQ message that a reading is ready is not generated following a data-recall operation.

NOTE 3:
The errors are cleared as follows:

Error 1: Correct the difference in input frequencies or change the measurement mode in use.

Error 2: The error is cleared when an in-range measurement is completed.

Error 3: The error is cleared when an in-range measurement is completed.

Error 4: The error is cleared when a valid numerical entry is made.

Error 5: The command string will be correctly executed up to the point at which the error occurs. The remainder of the string will be hand-shaken, but not executed. The error is cleared when the next valid command is received.

Error 6: Correct the input frequency or change the measurement mode in use.

EXPLANATION OF RESPONSE TO INTERFACE MESSAGES

14 The instrument will respond to all valid device-dependent commands which are received after it has been addressed to listen. Device-dependent commands are recognized as such because they are transmitted with the attention (ATN) message false.

15 The instrument also responds to a number of multi-line interface messages. These are recognized because they are transmitted with the ATN message true. Refer to Table 5.4, which gives the instrument's response to different bus messages. The following paragraphs detail the instrument's response to these messages. Any multi-line message not specifically mentioned is hand-shaken, but is otherwise ignored.

Address Messages

16 The instrument responds to address messages defined by the setting of the address switches, A1 to A5, on the rear panel.

17 On receipt of its listen address, the instrument becomes a listener. If it has previously been addressed to talk it ceases to act as a talker. If in the local control state when the address is received, the instrument goes to the remote control state provided that the REN message is true.

18 On receipt of its talk address, the instrument becomes a talker. If it has previously been addressed to listen it ceases to act as a listener. If in the local control state when the address is received, it will remain under local control.

19 If the instrument has been addressed to talk, and then receives the talk address of another device, it ceases to act as a talker.

Local Lockout

20 The instrument will respond to the local lockout (LLO) message regardless of its addressed state. The return-to-local function of the LOCAL key on the front panel is disabled (the RESET/CONTINUE function remains enabled when in local control).

21 Local lockout is cleared by sending the remote enable (REN) message false. This returns all devices on the bus to the local control state.

Device Clear and Selected Device Clear

22 The instrument only responds to the device clear (DCL) message and the selected device clear (SDC) message when it is in the remote control state. It will only respond to the SDC message if it is a listener, but will respond to the DCL message regardless of its addressed state.

23 The instrument responds to either message by reverting to the functions and settings of the power-up state. No change is made to the condition of the GPIB interface.

Response to Bus Messages

Message	Addressed State	Instrument Response
Address	Any	For listen address: Becomes a listener and goes to the remote control state. If previously addressed to talk, ceases to act as a talker. For talk address: Becomes a talker. If previously addressed to listen, ceases to be a listener. For talk address of another device: If previously addressed to talk, ceases to be a talker.
Local Lockout (LLO)	Any	LOCAL key disabled. (Cleared by sending the REN message false).
Device Clear (DCL) Selected Device Clear (SDC)	Any, but must be in remote control. Listen and in remote control	Reverts to power-up state.
Serial Poll Enable (SPE)	Any	Enters the serial poll mode state (SPMS). If addressed to talk while in this state, sends the status byte.
Serial Poll Disable (SPD)	Any	Enters the serial poll idle state (SPIS). If addressed to talk while in this state, sends data in the output message format.
Group Execute Trigger (GET)	Listen, and no measurement cycle in progress	Takes a measurement.
Go to Local (GTL)	Listen	Reverts to local control.
Untalk (UNT) Unlisten (UNL)	Talk Listen	Ceases to be a talker. Ceases to be a listener. The ADDR indicator is turned off.

Serial Poll Enable and Serial Poll Disable

24 The instrument responds to both the serial poll enable (SPE) message and the serial poll disable (SPD) message regardless of its addressed state.

25 The instrument responds to the SPE message by entering the serial poll mode state (SPMS). If the instrument is addressed to talk while in this state, it will put its status byte onto the bus instead of its normal data output string.

26 The instrument responds to the SPD message by leaving the SPMS and entering the serial poll idle state (SPIS). If the instrument is addressed to talk while in this state, it will put its data output string onto the bus provided data is available in the output buffer.

Group Execute Trigger

27 The instrument responds to the group execute trigger (GET) message provided that it is a listener and no measurement cycle is in progress. Except for the inability to retrigger during a measurement cycle, the response to the GET message is the same as to the device-dependent command T2.

Go to Local

28 The instrument responds to the go to local (GTL) message provided that it is a listener. The instrument reverts to the local control state, but remains addressed to listen. It will return to remote control on receipt of the first byte of a device-dependent command.

Untalk and Unlisten

29 If addressed to talk, the instrument will go to the talker idle state (TIDS) on receipt of the untalk message. If addressed to listen, it will go to the listener idle state (LIDS) on receipt of the unlisten message. The ADDR indicator will be turned off.

INPUT COMMAND CODES

30 When the instrument is addressed to listen it can be controlled by means of device-dependent commands given in the following tables:

31 If more than one command is to be sent, no delimiters are required. If necessary, commas, spaces and semicolons may be included in command strings as an aid to clarity without affecting the operation of the instrument. Each command string must be followed by an end-of-string terminating group. The permitted terminating groups are shown in Table 5.5.

TABLE 5.5

Permitted Terminators

1	2	3	4	5	6
LF	LF EOI true	CR EOI true	CR LF	CR LF EOI true	Last Character EOI true

TABLE 5.6

Instrument Preset Code

Function	Code
Set instrument functions and settings to the power-up state	IP

TABLE 5.7

Measurement Function Codes

Function	Code
Frequency A	FA
Period A	PA
Time interval	TI
Total A by B	TA
Phase of A relative to B	PH
Ratio A/B	RA
Check	CK
Total A	TM
Time	TC

TABLE 5.8

Input Control Codes

Function	Code	
	A Channel	B Channel
AC coupling selected	AAC	BAC
DC coupling selected	ADC	BDC
Positive slope trigger selected	APS	BPS
Negative slope trigger selected	ANS	BNS
X10 attenuator disabled	AAD	BAD
X10 attenuator enabled	AAE	BAE
A channel filtering enabled	AFE	
A channel filtering disabled	AFD	
A and B channels separate		BCS
A and B channels common		BCC

TABLE 5.9

Measurement Control Codes

Function	Code
Select continuous measurement mode	TØ (see NOTE 1)
Select one-shot measurement mode	T1 (see NOTE 2)
Take one measurement or start total A or time measurement	T2 (see NOTE 3)
Stop total A or time measurement	T3 (see NOTE 3)
Read present value without stopping totalize measurement	RF (see NOTE 4)
Null disabled	ND
Null enabled	NE
Delay disabled	DD
Delay enabled	DE
100 Average disabled	NA
100 Average enabled	AE
Reset (Stop measurement cycle and clear output buffer)	RE

NOTE 1:
When making continuous measurements the output buffer is updated at the end of each gate period. If the buffer is being read via the GPIB when the gate period ends, updating is delayed until reading is complete.

NOTE 2:
When one-shot measurements are being made, the output buffer is cleared each time command T2 is received. The measurement made must, therefore, be read before a further measurement cycle is triggered.

NOTE 3:
When making totalize measurements, commands T2 and T3 are used with TM. In this mode the readings made in successive totalize periods are cumulative. The RE command is used to reset the count to zero when required.

NOTE 4:
The RF command (reading on the fly) must be sent each time a reading is required. The reading is obtained when the instrument is made a talker.

TABLE 5.10

Store and Recall Codes

Function	Code
Recall unit type	RUT
Store display resolution number	SRS
Recall display resolution number	RRS
Store null value	SN (see NOTE 1)
Recall null value	RN (see NOTE 1)
Store delay value	SDT
Recall delay value	RDT
Recall special function register	RSF
Recall master software issue number	RMS
Recall GPIB software issue number	RGS

NOTE 1:
Numbers to be stored should follow the store command. The format to be used for numerical entry is given in Table 5.11. The limiting values for numerical entries are given in Table 5.12.

NOTE 2:
The instrument returns to the measurement mode automatically at the completion of a store or recall operation.

NOTE 3:
No SRQ message is generated for recalled data.

TABLE 5.11

Numerical Input Format

Byte	Interpretation	Permitted ASCII Characters
1	Sign of mantissa	+ or -
2	Most significant digit	0 to 9 or .
3	Digit	0 to 9 or .
4	Digit	0 to 9 or .
5	Digit	0 to 9 or .
6	Digit	0 to 9 or .
7	Digit	0 to 9 or .
8	Digit	0 to 9 or .
9	Digit	0 to 9 or .
10	Digit	0 to 9 or .
11	Least significant digit	0 to 9 or .
12	Exponent indicator	E or e
13	Sign of exponent	Space, + or -
14	More significant digit	0 to 9
15	Less significant digit	0 to 9

NOTE 1:
Spaces, nulls or zeros occurring immediately before byte 1 will be ignored.

NOTE 2:
Byte 1 may be omitted. A positive mantissa will then be assumed.

NOTE 3:
Bytes 2 to 11 may contain up to nine digits and a decimal point. If more than nine digits are entered without a decimal point, excess digits will be truncated. The excess digits will, however, increase the power of ten stored.

If fewer than nine digits are required the unused bytes may be omitted.

NOTE 4:
Spaces or nulls entered between bytes 11 and 12 will be ignored.

NOTE 5:
The exponent group, bytes 12 to 15, may be omitted.

NOTE 6:
Byte 13 may be omitted or transmitted as a space. In either case a positive exponent will be assumed.

NOTE 7:
Byte 15 may be omitted for a single-digit exponent.

NOTE 8:
Units are assumed to be seconds for delay time.

TABLE 5.12

Numerical Input Ranges

Function	Command Code	Numerical Limits	
		Low	High
Resolution	SRS	3	8
Null store	SN	1×10^{-9}	1×10^{10}
		0	
		-1×10^{10}	-1×10^{-9}
Delay time	SDT	200×10^{-6}	0.8

NOTE 1:
Delay time entries will be rounded up before storage, as follows:

1 ms to 800 ms in multiples of 1 ms, or a fixed delay of 200 µs.

NOTE 2:
Resolution entries will be rounded down to the next integer. The related gate times are shown in Table 5.13.

NOTE 3:
The exponential numbers format is shown in Table 5.11.

TABLE 5.13

Resolution Selection

Number of digits in Freq., Period, Time and Check.	Gate Time	Resolution number
8	10 s	8
7	1 s	7
6	100 ms	6
5	10 ms	5
4	1 ms	4
3	1 ms	3

TABLE 5.14

Special Function Codes

Function	Code
Enter special function nn in special function register	Snn

NOTE 1:
The list of special functions is given in Table 5.15.

NOTE 2:
A special function number entered in the register while the special functions are enabled will be enabled immediately.

TABLE 5.15

Special Functions

Function Number	Function Description
20	Normal operation
21	Frequency B
70	Basic 10 MHz check
71	LED check
80	Leading letters in output string
81	No leading letters in output string

Special Function Register

32 The special functions are stored in a register organised by decades. Only decades 2, 7 and 8 are used in this instrument. The first digit of a special function number indicates its position in the register and the second digit is stored in that location. If recalled, the special function register will be transmitted as a string of 21 ASCII characters. These are interpreted in Table 5.16.

TABLE 5.16

Output Message Format

Byte	Output Characters	Notes
1	'S' or space	Spaces transmitted if
2	'F' or space	SF 81 is programmed
3	'+'	
4, 5	0	
6	0 or 1	0 = SF20 selected 1 = SF21 selected
7-10	0	
11	0 or 1	0 = SF70 selected 1 = SF71 selected
12	0 or 1	0 = SF80 selected 1 = SF81 selected
13-15	0	
16	'E'	
17	'+'	
18, 19	0	
20	CR	
21	LF	

TABLE 5.17

Service Request Codes

Function	Code
Inhibit generation of SRQ	QØ
SRQ generated when error is detected	Q1
SRQ generated for measurement ready	Q2
SRQ generated for measurement ready or error detected	Q3
SRQ generated for frequency standard changeover	Q4
SRQ generated for frequency standard changeover or error detected	Q5
SRQ generated for measurement ready or frequency standard changeover	Q6
SRQ generated for measurement ready, error detected or frequency standard changeover	Q7

NOTE:
SRQ is not generated by data recalled from store.

TABLE 5.18

Alphabetic List of Command Codes

Code		Code	
AAC	A channel, AC coupling	ND	Null disabled *
AAD	A channel X10 attenuator disabled	NE	Null enabled *
AAE	A channel X10 attenuator enabled	PA	Period A
ADC	A channel, DC coupling	PH	Phase A relative to B
AE	100 Average enabled	Qn	SRQ mode *
AFD	A channel filtering disabled	RA	Ratio A/B
AFE	A channel filtering enabled	RDT	Recall delay time
ANS	A channel, -ve slope	RE	Reset measurement
APS	A channel, +ve slope	RF	Read total so far
BAC	B channel, AC coupling	RGS	Recall GPIB software issue
BAD	B channel X10 attenuator disabled	RMS	Recall master software issue number *
BAE	B channel X10 attenuator enabled	RN	Recall null value *
BCC	A and B channels common	RRS	Recall resolution *
BCS	A and B channel separate	RSF	Recall special function *
BDC	B channel, DC coupling	RUT	Recall unit type *
BNS	B channel, -ve slope	Snn	Special Function number *
BPS	B channel, +ve slope	SDT	Store delay time
CK	Check	SN	Store null value *
DD	Delay disabled	SRS	Store resolution *
DE	Delay enabled	TA	Total A by B
FA	Frequency A	TC	Time
IP	Instrument preset *	TI	Time interval
NA	100 Average function disabled	Tn	Measurement mode or Start/Stop reading

NOTE:
n represents a single digit.
* = Immediate Command, see Deferred Commands and Immediate Commands on Page 5-2.

INTRODUCTION

1 This section describes the principles of operation of the instrument, with respect to a number of block diagrams in the text, and describes the significant features of the circuits used with respect to the circuit diagrams given in Section 8. The block diagrams are annotated with the main circuit references to simplify cross referencing between the block diagram and circuit diagram.

2 In the circuit descriptions the integrated circuits are referred to by the circuit reference given on the appropriate circuit diagram. Note that a separate series of numbers, starting at IC1, is allocated to each assembly. Where an integrated circuit package contains more than one circuit, suffix letters are used to distinguish between them. Where it is required to identify a particular pin of an integrated circuit, the circuit reference, with suffix letter if appropriate, is followed by an oblique stroke and the required pin number.

FUNCTIONAL SYSTEMS

3 The instrument contains eight functional systems. These are:

(1) The channel A and channel B system.

(2) The measurement system.

(3) The display system.

(4) The keyboard system.

(5) The microprocessor system.

(6) The standby and IRQ system.

(7) The power supply system.

(8) The frequency standard system.

4 The functional relationship between the systems is illustrated in Fig 6.1. The measurement system is internally configured by the microprocessor system according to the instructions entered via the keyboard or GPIB system. The signal to be measured and the signal from the frequency standard are fed to the measurement system. The measured result is passed to the microprocessor system. If mathematical manipulation of the result is required, this is performed by the microprocessor before the final output is passed to the display or GPIB system.

5 The standby and IRQ system handles instructions to switch to standby, received from the keyboard system or the battery pack option, and interrupt requests made by other systems.

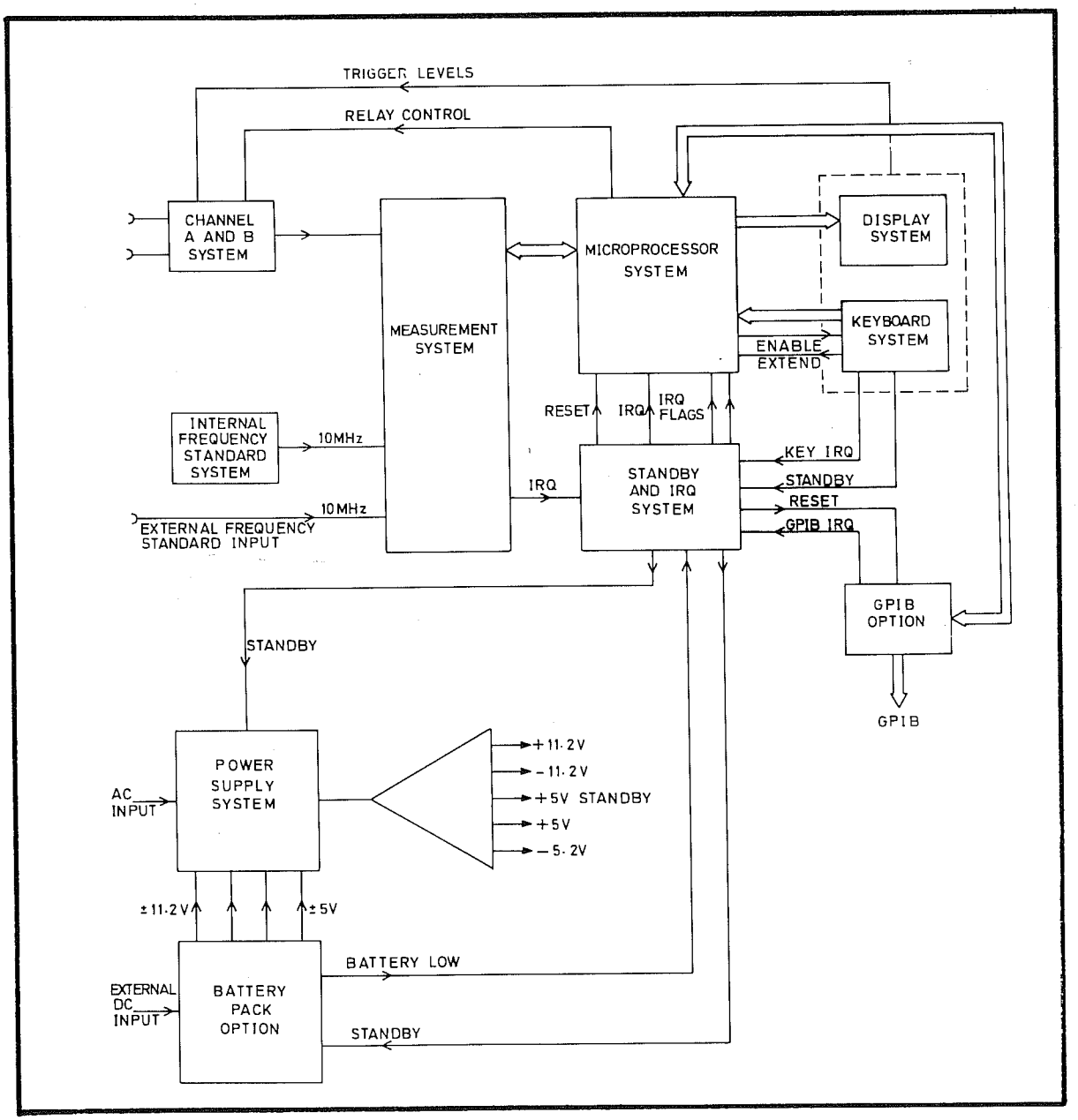


Fig 6.1 Functional Block Diagram

THE CHANNEL A AND CHANNEL B SYSTEM

Functional Description

6 The channel A and channel B system processes the signals applied at the channel A and channel B inputs to produce differential pairs of signals which are fed to the measurement system. A block diagram is given in Fig 6.2.

7 Each channel includes relay-controlled circuits which allow selection of AC/DC coupling and X1/X10 attenuation. The common A configuration (channel B signal disconnected and channel A signal connected to both amplifiers in parallel) can be selected.

8 The channel amplifiers feature separate high frequency and low frequency paths. The crossover frequency is nominally 5 kHz. Signal filtering can be introduced, in channel A only, by disconnecting the high frequency amplifier path and increasing the bandwidth of the low frequency path to 50 kHz nominal. The signals from the high and low frequency paths are combined, and drive a Schmitt trigger output stage.

9 The trigger levels for the two channels are derived from manual controls on the front panel.

10 Control signals for the system relays are supplied from the microprocessor system.

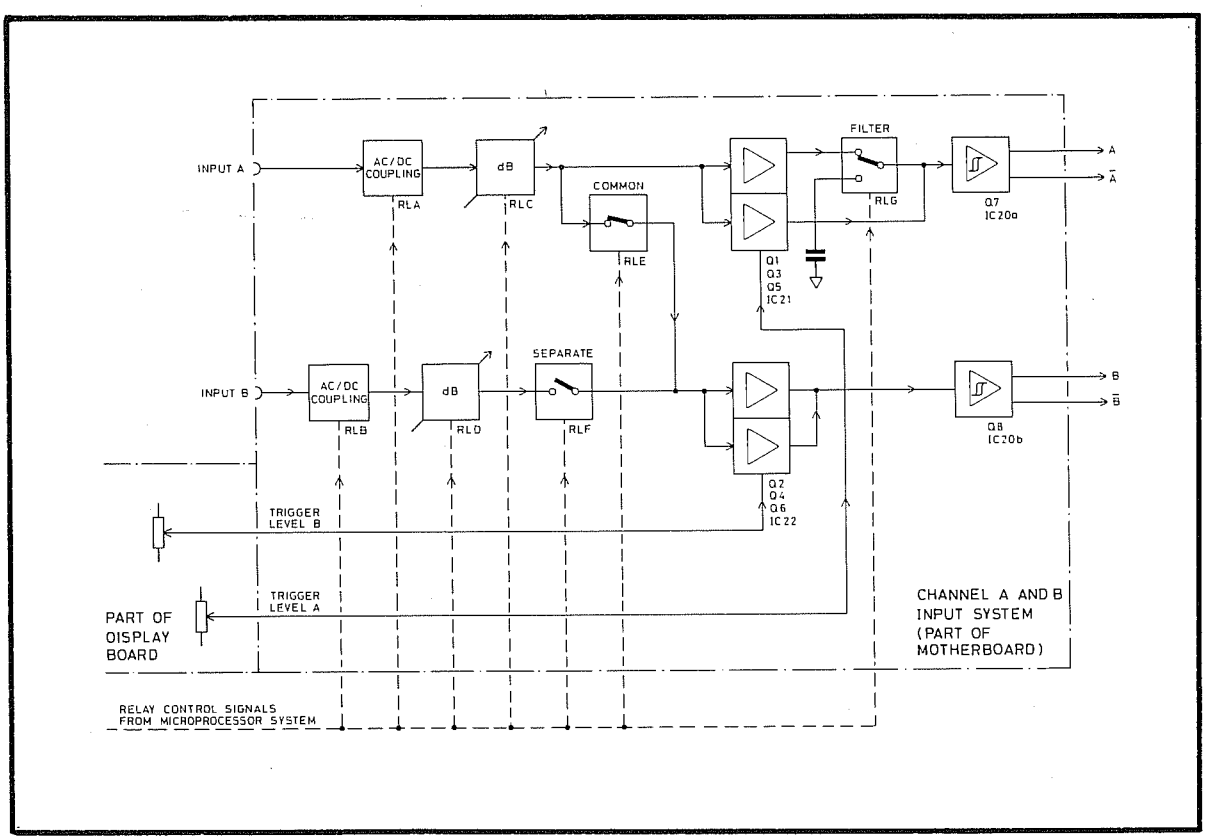


Fig 6.2 The Channel A and Channel B System

Circuit Description

11 The circuit diagram is shown in Fig 5 in Section 8.

12 When energised, RLA gives DC coupling of the input signal. With RLA de-energised the signal is AC coupled via C1. R3 limits the current surge which occurs if DC coupling is selected while C1 is in the charged state.

13 The X1/X10 attenuator is formed by R9, R10, and RLC. With RLC de-energised, the attenuator has a series element R9 and a shunt element formed by R10 and the amplifier impedance of 1MΩ in parallel. The attenuation is 20 dB (nominal). With RLC energised R9 is short circuited, giving 0 dB attenuation.

14 The signal is then fed to a combined limiter and fixed attenuator. R16, R21 and R22 form the attenuator; with D1, D2, D3 and D4 limiting the signal to about ±3.5 V. The attenuator insertion loss is about 1.5 dB.

15 The high-frequency channel buffer is a compound follower (Q1 and Q3) with a gain from Q1 gate to Q3 emitter of approximately 0.94.

16 The low-frequency channel buffer IC21 and Q5, receives its input from the potential divider R21, R22. The gain from the divider input to Q5 emitter is approximately 0.94. Any offset in the system can be nulled by adjusting R33.

17 When RLG is de-energised (channel A filter not selected) the signals from the two buffers are combined at the base of Q7 by the network C15 and R39. These components act as a low-pass filter to the output of the low frequency buffer, and as a high-pass filter to the output of the high frequency buffer. The crossover frequency is 5 kHz.

18 The signal at Q7 emitter is fed to the Schmitt trigger, IC20a, via the diode bridge formed by D9a, D9b, D10a and D10b. This protects the input of IC20a by limiting the signal swing to approximately ±2.5 V.

19 The differential output of IC20a forms the input to the measuring system. The hysteresis of IC20a, and therefore the channel sensitivity, can be set by adjusting R72.

20 The trigger level from the display board is attenuated by R58 and R54, giving a loss of 1.5 dB to compensate for the limiter loss in the signal path. It is then fed into the low-frequency buffer via R49. Feedback, taken from the emitter of Q7 to IC21/2 via R47 and R48, makes IC21/2 a virtual earth point, and the gain from the R49/R54 junction to the emitter of Q7 is -0.94. A 1 V DC level at the channel A input and a 1 V trigger level therefore combine to give 0 V at Q7 emitter. Thus the selected trigger point on the input signal is always brought to 0 V at Q7 emitter.

21 The trigger levels are derived from the supply rails on the display board. The circuit diagram is shown in Fig. 3 in Section 8. For channel A, variable resistor R3 is connected across the +5 V, -5.2 supplies, and the wiper taps off part of this voltage. The tapped voltage passes via S20 (normally closed) and is attenuated via R2 and the load resistances on the motherboard. R7 provides a buffered output to the front panel.

22 With the trigger control set to the switched 0 V position. S20 opens and the trigger level is grounded via the load resistors R58 and R54 on the motherboard. This gives an accurately set 0 V trigger level with maximum signal sensitivity.

23 The channel B trigger level control operates in a similar way.

24 When the channel A low-pass filter is selected, RLG is energised. This open circuits the high frequency channel, and connects C16 across the low frequency channel. The low frequency channel bandwidth is then nominally 50 kHz.

25 The circuit of channel B is similar to that of channel A, but is not provided with a low-pass filter. Energizing RLE connects the signal applied at the channel A input to both channel amplifiers, while de-energising RLF isolates the channel B input. RLE and RLF always operate simultaneously and in the opposite sense to each other.

26 The relays are controlled by the microprocessor system. The voltage levels on the control lines are latched in IC7, shown in Fig 6 in Section 8.

THE MEASUREMENT SYSTEM

Functional Description

27 The measurement circuits of the instrument are provided by two custom-built integrated circuits. These are the Multiple Counter and Control (MCC) circuits, MCC1 and MCC2. A block diagram is shown in Fig 6.3.

28 The circuits within MCC1 and MCC2 are configured by the microprocessor according to the measurement function in use. The recipromatic counting technique is used. With this technique the measured signal, not the counter clock pulses, controls the start and stop of the measurement period (gate time) as shown in Fig 6.4. The gate time therefore extends over an integral number of cycles of the measured waveform. The gate time is measured by counting the clock pulses which occur while the gate is open.

29 For all measurement functions the signals to be measured are fed directly to MCC2.

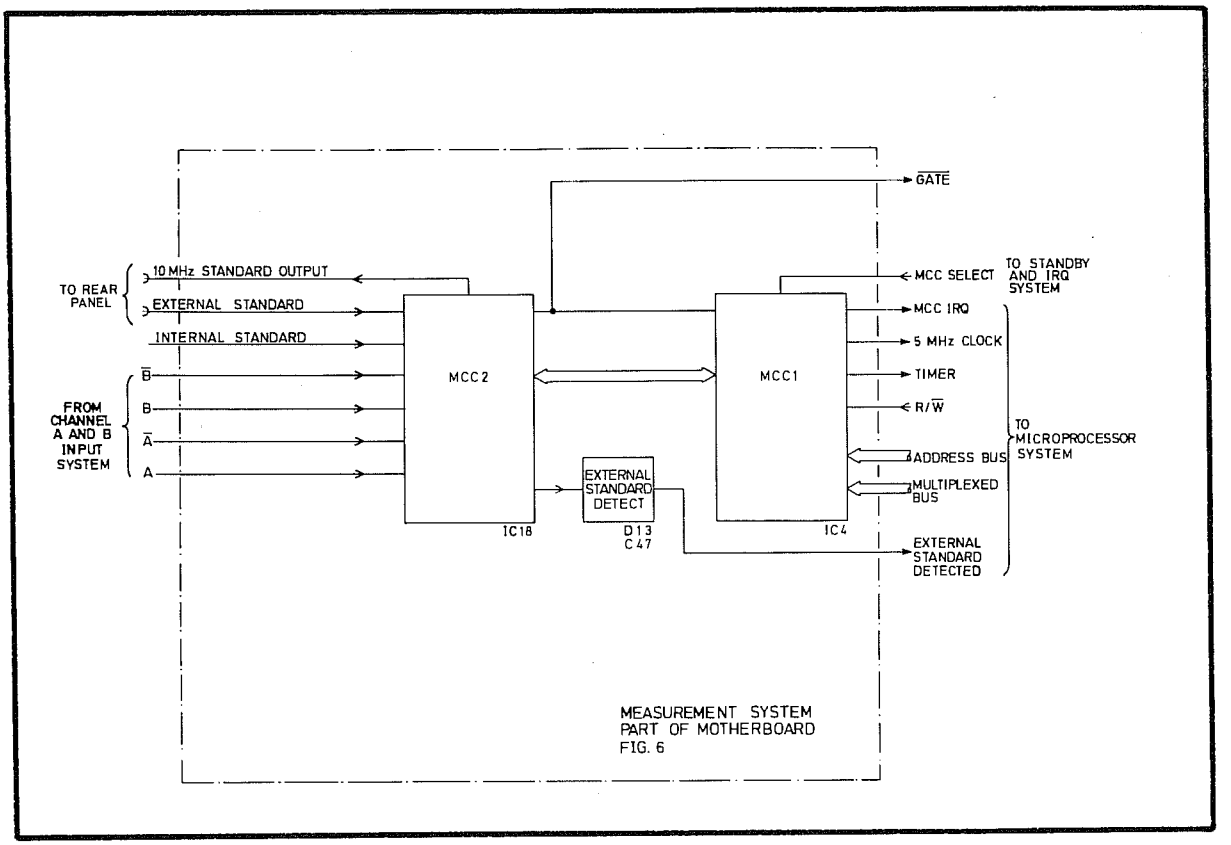


Fig 6.3 The Measurement System

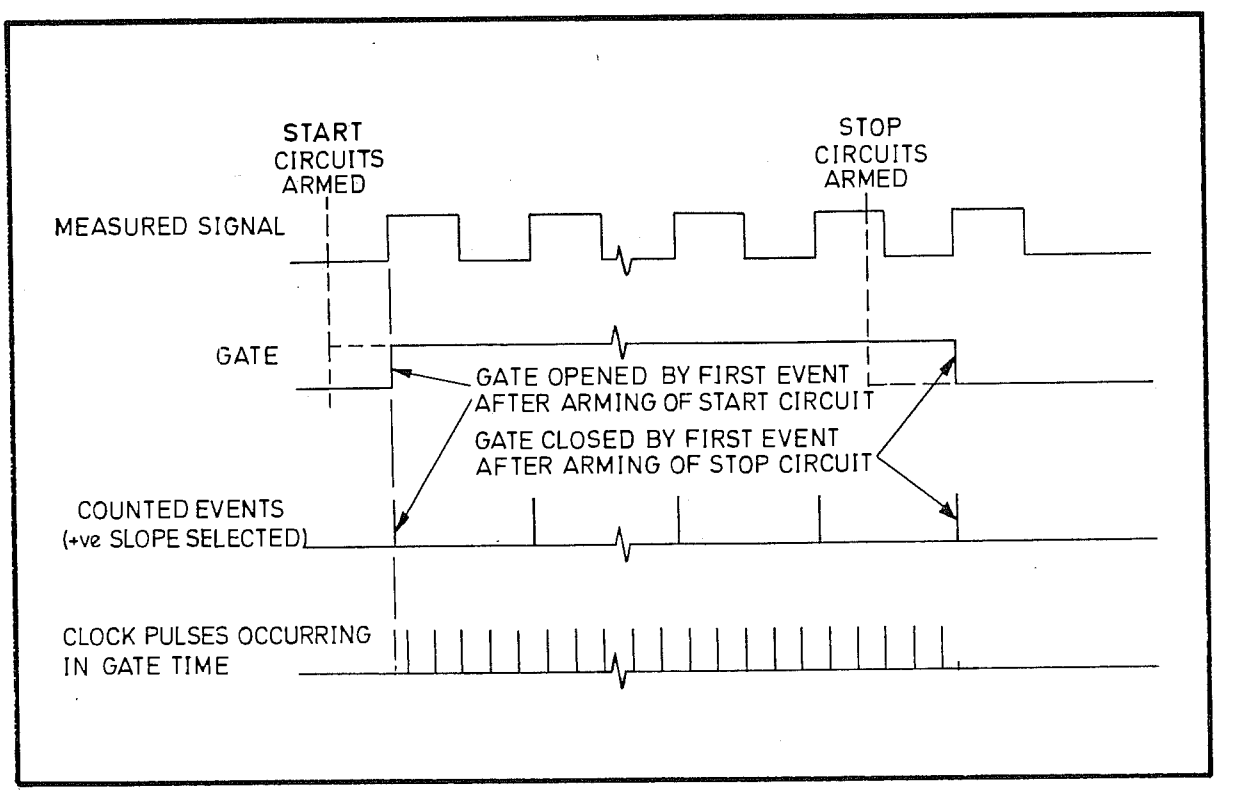


Fig 6.4 Basic Reciprocatic Counting Technique

30 At the end of each measurement period MCC1 generates an interrupt request for the microprocessor system. The registers within MCC1 are addressed using the address bus and the MCC SELECT line. The measured value is transferred to the microprocessor system via the multiplexed bus.

31 The internal and external frequency standard inputs are both fed to MCC2. The system will operate from the external standard provided that the input is of sufficient amplitude. A 10 MHz output, derived from the frequency standard in use, is made available at a socket on the rear panel when the Frequency Standard Input/Output option (Option 02) is fitted.

Circuit Description

32 The circuit diagram is shown in Fig 6 in Section 8.

Measured Signal Input

33 For all measurement functions, the differential outputs from channel A and channel B are applied to the measuring circuit at IC18/15, 16, 17 and 18.

Reference Frequency

34 The internal reference signal is applied to IC18/2 and the external reference signal, if present, to IC18/3. A buffered version of the external reference is present at IC18/24, and is applied to the detector D13/C47/R79. The detector output is fed to IC11/6, and is read periodically by the microprocessor. If the level is above the TTL logic '1' threshold, the microprocessor sets IC18/38 to logic '0' and the measurement system switches to use the external reference.

35 A 10 MHz signal, derived from the frequency standard in use, is present at IC18/37, and is fed via PL19 pin 1 to the 10 MHz STD OUTPUT socket (if fitted) on the rear panel.

36 A 10 MHz reference signal, derived from the internal frequency standard is present at IC18/36. This signal is applied to IC4/24.

Microprocessor Clock and Timer

37 A 5 MHz clock signal for the microprocessor (and the GPIB microprocessor if fitted) is taken from IC4/2. A 39.0625 kHz clock signal for the microprocessor timer is taken from IC4/4.

Control Signals

38 The logic levels on lines Q0 to Q4, between IC4 and IC18 are shown in Table 6.1. These levels are stable if no signals are applied to any of the channel inputs.

TABLE 6.1

Control Signals

Measurement	Control Line				
Function	Q0	Q1	Q2	Q3	Q4
FREQ A	1	0	1	1	0
FREQ B	1	0	0	1	0
PERIOD A	1	0	1	1	0
T.I. A→B	0	0	1	1	0
TOTAL A by B	1	0	0	1	1
RATIO A/B	1	0	1	1	1
CHECK	1	1	1	GATE	0
TOTAL A	1	0	1	1	0
TIME	1	0	1	1	0

NOTE (1) The FREQ B function is obtained with special function 21 active. (FREQ A with delay).

(2) In CHECK, Q3 will be '1' for GATE indicator on, and will be '0' for GATE indicator off.

THE DISPLAY SYSTEM

Functional Description

39 A block diagram of the system is given in Fig 6.5. The GPIB indicators, the GATE indicator, the channel A and channel B TRIGGER indicators and the STANDBY indicator are held on or off by control signals from other systems. The remainder of the display is multiplexed under the control of the display drivers.

40 To update the display, the microprocessor selects the appropriate display driver, using the MODE 1 and MODE 2 control lines. A string of nine 8-bit words (a control word and eight data words) is then put onto the bus. Each word is entered into a memory within the display driver under the control of the STROBE signal.

41 The display driver puts the data words onto its output bus in turn. For each data word, the appropriate numeric indicator or group of LEDs is enabled by a signal on its control line.

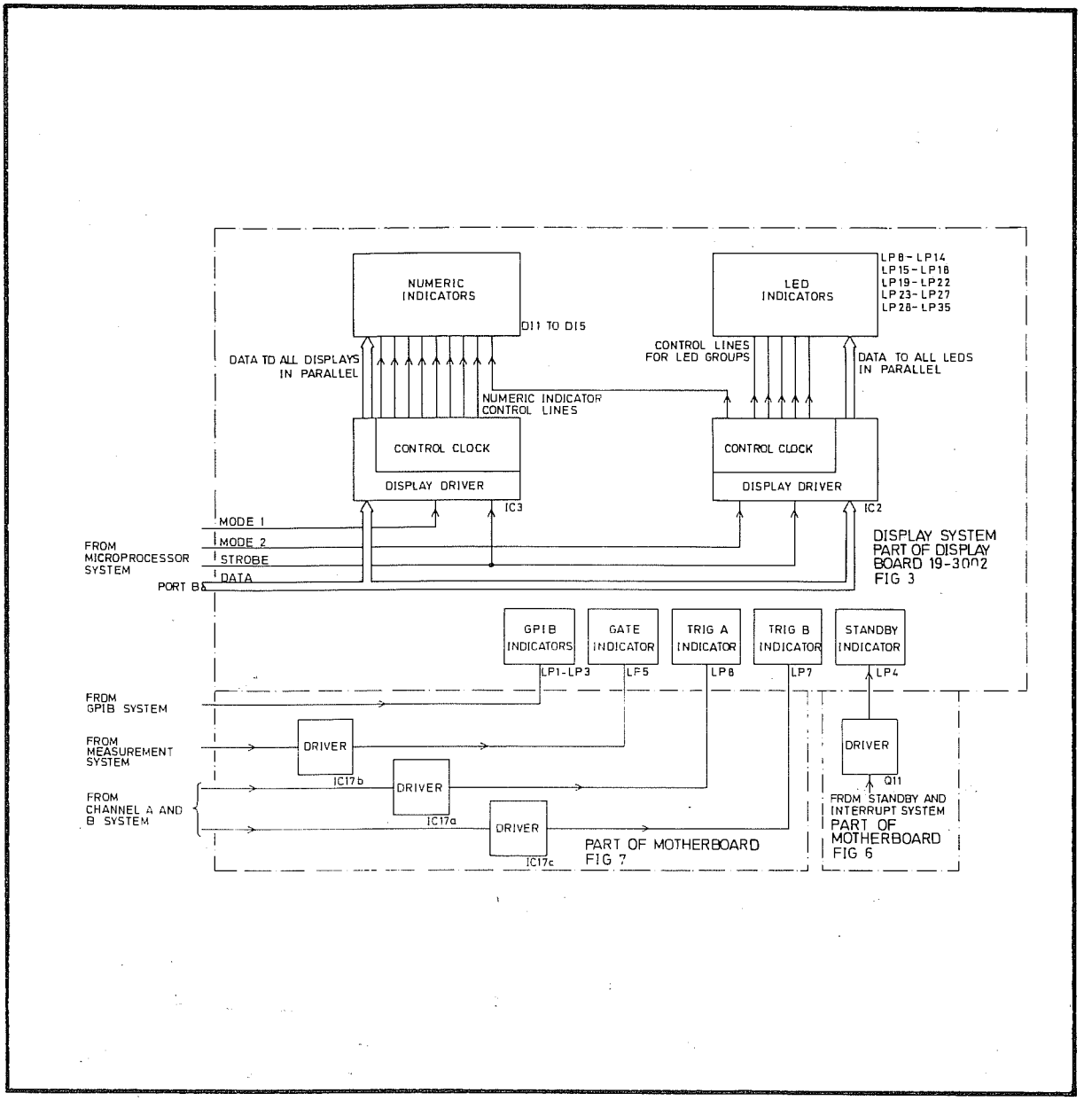


Fig 6.5 The Display System

Circuit Description

42 The circuit diagram is shown in Fig 3 in Section 8. The GPIB indicators, LP1, LP2 and LP3, are driven via SK1 from the GPIB system. The GATE indicator, LP5, is driven from the measurement system via a driver stage, shown in Fig 9, and SK2 pin 13. The TRIG indicators, LP6 and LP7, are driven from the channel A and B system via driver stages, shown in Fig 9, and SK2 pins 7 and 3. The STANDBY indicator, LP4, is driven via SK1 pin 8 from the standby and interrupt system. The remaining LED indicators and the numeric indicator DI5 are controlled by the display driver, IC2. Numeric indicators DI1 to DI4 are controlled by IC3.

43 Display data are stored in memory within IC2 and IC3. To change the data, the microprocessor puts a control word on the port B bus. The microprocessor writes this word into the display drivers by means of a negative pulse applied to the DISPLAY STROBE line at SK1 pin 4. The control word determines the operating mode of the display drivers.

44 The microprocessor then selects the display driver required by setting a logic '0' on the appropriate MODE line, at SK1 pin 3 or 6. Eight words containing display data are written into the selected display driver via the port B bus, controlled by eight negative-going pulses on the DISPLAY STROBE line.

45 The output of each display driver is multiplexed, under the control of an internal clock. Eight-bit display data (for seven segments + decimal point or eight LED indicators) are put onto the device output bus (pins 1 to 4 and 24 to 27). A positive pulse is then applied to the enablement line of the device or group of indicators which is to display the data. The enablement line waveforms consist of 500µs positive-going pulses at approximately 250 pps.

THE KEYBOARD SYSTEM

Functional Description

46 A block diagram of the system is given in Fig 6.6. The encoding of the keyboard data is performed within the system without microprocessor action. An interrupt request (IRQ) is made to the microprocessor when encoding is complete. Data transfer is initiated by the KEYBOARD ENABLE signal from the microprocessor.

47 The 18 keys are organised as a 16-key matrix and two extra keys. When a key is pressed, its position is encoded into a 5-bit word. One bit, carried on the $\overline{\text{KEYBOARD EXTEND}}$ line, indicates whether the key is in the matrix or is one of the extra keys. The remaining bits indicate the position of the key.

48 When a key is pressed, the encoder examines both the matrix and the extra keys, and generates a 4-bit code representing the key position.

49 If the key pressed is one of the extra two, the keyboard extend line is pulled low. If the key is in the main matrix the $\overline{\text{KEYBOARD EXTEND}}$ is isolated from the key line by D1, and remains at logic 1.

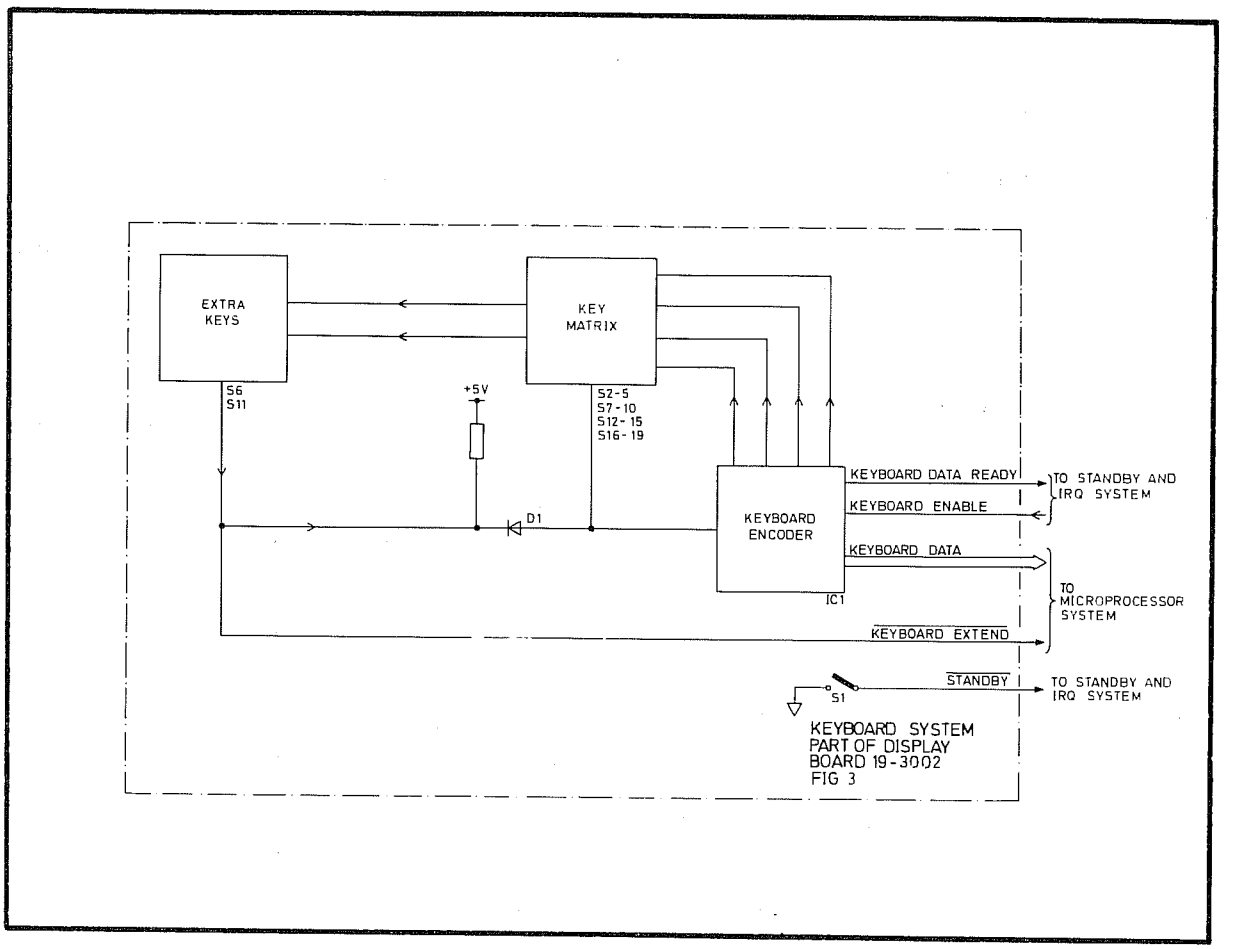


Fig. 6.6 The Keyboard System

Circuit Description

50 The circuit diagram is given in Fig 3 in Section 8. The keys are organised as a 16-key matrix and two extra keys, having common row lines connected to the encoder at IC1/7, 8, 10 and 11. The matrix has column lines, connected to IC1/1, 2, 3 and 4.

51 The encoder normally holds the row lines at logic '0'. When a key is pressed the corresponding column line is pulled to logic '0'. The encoder then scans the keyboard and stores a 4-bit code, corresponding to the row and column of the key, in an internal register.

52 The $\overline{\text{KEYBOARD EXTEND}}$ line indicates whether or not the key is in the matrix. The inputs to IC1 are normally held at logic '1', so that SK2 pin 11 is at logic '1'. If one of the extra keys (S6 or S11) is pressed, SK2 pin 11 will go to logic '0'. The column lines of the matrix are isolated from the inputs of IC1 by D1, so that the logic level at SK2 pin 11 is not changed when a key in the matrix is pressed.

53 When the key-position code has been stored, the encoder sets the KEYBOARD DATA READY line, at SK2 pin 4, to logic '1' giving a microprocessor interrupt. The microprocessor sets IC1/13 to logic '0', using the KEYBOARD ENABLE line, and the encoder puts the 4-bit code onto the bus. The microprocessor reads the code and the state of the KEYBOARD EXTEND line to find which key has been pressed.

THE MICROPROCESSOR SYSTEM

Functional Description

54 A block diagram of the system is given in Fig 6.7. The microprocessor used has a 5-bit bus for the high-order address bits and an 8-bit multiplexed bus which is used for the low-order address bits and for data. The low-order address bits are strobed into the address latch, which holds them on an 8-bit address bus, to free the multiplexed bus for data.

55 Two latches, fed from port B of the microprocessor, are used to maintain voltage levels on the instrument control lines. A third latch is used to read the status of the instrument flags via port B. The latches and registers for the connection of the multiplexed bus to the measurement system are in the measurement system, and are controlled by the MCC SELECT signal. The display data latches are in the display system, and are controlled by strobe and chip select signals obtained from port A.

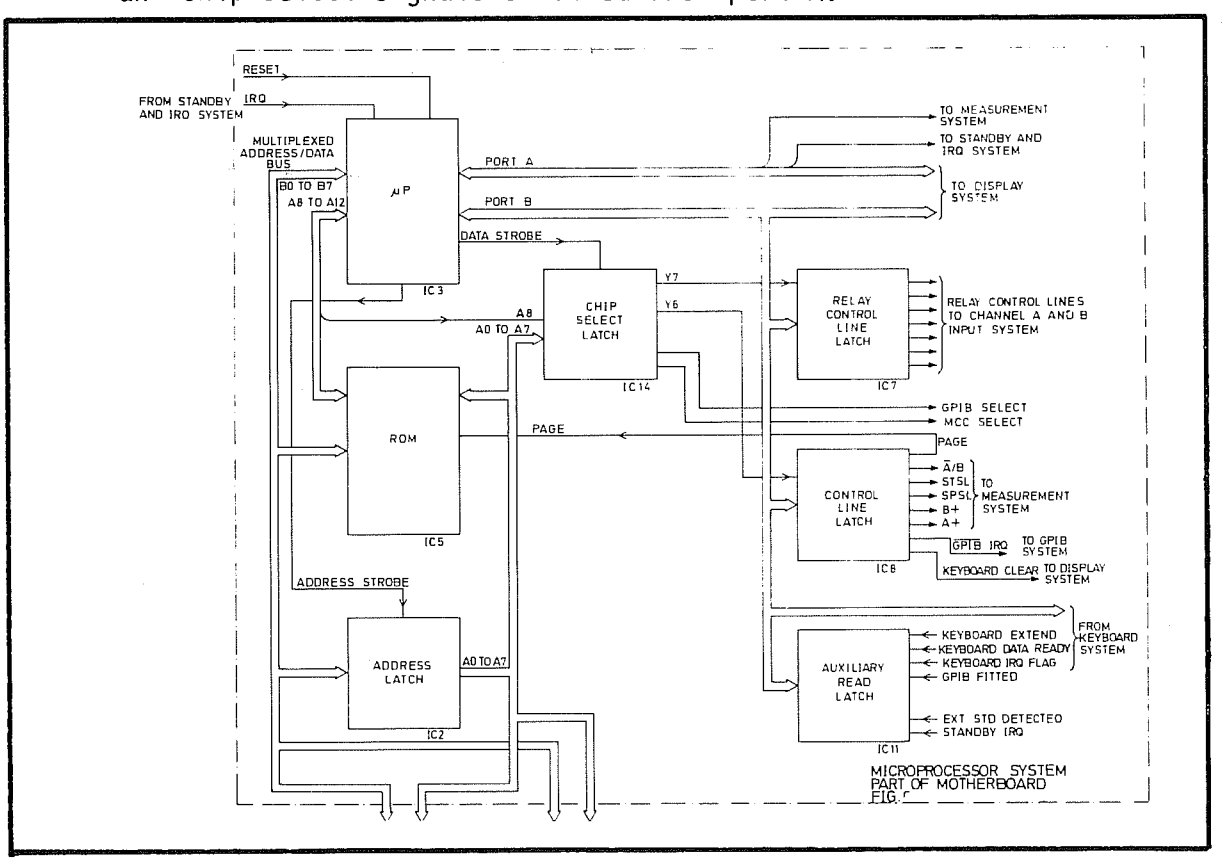


Fig 6.7 The Microprocessor System

Circuit Description

56 The circuit diagram is given in Fig 6 in Section 8. The microprocessor clock and timer signals are generated in the measurement system, and are fed to IC3/39 and IC3/37. A $\overline{\text{RESET}}$ signal is generated in the standby and IRQ system when the instrument is switched on or off, and is fed to IC3/1.

57 The microprocessor bus for the high-order address bits is designated A8 to A12. The multiplexed bus, used for the low-order address bits and for data is designated B0 to B7. The microprocessor also has two input/output ports PA0 to PA7 and PB0 to PB7.

Multiplexed Bus Operation

58 The microprocessor puts IC3/6 (ADDRESS STROBE) to logic '1' and IC3/4 (DATA STROBE) to logic '0'. This enables the address latch, IC2 (IC2/11 at logic '1') disables the ROM, IC5 (IC5/20 at logic '1') and disables the address decoder, IC14 (IC14/6 at logic '0').

59 The address is put onto lines B0 to B7 and A8 to A12. When the lines have settled the ADDRESS STROBE line is taken to logic '0'. The low-order bits of the address are latched into IC2, and are held on address lines A0 to A7. Lines B0 to B7 are now free for use as a data bus.

Address Decoding

60 The levels on address lines A6 to A8 are decoded in IC14 to provide the following outputs:

(1) $\overline{\text{MCC SEL}}$, the chip-select signal for IC4.
(2) $\overline{\text{GPIB SEL}}$, the chip-select signal for the GPIB address decoder.
(3) Y6, the chip select signal for output latch IC8.
(4) Y7, the chip select signal for output latch IC7.

61 These outputs are only available when IC14 is enabled by a logic '1' at IC14/6 and a logic '0' at IC14/4 and 5. The level at IC14/6 is set by the DATA STROBE output at IC3/4, which is at logic '1' when the multiplexed bus is available for data transfer. All outputs from IC14 are decoded from addresses with lines A9 to A12 at logic '0', when IC14/4 and 5 are held at logic '0' by the output from IC9a, b and d.

Input and Output Latches

62 The logic levels required on the instrument control lines and on the PAGE line (most significant bit of RAM address) are set into the output latches, IC7 and IC8, from data port B of the microprocessor. The latch strobe signals are decoded in IC14. Data may be read by the microprocessor from the input latch, IC11. The latch strobe signal is provided via data port A of the microprocessor.

THE STANDBY AND IRQ SYSTEM

Functional Description

63 The system generates reset signals for the microprocessor and GPIB interface, and the standby switching signal for the power supply system. It also combines the IRQ signals from the GPIB interface, the measurement system and the keyboard system for connection to the microprocessor. A block diagram is given in Fig 6.8.

64 Reset signals for the microprocessor and the GPIB interface are generated whenever power is applied to or removed from the instrument's power supply system.

65 On switching to standby, the standby signal from the keyboard system sets the standby IRQ latch. The latch outputs provide the standby IRQ and a standby flag for the microprocessor system. The standby IRQ output also clocks the standby ON/OFF latch to the set state. This provides signals to switch the power supply to standby, light the STANDBY indicator and disable IC13b, so inhibiting the other IRQs. At the end of the microprocessor interrupt routine the standby IRQ latch is reset, removing the standby IRQ. The state of the standby ON/OFF latch is not changed.

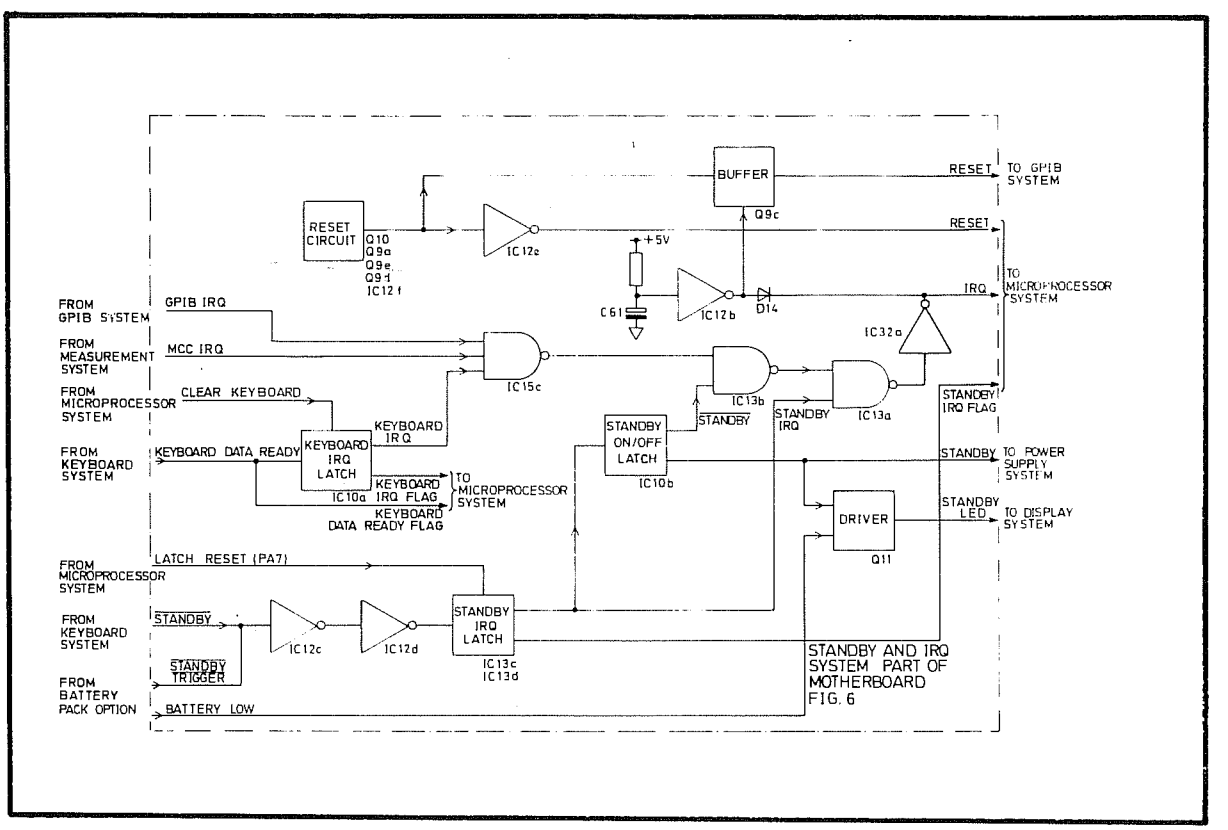


Fig 6.8 The Standby and IRQ System

66 While the instrument is in standby, the input to IC12b is held low and the IRQ input to the microprocessor is held high via D14. This inhibits all IRQs. The output from IC12b also holds the GPIB interface reset via Q9c.

67 On return from standby, the standby IRQ latch is again set by the standby signal from the keyboard system. The standby ON/OFF latch is clocked to the reset state, the power supply is returned to normal operation and IC13b is enabled. The input to IC12b rises as C61 charges, removing the reset signal from the GPIB interface and enabling the microprocessor IRQ input. The microprocessor is now able to accept the IRQ from IC13a. At the end of the restart sequence the standby IRQ latch is reset.

68 When the encoder in the keyboard system has data ready to be read by the microprocessor, the keyboard IRQ latch is clocked via the KEYBOARD DATA READY line. The latch outputs provide the keyboard IRQ and a keyboard IRQ flag. Once the keyboard has been identified as the source of the interrupt, the latch is reset by the microprocessor.

Circuit Description

69 The circuit diagram is shown in Fig 6 in Section 8.

Reset Circuit

70 The $\overline{\text{RESET}}$ signal is generated in the circuit containing Q10, Q9a, d and e, and C60. When the instrument is switched on, the input to IC12f is held low until C60 charges through R96, Q9a and R90. The output at IC12f/12 goes to logic '1' when power is applied, but drops to logic '0' after approximately 300 ms. This output is inverted by IC12e to provide the microprocessor reset and by Q9c to provide the GPIB reset.

71 If there is a reduction in the +5 V STANDBY supply, due to the instrument being switched off or to power failure, the potential across R91 falls. The potential at Q10 emitter is maintained by the charge in C60, so Q10 conducts. The current in R97 makes the base of Q9d positive, so the transistor conducts and holds the base of Q10 low until C60 is completely discharged. This ensures that a good reset action is obtained, even if the power is quickly restored.

Standby Operation

72 On switching to standby, PL1 pin 14 is taken to 0 V by the STANDBY key. Debouncing is provided by R89 and C57. The leading edge of the signal is sharpened in IC12c, C58, R93 and IC12d, and sets the standby IRQ latch, IC13c and d.

73 The negative-going output from IC13c/10 is passed via IC13a, IC12a and R101 to IC3/2, to provide a microprocessor interrupt. The positive-going output from IC13d/11 forms the standby IRQ flag (read by the microprocessor via IC11 during the interrupt routine) and clocks the standby latch, IC10b, to the set state.

74 The logic '0' level at IC10b/8 switches on Q11, and provides power for the STANDBY indicator via PL1 pin 8. The same output is applied to IC13b/5, and disables the other interrupts, which are connected to IC13b/6.

75 The logic '1' level at IC10b/9 shuts down the power supplies except the +5 V STANDBY and ±11 V supplies.

76 At the end of the interrupt routine the microprocessor resets the standby IRQ latch by applying logic '1' to IC13c/8 from IC3/7.

77 On return from standby, the standby IRQ latch is again set. This provides a microprocessor interrupt and sets the standby IRQ flag, as before. The positive-going output from IC13d/11 clocks the standby latch back to the reset state, so that the STANDBY indicator is turned off and the power supplies are restored. The microprocessor resets the standby IRQ latch at the end of the interrupt routine.

78 When the instrument is operating from the battery pack in the battery-save mode, the $\overline{\text{STANDBY TRIGGER}}$ control line (PL21 Pin 7 on Fig. 9) is taken to logic '0' after approximately one minute by the battery pack. This switches the instrument to the standby mode. The instrument is returned to the measurement mode by operation of the STANDBY key.

The IRQ Circuits

79 The KEYBOARD DATA READY line, at PL2 pin 4, goes to logic '1' when the keyboard encoder has data available. This clocks IC10a to the set state to provide a keyboard IRQ flag at IC11/11 and an interrupt signal at IC15c/9. Interrupts from the measurement system ($\overline{\text{MCC IRQ}}$) and the GPIB interface ($\overline{\text{GPIB IRQ}}$) are connected to IC15c/11 and IC15c/10.

80 If any of these interrupts occurs, IC15c/8 and IC13b/6 will go to logic '1'. Provided the standby latch, IC10b, is not set, IC13b/5 will be at logic '1' and the interrupt signal passes via IC13a and IC12a to IC3/2.

81 When the instrument is switched into or out of the standby state, the standby IRQ latch, IC13c and d, is set. The standby IRQ from IC13c/10 is fed to IC3/2 via IC13a and IC12a.

82 The circuit comprising R102, C61, IC12b and D14 disables the microprocessor interrupt input and holds the GPIB microprocessor reset line low (via Q9c) while the +5 V power supply to R102 is switched off. On return from standby, C61 charges and IC12b/4 goes to logic '0'. The microprocessor interrupt input is enabled and the GPIB microprocessor is reset. The delay in enabling the interrupts prevents the standby IRQ which occurs on return from standby from being acted upon before the power supplies are fully restored.

THE POWER SUPPLY SYSTEM

Functional Description

83 A block diagram of the system is given in Fig 6.9. The AC supply enters at a plug mounted on the rear panel, and passes via a fuse and RFI filter, mounted on the motherboard, to the line switch.

84 The switched supply is connected to the primary winding of the power transformer via the operating voltage range selector. This has the form of a plug-in printed circuit board, which is positioned according to the line voltage.

85 The transformer has a tapped secondary winding, which supplies two rectifiers.

86 The rectifiers feed regulators providing +11.2 V, -11.2 V, +5 V, +5 V and -5.2 V. Alternatively the raw supplies can be supplied by the Battery Pack Option, if fitted. The -5.2 V regulator and one of the +5 V regulators, which supply most of the instrument's circuits, are shut down by a signal from the microprocessor system when the instrument is switched to standby.

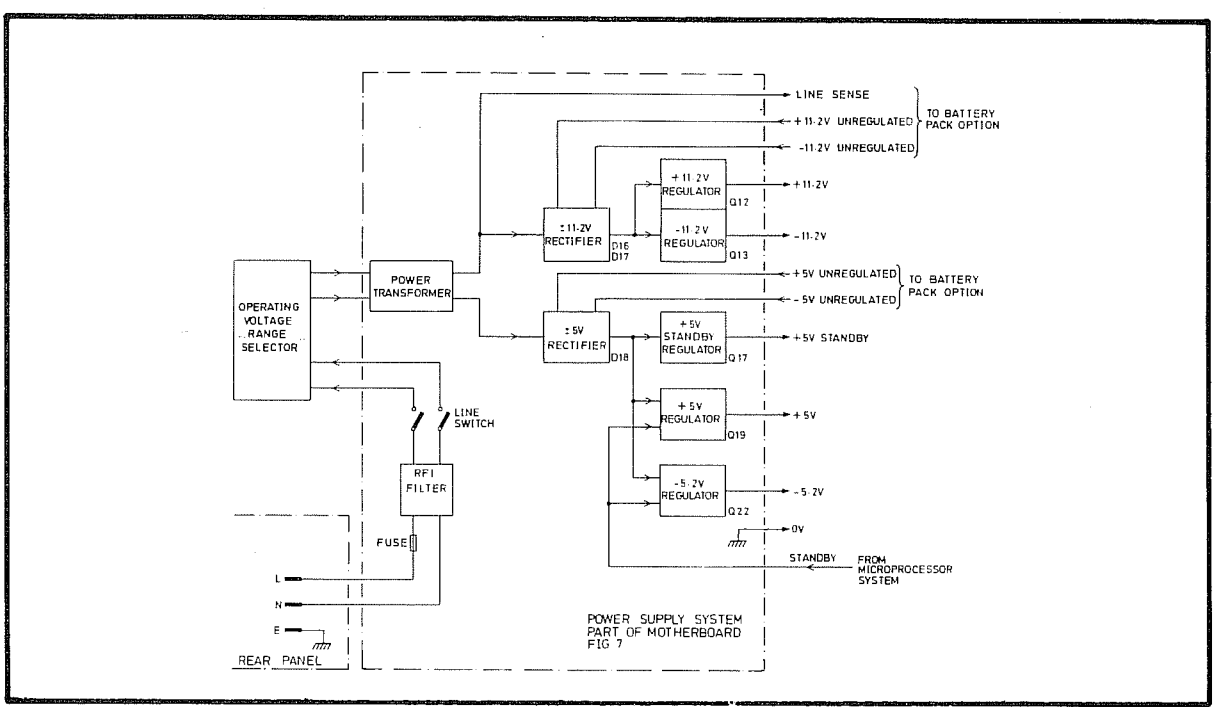


Fig 6.9 The Power Supply System

Circuit Description

87 The circuit diagram is shown in Fig 7 in Section 8. AC power connected at the power input plug passes via fuse FS1 and the RF filter, formed by L8, L9, C66, C68, and C69, to the POWER switch, S1b. The switched supply is connected to the primary windings of T1 via the tracks of a printed circuit board, which is inserted in SK8.

88 The secondary windings of T1 supply the ±5 V rectifier, D18, C76 and C77, and the ±11 V rectifier, D16a, D16b, D17a, D17b, C74 and C75. When the battery pack is in use, raw DC supplies at ±5 V and ±11 V are provided via PL21.

89 Regulated supplies at ±11.2 V are provided by zener diodes D19, D20 and emitter followers Q12 and Q13.

90 Regulated supplies at +5 V are provided by two discrete component regulators having series elements Q17 and Q19. The non-inverting inputs to the comparators, IC1c and IC1a, are fed from the zener diode D22, which is operated at an appropriate current to give a 5 V reference voltage. The outputs of the +5 V rails are separately compared to this reference to control the regulators via Q18 and Q20.

91 A regulated supply at -5.2 V is provided by a discrete component regulator having Q22 as its series element. The comparator inputs are held at approximately 0 V. The potential divider controlling the inverting input is connected across the +5 V and -5.2 V rails.

Standby Mode

92 When the instrument is switched to standby, the standby latch, IC10b on Fig 6, is clocked to the set state. The base of Q15 is pulled high, and IC1a/3 is pulled low. The base of Q20 is pulled low by IC1a, the base current of Q19 is cut off and the regulator is shut down. When the voltage of the +5 V rail falls, IC1b/6 goes more negative. The base of Q21 is taken towards 0 V by IC1b, so that the base current of Q22 is cut off and the -5.2 V regulator is shut down.

THE FREQUENCY STANDARD SYSTEM

Functional Description

93 The basic frequency standard and the TXCO option are 10 MHz oscillators, whereas frequency standards 9423 and 9444 each comprise a 5 MHz oscillator and a frequency doubler. A block diagram of the 9423 and 9444 oscillators is shown in Fig 6.10.

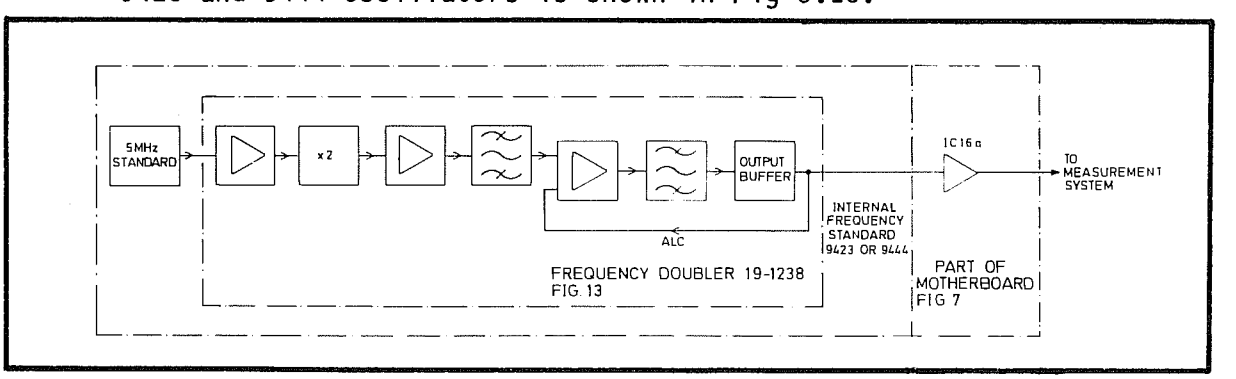


Fig 6.10 9423 and 9444 Oscillators

94 For all oscillator types the 10 MHz signal is passed to the measurement system via a buffer on the motherboard.

95 Signals from an external frequency standard are applied to a signal conditioning circuit on the motherboard. If a 10 MHz external frequency standard is used, the output of this circuit may be connected directly to the measurement system. For external frequency standards at sub-multiples of 10 MHz, the external frequency multiplier option is fitted between the conditioning circuit and the measurement system.

Circuit Description

Frequency Doubler

96 The circuit diagram of the frequency doubler, used with frequency standards 9423 and 9444, is given in Fig 13 in Section 8. The 5 MHz input is applied to the balanced amplifier containing Q1 and Q2. The base of Q3 is driven by the differential outputs from the amplifier, via D1 and D2, so that the frequency here is 10 MHz.

97 The 10 MHz signal is amplified and filtered in the two stages containing Q3 and Q5, and fed to pin 3 via the buffer, Q6.

98 The output signal is fed back via C6 to switch Q4 on during the positive peaks of the signal. The gain of Q5 is controlled by the potential across C3, which charges via R12 and discharges via Q4. If the output signal increases, the time for which Q4 conducts increases so that the mean potential across C3 decreases. The resulting decrease in gain of Q5 provides automatic level control.

Internal Frequency Standard Buffer

99 The buffer circuit is shown in Fig 7 in Section 8. The 10 MHz input at PL14 pin 5 is shaped and buffered in IC16a, before being fed to the measurement system at IC18/2. The inverting input of IC16a is connected to the bias voltage at IC16/11.

100 The basic frequency standard OSC1 is supplied with power via LK1 and PL14 pins 1 and 2. If any other frequency standard is fitted, LK1 is removed, cutting off power to OSC1. The frequency standard signal then passes via PL14/5 and C67 to the buffer IC16a.

External Frequency Standard Buffer

101 The buffer circuit is shown in Fig 7 in Section 8. The signal connected to the EXT. STD. INPUT socket on the rear panel is fed to PL20 pin 4. Protection against excessive signal amplitude is provided by D15a, D15b and R111.

102 The buffer comprises IC16b and IC16c. The inverting inputs are connected to the bias voltage at IC16/11. The second stage has feedback connected via R118 to give a Schmitt trigger action.

103 The differential output of the second stage is fed to PL16 pins 6 and 9 for use in the reference frequency multiplier option. If the option is not fitted, LK2 is fitted between pins 8 and 9 of PL16 to connect the signal to the measurement system at IC18 pin 3.

THE REFERENCE FREQUENCY MULTIPLIER (OPTION 10)

Functional Description

104 The block diagram of the multiplier is given in Fig. 6.11. The input to the circuit is taken from the EXT STD INPUT socket on the rear panel, via a signal conditioning circuit on the motherboard. The output of the circuit is passed to the measurement system. The $\overline{\text{BYPASS}}$ control line is held at logic '1' by the +5 V STANDBY supply.

105 The circuit contains a 10 MHz oscillator operating in a phase-locked loop. If an external reference signal of suitable amplitude is present at the EXT. STD. INPUT socket, a rectangular waveform at the reference frequency is fed to the external reference detector. The detector output triggers the switching signal generator. The oscillator is then enabled and the bypass logic connects the 10 MHz from the buffer and splitter to the output.

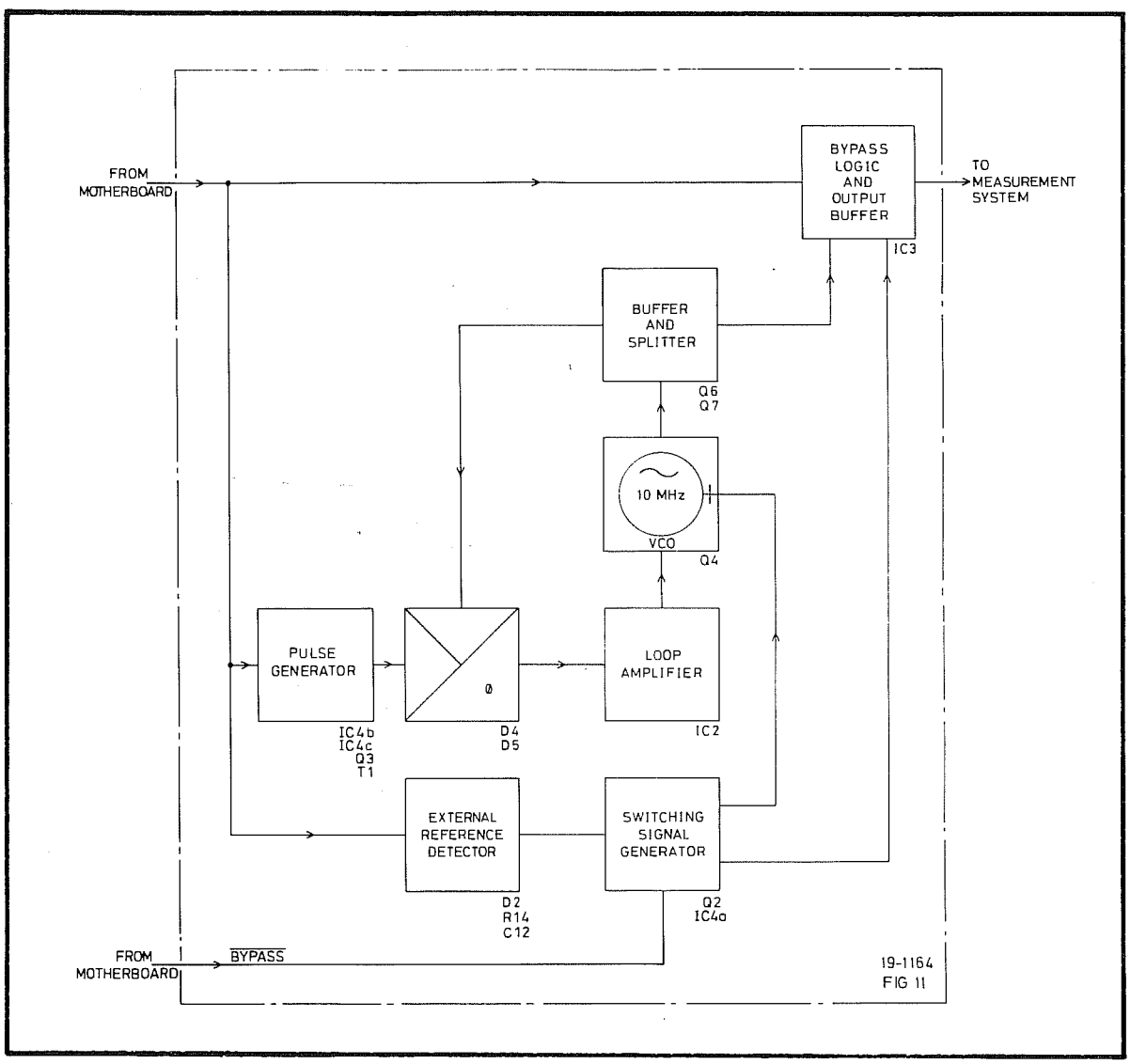


Fig. 6.11 The Reference Frequency Multiplier

106 The pulse generator output is fed to the phase detector, and forms the reference signal for the phase-locked loop. The phase detector is of the sampling type, allowing the oscillator to be phase-locked to a reference signal of 10 MHz or any sub-multiple of 10 MHz.

107 If no external reference signal of suitable amplitude is present at the EXT. STD. INPUT socket, the reference detector output does not trigger the switching signal generator. The oscillator is disabled and the bypass logic connects the circuit input to the output.

Circuit Description

108 The circuit diagram is given in Fig. 11 in Section 8.

Input Circuit and Pulse Generator

109 Two antiphase waveforms derived from the external reference signal enter the system at SK16 pins 6 and 9. The waveform from pin 9 is converted from ECL to TTL levels in Q1 and squared in IC4d before being applied to the pulse generator, IC4b and IC4c. The operation of this circuit is illustrated in Fig. 6.12.

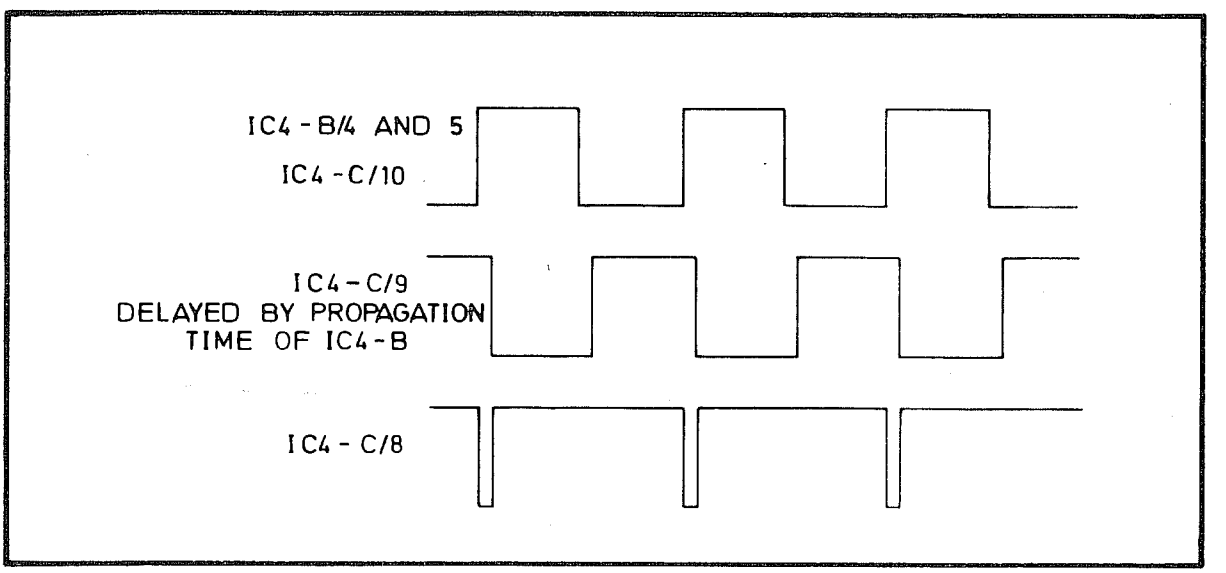


Fig. 6.12 Pulse Generator Waveforms

110 The negative-going pulses at IC4c/8 are used to switch Q3, which drives the transmission-line type transformer, T1. The transformer acts as a phase splitter, so that, for the duration of each pulse from IC4c/8, the sampling bridge of the phase detector is held forward biased, with the D4A/D5A and D4B/D5B junctions symmetrical about 0 V.

The Phase-Locked Loop

111 The loop oscillator active element is Q4. The oscillator frequency is controlled by the crystal XL1 and the varactor diode D1. The trimming capacitor C2 can be adjusted to compensate for a range of crystal and varactor tolerances.

112 The oscillator output drives a unity-gain cascode buffer, Q6/Q7. The buffered signal from the collector of Q7 forms the RF input to the phase detector.

113 When the sampling bridge of the phase detector is forward biased by the pulses from T1, the D5A/D5B junction adopts the same potential as the D4A/D4B junction. At other times the junctions are isolated from each other by the high impedance of the non-conducting diodes. The bridge output is therefore a series of samples of the loop oscillator waveform, taken at the frequency of the external frequency standard.

114 The phase detector output depends upon the relative frequency of the loop oscillator and the frequency standard, and upon the phase of the loop oscillator waveform at the instant of sampling. If the standard frequency is 10 MHz every cycle of the loop oscillator output is sampled, but if it is a sub-multiple of 10 MHz only every second, fourth, fifth or tenth cycle will be sampled. In all cases, however, provided the standard frequency is an exact sub-multiple of the loop oscillator frequency, the samples will be of constant amplitude. If the standard frequency is not an exact sub-multiple of the loop oscillator frequency the output pulses will be amplitude modulated.

115 The amplitude of each phase detector output pulse depends upon the instantaneous value of the loop oscillator waveform at the instant of sampling. The pulses are integrated in C7 to form the input to the loop amplifier IC2. When the loop is in lock the voltage across C7 maintains the voltage at IC2/6, and therefore across the varactor, at the level needed to maintain the loop oscillator at the lock frequency.

External Reference Detector and Bypass Switching

116 The output from IC4d/11 is fed to a detector formed by D2, C12 and R14. If no external reference signal is present at the EXT. STD. INPUT socket, SK16 pin 9 is held low, Q1 conducts and IC4d/11 is at logic '1'. The detector output, and therefore the base of Q2, is at +5 V and Q2 is switched off. A logic '0' level is applied to IC4a/2, giving a logic '1' at IC4a/3 and the base of Q5. The zener diode, D3, converts the logic levels from TTL to the level required to switch Q5. R8 and R9 provide ECL logic levels for IC3b and c.

117 With Q5 switched on the voltage across R4 holds the emitter of Q4 positive with respect to its base, disabling the oscillator. At the same time a logic '1' level taken from the junction of R8 and R9 is applied to IC3b/7 and IC3c/11. This disables IC3c and enables IC3a, so that the oscillator output line is open circuited and SK16 pin 6 is connected to SK16 pin 5 and 8 via IC3a and IC3d.

118 When an external reference signal is present at SK16 pin 9 the output from IC4d/11 is a TTL square wave at the external reference frequency. The detector output holds the base of Q2 negative, so that Q2 conducts and IC4a/2 is at logic '1'. Since IC4a/1 is held at logic '1' by +5 V at SK17 pin 4, IC4a/3 is at logic '0'. Under

these conditions Q5 is cut off and the loop oscillator is enabled. A logic '0' is applied to IC3b/7 and IC3c/11 from the junction of R8 and R9. This disables IC3a and enables IC3c, so that the oscillator output is connected to SK16 pins 5 and 8 via IC3c and IC3d.

THE GPIB INTERFACE (OPTION 55)

Introduction

119 The GPIB interface is a self-contained, microprocessor controlled system. It handles the transfer of data between its internal memory and the GPIB without involvement of the main instrument microprocessor. Data transfer is made one byte at a time, each transfer being controlled by the IEEE-488 handshake protocol. The circuit diagram is given in Fig 9 in Section 8.

120 The microprocessor $\overline{\text{RESET}}$ signal is derived from the standby and IRQ system. The clock signal is derived from MCC1, IC18, shown in Fig 8 in Section 8.

121 The microprocessor uses a multiplexed bus, the eight low-order bits being used for both address and data. The low-order address bits are put onto the bus first, and are latched into IC11 by the address strobe. The bus is then free for data use.

122 Data transfer between the microprocessors is initiated by an interrupt, and is controlled by a 3-wire handshake protocol. The transfer is in the form of a data string, the number of bytes in the string being indicated by the first byte.

Address Setting and Recognition

123 The microprocessor reads the settings of the address switches in switchbank S1, via its port B inputs, approximately every 1 ms and writes the settings into an address register within the general purpose interface adapter (GPIA) IC12.

124 When the interface address is set on the bus by the controller, it is recognised by the GPIA by comparison with the contents of the internal address register.

Reading From the Bus

125 When the interface is addressed to listen, the GPIA conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point IC12/27 is at logic '0', givng a logic '1' level at IC18d/11. This puts three of the bilateral switches in IC13 to the conducting state, so completing the RFD line. The logic '0' at IC12/27 also puts the buffers in IC14 and IC15 to the receive condition. Data from the bus enters the GPIA data-in register, and IC12/40 goes to logic '0' to provide an interrupt request to the microprocessor, IC9.

126 The microprocessor interrupt routine establishes the reason for the interrupt. The address decoder, IC8, is enabled via IC6c, IC6d, IC7a, IC7b and IC7c, using address lines GA7, 9, 10, 11 and 12. The decoder is addressed using lines GA4, 5 and 6, and gives the GPIA enable signal at IC8/15. The data-in register of the GPIA is addressed using the R/$\overline{W}$ line and lines GA0, 1 and 2. The microprocessor then reads the contents of the data-in register and transfers the data to memory.

127 When the data-in register has been read, the GPIA cancels the interrupt request and allows the data accepted (DAC) line to go high. The handshake routine then continues, and a further byte, if available is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

Writing to the Bus

128 When the GPIA is addressed to talk its internal data-out register will normally be empty. Under these conditions IC12/40 goes to logic '0' and provides an interrupt request to the microprocessor.

129 IC17a is in the reset state, giving a logic '1' at IC18d/12. Since IC12/27 is at logic '1' when the GPIA is addressed to talk, IC18d/13 is also at logic '1'. The resulting logic '0' at IC18d/11 open circuits three of the bilateral switches in IC13 to break the RFD line. The fourth bilateral switch conducts, due to the logic '1' at IC19c/10, and holds IC12/18 at 0 V. Even if the listening device asserts that it is ready for data, IC12 will not attempt to load the contents of the data-out register onto the bus.

130 The microprocessor interrupt routine establishes the reason for the interrupt. The microprocessor then enables the address decoder, IC8, via IC6c, IC6d, IC7a, IC7b and IC7c, using address lines GA7, 9, 10, 11 and 12. The decoder is addressed using lines GA4, 5 and 6, and gives the GPIA enable signal at IC8/15. The data-out register of the GPIA is addressed using the R/$\overline{W}$ line and lines GA0, 1 and 2, and a data byte is written into the register. The GPIA then cancels the interrupt request.

131 Following the data transfer, the microprocessor sets IC17a, using line PB7, to give a logic '0' at IC18d/12. This gives a logic '1' at IC18d/11, which enables three bilateral switches in IC13 and connects the RFD line. The fourth switch in IC13 is disabled, so releasing IC12/18 from 0 V. When the listening device asserts that is is ready for data, the GPIA loads the contents of the data-out register onto the bus and continues with the handshake routine.

132 When the data-out register has been read, the GPIA generates a further interrupt request. The microprocessor resets IC17a, using line PB6, giving a logic '1' at IC18d/12, so that the RFD line is again broken at IC13. The data transfer and data transmission sequence is then repeated.

Serial Poll

133 The status byte register of the GPIA is normally updated approximately every 1 ms by the microprocessor. When the interface is addressed to talk following the receipt of the serial poll enable (SPE) message, the GPIA puts the status byte onto the bus without further action by the microprocessor.

134 When the serial poll is completed, the controller sends the serial poll disable (SPD) message, which is detected by IC6a, IC6b, IC7d, IC18a and IC19b. The resulting logic '1' at IC17a/3 clocks IC17a to the reset condition, and gives a logic '1' at IC18d/12.

Data Transfer Between Microprocessors

135 Data transfer between microprocessors is made using the multiplexed data bus on both devices. Connection between the buses is made by means of a D-type latch, IC1 or IC2, depending on the direction of data transfer. All data transfers are initiated by the sending device. The first byte indicates the number of bytes to be transferred.

136 For data transfer to the GPIB microprocessor, the instrument microprocessor sets PL4 pin 22 ($\overline{\text{GPIB DATA IRQ}}$) low. This provides an interrupt request (IRQ) to the GPIB microprocessor via IC4d. As part of the interrupt routine, IC8 is enabled and addressed to give an enabling signal for IC5d. The microprocessor reads the IRQ flag via IC5d and data bus line 7 to establish that the IRQ is from the instrument and not the GPIA.

137 The GPIB microprocessor prepares to receive data, and then enables and addresses IC8 to give a signal which clocks IC16a via IC20b. The level set on line 0 of the data bus is transferred to IC16/5, and forms the ready for data (RFD) signal to the instrument microprocessor.

138 The instrument microprocessor enables and addresses IC3 to give an enabling signal to IC5c, reads the RFD signal, puts the first data byte on the bus and readdresses IC3 to give a clock signal which latches the data into IC1. It then addresses IC3 to give a clock signal for IC16b, so that the logic level set at IC16b/12 is transferred to IC16b/9 to form the data valid (DAV) signal to the GPIB microprocessor.

139 The GPIB microprocessor addresses IC8 to give a signal to enable IC5a, and reads the DAV signal via data bus line 6. It then cancels its RFD signal, addresses IC8 to give an output enable signal for IC1 (via IC20c) and reads the data. A data accepted (DAC) signal is sent via IC2 and the RFD signal is reset. The instrument microprocessor responds by cancelling its DAV signal and entering the next data byte into IC1. Data transfer continues in this manner until the required number of bytes have been received.

140 Data transfer from the GPIB microprocessor to the instrument processor follows a similar pattern. The IRQ signal is passed from port A line 0 via IC18b and IC4c. The IRQ flag is read by the instrument microprocessor during its interrupt routine, via IC5b (enabled by an output from IC3). The IRQ signal is cancelled by the instrument microprocessor setting data bus line 0 to logic '0' and then addressing IC3 to clock IC17b. The resulting logic '0' at IC17b/9 disables IC18b.

141 During data transfer from the GPIB interface to the instrument, the RFD signal is passed via IC16b and IC5a, the DAV signal via IC16b and IC5c, the DAC signal via IC1 and the data via IC2.

THE BATTERY PACK (OPTION 07)

Functional Description

142 The battery pack option allows the counter to be supplied from a +12 V internal battery pack (part of this option) or from an external DC supply. The output from the option is only partially regulated. Fine regulation is done on the motherboard in the normal way.

143 The option is based on a switch-mode flyback converter. It includes a charging circuit for the internal batteries, a battery condition monitor, and other circuits to maintain the charge and optimise battery life.

Flyback Converter

144 This type of switch-mode DC-DC converter relies for its operation on switching a direct current repeatedly on and off, at high frequency, through the primary of a flyback transformer. The resultant AC from the secondaries is rectified to produce a range of DC levels. Output levels are controlled by feedback to the switching circuit.

145 In the block diagram of the option, shown in Fig 6.13, direct current, from either the internal battery pack or an external DC supply, passes through the primary of the flyback transformer and through a transistor switch to ground.

146 Switching occurs at a frequency of approximately 40 kHz. Current is first switched on, allowing the magnetic field around the primary to build up. The current is then switched off and the collapsing field transfers its energy to the secondary windings. Secondary voltages are rectified and filtered to provide ±11.2 V UR, +5 V UR and -5.2 V UR.

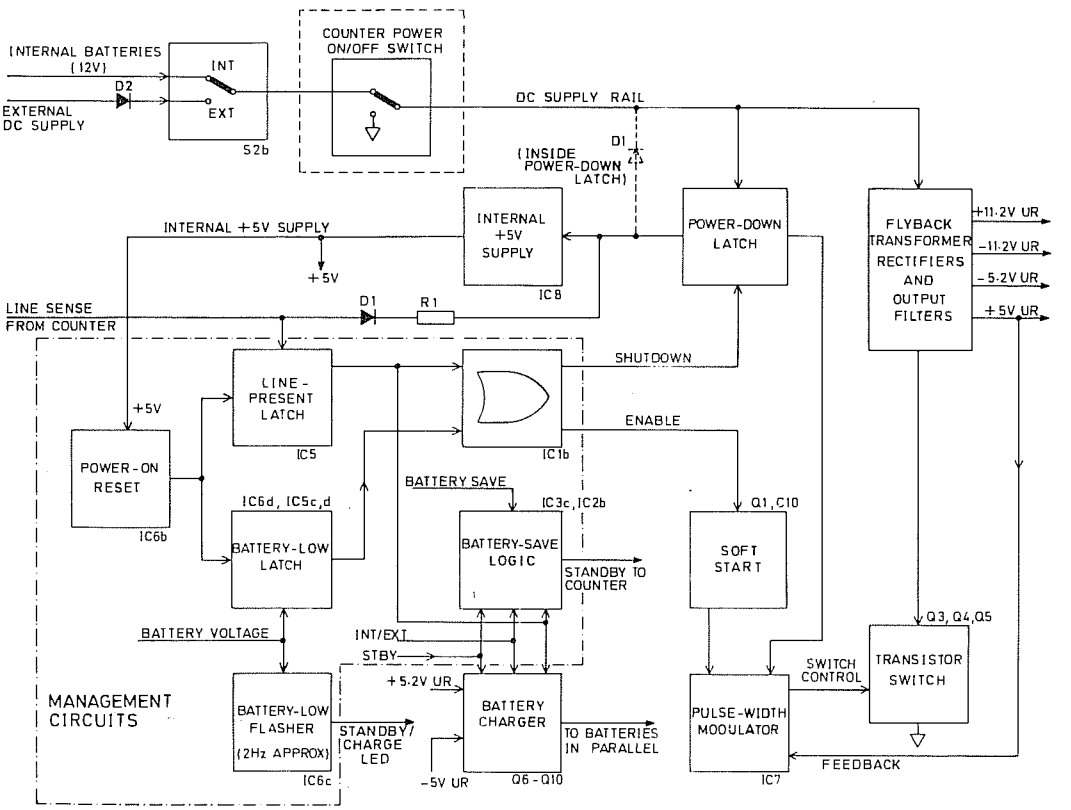


Fig 6.13 The Battery Pack

Feedback

147 For normal loads, the switching duty-cycle is such that the transformer core never has time to saturate, so the power transferred to the secondaries is proportional to the on time of the transistor switch. In the pulse-width modulator, the level of the +5 V output is compared with a reference voltage. If the +5 V is low, the on time of the switch is increased, and if it is high, the on time is reduced. Note that the switching frequency remains constant. Only the duty-cycle is changed.

148 At higher load levels, the duty-cycle is such that the secondary current does not have time to decay to zero between switching pulses. Therefore, the core still retains some energy at the end of the cycle. This means that the next on-time does not have to be increased to provide the extra power. Hence, beyond a certain load current, transistor on-time remains essentially constant. On-time will increase for a few cycles, however, at the instant the load current increases.

149 Feedback is taken from the +5 V UR rail because this has the heaviest load. Each of the other output levels is essentially governed by the ratio of its secondary turns to those of the +5 V UR secondary.

Soft Start

150 At switch-on, the +5 V output would initially be zero. Therefore the feedback circuit just described would create a large current surge. To prevent this, soft start circuitry ensures that the Q5 on pulses are initially very short, and are only gradually increased to normal. Soft start is enabled by a signal from the management circuits.

Power-Down Latch

151 This is essentially an on/off switch for the pulse-width modulator and for a +5 V regulator. It is on when the counter is being powered by the battery pack or an external DC supply. It is switched off when the battery is low (auto-shutdown), and when the counter is being powered from an AC (line) supply.

Management Circuits

152 Control of the battery-pack option, and its response to control switches and to variations of AC or DC supply levels is managed by the management circuits. These are identified in the block diagram.

Line Sense

153 When the counter is being powered from line, an AC signal is available on the line sense input. This is used to operate the line present latch, which disables the pulse-width modulator via the power-down latch.

Battery Low/Auto-Shutdown

154 The battery voltage is monitored by the battery-low latch and the battery-low flasher. If the voltage falls to around +11 V the STBY/CHRG LED on the front panel is flashed at 2 Hz. After approximately 15 minutes further operation, when the voltage has fallen to around 10.1 V, the battery-low latch will be set and the option will be shut down by the power-down latch.

Battery-Save Facility

155 If the battery-save facility is selected, the battery-save logic will switch the counter into standby mode one minute after it has been enabled.

Internal +5 V Supply

156 The control logic (management circuits) of the option need an independent +5 V supply. This is provided by a +5 V regulator.

157 When the counter is using an AC supply, the regulator is powered by a DC voltage derived from the line sense input. When one of the DC inputs is being used, the regulator is supplied by the DC supply rail via the power-down latch.

Power-On Reset

158 When power is switched on, +5 V is applied to the power-on reset circut. This circuit provides a pulse that resets the line-present and battery-low latches. If there is no AC input on line sense, the power-down latch will be cleared and the soft-start circuit enabled.

Battery Charging

159 The option includes a battery-charger capable of fully-charging a battery-pack within 14 hours, and a trickle-charger designed to top-up a previously charged battery.

Battery Charger

160 This circuit can only be enabled when the counter is powered from the line or from an external DC supply. The charger is powered from the +5 V UR and -5.2 V UR rails, and is enabled by the STBY signal from the STBY/CHRG button.

161 The +12 V battery-pack is formed by two +6 V batteries connected in series. When the charger is enabled, an internal relay configures the two batteries in parallel.

Trickle-Charging

162 Whenever the counter is powered from line, rectifier circuit D1/R1 derives a DC voltage from a 40 V peak-to-peak signal on the line sense input. This supplies approximately +14 V to the DC supply rail via D1 in the power-down latch. If the internal battery is selected, the DC supply rail provides a trickle-charge to top up the battery. Diode D2 prevents the external DC supply from being charged in this way.

Technical Description

163 The circuit of the battery-pack assembly is shown in Fig 6.17.

Power Sources

163 Option power can be supplied from line, from a external DC supply or from the battery pack.

165 When the counter is powered by line, a 40 V peak-to-peak, 50 Hz signal is applied to LINE SENSE at SK21-15. This is rectified by D1 to produce approximately 14 V DC. The voltage is fed via D1 (in the switch board assembly) to the DC supply rail. In the absencce of a line supply the internal battery pack or an external DC supply can be selected at S2.

166 In the EXT position, a DC supply plugged into JK1 is connected via SK21-3 and 4, S1a and SK21 pins 21 and 22, to the DC supply rail.

167 In the INT position of S2, the battery pack in connected to the DC supply rail by the same route.

Switching Circuit

168 Whenever IC7 is enabled, a nominal 40 kHz square wave signal at Pin 9 switches driver transistors Q3 and Q4 on and off in turn. (The totem-pole arrangement provides a fast switching action). This switches MOSFET Q5 on and off in time with the signal on IC7/9. The switching signal is derived from an internal oscillator, the frequency of which is controlled by the value of C13.

Flyback Transformer

169 Each time Q5 is switched off, the field generated around the primary winding collapses, generating a voltage in each of the secondaries. The polarity is such that the points marked with a dot will be negative.

170 The voltages are additive. They are rectified and filtered by D7-D10 and C16-C19 to produce ±11.2 V UR, +5 V UR and -5.2 V UR supplies. These are further regulated on the motherboard.

Level Control

171 A voltage proportional to the +5 V UR level is developed across R30 and connected to the error input (IC7/7) of the pulse-width modulator. The input is compared with the level of an internal reference voltage. The duty cycle of the signal at IC7/9 is modified accordingly.

172 R28 modifies the feedback level, allowing the controlled level to be set precisely.

Soft Start Circuit

173 R26 and C11 form a feedback-loop stability network for the circuit that compares reference and feedback levels. Shunting these components has the same effect as an increase in the +5 V UR level. This effect is used to produce a soft start at switch-on. The sequence is as follows.

174 When the switch-mode circuits are not operating, a high on IC1b/13 disables IC7 via the power-down latch and maintains Q1 in the conducting state, holding the base of Q2 at 0 V.

175 When IC1b/13 goes low, IC7 is enabled and Q1 is switched off, allowing C10 to charge via R24.

176 As its base voltage rises, Q2, which will initially conduct heavily, is gradually switched off, allowing IC7/8 to gradually adopt its own level, thus allowing the pulse-width modulator to operate normally.

Power-Down Latch

177 When there is no line supply, the +5 V regulator for the management circuits is powered by the DC supply rail, via the power-down latch. A power-up circuit formed by Q3, R8, R9 and C2, ensures that the latch is always opened at power-up. Once the management circuits are enabled, the latch condition will depend upon the logic signals generated by the management circuits.

178 At power-up, the base of Q3 is held low, switching on Q3 while C2 charges. The voltage developed across R7, switches on Q1, which in turn switches-on Q2, Q4 and Q5.

179 Q2 latches Q1 on by maintaining current through R7 and R4. Thus the circuit remains latched on when C2 is charged and Q3 switched off.

180 Q5 connects the DC supply rail to Vcc on IC7.

181 Q4 connects the DC supply rail to the +5 V regulator IC8, thereby energising the management circuits.

182 Unless the line supply is on, or the DC supply rail is low, the latch will remain open. However, if one of those conditions exists, a high on ICb/13 will drive the base of Q1 low, and thus break the connection between the DC supply rail, and IC7 and IC8. In this state the current drain on the DC supply rail will be almost nil.

Trickle-Charge Circuit

183 The 40 peak-to-peak line sense signal is rectified by D1/R1. This provides approximately +14 V DC to supply the +5 V regulator, and to trickle-charge the battery-pack (via D1 in the power-down latch).

Full-Charge Circuit

184 The charger circuit is powered by the +5 V UR and -5.2 V UR rails. When the counter is using the line supply, the two rails will be supplied from circuits on the motherboard, otherwise they will be supplied from the switch-mode circuits.

185 It is only possible to enable the charger when a line supply or an external DC supply is being used. When the internal +12 V supply is selected the charger is disabled by a ground on S2a.

186 The charger is enabled when STDBY goes high, generating a high on IC3d/11. This switches on Q6 and the constant current circuit formed by D11, Q7, R34 and RLA.

187 RLA1-RLA4 connect the two +6 V batteries, in parallel, between the -5.2 V UR rail and the cathode of D15.

188 To provide temperature stability, it is necessary to make the charger voltage vary with temperature at a rate of approximately -8 mV/^{o}C. This is done by using the base-emitter junction of Q8 (-2 mV/^{o}C) as a temperature sensor, and then multiplying the sensor voltage by four.

189 The circuit comprising Q8, IC4a, R40, Q9, Q10, D15, R41 and R38 performs the multiplication. IC4a adds the result to a reference voltage from the wiper of R36, which provides adjustment of the charger output voltage, nominally set at +7.63 V at 25^{o}C.

190 The required stable voltage for the reference divider chain R45, R36 and R37 is provided by D13 and R35.

191 Power transistor Q10 provides the current required to charge the batteries. As the charger current passes through R1, a voltage proportional to the current is developed across it. Part of this voltage, tapped across voltage divider R43/R44, is fed back to limit the charging current to 1 A. The feedback voltage, at the inverting input of IC4b, is compared with a fixed voltage developed across reference diode D11. A high voltage across R1 will reduce the base voltage of Q9, thereby reducing the current through Q10 and the batteries.

192 D15 prevents the batteries from becoming discharged due to fault conditions.

Line Sense Circuit

193 The presence of the 40 V peak-to-peak signal is detected by R8, R9, D5, D6, IC5a and IC5b.

194 R8 and R9 attenuate the signal, D5 and D6 limit it to +5 V and 0 V.

195 IC5a and IC5b form the line present latch, which is set by the first rising edge on I5b/6. Thus providing a high on IC1b/12 and IC3a/1. The line present latch will remain set until the unit is switched off.

Battery Low Indication and Auto-Shutdown

196 Battery voltage is monitored by IC6c via potential divider R10-R13. If the battery drops below approximately 11 V, IC6c will turn on the oscillator formed by IC3b and IC2d. The output of this oscillator (which is high when disabled) is then EXORed with the STBY signal and its output used to flash the STBY/CHRG led at approximately 2 Hz.

197 If the battery falls to below approximately 10.1 V, the output of IC6d (Battery-Down comparator) goes high and sets the battery-low latch (IC5c and d), giving a logic high at IC5c/10. This trips the power-down latch into the off state via IC1b and IC6a, shutting down the converter and reducing battery drain to almost nil.

NOTE:
With the internal battery selected, the battery-low indicator will start flashing approximately 15 minutes before the power-down latch disables the unit.

Power-On Reset Circuit

198 At power-up, the non-inverting input of IC6b rises to around 3.3 V. The inverting input, however, is held lower as C6 charges.

199 While its inverting input is low, IC6b/1 is high, clearing the battery-low and line present latches. Once C6 is charged, IC6b/1 will change state, allowing the latches to be controlled by the line-present and battery-low voltages.

Standby/Battery-Save Operation

200 Successive depressions of the STBY/CHRG button operate a bistable circuit on the motherboard. In the set state this puts the counter into standby mode and asserts STDBY at SK21 pin 16. In the clear state, the counter is put into normal operation mode and the STDBY line is at logic '0'. Control of the bistable circuit, and the effect of the STDBY signal, is modified by the NORMAL/BATTERY SAVE and EXTERNAL/INTERNAL switches.

201 When powered from an AC line (IC3a/1 high) or an external battery (IC3a/2 high), the STBY/CHRG button enables and disables the charger as previously described. When STBY is high, SK21 pin 7 is low. This drives the STBY LED, which in this case is used as a charging indicator. $\overline{\text{STBY TRIG}}$ is disabled at IC1a/2.

202 When powered by the internal battery both inputs to IC3a are low. This disables the charger and removes the disable from IC1a/2. In this case, the STBY/CHRG button is used to enable and disable the standby mode, and the STBY LED is used as a standby indication. The standby function is modified by the state of the NORMAL/BATTERY SAVE switch as follows:

(1) When S1 is in the NORMAL position, $\overline{\text{STBY TRIG}}$ is disabled at IC1a/5. If STDBY is asserted the unit is in standby mode and the STBY LED is on. If STDBY is negated, the unit is in normal operating mode and the STBY LED is off.

(2) When S1 is switched to the BATTERY SAVE position, IC3c/9 and IC1a/5 will go low. If STDBY is in its high sate, these changes will have no effect. However, if STDBY is low or is subsequently toggled to its low state, IC1a/3 will go low and IC3c/10 will go high.

(3) C2 transfers this high to IC2b/5, causing a high on IC2b/4. This has no effect on IC1a/4, which is clamped to +5 V by D3.

(4) As C2 charges, the current through R6 will fall exponentially, until after approximately 1 minute, IC2b/5 will fall below threshold level, taking IC1a/4 low.

(5) With all its inputs low, IC1a asserts $\overline{\text{STBY TRIG}}$, which toggles the standby bistable on the main unit (hence the STDBY signal), putting the counter into standby mode and lighting the STBY LED.

(6) Subsequent operation of the STBY/CHRG button will put the counter back into the normal operating mode, and initiate another one-minute cycle.

INTRODUCTION

1 This section is written in six parts, which relate to:

(1) Test equipment required.

(2) Dismantling and reassembly.

(3) Special functions for diagnostic purposes.

(4) Fault finding.

(5) Setting up instructions for use after repair, or if the instrument fails the overall performance verification.

(6) Overall performance verification procedure.

TEST EQUIPMENT REQUIRED

2 A complete list of the test equipment required to carry out the procedures described in this section is given in Table 7.1. The items required for each operation are listed at the start of the relevant instructions.

3 A particular model of test equipment is recommended in some cases, but other equipment having the required parameters given in Table 7.1 may be used. Although the procedures to be followed are given in general terms, they are based on the use of the recommended test equipment. Some modification to the procedure may be necessary if other test equipment is used.

DISMANTLING AND REASSEMBLY

Introduction

4 Instructions for dismantling and reassembling the instrument are limited to those areas where special care is needed or difficulty may be experienced.

WARNING: LETHAL VOLTAGE
DANGEROUS AC VOLTAGES ARE EXPOSED WHEN THE INSTRUMENT IS CONNECTED TO THE AC SUPPLY WITH THE COVERS REMOVED. SWITCH THE INSTRUMENT OFF AND DISCONNECT THE SUPPLY SOCKET FROM THE REAR PANEL BEFORE CARRYING OUT ANY DISMANTLING OR REASSEMBLY OPERATION.

TABLE 7.1

Test Equipment Required

Item	Description Recommended Model	Required Parameters
1	Signal Generator Racal-Dana 9087	Low phase noise. Frequency range 10 kHz to 120 MHz Output level 1 mV to 1 V 10 MHz INT STD OUTPUT.
2	Oscilloscope with X1 Probe and X10 Probe	Bandwidth 50 MHz
3	Digital Multimeter Racal Dana 4002A	Frequency range: DC to 10 MHz Level: 20 mV to 20 V ±0.1%.
4	Frequency Standard Racal-Dana 9475	10 MHz Accuracy better than ±3 parts in 10^{10}.
5	Audio Oscillator Racal-Dana 9083	Frequency range: 10 Hz to 5 kHz Level: 30 mV into 50 Ω
6*	High Resolution Counter Racal-Dana 1991	9 digits resolution in 1 second With 10 MHz external standard input connector.
7	Connecting Leads	50 Ω coaxial cable with BNC connectors. Length 1.5 m max.
8	T-piece	BNC, 50 Ω
9	Coaxial Load	BNC, 50 Ω
10 +	GPIB Controller HP-85	
11 +	GPIB Analyzer Racal Dana 488	
12	Trimming Tool	
13 #	Multimeter (Quantity 2) AVO 8 Mk II	DC current range: 0 to 2 A
14 #	Power Supply Racal-Dana 9232	Voltage range: 0 to 16 V Output current: 2 A
15 #	Test Lead	Red and black leads, 2.1 mm coaxial jack to bare ends. Red lead to coaxial jack centre conductor.

NOTES: # Only required if battery pack (Option 07) fitted.

* Only required if ovened oscillator options 04A or 04B fitted.

\+ Only required if GPIB option fitted (Option 55)

Instrument Covers

5 (1) Disconnect the power input socket from the rear panel.

(2) Remove the two screws securing the rear panel bezel: remove the bezel.

(3) If the handles are fitted, peel off the adhesive trim patch from both handles. Remove the two screws securing each handle: remove the handles and spacers.

(4) Remove the top cover by sliding it to the rear of the instrument.

(5) Remove the bottom cover by sliding it to the rear of the instrument.

6 To replace the covers, follow the reverse of the above procedure. Ensure that the top cover is fitted with the access holes towards the front of the instrument, and that the tongues on the ends of the covers are fitted under the edges of the front panel and rear bezel.

Front Panel

7 (1) Remove the instrument covers.

(2) Remove the clamping collars from the channel A and channel B inputs. A suitable slotted screwdriver is included in the Customer Service Support Kit.

(3) Remove the two screws securing the front panel to the side frame at both sides of the instrument.

(4) Ease the front panel forward until the display board disconnects from the motherboard at PL1 and PL2.

8 To replace the panel, follow the reverse procedure. Pass the POWER switch button through the aperture in the panel before securing the panel.

Rear Panel

9 (1) Remove the instrument covers.

(2) If the TCXO frequency standard is fitted, remove the screws securing it to the rear panel. Pull the PCB assembly upwards until the board disconnects from the motherboard at PL14.

(3) Remove the two screws securing the rear panel to the side frame at both sides of the instrument.

(4) Ease the panel away from the instrument to disconnect assembly 19-3003, if fitted, from the motherboard at PL19 and PL20.

(5) If an ovened frequency standard is fitted, disconnect the flying lead from PL14.

(6) Remove the nut and crinkle washer securing the rectifier bridge, D18, to the panel.

(7) Disconnect the green/yellow lead connecting the rear panel stud to the power input plug.

10 To replace the panel follow the reverse of the above procedure.

WARNING: LETHAL VOLTAGE
THE GROUNDING OF EXTERNAL METALWORK OF THE INSTRUMENT DEPENDS UPON THE CONNECTION BETWEEN THE REAR PANEL STUD AND THE POWER INPUT PLUG. ENSURE THAT THE GREEN/YELLOW LEAD IS CORRECTLY CONNECTED DURING REASSEMBLY.

Display Board

11 (1) Remove the instrument covers.

(2) Remove the front panel.

(3) Prise the caps off the trigger level control knobs, and loosen the collets securing the knobs to the control shafts. Remove the knobs and washers.

(4) Remove the three screws securing the display board to the front panel.

(5) Unsolder the loops of wire that connect the trigger level output terminals to the display board at terminal numbers 4 and 8. Straighten the wires to enable the board to be lifted clear of the front panel.

12 To replace the display board, follow the reverse of the above procedure. Ensure that the trigger level knob caps are fitted with the white line correctly oriented.

SPECIAL FUNCTIONS FOR DIAGNOSTIC PURPOSES

13 The special functions listed in Table 7.2 are provided for use during maintenance.

TABLE 7.2

Special Functions

Function No (GPIB)	Function + Key (front panel)	Special Function
20	FREQ A	Normal operation
21	FREQ A with DELAY	Frequency B
70	CHECK	10MHz check
71	CHECK with RECALL	LED check

Special Function 21

14 Special function 21 enables frequency to be measured via channel B when the FREQ A function is selected. From the front panel, it is activated by holding down the DELAY key for about 3s, until the DELAY LED lights.

Special Function 70

15 Special function 70 provides measurement of the 10 MHz internal frequency standard, and verifies operation of the microprocessor system, MCC1, and MCC2.

Special Function 71

16 Special function 71 exercises all the LEDs, except STANDBY, GATE, TRIG A, TRIG B, REM, ADDR and SRQ, at approximately 0.5 Hz. If the GPIB interface is fitted, the REM, ADDR and SRQ indicators light.

FAULT FINDING

17 A guide to fault location is given in the flow charts of Fig 7.1 to Fig 7.8. The charts provide a logical procedure for localising the fault to an area of circuit. When using the charts it is essential to begin at the start point in Fig 7.1 or Fig 7.6 and act according to the results of each decision box met in turn. Starting part way through any chart is unlikely to lead to satisfactory fault location.

18 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	2
Digital Multimeter	3
Coaxial Lead	7
GPIB Controller	10
GPIB Analyzer	11

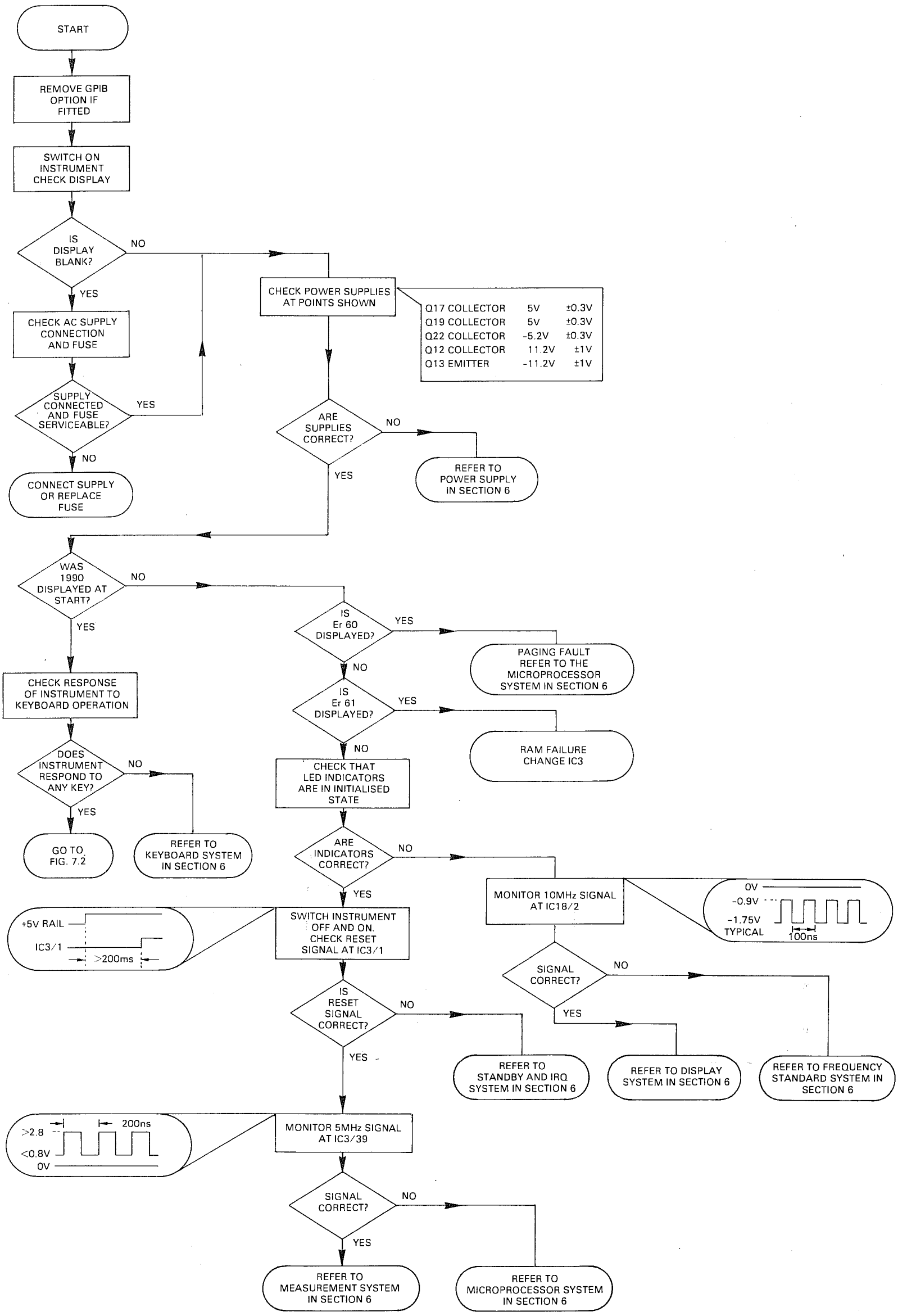


Fig 7.1 Fault Finding Flowchart - Part 1

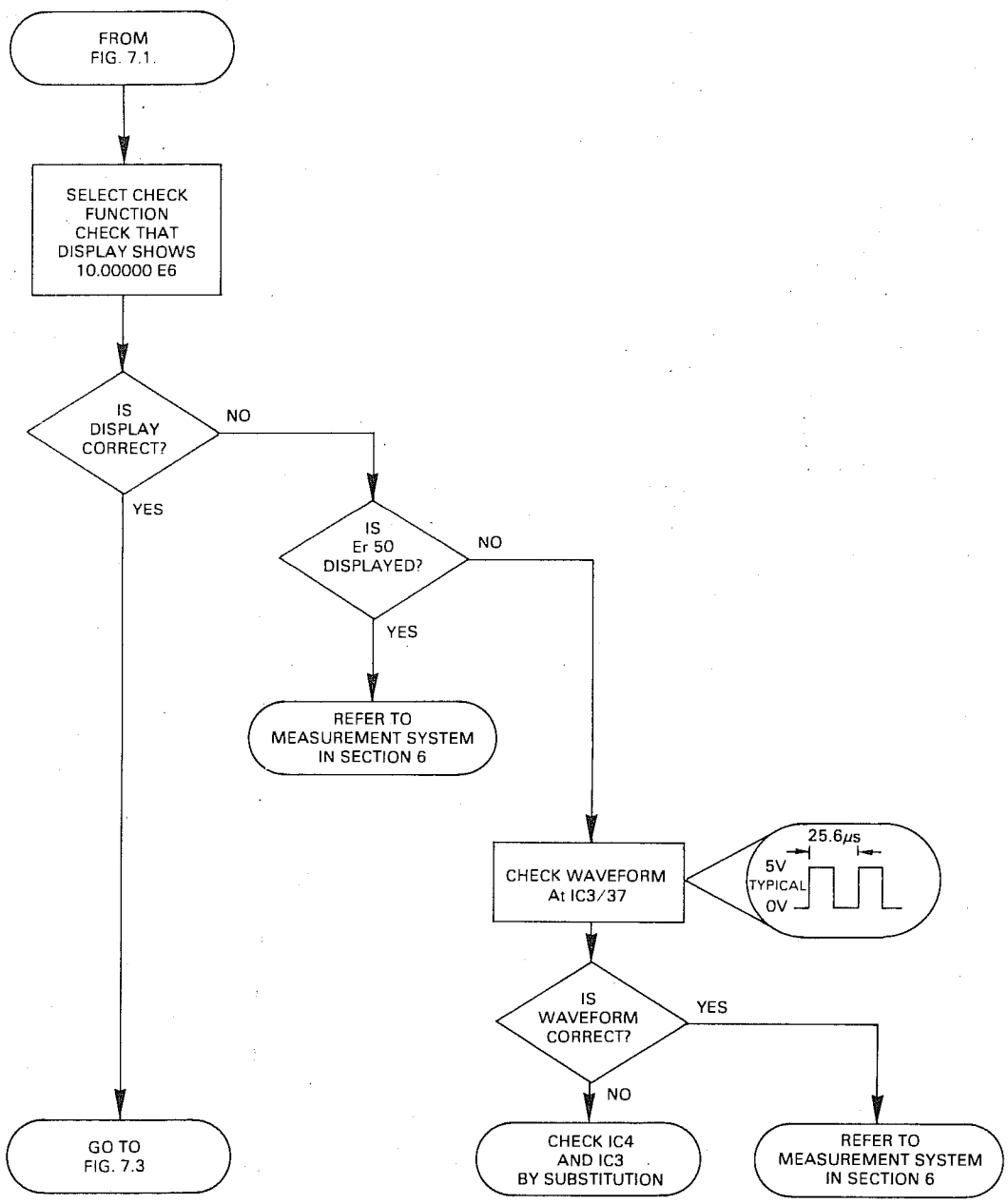


Fig 7.2 Fault Finding Flowchart - Part 2

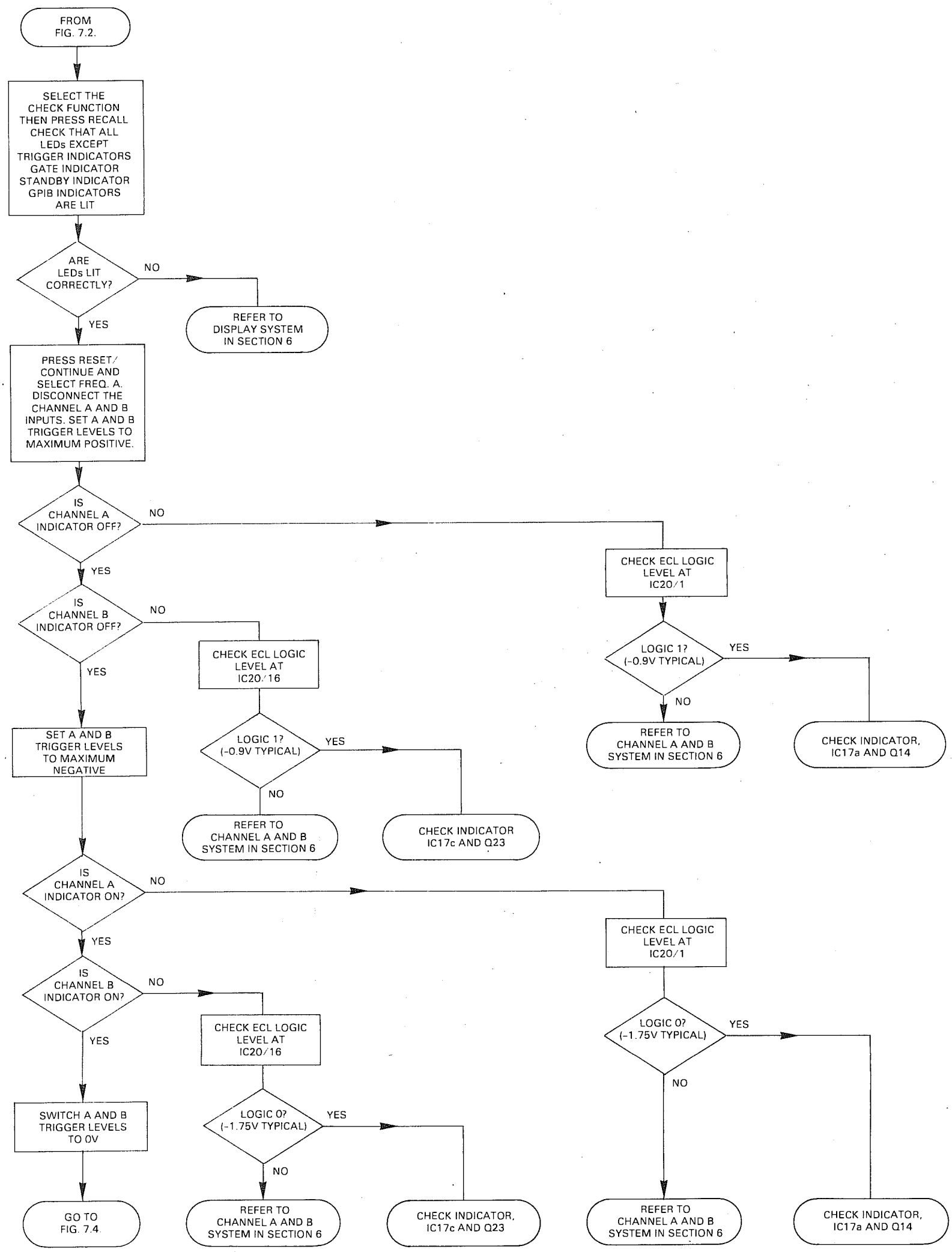


Fig 7.3 Fault Finding Flowchart - Part 3

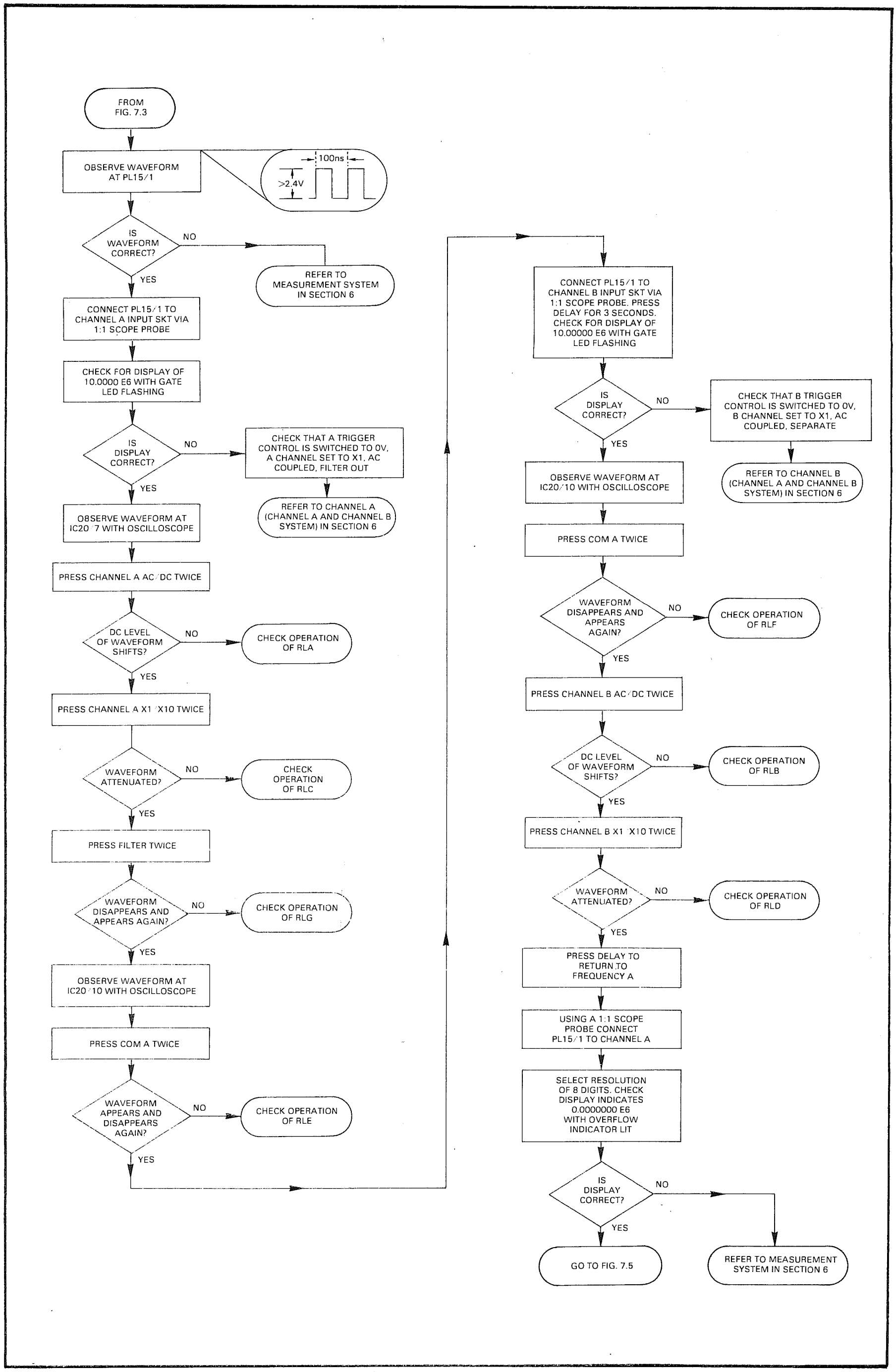


Fig 7.4 Fault Finding Flowchart - Part 4

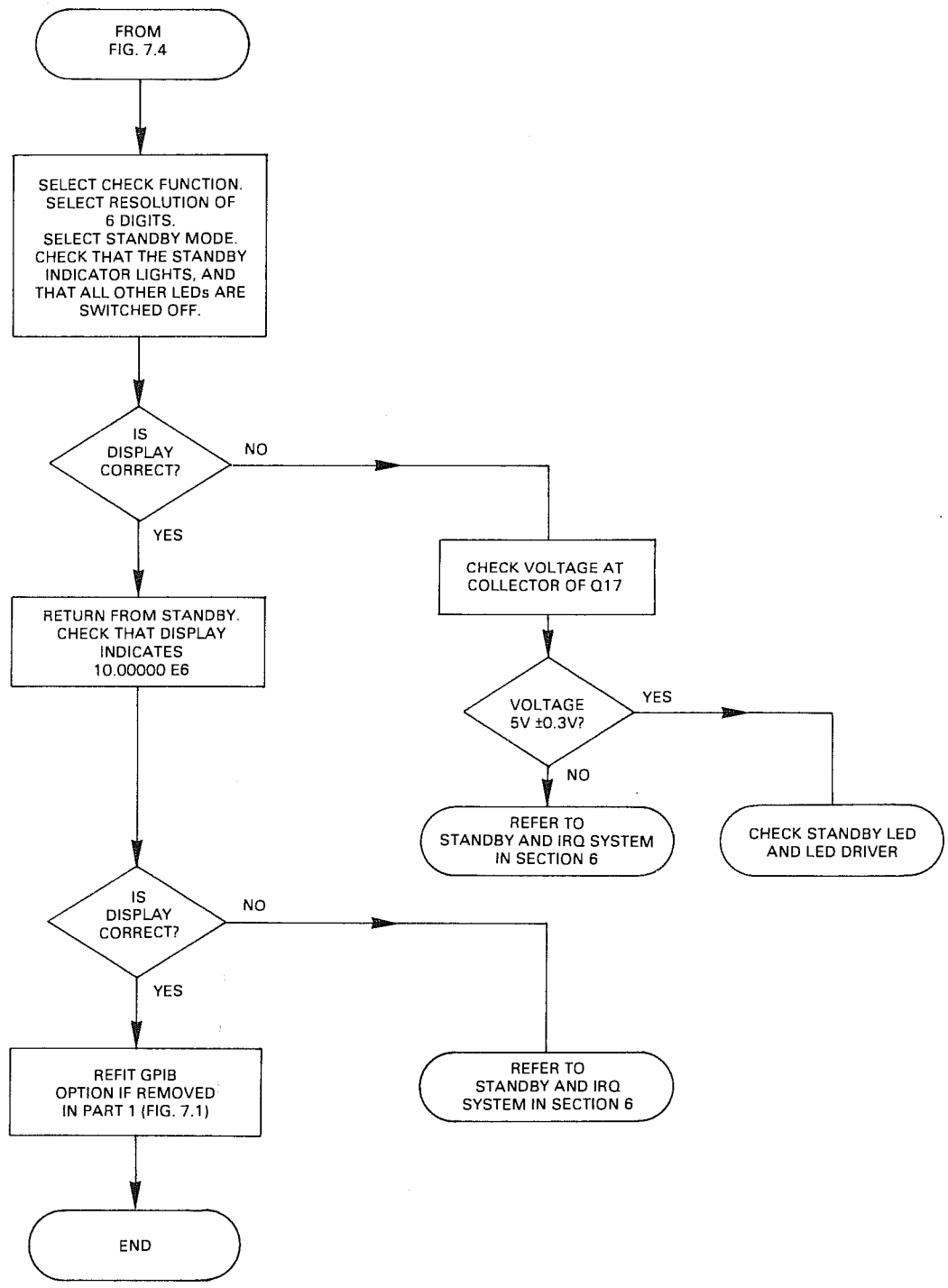


Fig 7.5 Fault Finding Flowchart - Part 5

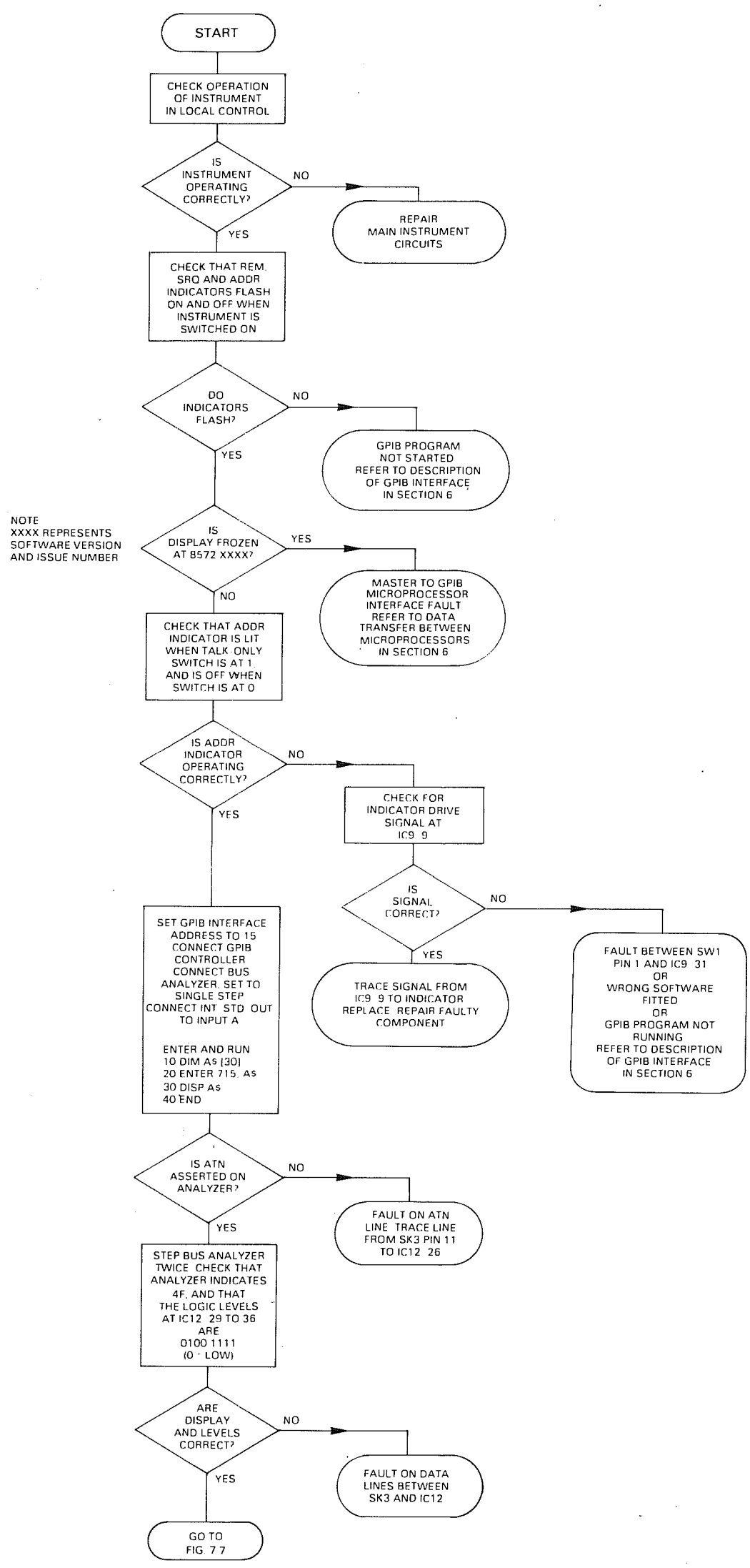


Fig 7.6 Fault Finding Flowchart - GPIB Part 1

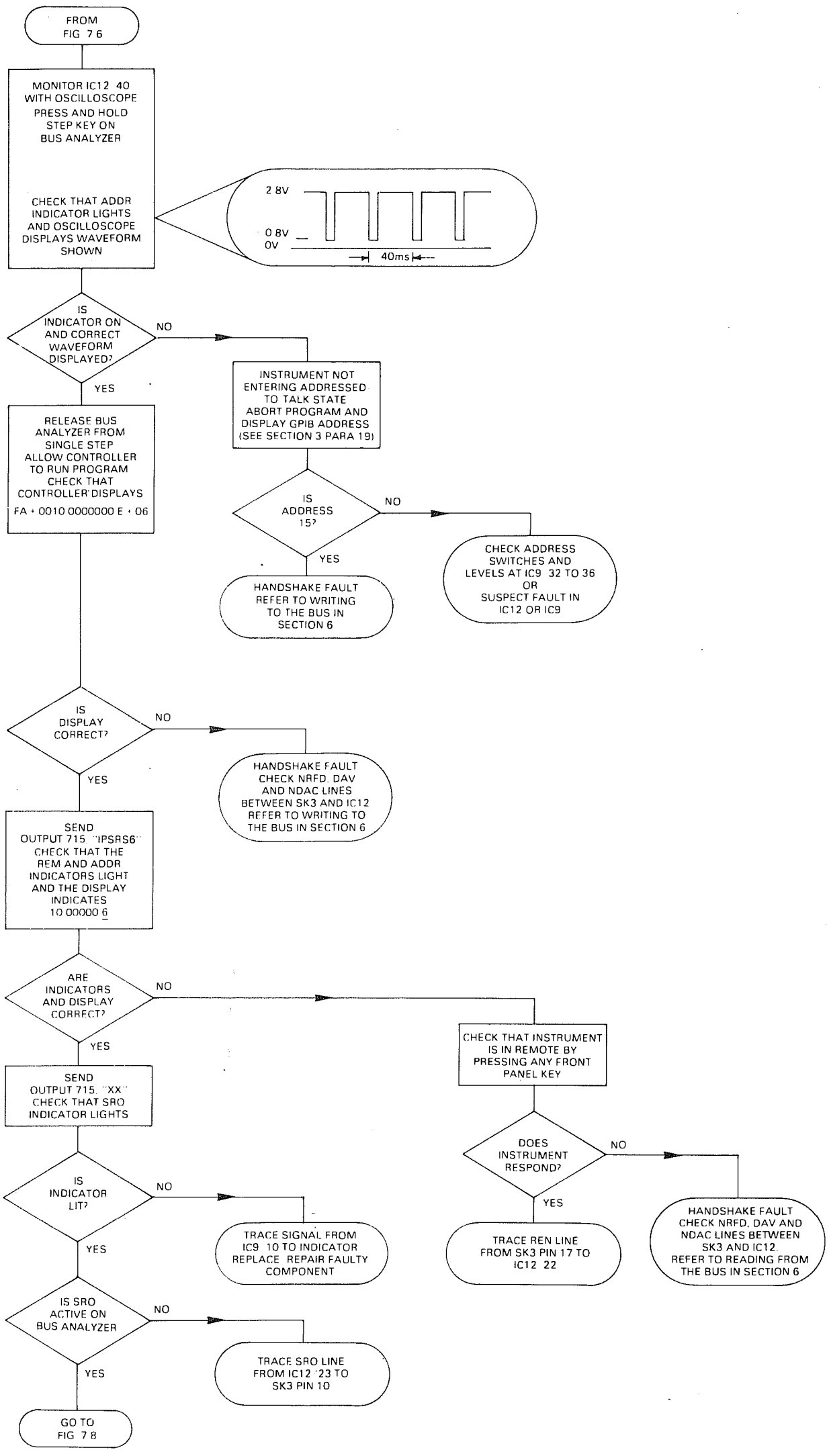


Fig 7.7 Fault Finding Flowchart - GPIB Part 2

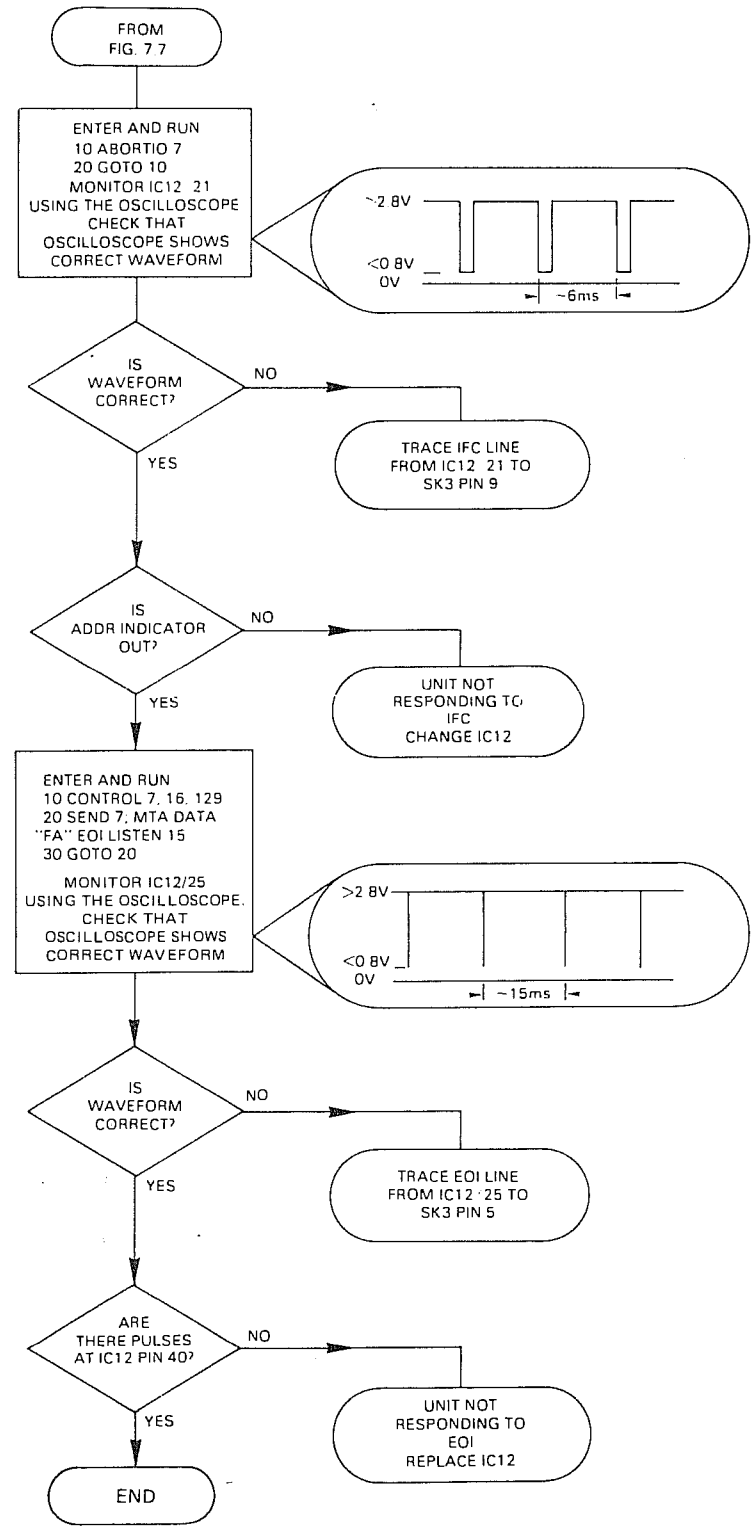


Fig 7.8 Fault Finding Flowchart - GPIB Part 3

SETTING UP AFTER REPAIR

Introduction

19 After repair, the relevant setting-up procedures from those given in the following paragraphs should be implemented before carrying out the overall specification check. The procedures should also be used if the instrument fails a routine specification check.

20 The ambient temperature must be maintained at 23 °C ± 2 °C throughout the procedures. The instrument should be powered from an AC supply, not a battery pack.

WARNING: LETHAL VOLTAGE
THESE PROCEDURES REQUIRE THE INSTRUMENT TO BE OPERATED WITH THE COVERS REMOVED. LETHAL VOLTAGE LEVELS ARE EXPOSED UNDER THESE CONDITIONS.

Channel A Input System

21 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Connecting Leads	7
T-piece	8
50 Ω load	9
Trimming tool	12

22 Set R72 fully counter-clockwise and R33 to its mid-position. R33 is located inside the screened module, as shown in Fig 7.9.

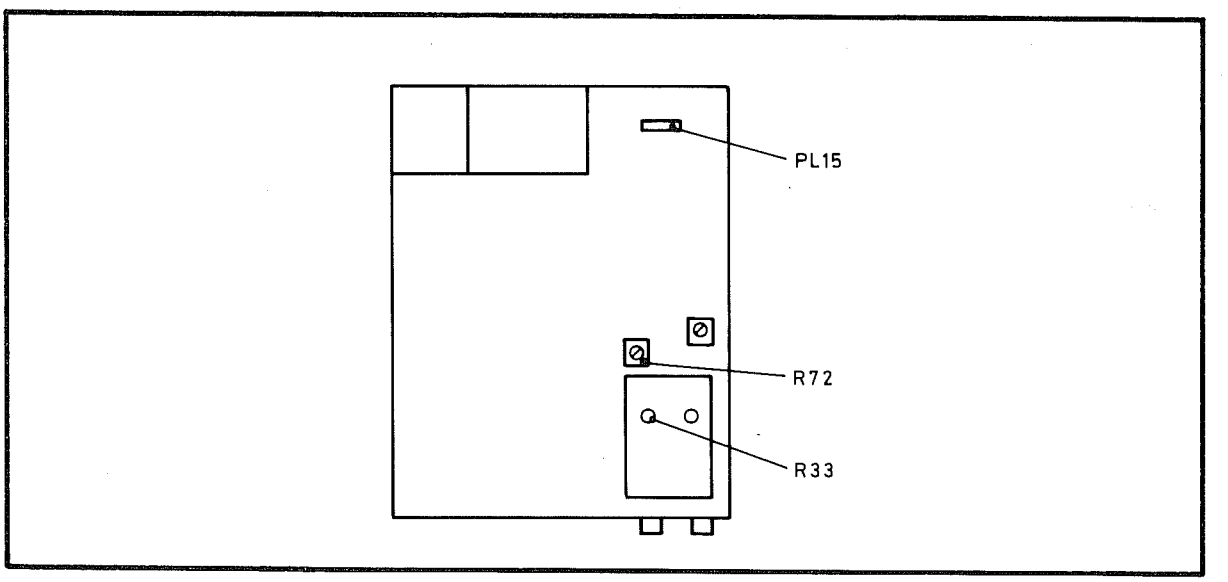


Fig 7.9 Location of R33, R72 and PL15

23 (1) Switch the 1990 on. Allow 10 min for the instrument to stabilise and ensure that the A trigger level control is switched to 0 V.

(2) Press the RESOLUTION ↓ key three times, until 000 is displayed.

(3) Connect the test equipment as shown in Fig 7.10. If the 1990 is not fitted with the frequency standard input/output option, use the X1 scope probe to connect the 10 MHz standard output of the signal generator to PL15/5.

(4) Set the signal generator output to 10 MHz at a level of 2.0 mV r.m.s.

(5) Verify that the EXT STD indicator is lit, and that the channel B TRIG indicator is not flashing.

(6) Adjust R33 to obtain the most stable display indication of 10.00 E6 ± 0.01 E6, with the GATE indicator flashing.

NOTE: Care is needed when adjusting R33. The display indication is random when R33 is set to either side of the correct position.

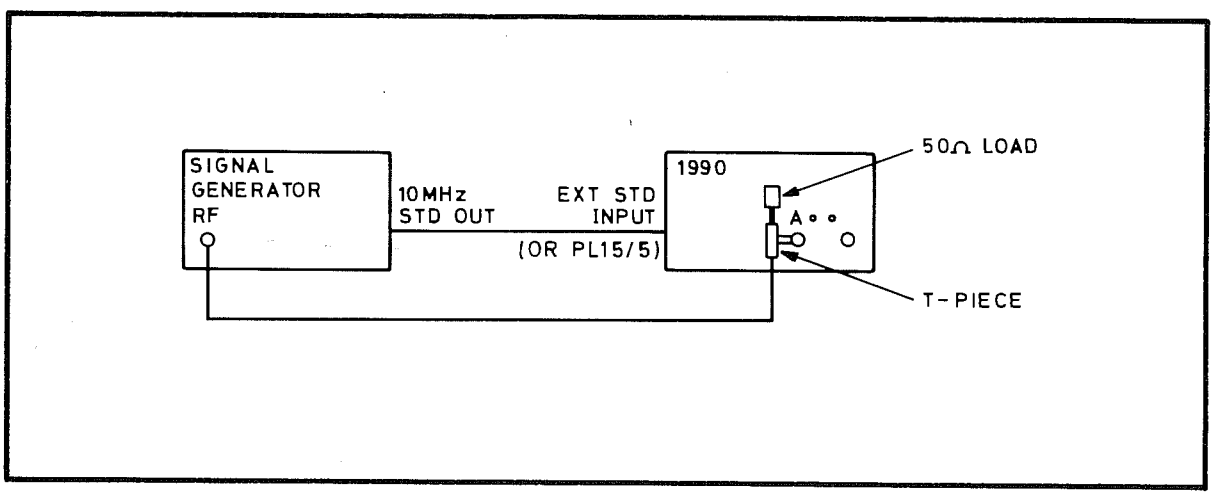


Fig 7.10 Connections for Channel A Input System Adjustment

24 (1) Switch off the RF output of the signal generator.

(2) Press the RESOLUTION ↑ key three times, until 000000 is displayed.

(3) Switch on the RF output of the signal generator.

(4) Increase the signal generator output to 8.0 mV r.m.s.

(5) Adjust R72 slowly clockwise until the display just becomes unstable. Turn back until the display is just stable, and indicates 10.00000 E6 ± 0.000001 E6.

(6) Reduce the signal generator output to 4 mV r.m.s. Verify that the GATE indicator stops flashing. If it does not, repeat steps (4) to (6).

(7) Switch off the 1990. Disconnect the test equipment.

Channel B Input System

25 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Connecting leads	7
T-piece	8
50Ω load	9
Trimming tool	12

26 Set R73 fully counter-clockwise and R36 to its mid-position. R36 is located inside the screened module, as shown in Fig 7.11.

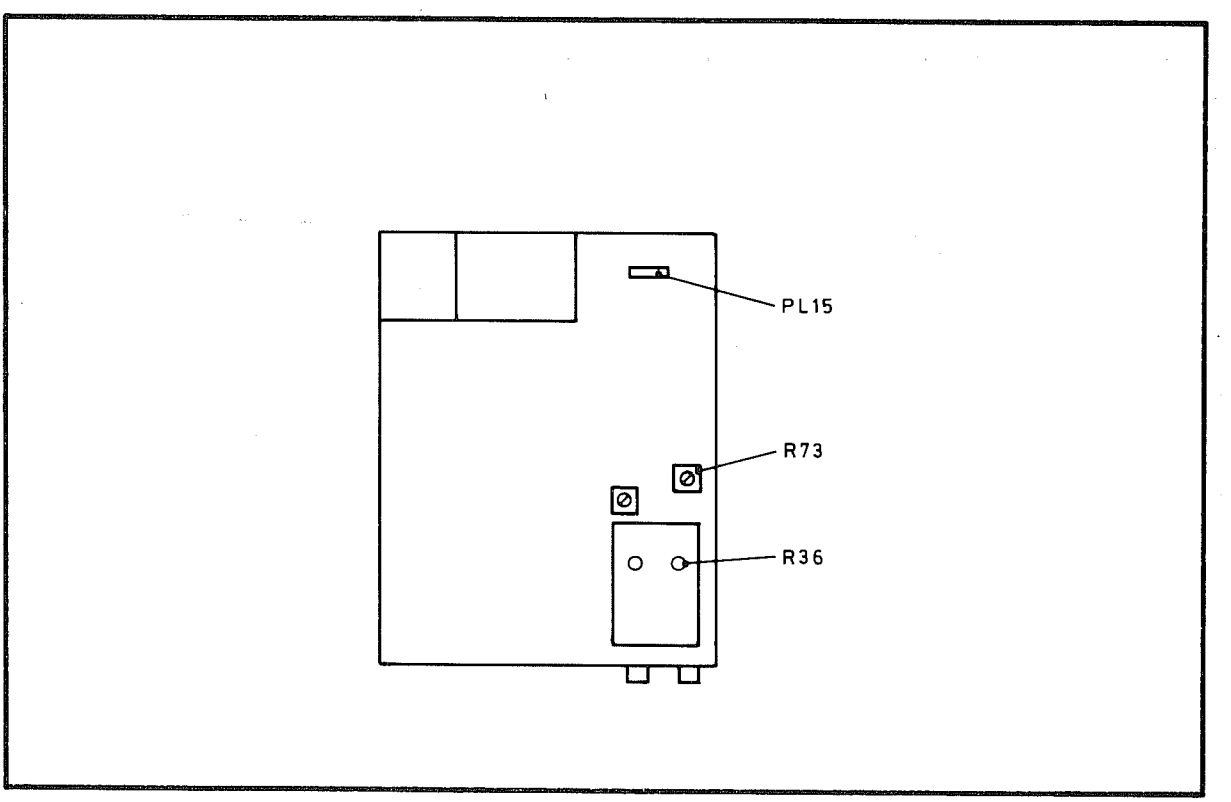


Fig 7.11 Location of R36, R73 and PL15

27 (1) Switch the 1990 on. Allow 10 min for the instrument to stabilise and ensure that the B trigger level control is switched to 0 V.

(2) Press [DELAY] for 3s, until the DELAY LED lights.

(3) Press the RESOLUTION ↓ key three times, until 000 is displayed.

(4) Connect the test equipment as shown in Fig 7.12. If the 1990 is not fitted with the frequency standard input/output option, use the X1 scope probe to connect the 10 MHz standard output of the signal generator to PL15/1.

(5) Set the signal generator output to 10 MHz at a level of 2.0 mV r.m.s.

(6) Verify that the EXT STD indicator is lit, and that the channel A TRIG indicator is not flashing.

(7) Adjust R36 to obtain the most stable display indication of 10.00 E6 ± 0.01 E6, with the GATE indicator flashing.

NOTE: Care is needed when adjusting R36. The display indication is random when R36 is set to either side of the correct position.

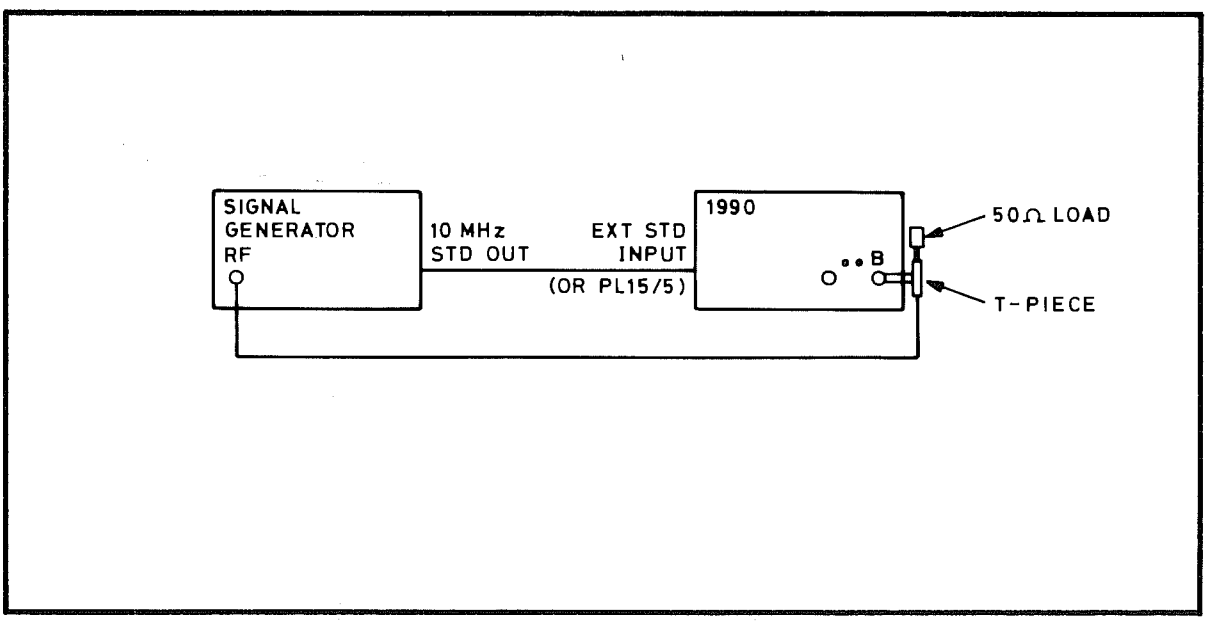


Fig 7.12 Connections for Channel B Input System Adjustment

28 (1) Switch off the RF output of the signal generator.

(2) Press the RESOLUTION ↓ key three times, until 000000 is displayed.

(3) Switch on the RF output of the signal generator.

(4) Increase the signal generator output to 8.0 mV r.m.s.

(5) Adjust R73 slowly clockwise until the display just becomes unstable. Turn back until the display is just stable, and indicates 10.00000 E6 ± 0.00001 E6.

(6) Reduce the signal generator output to 4 mV r.m.s. Verify that the GATE indicator stops flashing. If it does not, repeat steps (4) to (6).

(7) Switch off the 1990. Disconnect the test equipment.

Frequency Doubler 19-1238 (Options 04A and 04B only)

29 Test equipment required:

Item	Table 7.1 Item No.
Oscilloscope with X10 Probe	2
Trimming Tool	13

30 (1) Switch on the 1990. Allow a warm-up period of 10 minutes for option 04A and 30 minutes for option 04B.

(2) Monitor the signal at pin 3 using the oscilloscope and X10 probe. Verify that the frequency is 10 MHz.

(3) If necessary, adjust T1 and T2 to obtain a signal level not less than 0.5 V peak-to-peak.

(4) Monitor the DC voltage at TP1 using the oscilloscope and X10 probe. Adjust T1 and T2 to obtain the smallest possible voltage. Verify that the voltage achieved is in the range from 400 mV to 800 mV.

(5) Transfer the probe to pin 3. Verify that the signal frequency is 10 MHz and that the level is in the range from 0.8 V to 1.2 V.

(6) Switch off the 1990. Disconnect the test equipment.

Reference Frequency Multiplier 19-1164 (Option 10)

31 Test equipment required:

Item	Table 7.1 Item No.
Oscilloscope with X1 Probe	2
Frequency Standard	4
Connecting Lead	7
Trimming Tool	12

32 (1) Switch the 1990 on.

(2) Connect the frequency standard to the EXT. STD. INPUT socket. Verify that the EXT STD indicator lights.

(3) Monitor the DC voltage at TP1 using the oscilloscope and X1 probe.

(4) If necessary, adjust C2 to obtain a voltage of +2.5 V ±0.2 V.

(5) Switch off the 1990. Disconnect the test equipment.

Battery Pack 11-1625 (Option 07)

33 Test equipment required:

Item	Table 7.1 Item No.
Digital Multimeter	3
Multimeter (2)	13
Power Supply	14
Test lead	15

NOTE:
(1) The battery pack should be installed in the parent 1990.
(2) The battery tray should be in position, but disconnected at the flying lead (SK12/PL12).
(3) The numbers on mating pins of PL21 and SK21 do not correspond. Take care to connect test equipment to the points specified. Connection must be made to PL21 from the underside of the motherboard.

34 Connect the test equipment as shown in Fig. 7.13. DO NOT CONNECT THE 1990 TO AN AC SUPPLY.

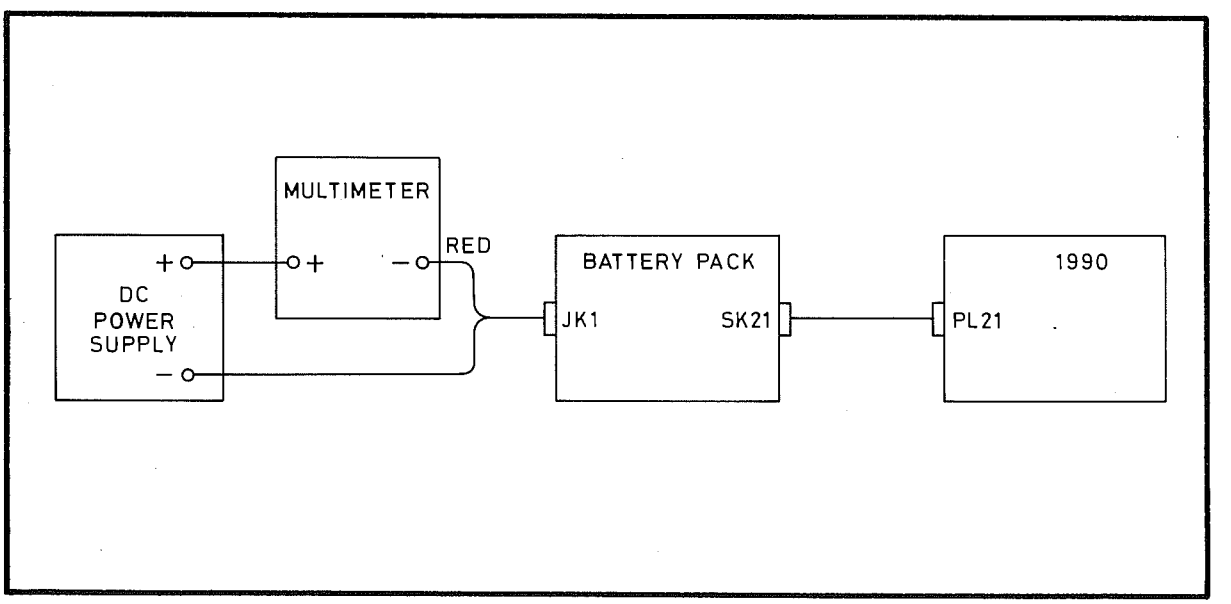


Fig 7.13 Connections for Battery Pack Test

35 (1) Set R10, R28 and R36 on the battery pack fully clockwise.

(2) Set the INTERNAL/EXTERNAL switch to EXTERNAL.

(3) Set the NORMAL/BATTERY SAVE switch to NORMAL.

36 (1) Set the multimeter to measure direct current greater than 2 A.

(2) Set the power supply output to 15 V.

(3) Switch on the 1990. Verify that the normal start-up sequence occurs.

37 (1) Set the digital multimeter to measure over the range from 4 V to 20 V DC.

(2) Connect the digital multimeter between PL21 pin 4 (positive) and PL21 pin 10 (0 V).

(3) If necessary, adjust R28 on the battery pack to obtain an indication of between 5.38 V and 5.40 V.

38 Use the digital multimeter to measure the voltage between PL21 pin 10 (0 V) and each of the points shown in Table 7.3. Verify that the voltages measured are as shown in column A.

TABLE 7.3

Battery Pack Voltage Levels

Test Point	Voltage Relative to PL21 Pin 10	
	A	B
PL21 pin 4	+5.38 V to +5.40 V	+5.36 V to +5.40 V
PL21 pin 5	-5.50 V to -5.95 V	-5.45 V to -6.00 V
PL21 pin 15	+14.50 V to +15.70 V	+14.40 V to +15.80 V
PL21 pin 14	-14.55 V to -15.75 V	-14.45 V to -15.85 V

39 Transfer the digital multimeter to measure the voltage between PL21 pin 19 (positive) and PL21 pin 10 (0 V). Adjust the power supply output to obtain an indication of 10.0 V to 10.2 V.

40 Use the digital multimeter to measure the voltage between PL21 pin 10 (0 V) and each of the points shown in Table 7.3. Verify that the voltages measured are as shown in column B.

41 (1) Turn R10 slowly counter-clockwise until the 1990 shuts down completely (all display LEDs go out).

(2) Verify that the current drawn from the power supply immediately after the 1990 shuts down, as indicated on the multimeter, is less than 50 µA (reduce the multimeter range as required).

(3) Verify that the current continues to fall towards zero.

(4) Set the multimeter to measure direct current greater than 2 A.

42 (1) Connect the digital multimeter between PL12 pin 1 (positive) and PL12 pin 3 (negative).

(2) Restore the power supply output to 15 V.

(3) Switch the 1990 off and on. Wait until the start-up sequence is completed.

(4) Verify that the digital multimeter indicates not more than 0.1 V.

(5) Switch the 1990 to standby.

(6) Adjust R36 on the battery pack until the digital multimeter indicates between 7.62 V and 7.64 V.

(7) Switch the 1990 off. Disconnect the digital multimeter.

43 (1) Set the second multimeter to measure direct current greater than 1.5 A.

(2) Connect the multimeter between PL12 pin 1 (positive) and PL12 pin 3 (negative).

(3) Disconnect the power supply and the multimeter. Connect the 1990 to an AC supply.

(4) Switch the 1990 on. Wait until the start-up sequence is completed.

(5) Switch the 1990 to standby. Verify that the current between PL12 pin 1 and PL12 pin 3 is between 0.9 A and 1.1 A.

(6) Switch the 1990 off.

44 (1) Disconnect the multimeter from PL12.

(2) Connect the battery at PL12/SK12.

(3) Select INTERNAL. If necessary, switch the 1990 on and select STANDBY to charge the battery. Switch the 1990 off.

(4) Disconnect the 1990 from the AC supply.

(5) Switch the 1990 on. Verify that the instrument can be switched in and out of standby.

(6) Switch the 1990 off. Lock R10, R28 and R36 with a small quantity of silicone rubber.

INTERNAL FREQUENCY STANDARD, ROUTINE CALIBRATION

Standard Oscillator and TCXO Option

45 Test equipment required:

Item	Table 7.1 Item No
Frequency Standard	4
Connecting lead	7
Trimming tool	12

46 (1) If the instrument is fitted with the standard oscillator, remove the covers.

(2) Switch on the 1990. Select FREQ A and verify that 000000 is displayed. Press the RESOLUTION ↑ key until 0000000 is displayed.

(3) Connect the test equipment as shown in Fig 7.14.

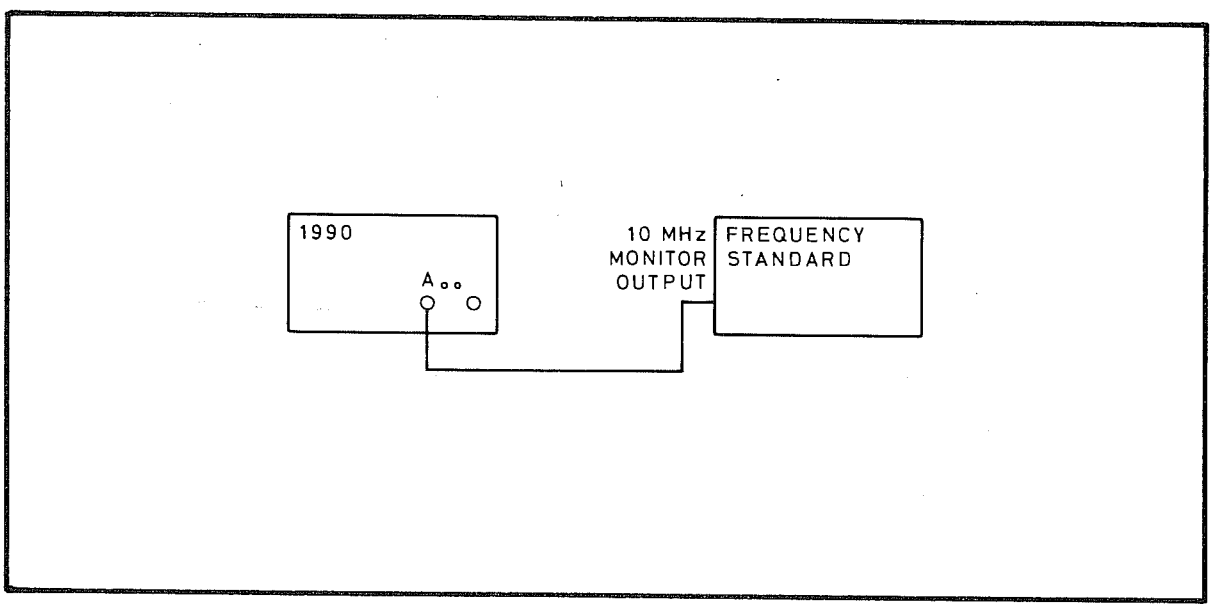


Fig 7.14 Connections for Internal Frequency Standard Adjustment : Standard Oscillator and TXCO Option

(4) Adjust the internal frequency standard to be as near 10 MHz as possible. The display limits are shown in Table 7.4. The standard oscillator is located on the motherboard. as shown in Fig 7.15, but the TCXO option may be adjusted via the rear panel.

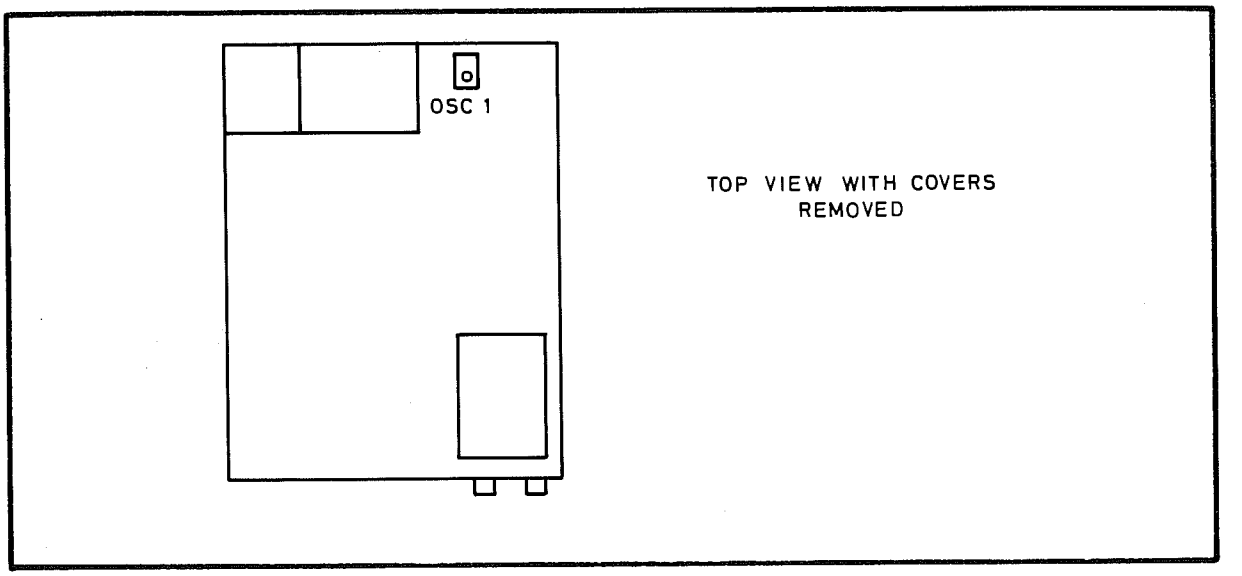


Fig 7.15 Location of Standard Oscillator OSC1

Table 7.4

Internal Frequency Standard Accuracy: Standard Oscillator and TCXO Option

Frequency Standard	1990 Display Limits	Accuracy
Standard oscillator	9.999995 E6 to 10.000005 E6	5 parts in 10^7
Option 04T (TCXO)	9.999999 E6 to 10.000001 E6	1 part in 10^7

(5) Switch off the 1990. Switch off and disconnect the test equipment

Ovened Oscillator Options 04A and 04B

47 Test equipment required

Item	Table 7.1 Item No
Frequency Standard	4
High resolution counter	6
Connecting leads	7
Trimming tool	12

(1) Switch on the 1990. Allow the instrument to warm up for 24 hours before making any adjustment

(2) Connect the test equipment as shown in Fig 7.16.

(3) Set up the high resolution counter for an external frequency standard, and a resolution of 9 digits.

(4) Adjust the frequency standard on the 1990, via the aperture in the rear panel, to be as near 10 MHz as possible. The display limits are shown in Table 7.5

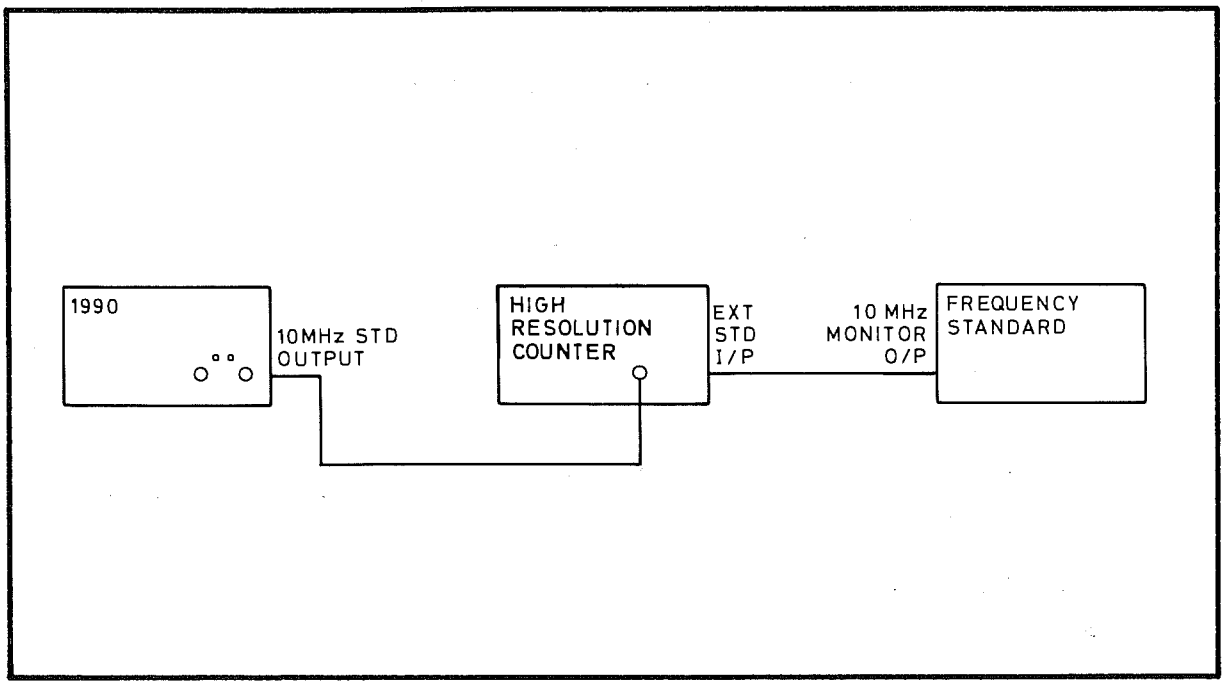


Fig 7.16 Connections for Internal Frequency Standard Adjustment : Ovened Oscillator Options

TABLE 7.5

Internal Frequency Standard Accuracy : Ovened Oscillator Options

Frequency Standard	High Res Counter Display Limits	Accuracy
Option 04A	9.99999990 E6 to 10.00000010 E6	1 part in 10^8
Option 04B	9.99999999 E6 to 10.00000001 E6	1 part in 10^9

(5) Switch off the 1990. Switch off and disconnect the test equipment.

OVERALL SPECIFICATION CHECK

Introduction

48 Satisfactory completion of the following performance verification procedures (PVPs) will confirm that the instrument is functional and meets its specification. Before commencing the specification check ensure that the instrument passes the test given in Section 3 Paragraphs 9 and 10. The PVPs should be carried out in the order given.

49 The following conditions must be maintained throughout the specification check:

(1) The instrument must be operated from an AC supply.

(2) The line voltage must be within the range indicated by the line voltage selector.

(3) The instrument covers must be fitted.

(4) The ambient temperature must be 23 °C ± 2 °C.

(5) The power supply to the frequency standard must be uninterrupted.

50 The instrument should be allowed to warm up for one hour (switched to standby, if required) before commencing the specification check.

Channel A Sensitivity PVP

51 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Audio Oscillator	5
Connecting Leads	7
T-piece	8
50Ω Load	9

52 (1) Switch on the 1990, and ensure that the channel A trigger level control is switched to 0V.

(2) Connect the test equipment as shown in Fig 7.17.

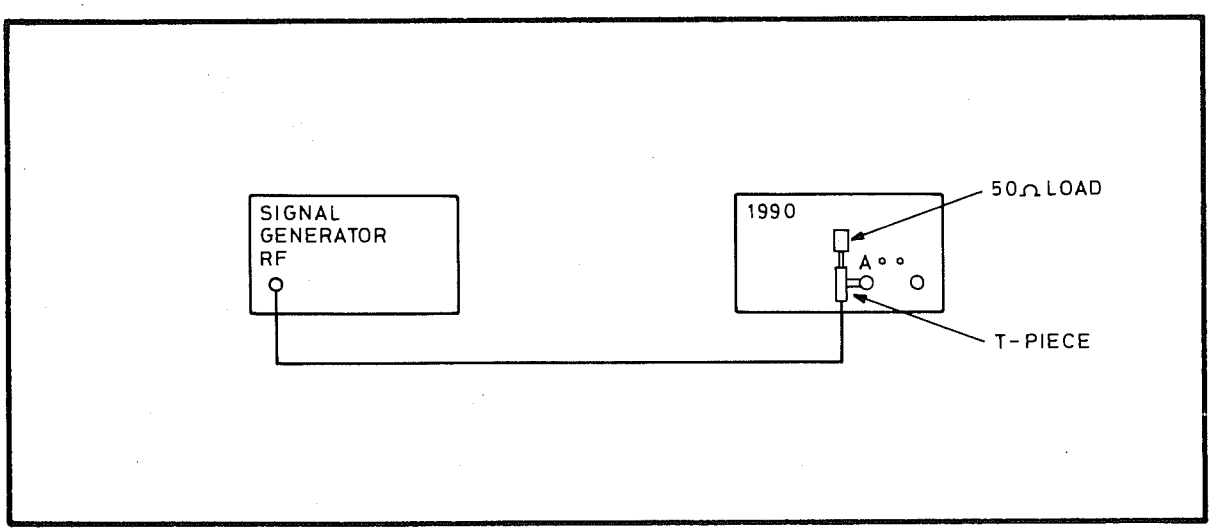


Fig 7.17 Connections for Channel A Sensitivity PVP

(3) Set the signal generator output to the frequencies shown in Table 7.6 in turn. Set the 1990 resolution to the corresponding value.

(4) At each frequency, determine the minimum input level to the 1990 which gives stable counting. Verify that this is not more than the level shown in the table.

(5) Disconnect the test equipment.

TABLE 7.6

Channel A Sensitivity

Frequency	1990 Resolution	Signal Level
120 MHz	6 digits	45 mV
100 MHz	6 digits	22 mV
10 MHz	6 digits	22 mV
100 kHz	6 digits	22 mV

53 (1) Connect the test equipment as shown in Fig 7.18.

(2) Set the audio oscillator output to the frequencies shown in Table 7.7 in turn. Set the 1990 resolution to the corresponding value.

(3) At each frequency, determine the minimum input level to the 1990 that gives stable counting. Verify that this is not more than the level shown in the table.

(4) Disconnect the test equipment.

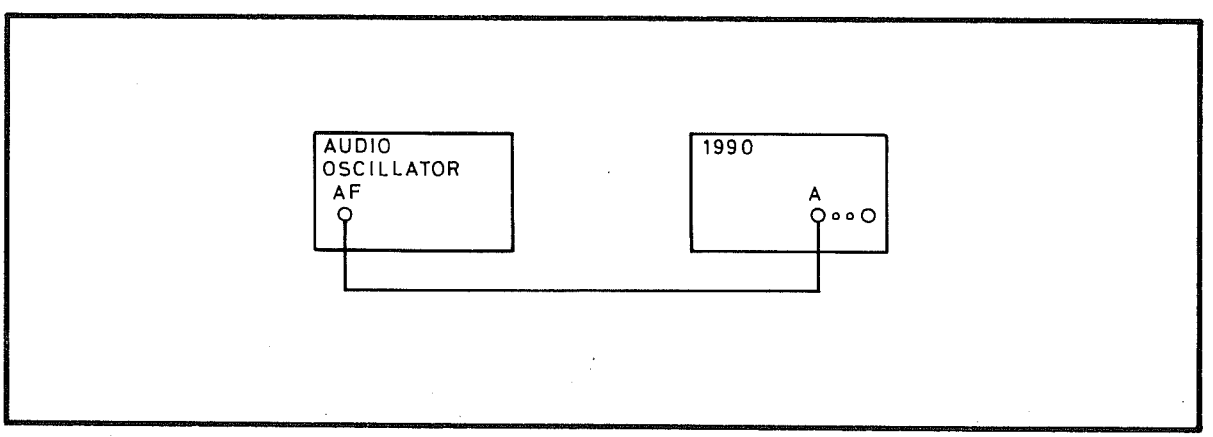


Fig 7.18 Connections for Channel A Sensitivity PVP (Part 2)

TABLE 7.7

Channel A Sensitivity

Frequency	1990 Resolution	Signal Level
5 kHz	3	22 mV
10 Hz	3	22 mV

Channel B Sensitivity PVP

54 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Audio Oscillator	5
Connecting Leads	7
T-piece	8
50Ω Load	9

55 (1) Ensure that the channel B trigger level control is set to 0 V.

(2) Connect the test equipment as shown in Fig 7.19.

(3) Press the DELAY key for 3s, until the DELAY LED comes on.

(4) Set the signal generator output to the frequencies shown in Table 7.8 in turn. Set the 1990 resolution to the corresponding value.

(5) At each frequency, determine the minimum input level to the 1990 that gives stable counting. Verify that this is not more than the level shown in the table.

(6) Disconnect the test equipment.

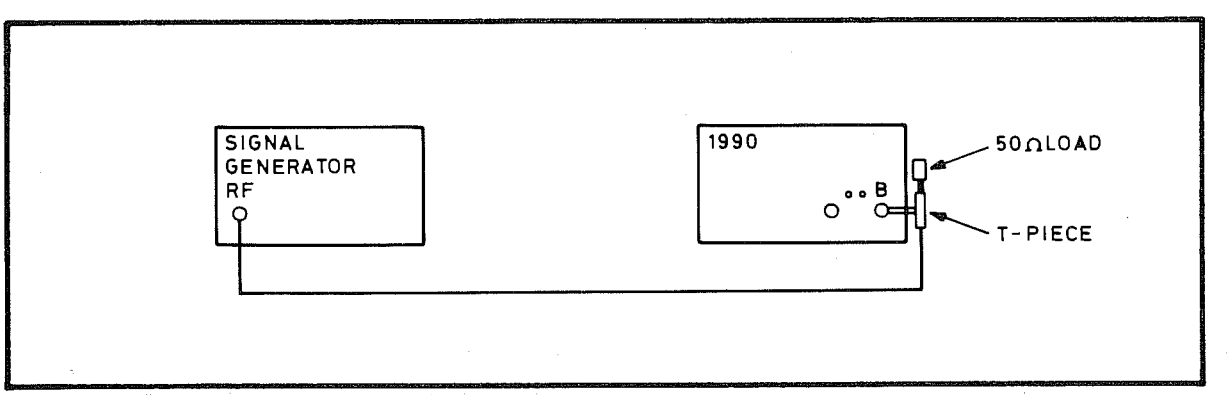


Fig 7.19 Connections for Channel B Sensitivity PVP

TABLE 7.8

Channel B Sensitivity

Frequency	1990 Resolution	Signal Level
100 MHz	6 digits	22 mV
10 MHz	6 digits	22 mV
100 kHz	6 digits	22 mV

56 (1) Connect the test equipment as shown in Fig 7.20.

(2) Set the audio oscillator output to the frequencies shown in Table 7.9 in turn. Set the 1990 resolution to the corresponding value.

(3) At each frequency, determine the minimum input level to the 1990 that gives stable counting. Verify that this is not more than the level shown in the table.

(4) Press DELAY

(5) Disconnect the test equipment.

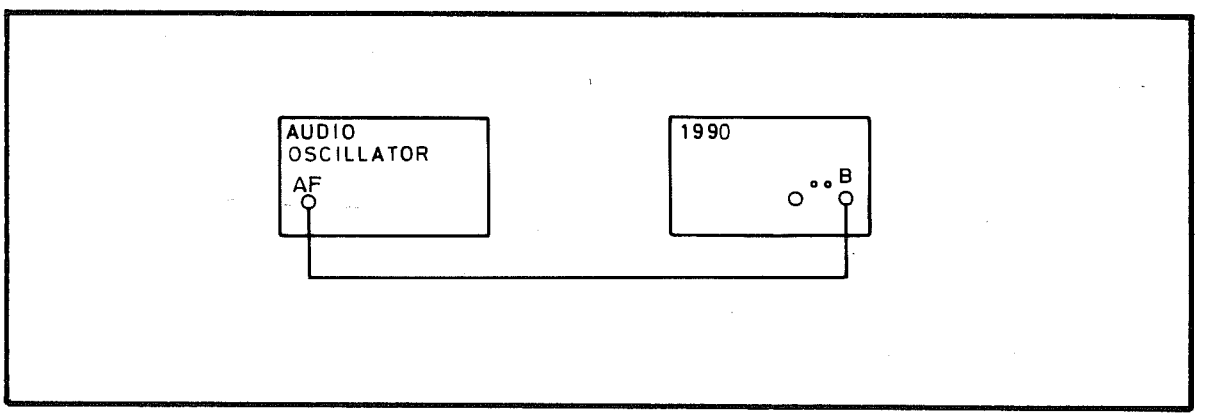


Fig 7.20 Connections for Channel B Sensitivity PVP (Part 2)

TABLE 7.9

Channel B Sensitivity

Frequency	1990 Resolution	Signal Level
5 kHz	3	22 mV
10 Hz	3	22 mV

Attenuator PVP

57 Test Equipment required

Item	Table 7.1 Item No.
Signal Generator	1
Connecting lead	7
T-piece	8
50Ω load	9

58 (1) Ensure that both trigger level controls are switched to 0 V. Select 6 digits resolution on the 1990, and connect the test equipment as shown in Fig 7.21.

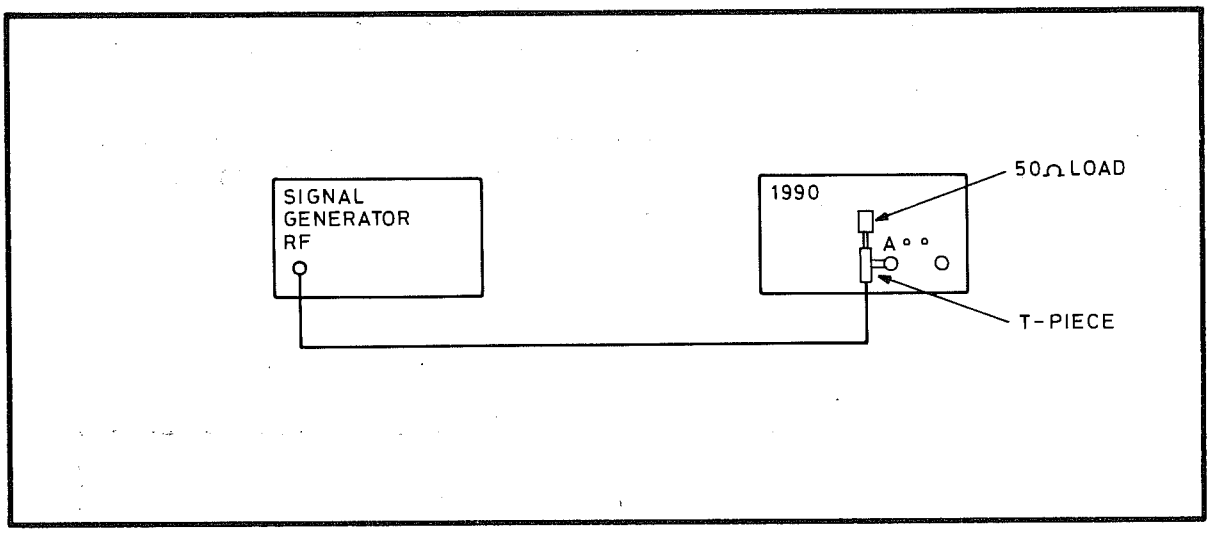


Fig 7.21 Connections for Attenuator PVP

(2) Set the signal generator to 1 MHz, and set the output level so that the 1990 just counts correctly

(3) Select the X10 attenuator on channel A, and increase the signal generator output level until the 1990 just counts correctly again. The increase should be in the range 17.5 to 22.5 dB.

(4) Disable the X10 attenuator on channel A.

(5) Transfer the signal to channel B of the 1990, and press DELAY for 3s, until the DELAY LED is lit.

(6) Repeat sections (2) to (4) above, using the channel B attenuator.

(7) Press DELAY again, and disconnect the equipment.

Filter PVP

59 Test Equipment required

Item	Table 7.1 Item No.
Signal Generator	1
Connecting lead	7
T-piece	8
50Ω lead	9

60 (1) Ensure that the channel A trigger level control is switched to 0 V. Connect the test equipment as shown in Fig 7.22.

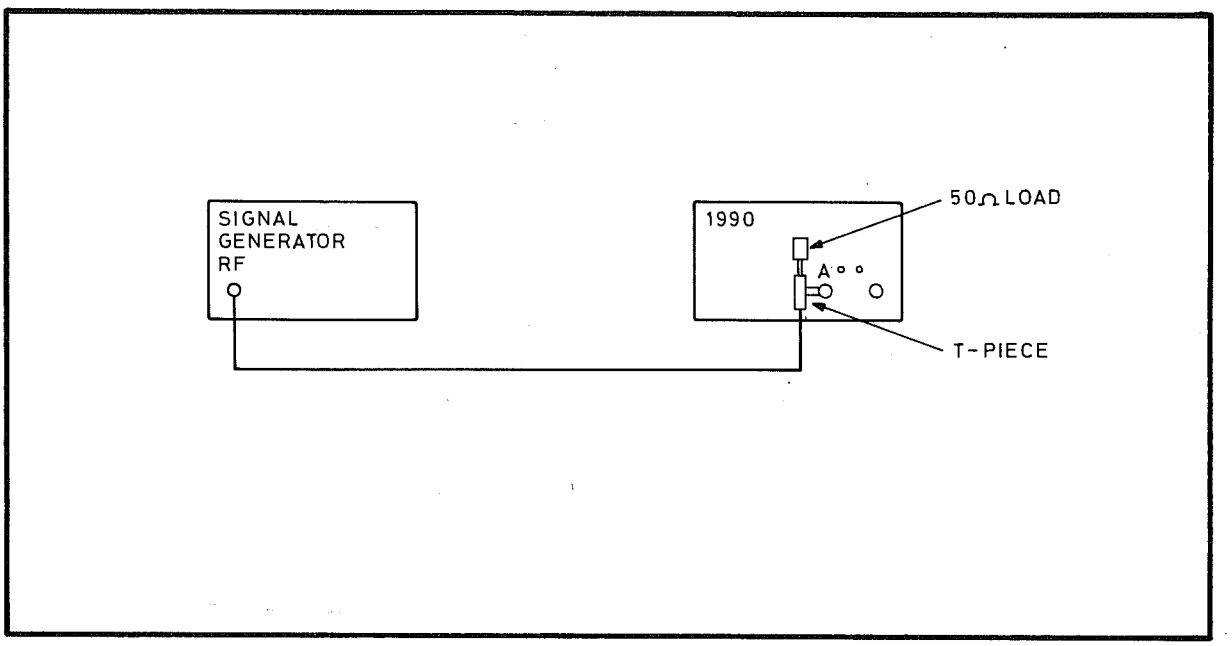


Fig 7.22 Connections for Filter PVP

(2) Set the signal generator to 100 kHz, and measure the sensitivity of the 1990 at 100 kHz.

(3) Select the filter, and check that the unit stops counting.

(4) Increase the level by a factor of 2, and check that the unit counts 100 kHz correctly, as in (2).

(5) Disable the filter.

Time Internal PVP

61 Test equipment required

Item	Table 7.1 Item No.
Signal Generator	1
Connecting lead	7
T-piece	8
50Ω lead	9

62 (1) Ensure that both trigger level controls are switched to 0 V. Connect the test equipment as shown in Fig 7.23.

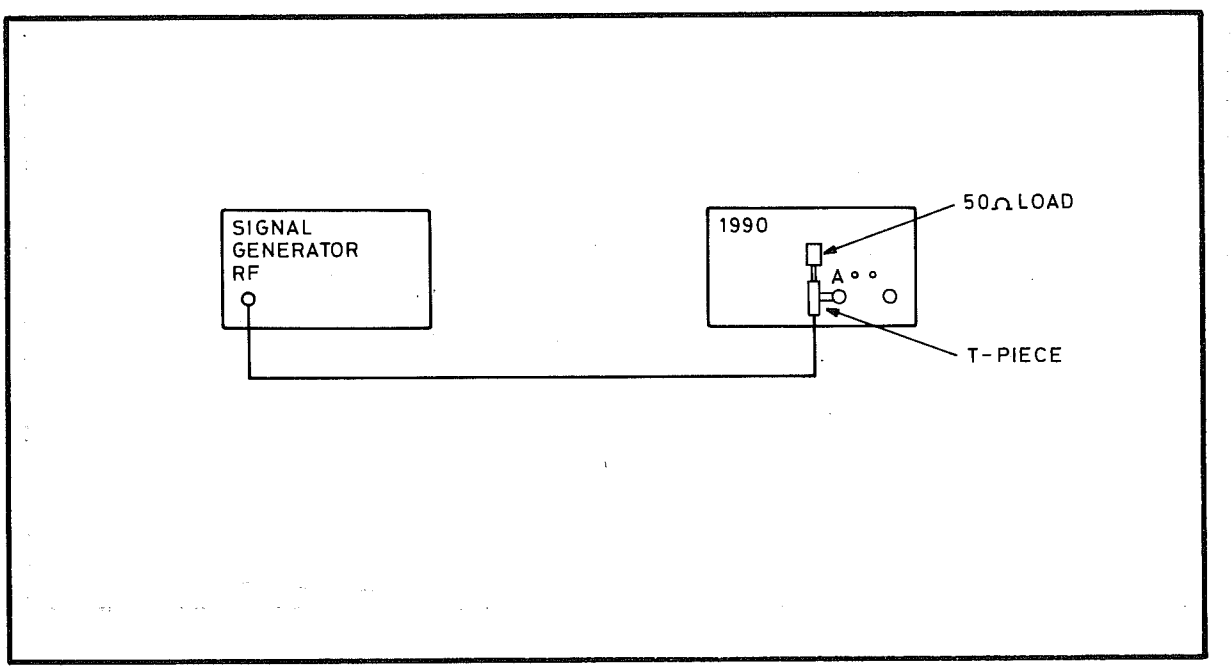


Fig 7.23 Connections for Time Interval PVP

(2) Set the signal generator to 1 MHz at 450 mV, and select T.I. A B and COM A on the 1990. With the trigger slope settings as shown in Table 7.10, check that the readings are within the limits given.

TABLE 7.10

Time Interval PVP Readings

A trigger slope	B trigger slope	Display
+	+	0oo ± 1oo E - 9s *
+	-	500 ± 1oo E - 9s
-	-	0oo ± 1oo E - 9s *
-	+	500 ± 1oo E - 9s

* Occasionally the instrument may measure one whole period instead of zero. This is acceptable provided that the display reads 1000ns ± 100ns.

(3) Set + slope on both channels, disable COM A, and select FREQ. A. Disconnect the equipment.

Trigger Level PVP

63 Test equipment required

Item	Table 7.1 Item No.
Digital Multimeter	3

64 (1) Connect the test equipment as shown in Fig 7.24.

(2) Set the multimeter to measure DC volts.

(3) Turn the A trigger level control to the positions shown in Table 7.11, and verify that the multimeter readings are within the limits specified.

Table 7.11

Trigger Level Output Voltages

Control position	Multimeter reading
Fully clockwise	+2.60 V to +3.36 V
Fully anticlockwise but not switched	-2.60 V to -3.36 V
Switched 0 V	0 V ± 10 mV

(4) Transfer the multimeter to the channel B trig level output.

(5) Turn the B trigger level control to the positions shown in Table 7.11. Verify that the multimeter readings are within the limits specified.

(6) Disconnect the test equipment.

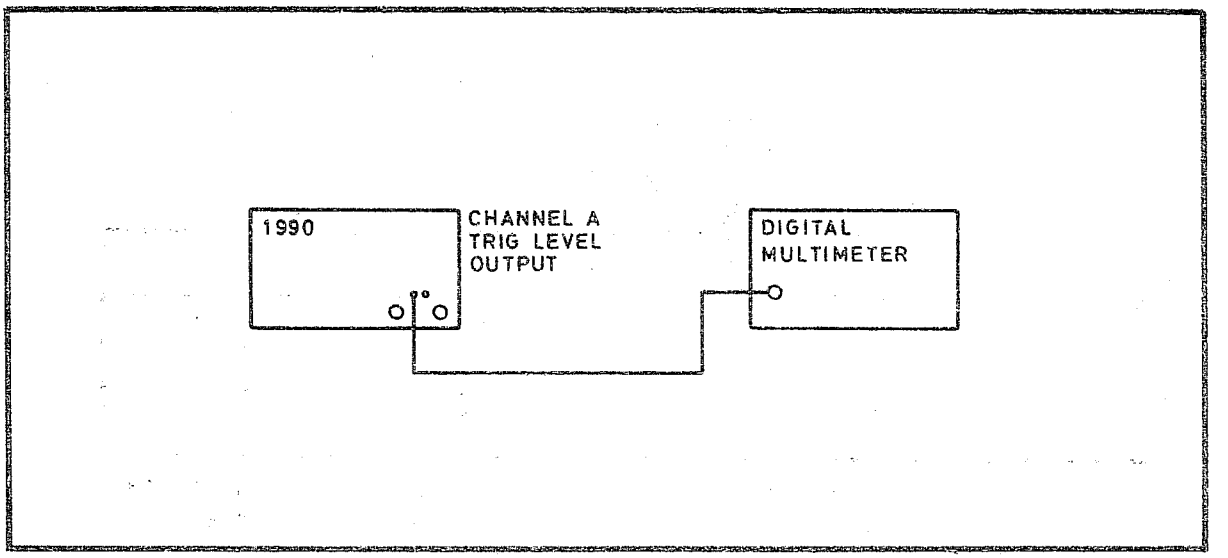


Fig 7.24 Connections for Trigger Level PVP

AC/DC Coupling PVP

65 Test equipment required

Item	Table 7.1 Item No.
Oscilloscope with X1 probe	2

66 (1) Use the oscilloscope and probe to set the B trigger level to about + 2 V.

(2) Connect the test equipment as shown in Fig 7.25.

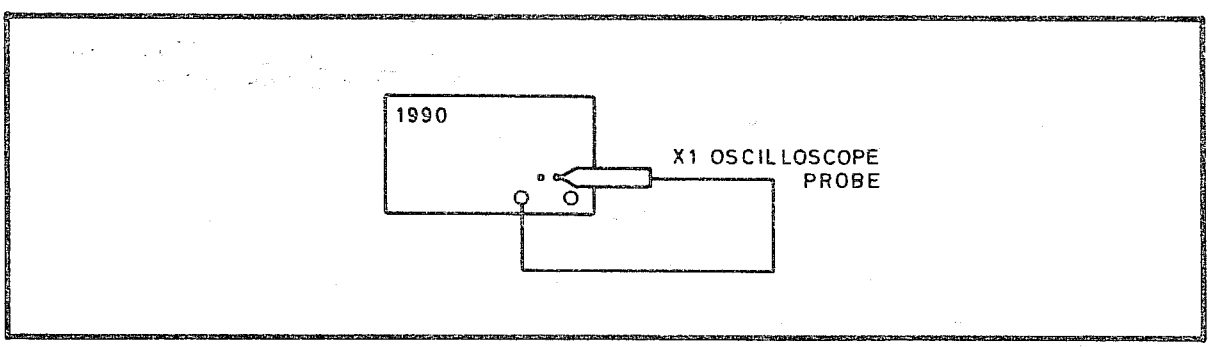


Fig 7.25 Connections for A Channel AC/DC Coupling PVP

(3) Check that AC coupling is selected on Channel A, and slowly turn the A trigger level control clockwise from its 0 V switched position. Note the point at which the A TRIG LED goes out, and verify that the control is near the centre of its range. Return to the switched 0 V position.

(4) Select DC coupling on Channel A. Turn the A trigger level control slowly clockwise and again note the point at which the A TRIG LED goes out. The A and B trigger level controls should be in approximately the same position.

(5) Transfer the probe to the A trigger level output and use the oscilloscope to set the A trigger level to about +2 V. Apply this level via the probe to the B input, and turn the B trigger level to its switched 0 V position.

(6) Confirm that the B TRIG LED goes out as the B TRIG LEVEL control passes 0 in a clockwise direction.

(7) Return the B TRIG LEVEL control to the switched 0 V position.

(8) Select DC coupling on channel B.

(9) Repeat (6); leaving the B TRIG LEVEL CONTROL in the position at which the B TRIG LED goes out. Confirm that the A and B TRIG LEVEL controls are in approximately the same physical position.

(10) Select AC coupling on both channels, and return both TRIG LEVEL controls to the switched 0 V position. Disconnect the test equipment.

External Standard Input Sensitivity PVP (Reference Option 02 only)

67 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Connecting Lead	7
T-Piece	8
50Ω Load	9

68 (1) Connect the equipment as shown in Fig 7.26.

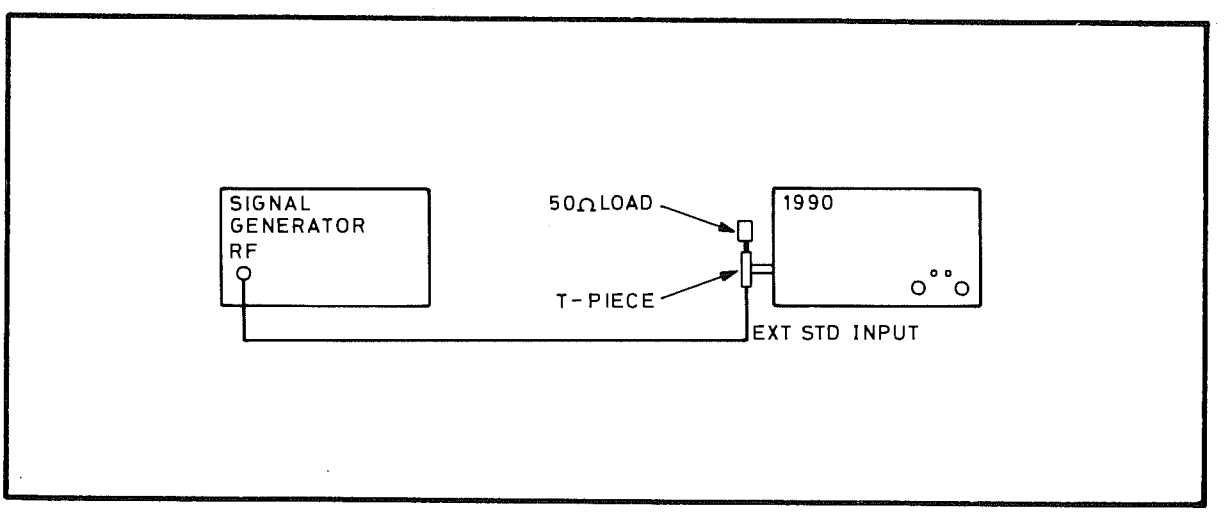


Fig 7.26 Connections for External Standard Input Sensitivity PVP

(2) Set the signal generator output to 10 MHz at a level of 100 mV.

(3) Slowly increase the signal level until the 1990 EXT STD indicator lights steadily.

(4) Verify that the signal level is not more than 250 mV r.m.s.

(5) Disconnect the test equipment.

10 MHz Standard Output Level PVP (Reference Option 02 only)

69 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	2
Connecting Lead	7
T-piece	8
Load	9

70 (1) Connect the test equipment as shown in Fig 7.27.

(2) Verify that the peak-to-peak amplitude of the displayed waveform is 1.0 V ±0.4 V. Verify that the mark/space ratio is between 30:70 and 70:30.

(3) Disconnect the test equipment.

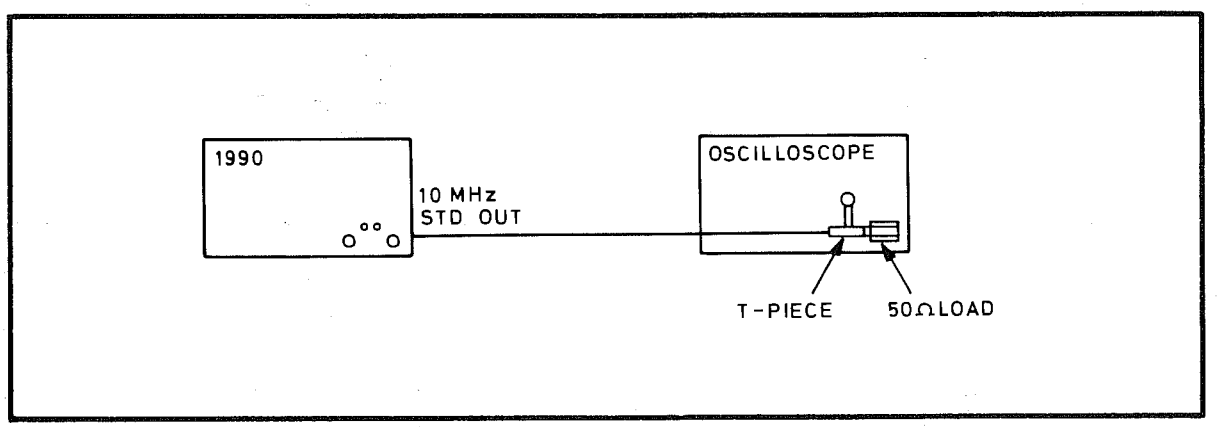


Fig 7.27 Connections for 10 MHz Standard Output Level PVP

Internal Frequency Standard PVP

Standard Oscillator and TXCO Option

71 Test equipment required:

Item	Table 7.1 Item No
Frequency Standard	4
Connecting Lead	7

72 (1) Select 7 digit resolution on the 1990, and verify that 0000000 is displayed. Check that both trigger level controls are in the switched 0 V position

(2) Connect the test equipment as shown in Fig 7.28.

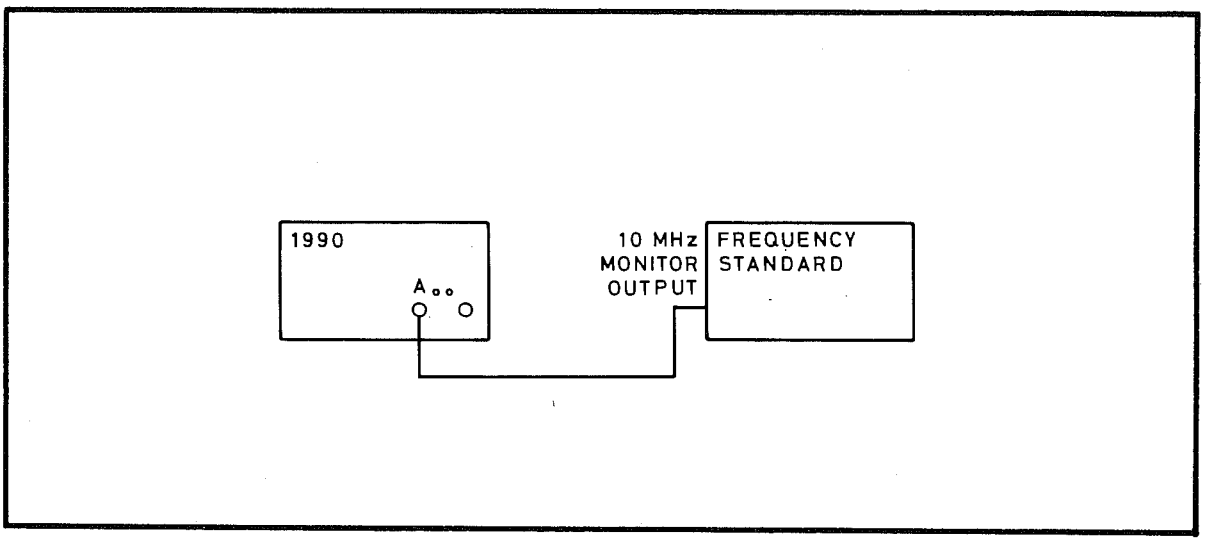


Fig 7.28 Connections for Internal Frequency Standard PVP: Standard Oscillator and TXCO Option

(3) Verify that the value displayed is within the limits shown in Table 7.12.

TABLE 7.12

Internal Frequency Standard Accuracy: Standard Oscillator and TXCO Option

Frequency Standard	1990 Display Limits	Accuracy
Standard Oscillator	9.999985 E6 to 10.000015 E6	15 parts in 10^7
Option 04T (TXCO)	9.999997 R6 to 10.000003 E6	3 parts in 10^7

73

Item	Table 7.1 Item No.
Frequency standard	4
High resolution counter	6
Connecting Leads	7

(1) Ensure that the 1990 has been switched on for 24 hours prior to making measurements.

(2) Connect the test equipment as shown in Fig 7.29

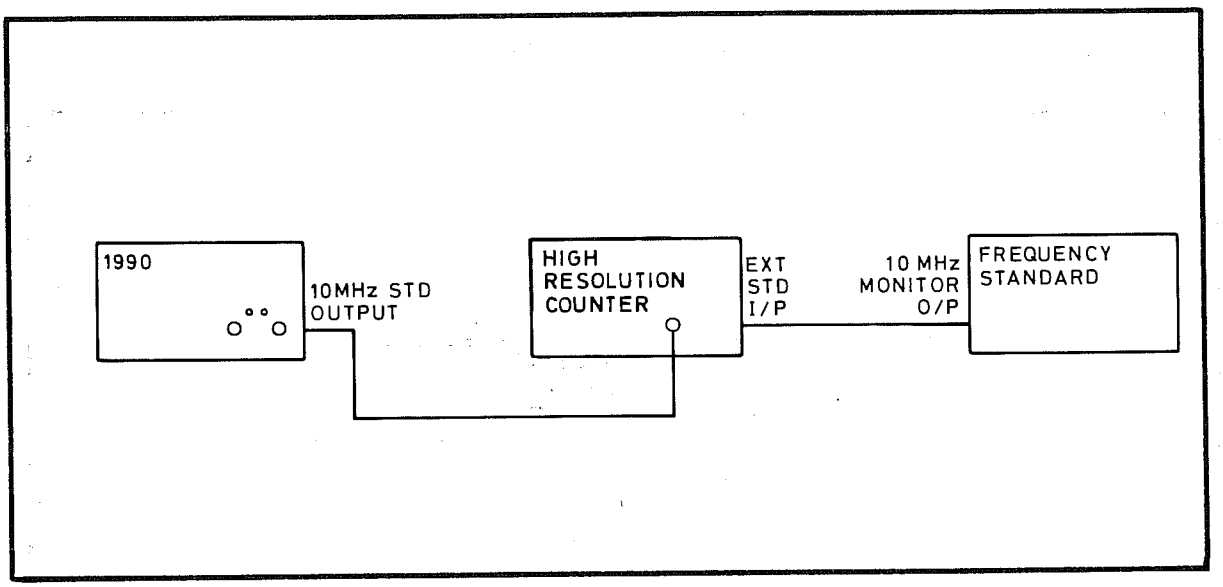


Fig 7.29 Connectors for Internal Frequency Standard PVP: Ovened Oscillator Options

(3) Set up the high resolution counter for an external frequency standard, and a resolution of 9 digits.

(4) Verify that the frequency displayed on the 1991 is within the limits shown in Table 7.13.

TABLE 7.13

Internal Frequency Standard Accuracy: Ovened Oscillator Options

Frequency Standard	High Res Counter Display Limits	Accuracy
Option 04A	9.999999 70 E6 to 10.00000030 E6	3 parts in 10^9
Option 04B	9.999999 97 E6 to 10.00000003 E6	3 parts in 10^9

(5) Switch off the 1990. Switch off and disconnect the test equipment.

PARTS LIST

BNC MOUNTING BOARD 19-3003

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
		PC Board			18-1206
SK19		Connector			23-5159
SK20		Connector			23-5159
SK24		BNC socket			23-3421
SK26		BNC socket			23-3421

PARTS LIST

DISPLAY ASSEMBLY 19-3002

Fig 3

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Resistors			W		
R1	10k		0.1	5	20-1538
R2	820		0.1	5	20-1535
R3/S20	10k	POT (Modified)		20	16-6001
R4	820		0.1	5	20-1538
R5/S21	10k	POT (Modified)		20	16-6001
R6	9x10k	SIL Array			20-5521
R7	10k		0.1	5	20-1538
R8	10k		0.1	5	20-1538
Capacitors			V		
C1	100n	Ceramic	50	20	21-1708
C2	100n	Ceramic	50	20	21-1708
C3	100n	Ceramic	50	20	21-1708
C4	4.7µ	Electrolytic	63	20	21-0750
C5	100n	Ceramic	50	20	21-1708
C6	100n	Ceramic	50	20	21-1708
C7	100n	Ceramic	50	20	21-1708
Diodes					
D1		Silicon 1N4149			22-1029
LP1		LED red			26-5026
LP2		LED red			26-5026
LP3		LED red			26-5026
LP4		LED red			26-5026
LP5		LED red			26-5026
LP6		LED red			26-5026
LP7		LED red			26-5026
LP8		LED red			26-5026
LP9		LED red			26-5026
LP10		LED red			26-5026
LP11		LED red			26-5026
LP12		LED red			26-5026
LP13		LED red			26-5026
LP14		LED orange			26-5027
LP15		LED red			26-5026

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
LP16		LED red			26-5026
LP17		LED red			26-5026
LP18		LED red			26-5026
LP19		LED red			26-5026
LP20		LED red			26-5026
LP21		LED red			26-5026
LP22		LED red			26-5026
LP23		LED red			26-5026
LP24		LED red			26-5026
LP25		LED red			26-5026
LP26		LED red			26-5026
LP27		LED red			26-5026
LP28		LED red			26-5026
LP29		LED red			26-5026
LP30		LED red			26-5026
LP31		LED red			26-5026
LP32		LED red			26-5026
LP33		LED red			26-5026
LP34		LED red			26-5026
LP35		LED red			26-5026
Integrated Circuits					
IC1		MM74C922N			22-4779
IC2		7218AIJI			22-4778
IC3		7218AIJI			22-4778
Displays					
D11		Seven-segment display; double digit			26-1512
D12		Seven-segment display; double digit			26-1512
D13		Seven-segment display; double digit			26-1512
D14		Seven-segment display; double digit			26-1512
D15		Seven-segment display; single digit			26-1511
Miscellaneous					
S1-S19		Switch			23-4125
SK1		Socket 14 way			23-5160
SK2		Socket 16 way			23-5185
		Button Grey			15-0703
		Button Blue			15-0705

PARTS LIST

MOTHERBOARD ASSEMBLY 19-3004

Figs 5, 6 and 7

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Resistors			W		
R1	10	Chip		5	20-5771
R2	10	Chip		5	20-5771
R3	100	Chip		5	20-5764
R4	100	Chip		5	20-5764
R5	12	Chip		5	20-5772
R6	12	Chip		5	20-5772
R7	68	Chip		5	20-5780
R8	68	Chip		5	20-5780
R9	900k		0.5	0.25	20-7523
R10	111k		0.25	0.25	20-7522
R11	900k		0.5	0.25	20-7523
R12	111k		0.25	0.25	20-7522
R13	10	Chip		5	20-5771
R14	150	Chip		5	20-5783
R15	100	Chip		5	20-5764
R16	150k		0.5	5	20-3154
R17	150k		0.5	5	20-3154
R18	470	Chip		5	20-5765
R19	470	Chip		5	20-5765
R20	470	Chip		5	20-5765
R21	442k		0.25	1	20-7551
R22	412k		0.25	1	20-7550
R23	470	Chip		5	20-5765
R24	442k		0.25	1	20-7551
R25	412k		0.25	1	20-7550
R26	47	Chip		5	20-5778
R27	330	Chip		5	20-5787
R28	470	Chip		5	20-5765
R29		Not Used			
R30	330	Chip		5	20-5787
R31	470	Chip		5	20-5765
R32	3.3k	Chip		5	20-5797
R33	10k	POT			20-7071
R34	4.7k	Chip		5	20-5799
R35	3.3k	Chip		5	20-5797

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
R36	10k	POT			20-7071
R37	4.7k	Chip		5	20-5799
R38	220	Chip		5	20-5785
R39	1k	Chip		5	20-5792
R40	1k	Chip		5	20-5792
R41	27k	Chip		5	20-5806
R42	220	Chip		5	20-5785
R43	1k	Chip		5	20-5792
R44	1k	Chip		5	20-5792
R45	27k	Chip		5	20-5806
R46	10	Chip		5	20-5771
R47	10k	Chip		5	20-5768
R48	412k		0.25	1	20-7550
R49	442k		0.25	1	20-7551
R50	10k	Chip		5	20-5768
R51	412k		0.25	1	20-7550
R52	442k		0.25	1	20-7551
R53	470	Chip		5	20-5765
R54	1k	Chip		5	20-5792
R55	470	Chip		5	20-5765
R56	1k	Chip		5	20-5792
R57	10	Chip		5	20-5771
R58	180	Chip		5	20-5784
R59	180	Chip		5	20-5784
R60	3.3k	Chip		5	20-5797
R61	3.3k	Chip		5	20-5797
R62	3.3k	Chip		5	20-5797
R63	3.3k	Chip		5	20-5797
R64	4.7k	Chip		5	20-5799
R65	4.7k	Chip		5	20-5799
R66	4.7	Chip		5	20-5866
R67	4.7	Chip		5	20-5866
R67	47	Chip		5	20-5778
R68	4.7	Chip		5	20-5866
R69	47	Chip		5	20-5778
R70	10k	Chip		5	20-5768

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
R71	10k	Chip		5	20-5768
R72	10k	POT			20-7071
R73	10k	POT			20-7071
R74	330	Chip		5	20-5787
R75	330	Chip		5	20-5787
R76	330	Chip		5	20-5787
R77	330	Chip		5	20-5787
R78	10k	Chip		5	20-5768
R79	1.5k	Chip		5	20-5794
R80	220	Chip		5	20-5785
R81	10	Chip		5	20-5771
R82	330	Chip		5	20-5787
R83	330	Chip		5	20-5787
R84		Not Used			
R85	68	Chip		5	20-5780
R86		Not Used			
R87	100k	Chip		5	20-5813
R88	4.7k	Chip		5	20-5799
R89	4.7k	Chip		5	20-5799
R90	6.8k	Chip		5	20-5801
R91	100k	Chip		5	20-5813
R92	10k	Chip		5	20-5768
R93	10k	Chip		5	20-5768
R94	2.2k	Chip		5	20-5796
R95	10k	Chip		5	20-5768
R96	68	Chip		5	20-5780
R97	10k	Chip		5	20-5768
R98	4.7k	Chip		5	20-5799
R99	2.2k	Chip		5	20-5796
R100	4.7k	Chip		5	20-5799
R101	10k	Chip		5	20-5768
R102	10k	Chip		5	20-5768
R103	10k	Chip		5	20-5768
R104	100k	Chip		5	20-5813
R105	1k	Chip		5	20-5792
R106	330	Chip		5	20-5787
R107	10k	Chip		5	20-5768
R108	10k	Chip		5	20-5768
R109	1k	Chip		5	20-5792
R110	10k	Chip		5	20-5768

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
R111	1k	Chip		5	20-5792
R112	1k	Chip		5	20-5792
R113	120k	Chip		5	20-5851
R114	1k	Chip		5	20-5792
R115	3.3k	Chip		5	20-5797
R116	470	Chip		5	20-5765
R117	1k	Chip		5	20-5792
R118	470	Chip		5	20-5765
R119	1k	Chip		5	20-5792
R120	1k	Chip		5	20-5792
R121	1k	Chip		5	20-5792
R122	150	Chip		5	20-5783
R123	1.5k	Chip		5	20-5794
R124	1.5k	Chip		5	20-5794
R125	150	Chip		5	20-5783
R126	9x1k	S.I.L. Array			20-5541
R127	220	Chip		5	20-5785
R128	4.7k	Chip		5	20-5799
R129	4.7k	Chip		5	20-5799
R130	1k	Chip		5	20-5792
R131	1.5k	Chip		5	20-5794
R132	5x10k	S.I.L. Array			20-5562
R133		Not Used			
R134	1k	Chip		5	20-5792
R135	1k	Chip		5	20-5792
R136	1k	Chip		5	20-5792
R137	220	Chip		5	20-5785
R138	4.7k	Chip		5	20-5799
R139	120		0.25	5	20-2121
R140		S.I.L. Array			20-5556
R141	120		0.25	5	20-2121
R142	120		0.25	5	20-2121
R143	1k	Chip		5	20-5792
R144	220	Chip		5	20-5785
R145	18	Chip		5	20-5763
R146	68	Chip		5	20-5780
R147	1k	Chip		5	20-5792
R148	10	Chip		5	20-5771

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Capacitors			V		
C1	20n	Chip	400		21-1847
C2	20n	Chip	400		21-1847
C3	6.8p	Chip	400		21-1859
C4	47p	Chip	50		21-1795
C5	6.8p	Chip	400		21-1859
C6	47p	Chip	50		21-1795
C7	10n	Chip	50		21-1801
C8	33p	Chip	400		21-1865
C9	10n	Chip	50		21-1801
C10	10n	Chip	50		21-1801
C11	33p	Chip	400		21-1865
C12	10n	Chip	50		21-1801
C13	10n	Chip	50		21-1801
C14	10n	Chip	50		21-1801
C15	33n	Chip	50		21-1808
C16	3.3n	Chip	50		21-1858
C17	33n	Chip	50		21-1808
C18	100n	Ceramic	50		21-1647
C19	100n	Ceramic	50		21-1647
C20	10n	Chip	50		21-1801
C21	47µ	Electrolytic	25		21-0789
C22	10n	Chip	50		21-1801
C23	10n	Chip	50		21-1801
C24	10n	Chip	50		21-1801
C25	10n	Chip	50		21-1801
C26	10n	Chip	50		21-1801
C27	10n	Chip	50		21-1801
C28	10n	Chip	50		21-1801
C29	47µ	Electrolytic	25		21-0789
C30	47µ	Electrolytic	25		21-0789
C31	47µ	Electrolytic	25		21-0789
C32	10n	Chip	50		21-1801
C33	10n	Chip	50		21-1801
C34	10n	Chip	50		21-1801
C35		Not Used			

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
C36		Not Used			
C37	10n	Chip	50		21-1801
C38	47µ	Electrolytic	25		21-0789
C39	10n	Chip	50		21-1801
C40	47µ	Electrolytic	25		21-0789
C41	47µ	Electrolytic	25		21-0789
C42	47µ	Electrolytic	25		21-0789
C43	10n	Chip	50		21-1801
C44	10n	Chip	50		21-1801
C45	10n	Chip	50		21-1801
C46	47µ	Electrolytic	25		21-0789
C47	10n	Chip	50		21-1801
C48	47µ	Electrolytic	25		21-0789
C49	10n	Chip	50		21-1801
C50	33n	Chip	50		21-1808
C51	10n	Chip	50		21-1801
C52	47µ	Electrolytic	25		21-0789
C53		Not Used			
C54		Not Used			
C55	10n	Chip	50		21-1801
C56	10n	Chip	50		21-1801
C57	1µ	Electrolytic	50		21-0779
C58	1n	Chip	50		21-1800
C59	33n	Chip	50		21-1808
C60	47µ	Electrolytic	25		21-0789
C61	1µ	Electrolytic	50		21-0779
C62	33n	Chip	50		21-1808
C63	33n	Chip	50		21-1808
C64	33n	Chip	50		21-1808
C65	20n	Chip	50		21-1847
C66	47n	Polypropylene	250		21-7003
C67	10n	Chip	50		21-1801
C68	2.5n	Polypropylene	250		21-7002
C69	2.5n	Polypropylene	250		21-7002
C70	10n	Chip	50		21-1801
C71	10n	Chip	50		21-1801
C72	33n	Chip	50		21-1808
C73	47µ	Electrolytic	25		21-0789
C74	220µ	Electrolytic	25		21-0794
C75	220µ	Electrolytic	25		21-0794

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
C76	10,000µ	Electrolytic	16		21-0683
C77	4700µ	Electrolytic	16		21-0667
C78	10n	Chip	50		21-1801
C79	10n	Chip	50		21-1801
C80	47µ	Electrolytic	25		21-0789
C81	1µ	Electrolytic	50		21-0779
C82	220p	Chip	50		21-1838
C83	220p	Chip	50		21-1838
C84	220p	Chip	50		21-1838
C85	10n	Chip	50		21-1801
C86	47µ	Electrolytic	25		21-0789
C87	47µ	Electrolytic	25		21-0789
C88	47µ	Electrolytic	25		21-0789
C89	47µ	Electrolytic	25		21-0789
C90	10n	Chip	50		21-1801
C91	47µ	Electrolytic	25		21-0789
C92	33n	Chip	50		21-1808
C93	33n	Chip	50		21-1808
C94	4.7µ	Electrolytic	50		21-0785
C95	4.7µ	Electrolytic	50		21-0785
C96	4.7µ	Electrolytic	50		21-0785
C97	4.7µ	Electrolytic	50		21-0785
Diodes					
D1		Zener BZX84C2V7			22-1876
D2		Silicon BAT18			22-1098
D3		Silicon BAT18			22-1098
D4		Zener BZX84C2V7			22-1876
D5		Zener BZX84C2V7			22-1876
D6		Silicon BAT18			22-1098
D7		Silicon BAT18			22-1098
D8		Zener BZX84C2V7			22-1876
D9		Dual BAV99			22-1096
D10		Not used			
D11		Not used			
D12		Dual BAV99			22-1096
D13		Silicon BAS16			22-1093
D14		Silicon BAS16			22-1093
D15		Dual BAV99			22-1096
D16		Dual BAV99			22-1096
D17		Dual BAV99			22-1096
D18		Bridge Rectifier VH248			22-1662
D19		Zener BZX84C12V			22-1892
D20		Zener BZX84C12V			22-1892

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
D21		Silicon BAS16			22-1093
D22		Zener BZX79B5V1			22-1857
D23		Silicon BAS16			22-1093
D24		Silicon BAS16			22-1093
Transistors					
Q1		BF256A			22-6163
Q2		BF256A			22-6163
Q3		BFS17			22-6206
Q4		BFS17			22-6206
Q5		3906			22-6199
Q6		3906			22-6199
Q7		BFS17			22-6206
Q8		BFS17			22-6206
Q9		CA3083			22-4216
Q10		3906			22-6199
Q11		3906			22-6199
Q12		3904			22-6197
Q13		3906			22-6199
Q14		MPS3640			22-6018
Q15		3904			22-6197
Q16		MPS3640			22-6018
Q17		BDT92			22-6153
Q18		3904			22-6197
Q19		BDT92			22-6153
Q20		3904			22-6197
Q21		3906			22-6199
Q22		BDT91			22-6152
Q23		MPS3640			22-6018
Integrated Circuits					
IC1		MC3403			22-4262
IC2		74HCT373			22-4808
IC3		MC146805E2			22-8307
IC4		MCC1			22-8403
IC5		Programmed ROM			22-8586

NOTE: When ordering a replacement for IC5 it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
IC6		74LS04			22-4533
IC7		74LS373			22-4585
IC8		74HCT373			22-4808
IC9		74LS32			22-4578
IC10		74LS74			22-4534
IC11		74HCT244			22-4807
IC12		40106			22-4756
IC13		4011			22-4700
IC14		74LS138			22-4587
IC15		74LS10			22-4557
IC16		10116			22-4528
IC17		10116			22-4528
IC18		MCC2			22-8404
IC19		Not Used			
IC20		9687DG			22-4686
IC21		CA3140E			22-4269
IC22		CA3140E			22-4269
Inductor					
L1	100µH	Choke			23-7213
L2	100µH	Choke			23-7213
L3	100µH	Choke			23-7213
L4	100µH	Choke			23-7213
L5	100µH	Choke			23-7213
L6	100µH	Choke			23-7213
L7	100µH	Choke			23-7213
L8	40µH	Choke Mains			23-7217
L9	40µH	Choke Mains			23-7217
Connectors					
PL1		Plug 2 x 7			23-5162
PL2		Plug 2 x 8			23-5184
PL3		Not Used			
PL4		Not Used			
PL5		Not Used			
PL6		Not Used			
PL7		Not Used			
PL8		Not Used			
PL9		Not Used			
PL10		Not Used			

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
PL11		Not Used			
PL12		Not Used			
PL13		Not Used			
PL14		Plug 6 way			23-5188
PL15		Plug 5 way			23-5164
PL16		Plug 10 way			23-5165
PL17		Plug 5 way			23-5164
PL18		Not Used			
PL19		Plug 2 x 2			23-5161
PL20		Plug 2 x 2			23-5161
PL21		Plug 2 x 10			23-5168
SK1		Not Used			
SK2		Not Used			
SK3		Not Used			
SK4		IC socket 28 way			23-3290
SK5		BNC socket			17-1039
SK6		BNC socket			17-1039
SK7		Not Used			
SK8		Mains Selector Socket			23-5177
SK9		Not Used			
SK10		Mains Socket			23-3429
Miscellaneous					
FS1		Fuse Holder			23-0062
LK1		Link			23-5180
LK2		Link			23-5180
S1		Mains Switch			23-4124
T1		Mains Transformer			17-4102
RLA		Relay G57DX424			23-7529
RLB		Relay G57DX424			23-7529
RLC		Relay G57DX423			23-7528
RLD		Relay G57DX423			23-7528
RLE		Relay G57DX424			23-7529
RLF		Relay G57DX424			23-7529
RLG		Relay GT831C-238			23-7530
OSC1		Crystal Oscillator 10MHz			23-9134

PARTS LIST

GPIB ASSEMBLY 19-1146

Fig 9

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Resistors	Ω		W		
R1	9x3.3k	SIL Array			20-5532
R2	56	Carbon Film	0.25	5	20-2560
R3	9x3.3k	SIL Array			20-5532
R4	330	Carbon Film	0.25	5	20-2331
R5	330	Carbon Film	0.25	5	20-2331
R6	330	Carbon Film	0.25	5	20-2331
R7	5x3.3k	SIL Array			20-5531
R8	18	Carbon Film	0.25	5	20-2180
R9	56	Carbon Film	0.25	5	20-2560
R10	9x100k	SIL Array			20-5522
R11	5x100k	SIL Array			20-5558
Capacitors	F		V		
C1	47µ	Electrolytic	25	20	21-0789
C2	100n	Ceramic	50	20	21-1708
C3	100n	Ceramic	50	20	21-1708
C4	100n	Ceramic	50	20	21-1708
C5	100n	Ceramic	50	20	21-1708
C6	100n	Ceramic	50	20	21-1708
C7	100n	Ceramic	50	20	21-1708
C8	100n	Ceramic	50	20	21-1708
C9	10n	Ceramic	25	-20+80	21-1545
C10	10n	Ceramic	25	-20+80	21-1545
Integrated Circuits					
IC1		74HCT374			22-4809
IC2		74HCT374			22-4809
IC3		74HCT138			22-4806
IC4		7407			22-4063
IC5		74LS125			22-4657

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
IC6		74HCT02			22-4801
IC7		74HCT00			22-4800
IC8		74HCT138			22-4806
IC9		MC146805E2			22-8307
IC10		Programmed ROM			22-8587
NOTE: When ordering a replacement for IC10, it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.					
IC11		74HCT373			22-4808
IC12		68488			22-8305
IC13		4066			22-4761
IC14		75161			22-4284
IC15		75160			22-4283
IC16		74HCT74			22-4805
IC17		74HCT74			22-4805
IC18		74HCT00			22-4800
IC19		74HCT02			22-4801
IC20		74HCT32			22-4804
Miscellaneous					
		IC Socket, 28-way			23-3290
		IC Socket, 40-way			23-3297
		IC Socket, 14-way			23-3309
SK3		Connector, 24-way			23-3434
S1		Switch, 6-way, DIL			23-4102

PARTS LIST

REFERENCE FREQUENCY MULTIPLIER ASSEMBLY 19-1164

Fig 11

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Resistors	Ω		W		
R1	220	Chip	0.125	5	20-5785
R2	10k	Chip	0.125	5	20-5768
R3	12k	Chip	0.125	5	20-5802
R4	1.8k	Chip	0.125	5	20-5795
R5	100k	Chip	0.125	5	20-5813
R6	560k	Chip	0.125	5	20-5817
R7	10k	Chip	0.125	5	20-5768
R8	2.2k	Chip	0.125	5	20-5796
R9	2.2k	Chip	0.125	5	20-5796
R10	560	Chip	0.125	5	20-5789
R11	1.8k	Chip	0.125	5	20-5795
R12	330	Chip	0.125	5	20-5787
R13	2.2k	Chip	0.125	5	20-5796
R14	10k	Chip	0.125	5	20-5768
R15	10k	Chip	0.125	5	20-5768
R16	820	Chip	0.125	5	20-5791
R17	56	Chip	0.125	5	20-5779
R18	330	Chip	0.125	5	20-5787
R19	1.8k	Chip	0.125	5	20-5795
R20	56	Chip	0.125	5	20-5779
R21	56	Chip	0.125	5	20-5779
R22	820	Chip	0.125	5	20-5791
R23	1.8k	Chip	0.125	5	20-5795
R24	1.8k	Chip	0.125	5	20-5795
R25	1.8k	Chip	0.125	5	20-5795
R26	1.8k	Chip	0.125	5	20-5795
R27	220	Chip	0.125	5	20-5785
R28	220	Chip	0.125	5	20-5785
R29	220	Chip	0.125	5	20-5785
R30	220	Chip	0.125	5	20-5785
R31	220	Chip	0.125	5	20-5785

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	33n	Chip	50	10	21-1808
C2	2-15p	Variable			21-6043
C3	220p	Chip	50	5	21-1838
C4	220p	Chip	50	5	21-1838
C5	33n	Chip	50	10	21-1808
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	10n	Chip	50	20	21-1801
C9	10n	Chip	50	20	21-1801
C10	10n	Chip	50	20	21-1801
C11	10n	Chip	50	20	21-1801
C12	10n	Chip	50	20	21-1801
C13	33n	Chip	50	10	21-1808
C14	33n	Chip	50	10	21-1808
C15	10n	Chip	50	20	21-1801
Diodes					
D1		Varactor (MV1640)			22-1097
D2		Silicon (BAS16)			22-1093
D3		Voltage regulator (BZX84C4V7)			22-1882
D4		Silicon (BAV99)			22-1096
D5		Silicon (BAV99)			22-1096
Transistor					
Q1		3904			22-6197
Q2		3906			22-6199
Q3		3906			22-6199
Q4		3904			22-6197
Q5		3904			22-6197
Q6		3904			22-6197
Q7		3904			22-6197
Integrated Circuits					
IC1		Not Used			
IC2		741			22-4292
IC3		MC10102			22-4514
IC4		74LS132			22-4582

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Connectors					
SK16		Socket, 5-way			23-5166
SK17		Socket, 10-way			23-5167
Transformer					
T1		Transformer to Racal-Dana specification			17-3226

PARTS LIST

REFERENCE FREQUENCY DOUBLER ASSEMBLY 19-1238

Fig 13

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
	Ω		W		
R1	33	Chip	0.125	5	20-5776
R2	100	Chip	0.125	5	20-5764
R3	100	Chip	0.125	5	20-5764
R4	1k	Chip	0.125	5	20-5792
R5	470	Chip	0.125	5	20-5765
R6	470	Chip	0.125	5	20-5765
R7	1.5k	Chip	0.125	5	20.5794
R8	3.9k	Chip	0.125	5	20-5798
R9	3.9k	Chip	0.125	5	20-5798
R10	1.5k	Chip	0.125	5	20-5794
R11	1k	Chip	0.125	5	20-5792
R12	39k	Chip	0.125	5	20-5808
R13	15k	Chip	0.125	5	20-5803
R14	330k	Chip	0.125	5	20-5816
R15	10k	Chip	0.125	5	20-5768
R16	1k	Chip	0.125	5	20-5792
R17	3.9k	Chip	0.125	5	20-5798
R18	3.9k	Chip	0.125	5	20-5798
R19	100	Chip	0.125	5	20-5764
R20	1k	Chip	0.125	5	20-5792
Capacitors					
	F		V		
C1	10n	Chip	50	20	21-1801
C2	10n	Chip	50	20	21-1801
C3	10n	Chip	50	20	21-1801
C4	10n	Chip	50	20	21-1801
C5	10n	Chip	50	20	21-1801
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	10n	Chip	50	20	21-1801

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Diodes					
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
Transistors					
Q1		2N3906			22-6008
Q2		2N3906			22-6008
Q3		2N3904			22-6007
Q4		2N3904			22-6007
Q5		2N3904			22-6007
Q6		2N3904			22-6007
Inductors					
	H				
L1	100µ	Choke		10	23-7213
T1		10.7 MHz IF Transformer			23-7149
T2		10.7 MHz IF Transformer			23-7149

PARTS LIST

OSCILLATOR ASSEMBLY 19-1208

Fig 14

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors	F		V		
C1	100n	Ceramic	50	20	21-1708
Connector					
SK14		Connector, 5-way			23-5166
Oscillator					
	10MHz	Oscillator, temperature compensated			23-9135

PARTS LIST

BATTERY PACK 11-1625

Fig 17

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
CHASSIS COMPONENTS					
	Ω		W		
R1	5.6	Wire Wound	10	5	20-5081
		Battery Chassis Assembly (complete with batteries B1 and B2)			11-1723
		Cableform			10-2906
FS2		Fuselink 1¼ in x ¼ in	3AT		23-0069
FS3		Fuselink 1¼ in x ¼ in	3AT		23-0069
BATTERY BOARD ASSEMBLY 19-1203					
Resistors					
	Ω		W		
R1	39	Carbon Film	0.25	5	20-2390
R2	1M	Chip	0.125	5	20-5770
R3	4.7k	Chip	0.125	5	20-5799
R4	1M	Chip	0.125	5	20-2560
R5	56	Carbon Film	0.25	5	20-2560
R6	10M	Carbon Film	0.25	10	20-2106
R7	1M	Chip	0.125	5	20-5770
R8	560k	Chip	0.125	5	20-5817
R9	560k	Chip	0.125	5	20-5817
R10	50k	Variable			20-7086
R11	56k	Chip	0.125	5	20-5810
R12	1k	Chip	0.125	5	20-5792
R13	22k	Chip	0.125	5	20-5805
R14	1M	Chip	0.125	5	20-5817
R15	560k	Chip	0.125	5	20-5817

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
R16	1M	Chip	0.125	5	20-5770
R17	10k	Chip	0.125	5	20-5768
R18	1M	Chip	0.125	5	20-5770
R19	1M	Chip	0.125	5	20-5770
R20	1M	Chip	0.125	5	20-5770
R21	10MM	Carbon Film	0.25	10	20-2106
R22	10k	Chip	0.125	5	20-5768
R23	10k	Chip	0.125	5	20-5768
R24	100k	Chip	0.125	5	20-5813
R25	56k	Chip	0.125	5	20-5810
R26	220	Chip	0.125	5	20-5785
R27	1k	Carbon film	0.25	5	20-2102
R28	20k	Variable			20-7116
R29	22k	Chip	0.125	5	20-5805
R30	22k	Chip	0.125	5	20-5805
R31	4.7k	Chip	0.125	5	20-5799
R32	4.7k	Chip	0.125	5	20-5799
R33	180	Carbon Film	0.25	5	20-2181
R34	68	Carbon Film	0.5	5	20-3680
R35	180	Chip	0.125	5	20-5784
R36	50k	Variable			20-7086
R37	220k	Chip	0.125	5	20-5829
R38	10k	Chip	0.125	5	20-5768
R39	3.9k	Chip	0.125	5	20-5798
R40	560	Chip	0.125	5	20-5789
R41	39k	Chip	0.125	5	20-5808
R42	1k	Chip	0.125	5	20-5792
R43	27k	Chip	0.125	5	20-5806
R44	10k	Chip	0.125	5	20-5768
R45	8.2k	Chip	0.125	5	20-5767
R46	1k	Chip	0.125	5	20-5792
R47	1M	Chip	0.125	5	20-5770
R48	100k	Chip	0.125	5	20-5813
R49	10M	Carbon Film	0.25	10	20-2106
R50	150	Carbon Film	0.5	5	20-3151
R51	10k	Chip	0.125	5	20-5768

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	330n	Electrolytic	50		21-0793
C2	10µ	Electrolytic	16		21-0775
C3	100n	Ceramic			21-1708
C4	100n	Ceramic			21-1708
C5	220p	Chip			21-1838
C6	330n	Electrolytic	50		21-0793
C7	10n	Chip			21-1801
C8	1.5µ	Electrolytic	50		21-0787
C9	33n	Ceramic			21-1547
C10	22µ	Electrolytic	16		21-0776
C11	33µ	Electrolytic	25		21-0782
C12	100n	Electrolytic	50		21-0778
C13	10n	Ceramic			21-1752
C14	100n	Electrolytic	50		21-0778
C15	330µ	Electrolytic	40		21-0687
C16	100n	Ceramic			21-1708
C17	100n	Ceramic			21-1708
C18	10µ	Electrolytic	16		21-0716
C19	10µ	Electrolytic	16		21-0716
C20	10n	Chip			21-1801
C21	10n	Chip			21-1801
C22	10n	Chip			21-1801
C23	47µ	Electrolytic	25		21-0789
C24	47µ	Electrolytic	25		21-0789
C25	1µ	Electrolytic	50		21-0779
Diodes					
D1		Silicon (1N4002)			22-1602
D2		Silicon (1N4149)			22-1029
D3		Silicon (1N4149)			22-1029
D4		Silicon (1N4149)			22-1029
D5		Silicon (1N4149)			22-1029

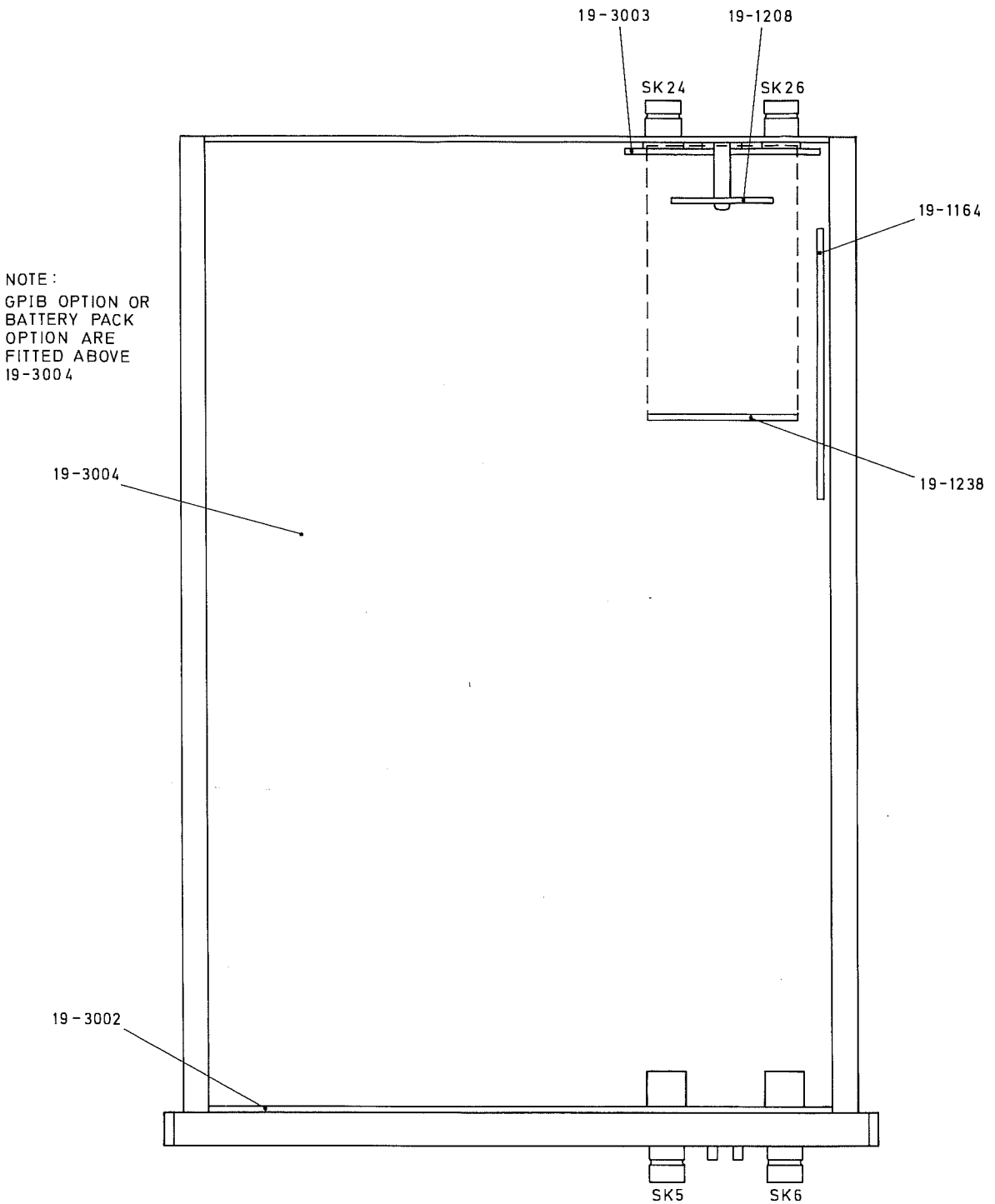
Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
D6		Silicon (1N4149)			22-1029
D7		Avalanche (BYV95A)			22-2009
D8		Avalanche (BYV95A)			22-2009
D9		Schottky (MBR340P)			22-2008
D10		Schottky (MBR340P)			22-2008
D11		Voltage regulator (BZX79B3V9)			22-1825
D12		Silicon (1N4002)			22-1602
D13		Voltage regulator (BZX79B5V6)			22-1856
D14		Silicon (1N4149)			22-1029
D15		Silicon (1N5401)			22-2010
Transformers					
T1					17-4104
Transistors					
Q1		2N3904			22-6007
Q2		2N3906			22-6008
Q3		2N3904			22-6007
Q4		2N3906			22-6008
Q5		BUZ21			22-6208
Q6		2N3904			22-6007
Q7		MJE371			22-6139
Q8		2N3904			22-6007
Q9		2N3904			22-6007
Q10		BDT92			22-6153
Integrated Circuits					
IC1		4072			22-4770
IC2		4030			22-4729
IC3		4001			22-4738
IC4		CA358E			22-4295
IC5		4001			22-4738
IC6		LM339N			22-4249
IC7		LA5632OP			22-4291
IC8		78L05			22-4247

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Connectors					
SK21		Connector 24-way			23-5169
Miscellaneous					
RLA		Relay			23-7531

SWITCH BOARD ASSEMBLY 19-1242

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number
Resistors					
	Ω		W		
R1	100k	Chip	0.125	5	20-5813
R2	10k	Chip	0.125	5	20-5768
R3	10k	Chip	0.125	5	20-5768
R4	100k	Chip	0.125	5	20-5813
R5	1k	Chip	0.125	5	20-5792
R6	1k	Chip	0.125	5	20-5792
R7	10k	Chip	0.125	5	20-5768
R8	100k	Chip	0.125	5	20-5813
R9	10k	Chip	0.125	5	20-5768
R10	10k	Chip	0.125	5	20-5768
Capacitors					
			V		
C1	200µ	Electrolytic	40		21-0686
C2	100n	Ceramic			21-1708
Diodes					
D1		Silicon 1N4002			22-1602
D2		Schottky (MBR340P)			22-2008

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Transistors					
Q1		2N3904			22-6007
Q2		2N3906			22-6008
Q3		2N3906			22-6008
Q4		2N3906			22-6008
Q5		2N3906			22-6008
Q6		2N3906			22-6008
Miscellaneous					
JK1		Socket			23-3433
S1		Switch SPDT			23-4126
S2		Switch DPDT			23-4127
FS1		Fuselink $1\frac{1}{4}$in x $\frac{1}{4}$in	3AT		23-0069
		Fuseholder for FS1			23-0062
		Top for 23-0062			23-0063



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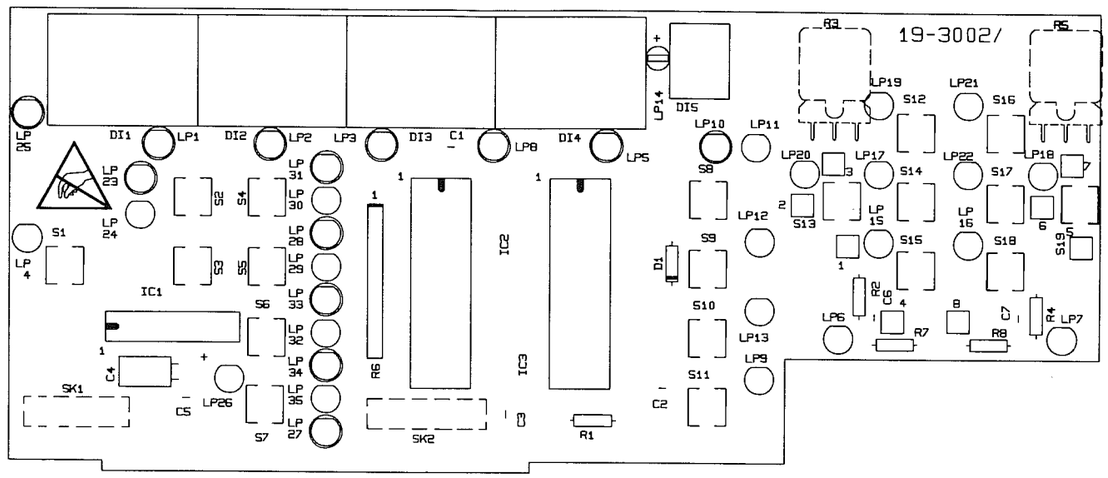
Internal Layout

Fig. 1



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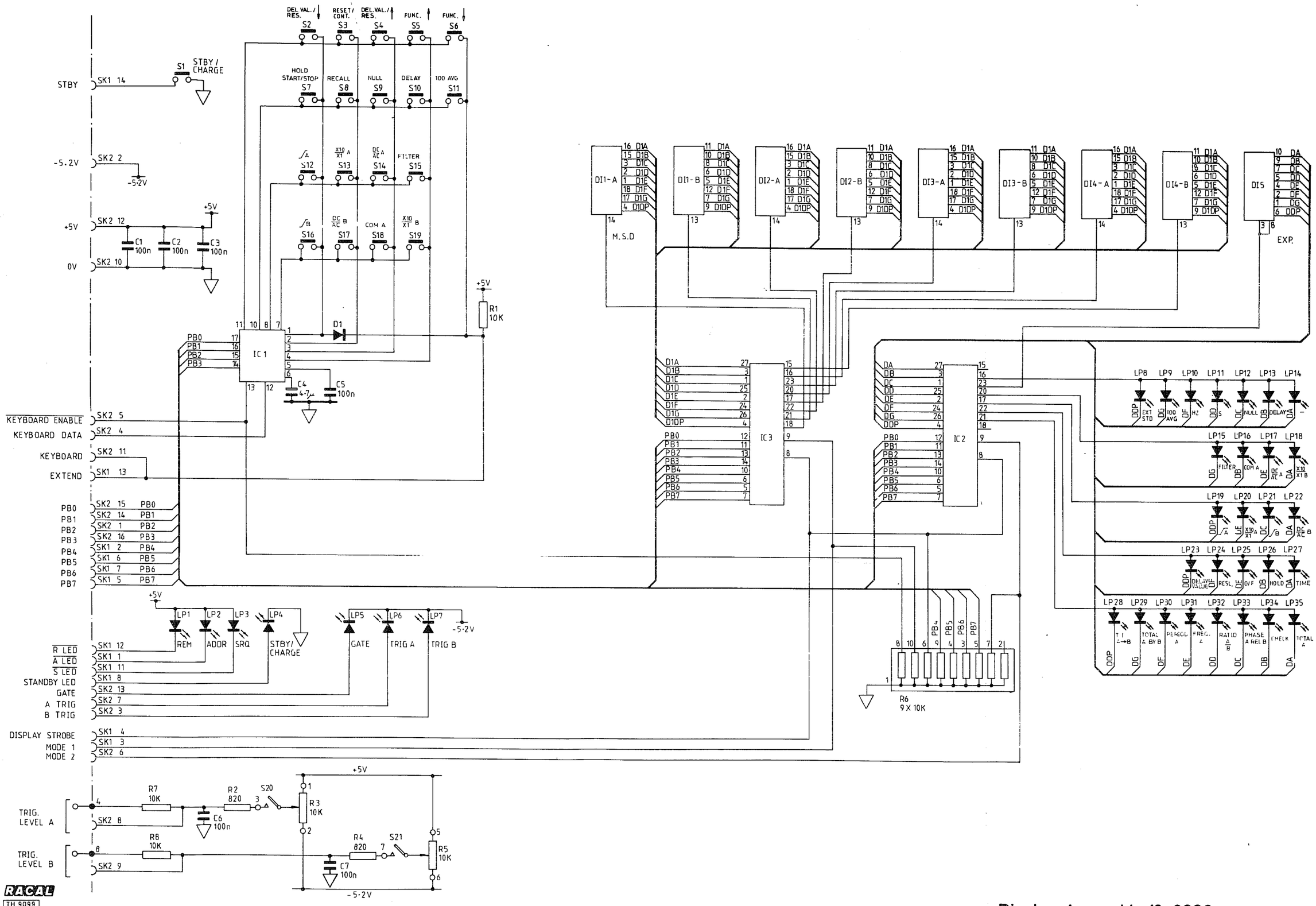
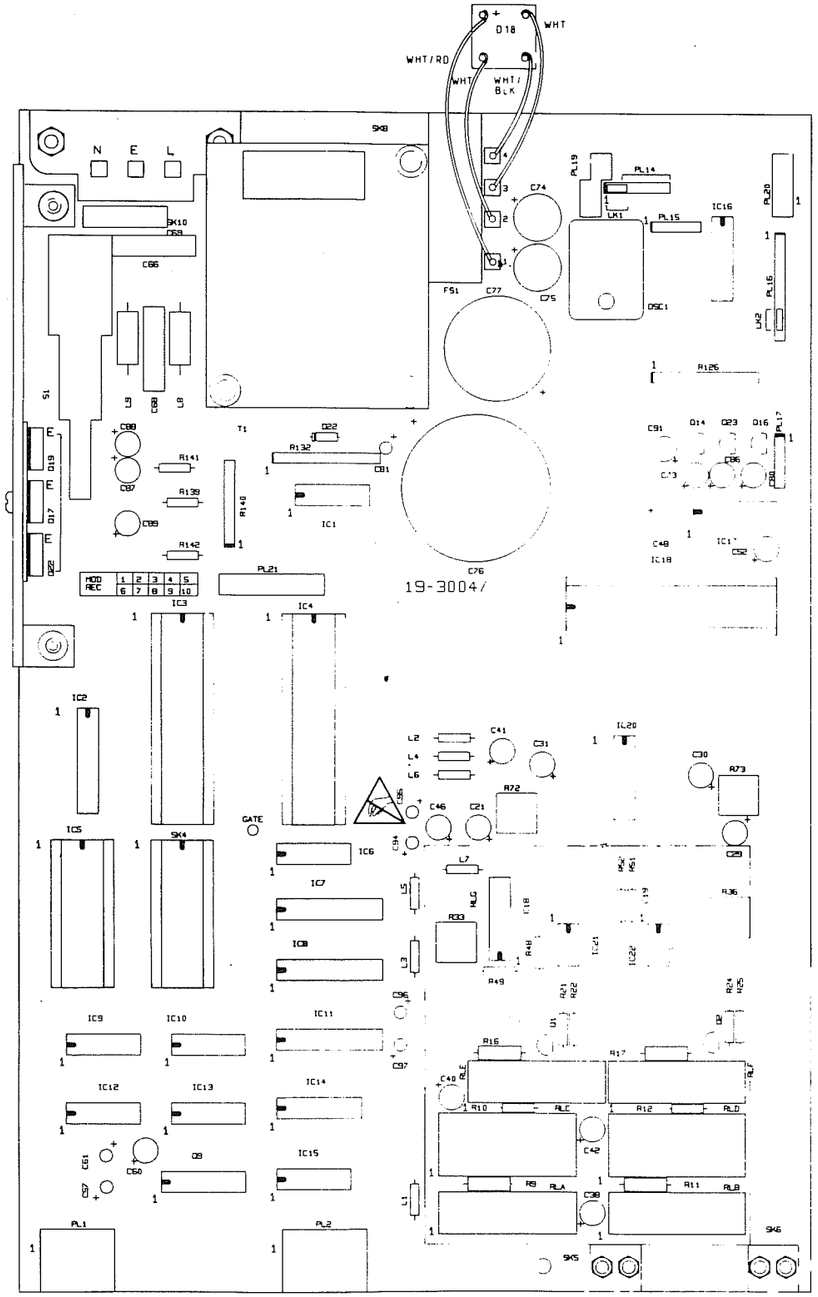
Display Assembly 19-3002 :
Component Layout

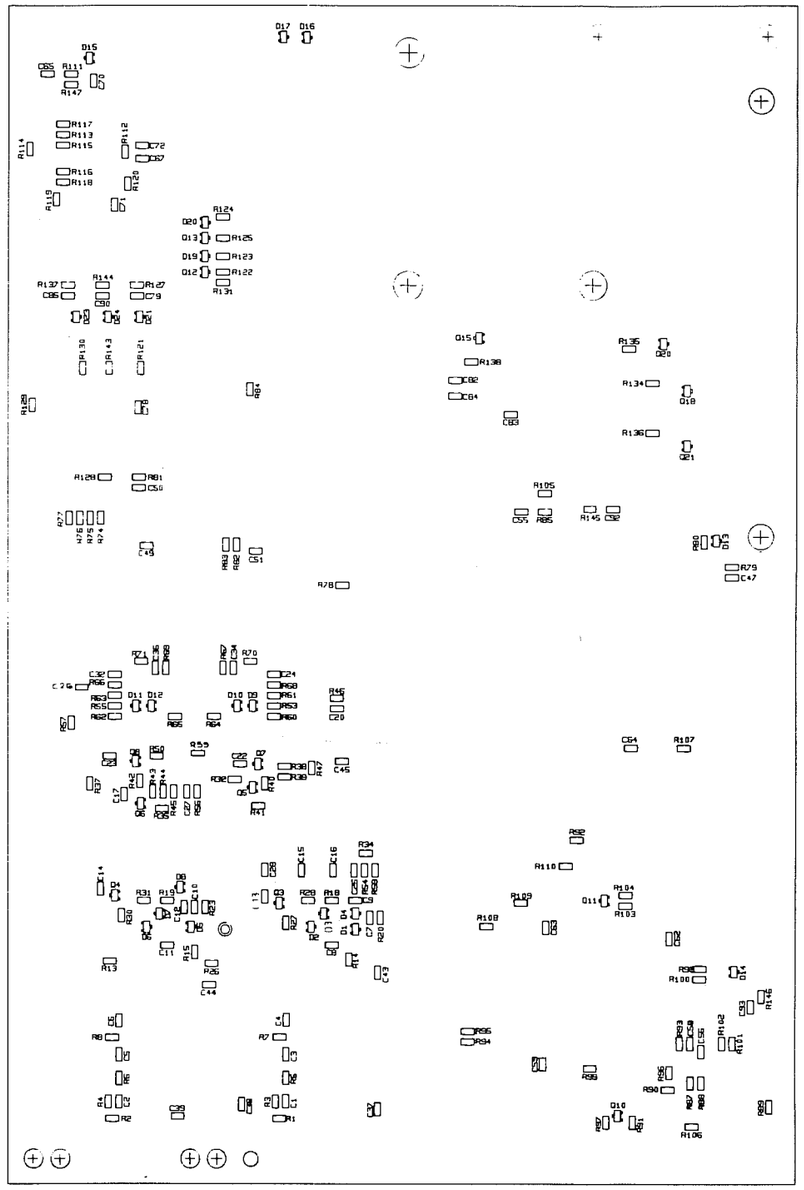
Fig.2



Display Assembly 19-3002 :
Circuit Diagram

Fig. 3





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Motherboard Assembly 19-3004:
Component Layout Fig. 4

SK5
I/P A
RLA 1
R1 10
R3 100
C1 20n
R5 12
AC / DC COUPLING
R9 900K 1/2W 0·25%
RLC 1
C3 6·8p
R7 68
C4 47p
R10 111K 0·25%
X1 / X10 ATTEN.
R14 150
R16 150K 1/2W
C8 33p
C7 10n
D1 2·7V
D2
R20 470
+5V A
C13 10n
Q1
Q3
L.F. FILTER
R27 330
R28 470
-5·2V A
C15 33n
RLG 1
R38 220
Q7
C22 10n
C16 3·3n
R39 1K
D3
D4 2·7V
C9 10n
R18 470
-5·2V A
RLE 1
B COMMON
LIMITER
R21 412K 1/4W 1%
R22 412K 1/4W 1%
+11·2V C
R32 3·3K
IC 21
Q5
'A' OFFSET NULL
R33 10K
R34 4·7K
-11·2V C
R40 1K
R41 27K
C18 100n
R47 10K
R48 412K 1/4W 1%
R49 442K 1/4W 1%
R26 47
R53 470
C24 10n
-5·2V A
+5V A +5V B
C30 47µ
C32 10n
R60 3·3K
D9b D10b D9a D10a
R61 3·3K
-5·2V A
LIMITER
R66 4·7
+5V
IC20a
R64 4·7K
R67 47
C34 10n
R70 10K
R72 10K 'A' HYST SET
-5·2V A
TO SHT.3 IC18 PIN15
TO SHT.3 IC18 PIN16
SHT.4 IC17 PIN4
R58 180
C96 4·7µ
C97 4·7µ
R54 1K
C25 10n
PL2
B
'A' TRIG LEVEL FROM DISPLAY BOARD

SK6
I/P B
RLB 1
R2 10
R4 100
C2 20n
R6 12
AC / DC COUPLING
R11 900K 1/2W 0·25%
RLD 1
C5 6·8p
R8 68
C6 47p
R12 111K 0·25%
X1 / X10 ATTEN
R13 10
RLF 1
B SEPARATE
R15 100
R17 150K 1/2W
C11 33p
C10 10n
D5 2·7V
D6
R23 470
+5V B
C14 10n
Q2
Q4
R30 330
R31 470
-5·2V B
C17 33n
R42 220
Q8
C23 10n
D7
D8 2·7V
C12 10n
R19 470
-5·2V B
LIMITER
R24 442K 1/4W 1%
R25 412K 1/4W 1%
+11·2V C
R35 3·3K
IC 22
Q6
'B' OFFSET NULL
R36 10K
R37 4·7K
-11·2V C
R43 1K
R44 1K
R45 27K
C19 100n
R50 10K
R51 412K 1/4W 1%
R52 442K 1/4W 1%
R55 470
C26 10n
-5·2V B
-5·2V A -5·2V B
C31 47µ
C33 10n
+5V B
R62 3·3K
D11b D12b D11a D12a
R63 3·3K
-5·2V B
LIMITER
R68 4·7
-5·2V
IC20b
R65 4·7K
R69 47
C35 10n
R71 10K
R73 10K 'B' HYST SET
-5·2V B
TO SHT 3 IC18 PIN17
TO SHT 4 IC17 PIN12
SHT 3 IC18 PIN18
R59 180
C94 4·7µ
C95 4·7µ
R56 1K
C27 10n
PL2
9
'B' TRIG LEVEL FROM DISPLAY BOARD

+5V
C36 10n
RLA
RLB
RLC
RLD
RLE
RLF
RLG
C37 10n
C38 47µ
C39 10n
C40 47µ
C41 47µ
C42 47µ
C43 10n
C44 10n
C45 10n
C46 47µ
L1 100µ
L2 100µ
L3 100µ
L4 100µ
L5 100µ
L6 100µ
L7 100µ
TO SHT 3
IC7 PINS 2,5,6,
9,12,15,16
RELAY CONTROL

+11·2V
R46 10
+11·2V C
C20 10n
C21 47µ
R57 10
C28 10n
C29 47µ
-11·2V C
-11·2V

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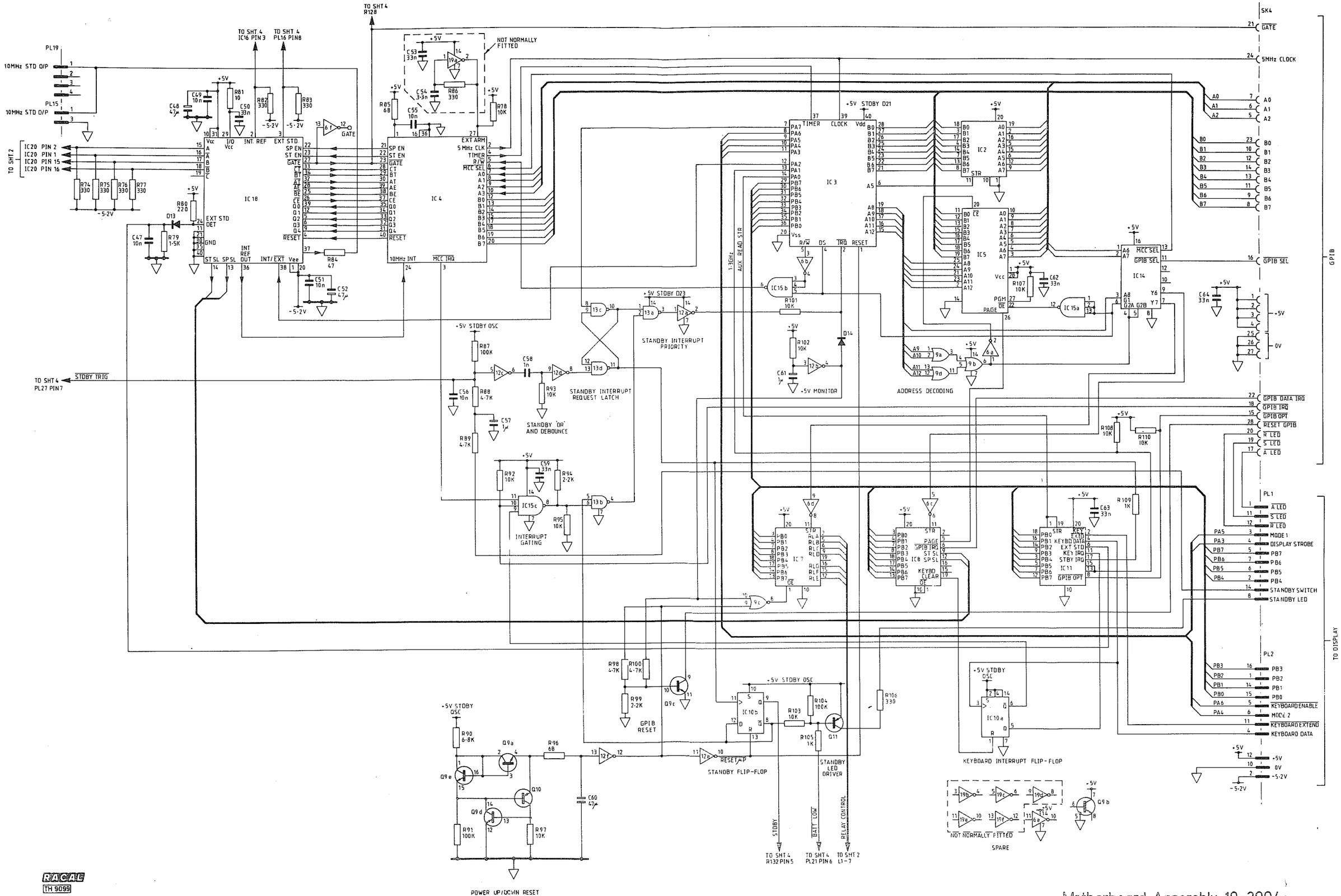
Motherboard Assembly 19-3004:
Circuit Diagram Fig.5



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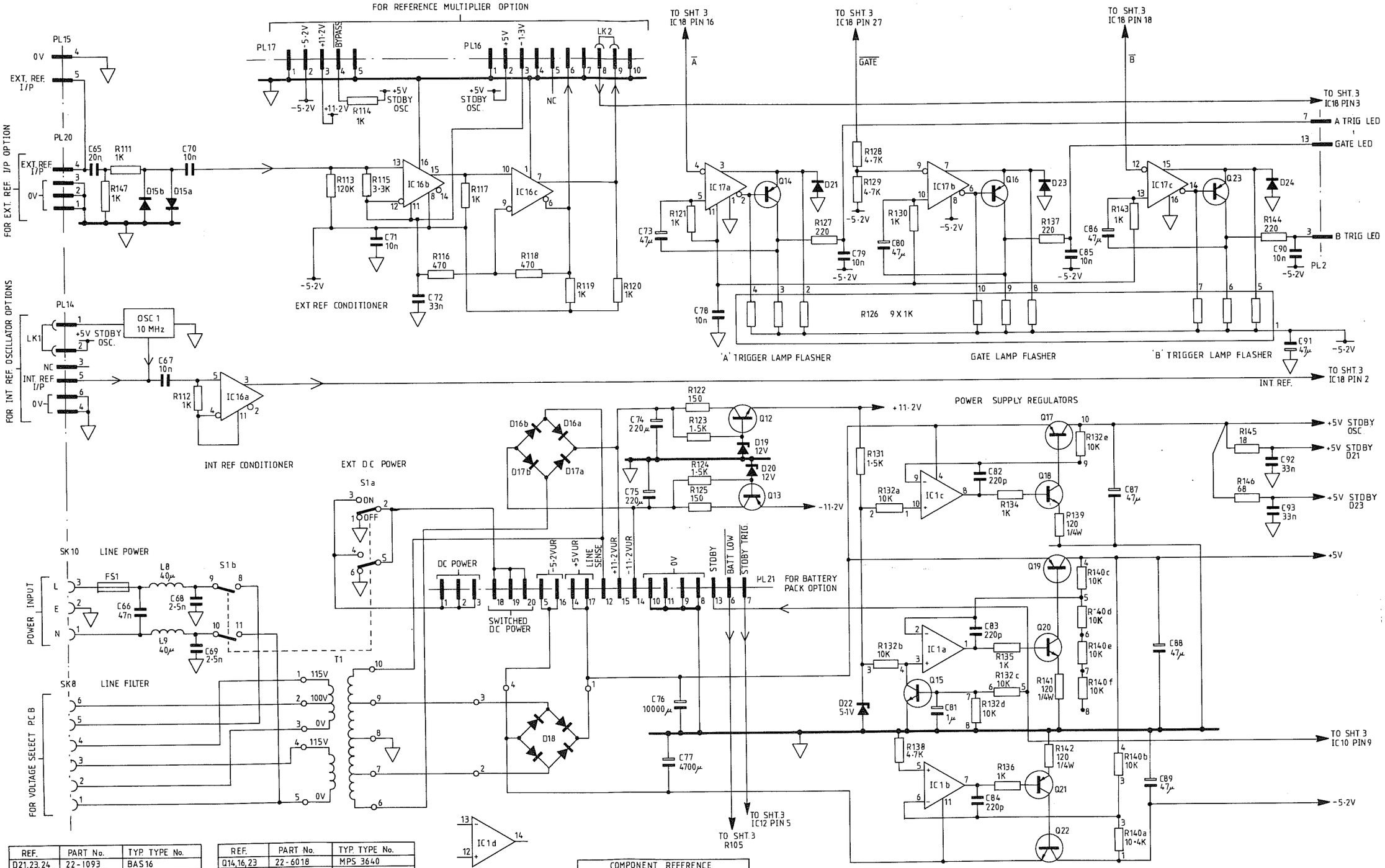
Motherboard Assembly 19-3004:
Circuit Diagram Fig. 6



REF.	PART No.	TYP. TYPE No.
D21,23,24	22-1093	BAS16
D15,16,17	22-1096	BAV99
D18	22-1662	VH248
D22	22-1857	BZX79B5V1
D19,20	22-1892	BZX84C12V
IC1	22-4262	MC3403
IC16,17	22-4528	10116

REF.	PART No.	TYP. TYPE No.
Q14,16,23	22-6018	MPS 3640
Q22	22-6152	BDT91
Q17,19	22-6153	BDT92
Q12,15,18,20	22-6197	SO3904
Q13,21	22-6199	SO3906

COMPONENT REFERENCE	
R111-132,134-147	PL2,14-17,20,21
C65-93	SK8,10
D15-24	S1
Q12-23	T1
L8,9	OSC1
IC 1,16,17	LK1,2 FS1

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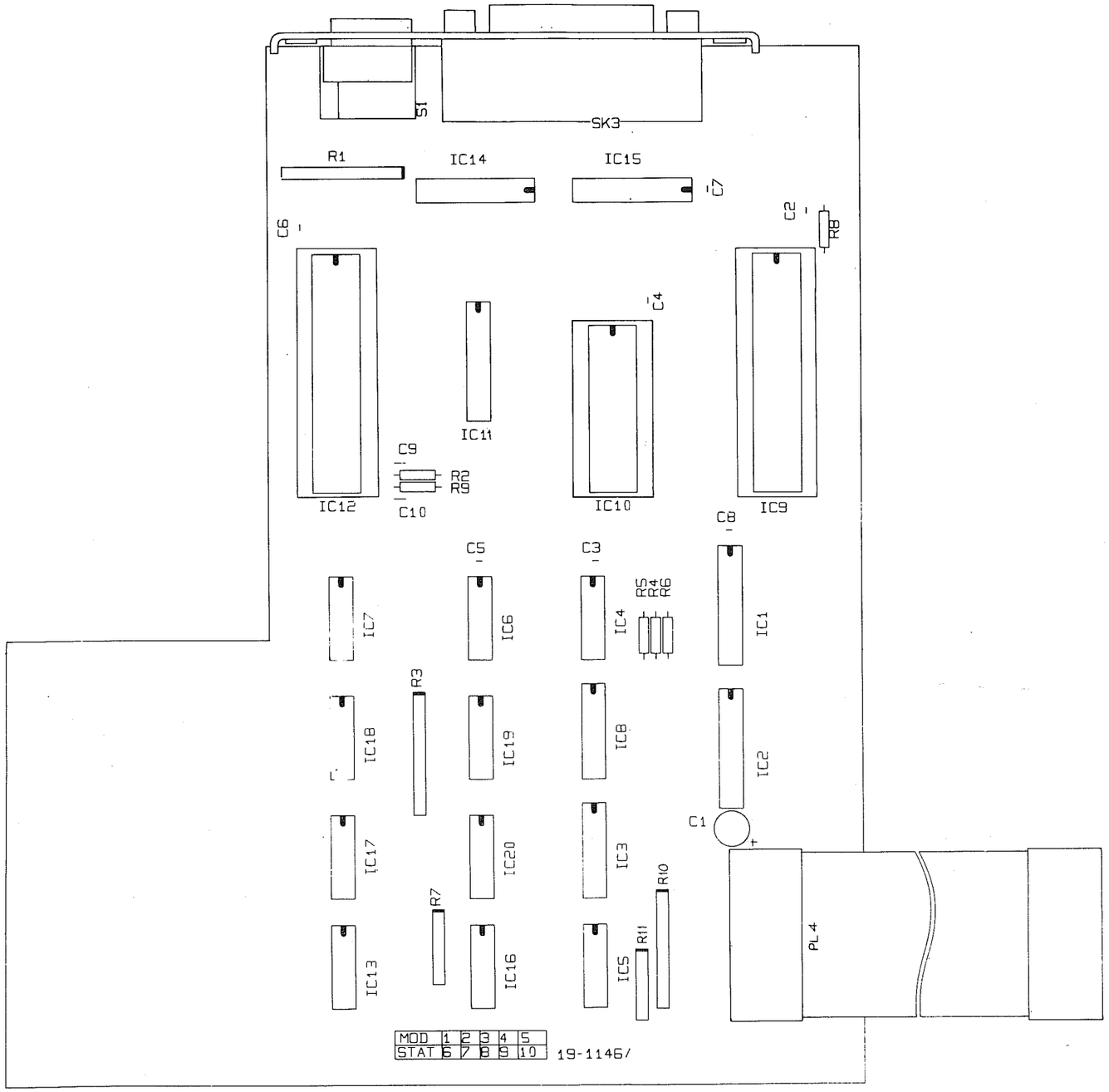
Motherboard Assembly 19-3004:
Circuit Diagram

Fig.7



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GPIB Assembly 19-1146 :
Component Layout Fig. 8

PL4 1
PL4 2
PL4 3
PL4 4
+5V
C1 47µ
PL4 25
PL4 26
PL4 27
0V
RESET GPIB
PL4 28
5MHZ CLOCK
PL4 24
GATE
PL4 21
GPIB OPT
PL4 15
B0
B1
B2
B3
B4
B5
B6
B7
PL4 23
PL4 10
PL4 12
PL4 14
PL4 13
PL4 11
PL4 9
PL4 8
A0
A1
A2
PL4 7
PL4 6
PL4 5
GPIB SEL
PL4 16
GPIB DATA IRQ
PL4 22
R1 3.3k
R3 3.3k
R7 3.3k
R10 100k
R11 100k
R1-B 3.3k
C8 100n
C2 100n
R8 18
C4 100n
C3 100n
C5 100n
IC1
IC2
IC3
IC4-D
IC5-A
IC5-B
IC5-C
IC5-D
IC6-A
IC6-B
IC6-C
IC6-D
IC7-A
IC7-B
IC7-C
IC7-D
IC8
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC16-A
IC16-B
IC17-A
IC17-B
IC18-A
IC18-B
IC19-B
IC19-C
IC19-D
IC20-A
IC20-B
IC20-C
IC20-D
S1
R2 56
R9 56
C9 10n
C10 10n
C6 100n
C7 100n
R3 3.3k
SK3 12
SK3 18
SK3 19
SK3 20
SK3 21
SK3 22
SK3 23
SK3 24
SK3 7 NRFD
SK3 11 ATN
SK3 6 DAV
SK3 10 SRQ
SK3 8 NDAC
SK3 17 REN
SK3 5 EOI
SK3 9 IFC
SK3 1 DIO1
SK3 2 DIO2
SK3 3 DIO3
SK3 4 DIO4
SK3 13 DIO5
SK3 14 DIO6
SK3 15 DIO7
SK3 16 DIO8
PL4 18 GPIB IRQ
PL4 20 R LED
PL4 17 A LED
PL4 19 S LED
R6 330
R4 330
R5 330

NOTE: SIGNALS ON SK3 ARE NEGATIVE LOGIC

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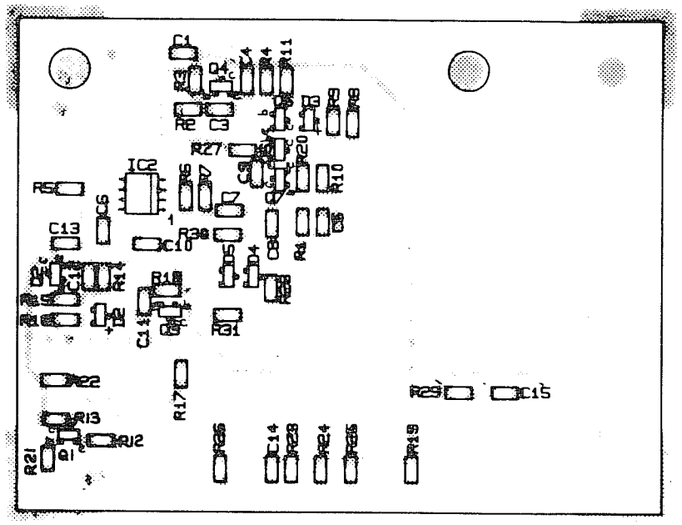
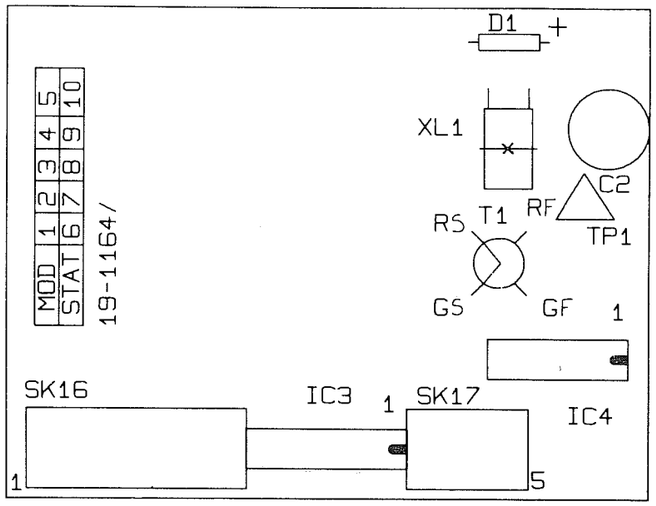
GPIB Assembly 19-1146:
Circuit Diagram Fig. 9

TRACKSIDE VIEW



COMPONENT SIDE VIEW



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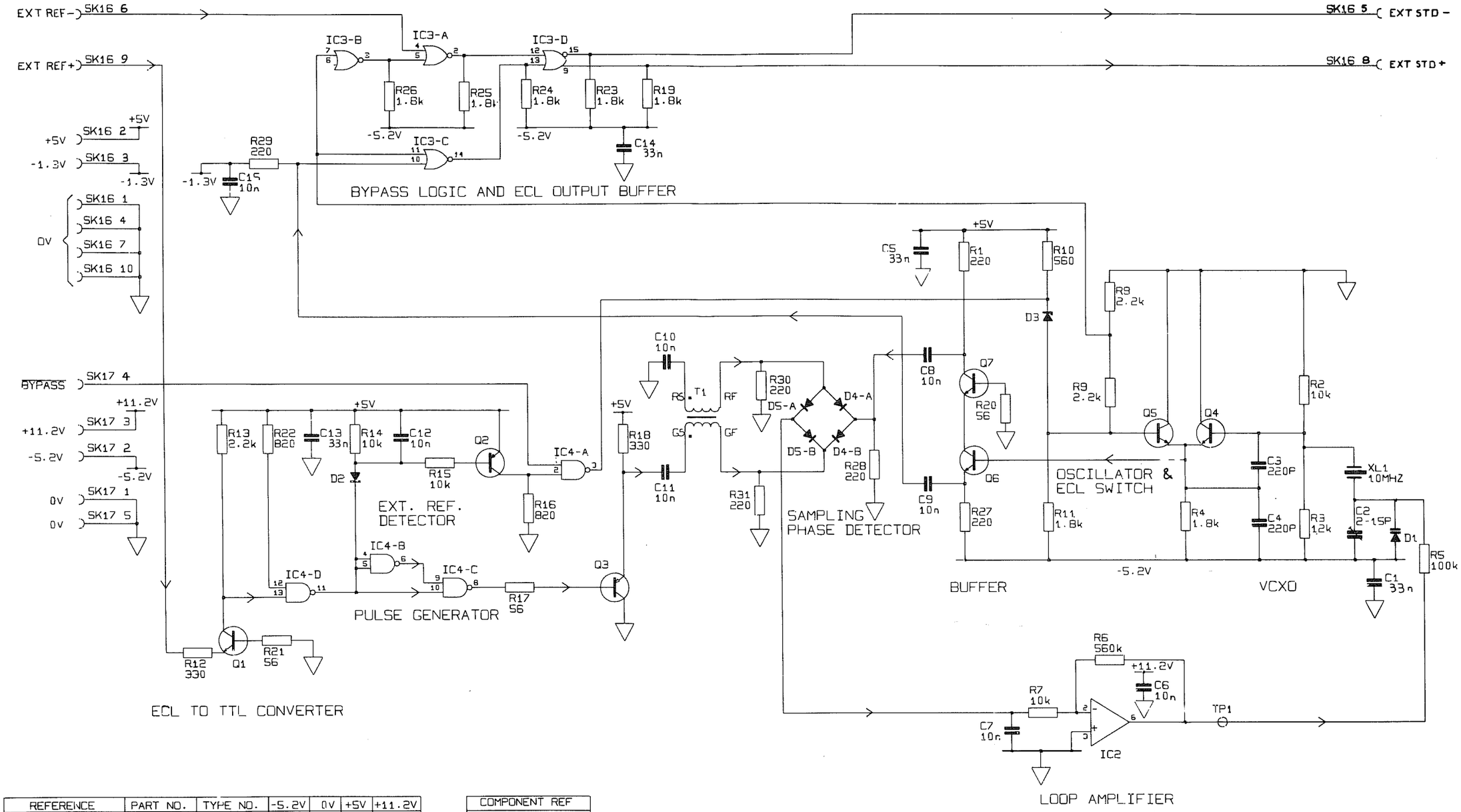
Reference Frequency Multiplier
19-1164 : Component Layout Fig. 10



REFERENCE	PART NO.	TYPE NO.	-5.2V	0V	+5V	+11.2V
D2	22-1093	BAS16				
D4,5	22-1096	BAV99				
D1	22-1097	MV1640				
D3	22-1882	BZX84C4V7				
IC2	22-4292	FFC2741UC	4			7
IC3	22-4514	MC10102	8	1,16		
IC4	22-4582	74LS132		7	14	
Q1, 4-7	22-6197	FMMT3904				
Q2, 3	22-6199	FMMT3906				

COMPONENT REF
R1-31
C1-15
D1-5
IC2-4
Q1-7
T1
XL1
SK16,17

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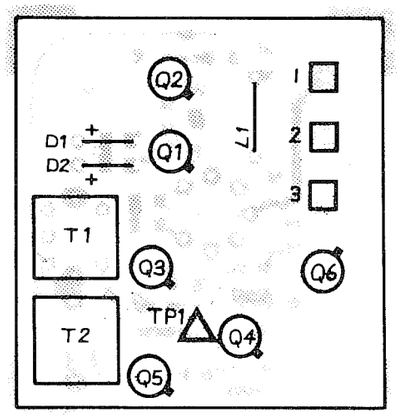
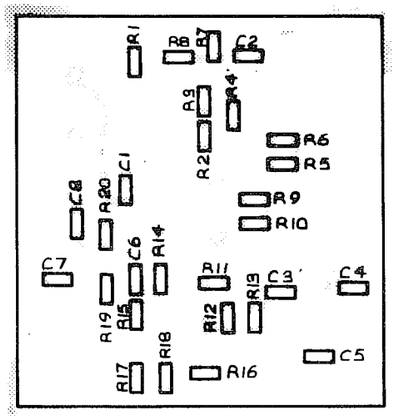
Reference Frequency Multiplier
19-1164 : Circuit Diagram **Fig.11**



VIEWED FROM COMPONENT SIDE



VIEWED FROM TRACK SIDE

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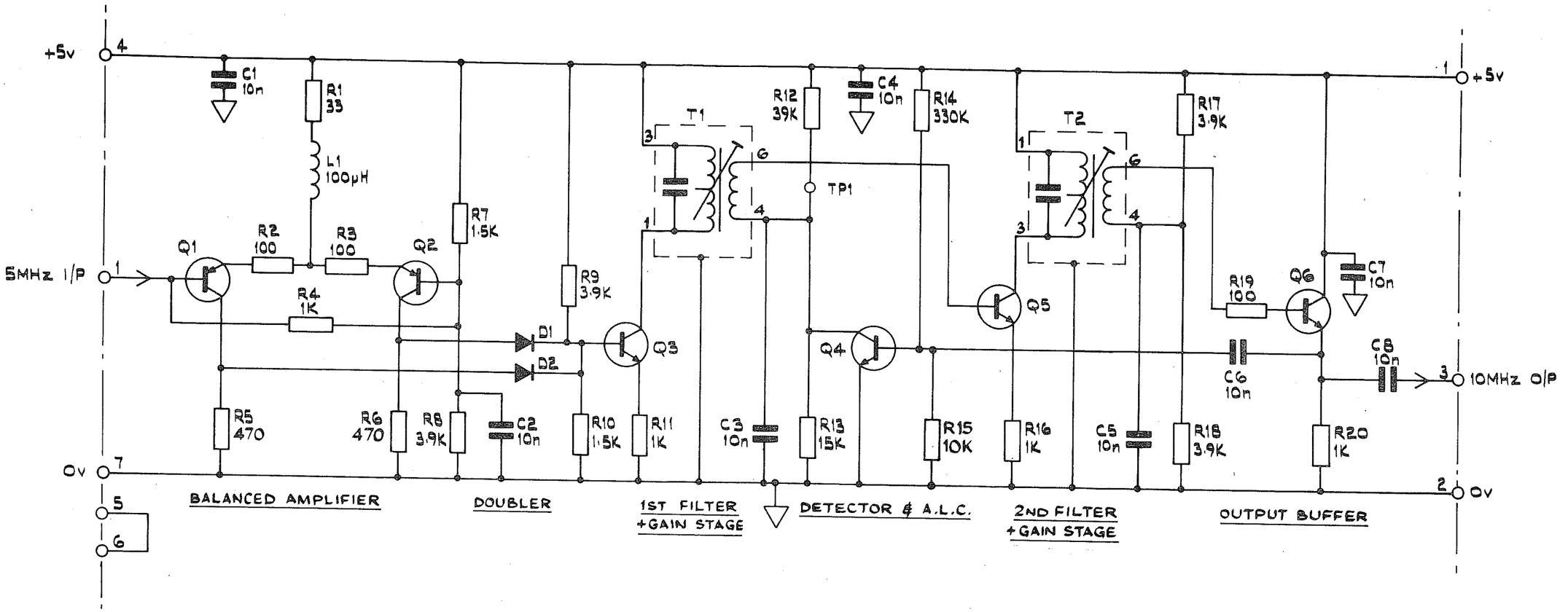
Reference Doubler 19-1238 :
Component Layout Fig. 12



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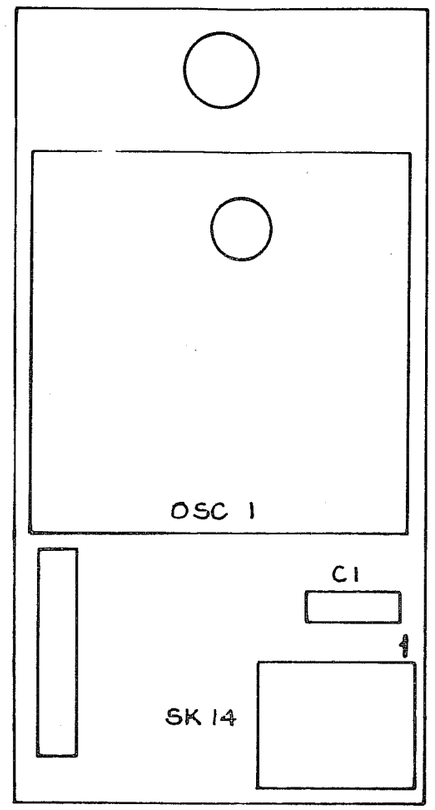
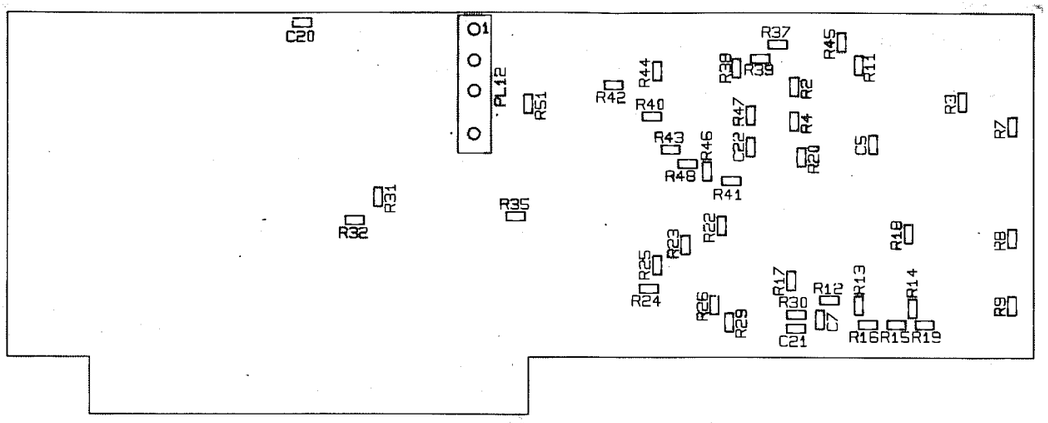
Reference Doubler 19-1238:
Circuit Diagram

Fig. 13

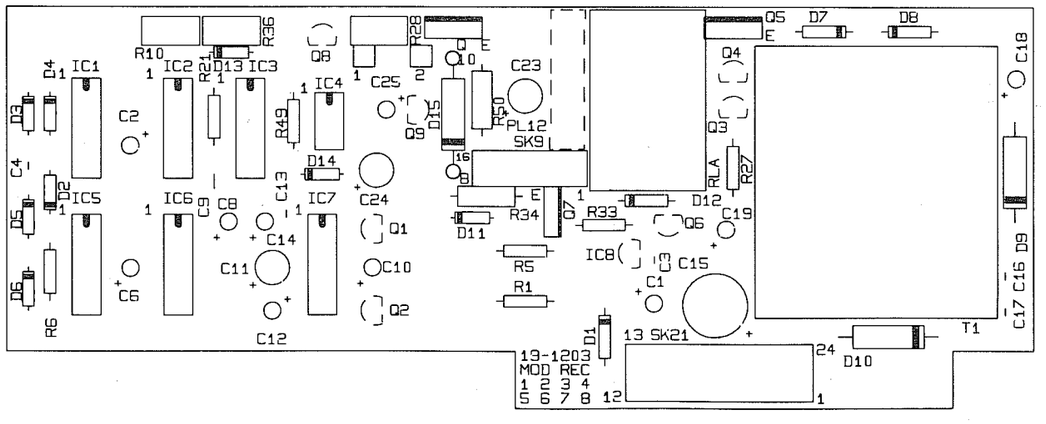


Oscillator Assembly 19-1208:
Component Layout Fig. 14

TRACKSIDE VIEW



COMPSIDE VIEW



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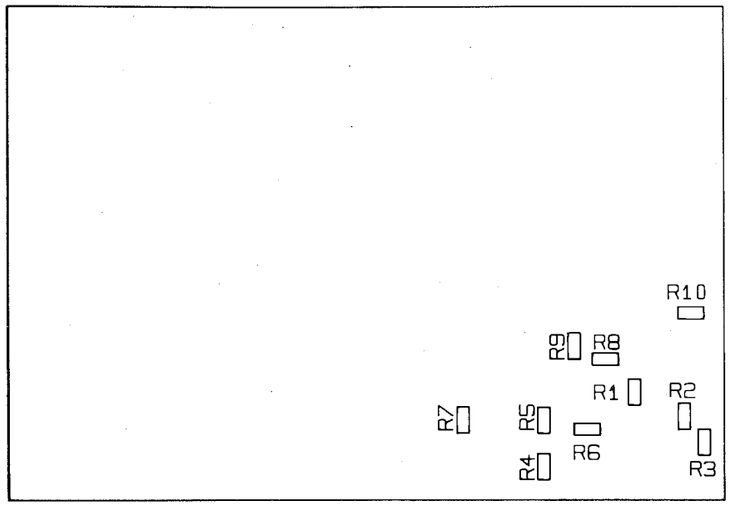
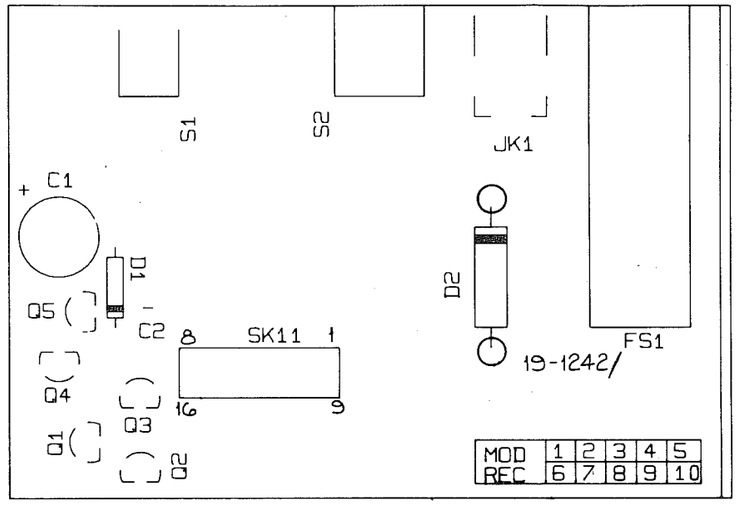
Battery Board Assembly:
Component Layout Fig.15

TRACKSIDE VIEW



COMPONENT SIDE VIEW



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Switchboard Assembly 19-1242:
Component Layout Fig.16

19-1203
BATTERY BD. ASSY

SWITCHED D.C. POWER

SK21 21 22 23 KEY 24

SK21 8 STBY TRIG

SK21 7 BATT LOW

MANAGEMENT CIRCUITS

POWER-DOWN LATCH
PART 19-1242 SWITCH BD. ASSY

CONVERTER

CHARGER

PART 19-1242
SWITCH BD. ASSY

11-1723

MOUNTED ON 11-1722

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19-1203		
REFERENCE	PART No	TYP TYPE No
D2-6,14	22-1029	1N4149
D1,12	22-1602	1N4002
D11	22-1625	BZX79B3V9
D13	22-1856	BZX79B5V6
D9,10	22-2008	MBR340P
D7,8	22-2009	BYV95A
D15	22-2010	1N5404
IC8	22-4247	78L05
IC6	22-4249	LM339N
IC7	22-4291	LAS6320P
IC4	22-4295	CA358E
IC2	22-4729	4030
IC3,5	22-4738	4001
IC1	22-4770	4072
Q1,3,6,8,9	22-6007	2N3904
Q2,4	22-6008	2N3906
Q7	22-6139	MJE371
Q10	22-6153	BDT92
Q5	22-6206	BUZ21

COMP REF	19-1203
R1-51	PL12
C1-25	SK9,21
D1-15	T1
IC1-8	
Q1-10	
RLA	

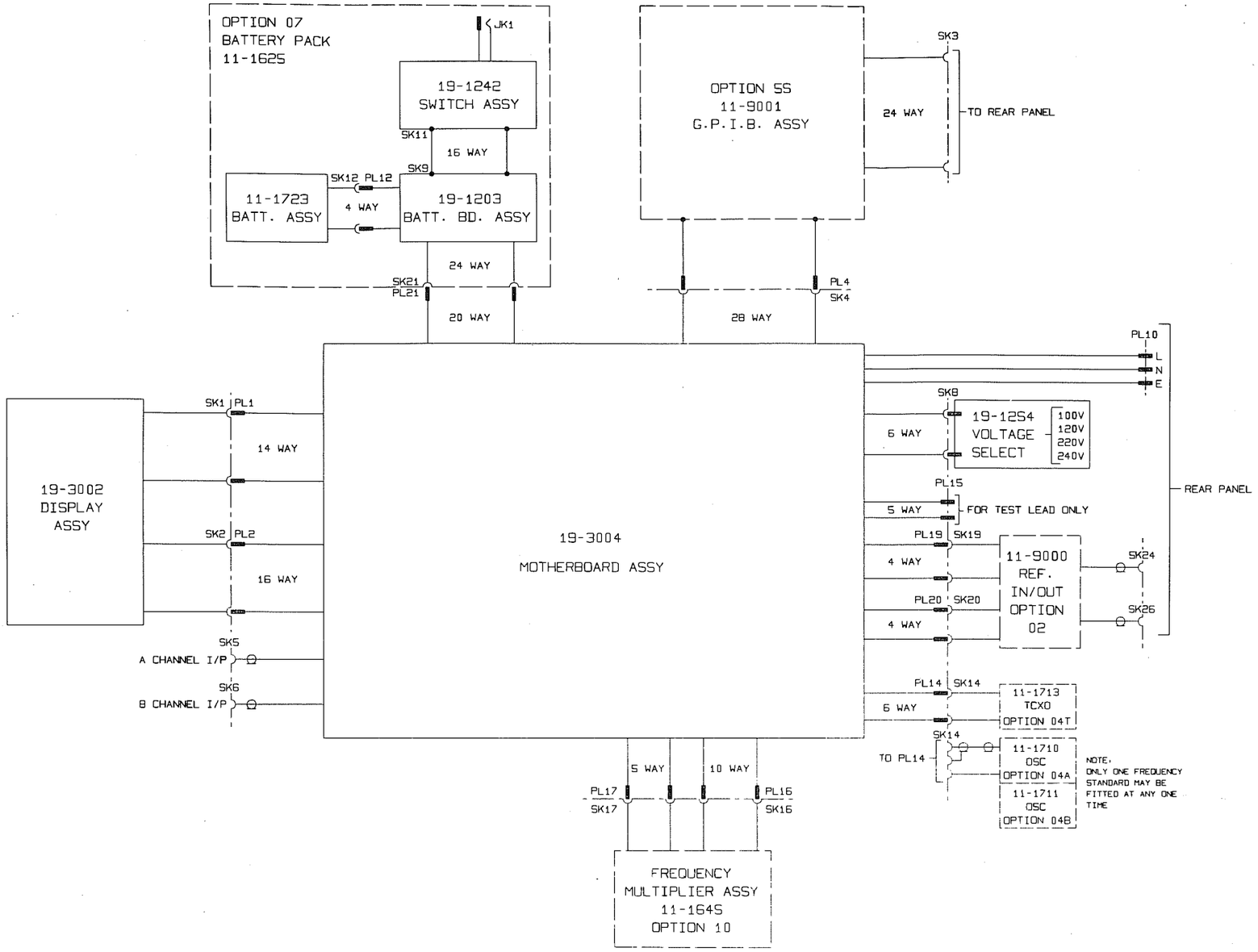
19-1242		
REFERENCE	PART No	TYP TYPE No
D1	22-1602	1N4002
D2	22-2008	MBR340P
Q1	22-6007	2N3904
Q2-5	22-6008	2N3906

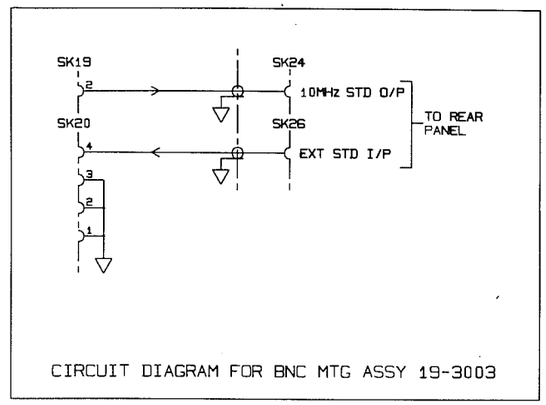
COMP REF	19-1242
R1-10	JK1
C1,2	S1
D1,2	S2
Q1-5	SK11
FS1	

COMP REF	11-1723
B1,2	
FS2,3	

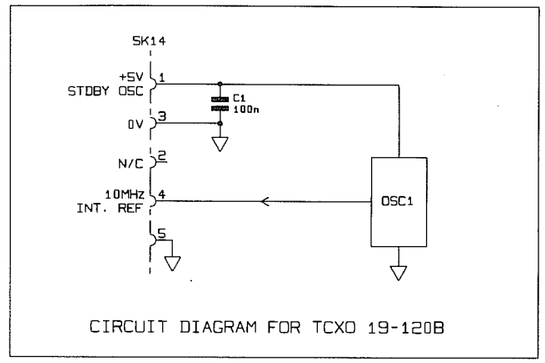
COMP REF	11-1625
R1	

Battery Pack Assembly 11-1625 :
Circuit Diagram Fig. 17





CIRCUIT DIAGRAM FOR BNC MTG ASSY 19-3003



CIRCUIT DIAGRAM FOR TCXO 19-1208

14 WAY	PL1	SK1
	PIN	PIN
STANDBY SWITCH	14	14
KEYBOARD EXTEND		13
PB4	2	2
PB5	6	6
PB6	7	7
PB7	5	5
R LED	12	12
A LED	1	1
S LED	11	11
STANDBY LED	8	8
DISPLAY STROBE	4	4
MODE 1	3	3

16 WAY	PL/SK2
	PIN
-5.2V	2
0V	10
+5V	12
KEYBOARD ENABLE	5
KEYBOARD DATA	4
KEYBOARD EXTEND	11
PB0	15
PB1	14
PB2	1
PB3	16
GATE LED	13
A TRIG LED	7
B TRIG LED	3
MODE 2	6
A TRIG LEVEL	8
B TRIG LEVEL	9

24 WAY	SK3
	PIN
0V	12.18.19.20 21.22.23.24
NRFD	7
ATN	11
DAV	6
SRQ	10
NDAC	8
REN	17
EOI	5
IFC	9
DIO1	1
DIO2	2
DIO3	3
DIO4	4
DIO5	13
DIO6	14
DIO7	15
DIO8	16

28 WAY	SK/PL4
	PIN
+5V	1.2.3.4
0V	25.26.27
RESET GPIB	28
SMHz CLOCK	24
GATE	21
GPIB OPT	15
B0	23
B1	10
B2	12
B3	14
B4	13
B5	11
B6	9
B7	8
A0	7
A1	6
A2	5
GPIB SEL	16
GPIB DATA IRQ	22
GPIB IRQ	18
R LED	20
A LED	17
S LED	19

16 WAY	SK9.11
	PIN
0V	4.5.6.12
NORM/BS	14
EXT/INT	13
POWER EXT/INT	1.2.3
BATTERY	9.10.11

4 WAY	PL/SK12
	PIN
BATTERY 1 0V	3
BATTERY 1 +6V	1
BATTERY 2 +6V	4
BATTERY 2 0V	2

6 WAY	PL14	SK14
	PIN	PIN
+5V PXO	1	
0V	4.6	3.5
10MHz INT REF	5	4
+5V STDBY OSC	2	1

5 WAY	PL15
	PIN
10MHz STD O/P	1
0V	3.4
EXT REF I/P	5

10 WAY	PL16	SK16
	PIN	PIN
+5V STDBY OSC	2	2
-1.3V	3	3
0V	1.4.7.10	1.4.7.10
EXT REF -	6	6
EXT REF +	9	9
EXT STD -		5
EXT STD +	8	8

5 WAY	PL/SK17
	PIN
+11.2V	3
-5.2V	2
0V	1.5
BYPASS	4

4 WAY	PL19	SK19
	PIN	PIN
10MHz STD O/P	1	2

4 WAY	PL/SK20
	PIN
0V	1.2.3
EXT REF I/P	4

PL21 - 20 WAY SK21 - 24 WAY	PL21	SK21
	PIN	PIN
D.C. POWER	1.2.3	1.2.3.4
SWITCHED D.C. POWER	18.19.20	21-24
-5V UR	5.16	6.19
+5V UR	4.17	5.20
LINE SENSE	12	15
+11.2V UR	15	18
-11.2V UR	14	17
0V	8.9.10.11	9-14
STDBY	13	16
BATT LOW	6	7
STDBY TRIG	7	8

RACAL
TH 9099

Interconnections Fig. 18