

MODEL 8160A

NBS FREQUENCY STANDARD RECEIVER

WARRANTY

Spectracom Corporation warrants to the original purchaser each new instrument to be free from defects in material and workmanship for a period of one year after shipment. Repair or replacement, at our option, will be made when our examination indicates that defects are due to workmanship or materials. Electron tubes, batteries, fuses, and lamps that have given normal service are excluded from warranty coverage. All warranty returns must first be authorized in writing by the factory.

This warranty does not apply to any of our products which have been repaired or altered by persons not authorized by Spectracom Corporation or not in accordance with instructions furnished by us. If the instrument is defective as a result of misuse, improper repair, or abnormal conditions or operations, or if any serial number or seal has been removed or altered, the warranty is void and repairs will be billed at cost.

This warranty is in lieu of all other obligations or liabilities expressed or implied and Spectracom Corporation neither assumes nor authorizes any person to assume for them, any other liability in connection with sales of its products.

REPAIR AND MAINTENANCE

Instruments should be returned only upon prior written authorization from Spectracom Corporation or its authorized sales and service representative. Warranty repair will be made upon written request. Please provide the following information in order to enable us to serve you efficiently:

1. Model Number and type
2. Serial Number
3. Description of trouble
4. Conditions and hours of use

Upon receipt of this information our service department will send you service data or shipping instructions. Transportation to the factory is to be prepaid by purchaser.

For assistance contact your nearest Spectracom representative.

CERTIFICATE OF TRACEABILITY

SPECTRACOM CORPORATION hereby certifies that its Model 8160A NBS Frequency Standard Receiver provides direct traceability to the National Bureau of Standards reference frequency as transmitted by station WWVB in Fort Collins, CO, with carrier frequency of 60 KHz.

Automatic verification is provided by the station-identifying phase shift of 45° that appears on the carrier signal at 10 minutes after each hour, returning to normal five minutes later. This phase shift appears in the readout as an offset of about 2.1 microseconds on the front panel meter and on a strip chart recorder trace.

When properly installed and maintained, the Model 8160A provides measurement accuracy and resolution as published in the equipment's instruction manual.

SPECTRACOM CORPORATION

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SECTION 1

INSTALLATION

1.1 Installation

1.2 Specifications

SECTION 1: INSTALLATION

1.0 INTRODUCTION

The SPECTRACOM Model 8160A NBS FREQUENCY STANDARD RECEIVER is a frequency calibration instrument that can be used to calibrate standard oscillators to an accuracy of 1×10^{-11} . The calibration is directly traceable to the National Bureau of Standards. The SPECTRACOM MODEL 8206 ferrite loop antenna is used with the MODEL 8160A.

The MODEL 8160A receives the 60 KHz signal transmitted by the National Bureau of Standards in Fort Collins, Colorado. Phase locked signals of 0.1, 1.0, 5.0, or 10.0 MHz are switch-selectable at the NBS OUTPUT connector.

The internal phase comparator compares the phase of the LOCAL INPUT signal with the received signal. The comparator operating frequency is switch selectable to one of the four standard frequencies of 0.1, 1.0, 5.0, or 10.0 MHz. The front panel meter displays the relative phase drift between the NBS signal and the LOCAL INPUT. The meter range is normally set to 50 microseconds full scale. A rear panel switch changes the scale to 10 microseconds full scale.

An auxillary output jack provides drive for a MODEL 8210 Strip Chart Recorder for long-term monitoring of oscillator performance.

Green and red LOCK/UNLOCK LEDs indicate signal reception and phase locking to the WWVB carrier.

1.1 INSTALLATION

1.1.1 Unpacking

In the event of damage to the shipping carton or if there is hidden damage to the equipment, but the carton is not damaged, be sure to contact the carrier immediately so their representative can witness the damage. If you fail to report shipping damage immediately you may forfeit any claim against the carrier. You should also notify SPECTRACOM CORPORATION of shipping damages so we can help you obtain a replacement or repair the equipment.

Be sure to remove all items of equipment and accessories from the shipping carton.

1.1.2 Reshipment

If it is necessary to return the unit to the factory, the original shipping carton should be used. If it is not available, a carton made of 250# test corrugated paper with at least two inches of polyethylene foam surrounding the unit must be used. The unit should be sealed in a plastic bag for moisture protection. Authorization for return must be obtained from SPECTRACOM.

1.1.3 Input Power

The equipment can be operated from either 115 or 230 VAC $\pm 10\%$, 50/60 HZ line power. The slide switch on the rear panel selects either of the two line voltages. BEFORE TURNING ON THE EQUIPMENT BE SURE THAT THIS SWITCH IS IN THE CORRECT POSITION. The unit is shipped in the 115 VAC position unless otherwise requested. If the line voltage switch is moved the fuse must be changed, 3/8 AMP for 230 VAC or 3/4 AMP for 115 VAC, as indicated on the rear panel.

1.1.4 Operating Environment

The equipment is designed for operation in a room temperature laboratory environment. Operation at temperatures exceeding 0 to +50°C may cause equipment malfunction or damage.

1.1.5 Bench Operation

The unit is equipped with feet and a tilt bar for use on a bench-top surface.

1.1.6 Antenna Installation/Location

The antenna should be mounted a minimum of 25 feet from the receiver to prevent regeneration, and at least 2 feet from any steel beams, roof decking or pipes that may cause detuning and signal loss. Noise sources such as large electric motors, power lines, oscilloscopes, TV sets, fluorescent or neon lights that blink, and any equipment containing a switching power supply may be a cause of interference. Large steel structures that are directly in line with the directional antenna will cause poor reception. DO NOT mount the antenna under a metal roof or inside a building with heavy steel structural supports that will shield the antenna from the signal.

The antenna should be mounted where it will not be disturbed, using the antenna mount MODEL 8211. The antenna should be positioned as shown in Figure 1-1, ANTENNA MOUNT MODEL 8211, and aimed using the map in Figure 1-2, GREAT CIRCLE MAP CENTERED ON FORT COLLINS, COLORADO, for maximum signal reception.

When the lead-in coaxial cable (RG-58/U is recommended) is connected from the BNC connector on the antenna to the BNC ANTENNA connector on the receiver the system is ready for use, if the antenna has been installed and aimed properly. The antenna has a built-in preamplifier inside the housing that receives its operating voltage through the center conductor of the coaxial cable, therefore the center conductor and the shield of the cable must be continuous from the antenna to the receiver. A short circuit in this line will not damage the equipment as the power supply is adequately protected.

The antenna may be located up to 1/2 mile from the receiver.

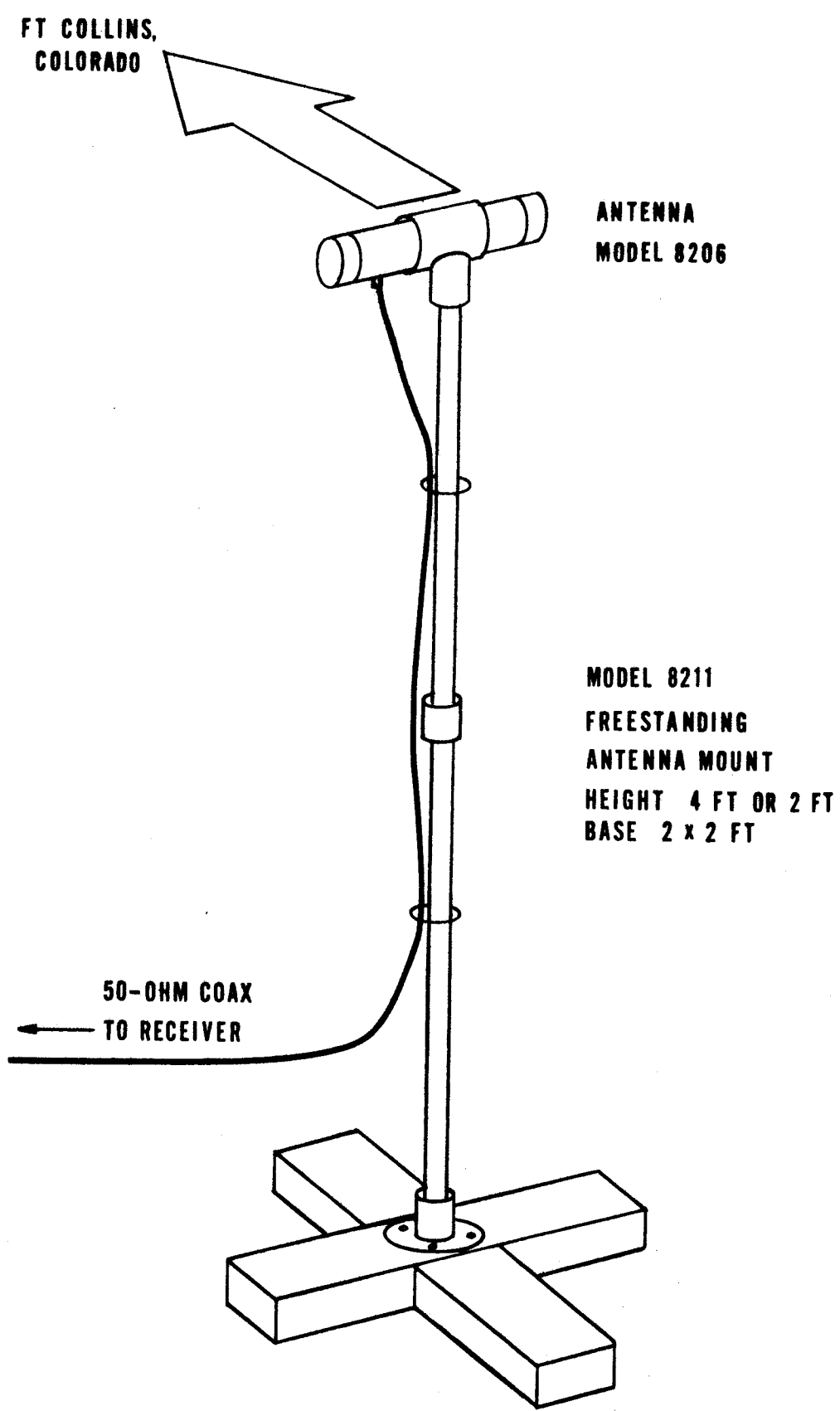
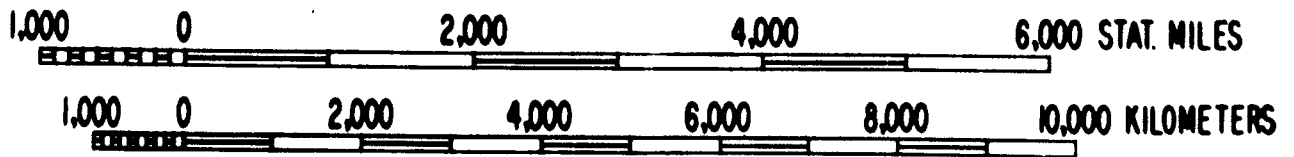
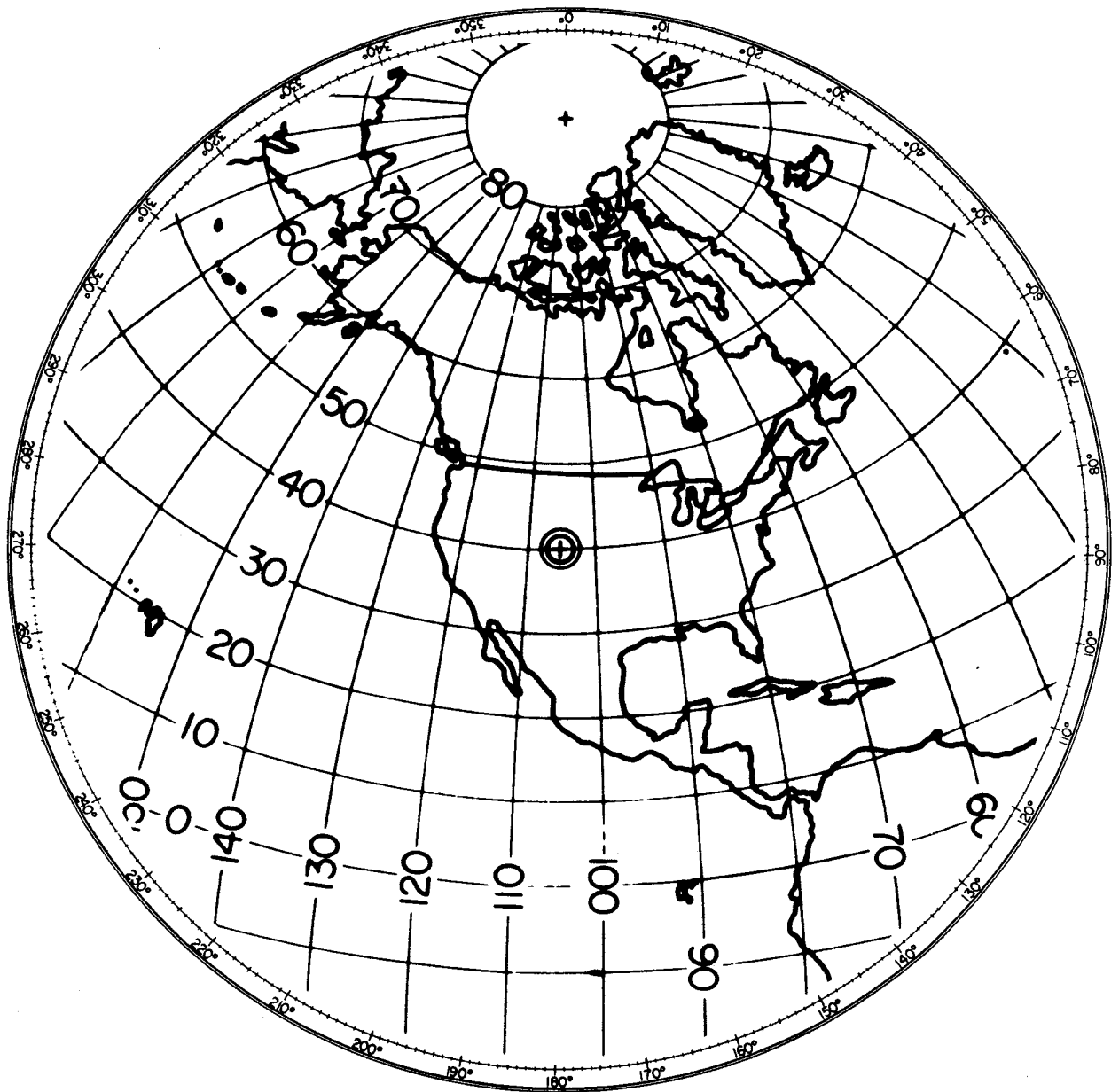


FIGURE 1-1 MODEL 8206 ANTENNA AND MODEL 8211 MOUNT



TO AIM ANTENNA AT FORT COLLINS, COLORADO, DETERMINE COMPASS HEADING FROM THIS MAP.

Draw a straight line from the receiver location through Fort Collins, Colo. at the center of the map. Continue until the line intersects the outer ring. The point at which the line intersects the outer ring indicates the compass heading for Fort Collins from your location.

FIGURE 1-2 GREAT CIRCLE MAP CENTERED ON FORT COLLINS

1.1.7 Signal Strength

The MODEL 8160A WWVB receiver can be used to measure relative field strength of the received 60-KHz signal. This signal strength measurement may be used to optimize reception when installing the receiver and aiming the antenna.

The MODEL 8160A receiver employs a synchronous AGC which responds to the 60 KHz WWVB signal and is not affected by noise. The AGC voltage level provides an excellent indication of signal strength.

To measure the AGC voltage, remove the cover of the unit and, using Figure 1-3, ASSEMBLY DRAWING-MAINFRAME, find test points TP3 and TP6 on the A2 Receiver Assembly. Place the negative lead of a high-impedance DC voltmeter at TP3 (ORANGE) and the positive lead at TP6 (BLUE).

In a field strength of 100 microvolts/meter, the AGC voltage will be about +2.0 VDC when the MODEL 8206 ANTENNA is properly orientated. The AGC voltage will be higher in stronger signal areas, rising to a limiting level of +3.0 VDC or more as front end input voltage exceeds 100 microvolts.

As the signal strength decreases to the receiver's phase lock threshold of 0.2 microvolts, the AGC voltage will decrease to +1.0 VDC. Below this level, the red UNLOCK indicator will come on. If the input signal is removed completely, the AGC voltage will decrease to a varying level near 0 volts. As the signal is reapplied and increased, the receiver will again lock at an AGC level of 1.0 VDC.

To use the AGC voltage to aid in antenna orientation, place the antenna so that the AGC voltage is maximized. The circuit that produces the AGC voltage has a very long time constant, so a pause of 30 to 60 seconds is necessary after each move of the antenna to allow the AGC to stabilize at a new level.

A few minutes of experimentation will produce a good antenna orientation.

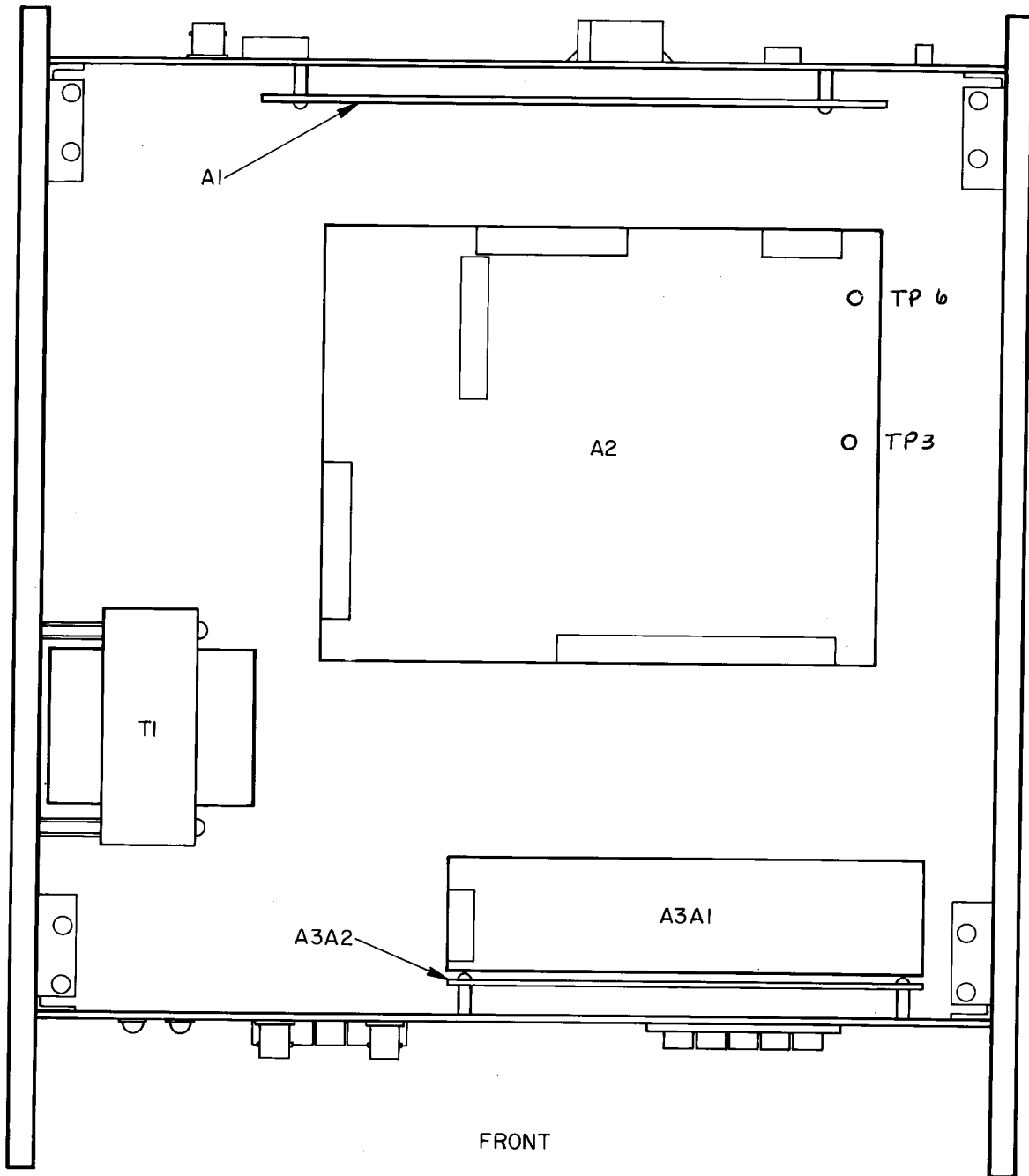


FIGURE 1-3 ASSEMBLY DRAWING - MAINFRAME

1.2 SPECIFICATIONS

RECEIVER/COMPARATOR SENSITIVITY

0.4 uV rms into 50 ohms. Minimum field strength at antenna, 30 uV per meter when used with Model 8206 Antenna.

PHASE LOCKED OUTPUT

0.1, 1.0, 5.0, or 10 MHz, front panel selectable, TTL compatible (fan out, 2 max.) 3.4V rectangular positive pulses into 93 ohms minimum resistive load. Phase locked to WWVB carrier.

LOCAL COMPARATOR INPUT

0.1, 1.0, 5.0, 10 MHz, front panel selectable, 100 mV rms minimum into 1000 ohms.

RECEIVED STANDARD FREQUENCY

60 KHz, NBS Station WWVB.

PHASE COMPARATOR

Front panel meter indicates phase changes of local input signal with respect to internal phase locked oscillator. Selectable scales of 50 usec and 10 usec relative time. Rear panel terminals provide drive to external strip chart recorder with 0-1 mA movement.

FREQUENCY ERROR COUNTER

Local input signal is counted using internal phase locked oscillator as the reference. Three digit display with overflow indication lamp and counter gate lamp. Push button for manual reset. Three gate times give resolution and error ranges as follows:

GATE TIME	RESOLUTION FOR 10.0 MHZ INPUT	DISPLAY RANGE
1.0 sec	1.0 Hz	1 KHz
10 sec	0.1 Hz	100 Hz
100 sec	0.01 Hz	10 Hz

PHASE LOCK INDICATION

Green front panel lamp indicates phase LOCK.

Red front panel lamp indicates phase UNLOCK due to insufficient signal strength or antenna disconnect.

MECHANICAL & INSTALLATION

SIZE 5.25H x 13.5D x 12.75W (inches) Height is 6 inches including feet. 133H x 343D x 324 (mm) Height is 152 mm including feet. Handles protrude 1.75 inches (45 mm) from front panel. Allow 2-3 inches cable clearance at rear.

WEIGHT 14 lbs.(6.35 Kg.) Shipping Wt. 18 lbs.(8.17 Kg.)

LINE POWER 115/230 VAC \pm 10%, 50/60 Hz, 40VA.

OPERATING TEMPERATURE 0 to 50° C.

MODEL 8206 LOOP ANTENNA

OPERATION

High gain directional ferrite loop in housing 14 1/2 L x 2 3/4 Dia.(inches), 368 L x 70 Dia.(mm). The built-in preamplifier receives DC power over the coaxial cable center conductor from the receiver. Equivalent electrical height 5.0 cm. May be located up to 1/2 mile from receiver.

INSTALLATION

1 Inch trade size female pipe thread at center of tubular housing for mounting. Input connector type BNC.

OPTIONS AND ACCESORIES

OPTION 01 Rack Mount Kit

OPTION 05 Time Code Output

Standard on all units S/N 0476 and above.

OPTION 14 60Hz Comparator

OPTION 15 Timing Pulse Output

OPTION 28 1KHz Output

MODEL 8171 SYNCHRONIZED CLOCK

Decodes the WWVB Time Signal

MODEL 8207 PREAMPLIFIER

Provides 40 dB gain in antenna feed line, making overall sensitivity 10 nanovolts, allows operation with signal strength as low as 0.6 uv per meter. Intended for use in areas where signal strength is below 30 uV/meter. Not usually necessary in the continental U.S. or Southern Canada.

MODEL 8211 ANTENNA MOUNT

for 8206, 4 ft. high.

MODEL 8210 STRIP CHART RECORDER

Operates on 60 Hz line power, 50 Hz unit available on special order.

SECTION 2

OPERATION

- 2.1 Initial Turn On
- 2.2 Frequency Calibration
- 2.3 Frequency Error Calculation
- 2.4 Strip Chart Recorder
- 2.5 Frequency Counter
- 2.6 NBS Output
- 2.7 Front Panel Functions
- 2.8 Rear Panel Functions

SECTION 2: OPERATION

2.1 INITIAL TURN ON

After the receiver and antenna have been installed plug the receiver into the power line, MAKING SURE THAT THE REAR PANEL SLIDE SWITCH, AND LINE FUSE ARE CORRECT. Turn on the POWER switch and note that the red UNLOCK light is on. Within one minute the green LOCK light will turn on. If the red UNLOCK light stays lit, indicating insufficient signal is being received, recheck the antenna installation as described in Section 1.

2.2 FREQUENCY CALIBRATION

Connect the local signal to be compared with the NBS signal to the LOCAL INPUT BNC connector. The frequency of the local signal must be the same as the frequency selected at the FREQUENCY-MHZ switches. Changes in the phase relationship between the local signal and the reference are indicated by meter movement. If the meter is stable there is zero drift in phase relationship, and the local signal is on frequency. If the meter moves slowly, it is measuring phase drift or slight frequency error. With the meter set to read 0-50 microseconds the local signal is divided to 20 KHz for phase comparison, and one complete deflection of the meter from end to end represents 50 microseconds (360° at 20 KHz). When using the 10-microsecond meter scale, the phase comparison is made at 100 KHz, causing the scale to represent only 10 microseconds (360° at 100 KHz) from end to end.

With the phase switch in the 10-microsecond position a 1.0-Hz frequency difference at 100 KHz is indicated by the meter moving steadily from one end of the scale to the other once each second. When the maximum deflection is reached the meter will return rapidly to the far end of the scale and begin to move across the scale again. If the local frequency is higher than the reference, the travel of the meter is from left to right, representing increasing phase lead. If the local signal frequency is low, the meter will move from right to left indicating increasing phase lag.

If the frequency error is too large for the meter to follow, attach an oscilloscope to the RECORDER OUTPUT jacks on the rear panel and monitor the phase detector sawtooth waveform output. Adjust the local oscillator until the sawtooth waveform has a period greater than one second. At this point, the front panel meter can be used.

Adjust the local frequency until the meter is not moving. The longer the phase drift is monitored, the greater the precision of the calibration. For longer observations, over periods of hours or days, a Model 8210 Strip Chart Recorder should be used.

To identify the WWVB signal NBS advances the carrier phase 45° at 10 minutes after every hour and returning to normal phase at 15 minutes after the hour. These phase changes cause the meter to deflect 2.1 microseconds for a 5-minute period every hour. To observe these

differences, connect a standard oscillator that is known to be on frequency and compare it against the received NBS signal. Observe the meter deflections at 10 and 15 minutes after the hour.

2.3 FREQUENCY ERROR CALCULATION

Frequency error is measured by the speed that the meter deflects in its slow travel across the scale, or by noting the slope of the recorder trace on the paper. Here is an example:

In a three hour period, the recorder trace moved (or the meter needle moved) from left to right a total distance of 160 microseconds. If the scale setting is 0-50 microseconds, the trace would move completely across the paper (or scale) slightly more than three times. The calculation is made by dividing the phase movement expressed in seconds by the time during which the the movement occurred, also expressed in seconds:

$$\frac{\text{Phase Movement (seconds)}}{\text{Time for Movement to Occur (seconds)}} = \frac{160 \times 10^{-6}}{3 \times 3600} = 1.48 \times 10^{-8}$$

In this example, the local frequency is 1.48 parts in 10^{-8} , or 148 parts per million high.

One part in 10^{11} , can be resolved in eight hours using the 10 microsecond scale if atmospheric noise conditions are favorable.

Figure 2-1 Error Calculation Chart can be used to find the frequency error as a function of time and phase change.

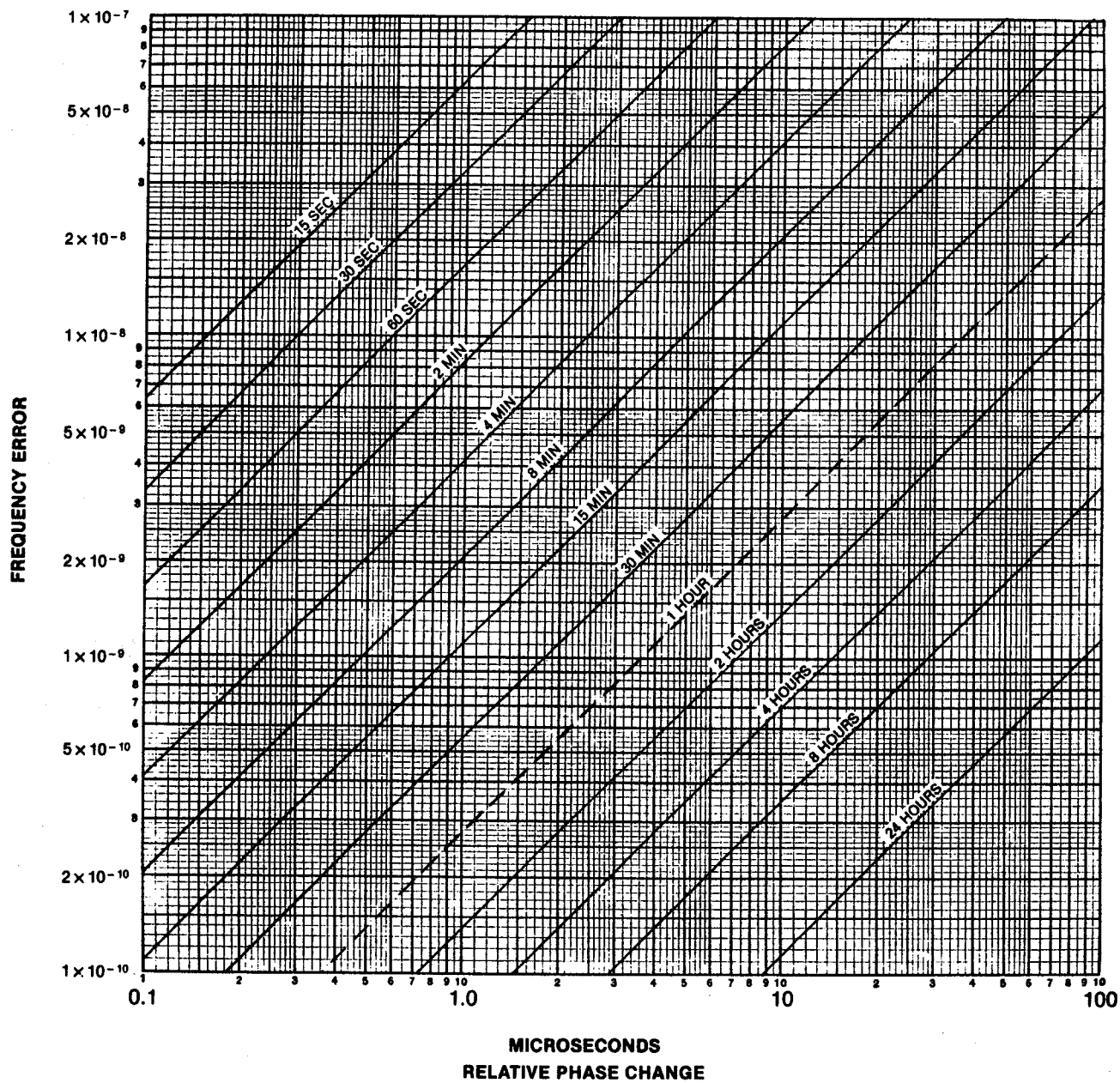


FIGURE 2-1 ERROR CALCULATION CHART

2.4 STRIP CHART RECORDER

Terminals are provided on the rear panel for driving a MODEL 8210 Chart Recorder. When connected, the recorder gives a long-term record of excursions of the phase meter. Samples of charts and descriptions are shown in Figures 2-2 TRACE 1 through Figure 2-8 TRACE 7.

If a chart recorder other than a MODEL 8210 is used it must have a 0-1 mA meter movement and a paper speed of 1.0 inch per hour. The positive recorder terminal is connected to the red terminal and negative to the black terminal on the rear panel of the 8160A.

Figure 2-2 TRACE 1 shows an oscillator that is drifting high. Note the trace slopes to the right.

Figure 2-3 TRACE 2 shows a downward drifting test oscillator.

Figure 2-4 TRACE 3 shows a typical 24 hour trace, diurnal shift, and some signal degradation during the night. Note the 2-microsecond phase shift that identifies the signal received from WWVB.

Figure 2-5 TRACE 4 shows overnight signal degeneration.

Figure 2-6 TRACE 5 is an example of a momentary unlock condition.

Figure 2-7 TRACE 6 is a trace made on a noisy day.

Figure 2-8 TRACE 7 was made on a day with frequent sun flares.

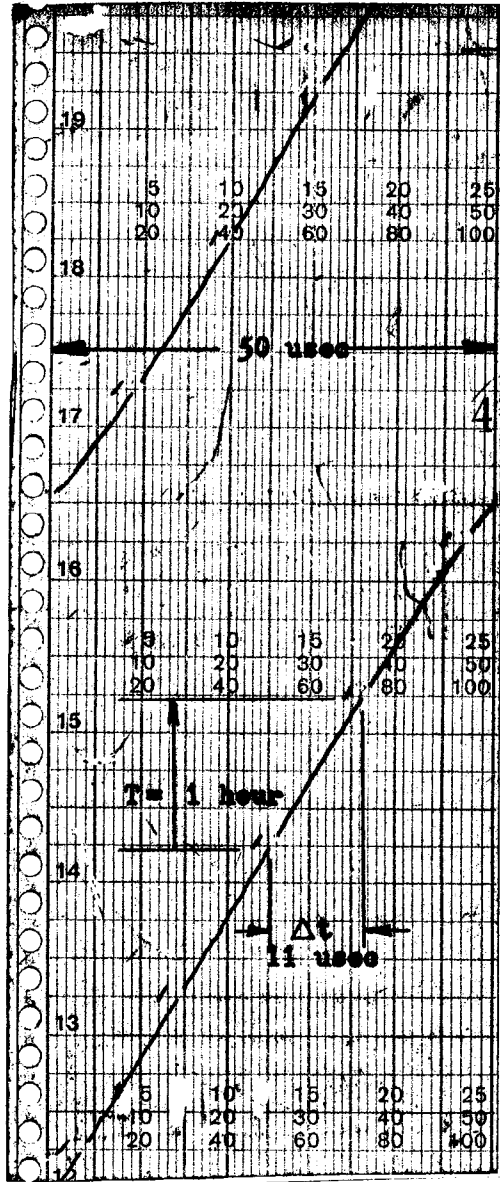


FIGURE 2-2 TRACE 1 shows that the oscillator error is positive (frequency is high) because the trace slopes to the right. A close approximation of drift can be made by noting the phase drift in microseconds that occur in one hour. Divide this by 3.6, yielding frequency error expressed as parts in 10^9 .

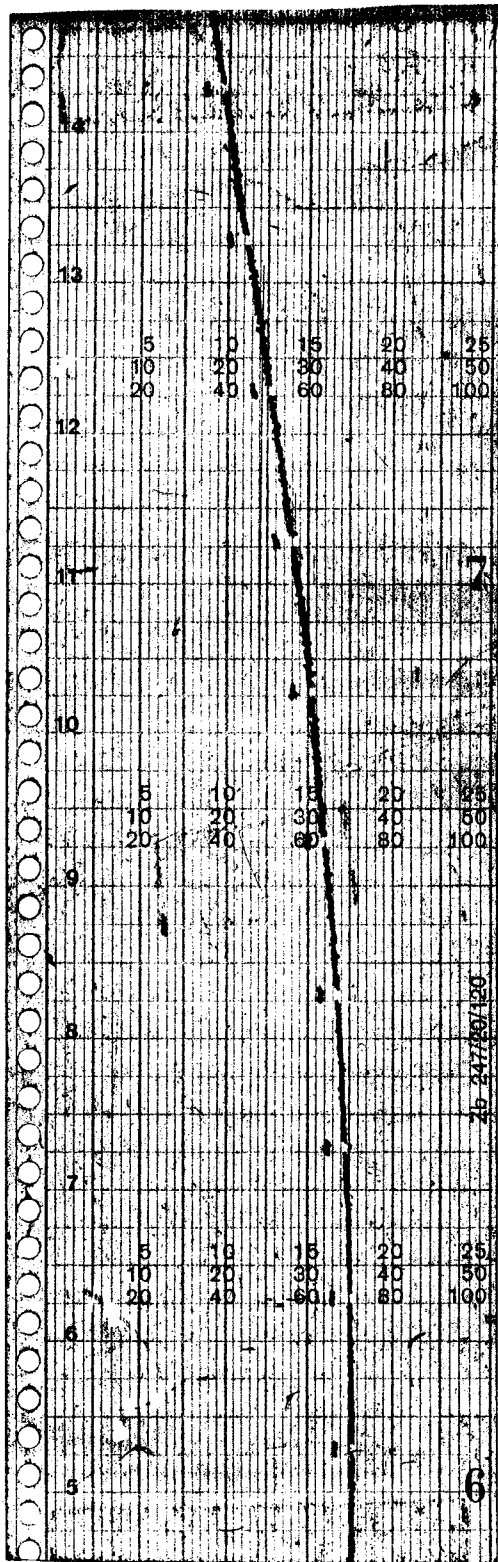


FIGURE 2-3 TRACE 2 The trace shows an oscillator which drifted low in frequency by almost 1×10^{-9} in a 9 hour period.

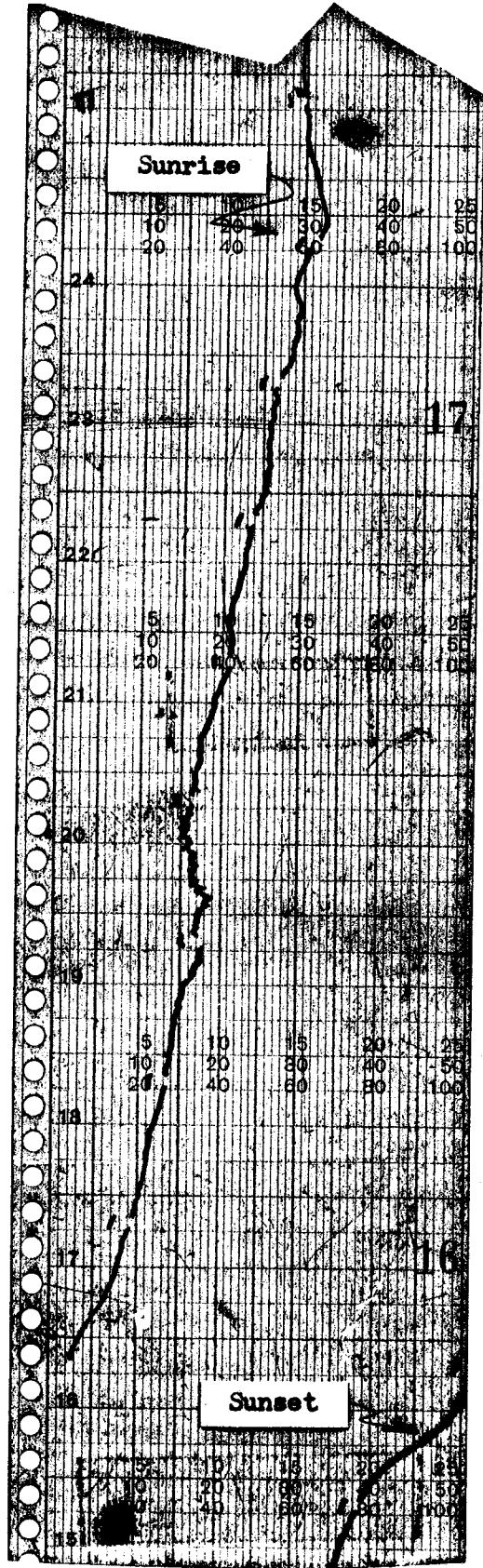


FIGURE 2-4 TRACE 3 The trace shows overnight signal degradation between sunset and sunrise. This effect will vary considerably with geographic location and with time of year, as well as with daily propagation variations.

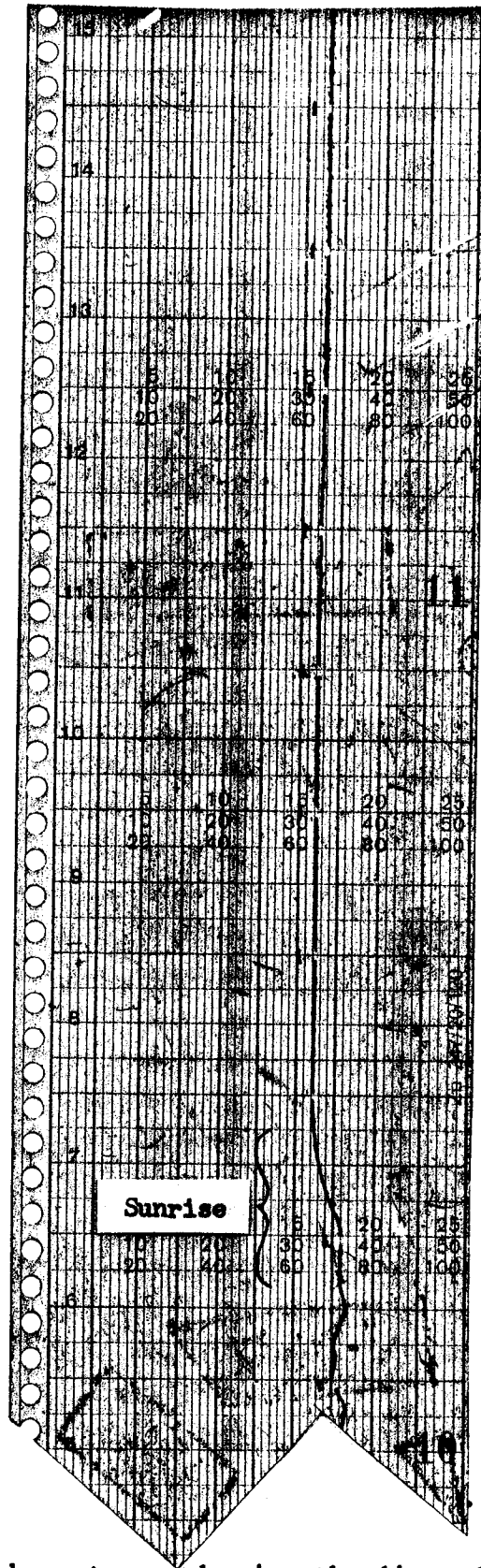
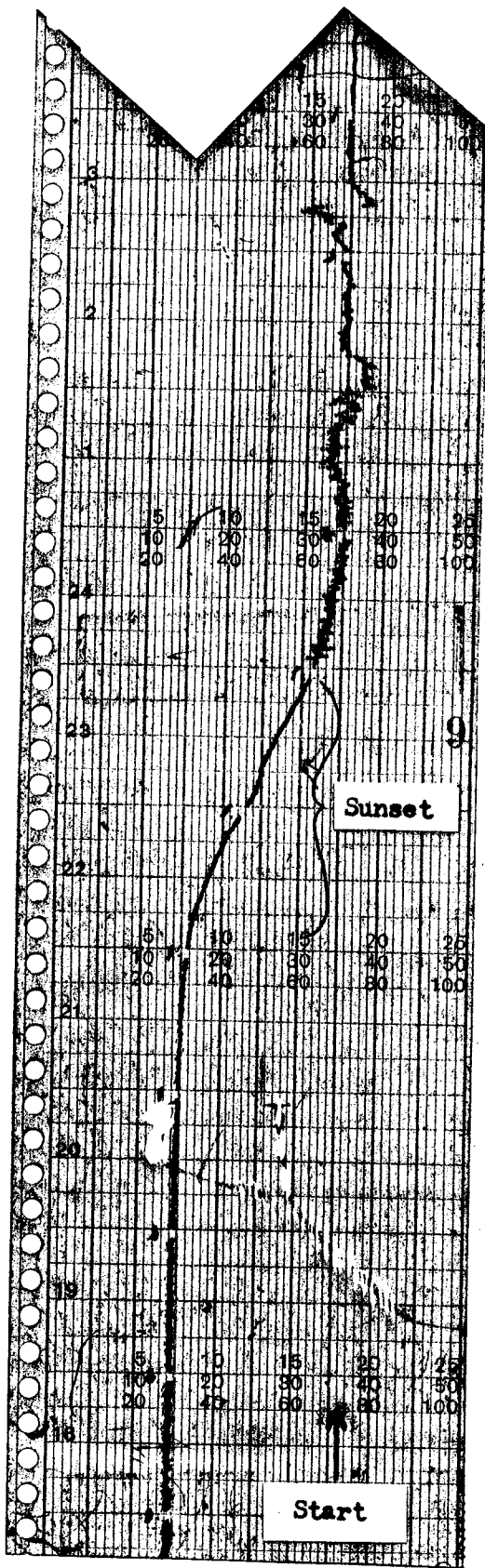


FIGURE 2-5 TRACE 4 is a typical 24-hour trace showing the diurnal shift and some signal degradation during the night. After sunrise the trace shows oscillator error to be only a few parts in 10^{-11} .

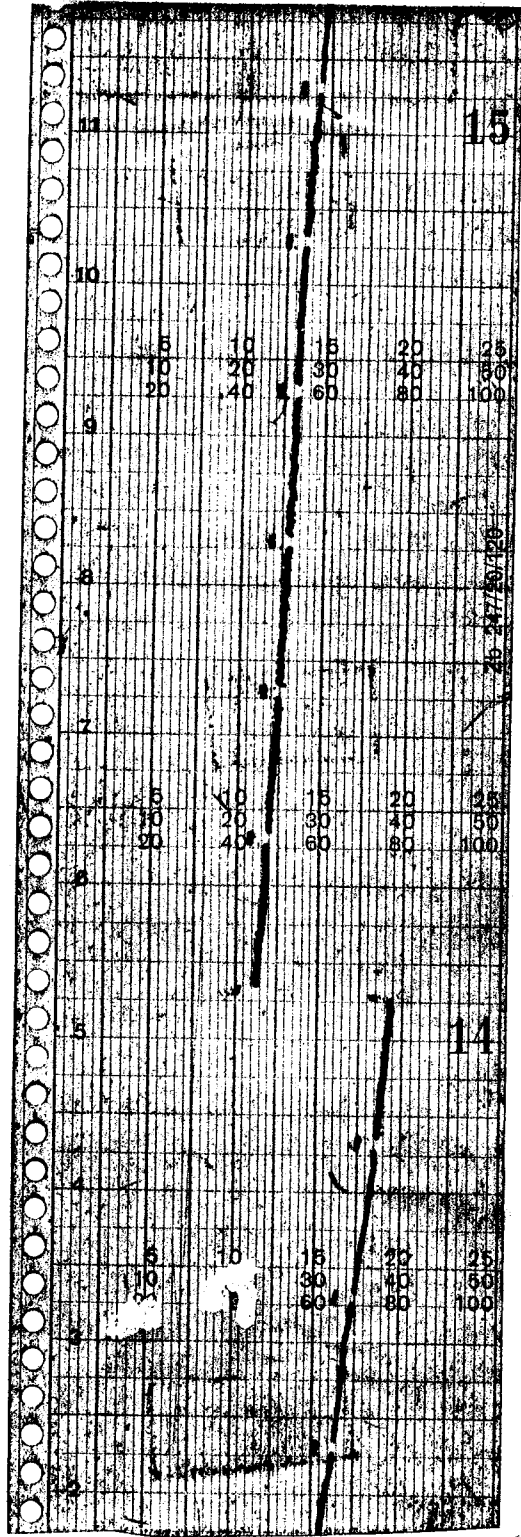


FIGURE 2-6 TRACE 5 The trace shows a momentary unlock condition due to noise bursts or signal fading. When receiver phase lock is re-established the trace starts at a new position on the scale.

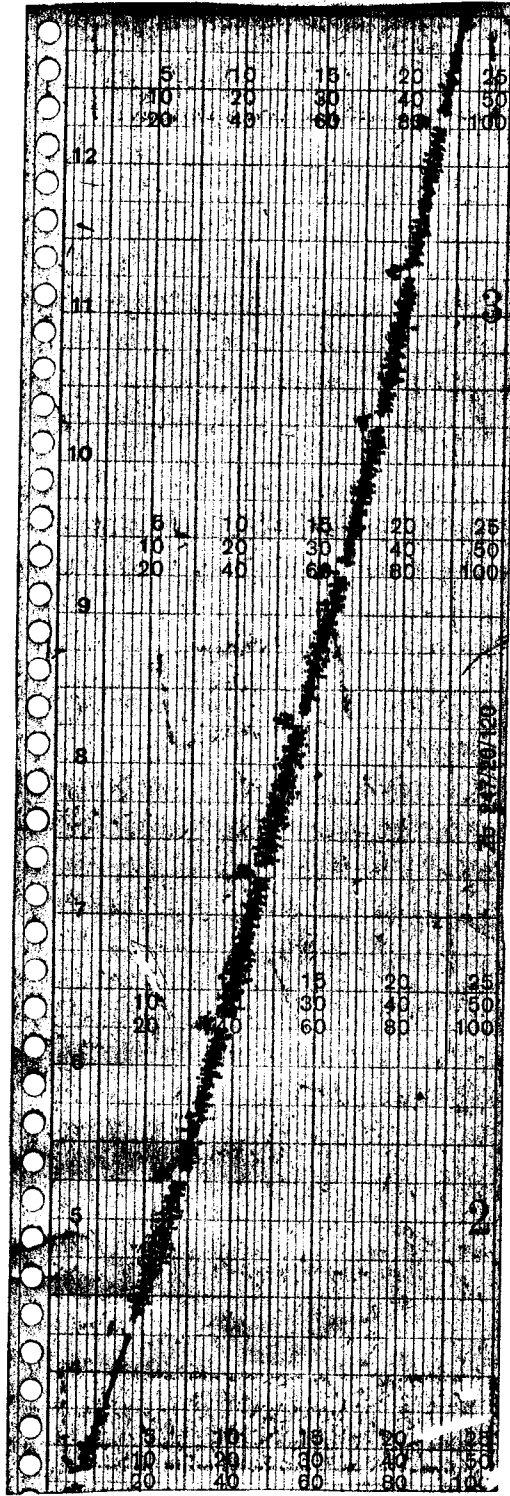


FIGURE 2-7 TRACE 6 The trace was made on a very noisy day, causing a trace width of about four microseconds. This problem is encountered less frequently with improved antenna placement.

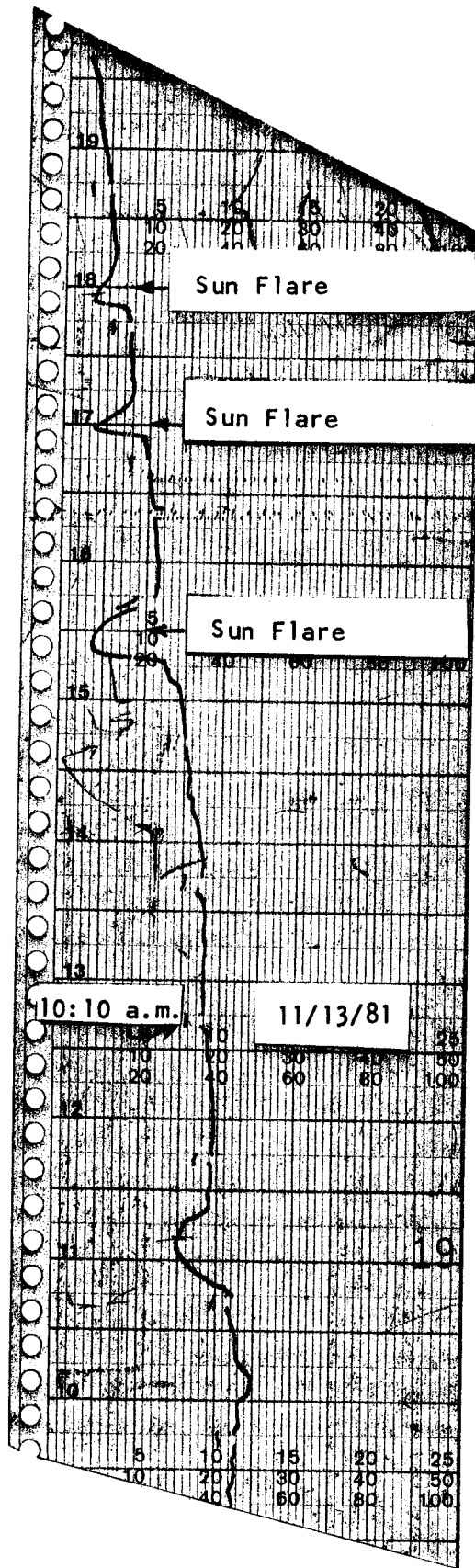


FIGURE 2-8 TRACE 7 was made on a day with frequent sun flares.

2.5 FREQUENCY COUNTER

Apply power to the counter by depressing the OFF/ON button under the display. The counter counts the local signal input frequency using the NBS signal as the time base for gating. The local input should be within 1 KHz of the frequency selected at the front panel because only the last three digits are displayed and larger errors will give misleading or ambiguous readings.

Depress the 1.0 second gate button, and observe the frequency readout. A reading 5 Hz high will display 005, a reading 5 Hz low will display 995, because only the last three digits of the frequency are displayed. If the error is low and more precision is required, depress the 10 second gate button and take another reading. The display shows the last two digits before the decimal, and one after, indicating a resolution of 00.1 Hz. The 100 second gate indicates a 0.01 Hz resolution, but the error must be less than 10 Hz for a valid reading.

When using longer gate periods, the RESET button may be used to start another gate period. The gate duty cycle is 4 to 1 (open to close), with the GATE indicator lit when the gate is open and the unit is counting. The OVERFLOW indicator is a reminder that only the last three digits of the frequency are displayed.

2.6 NBS OUTPUT

The frequency of the output signal is selected by depressing one of the FREQUENCY-MHZ switches located below the signal connectors on the front panel. The output signal obtained when a frequency is selected is phase locked to the WWVB 60 KHz carrier. This standard output frequency can be used for checking the accuracy of frequency counters. Note that some noise will be present in the form of pulse jitter due to atmospheric noise at the receiver antenna. The counting error caused by this noise is usually not more than a few parts in 10^8 in a one second averaging period. Longer averaging periods will decrease the effect of the jitter. The long-term accuracy of this signal is as good as that of the WWVB carrier signal that it is phase locked to.

The length of coaxial cable that is used to feed the signal to the load is critical because the output is a TTL square wave. 93-ohm terminated cable should be used for long runs where waveform must be preserved.

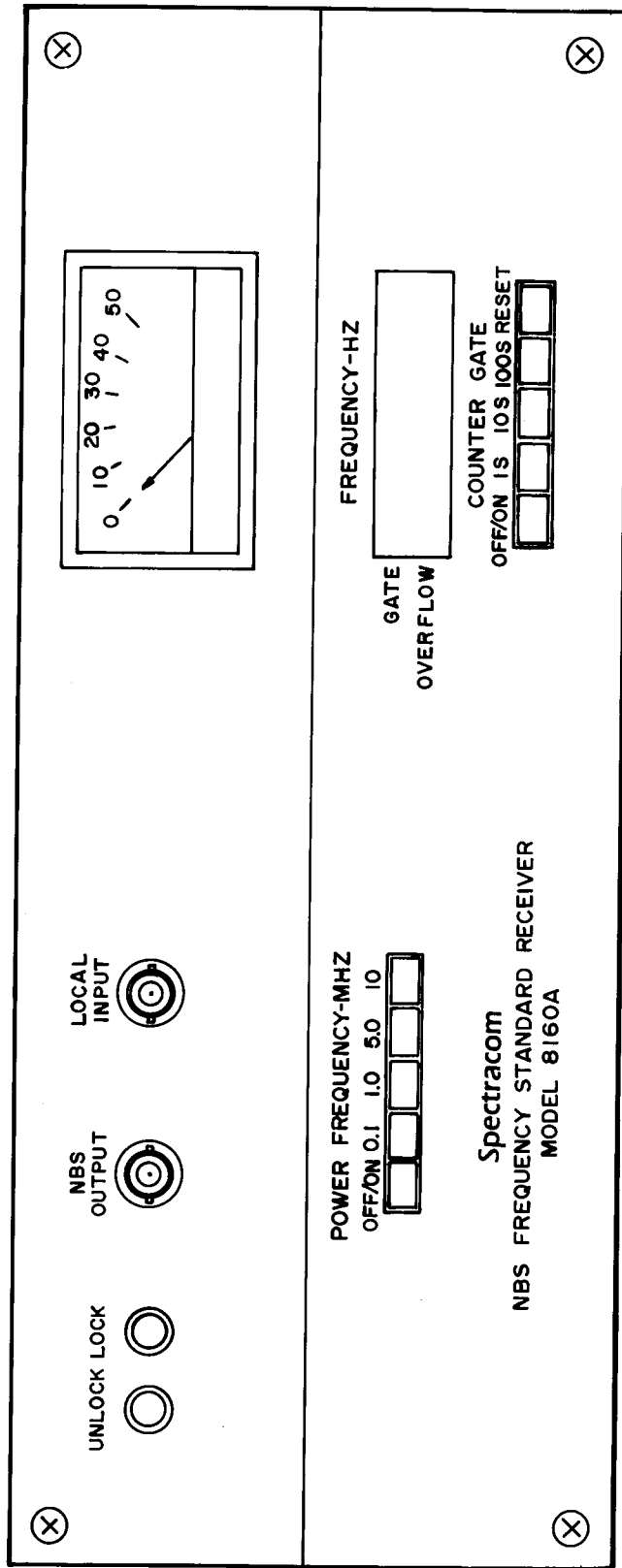


FIGURE 2-9 MODEL 8160A FRONT PANEL

2.7 FRONT PANEL FUNCTIONS

Use Figure 2-9, 8160A FRONT PANEL, to locate the following.

POWER Switch Depressing the POWER switch turns the unit on.

FREQUENCY-MHZ SWITCHES (0.1, 1.0, 5.0, 10) These pushbuttons select the frequency of operation associated with the two BNC connectors on the front panel (see NBS OUTPUT and LOCAL INPUT descriptions below). The frequencies measured by the counter on the front panel are also determined by these switches.

UNLOCK/LOCK LAMPS The red UNLOCK lamp, when lit, indicates that the receiver is not locked to the WWVB carrier. This condition is usually caused by improper antenna placement (see ANTENNA LOCATION in Section 1). The green LOCK lamp indicates that the receiver is phase locked with WWVB.

NBS OUTPUT This BNC connector provides an output signal that is phase locked to the WWVB signal whenever the green LOCK lamp is lit. The output frequency is selected with the FREQUENCY-MHZ switches.

LOCAL INPUT This BNC connector is the input jack for local frequency that is to be calibrated or to track against WWVB. Input frequencies must be the same as the selected frequencies.

PANEL METER (PHASE COMPARISON) Readout is phase comparison in microseconds of relative time. The scale, 50 or 10 microseconds, is selected on the rear panel.

COUNTER DISPLAY (FREQUENCY-HZ) This three digit display shows the last three digits of the count of the local input frequency. All higher order digits cause the OVERFLOW indicator to light. This light will stay on after the first count period is complete. The GATE light is on during the open gate period when the unit is counting.

COUNTER GATE CONTROLS The ON/OFF switch applies power to the counter when the button is pressed. The three center buttons are used to select the gate time/resolution of the count. The RESET button resets the display to zero and starts a new gate period.

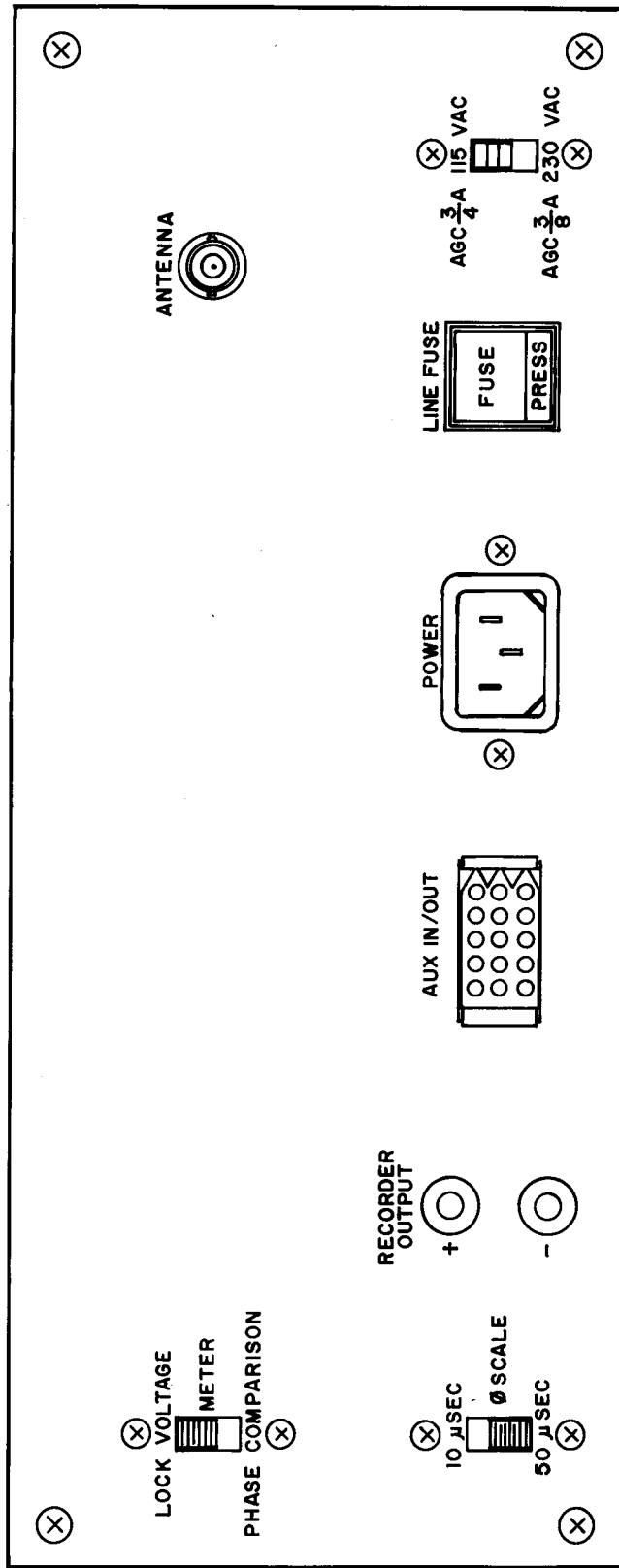


FIGURE 2-10 MODEL 8160A REAR PANEL

2.8 REAR PANEL FUNCTIONS

Use Figure 2-10, 8160A REAR PANEL, to locate the following.

METER SWITCH This switch selects LOCK VOLTAGE or PHASE COMPARISON information to be displayed by the front panel meter.

PHASE SCALE SWITCH This switch selects 10 usec. or 50 usec. scales for phase comparison.

RECORDER OUTPUT These jacks are used to drive an external recorder with 0-1 mA meter movement.

AUX IN/OUT (J6) Auxillary and remote functions of the receiver are available at this 15-pin connector. Use Figure 2-3, AUX IN/OUT J6 a view from the rear of the unit, to locate the pins.

PIN 1 PHASE COMPARATOR OUTPUT (+). For driving an external meter or chart recorder with a 0-1 mA meter movement. This pin is wired in parallel with the red RECORDER OUTPUT jack.

PIN 2 PHASE COMPARATOR OUTPUT (-). This pin is wired in parallel with the black RECORDER OUTPUT jack.

PIN 3 NO CONNECTION

PIN 4 TIME CODE OUTPUT (GND). Option 05 only.

PIN 5 PHASE LOCK OUTPUT (+). Option 05 only. Used for monitoring of receiver phase lock condition. This pin will be ground when the unit is unlocked, and +5 VDC behind 3.3K ohms when the unit is locked.

PIN 6 NO CONNECTION

PIN 7 TIME CODE OUTPUT (+). Option 05 only. Logic high is +5 VDC behind 3.3K ohms, logic low is ground.

PIN 8 60-HZ PHASE LOCKED OUTPUT (+). Options 14 & 15 only. TTL compatible (fan out, 2 maximum) 3.4 V rectangular positive pulses into 93 ohms minimum resistive load.

PIN 9 60-HZ PHASE LOCKED OUTPUT (GND). Options 14 & 15 only.

PIN 10 1.0-HZ PHASE LOCKED OUTPUT (+). Options 14 & 15 only. TTL compatible (fan out, 2 maximum) 3.4 V rectangular positive pulses into 93 ohms minimum resistive load.

PIN 11 1.0-HZ PHASE LOCKED OUTPUT (GND). Options 14 & 15 only.

PIN 12 1-KHZ OUTPUT. Option 28 only. TTL compatible (fan out, 2 maximum) 3.4 V rectangular positive pulses into 93 ohms minimum resistive load.

PIN 13 10-MHZ PHASE LOCKED OUTPUT (+). Option 05 only. TTL compatible (fan out, 2 maximum) 3.4 V rectangular positive pulses into 93 ohms minimum resistive load.

PIN 14 10-MHZ PHASE LOCKED OUTPUT (GND). Option 05 only.

PIN 15 1-KHZ OUTPUT (GND). Option 28 only.

POWER This is the input connector from the power source.

LINE FUSE This is the main power fuse for the unit. When operating this unit at 115 VAC use a 3/4 Amp fuse. If the unit is to be operated at 230 VAC use a 3/8 Amp fuse.

115 VAC/230 VAC SWITCH

TO PREVENT DAMAGE TO THE UNIT VERIFY THAT THIS SWITCH IS SET TO THE CORRECT INPUT VOLTAGE AND THAT THE CORRECT FUSE IS INSERTED IN THE FUSE HOLDER.

ANTENNA This BNC connector is the antenna input to the receiver.

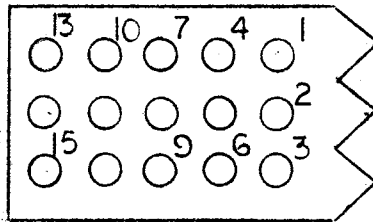


FIGURE 2-11 AUX IN/OUT

SECTION 3

PRINCIPLES OF OPERATION

- 3.1 General
- 3.2 RF Amplifier A1
- 3.3 Receiver Assembly A2
- 3.4 Counter A3

SECTION 3 PRINCIPLES OF OPERATION

3.0 INTRODUCTION

This section of the manual contains functional information on the RF AMPLIFIER A1, RECEIVER ASSEMBLY A2, COUNTER A3, COUNTER DISPLAY A3A1, and COUNTER TIME BASE A3A2.

3.1 GENERAL

Figure 3-1 MODEL 8160A RECEIVER BLOCK DIAGRAM shows the functional building blocks of the receiver. The 60 KHz WWVB signal is amplified and filtered by the RF Amplifier Assembly A1. A 10 MHz voltage-controlled crystal oscillator is phase locked to the 60 KHz signal. The divider in the phase locked loop provides switch selectable outputs of 10.0, 5.0, 1.0, and 0.1 MHz at the NBS OUTPUT connector on the front panel.

If option 05 is installed, (Standard on all units S/N 0476 and above) the time code modulation on the WWVB carrier is synchronously detected and brought out the AUX IN/OUT connector J6 on the rear panel. The WWVB time code is generated by the reduction of the carrier power by 10 dB at the beginning of each second. It is restored to full power 200 milliseconds later for a binary zero, 500 milliseconds later for a binary one, 800 milliseconds later for a position identifier. Decoding a one-minute stream yields day of the year, time of day, and a correction factor for converting from atomic time, UTC, to earth time, UT1. Figure 3-2 WWVB TIME CODE FORMAT shows the coded data in a one-minute stream.

The 10-dB reduction of WWVB carrier power is inverted in the demodulation process and appears as a positive-going TTL-compatible signal at the AUX IN/OUT J6 on the rear of the unit.

Figure 3-1 MODEL 8160A RECEIVER BLOCK DIAGRAM contains the logical blocks that make up the phase comparator. The local signal that is to be compared against WWVB must be one of the four standard frequencies, 0.1, 1.0, 5.0, or 10.0, MHz selected at the front panel FREQUENCY-MHZ switches. These switches control the divider that divides the input signal down to 20 KHz, for a full-scale meter deflection of 50 microseconds. The output of the comparator is also fed to an integrator that drives a buffer amplifier the output of which drives the front panel meter.

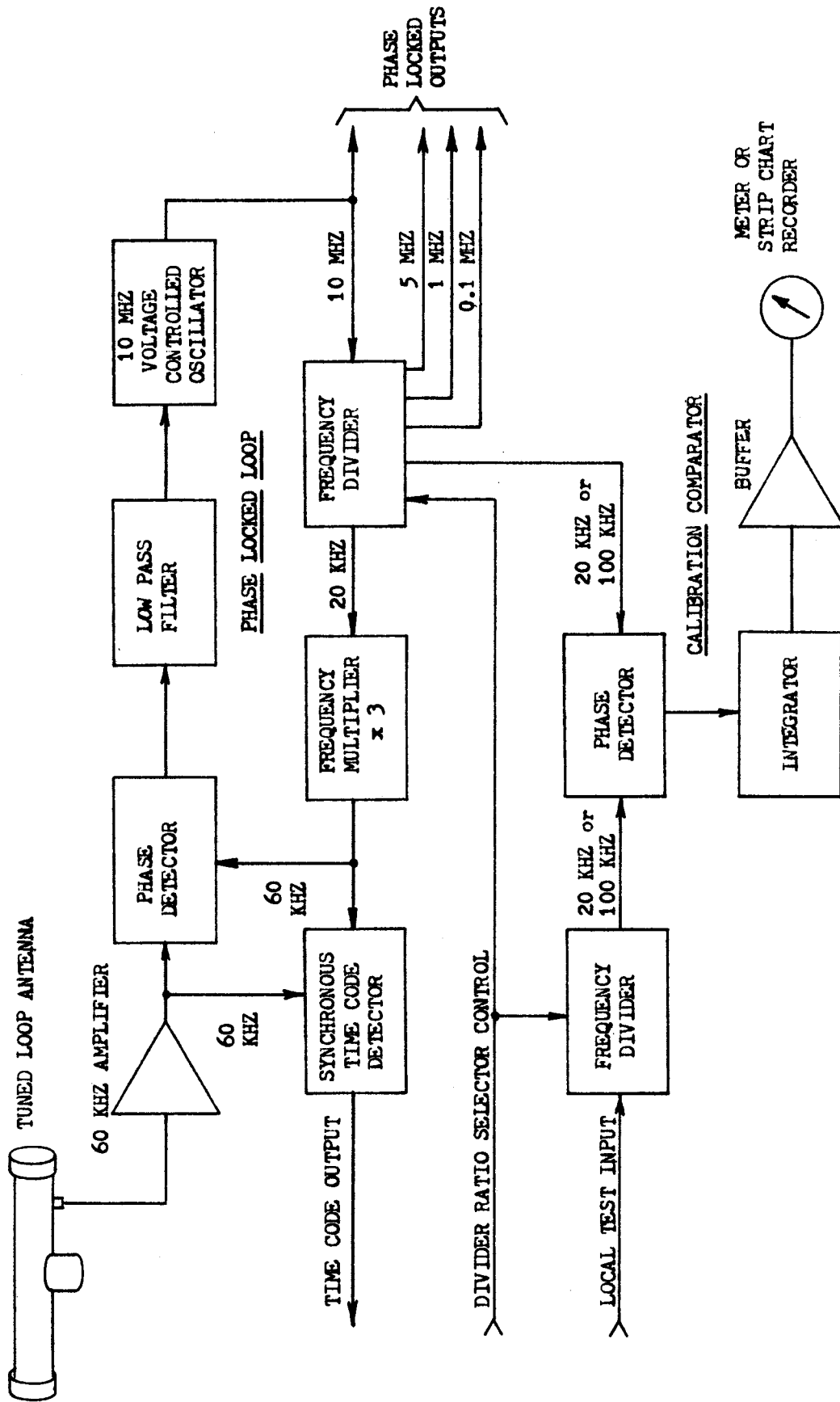


FIGURE 3-1 MODEL 8160A RECEIVER BLOCK DIAGRAM

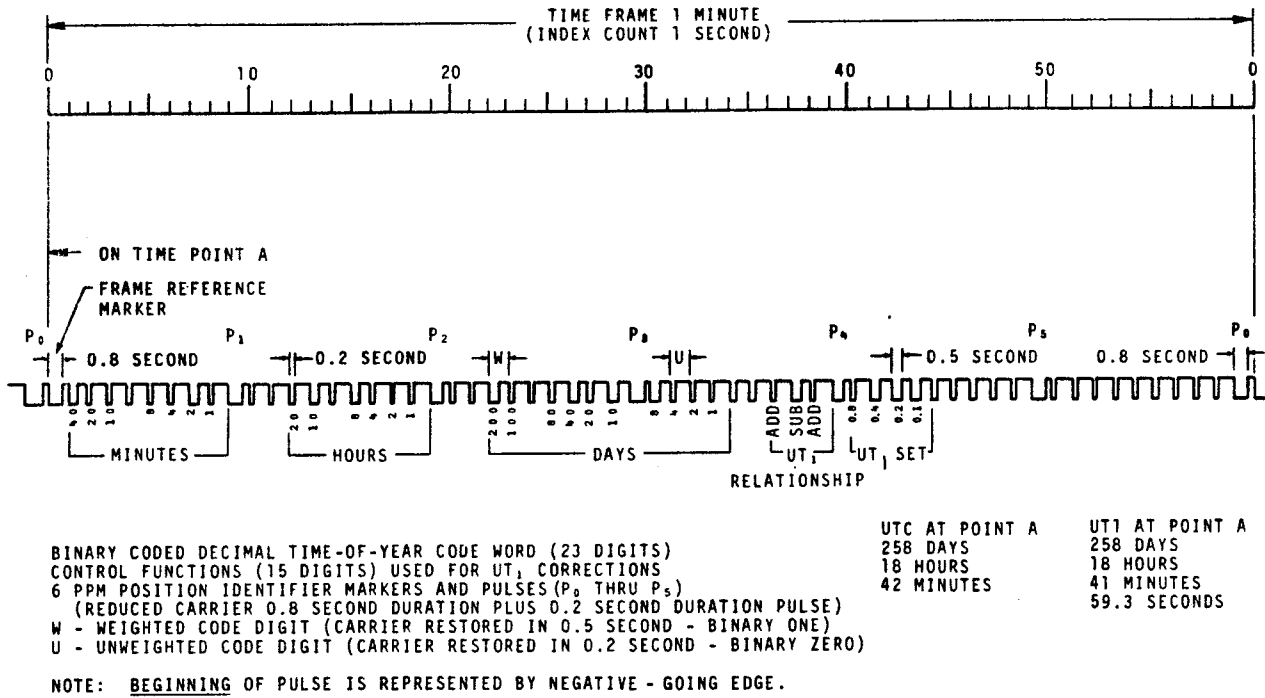


FIGURE 3-2 WWVB TIME CODE FORMAT

3.2 RF AMPLIFIER A1

The RF Amplifier Assembly filters and amplifies the signal. Figure 3-3 is the schematic diagram and Figure 3-4 is the component location diagram.

The signal from the antenna is applied to T1 which matches the 50-ohm input impedance. The secondary of T1 and C2 form a 60-KHz tuned circuit with a 200-Hz bandwidth. The output of Q1 is applied to a narrow bandpass filter, made up of Q2, Y1, C7, C8, C9, and C10, centered at 60 KHz. The filter bandwidth is 30 Hz, with C8 trimming the bandpass center frequency at 60 KHz. C9 and C10 couple to the output of Y1 a signal that is 180° out of phase and tuned to null 100 KHz. This tuning provides a sharp bandpass response at 60 KHz with very good high frequency rejection.

The output of the crystal filter is fed to U1. The output of U1 is tuned by L3, C14, C15, and C23. Amplifier U1 provides AGC for the receiver. Trimmer R19 provides AGC level adjustment to U1 at the gain control input U1 pin 5. The output of U1 is coupled to U2 by C16. The output of U2 goes to emitter follower Q3 providing the output signal to the A2 Receiver Assembly through P2-3.

The supply voltage, +12 VDC, enters the board at P2-1, from the A2 Assembly, through R18, L2, and L1, to power the amplifier stages. The 12 volts also goes to S1, R2 and through T1 to provide power to the antenna preamplifier. If a Model 8207 Line Preamplifier is used, S1 should be set to P.

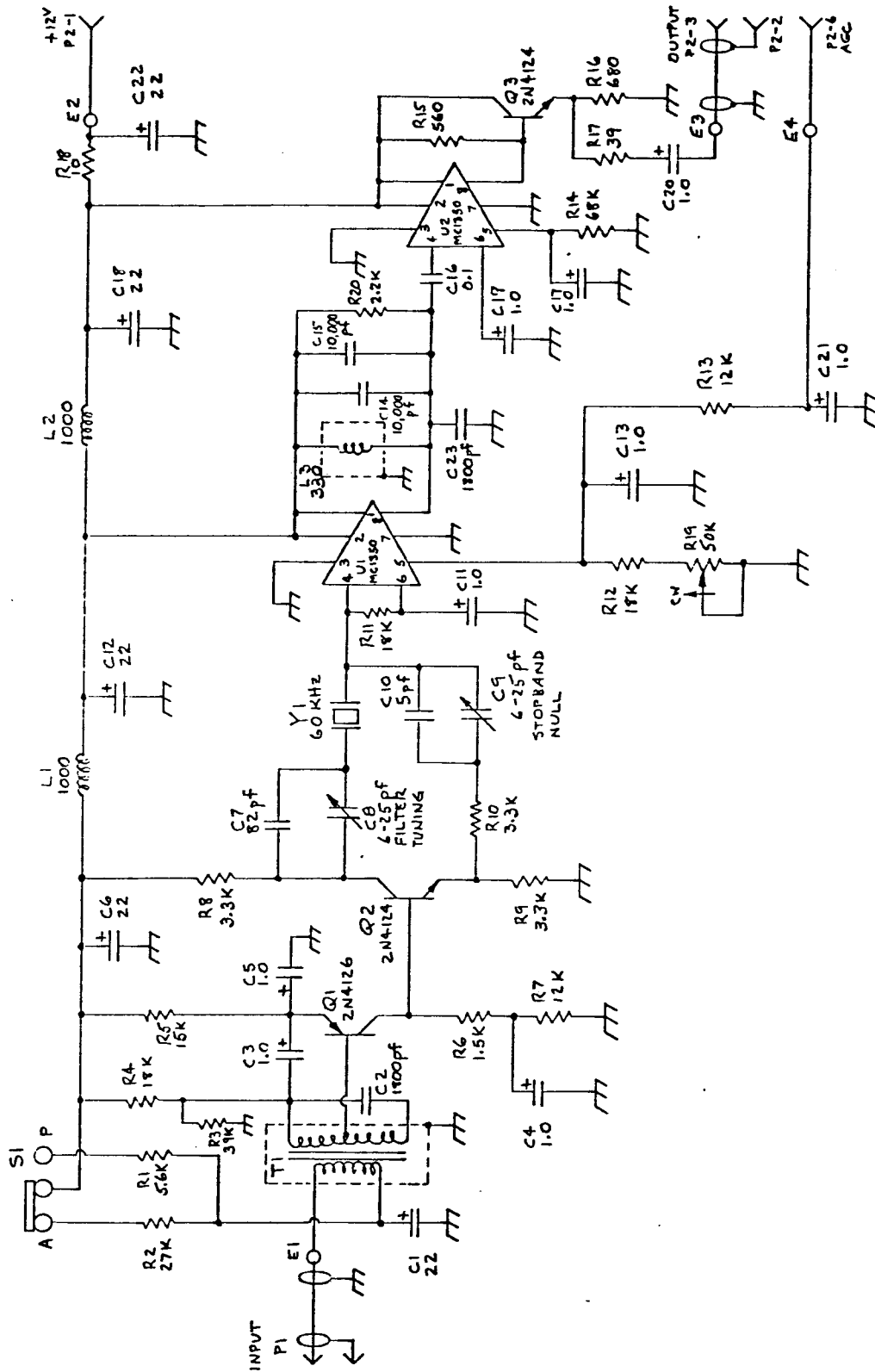


FIGURE 3-3 RF AMPLIFIER - A1 - SCHEMATIC

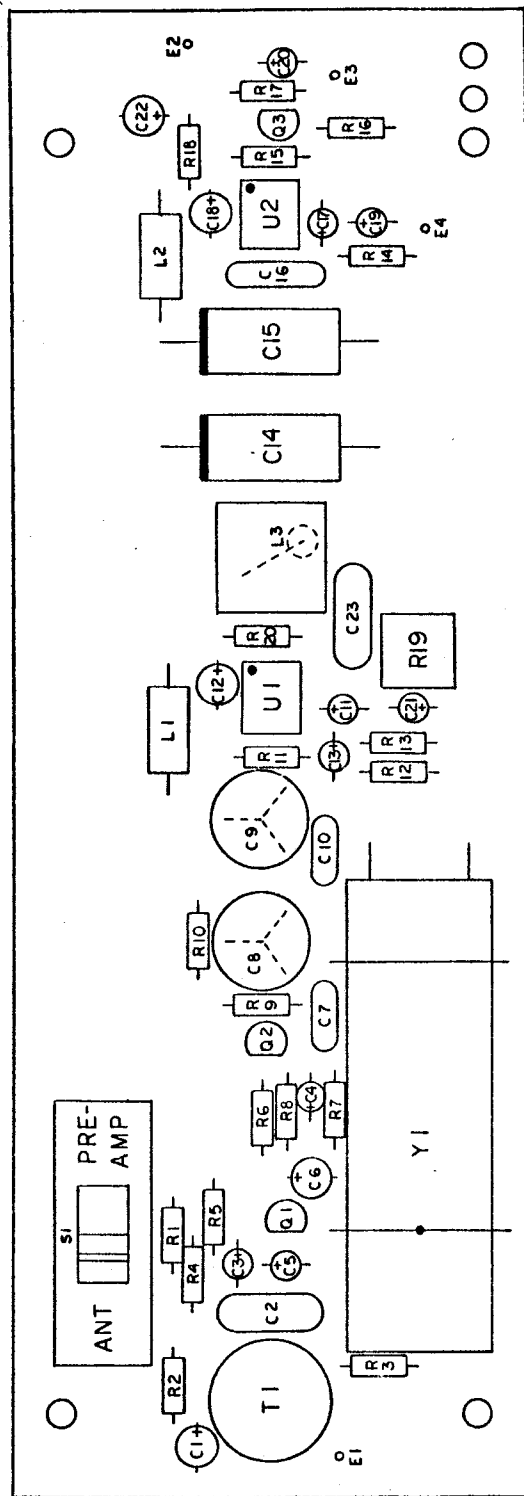


FIGURE 3-4 RF AMPLIFIER - AI - COMPONENT LOCATION DIAGRAM

3.3 RECEIVER ASSEMBLY A2

The Receiver Assembly A2 functions are:

1. Provides synchronous detection of the carrier frequency and translates it to 10 MHz.
2. Provides AGC voltage.
3. Time code detection.
4. Phase lock/unlock indication.
5. Derivation of front panel NBS OUTPUT signal from the 10 MHz phase locked oscillator.
6. Buffering, amplifying and dividing the external local oscillator input at the LOCAL INPUT connector and feeding it to the phase comparator.
7. The phase comparator which compares the local input frequency with the phase locked oscillator output to determine frequency error and drift.
8. The +12 VDC, -12 VDC, and +5 VDC power supplies are located on this assembly.

Figure 3-5 is the schematic diagram. Figure 3-6 is the component location diagram.

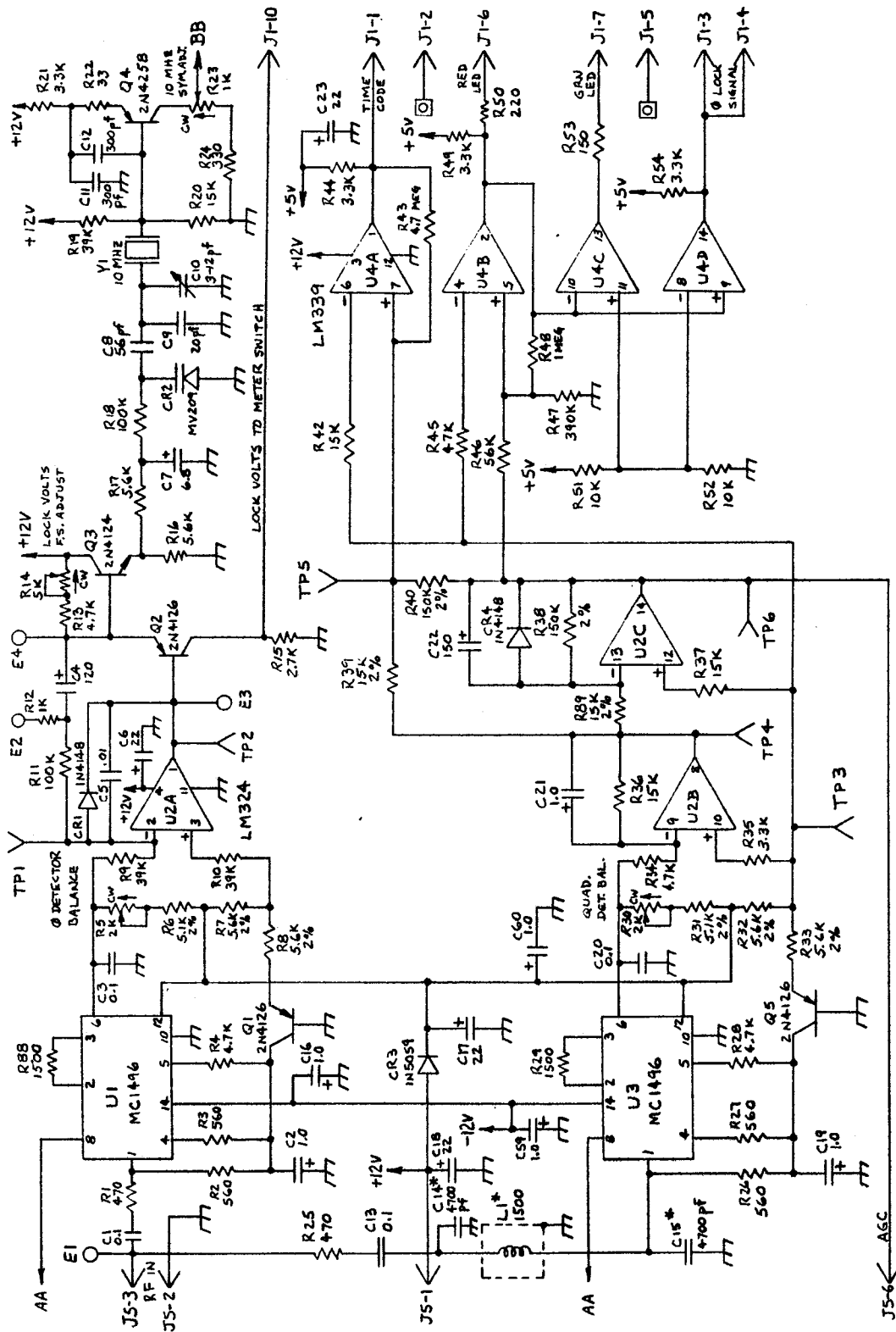
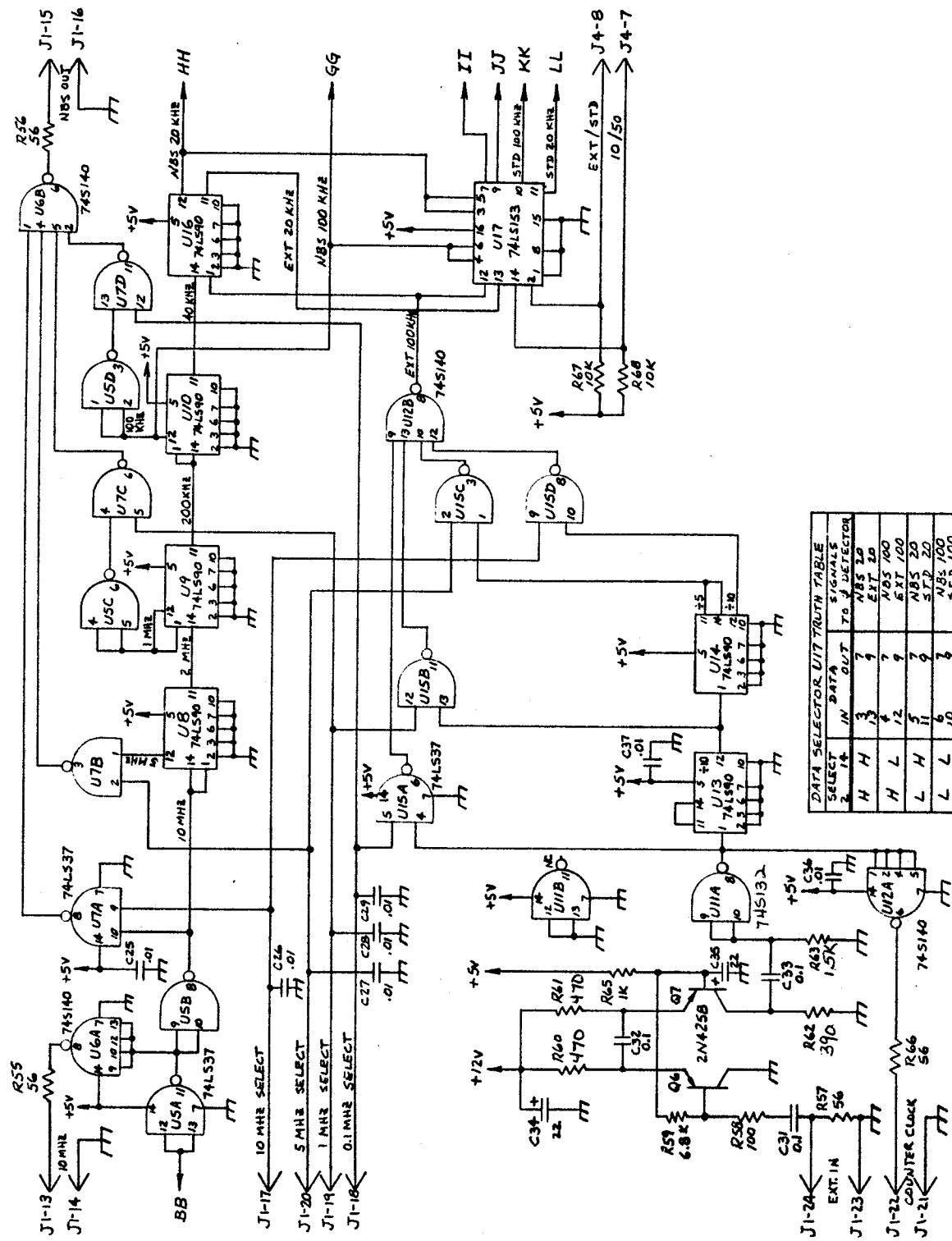


FIGURE 3-5 RECEIVER - A2 - SCHEMATIC, SHEET 1 OF 3



DATA SELECTOR U17 TRUTH TABLE			
SELECT	IN	DATA OUT	SIGNALS TO DATA SELECTOR
1	H	H	NBS 20
2	H	L	NBS 100
3	L	H	NBS 20
4	L	L	NBS 100

FIGURE 3-5 RECEIVER - A2 - SCHEMATIC, SHEET 2 OF 3

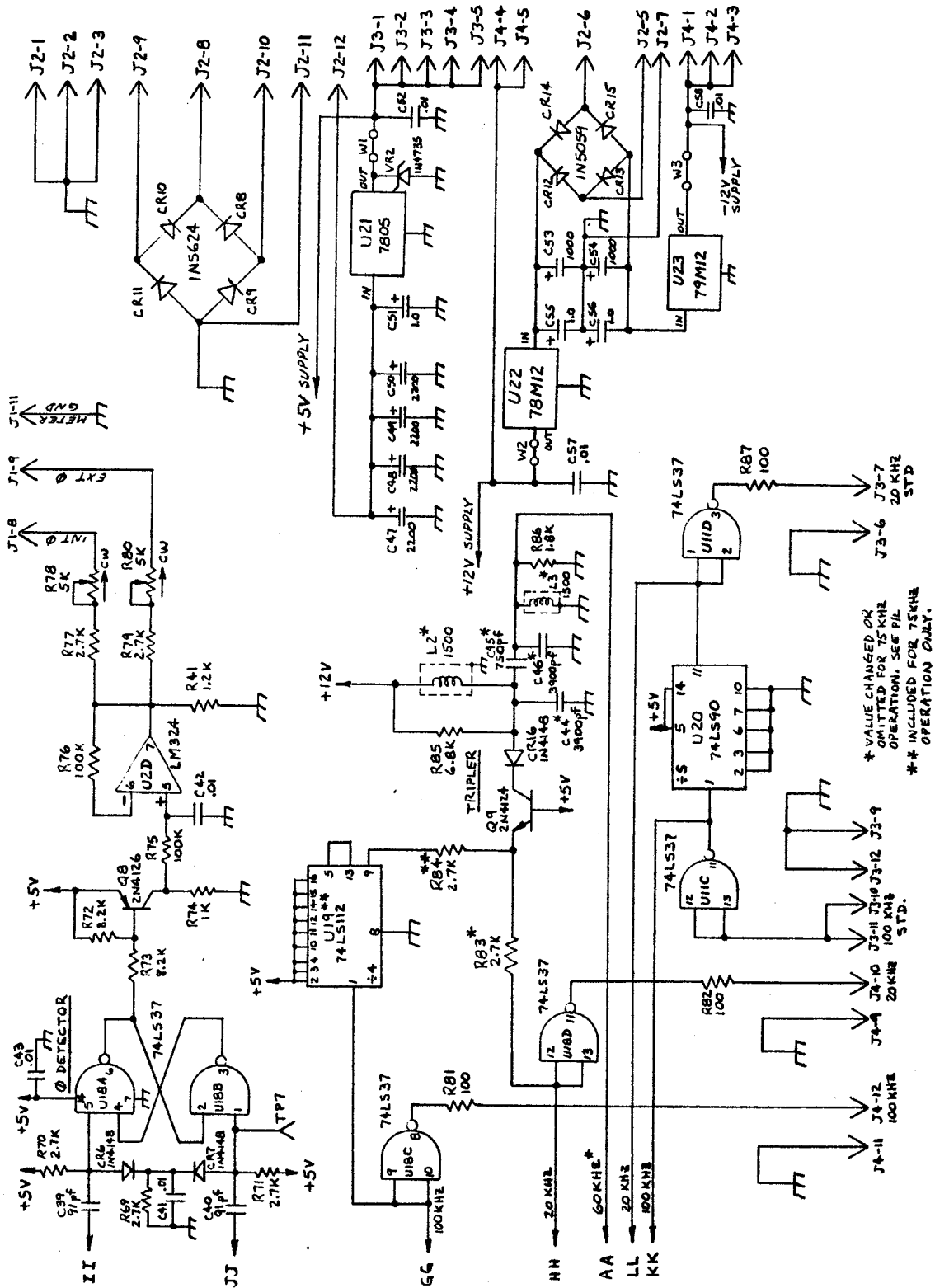


FIGURE 3-5 RECEIVER - A2 - SCHEMATIC, SHEET 3 OF 3

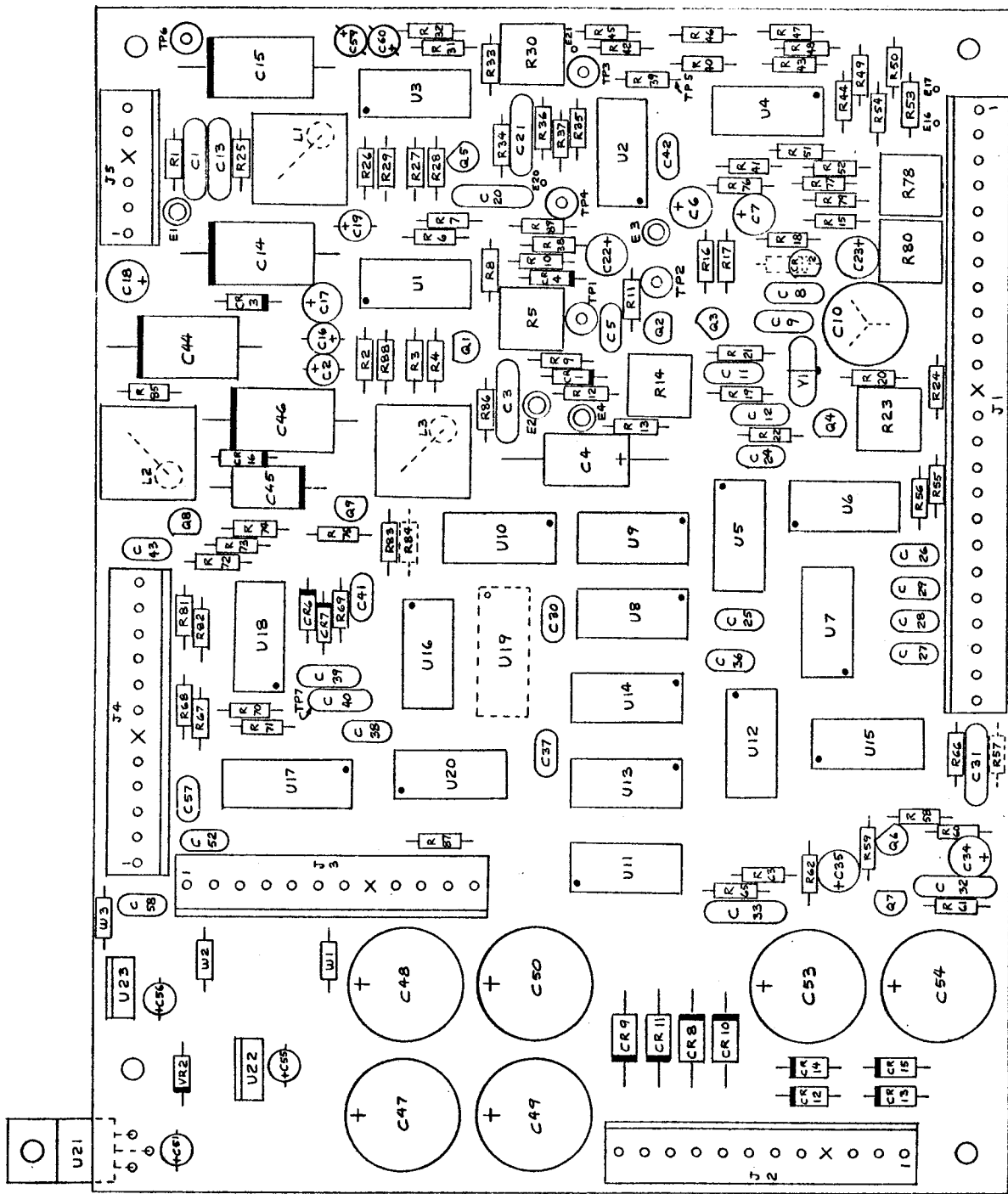


FIGURE 3-6 RECEIVER - A2 - COMPONENT LOCATION DIAGRAM

3.3.1 Phase Locked Loop

The reference input to the phase detector U1-1 comes from the A1 Assembly. The comparison frequency input to phase detector U1-8 is derived from the phase locked oscillator. The output from U1 is a DC voltage which is a function of the phase difference of these 60-KHz signals. The output is amplified by U2A, the loop filter/amplifier. This amplified DC voltage is further amplified by Q2 and Q3 where it becomes the VCO control voltage which pulls the oscillator (Q4 and Y1) into phase lock with the incoming carrier frequency from WWVB. This oscillator pulling is performed by the DC voltage which appears on the upper end of voltage variable capacitor CR2. The oscillator output frequency is held exactly at 10 MHz by the DC voltage applied to the VCO control line. The collector output from Q4 is buffered by gate U5A and divided by U8, U9, U10, and U16. At various points along the divider chain frequencies are selected and fed to the NBS OUTPUT connector at the front panel through gate U6B. NBS output frequency is selected by the FREQUENCY-MHZ switches through gates U7A, U7B, U7C, and U7D. This phase locked signal is divided down to 100 KHz and 20 KHz. These frequencies are buffered by U18A, U18D, and U18B which feed S1.

The 20-KHz output is injected to tripler stage Q9 where the output 60 KHz is filtered and fed back into the comparison input of phase detector U1-8. The phase locked loop translates the incoming 60-KHz carrier frequency from WWVB to 10 MHz at the crystal oscillator output, and divides it down to 60 KHz for comparison in the phase detector.

3.3.2 AGC Loop

The input from the RF Amplifier A1 goes to U3-1 phase detector after being shifted in phase 90° by C14, C15, and L1. U3-6 quadrature phase detector output goes high only when the inputs at U3-1 and U3-8 are in quadrature at 60 KHz. The output level from this phase detector is proportional to the level of the incoming carrier, and provides the basis for time code amplitude detection, and AGC voltage generation.

The phase detector output is amplified by U2B, the time constant of which is approximately 15 milliseconds. The output of U2B is split in two directions: first, through R39 to voltage comparator U4A where small amplitude variations in signal are detected and provide the time code output. Second, through R89 to amplifier U2C that has an integrating time constant of approximately 25 seconds. The slowly varying output of U2C is used as the AGC voltage. This AGC voltage is fed back to the RF AMPLIFIER A1 to control the gain of the input stage.

Because the AGC voltage is derived from the output of a quadrature detector, it is present only after phase lock is achieved, and becomes the basis for synchronous AGC. The gain of the amplifier in the front end is maximum until phase lock occurs. After phase lock is achieved the input amplifier gain is reduced to a level sufficient to provide a reference for the phase locked loop and other stages in the Receiver Assembly A2. No stages are allowed to saturate or be overdriven in strong signal conditions.

TP3 is located at the reference voltage against which AGC amplifier U2C operates. The voltage measured from TP3 to TP6 is proportional to the input signal level and can be used as an indication of signal strength. Optimum receiver operation is obtained when the antenna is adjusted and aimed to maximize this AGC voltage.

The AGC voltage is used by the voltage comparators U4B, U4C, and U4D to indicate phase lock. When the AGC voltage measured from TP3 to TP6 rises to approximately 1.0 VDC, the output of comparator U4B goes high turning off the red UNLOCK front panel indicator. When lock is acquired, the green LOCK indicator goes on. The output of U4D goes high and provides an output at J2-2 showing that phase lock has been achieved. This output is wired to J6-5 on the rear panel.

3.3.3 Phase Detector Balance Adjustment

The output of phase detector U1 for the phase locked loop control is balanced by adjustment of trimmer R5. The output of the quadrature phase detector U3 is balanced by adjusting trimmer R30.

3.3.4 Phase Comparator

When a local oscillator to be calibrated is connected to the LOCAL INPUT jack on the front panel the signal is injected at J2-11. The buffer amplifier Q6-Q7 feeds the signal to gate U11D where it is divided by U13 and U14. Gates U15A, U15B, U15C and U15D are used to select the appropriate divider output to provide a 100 KHz signal to S1 and divider U20.

If the phase comparator selector switch, S1 on the rear panel, is placed in the 50-usec position then the inputs to the phase detector U11B and U11A will be 20 KHz derived from the NBS received signal and 20 KHz from the signal being measured. The phase detector output will cause the meter to read 50 microseconds full scale.

If the rear-panel phase comparator scale switch, S1, is placed in the 10 usec position then the inputs to the phase detector will be 100 KHz derived from the NBS signal and 100 KHz derived from the signal being measured. The phase detector output will cause the meter to read 10 microseconds full scale.

U11A and U11B are connected as a flip-flop phase detector with an output pulse width that is proportional to the relative phase relationship between the two input pulses. Buffering of this output pulse is done by Q8, and integration of the output pulse by R75 and C42. Buffer amplifier U2D then drives the front panel meter and the AUX OUTPUT for an external meter or chart recorder. Full scale adjustments of both are made by adjusting the current to ground through a milliammeter at each output to exactly 1.0 mA with no local signal input and with TP7 grounded, causing the phase detector to indicate full scale. Trimmer resistor R80 adjusts full scale setting of AUX OUTPUT and R78 is used to adjust the front panel full scale meter reading.

3.3.5 Power Supplies

The power supply is shown in Figure 3.1 Model 8160A Receiver Block Diagram. The +5V is derived by voltage regulator U21, and VR2. This voltage is used to power the TTL circuits.

The +12V is derived by voltage regulator U22, and the -12V at U23.

3.4 COUNTER A3

This three digit counter is a high-resolution digital means of measuring the error of a standard frequency when it is fed into the local input jack on the Model 8160A front panel. The counter uses as its time base the NBS output signal which is phase locked to the incoming WWVB carrier frequency. Only three of the lower order digits are displayed on the front panel. All of the higher order digits are allowed to overflow the counter since the standard frequency being counted is a known frequency, and only the frequency error is unknown.

Three gate periods may be selected: 1 second, 10 seconds, and 100 seconds. These gate periods provide measurement resolution of 1 Hz, 0.1 Hz, and 0.01 Hz for a 10 MHz signal into the LOCAL INPUT. The decimal point is automatically positioned when the gate period is selected using the front panel pushbuttons underneath the display.

Because of the long gate periods that may be selected, a manual reset button is provided to begin a measurement period again before the gate period is completed.

An LED indicator shows when the gate is "open" and counting is proceeding. A second indicator LED shows counter "overflow" which occurs continuously after the first gate period has passed. This reminds the operator that only the last three digits of the count are being displayed, and the remaining higher order digits have overflowed to the left of the readout.

When measuring the frequency of an oscillator, the measurement may be converted into fractional frequency error by dividing the absolute error by the frequency of the oscillator. For example, a readout of 0.07 Hz when measuring a 1-MHz oscillator would yield a fractional frequency error of 7 parts in 10^8 . Similarly, a reading of 9.93 Hz yields a fractional frequency error of 7 parts in 10^8 . In this case the oscillator is low by that amount.

3.4.1 Circuit Description

The counter is divided into two circuit boards, A3A1 Display Assembly, which contains the digital displays, the counter chips, and some timing controls for latch strobe, reset, etc. The second circuit board, A3A2, is the time base assembly, which generates the counter's gate pulse from a 20-KHz input which is derived from the phase locked oscillator in the WWVB receiver. This board also contains the pushbutton selector switches for choosing gate period and manual reset.

The schematic diagram of the counter is shown in Figure 3-7. Figures 3-8 and 3-9 show the component locations for the A3A1 and A3A2 assemblies.

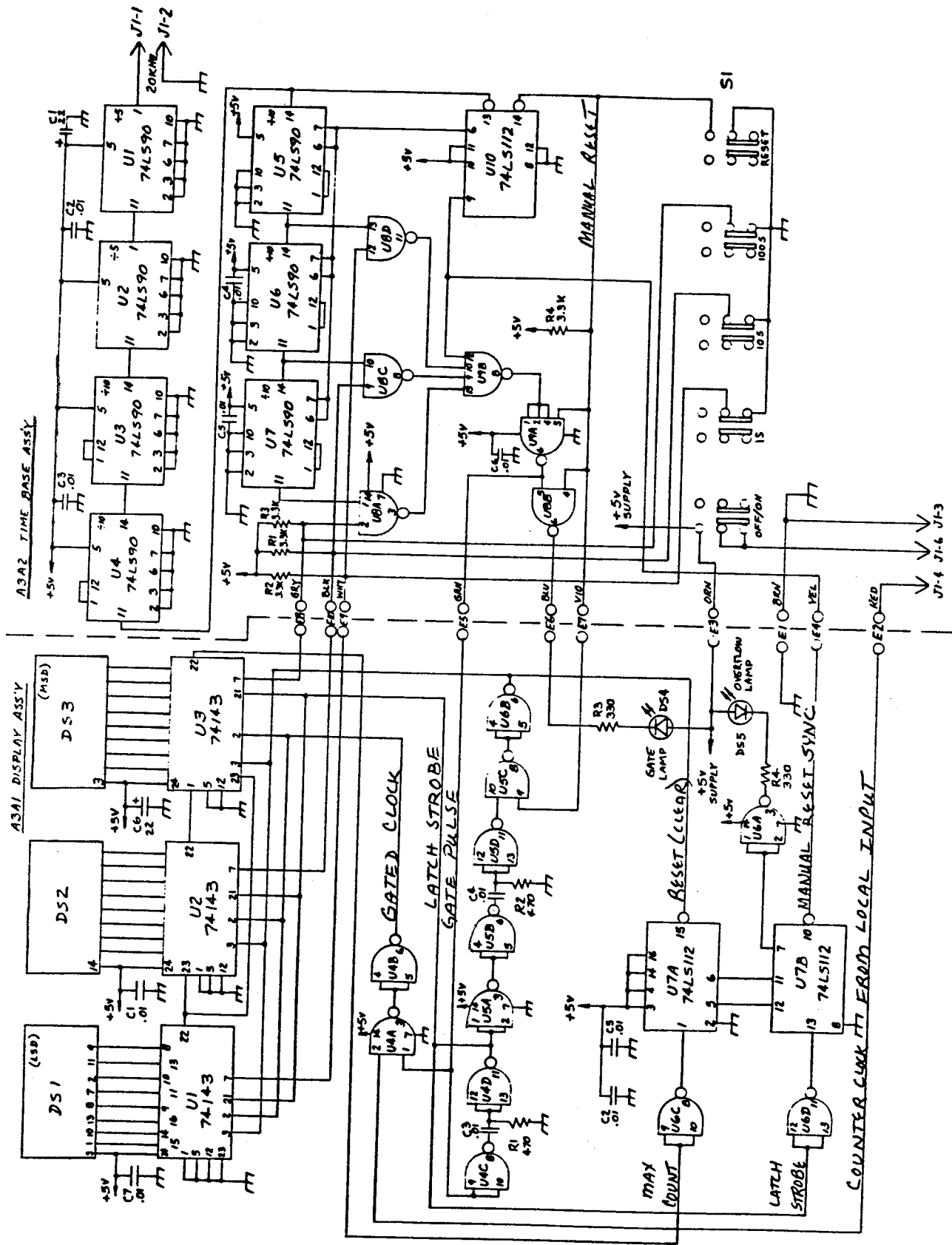


FIGURE 3-7 COUNTER - A3 - SCHEMATIC

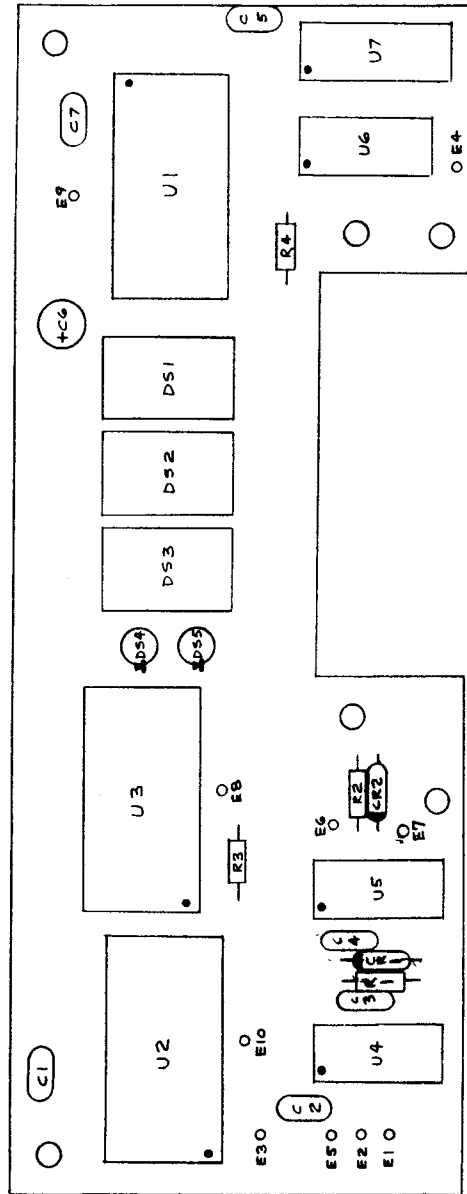


FIGURE 3-8 COUNTER DISPLAY - A3A1 - COMPONENT LOCATION DIAGRAM

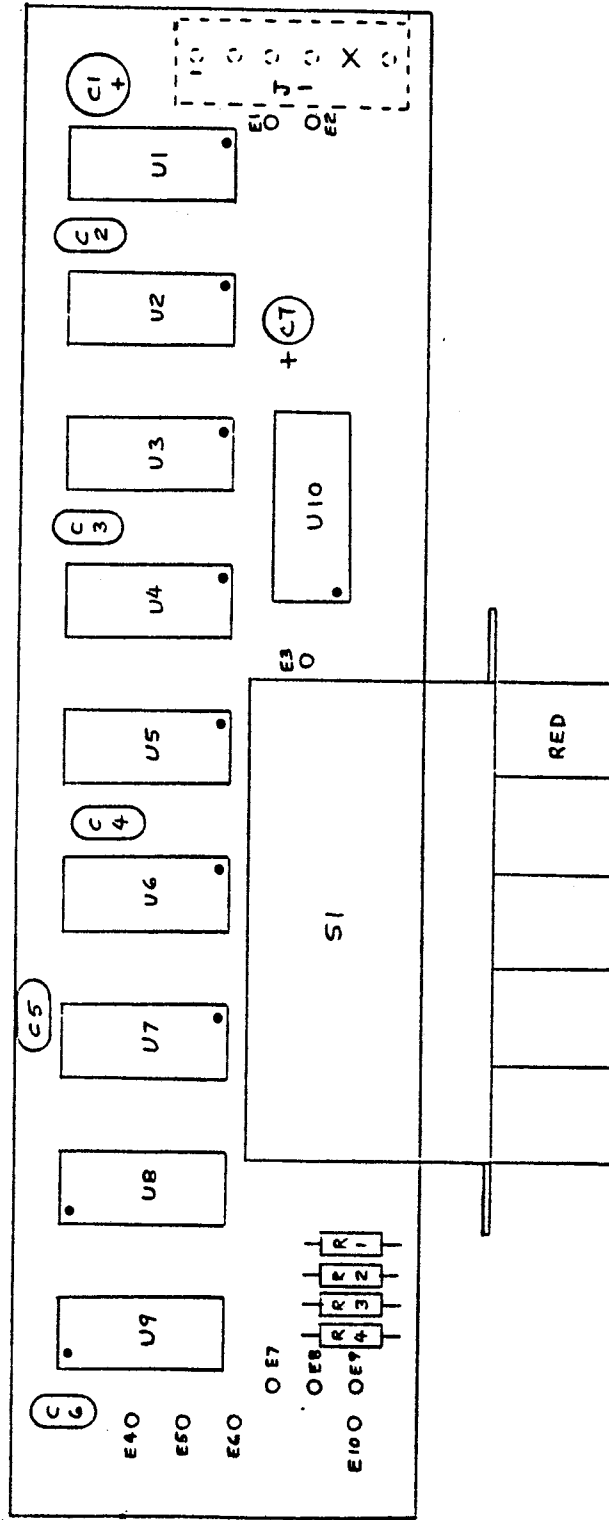


FIGURE 3-9 COUNTER TIME BASE - A3A2 - COMPONENT LOCATION DIAGRAM

3.4.2 Counter Display A3A1

DS1, DS2, and DS3 are the LED digits which display the frequency count. DS1 is the least significant digit, viewed by the operator on the right of the display. U1, U2, and U3 are the decade counters. The local input from the front panel is counted by these chips, under gate control furnished by the A3A2 board. U4A is the "gate" for the counter which turns on and off the local input signal which is being counted by the counter. The clock signal being counted is fed to pin 2 of this gate and the gate pulse from the time base assembly is fed to pin 1, allowing the clock signal to pass through when the gate pulse is high, and shutting it off when the gate pulse is low. U4C and U4D provide a narrow pulse, slightly delayed from the falling edge of the gate pulse which strobes the counter latches when a count period is completed. U5 and U6B provide a reset pulse which clears the counter after the latch strobing is complete. The counter is then ready to begin another count period when the next gate pulse arrives. Whenever the gate is open and the counter is counting, the gate lamp, DS4, is lit.

U7 consists of two flip-flops which coordinate the lighting of the overflow lamp, DS5. This lamp is lit and latched on whenever a latch strobe pulse is received, signifying the end of a count period, and maximum count output pulses have been received from the most significant digit counter, U3 pin 22. The lamp turns on at the end of the first gate period and remains on until a manual reset pulse is received or until the local input clock signal is removed and the counter no longer has a signal to count.

3.4.3 Counter Time Base A3A2

Integrated circuits U1 through U7 are dividers which provide the three selectable gate periods from the 20-KHz input from the receiver. The outputs from U5, U6, and U7 are the three selectable gate pulses with 4:1 duty cycles. U5 provides the 1-second gate, U6 provides the 10-second gate, and U7 the 100-second gate. All three IC's have an output duty cycle of 4:1 that is, the gate pulses are high for either 1, 10, or 100 seconds and low for 1/4 of this amount of time. U8 and U9 are used to select the appropriate gate pulse to feed to the A3A1 circuit board under control of the pushbutton selector switch. U10 synchronizes the beginning of a manual reset command so that counting does not begin in the middle of a gate period.

SECTION 4

OPTIONS AND ACCESSORIES

- 4.1 Option 01, Rack Mount Kit
- 4.2 Option 05, Time Code Output
- 4.3 Option 14, 60 Hz Comparator
- 4.4 Option 15, Timing Pulse Output
- 4.5 Option 28, 1 KHz Output

SECTION 4: OPTIONS AND ACCESSORIES

4.1 OPTION 01 RACK MOUNT KIT

Units purchased with the rack mount kit option must be modified as shown in Figure 4-1, RACK MOUNT OPTION 01.

4.1.1 Installation

1. Remove feet and tilt bar.
2. Remove vinyl-covering from panels behind the handles on the sides of the unit.
3. Install the rack mounting brackets to the sides of the unit using oval head #10-32 x 3/8 screws provided.
4. Install panel extension.
5. Install unit in rack using truss head #10-32 x 3/8 screws.

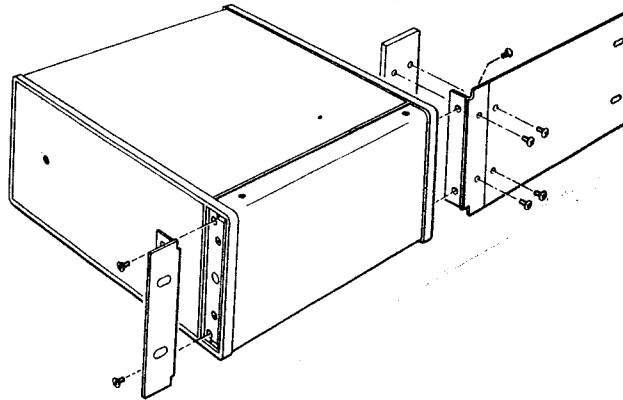


FIGURE 4-1 RACK MOUNT OPTION 01

4.2 OPTION 05 TIME CODE OUTPUT (STANDARD ON ALL UNITS S/N 0476 AND ABOVE)

The time code generated by WWVB is used for the calibration of synchronous clocks and other timekeeping equipment. The time code modulation consists of once-per-second pulsed amplitude reductions of 10 dB, lasting 200, 500, and 800 milliseconds. Decoding a one-minute data stream of this BCD time code gives date, time of day, and a correction factor for converting from atomic time to celestial time. Outputs are a TTL DC level shift, and a 10 MHz TTL signal, phase locked to the WWVB carrier. They can be monitored at the AUX IN/OUT connector, J6, on the rear panel. The SPECTRACOM MODEL 8171 WWVB Synchronized Clock can be used to decode the time.

4.3 OPTION 14 60Hz COMPARATOR (Includes Option 15)

This option enables the instrument to compare power line frequencies with the 1000th subharmonic of the 60 KHz WWVB carrier, establishing direct traceability to the National Bureau of Standards.

Phase Comparator: Full-scale meter range is one cycle at 60 Hz (16.7 msec of relative time). Allows real time setting of generator frequency to within 0.01 Hz of 60 Hz compared to WWVB. Measurement time of 10 seconds yields resolution of 0.001 Hz; 100 seconds, 0.0001 Hz, etc. Accuracy limitation is 1×10^{-11} with good signal reception, and worst case is typically 1×10^{-5} during complete loss of signal. External meter or chart recorder with 0-1 mA movement may be driven from rear panel output.

Frequency Counter: Three digit display with overflow, gate lamps, and manual reset button. Selectable gate times of 1, 10, and 100 seconds give resolutions of 1, .01, and 0.01 Hz respectively. Gate signal is phase locked to WWVB carrier, with accuracy of 1×10^{-7} under normal reception conditions, 1×10^{-5} after complete loss of signal. Readout accuracy is ± 1 count.

Panel Selector Switch: "LOCAL" position allows unit to be used for normal frequency standard calibrations at 0.1, 1.0, 5.0, or 10.0 MHz. "INT LINE" position causes unit to compare the power line from which the unit is operating with WWVB. "EXT LINE" position allows comparison of an external line frequency with WWVB when fed into the front panel BNC connector.

NOTE

THE FRONT PANEL CHANGES WHEN OPTION 14 IS INSTALLED.

Figure 4-2 sheets 1 and 2 are the schematic diagrams for OPTION 14 and 15. Figure 4-3 is the component location diagram for these options.

4.4 OPTION 15 TIMING PULSE OUTPUT

This option provides both 60 Hz and 1.0 Hz at the rear panel AUX/OUTPUT J6 which are phase locked to the WWVB carrier. The 60 Hz signal can be monitored at J6-8. J6-9 is the ground return. The 1.0 Hz output is on J6-10. J6-11 is the ground return. The pulses use symmetrical 3.4 V rectangular positive pulses that are TTL compatible. These outputs will also drive terminated lines with impedances as low as 93 ohms resistive.

Typical long-term accuracy with normal signal reception is 1×10^{-11} and short-term accuracy for a one-second averaging time is 1×10^{-7} . During loss of signal accuracy gradually decreases to typically worst case of 1×10^{-5} .

A rear panel indication of receiver lock can be monitored at J6-5. The levels are ground when unlocked and +5 V behind 3300 ohms when locked. If Option 14 is ordered, then Option 15 is present.

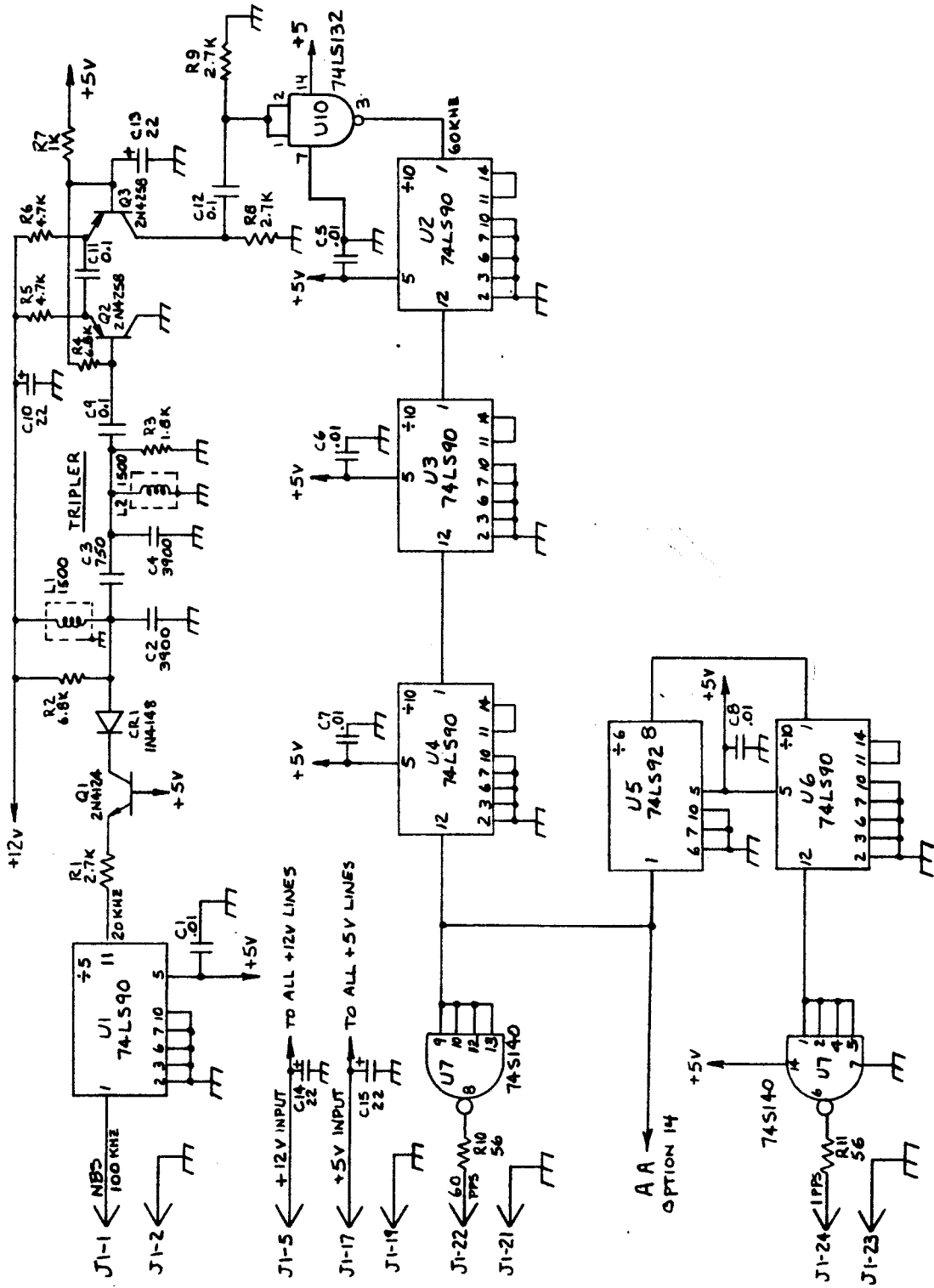


FIGURE 4-2 OPTION 14 - SCHEMATIC, SHEET 1 OF 2
 OPTION 15 - SCHEMATIC, SHEET 1 OF 1