MODEL 8164

WWVB DISCIPLINED OSCILLATOR

INSTRUCTION MANUAL

PLEASE NOTE OUR NEW ADDRESS

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REVISION 3.0 - 08/89
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2. SERIAL NUMBER
3. DESCRIPTION OF TROUBLE
4. CONDITIONS AND HOURS OF USE

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DEPARTMENT_____ MAIL STOP_____

COMPANY_____ MODEL NUMBER_____

ADDRESS_____ SERIAL NO._____

CITY_____ DATE INSTALLED_____

STATE_____ ZIP_____

PHONE_____ EXT._____

REMARKS: (PROBLEMS, SUGGESTIONS, ETC.)_____

MODEL 8164

S/N 8164 _____

CERTIFICATE OF TRACEABILITY

SPECTRACOM CORPORATION HEREBY CERTIFIES THAT ITS MODEL 8164 STANDARD FREQUENCY RECEIVER PROVIDES DIRECT TRACEABILITY TO THE NATIONAL BUREAU OF STANDARDS REFERENCE FREQUENCY AS TRANSMITTED BY STATION WWVB IN FORT COLLINS, COLORADO, WITH CARRIER FREQUENCY OF 60 KHZ.

AUTOMATIC VERIFICATION IS PROVIDED BY THE STATION IDENTIFYING PHASE SHIFT OF 45° THAT APPEARS ON THE CARRIER SIGNAL AT 10 MINUTES AFTER EACH HOUR, RETURNING TO NORMAL FIVE MINUTES LATER. THIS PHASE SHIFT APPEARS IN THE READOUT AS AN OFFSET IN THE STRIP CHART RECORD AND ON THE PANEL METER.

WHEN PROPERLY INSTALLED AND MAINTAINED, THE MODEL 8164 PROVIDES MEASUREMENT ACCURACY AND RESOLUTION AS PUBLISHED IN THE EQUIPMENT'S INSTRUCTION MANUAL.

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SPECTRACOM CORPORATION

MODEL 8164

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MODEL 8164

SECTION 1

INSTALLATION

1.0 INTRODUCTION

The SPECTRACOM MODEL 8164 WWVB RECEIVER DISCIPLINED OSCILLATOR* is a frequency standard with accuracy directly traceable to the National Bureau of Standards. The SPECTRACOM MODEL 8206 ferrite loop antenna is used to receive to 60 kHz carrier of WWVB.

The Model 8164 is continuously monitored against WWVB and kept on frequency by a microprocessor. The oscillator outputs can be used as a precise external input for transmitters, receivers, counters, synthesizers, and other electronic equipment. Figure 1-1 shows the Model 8164 Disciplined Oscillator and the Model 8206 Antenna.

1.1 FEATURES

The Model 8164 WWVB Receiver-Disciplined Oscillator offers the following features:

BUILT-IN PHASE COMPARATOR - may be used to compare the phase of the internal ovenized oscillator or local input with the received WWVB signal. Results are recorded on the strip chart recorder.

TRACEABILITY - verification to the National Bureau of Standards is done by noting the hourly WWVB phase shift identification. The hourly offsets appear as "tick" marks on the strip chart recording.

ALARM STATUS - operational status is communicated by alarm lamps and RS-422 alarm outputs.

SELECTABLE FRONT PANEL OUTPUTS - 0.1, 1.0, 5.0 or 10 MHz TTL compatible signals of the phase locked and standard oscillator outputs.

FREQUENCY OFFSETS - with the addition of a frequency offset option, the internal 10 MHz standard oscillator is offset a precise amount. The offset frequency used as a reference to a television or paging transmitter reduces or eliminates co-channel interference.

DISTRIBUTION OUTPUTS - with the addition of Option 03, Built-In Distribution Amplifier, up to 25 remote stations may use the standard outputs as a common time base.

1.2 UNPACKING

Upon receipt, the carton and its contents should be carefully examined. If there is damage to the carton which results in damage to the unit, contact the carrier immediately so his representative may witness such damage. If you fail to report shipping damage immediately, you may forfeit any claim against the carrier. You should also notify Spectracom Corporation of shipping damage or shortages so that we can help you obtain a replacement or repair the damaged equipment.

* PATENT NO 4,525,685

FIGURE 1-1 MODEL 8164 WWVB RECEIVER-DISCIPLINED OSCILLATOR AND MODEL 8206 ANTENNA

Carefully open the shipping carton and remove the packing list from the envelope on the outside of the carton. Check the packing list against the contents to be sure all items have been received, including an owner's manual and ancillary kit.

Retain the carton and packing materials in the event the unit needs to be reshipped or returned to the factory.

1.3 RESHIPMENT

Use the original shipping carton if it is necessary to return the unit to the factory. If it is not available, a carton of at least 250 pound test corrugated paper with at least two inches of polyethylene foam surrounding the unit must be used. Seal the unit in a plastic bag for moisture protection and include a note stating the reason for the return. Return authorization must be obtained from Spectracom. IF OPTION 34 IS INSTALLED, BE SURE TO SWITCH THE REAR PANEL BATTERY SWITCH TO EXT TO DISCONNECT THE BATTERY PRIOR TO SHIPPING.

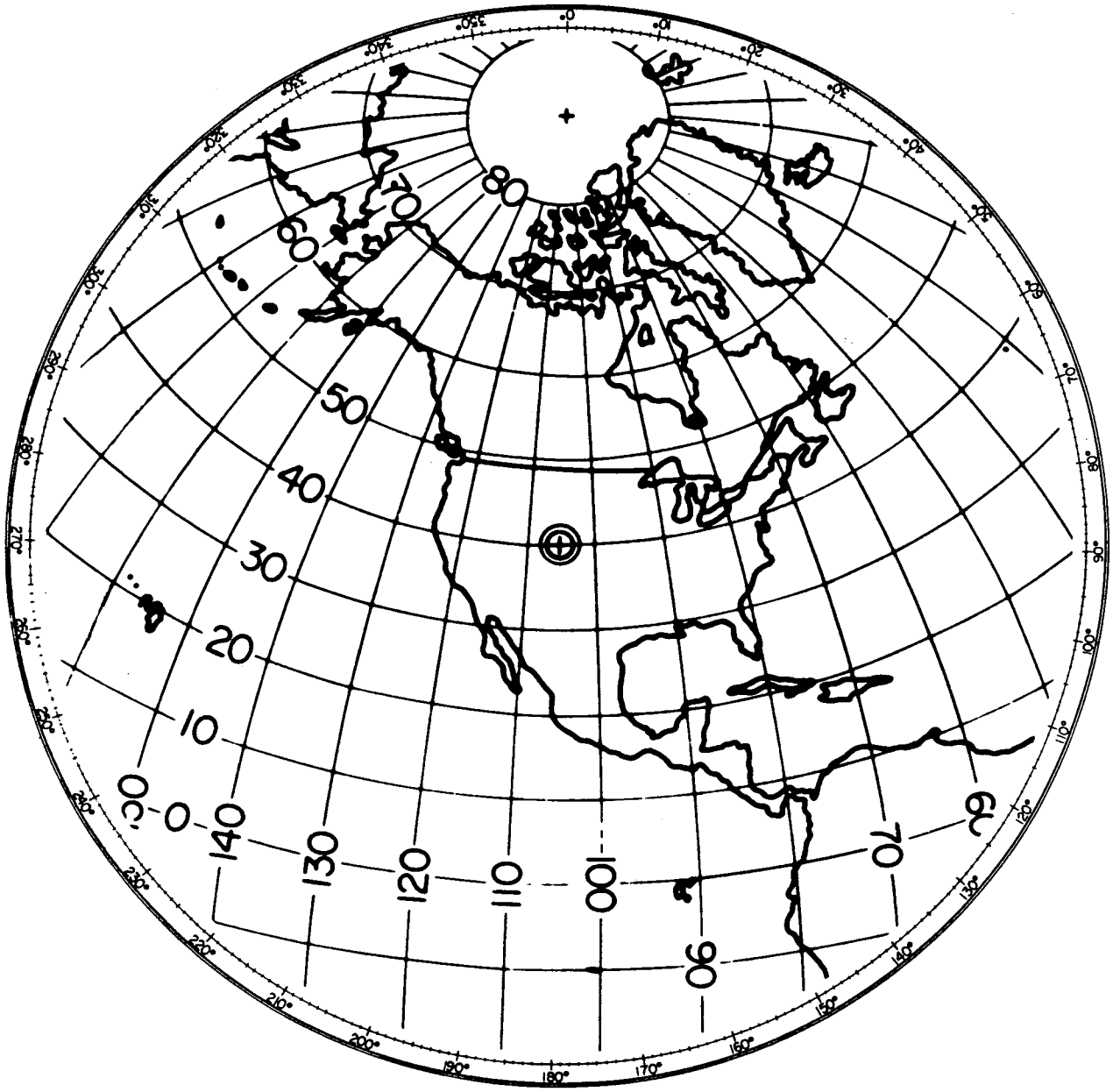
1.4 MODEL 8206 LOOP ANTENNA

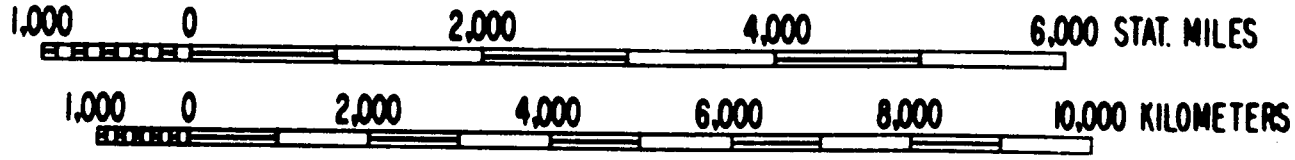
The Model 8206 is a high gain directional ferrite loop antenna in a tubular housing 14-1/2L x 2-3/4 Dia (inches). It contains a built-in preamplifier which receives its DC power from the receiver over the coaxial cable center conductor. The antenna equivalent electrical height is 5.0 cm.

1.5 ANTENNA LOCATION

The antenna should be mounted a minimum of 25 feet from the receiver to prevent regeneration. The antenna MUST NOT be positioned next to the receiver or on top of it. Doing so will make the results obtained with the equipment meaningless even though the green lock lamp on the receiver front panel may be lit.

The antenna must be at least three feet from any steel beams, roof decking, pipes, etc., as metal will detune the antenna and can cause as much as 20 dB degradation of the signal-to-noise ratio. The antenna must not be mounted under a metal roof or inside a building with heavy steel structural supports, as these shield the antenna from the signal. Roof tops are generally best if a clear shot toward Fort Collins is available without being blocked by a large steel structure. Attics are ideal sites if the roof and rafters are not metallic. The signal-to-noise ratio will be optimized if the antenna is located as far as possible from local RF noise sources such as TV sets, or fluorescent or neon lamps that blink or sputter on and off. Any equipment containing a switching power supply is a probable cause of interference.





TO AIM ANTENNA AT FORT COLLINS, COLORADO, DETERMINE COMPASS HEADING FROM THIS MAP.

Draw a straight line from the receiver location through Fort Collins, Colo. at the center of the map. Continue until the line intersects the outer ring. The point at which the line intersects the outer ring indicates the compass heading for Fort Collins from your location.

FIGURE 1-2 GREAT CIRCLE MAP CENTERED ON FORT COLLINS, COLORADO

1.6 ANTENNA INSTALLATION

The antenna should be supported by a non-metallic pipe such as one-inch PVC water pipe and mounted where it will not be disturbed. Holding the antenna two or three feet off the ground or rooftop is adequate in most cases. The tubular housing must be positioned broadside to Fort Collins, Colorado, where the transmitter is located (see Figure 1-3) and horizontal to the ground to allow maximum signal reception. No signal will be received if the tube points directly toward the transmitter site, as the antenna pattern nulls are located off the ends of the tube. The Great Circle map shown in Figure 1-2 is used to determine the correct antenna orientation per receiver location. The antenna position may be optimized using the signal strength measurement described in Section 2, Operation.

> CAUTION: HANDLE THE ANTENNA WITH CARE. DROPPING OR ROUGH HANDLING MAY CRACK THE FERRITE CORE POSSIBLY DETUNING THE ANTENNA, RENDERING IT USELESS.

When the lead-in coaxial cable (RG-58/U is recommended) is connected from the antenna to the receiver, the system is ready for use if the antenna has been installed and aimed properly. The antenna has a built-in preamplifier that receives its DC operating voltage through the coaxial cable; therefore, both the center conductor and the shield of the cable must be continuous from the antenna to the receiver. Antenna cables can be run up to 2,000 feet providing care is taken to avoid paralleling noise sources whenever possible.

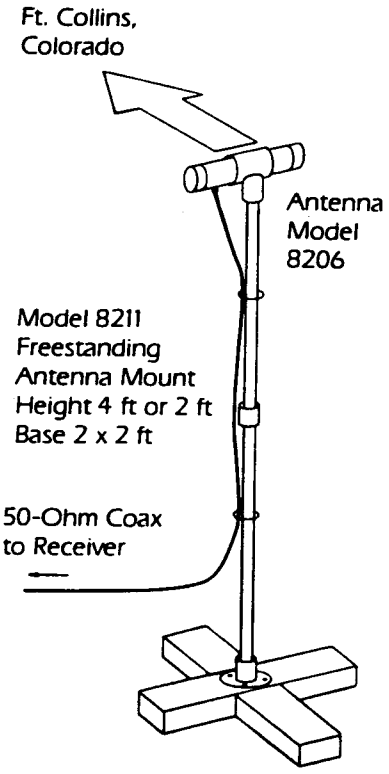


FIGURE 1-3 ANTENNA MOUNT MODEL 8211

1.7 MODEL 8211 ANTENNA MOUNT

The Model 8211 Antenna Mount as shown in Figure 1-3, consists of two 2-foot sections of 1" PVC pipe with male and female adapters. The base contains a mounting flange and two cross members. If the antenna-to-PVC pipe connection is tight, spray both pieces with a silicon lubricant. If only one of the 2-foot mast sections is used, the center of gravity will be lower, thus improving the mounting stability. The base should be fastened or weighted to the roof for wind stability.

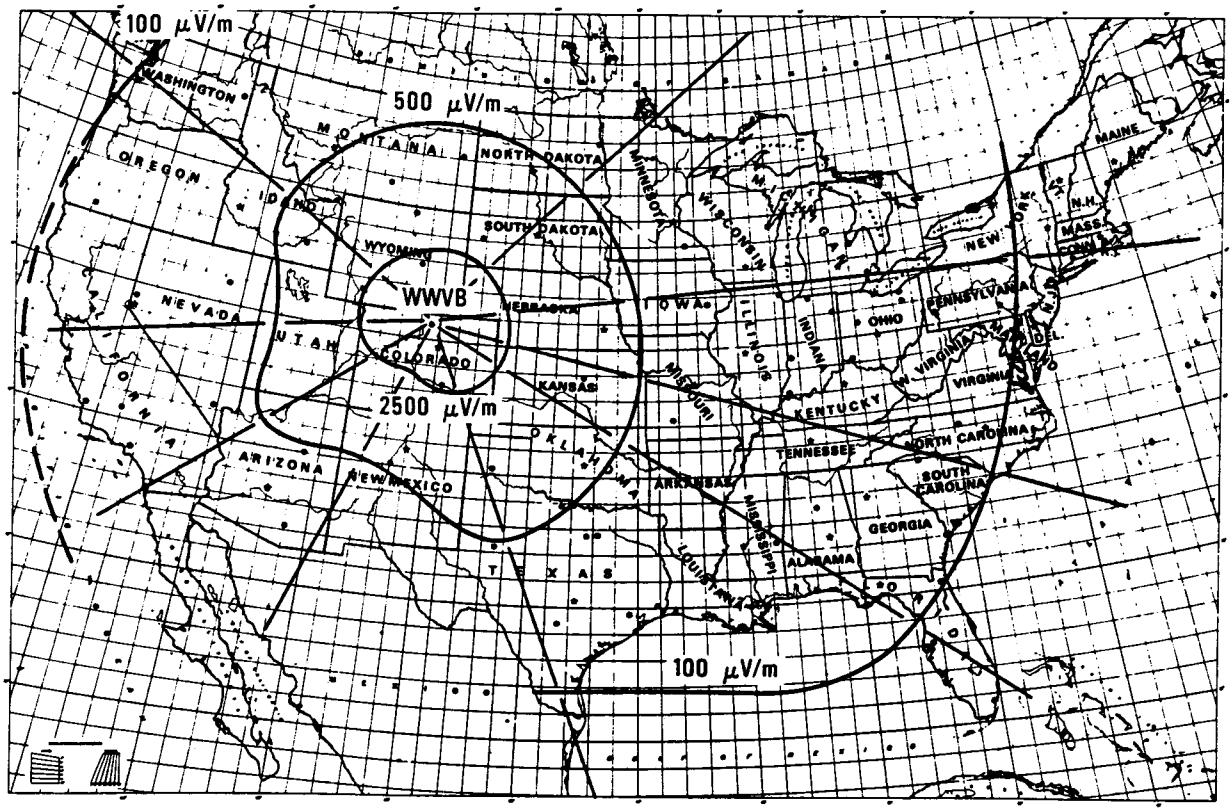


FIGURE 1-4 MEASURED FIELD INTENSITY CONTOURS WWVB @ 13 KW ERP

1.8 MODEL 8207 PREAMPLIFIER INSTALLATION

The Spectracom Model 8207 Preamplifier is a low noise, tuned, 60 kHz line amplifier used in the antenna feed line wherever the WWVB signal strength is less than 50 μV/meter at the Model 8206 Loop Antenna or less than 0.4 μV at the receiver antenna terminal. Typical locations where the preamplifier is probably required are Hawaii, Alaska, Puerto Rico, and the Canal Zone. Figure 1-4 shows the measured average signal strength for the contiguous 48 states. Atmospheric conditions may cause short term degradation of field intensity. The Model 8207 Preamplifier provides approximately 40 dB of gain between the antenna and receiver increasing sensitivity to 4.0 nanovolts.

The preamplifier is connected in the antenna feed line with INPUT connected

to the antenna and OUTPUT connected to the receiver. Because of the high gain of the system, it is recommended that the preamplifier be located at least 10 feet away from the receiver. The antenna must be least 25 feet beyond the preamplifier. Switch A1S1 of the receiver RF Amplifier must be set at its right-hand position, marked PREAMP or P, prior to equipment turn-on, to apply DC voltage to the Model 8207 on the antenna feed line. If the preamplifier is removed from the system, the switch must be placed in the left-hand position, marked ANT or A prior to turn-on.

1.9 BENCH OPERATION

The unit is equipped with 4 feet for standing on a benchtop surface, and a tilt bar for a convenient viewing angle.

1.10 RACK MOUNT OPTION 01

Units purchased with the rack mount kit are not provided with the tilt stand. The four mounting feet are included but these may be removed when the receiver is installed in a rack.

The rack mount panel extensions are installed by removing the vinyl-covered filler panels located just behind the handles on the sides of the enclosure. The rack mounting brackets are installed using the oval head #10-32 x 3/8 screws provided. Truss head #10-32 x 3/8 screws are furnished to mount the unit to the rack. (See Figure 1-5.)

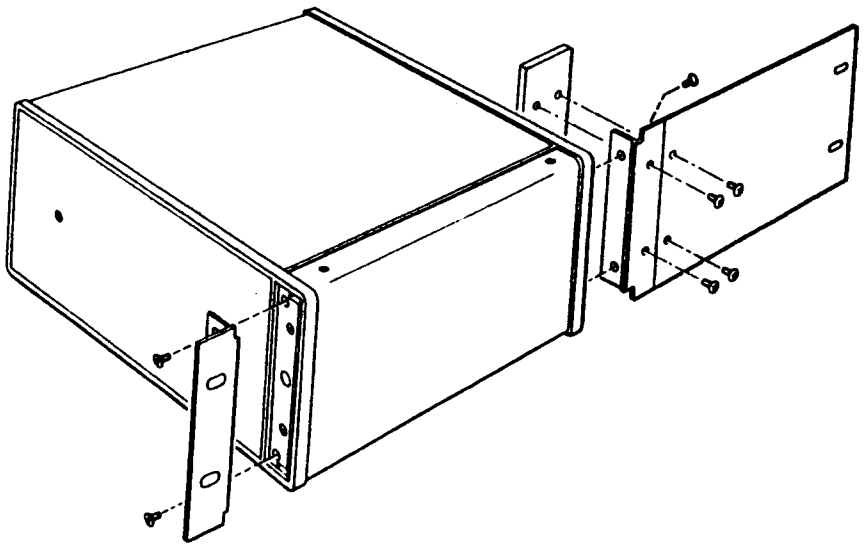


FIGURE 1-5 RACK MOUNT OPTION 01

1.11 RACK MOUNT WITH SLIDES OPTION 11

The chassis section of the slides are attached to the sides of the receiver using the #10-32 x 3/4 screws provided. The filler plates are located between the slides and the receiver sides.

The stationary section of each rack slide must be assembled to the proper length for the rack being used, using the brackets, screws, and nuts provided. The slides are bolted to the front and rear channels of the rack using the 10-32 x 1/2 screws and nut plates as shown in Figure 1-6. Additional panel mounting angles (such as Emcor No. PMA) may be added to the rack cabinet for securing the front ends of the stationary slide sections if needed. They should be located immediately behind the panel mounting angles to which the equipment panel extensions will be fastened.

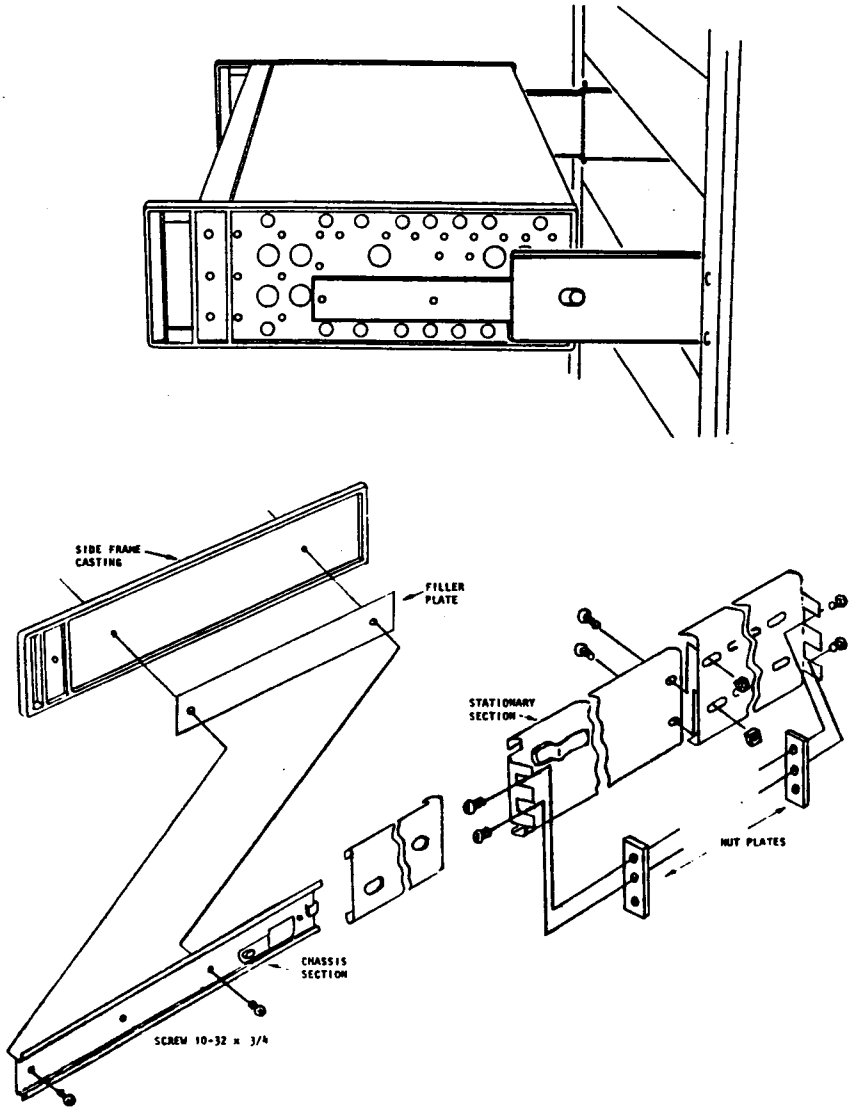


FIGURE 1-6 RACK MOUNT WITH SLIDES OPTION 11

1.12 PREPARATION FOR USE

1.12.1 LINE POWER

The line power switch and line fuse are factory selected for operation from a 115 VAC ±10%, 60 Hz power line.

Operation from a 230 VAC ±10%, 60 Hz power line requires switching the line power switch to 230 VAC position and substituting the line fuse to the corresponding value.

Plug the supplied line cord into the POWER connector and a properly grounded outlet of the selected voltage. The LINE INTERRUPT lamp will latch on indicating power to the unit has been interrupted and restored and the oscillator may require a warm-up period. Depress the RESET button to extinguish the lamp.

1.12.2 Battery Switch

Place the battery switch to the INT position on all units equipped with Option 34, SmartStart™, otherwise the switch may be left in the EXT position. The serial number tag will list the options installed in the unit.

Placing the battery switch to INT allows the Option 34 battery pack to be float charged and available as the oscillator standby power supply.

1.12.3 ANTENNA AND PREAMPLIFIER

Install the Model 8206 Antenna and the Model 8207 Preamplifier (if applicable) as outlined previously in this section.

1.12.4 INITIAL TURN ON

Depress the front panel power switch, the CPU lamp will briefly light then the UNLOCK and SIGNAL lamps will turn on. Once the receiver phase locks to WWVB the LOCK and GATE lamps latch on extinguishing the UNLOCK and SIGNAL lamps. The FREQ lamp will latch on at power up if the unit does not have Option 34, SmartStart™. The receiver will require a 3-4 synchronization period. During this period of time, the FREQ lamp may turn on in Option 34 units. This occurs when a valid frequency measurement is not within 1.0 E-8 of its expected frequency value. This condition is normal for cold oscillator start-ups. Option 34 units must depress the RESET button to clear the FREQ lamp, non-Option 34 units will self clear the FREQ lamp.

MODEL 8164

SECTION 2

OPERATION

2.0 INTRODUCTION

This section describes the front and rear panel functions, internal switches, and operational information for the Model 8164 WWVB Receiver-Disciplined Oscillator.

2.1 FRONT PANEL FAMILIARIZATION

Figure 2-1, Model 8164 Front Panel, and the following paragraphs describe the front panel functions.

2.1.1 FRONT PANEL CONTROLS

POWER ON/OFF - Depressing this button turns on and off the Model 8164.

> NOTE: Although the power switch may be in the OFF position, power is still applied to the oscillator assembly.

FREQUENCY - 0.1, 1.0, 5.0, 10.0. These switches select the frequency of operation associated with the NBS OUTPUT, LOCAL INPUT and front panel STANDARD OUTPUT.

RESET - This momentary contact pushbutton resets the latched alarm lamps.

RECORDER ON/OFF - This switch turns the strip chart recorder on and off. The meter movement will function in the OFF position providing the striker bar is not in contact with the meter needle.

RECORDER EXP - Depressing this pushbutton expands the meter/recorder scale to read 10 microseconds full scale. When the button is not depressed, the full scale reading is 50 microseconds. The 50 microsecond scale is the recommended setting for chart recordings.

RECORDER V - Depressing this pushbutton causes the strip chart recorder to display VCO lock voltage. The lock volts reading should be approximately center scale when phase locked to WWVB. Refer to Section 6.1 of this manual for additional information on lock volts.

When the pushbutton is not depressed. The strip chart recorder displays the resultant phase comparison of the internal oscillator or local input against WWVB.

COMPARATOR - This toggle switch selects the comparator input to be monitored and read out on the strip chart recorder. In the left position, the recorder monitors the phase relationship between the local input frequency and WWVB. In the right position, the internal frequency standard phase relationship is tracked by the recorder.

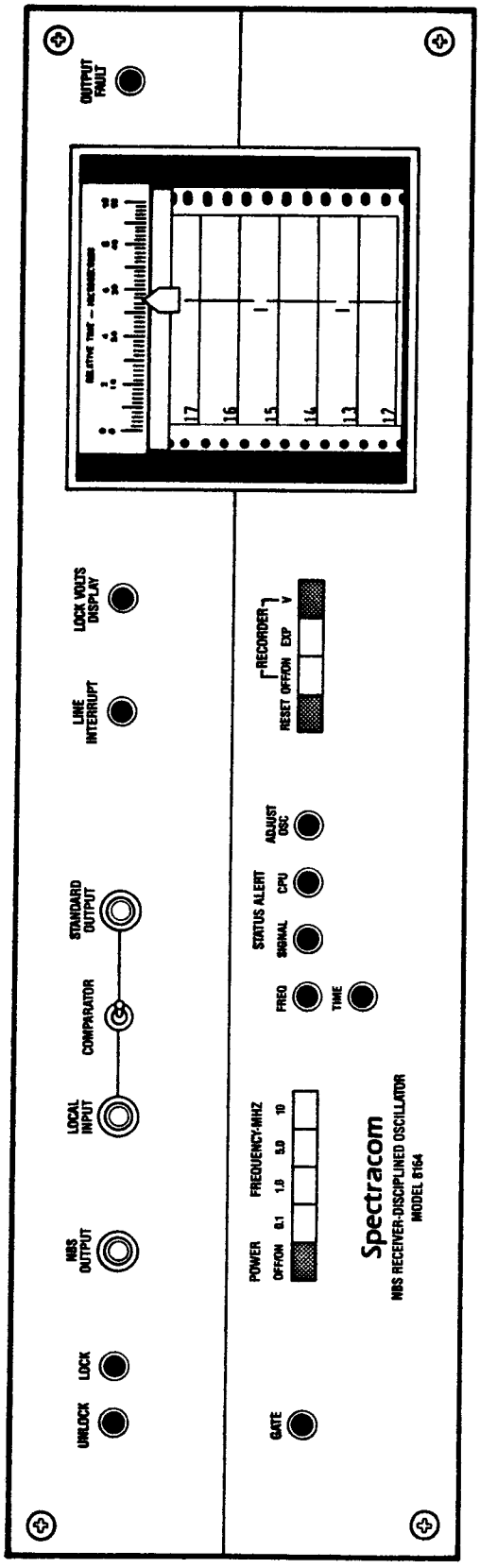


FIGURE 2-1 MODEL 8164 FRONT PANEL

2.1.2 FRONT PANEL DISPLAYS

UNLOCK - This lamp is lit when there is insufficient signal received for the receiver to lock to the WWVB carrier.

LOCK - This lamp is lit when the receiver is locked to WWVB.

LINE INTERRUPT - This lamp indicates that power to the unit has been interrupted and restored and the standard oscillator may require a warm-up period. A warm-up period is not required for units with Option 34. The lamp will remain lit until the RESET button is depressed.

LOCK VOLT DISPLAY - This lamp warns that the strip chart recorder is displaying VCO lock voltage NOT phase comparison.

OUTPUT FAULT - This lamp is latched on when a loss of signal is detected at the four rear panel STANDARD OUTPUTS. A signal loss may be caused by an external short or internal failure. Reflections from an unterminated line may cancel the signal at the rear panel, causing an output fault. The RESET switch turns the lamp off if the fault has been corrected.

GATE - This lamp indicates the gate interval over which the internal standard is measured against the phase locked reference. The gate period is 1000 seconds.

FREQ - This lamp is the frequency error alarm. The lamp is latched on if subsequent measurements are off by more than 1.0 E-8. Once the receiver resynchronizes to within 1.0 E-8 of the expected frequency, the alarm may be cleared by depressing the RESET button. This normally takes 3-4 hours under good signal conditions. This lamp is active if the internal switch A6U1-7 FREQ is switched ON.

SIGNAL - This lamp is the WWVB signal lamp. At power on the lamp is lit. The lamp is turned off when phase lock to the WWVB carrier is achieved. If phase lock with WWVB is lost for more than 10 hours, the lamp is latched on. The lamp is turned off by the front panel RESET switch.

CPU - The lamp is latched on if there is a microprocessor watchdog timer failure. The front panel RESET switch will turn this lamp off.

ADJUST OSC - This lamp is latched on if the 10 MHz standard oscillator requires adjustment of its coarse tuning control. Refer to the service information section of this manual for oscillator calibration procedures. The lamp is turned off by the front panel RESET switch.

TIME - This lamp is the time difference alarm. The lamp illuminates at power on. The lamp is turned off after the NBS 1 Hz and STD 1 Hz are time locked to the time code. If the time difference between NBS 1 Hz and STD 1 Hz exceeds 4 milliseconds, the alarm is latched on. The front panel RESET switch turns off this alarm. This lamp is active if the internal switch, A6U1-8 PHASE is switched ON.

STRIP CHART RECORDER - Displays phase comparison of internal oscillator or local input against WWVB. Selectable phase scales of 0-50 or 0-10 microseconds full scale relative time. May be switched to monitor receiver VCO lock voltage. Refer to Section 2.5 for chart recording examples.

The chart speed is factory set for 20 mm/hr, and may be changed to 10 mm/hr or 60 mm/hr by substituting the chart speed cam. The chart paper is scaled in hours for all three speeds of operation. Chart paper may be purchased from Spectracom. The part number for 10 rolls of chart paper is MP00025. A roll will last approximately one month with the 20 mm/hr chart speed. Refer to the strip chart recorder operator's manual for information on chart speed and paper changes.

2.1.3 FRONT PANEL INTERFACE

NBS OUTPUT - This BNC connector provides an output signal that is phase locked to the Bureau of Standards signal whenever the phase lock lamp is lit. The output frequency is selected by means of the Frequency-MHz switches described previously. The output impedance is 100 ohms. The open circuit output low level voltage is less than 0.5 volts and the high level voltage is typically 3.4 volts. The signal is TTL compatible into loads greater than 120 ohms. Refer to paragraph 2.4 for detailed information of the NBS OUTPUT.

LOCAL INPUT - The BNC connector is the input jack for local oscillators to be calibrated or tracked against WWVB. The input frequency must be the same as that chosen by the Frequency-MHz switch. The LOCAL INPUT connector accepts signals between 100 mV rms and 3.5 V rms and has an input impedance of 50 ohms. The use of this connector is described in Section 2.6, Using the Phase Comparator.

STANDARD OUTPUT - This BNC connector outputs frequencies derived from the internal standard oscillator. The output frequency is selected with the Frequency-MHz switches. The output impedance is 100 ohms. The open circuit output low level voltage is less than 0.5 volts and the high level voltage is typically 3.4 volts. The signal is TTL compatible into loads greater than 120 ohms.

2.2 REAR PANEL FAMILIARIZATION

Figure 2.2, Model 8164 Rear Panel, and the following paragraphs describe the rear panel functions.

2.2.1 REAR PANEL FUSES

BATTERY FUSE - This fuse protects the oscillator power supply. Replace with AGC 3/8 A, 250 V.

LINE FUSE - This is the main power fuse for the unit. The receiver is shipped from the factory for operation at 115 VAC. If the unit is to be operated at 230 VAC, this fuse must be changed to the value listed by the 115 VAC/230 VAC switch.

2.2.2 REAR PANEL SWITCHES

115 VAC/230 VAC - The Model 8164 may be operated from either 115 VAC ±10% or 230 VAC ±10%. Move this switch to the corresponding line voltage available.

BATTERY INT/EXT - This switch selects the source of the oscillator standby supply. The standby supply powers the standard oscillator whenever AC power is lost. This avoids settling and retrace problems when the AC power returns.

When this switch is in the INT position an internal battery pack is selected as the standby supply. The batteries are continuously float-charged whenever line power is connected to the unit. The battery pack contains sealed lead-acid cells that require no maintenance. The battery pack provides a minimum of 36 hours of standby operation and is included with Option 34, Smart Start.

> NOTE: Option 34 Units.
>
> The internal battery has been disconnected for shipment by placing this switch in the EXT position. To reconnect the battery, return the switch to the INT position.

If the unit will be disconnected from AC power for more than 36 hours or if the unit is returned to the factory for repair, place the switch in the EXT position.

In the EXT position the switch selects an external battery as a standby supply. The external battery connections are made at the rear panel AUX IN/OUT connector. See PIN 3 of the AUX IN/OUT connector description for battery recommendations.

2.2.3 REAR PANEL INTERFACE

STANDARD OUTPUTS - These BNC connectors output the internal standard oscillator at frequencies of 0.1, 1.0, 5.0 and 10.0 . The output signals are 600 mV rms sine waves into a 50 ohm load. The harmonic suppression is 30 dB. When used without termination, the output is TTL compatible.

Units equipped with Option 03, Built in Distribution Amplifier, output the standard 10 MHz on a 12 VDC offset. These outputs are used to drive Spectracom Frequency Distribution Taps. Refer to the Option section of this manual for Option 03 information.

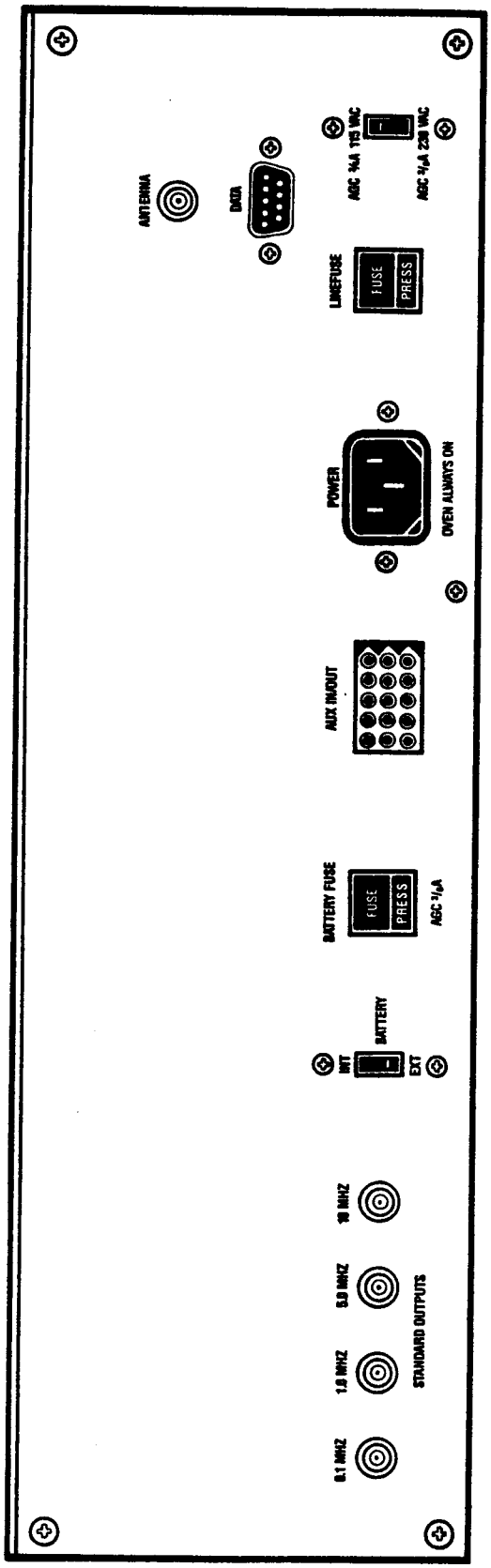


FIGURE 2-2 MODEL 8164 REAR PANEL

AUX IN/OUT - Auxiliary and Remote functions of the receiver are available at this 15 pin connector. Use Figure 2-3, AUX IN/OUT CONNECTOR, to locate the pins.

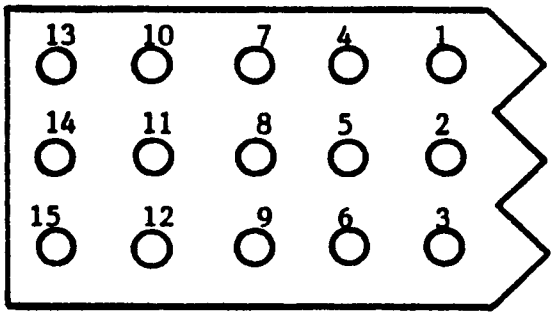


FIGURE 2-3 AUX IN/OUT CONNECTOR

PIN 1 - MINOR ALARM OUTPUT - This is the non-inverted RS-422 alarm output. This signal is positive relative to PIN 2, MINOR Alarm Output when an alarm is asserted. An alarm is asserted whenever a STATUS ALERT lamp or OUTPUT FAULT lamp indicates a failure. The signal returns to normal when the alarm condition is corrected.

PIN 2 - MINOR ALARM OUTPUT - This is the inverted RS-422 alarm output. This signal is negative relative to PIN 1, MINOR Alarm Output when an alarm is asserted as described above. The external cable for PINs 1 and 2 should be twisted pair terminated into 120 ohms.

PIN 3 - EXTERNAL BATTERY INPUT - For continuous oven and oscillator operation in the event of power failure, an external battery can be connected here. The battery will be float-charged whenever line power is on. The maximum charge rate is 250 mA. Recommended battery type is sealed lead-acid, 24 VDC, 1-2 A-H or greater capacity. The BATTERY switch must be in the EXT position.

PIN 4 - TIME CODE AND PHASE LOCK OUTPUT GROUND - This ground pin is used in the 8171A interconnection cable.

PIN 5 - PHASE LOCK OUTPUT - Used for monitoring of receiver phase lock status. This pin will be ground when the unit is unlocked, and +5 VDC behind 3.3K ohms when the unit is locked. This pin is used in the 8171A interconnection cable.

PIN 6 - EXTERNAL BATTERY INPUT GROUND - This pin is tied to chassis ground, used for external battery ground.

PIN 7 - TIME CODE OUTPUT - The time code modulation on the WWVB carrier is synchronously detected and brought out on this pin. Logic high is +5V behind 3.3K ohms, logic low is ground. This pin is used in the 8171A interconnection cable.

PIN 8 - MAJOR ALARM OUTPUT - This is the non-inverted RS-422 alarm output. This lead is positive relative to PIN 9 when the function is asserted. The function is asserted whenever a STATUS ALERT lamp or OUTPUT FAULT lamp indicates a failure. The signal returns to normal when the alarm condition is corrected.

PIN 9 - MAJOR ALARM OUTPUT - This is the inverted RS-422 alarm output. This lead is negative relative to PIN 8 when the front panel STATUS ALERT lamp or OUTPUT FAULT lamp indicates a failure. The signal returns to normal when the alarm condition is corrected. The external cable for PIN 8 and PIN 9 should be twisted pair and terminated into 120 ohms.

PIN 10 - MAJOR ALARM GROUND - The external cable for PIN 8 and PIN 9 should be a twisted pair. This ground is reserved for the ground shield of this cable.

PIN 11 - 10 MHz STD - This is the non-inverted lead from an RS-422 driver. This signal is the processor-controlled 10 MHz quartz crystal oscillator.

PIN 12 - 10 MHz STD - This is the inverted lead from an RS-422 driver. This signal is the processor-controlled 10 MHz quartz crystal oscillator. The external cable for PIN 12 and PIN 11 should be a twisted pair and terminated into 120 ohms. PIN 15 is reserved for the cable shield.

PIN 13 - 10 MHz PHASE LOCKED OUTPUT - This TTL compatible 10 MHz signal is phase locked to WWVB. The signal is used in the 8171A interconnection cable.

PIN 14 - 10 MHz PHASE LOCKED OUTPUT GROUND.- This pin provides the cable shield ground for the 10 MHz phase locked output.

PIN 15 - 10 MHz STANDARD GROUND - This pin is the cable shield for the RS-422 10 MHz signal.

MATING CONNECTOR - The mating connector and pins are found in the Model 8164 Ancillary Kit. Replacements may be purchased through Spectracom Corporation or a MOLEX Distributor.

DESCRIPTION	SPECTRACOM P/N	MFG. AND P/N
15 Pin Plug	P01115	MOLEX 03-09-2151
Socket Pins	P01100	MOLEX 02-09-2118

The crimping tools for the pins is MOLEX 11-01-0002. The extractor tool is MOLEX 11-03-0006. There is no insertion tool required.

POWER - This is the input power connector for the detachable line cord. The chassis is earth grounded to protect against electrical shock.

ANTENNA - This BNC connector is the antenna input to the receiver. The antenna also receives DC power from this connector.

DATA - This connector is Series D, 9-pin receptacle. The pin locations are shown in Figure 2-4. The serial channel transmits/receives an asynchronous frame that consists of a start bit, 7 data bits, a mark bit, and a stop bit. Baud rate is dip switch selectable. Table 2-1 lists baud rates and the corresponding switch settings. Refer to Section 2.9 for receiver printouts and commands.

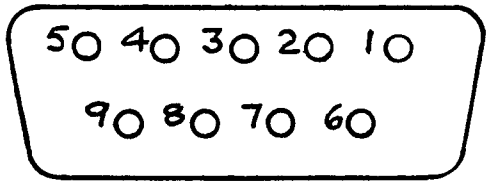


FIGURE 2-4 DATA CONNECTOR

PIN 4 SERIN - This is an RS-232C signal. Serial ASCII characters are input via this pin.

PIN 5 SEROUT - This is an RS-232C signal. Serial ASCII characters are output via this pin.

PIN 7 ON-TIME - This is a TTL-compatible 1-Hz square wave is derived from the standard 10 MHz oscillator.

PIN 9 GND - Signal ground

2.3 INTERNAL SWITCHES

2.3.1 ANT/PREAMP

This switch is found on the A1 RF Amplifier Board. This switch should be in the "A" position unless a Model 8207 In-Line Preamplifier has been installed. Then the switch must be placed in the "P" position to allow extra power to drive the antenna and preamp combination.

2.3.2 DIP SWITCHES

There are two 8-position DIP switches located on the A6 FTC Board.

The internal switches are set as indicated below when the unit is shipped from the factory:

A6U1-1	Spare	OFF	A6U18-1	Auto Reset	OFF
U1-2	DA One	OFF	U18-2	Spare C4	OFF
U1-3	DA Zero	OFF	U18-3	Spare C3	OFF
U1-4	GATE-10	OFF	U18-4	Spare C2	OFF
U1-5	Lamp	OFF	U18-5	Spare C1	OFF
U1-6	Test	OFF	U18-6	Baud 2	ON
U1-7	Freq	ON	U18-7	Baud 1	ON
U1-8	Phase	OFF	U18-8	Baud 0	OFF

2.3.3 SWITCH A6U1

Plus or Minus Offset - Spare A6U1-1: This switch controls the direction of the frequency offset selected. The offset is positive when the switch is ON and negative when OFF. This switch is used with the optional frequency offset function.

Minimum Frequency - DA ONE A6U1-2: When the TEST switch is ON and DA ONE switch is ON the output of the D/A converter is all 1's. This adjusts the 10 MHz standard to its minimum value. Used during the frequency range adjustment procedure.

Maximum Frequency - DA ZERO A6U1-3: When the TEST switch is on and DA Zero switch in ON the output of the D/A converter is all zeros. This adjusts the 10 MHz standard to its maximum value and is used during the course frequency adjustment procedure.

10-Second Measurement Gate - GATE10 A6U1-4: With the TEST switch ON and the GATE10 switch ON, the measurement gate time is changed from 1000 seconds to 10 seconds. This switch is used during the frequency adjustment procedure of the 10 MHz standard oscillator.

Lamp Test - LAMP A6U1-5: With the TEST switch ON the Lamp Test switch will turn on the alarm lamps.

Enable Test Switch - TEST A6U1-6: This switch in the ON position enables test switches U1-2 through U1-5. For normal operation it should be placed in the OFF position.

Enable Frequency Correction - FREQ A6U1-7: When this switch is in the ON position, the 10 MHz standard oscillator is automatically kept on frequency.

Enable Phase Correction - PHASE A6U1-8: When this switch is ON the accumulated time error of the standard 10 MHz oscillator is measured by comparing the oscillator output with the received time code. As time error accumulates, small corrections slew the oscillator to make up for lost or gained time. This function is typically not used with the Model 8164 and should be left in the OFF position.

2.3.4 SWITCH A6U18

Auto Reset A6U18-1: Not used on the Model 8164. Place this switch in the OFF position.

Spare C4, Spare C3, Spare C2, Spare C1 - A6U18-2,3,4,5: These switches enter the binary equivalent of the frequency offset channel selected. If no offset of the 10 MHz output is required, turn these switches to the OFF position. The switches are only used with a frequency offset option. Refer to the Option section of this manual.

Baud 2, Baud 1, Baud 0 - A6U18-6,7,8: These switches select the baud rate in/out of the DATA connector on the rear panel. The bit rate switch coding is shown in Table 2-1, BIT RATE.

Baud	A6U18-6 Baud 2	-7 Baud 1	-8 Baud 0
SPARE	1	1	1
300	1	1	0
600	1	0	1
1200	1	0	0
2400	0	1	1
4800	0	1	0
9600	0	0	1
SPARE	0	0	0

TABLE 2-1 BIT RATE

NOTE: The spare switch positions will cause the baud rate to be set to 300.

2.4 NBS OUTPUT

The frequency of the NBS output signal is selected by depressing one of the FREQUENCY- MHz switches located on the front panel. The output frequency obtained by pressing a button is phase locked to the WWVB 60 kHz carrier. This output frequency can be used as a standard for checking the accuracy of frequency counters, or used as a standard frequency signal. Note that noise will be present in the form of pulse jitter due to atmospheric noise at the receiver antenna. The counting error caused by this noise is usually not more than ±1.0 E-7 in a one-second averaging period. Longer averaging periods will decrease the effect of the jitter. The long term accuracy of this signal is as good as that of the WWVB carrier signal to which it is phase locked.

2.5 WWVB IDENTIFICATION AND SAMPLE CHART RECORDINGS

WWVB identifies itself by advancing the carrier phase by 45° at 10 minutes past the hour and returning to nominal at 15 past the hour. Figure 2-5 shows the 2.1 microsecond hourly offsets. These offsets provide instant verification of traceability to the National Bureau of Standards.

The following examples are typical strip chart recordings showing initial turn on, diurnal shift, sun flares and noisy reception. All strip chart recordings were made at 20 mm/hr paper speed and 50 microseconds full scale.

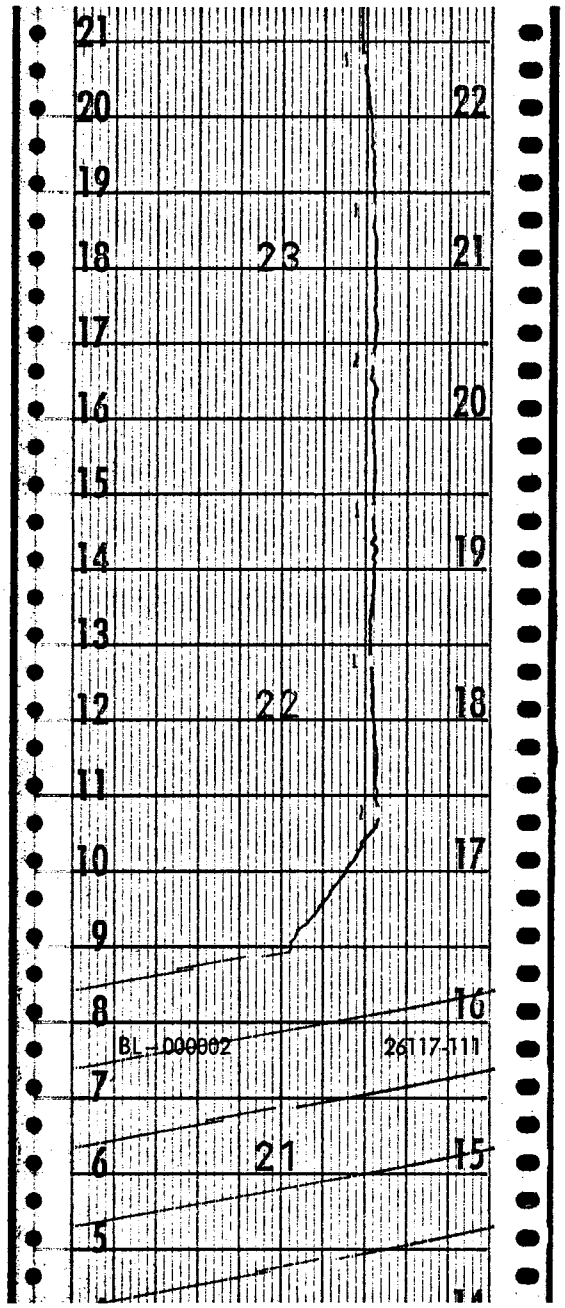


FIGURE 2-5 INITIAL START-UP AND WWVB IDENTIFICATION

At power-on, the chart recording will look like the lower portion of Figure 2-5. The internal frequency standard is measured and then brought on frequency by the microprocessor. This process typically takes 3-4 hours under good signal conditions. Option 34, SmartStart eliminates the re-synchronization period at power-on.

The received WWVB signal is affected by changes in the propagation path. These changes appear as phase shifts on the strip chart recorder. The diurnal effect is caused by the ionosphere lowering at sunrise and rising at sunset. The lowering ionosphere shortens the propagation path causing the received phase to advance. The rising ionosphere lengthens the propagation path delaying the received signal. An example of diurnal shifts is shown in Figure 2-6.

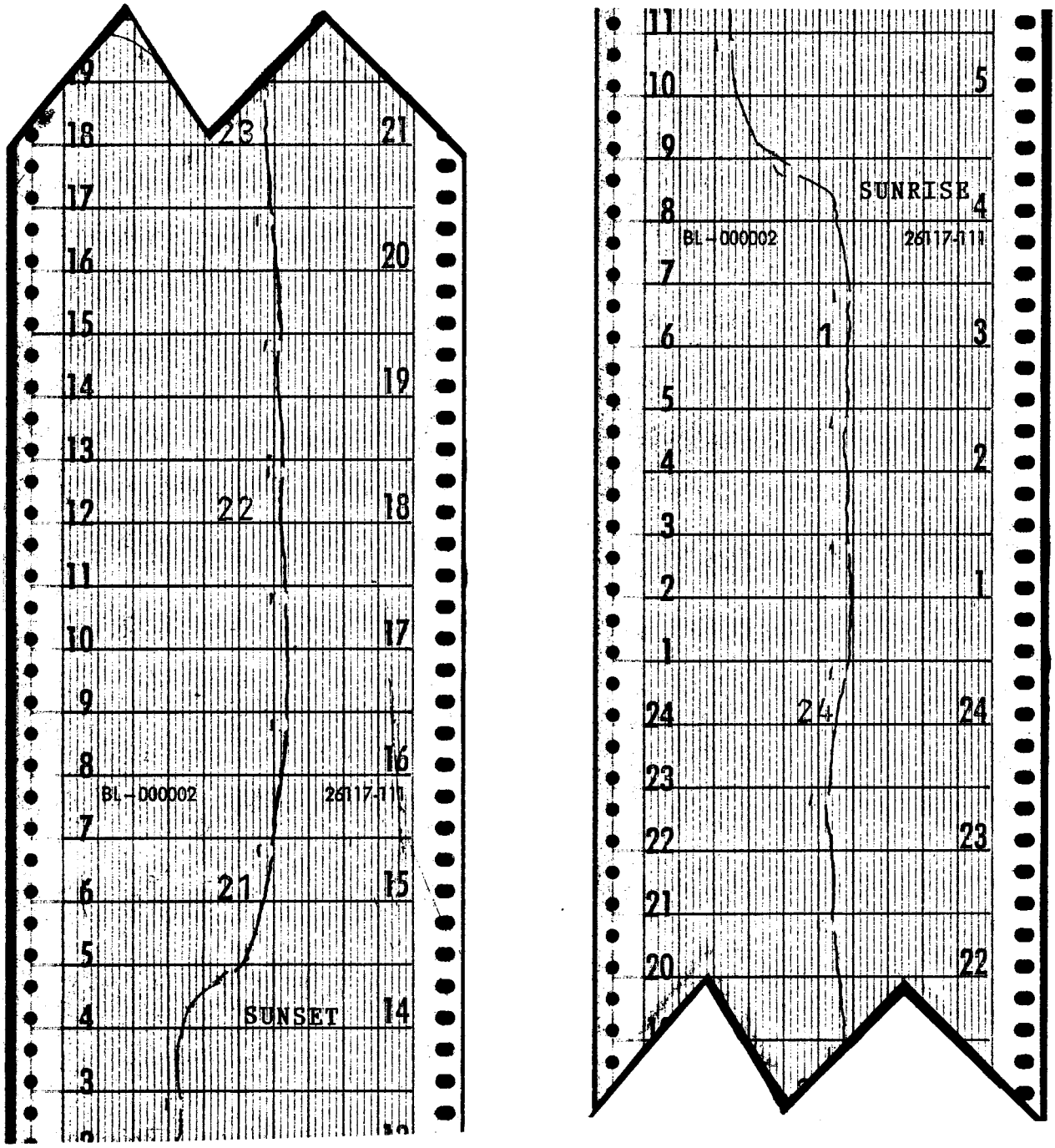


FIGURE 2-6 DIURNAL SHIFTS

Figure 2-7 was made on a day with frequent sun flares. Figure 2-8 was made on a noisy day. The signal was degraded enough to cause the receiver to unlock.

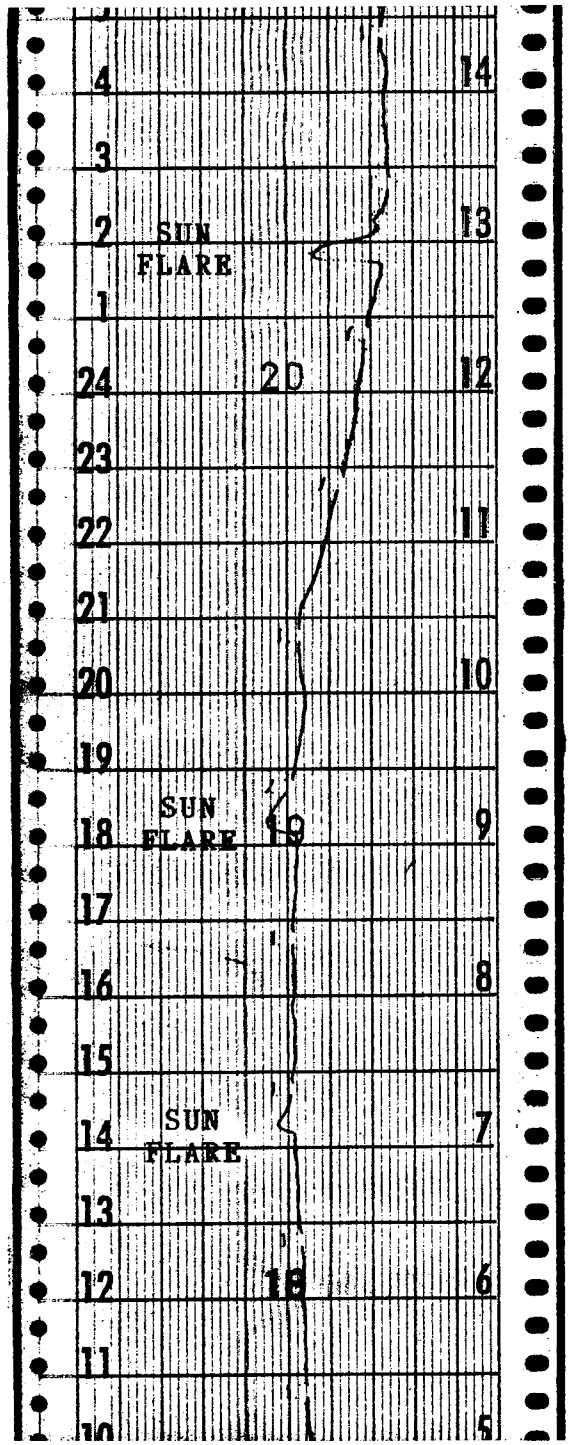


FIGURE 2-7 SUN FLARES

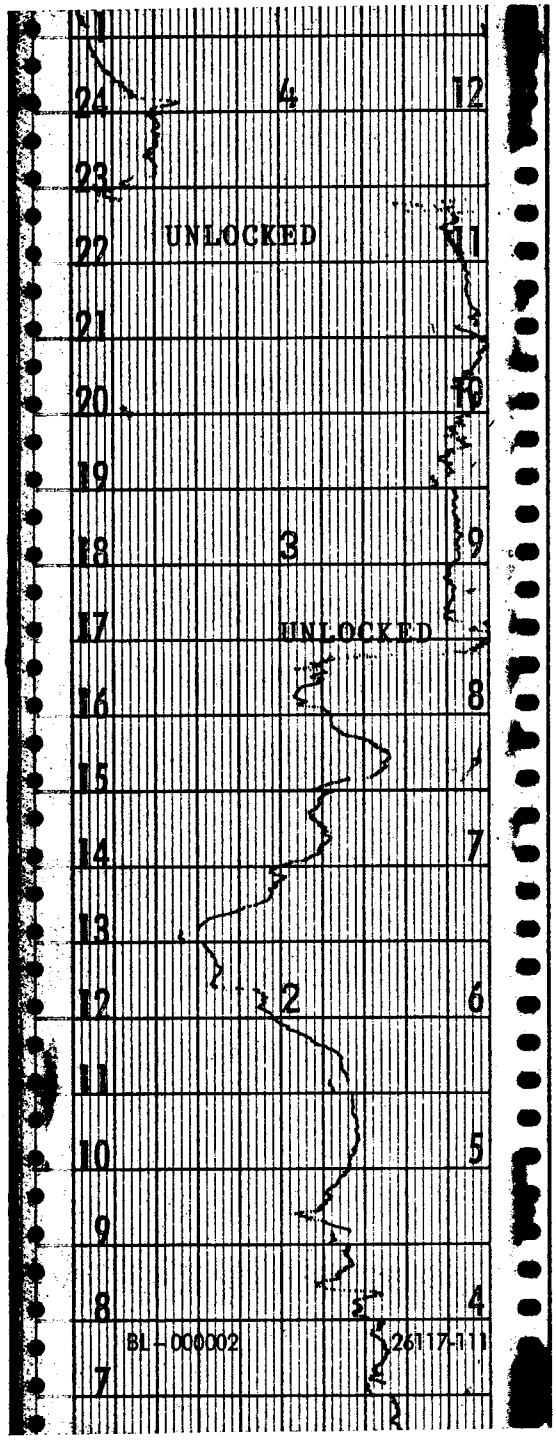


FIGURE 2-8 NOISY TRACE

2.6 USING THE PHASE COMPARATOR

2.6.1 LOCAL INPUT

Connect the signal that you wish to calibrate to the LOCAL INPUT connector. Move the comparator toggle switch to the left hand position. This allows the local input to be compared against the NBS reference. Depress the corresponding frequency selection switch.

The front panel meter displays the relative phase difference between the two signals. The meter will move to the right whenever the local input is higher in frequency than the NBS reference, and to the left whenever it is lower in frequency.

When the meter needle reaches one end of the scale, it will return to the opposite end of the scale and begin again its travel in the same direction. The rate at which the meter moves is proportional to the rate of phase change or frequency error between the two signals.

The relative frequency error, F, may be determined from the formula:

$$F = \frac{\Delta t}{T}$$

where: Δt = amount of phase change between the signal express in seconds.

T = time interval in seconds over which the phase change measurement occurred.

For example, if it takes 50 seconds for the meter to deflect full scale (50 microseconds), then the frequency error of the local signal is:

$$\text{Relative Frequency Error} = \frac{50 \times 10^{-6} \text{ (seconds)}}{50 \text{ (seconds)}}$$

$$\text{Relative Frequency Error} = 1.0 \text{ E-6}$$

The full scale setting may be changed from 50 microseconds to 10 microseconds by depressing the recorder EXP switch. Use the 10 microsecond scale to adjust the local oscillator until the meter stops moving, then return to the 50 microsecond scale to record the phase comparison. The 10 microsecond scale setting is not recommended for recording because phase shifts and received noise makes chart recording interpretation difficult.

2.6.2 ERROR CALCULATION FROM A CHART RECORDING

The chart recorder provides a permanent record of the phase comparison between WWVB and the internal oscillator or local input. Calibrations using a chart recorder approach resolutions of 1.0 E-11 in a 24 hour period. Without a chart recorder, phase shifts due to the diurnals or other propagation path changes may be incorrectly interpreted as changes in oscillator frequency, thus reducing the accuracy of the calibration. The best phase tracking results are obtained when the signal path from the transmitter and the receiver is in all daylight.

Figure 2-9 is the resultant phase comparison between WWVB and a local input. The relative frequency error is determined by dividing the phase movement expressed in seconds by the time in seconds over which the movement occurred.

$$\text{Relative Frequency Error} = F = \frac{\text{Phase Change (seconds)}}{\text{Time Interval (seconds)}} = \frac{\Delta t}{T}$$

From the example in Figure 2-9, over a 1 hour period an 11 microsecond phase change occurred. The relative frequency error is:

$$\text{Relative Frequency Error} = \frac{11 \times 10^{-6} \text{ seconds}}{1 \text{ hr.} \times 3600 \frac{\text{seconds}}{\text{hour}}} = 3.1 \times 10^{-9}$$

In this example, the local input is high in frequency by 3.1 E-9.

The measurement interval can be determined from the WWVB hourly offsets or using the appropriate hour scale on the chart paper. Figure 2-10, "Error Calculation Chart" can be used to find frequency error as a function of phase change and time.

Chart Speed Scales
10 mm/hr 60 mm/hr 20 mm/hr

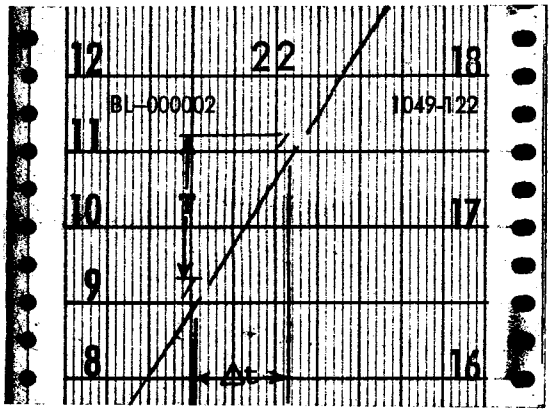


Figure 2-9 is the resultant phase comparison of a local input against WWVB. The left to right slope indicates the local input is higher in frequency than the received WWVB reference.

Full Scale = 50 microseconds
Chart Speed = 20 mm/hr
Measurement Interval = 1 Hr.
Phase Change = 11 microseconds

FIGURE 2-9 PHASE COMPARISON

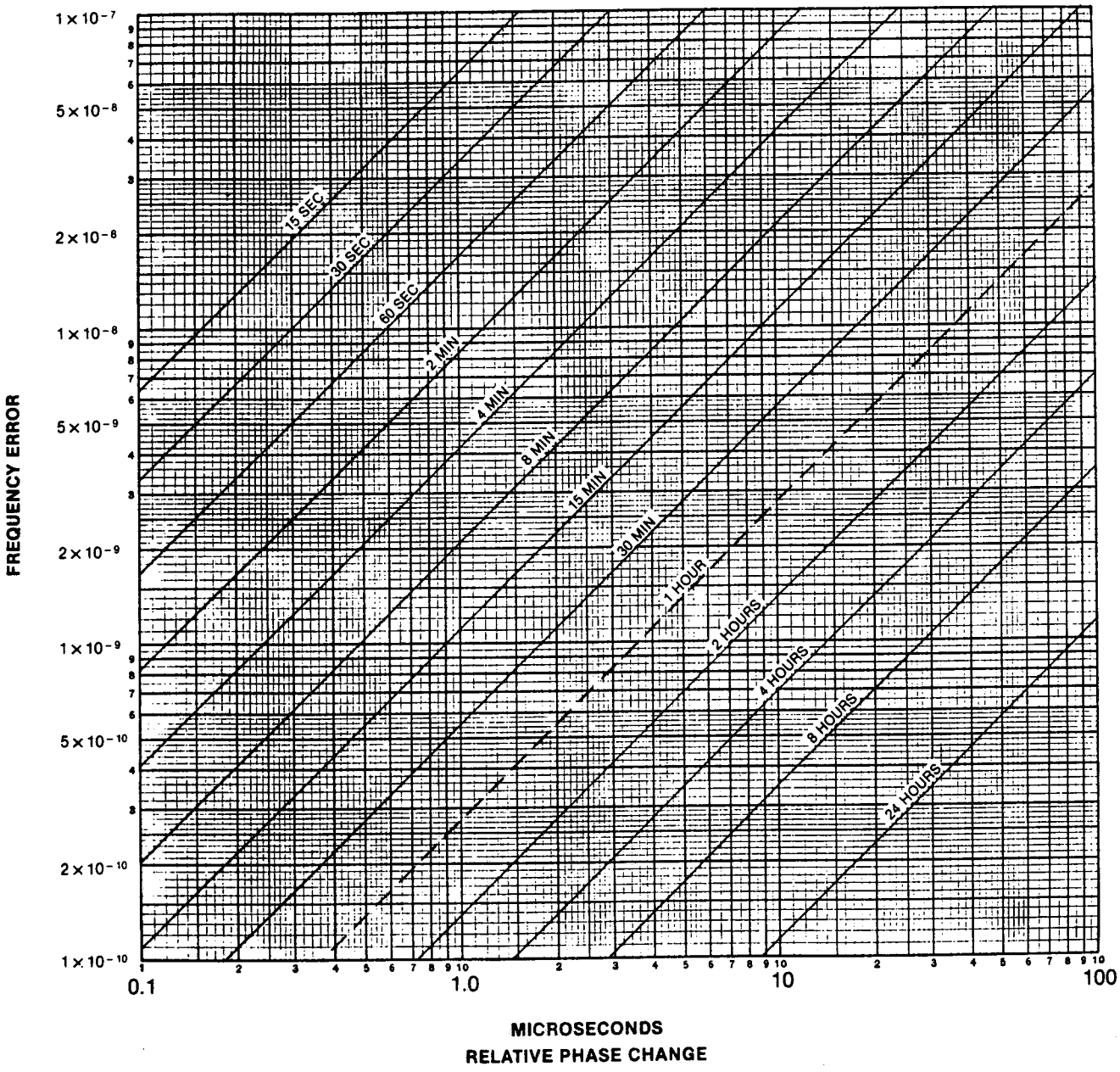


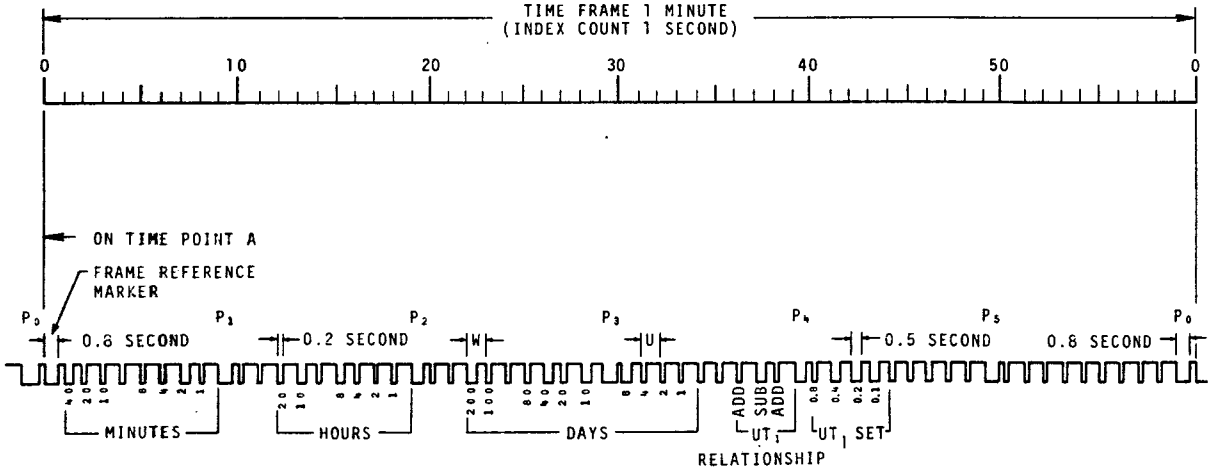
FIGURE 2-10 ERROR CALCULATION CHART

2.7 TIME CODE OUTPUTS

Time code modulation is provided on the WWVB carrier for use in synchronizing accurate clocks and other time-keeping equipment. The modulation consists of once-per-second pulsed amplitude reductions of 10 dB, lasting either 200, 500, or 800 milliseconds. Decoding a one minute data stream yields date, time of day, and a correction factor for converting from atomic time (Coordinated Universal Time or UTC) to celestial time (UT1). (See Figure 2-11)

Atmospheric noise levels at 60 kHz are frequently very bad, and will sometimes cause false pulses to appear on the demodulated time code output. The noise levels are extremely variable, depending on factors such as season, time of day and geographical location. Noise is lower in the northern latitudes during winter daytime hours, and higher at night during the summer in southern latitudes. In U.S. coastal areas, where the WWVB signal strength is nominally 100 μV per meter, the signal-to-noise ratio may be as bad as -23 dB in a 1-kHz bandwidth. The Spectracom receiver, due to its unique synchronous detector with extremely narrow bandwidth, will stay phase locked to the WWVB carrier with signal-to-noise ratios as poor as -35 dB. Time code errors will occur on bad days, however, and error detection techniques such as those used in Spectracom's Model 8171 Synchronized Clock are necessary if the output data is to be useful.

The 10 dB reduction of the WWVB carrier is inverted in the demodulation process and appears at the output as a positive-going TTL-compatible pulse. The signal is available at PIN 7 of the AUX IN/OUT connector (J8) on the rear panel, and may be used to synchronize the Model 8171 Synchronized Clock.



BINARY CODED DECIMAL TIME-OF-YEAR CODE WORD (23 DIGITS)
CONTROL FUNCTIONS (15 DIGITS) USED FOR UT_1 CORRECTIONS
6 PPM POSITION IDENTIFIER MARKERS AND PULSES (P_0 THRU P_5)
(REDUCED CARRIER 0.8 SECOND DURATION PLUS 0.2 SECOND DURATION PULSE)
W - WEIGHTED CODE DIGIT (CARRIER RESTORED IN 0.5 SECOND - BINARY ONE)
U - UNWEIGHTED CODE DIGIT (CARRIER RESTORED IN 0.2 SECOND - BINARY ZERO)

NOTE: BEGINNING OF PULSE IS REPRESENTED BY NEGATIVE - GOING EDGE.

UTC AT POINT A	UT1 AT POINT A
258 DAYS	258 DAYS
18 HOURS	18 HOURS
42 MINUTES	41 MINUTES
	59.3 SECONDS

FIGURE 2-11 WWVB TIME CODE FORMAT

2.8 SIGNAL STRENGTH

The Spectracom receiver may be used to measure relative field strength of the 60 kHz signal. This measurement may be used to optimize reception by indicating the best location and orientation of the antenna.

The WWVB receiver employs synchronous AGC which responds to the 60-kHz signal only and is not affected by noise. The AGC level, therefore, provides an excellent indication of signal strength.

To measure this AGC voltage, open the cover of the receiver and locate test points TP3 and TP6 on the Receiver board A2. Place the positive lead of a DC voltmeter on TP6 (blue) and the negative lead on TP3 (orange). The voltage will be approximately 2.0 VDC at a field strength of 100 μV/meter using a properly oriented Model 8206 Loop Antenna. The AGC voltage will increase in strong signal locations, rising to a limiting value of approximately +3.6 volts as the front end input increases.

As the signal strength decreases to the receiver phase lock threshold of about 0.2 μV, the AGC voltage decreases to about +1.0 VDC. The red UNLOCK panel lamp will light below this level. The AGC voltage will decrease to a varying level around zero if the input signal is removed completely. As the signal is re-applied and increased, the receiver will again lock at an AGC level of approximately 1.0 volt.

The relative signal strength measurement may be used to aid antenna orientation by placing the antenna so as to maximize the AGC voltage measurement. The circuit that develops the AGC voltage has a very long time constant, so that a pause of 30 to 60 seconds is necessary after each move of the antenna to allow the AGC to stabilize at the new level. A few minutes of experimentation should produce optimum antenna orientation.

2.9 RECEIVER PRINTOUTS AND COMMANDS

The FTC will print out a number of different records reflecting its status and monitored results. These records include:

Time Lock Step Record
Frequency Measurement Record
Valid Frequency Measurement Record
Restart Record
D/A Set Record

Examples of each of these records shown and explained below. All numeric values in the records are in hexadecimal.

2.9.1 TIME LOCK STEP RECORD

Time Lock Step Records are preceded by an -> and is not pertinent to the Model 8164 operation.

2.9.2 FREQUENCY MEASUREMENT RECORD

```
**TIME=794157 FREQ=0002540BE403 DA=05BB SHIGH=01 PHASE=0052 GOOD=03BA LO/HI=FFF8
**TIME=794540 FREQ=0002540BE3FD DA=05BB SHIGH=01 PHASE=0052 GOOD=0103 LO/HI=FFED
```

Frequency Measurement Records are generated at the end of each frequency measurement gate period. Except for testing, the gate period is 1000 seconds. SHIGH, PHASE, GOOD and LO/HI are parameters used in the Time Lock process and are not applicable to the Model 8164. TIME, FREQ and DA are explained below:

TIME — This is the time in seconds since power on.

FREQ — This is the actual Frequency Count in hexadecimal for the gate period. A perfect count for 1000 seconds would read: 0002540BE400.

DA — This is the current D/A value at the time of the record.

2.9.3 VALID FREQUENCY MEASUREMENT RECORD

```
DA_ADJ=0682 FREQ_ADJ=0682 INDX=03 LOST_LOCK=0033
AVGERR=00000000000F LAST=05BB ADJ=0006 CURR=05C1
```

Valid Frequency Measurement Records are generated each time three Frequency Measurement Records have been generated and when three of the last three or four records indicate frequency counts which agree within 10 counts of each other (1.0 E-9).

DA-ADJ — This is the D/A Adjustment Count. This counter counts the number of times that the D/A has been adjusted since power up. The D/A is adjusted when Valid Frequency Measurements are made.

FREQ-ADJ — This is the Frequency Adjust Count. This counter counts the number of Valid Frequency Measurements since power up.

INDX — This is the last index used in the circular table of four frequency measurements.

LOST-LOCK — This is the Lost Lock Count. This counter counts the number of times that the WWVB receiver has lost lock since power up.

AVGERR — This is the Average Error of the three frequency counts used in the Valid Frequency Measurement relative to a perfect count.

LAST This is the current D/A value.

ADJ This is the D/A Adjustment Value. This is the computed magnitude of the adjustment which should be applied to the current D/A value to correct for the Average Error. If the error is positive, this value will be added to the current D/A value, else it will be subtracted.

CURR This is the new D/A value which will be used.

2.9.4 RESTART RECORD COMMAND

RESTART AT 000016

Restart Records are generated any time an "R" is typed at the terminal. Current frequency counting is aborted and restarted. The record indicates the time at which the gate period was restarted.

2.9.5 D/A SET RECORD COMMAND

D/A SET TO 04C0 AT 000014

D/A Set Records are generated any time the D/A is manually set.To set the D/A, a "D" is typed at the terminal. The value that the D/A is set "to" is shown as well as the time "at" which it was set.

2.9.6 LOG RECORD COMMAND

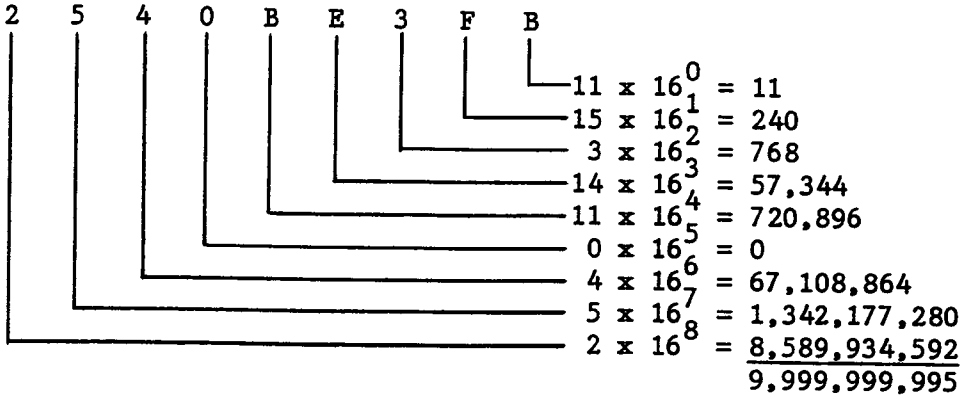
A complete log of receiver functions is printed when "L" is typed into the terminal.

2.9.7 FREQUENCY CONVERSION TABLE

FREQ. (DECIMAL)	FREQ. COUNT (HEX) (GATE=10)	FREQ. COUNT (HEX) (GATE=1000)
10,000,002.500	000005F5E119	0002540BEDC4
10,000,000.100	000005F5E101	0002540BE464
10,000,000.050	000005F5E100	0002540BE432
10,000,000.010	000005F5E100	0002540BE40A
10,000,000.000	000005F5E100	0002540BE400
9,999,999.990	000005F5E100	0002540BE3F6
9,999,999,950	000005F5E100	0002540BE3CE
9,999,999,900	000005F5E0FF	0002540BE39C
9,999,992.50	000005F5E0B5	0002540BC6B4

2.9.8 HEXADECIMAL TO DECIMAL CONVERSION

EXAMPLE: Find the output frequency in hertz from a printout frequency measurement of 0002540BE3FB .



Divide the total number of cycles counted by the 1000 second gate period to solve for the output frequency.

$$\frac{9,999,999,995 \text{ cycles}}{1,000 \text{ seconds}} = 9,999,999.995 \text{ Hz}$$

MODEL 8164

SECTION 3

SPECIFICATIONS

3.0 INTRODUCTION

This section contains detailed electrical and mechanical specifications for the Model 8164 WWVB Receiver Disciplined Oscillator.

3.1 RECEIVER/COMPARATOR

RECEIVED STANDARD FREQUENCY: 60 kHz, NBS Station WWVB

SENSITIVITY: 0.4 μV rms into 50 ohms. Minimum field strength at antenna, 30 μV per meter when used with Model 8206 antenna.

SIGNAL-TO-NOISE RATIO: -35 dB worst case to remain phase locked to the carrier.

NBS OUTPUT: Phase locked to WWVB carrier, 0.1, 1.0, 5.0 or 10 MHz output. Frequency selected by front panel pushbutton. The output impedance is 100 ohms. The open circuit output low level voltage is less than 0.5 volts and the high level voltage is typically 3.4 volts. The signal is TTL compatible into loads greater than 120 ohms. Noise jitter is typically 1.0 E-7 in a 1 second gate period.

PHASE LOCK INDICATION: Green panel lamp indicates phase lock to WWVB. Red lamp indicates phase unlock.

LOCAL COMPARATOR INPUT: 0.1, 1.0, 5.0, or 10.0 MHz, front panel selectable, 100 mV rms minimum into 50 ohms.

TIME CODE: BCD yielding date, time of day, and a correction factor for converting from atomic time to celestial time.

3.2 FREQUENCY STANDARD OUTPUTS

FRONT PANEL: 0.1, 1.0, 5.0, or 10 MHz, front panel selectable. The output impedance is 100 ohms. The open circuit output low level voltage is less than 0.5 volts and the high level voltage is typically 3.4 volts. The signal is TTL compatible into loads greater than 120 ohms.

REAR PANEL: Separate outputs at 0.1, 1.0, 5.0, and 10 MHz, 600 mV rms sine wave into 50 ohms, 30 dB harmonic suppression. Without termination output is TTL-compatible.

If Option 03 is added, these four outputs are converted to drive Frequency Distribution Line Taps only. In this version, all four rear panel outputs provide 10 MHz sine waves and 12 VDC to 50-ohm cable that drives the Line Taps. In both versions, OUTPUT FAULT lamp shows absence of signal at any output connector.

3.2.1 FREQUENCY STANDARD STABILITY

LONG TERM: Accuracy is typically held to within ±1.0 E-9.

SHORT TERM STABILITY: 2.0 E-10 rms over 10 successive 10-second counts.

TEMPERATURE: ±5.0 E-10 per °C maximum, 0-50°C.

LOAD: ±1.0 E-11 for any load change.

SUPPLY VOLTAGE: ±2.5 E-10 maximum for +10% voltage change.

WARM-UP AT 25°C: Within ±2.0 E-9 of NBS reference 4 hours after receiver phase locks to WWVB.

3.2.2 FREQUENCY ADJUSTMENTS

FINE: Microprocessor controlled with an adjustment resolution of 2.44 E-10

COARSE: Internal adjustment with ±2.5 E-6 minimum range.

3.3 STANDBY SUPPLY

EXTERNAL: Rear panel AUX IN/OUT connector Pin 3 accepts 22-30 VDC for oscillator standby power during AC line interruptions. Suitable for used with lead-acid batteries. Current drain during power interruption is 40 ma typical, 200 ma maximum. The external battery is float-charge at a 200 ma rate, voltage limited and temperature compensated.

OPTION 34 BATTERY PACK: Mounted internally weight 6 lbs. Allows 50 hours typical operation at +25°C, 36 hours minimum standby operation during AC line interruption. Recharge rates, 33% in 6 hours, 66% in 12 hours, 100% in 36 hours.

3.4 STRIP CHART RECORDER

READOUT: Displays comparison of local input signal or internal frequency standard with WWVB. May be switched to monitor receiver phase lock voltage. Readings are permanently recorded on chart paper. Real-time readout on edgewise meter with 2.4 inch scale at the top of the panel display.

CHART SPEEDS: Chart recorder speed as shipped from the factory is 20 mm per hour. The speed may be changed to 10 or 60 mm per hour by substituting the cams supplied with the Simpson manual. Refer to the Simpson Operators Manual for instructions on chart speed changing and paper replacement.

PHASE COMPARISON SCALE: Selectable 0-50 or 0-10 microsecond full scale relative time.

PAPER: 52 ft. reel, 2.75 inches wide, pressure sensitive, rectilinear scales. One roll lasts for 1 month of continuous use. The time scale and hour markers are printed on the chart paper. Replacement paper may be ordered through Spectracom Corporation. Order part number MP00025 for a box of 10 rolls.

3.5 ALARM LAMPS

OUTPUT FAULTS: Indicates the disappearance of standard output signal from any of the four rear-panel outputs.

FREQ: Standard oscillator is off frequency by more than 1.0 E-8.

SIGNAL: Lamp is on if receiver phase lock is lost for more than 10 hours.

CPU: Indicates microprocessor failure.

ADJUST OSC: Standard oscillator has aged so that the microprocessor must pull it to within 1.0 E-7 of the end of its fine adjustment range to hold it on frequency. Warns that internal coarse oscillator adjustment should be made within three months. Occurs every few years.

TIME: With Timelock™ activated, indicates time error accumulation of more than four milliseconds.

3.6 ALARM OUTPUTS

SIGNAL: RS-422

ALARM: An alarm is triggered whenever any of STATUS ALERT or OUTPUT FAULT lamps light. The alarm is reset when the fault has been cleared. The alarm outputs are found on the rear panel AUX IN/OUT connector.

3.7 DATA STRUCTURE

SIGNAL: RS-232C

CHARACTER STRUCTURE: 1 start bit, 7 data bits, 1 mark bit, and 1 stop bit.

BAUD RATE: Dip switch programmable from 300 to 9600 baud.

3.8 MECHANICAL & INSTALLATION

LINE POWER: 115/230 VAC ±10%, 60 Hz. Consumes 60 VA.

OPERATING TEMPERATURE: 0 to 50°C.

SIZE:
Panel Height	5.25 in.	(133 mm)
Panel Width	17 in.	(432 mm)
Depth	13.5 in.	(343 mm)
Weight	21 lbs.	(9.5 Kg)
Ship Wt.	25 lbs.	(11.3 Kg)

Handles extend 1.75 in. from front panel.
Allow 2-3 inches cable clearance at rear.

MODEL 8164

SECTION 4

PRINCIPLES OF OPERATION

4.0 INTRODUCTION

The receiver consists of an RF Amplifier Assembly, a Receiver Assembly, and Oscillator and Power Supply Assembly, an Output Amplifier Assembly, and a Frequency and Time Comparator Assembly, FTC, as shown in the Block Diagram, Figure 4-1, and Mainframe Schematic Figure 4-2.

The 60-kHz output of the RF Amplifier Assembly is fed to the Receiver Assembly where the carrier is detected and translated to a phase locked 10-MHz. The AGC voltage is generated in the Receiver Assembly for use in controlling the gain of the RF Amplifier during phase lock conditions.

The output of the 10-MHz frequency standard, located in the Oscillator and Power Supply Assembly, is fed to the Output Amplifier Assembly for distribution and is also divided down to 100 kHz for phase comparison with the WWVB-derived signal.

The NBS 10-MHz signal is fed to the FTC Assembly and used as a time base for measuring the STD 10 MHZ signal. The TIME CODE from the Receiver Assembly is fed to the FTC Assembly where accumulated time error is measured and optionally nulled out.

4.1 RF AMPLIFIER A1 (P/N 001100)

The RF Amplifier Assembly filters and amplifies the signal. Figure 4-3 is the schematic diagram and Figure 4-4 is the component location diagram.

The signal from the antenna is applied to T1 which matches the 50-ohm input impedance. The secondary of T1 and C2 form a 60-kHz tuned circuit with a 200-Hz bandwidth. The output of Q1 is applied to a narrow 60-kHz band-pass filter, made up of Q2, Y1, C7, C8, C9, and C10. The filter bandwidth is 30 Hz, with C8 trimming the band-pass center frequency at 60 kHz. C9 and C10 couple to the output of Y1 a signal that is 180° out of phase and tuned to null 100 kHz. This tuning provides a sharp band-pass response at 60 kHz with very steep high frequency rejection.

The output of the crystal filter is fed to U1. The output of U1 is tuned by L3, C14, C15, and C23. Amplifier U1 provides AGC for the receiver. Trimmer R19 provides AGC level adjustment to U1 at the gain control input U1 pin 5. The output of U1 is coupled to U2 by C16. The output of U2 goes to emitter follower Q3 providing the output signal to the A2 Receiver Assembly through P2-3.

The supply voltage, +12 VDC, enters the board at P2-1, from the A2 Assembly, through R18, L2, and L1, to power the amplifier stages. The 12 volts also goes to S1, R2 and through T1 to provide power to the antenna preamplifier. If a MODEL 8207 LINE PREAMPLIFIER is used, S1 should be set to P.

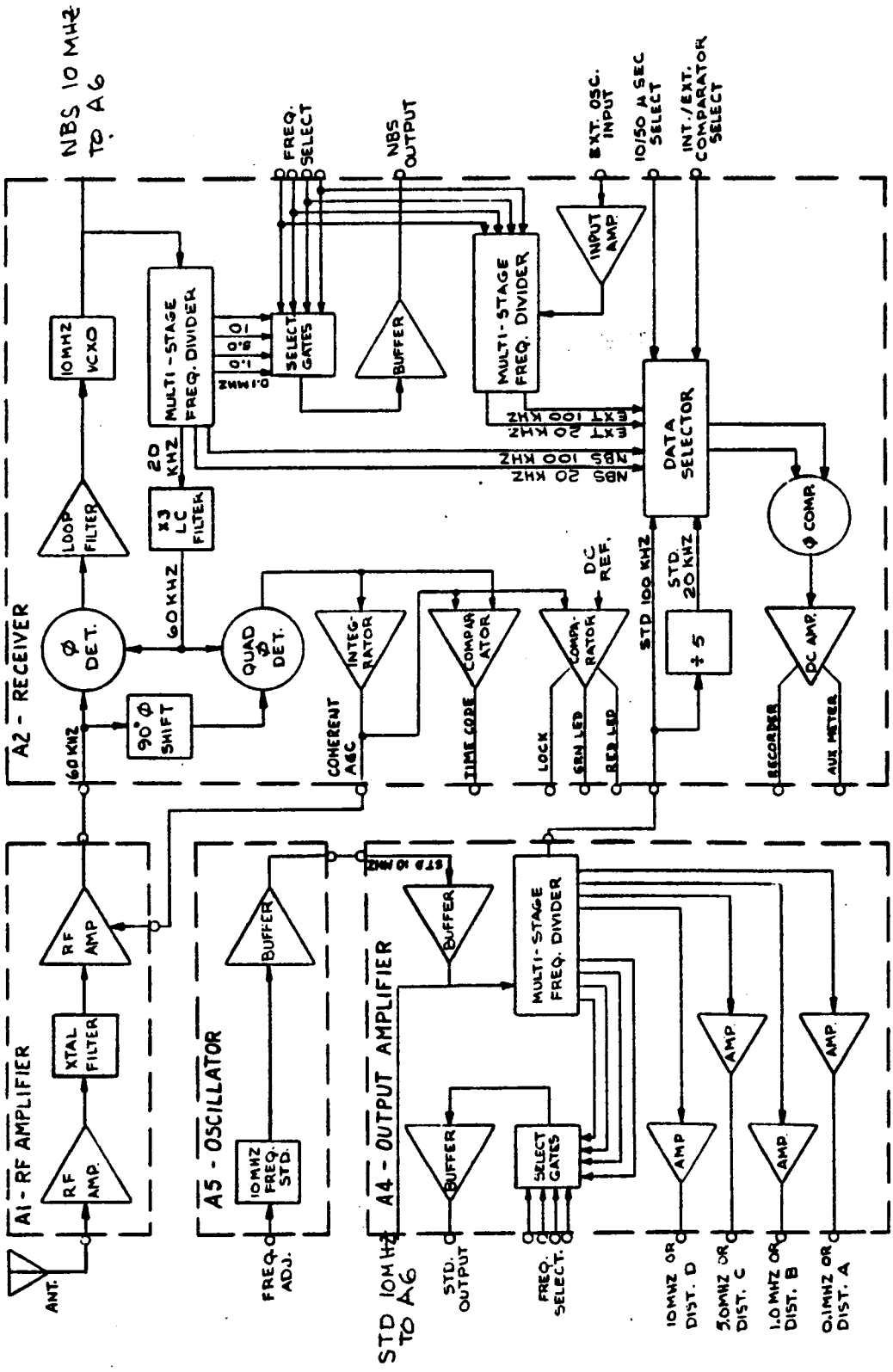


FIGURE 4-1 MODEL 8164 BLOCK DIAGRAM, SHEET 1 OF 2

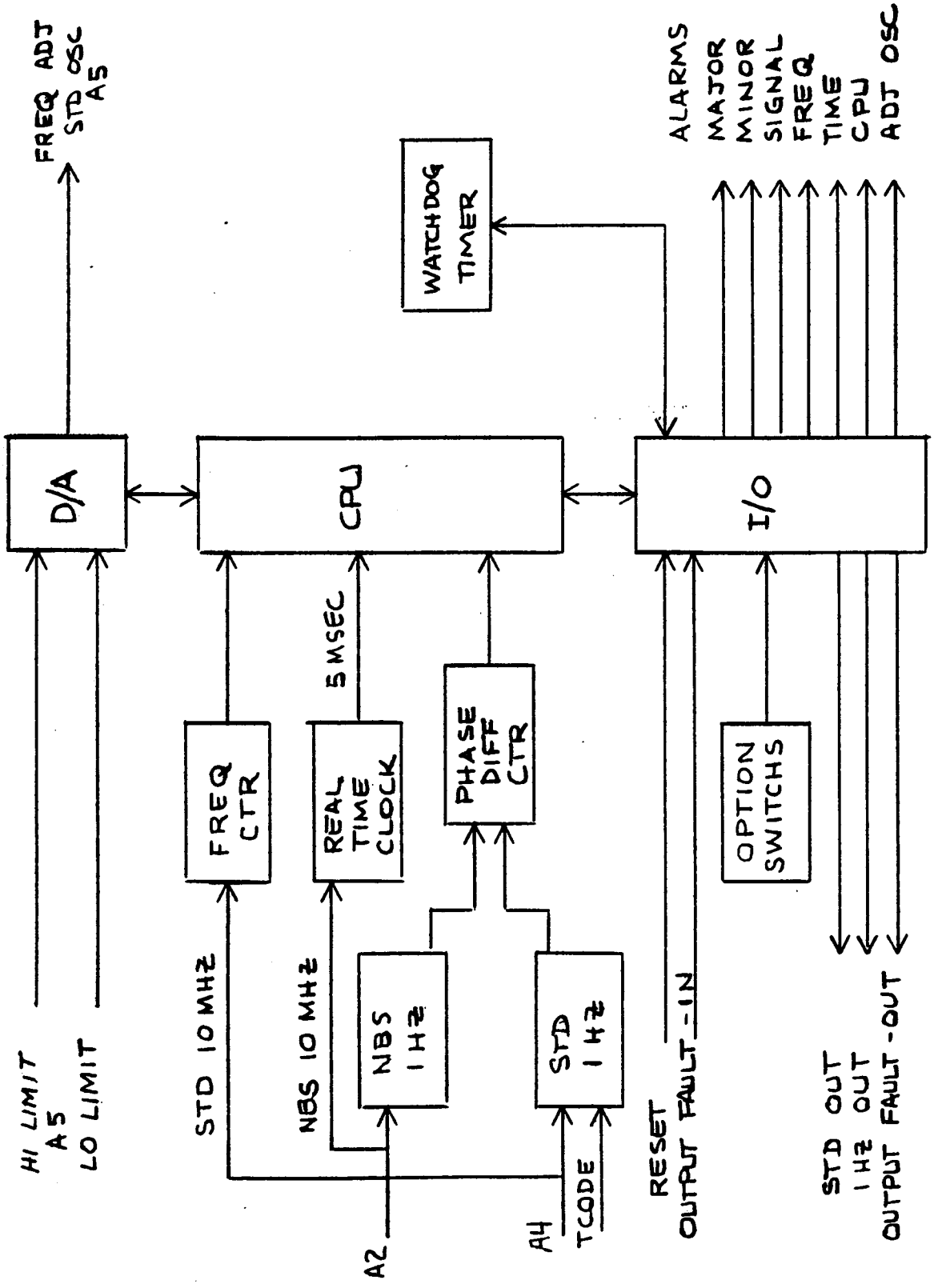


FIGURE 4-1 MODEL 8164 BLOCK DIAGRAM, SHEET 2 OF 2

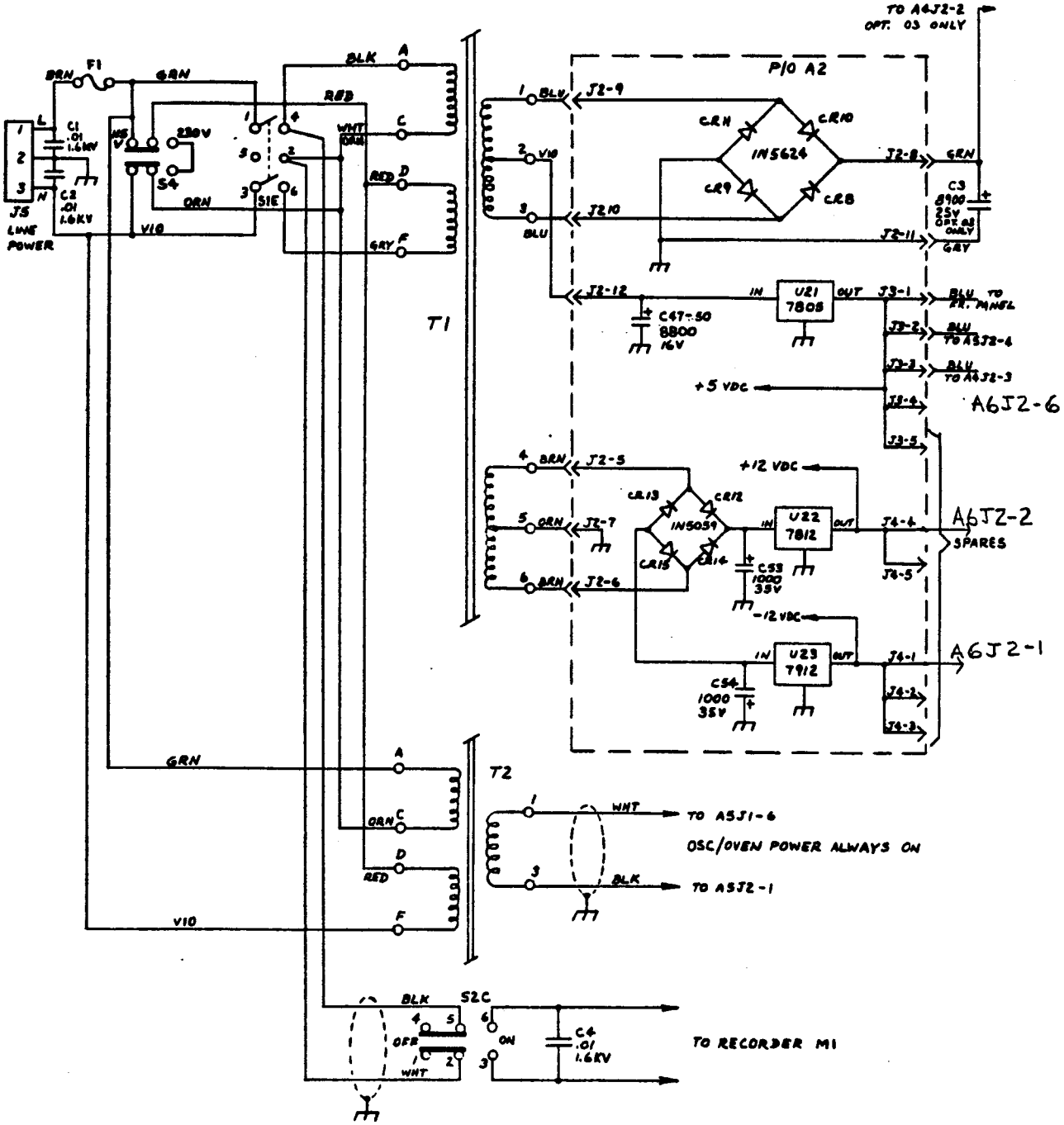


FIGURE 4-2 MODEL 8164 MAINFRAME SCHEMATIC, SHEET 1 OF 3

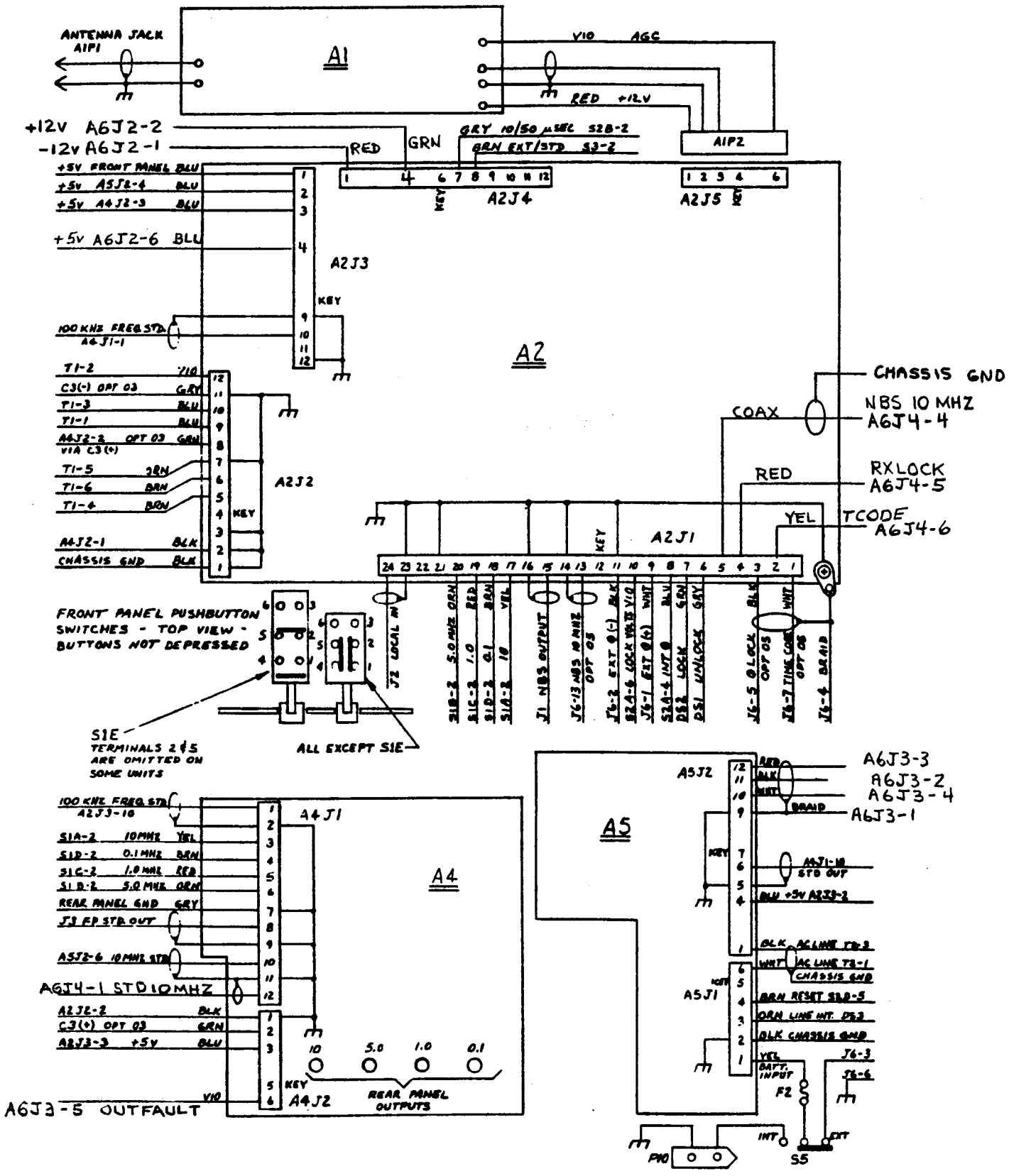


FIGURE 4-2 MODEL 8164 MAINFRAME SCHEMATIC, SHEET 2 OF 3

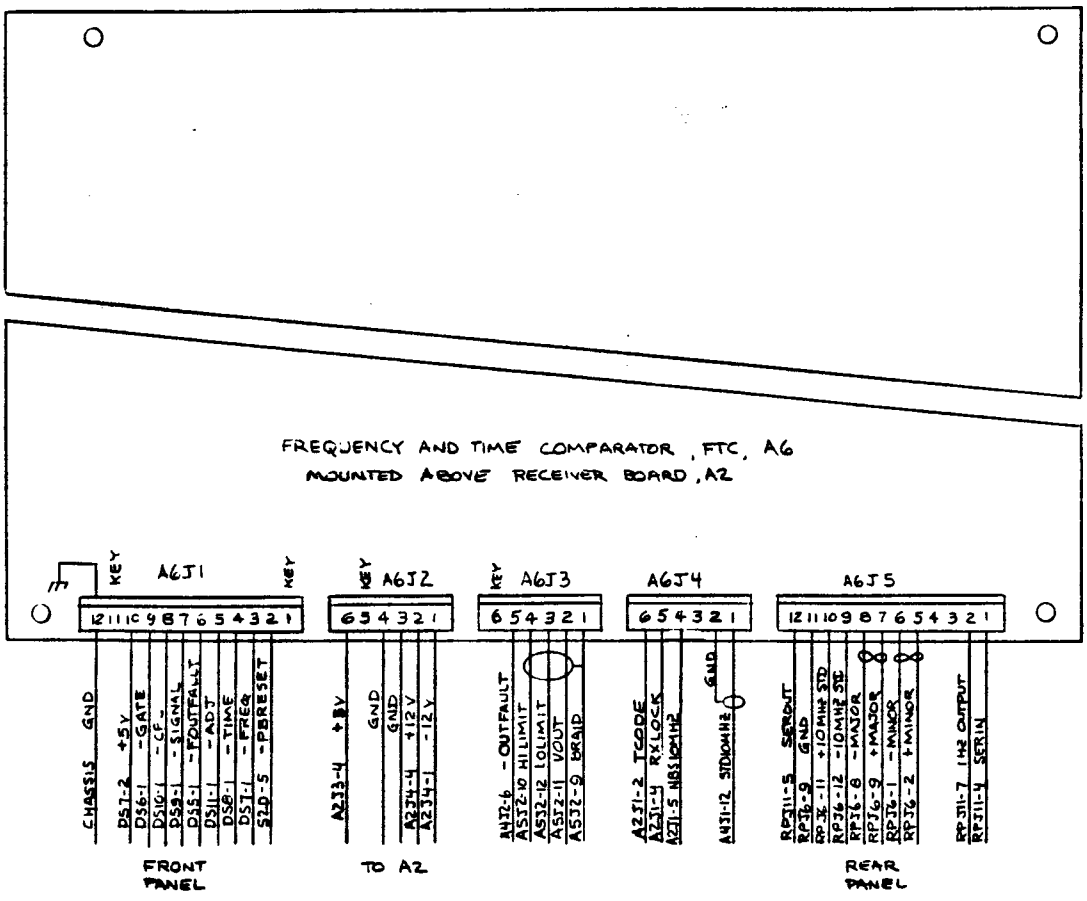


FIGURE 4-2 MODEL 8164 MAINFRAME SCHEMATIC, PAGE 3 OF 3

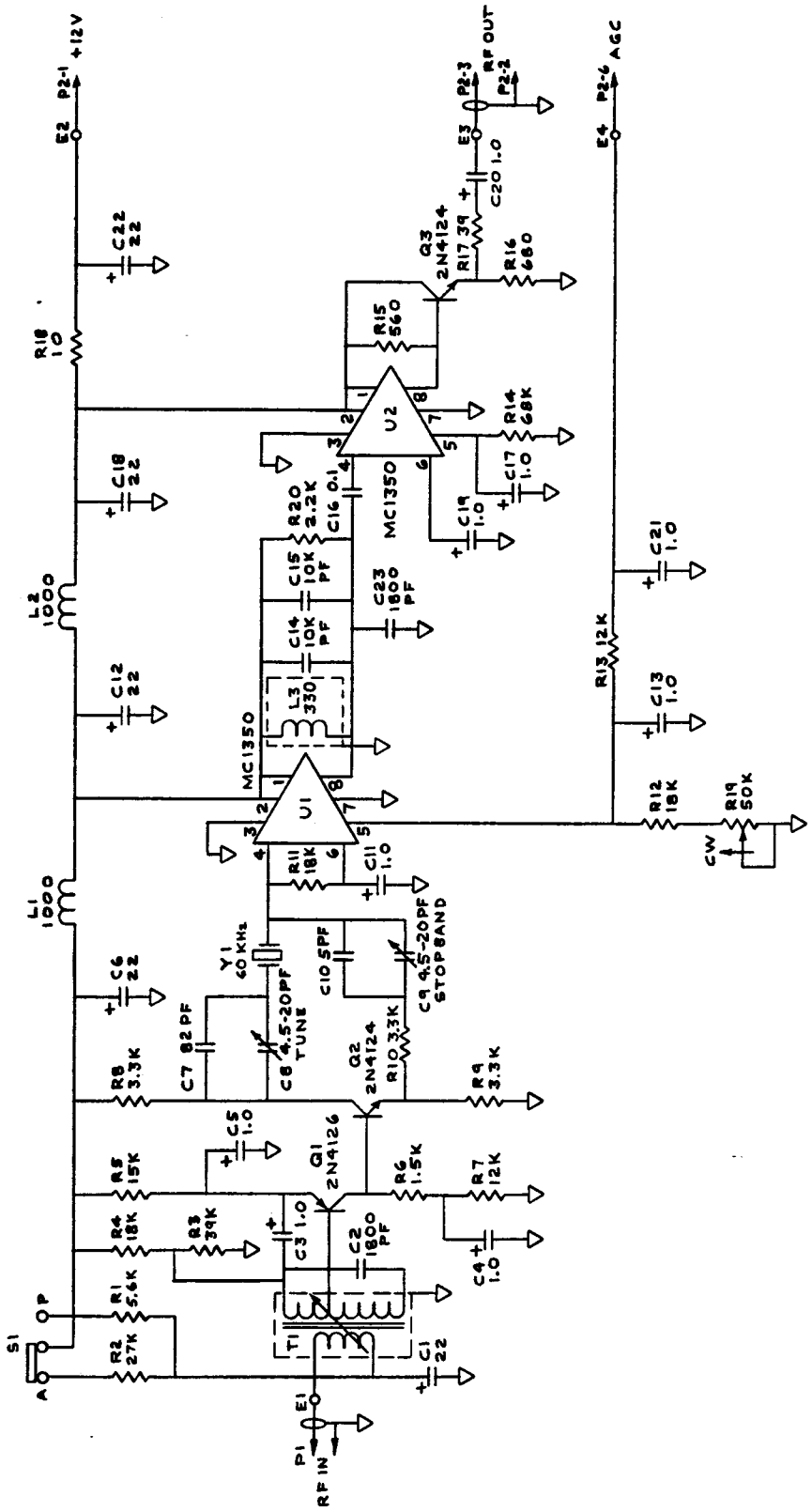


FIGURE 4-3 RF AMPLIFIER A1 SCHEMATIC DIAGRAM

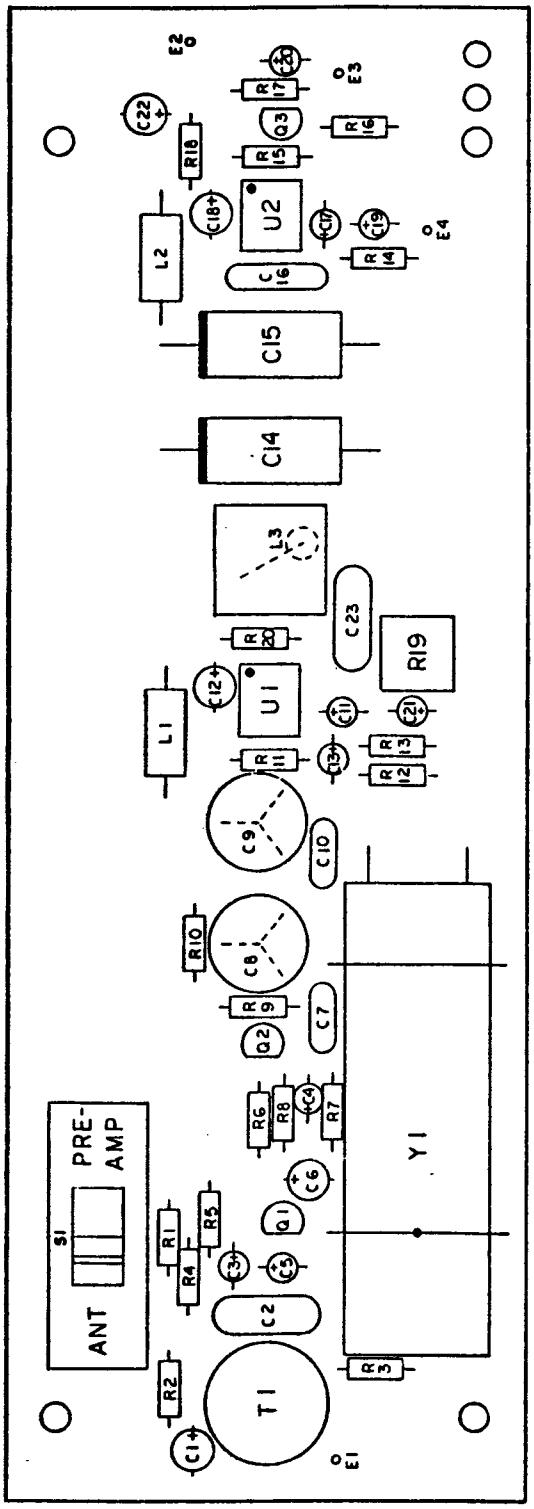


FIGURE 4-4 RF AMPLIFIER A1 COMPONENT LOCATION DIAGRAM

4.2 RECEIVER ASSEMBLY A2 (P/N 001200)

The Receiver Assembly A2 functions are:

1. Provides synchronous detection of the carrier frequency and translates it to 10 MHz.

2. Provides AGC voltage.

3. Time code detection.

4. Phase lock/unlock indication.

5. Derivation of front panel NBS OUTPUT signal from the 10 MHz phase locked oscillator.

6. Buffering, amplifying and dividing the external local oscillator input at the LOCAL INPUT connector and feeding it to the phase comparator.

7. The phase comparator which compares the local input or the internal standard oscillator with the phase locked output to determine frequency error and drift.

8. The +12 VDC, -12 VDC, and +5 VDC power supplies are located on this assembly.

Figure 4-5 is the schematic diagram. Figure 4-6 is the component location diagram.

The signal from the RF Amplifier Assembly is fed into connector J5-3. It goes to the phase locked loop, U1 and U2A, which provides synchronous detection of the carrier frequency and translates it to 10 MHz. The second is through U3 and U2B to provide AGC voltage, time code detection, and phase lock/unlock indication.

4.2.1 PHASE LOCKED LOOP

The reference input to the phase detector U1-1 comes from the A1 Assembly. The comparison frequency input to phase detector U1-8 is derived from the phase locked oscillator. The output from U1 is a DC voltage which is a function of the phase difference of these 60 kHz signals. The output is amplified by U2A, the loop-filter/amplifier. This amplified DC voltage is further amplified by Q2 and Q3 where it becomes the VCO control voltage which pulls the oscillator (Q4 and Y1) into phase lock with the incoming carrier frequency from WWVB. This oscillator pulling is performed by the DC voltage which appears on the cathode of varicap CR2. The oscillator output frequency is held exactly at 10 MHz by the DC voltage applied to the VCO control line. The collector output from Q4 is buffered by gate U5A and divided by U8, U9, U10, and U16. At various points along the divider chain frequencies are selected and fed to the NBS OUTPUT connector at the front panel through gate U6B. NBS output frequency is selected by the FREQUENCY-MHZ switches through gates U7A, U7B, U7C, and U7D.

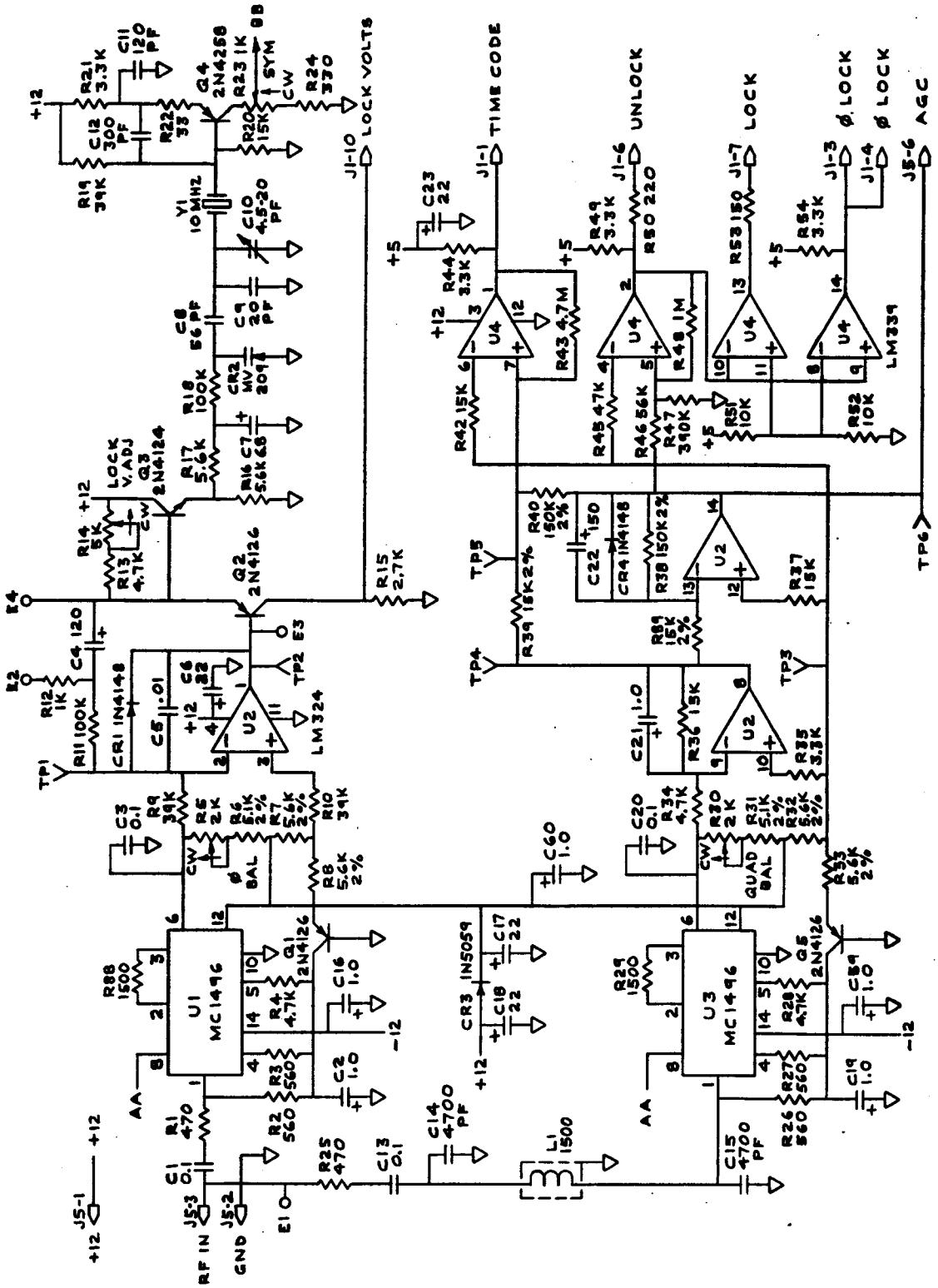


FIGURE 4-5 RECEIVER ASSEMBLY A2 SCHEMATIC DIAGRAM SHEET 1 OF 3

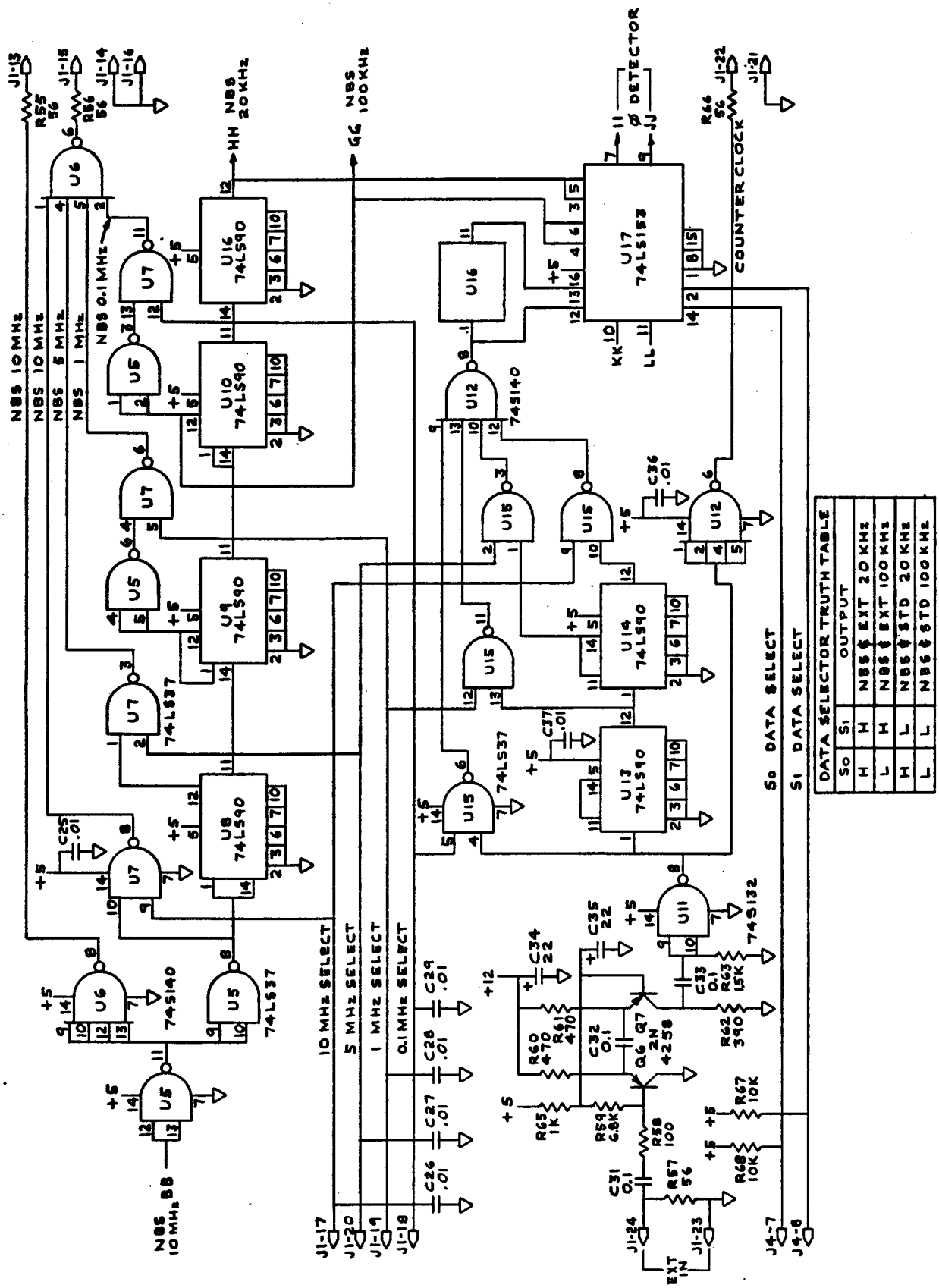


FIGURE 4-5 RECEIVER ASSEMBLY A2 SCHEMATIC DIAGRAM SHEET 2 OF 3

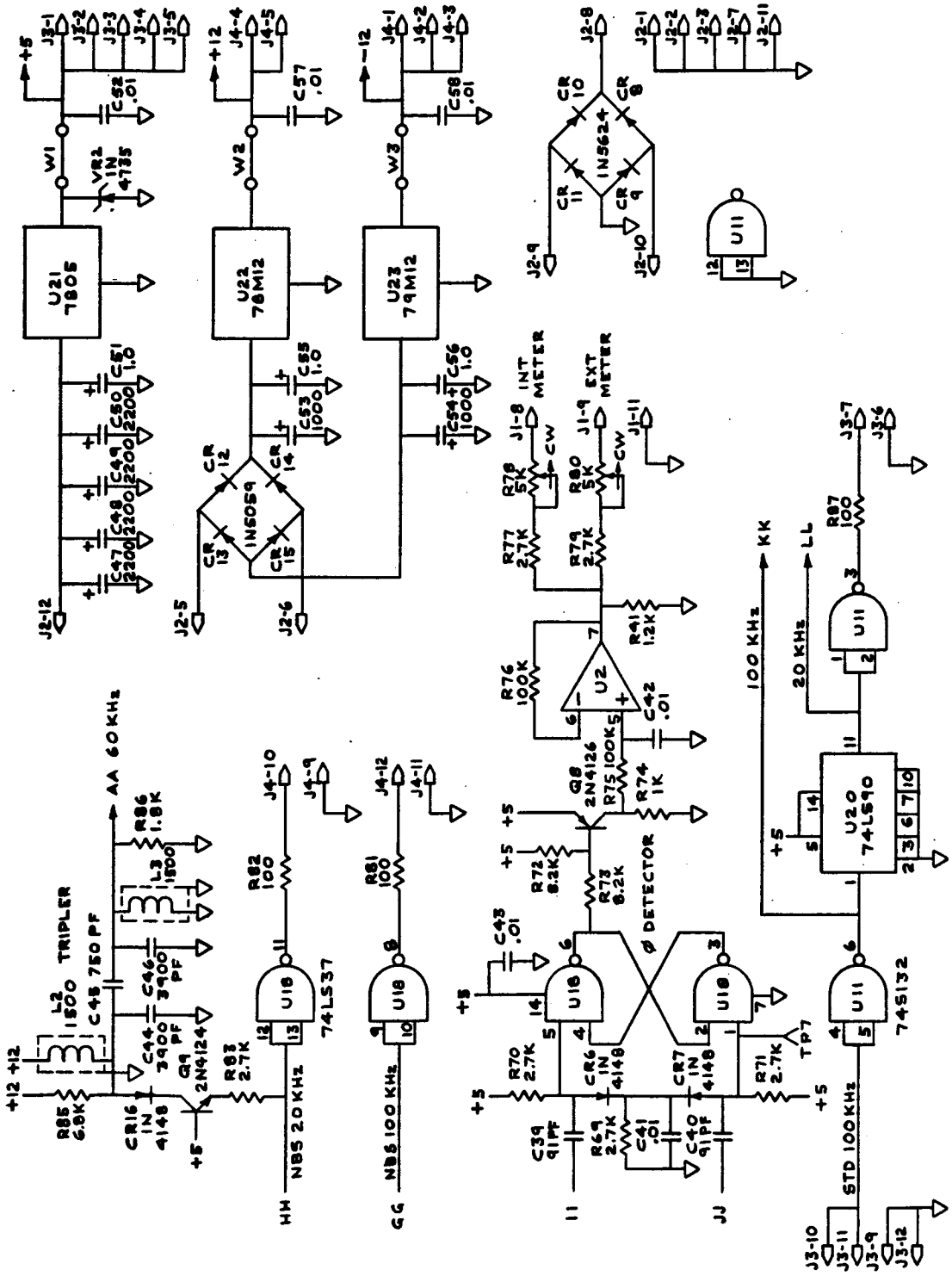


FIGURE 4-5 RECEIVER ASSEMBLY A2 SCHEMATIC DIAGRAM SHEET 3 OF 3

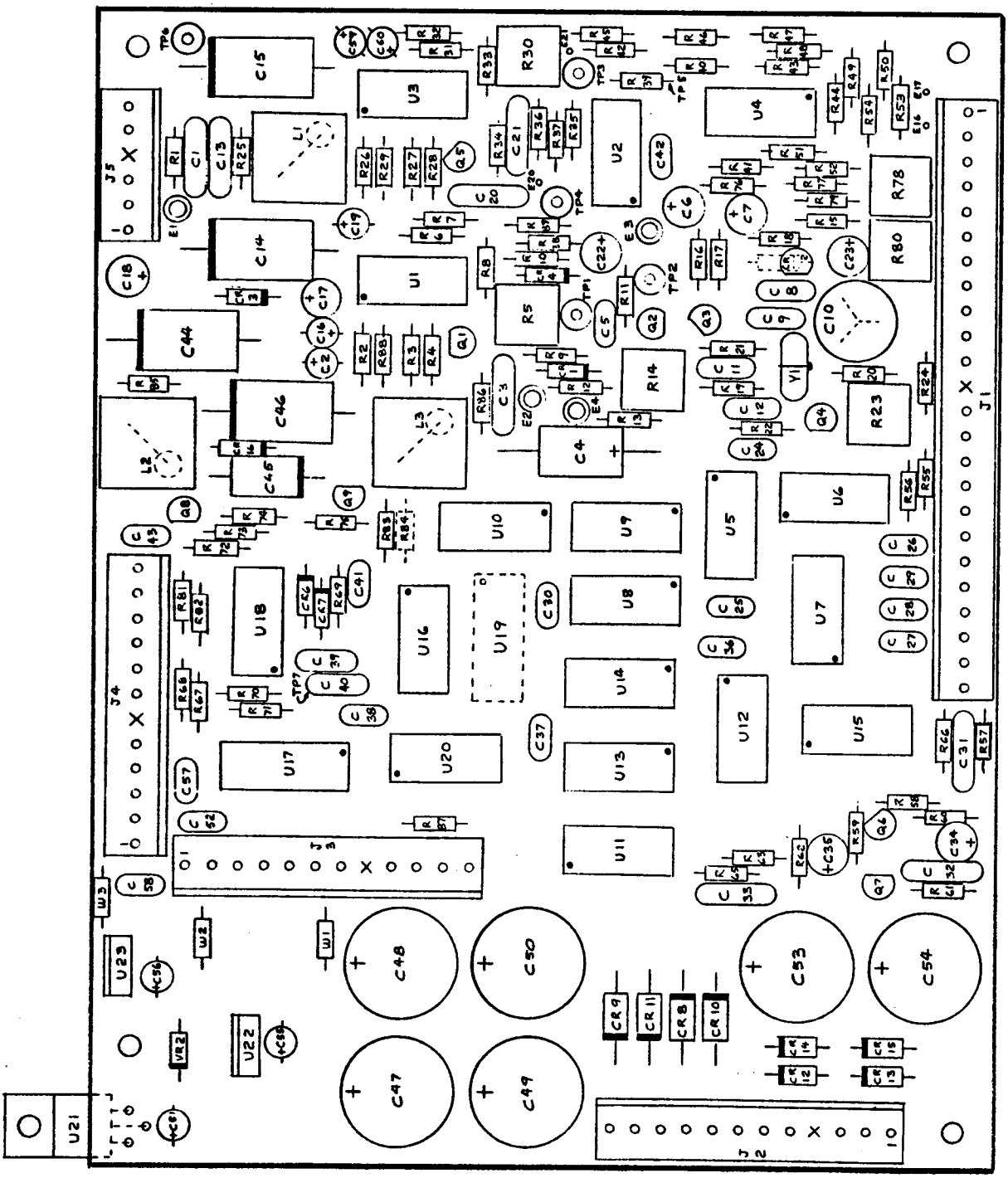


FIGURE 4-6 RECEIVER ASSEMBLY A2 COMPONENT LOCATION DIAGRAM

This phase locked signal is divided down to 100 kHz and 20 kHz. These frequencies are fed to the signal selector U17 and buffered by U18C & U18D.

The 20 kHz output is injected to tripler stage Q9 where the output, 60 kHz, is filtered and fed back into the comparison input of phase detector U1-8. The phase locked loop translates the incoming 60 kHz carrier frequency from WWVB to 10 MHz at the crystal oscillator output, and divides it down to 60 kHz for comparison in the phase detector.

4.2.2 AGC LOOP

The input from the RF Amplifier A1 goes to U3-1 phase detector after being shifted in phase 90° by C14, C15, and L1. U3-6 quadrature phase detector output goes high only when the inputs at U3-1 and U3-8 are in quadrature at 60 kHz. The output level from this phase detector is proportional to the level of the incoming carrier, and provides the basis for time code amplitude detection, and AGC voltage generation.

The phase detector output is amplified by U2B, the time constant of which is approximately 15 milliseconds. The output of U2B is split in two directions: first, through R39 to voltage comparator U4A where small amplitude variations in signal are detected and provide the time code output. Second, through R89 to amplifier U2C that has an integrating time constant of approximately 25 seconds. The slowly varying output of U2C is used as the AGC voltage. This AGC voltage is fed back to the RF AMPLIFIER A1 to control the gain of the input stage.

Because the AGC voltage is derived from the output of a quadrature detector, it is present only after phase lock is achieved, and becomes the basis for synchronous AGC. The gain of the amplifier in the front end of the amplifier is running wide open until phase lock occurs. After phase lock is achieved, the input amplifier gain is reduced to a level sufficient to provide a reference for the phase locked loop and other stages in the Receiver Assembly A2. No stages are allowed to saturate or be over-driven in strong signal conditions.

TP3 is located at the reference voltage against which AGC amplifier U2C operates. The voltage measured from TP3 to TP6 is proportional to the input signal level and can be used as an indication of signal strength. If the antenna is adjusted and aimed to maximize this AGC voltage, optimum receiver operation is obtained.

The AGC voltage is used by the voltage comparators U4B, U4C, and U4D to indicate phase lock. When the AGC voltage measured from TP3 to TP6 rises to approximately 1.0 VDC, the output of comparator U4B goes high turning off the red UNLOCK front panel indicator. When lock is acquired, the green LOCK indicator goes on. Output of U4D goes high and provides an output showing that phase lock has been achieved.

4.2.3 PHASE DETECTOR BALANCE ADJUSTMENT

The output of phase detector U1 for the phase locked loop control is balanced by adjustment of trimmer R5. The output of the quadrature phase detector U3 is balanced by adjusting trimmer R30.

4.2.4 PHASE COMPARATOR

When local oscillators to be calibrated are connected to the LOCAL INPUT jack on the front panel, they appear at the "external input" terminals of the A2 Receiver Assembly at J1 pin 24. The buffer amplifier Q6-Q7 feeds the signal to gate U11A where it is then divided in frequency by U13 and U14. Gates U15A, U15B, U15C and U15D are used to select the appropriate divider output to provide a 100 kHz signal to data selector U17.

The operation of data selector U17 is shown in the truth table in Sheet 2 of the A2 Receiver Assembly schematic. The function of data selector U17 is to select the appropriate signal to be fed into each port of the phase detector U18. The two outputs from U17 are chosen by selecting the appropriate combination of highs and lows on inputs 2 and 14. Referring to the truth table for data selector U17, we can see that if both pins 2 and 14 are high, then output pins 7 and 9 will provide NBS 20 kHz and External 20 kHz to the phase detector inputs. Under this condition, the phase detector output will cause the meter to read 50 microseconds full scale (the reciprocal of 20 kHz is 50 microseconds, or one full cycle of a 20 kHz signal.) If the front panel phase comparator selector switch is put into the STANDARD OUTPUT position, then a low appears at pin 2 of the data selector and 20 kHz derived from the internal frequency standard signal. If the data selector is set up to provide 100 kHz signals to the phase comparator then the full scale reading of the output meter will be 10 microseconds (one full cycle at 100 kHz.)

U18A and U18B are connected as a flip-flop phase detector whose output pulse width is proportional to the relative phase relationship between the two input signal pulses. Buffering of this output pulse is provided by Q8, and integration of the output pulse by R75 and C42. Buffer amplifier U2D then drives the front panel meter and the rear panel auxiliary output for an external meter or chart recorder. Full scale adjustments of both are made by adjusting the current to ground through a milliammeter at each output to exactly 1.0 mA with no local signal input and with TP7 grounded, causing the phase detector to indicate full scale. Trimmer resistor R80 adjusts full scale setting of rear panel output and R78 is used to adjust the front panel full scale meter reading.

4.2.5 POWER SUPPLIES

Three terminal regulators U21, U22, and U23 provide output voltages of +5.0 volts, +12.0 volts, and -12.0 volts. Because U21 which provides the +5.0 volts is the most heavily loaded of the voltage regulators, it is heat sunk to the chassis at the rear left corner of the circuit board. Regulators U22 and U23 are loaded more lightly and do not require heat sinking.

When Option 03, Built-In Frequency Distribution Amplifier, is provided in the unit, an additional +12.0 volts supply is provided as a part of the A4 Output Amplifier Assembly. This additional +12 volt supply also is given more filtering.

4.3 OUTPUT/DISTRIBUTION AMPLIFIER A4 (P/N 002400)

The internal frequency standard oscillator output is fed to the 10 MHz standard input of the A4 Output Amplifier Assembly at J1 pin 10 where it is buffered and amplified by Q1 and Q2. See Figure 4-7, A4 Output Assembly Schematic and Figure 4-8, A4 Component Location Diagram. From there the signal goes through gates U1A and U1B where it is sent through gates U4C and U8A directly to the rear panel output after being filtered by L1, L2, and C17. Similarly, the divided down signals at 5.0 MHz, 1.0 MHz, and 0.1 MHz are fed to their respective output jacks at the rear panel after frequency division at U5, U6, and U7, respectively.

The drive levels from the rear panel outputs are sinusoidal at 4.0 volts peak-to-peak. Diodes CR2, CR6, CR10, and CR14 allow current sinking by output drivers U8 and U9 thus enabling TTL circuitry to be driven by these outputs, if the output coaxial lines are not terminated. If the outputs are terminated with 50 ohms, the output wave shape is still sinusoidal but at a reduced voltage level, approximately 0.6 volts rms.

The presence of output signal at each of these rear panel jacks is detected by a diode/capacitor combination at each output jack and used as a signal for front panel indication of output fault. If the rear panel output at anyone of these four jacks is not present, the red lamp on the front panel of the unit is lit indicating an output fault.

Detector outputs at all four jacks are gated together through diodes CR5, CR9, CR13, CR17 and fed to a transistor switch consisting of Q5, Q4, and Q3 which lights the OUTPUT FAULT lamp in the absence of output signal.

The output signals as they are divided are fed to gates U4, U3, and U2 and are selectively fed to the front panel STANDARD OUTPUT jack according to the front panel output frequency selector pushbutton and to the FTC Assembly A6.

4.4 OSCILLATOR AND POWER SUPPLY ASSEMBLY A5 (P/N 002500)

Oscillator U1 is a high-stability, oven-controlled quartz crystal oscillator. The board consists of control circuitry and an oscillator power supply. The output frequency from the board is 10.0 MHz. (See Figure 4-9 for the schematic and Figure 4-10 for the component location diagram.)

4.4.1 OSCILLATOR CONTROL CIRCUITRY

The +5 volts DC is fed into the oscillator at pin 1 where it drives the output stages and the output buffer stage Q1. The +21 volts DC is fed into pin 5 of the oscillator where it powers the oven and the oscillator. This voltage is double-regulated and filtered extremely well before it reaches the oscillator.

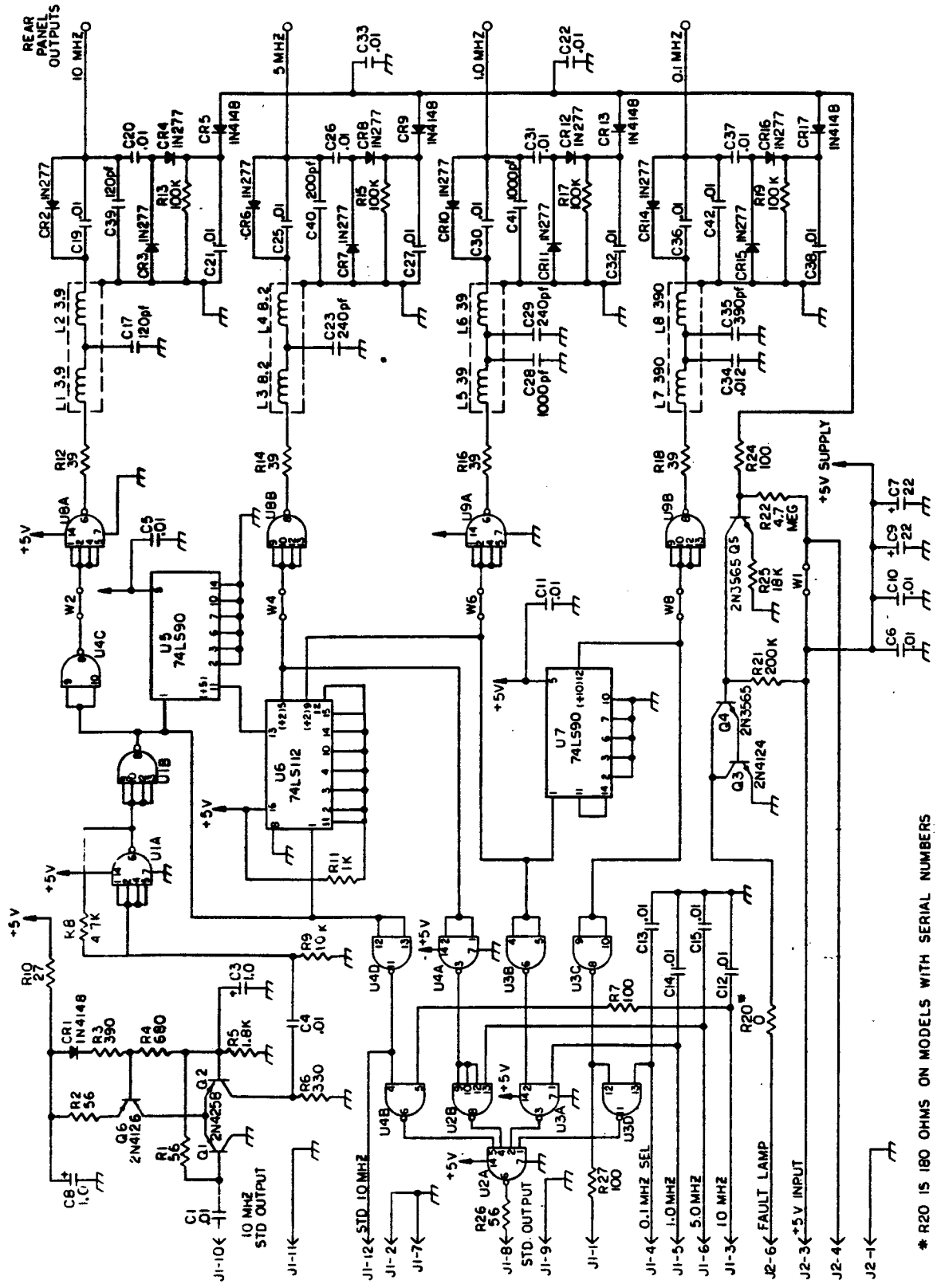


FIGURE 4-7 OUTPUT ASSEMBLY A4 SCHEMATIC DIAGRAM

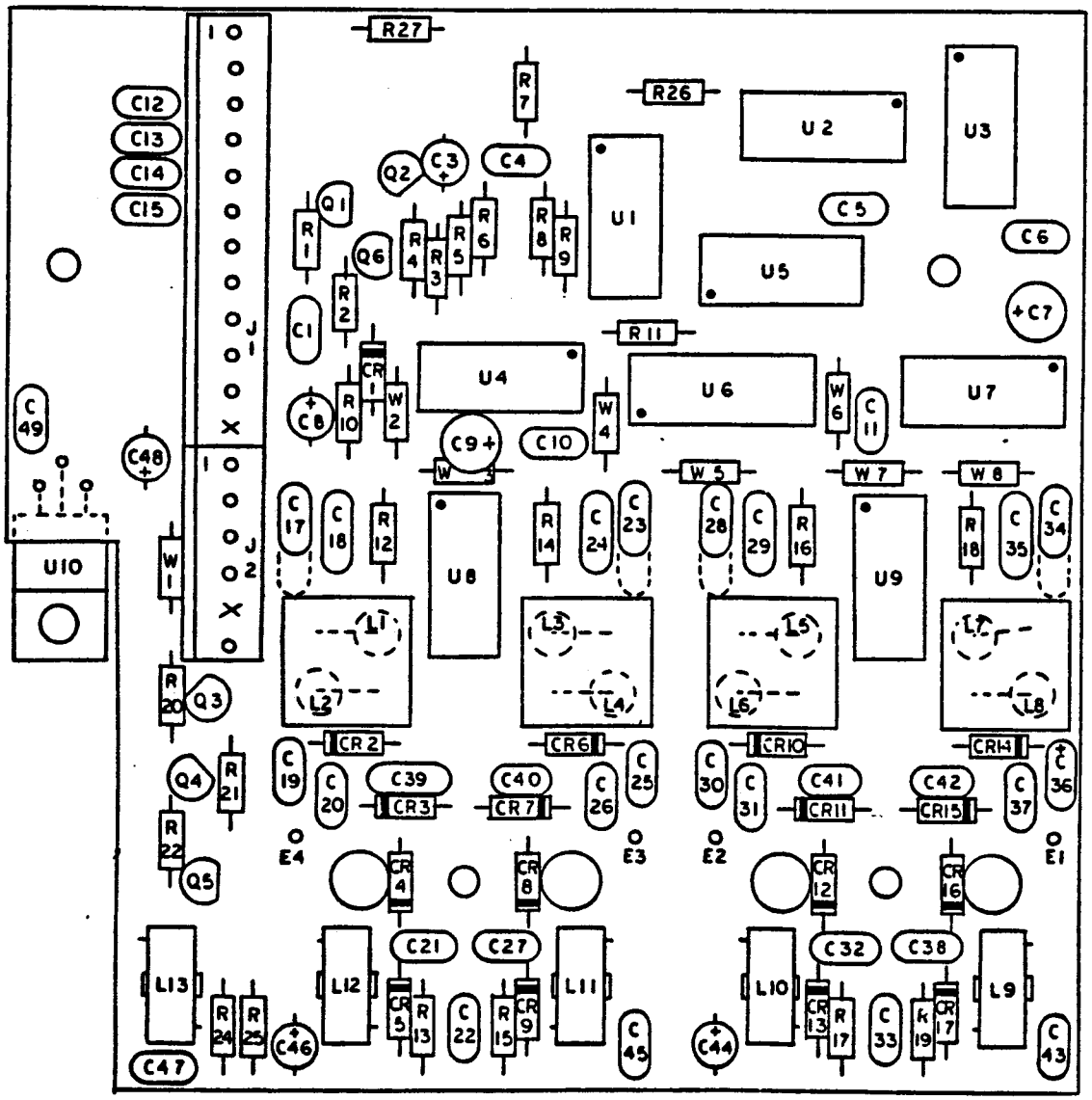


FIGURE 4-8 OUTPUT ASSEMBLY A4 COMPONENT LOCATION DIAGRAM

4.4.2 VOLTAGE REGULATORS

A diode bridge consisting of CR1 through CR4 feeds the primary regulator Q5, Q6, Q7, Q8, and Q10. Current is limited by Q5 as sensed at R14 and voltage is limited by Q8 as sensed by the voltage divider in its base circuit and VR1. Q10 provides output limiting for both voltage and current and holds the output voltage at the cathode of CR7 at exactly 27.6 volts.

If Option 34 is provided, the battery is connected at the cathode of CR7 via the battery fuse. A 24-volt lead-acid battery will be trickle-charged at 27.6 volts continuously when connected at this point. Maximum battery charging current under low charge conditions is approximately 200 milliamps, and final trickle-charge level is about 2.0 milliamps under full charge conditions.

If the primary power is disconnected from the unit, diode CR7 becomes back-biased by the battery voltage, effectively removing the primary voltage regulator from the circuit, and power is furnished to the secondary regulator U2 by the battery.

4.4.3 SECONDARY REGULATORS

Regulators U2 and series pass transistor Q9 drop the battery voltage and regulate it at 21.0 volts DC to power the oscillator and oven.

4.4.4 VOLTAGE ADJUSTMENTS

Primary output regulator voltage of 27.6 volts at +25°C is adjusted at trimmer resistor R18. This voltage should be adjusted by -50 millivolts per degree C if the temperature varies from +25°C. This provides optimum battery charging performance. Secondary regulator output voltage is adjusted to exactly 21.0 volts DC by trimmer resistor R25.

4.4.5 OSCILLATOR ADJUSTMENTS

The oscillator coarse frequency adjustment and trimmer resistor R4 are used for centering the oscillator frequency (only after 24 hours of warm-up) and for calibrating the control voltage.

4.4.6 LINE INTERRUPT DETECTOR

Transistors Q2, Q3, and Q4 provide an indication of line interruption after power has been restored following a power failure. When the voltage from the diode bridge disappears and is then restored, Q4 causes the front panel LINE INTERRUPT lamp to remain lit until the reset line is grounded by pushing the front panel momentary-contact pushbutton. This causes Q3 and Q2 to hold transistor Q4 in the OFF position causing the front panel indicator to be extinguished. The front panel LINE INTERRUPT lamp warns the operator that a power interruption has occurred and that oscillator warm-up must be accomplished before completely stable frequencies are obtained from the oscillator.

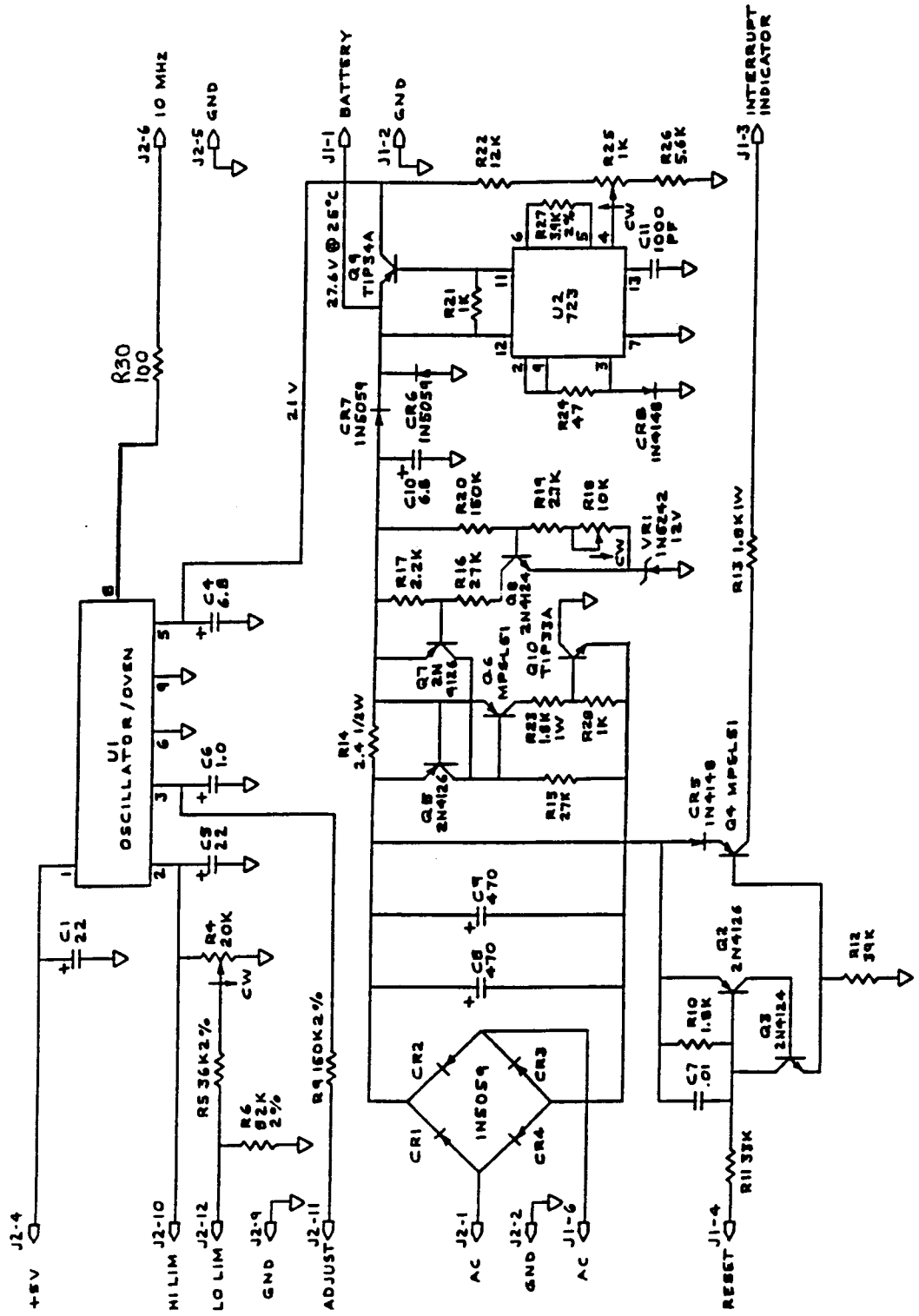


FIGURE 4-9 OSCILLATOR AND POWER SUPPLY A5 SCHEMATIC DIAGRAM

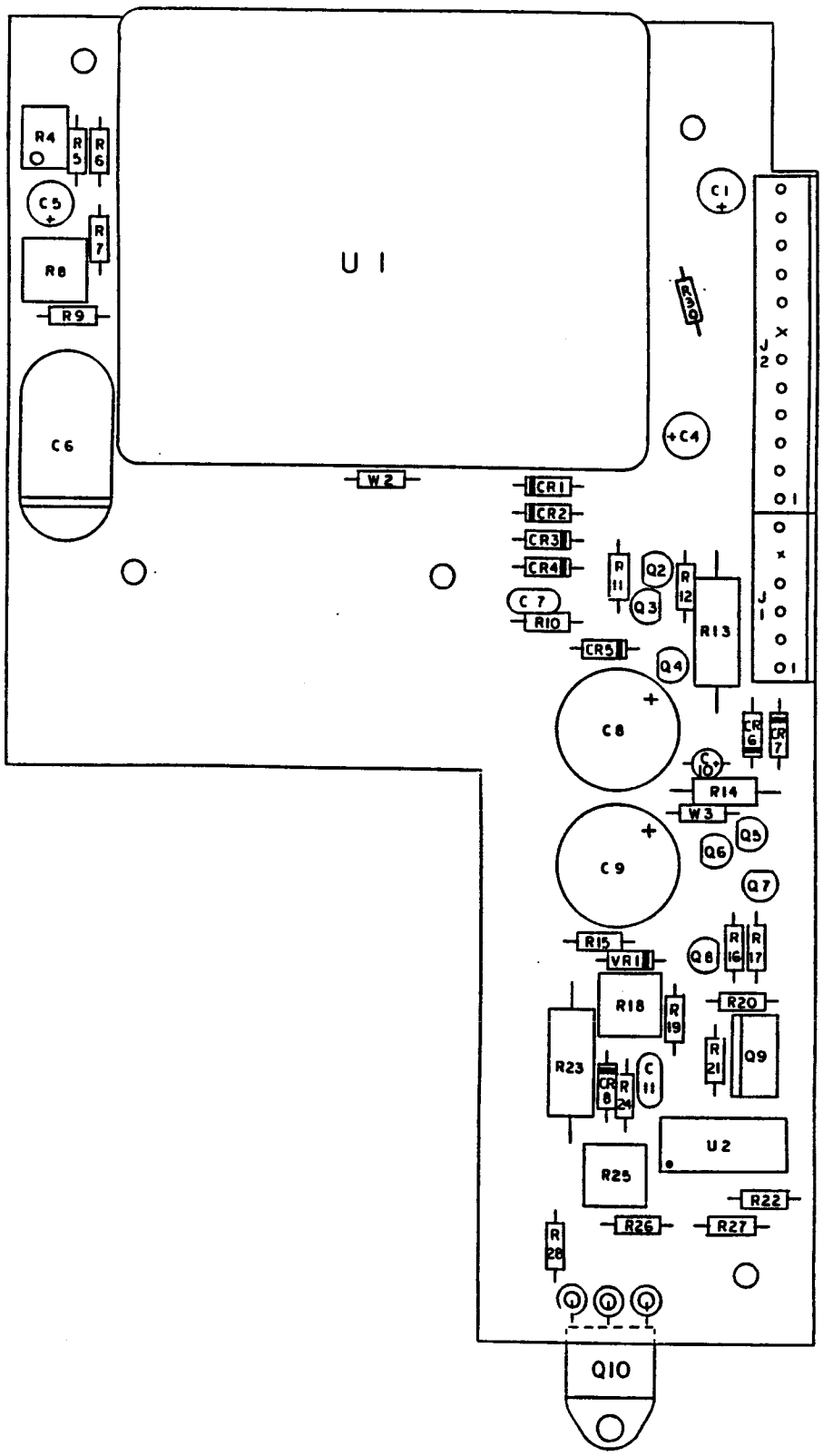


FIGURE 4-10 OSCILLATOR AND POWER SUPPLY A5 COMPONENT LOCATION DIAGRAM

4.5. FREQUENCY AND TIME COMPARATOR A6 P/N 018100

The Frequency-Time Comparator (FTC) consists of a number of functional elements including:

1. Central Processing Unit
2. Real-time Clock
3. Frequency Counter
4. NBS 1-Hz Clock
5. STD 1-Hz Clock
6. Phase Difference Counter
7. D/A Converter
8. Watchdog Timer
9. Miscellaneous I/O

The Central Processor provides for the overall control and logical operation of the FTC. The Central Processor is an 8031 and associated peripheral circuits including external ROM and RAM.

The Real-time Clock (RTC) provides a timing reference for software controlled activities such as the frequency counter gate and time code (TCODE) decoding. The RTC provides interrupts to the processor at 5 millisecond intervals. The RTC is derived by dividing down the NBS-10 MHz from the WWVB phase-locked receiver.

The Frequency Counter provides for the measurement of the frequency of the STD 10-MHz oscillator. The gate for the counter is derived from the NBS 10-MHz which is phase locked to the WWVB carrier. Frequency counting provides for the accurate control of the frequency standard.

The NBS 1-Hz is a 1-Hz signal derived by dividing down the NBS 10-Mhz. The NBS 1-Hz is used in decoding the time code (TCODE) received by the WWVB receiver and in providing a reference for determining the cumulative time error.

The STD 1-Hz is a 1-Hz signal derived by dividing down the STD 10-MHz. This division process provides for the tracking of cumulative frequency error in the frequency standard.

The Phase Difference Counter provides for the reading of the phase difference between the NBS 1-Hz and the STD 1-Hz. The phase difference represents the actual cumulative frequency error, where the NBS 1-Hz is used as the reference and the STD 1-Hz is used as the accumulator.

The frequency of the standard 10 MHz is adjusted by a control voltage which is provided by the D/A converter. The Central Processor, through the

frequency counter, will continuously make measurements of the standard 10 MHz. As frequency adjustments are required, the central processor will make them by changing the VCO control voltage fed to the oscillator from the D/A converter.

As a part of operating software, the central processor is required to periodically generate an output pulse to the Watchdog Timer. The Watchdog Timer will generate an alarm if the periodic pulses are not received. This provides a basic "sanity" check and alarm for the central processor.

Figure 4-11 is the schematic for the FTC board and Figure 4-12 is the assembly drawing. The following subsections discuss its functions.

4.5.1 CENTRAL PROCESSOR

The Central Processor portion of the FTC consists of: the 8031 microprocessor (U13), an address latch (U12), a Read Only Memory (U6), a Random Access Memory (U5), and an address decoder (U8). The 11.059 MHz crystal serves as the clock for the CPU. The CPU (U13) fetches instructions from the ROM (U6) by latching the low order address in U12, placing the high order address on pins 21 through 25, and reading the data bus on pins 32 through 39. The PSEN signal is used to gate the ROM data onto the data bus. The reading and writing of data to/from the RAM (U5) is similarly accomplished, however, the RD signal is used to gate data to the bus and the WR signal is used to latch data from the bus. The peripheral devices used by the CPU for various functional elements are accessed as external RAM by the CPU. Separate addressing of each of these peripheral devices is accomplished through the address decoder (U8), although instructions and data to have separate address space. The data space is shared with the peripheral devices. A summary of the address map is provided below:

Instruction Space

0000-1FFF	ROM (U6)

Data Space

0000-07FF	RAM (U5)
0800-0803	8254 Counter/Timer (U4)
0804-0807	8254 Counter/Timer (U3)
0808-080B	8254 Counter/Timer (U2)
080C-080F	8255 Parallel I/O (U7)
0810-0817	DAC1230 D/A Converter (U16)

Internal to the CPU is a UART and associated baud rate generator. This provides for the connection of a teleprinter for logging and control purposes. The baud is set by software based on the switch settings of U18-6 through U18-8. The serial data is output via TXD (U13-11) and converted to RS-232 levels via U23. Incoming serial data is converted. from RS-232 levels to TTL levels via U27 and input to the CPU-UART via RXD (U13-10).

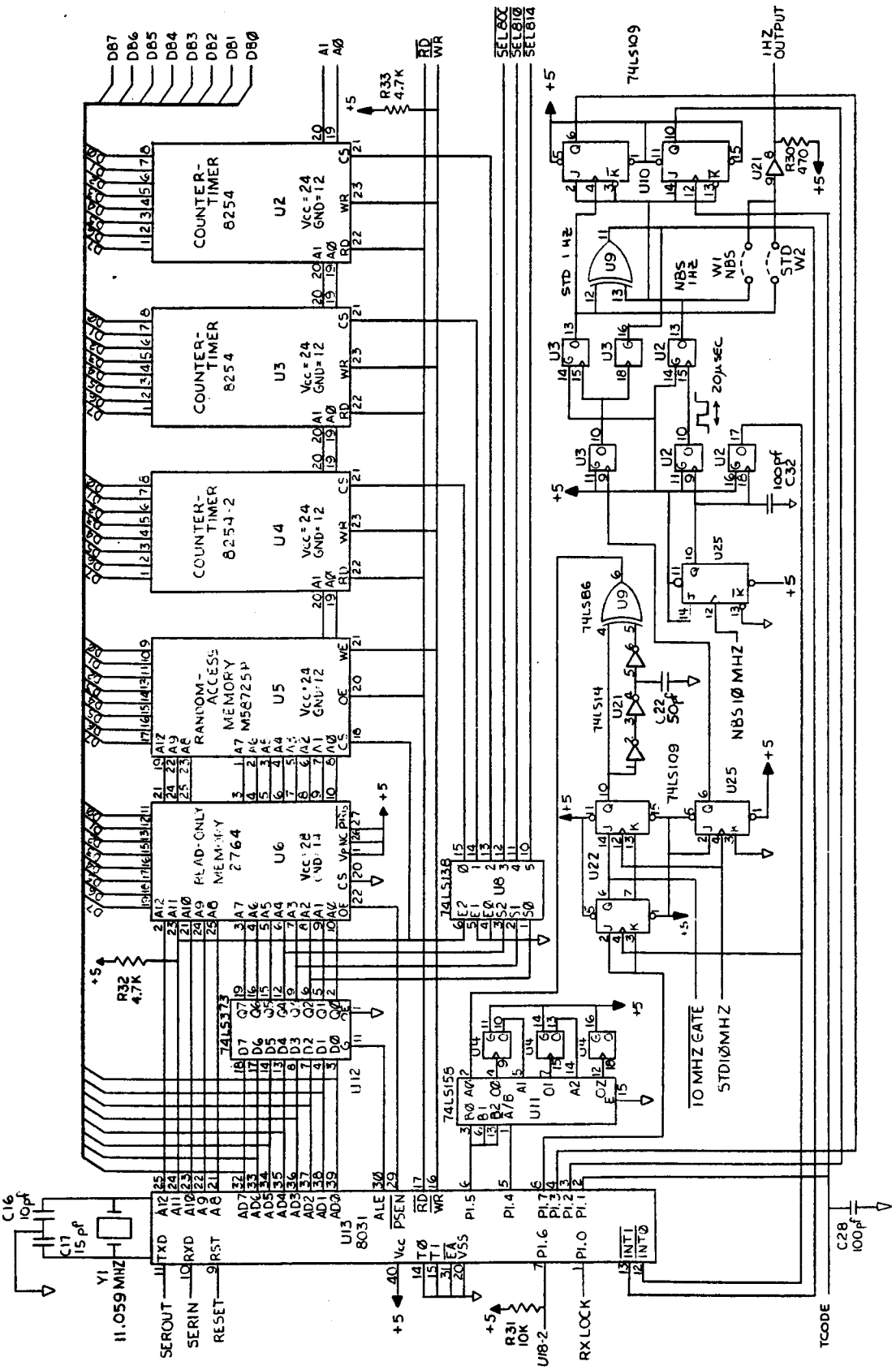


FIGURE 4-11 FTC A6 SCHEMATIC DIAGRAM SHEET 1 OF 2

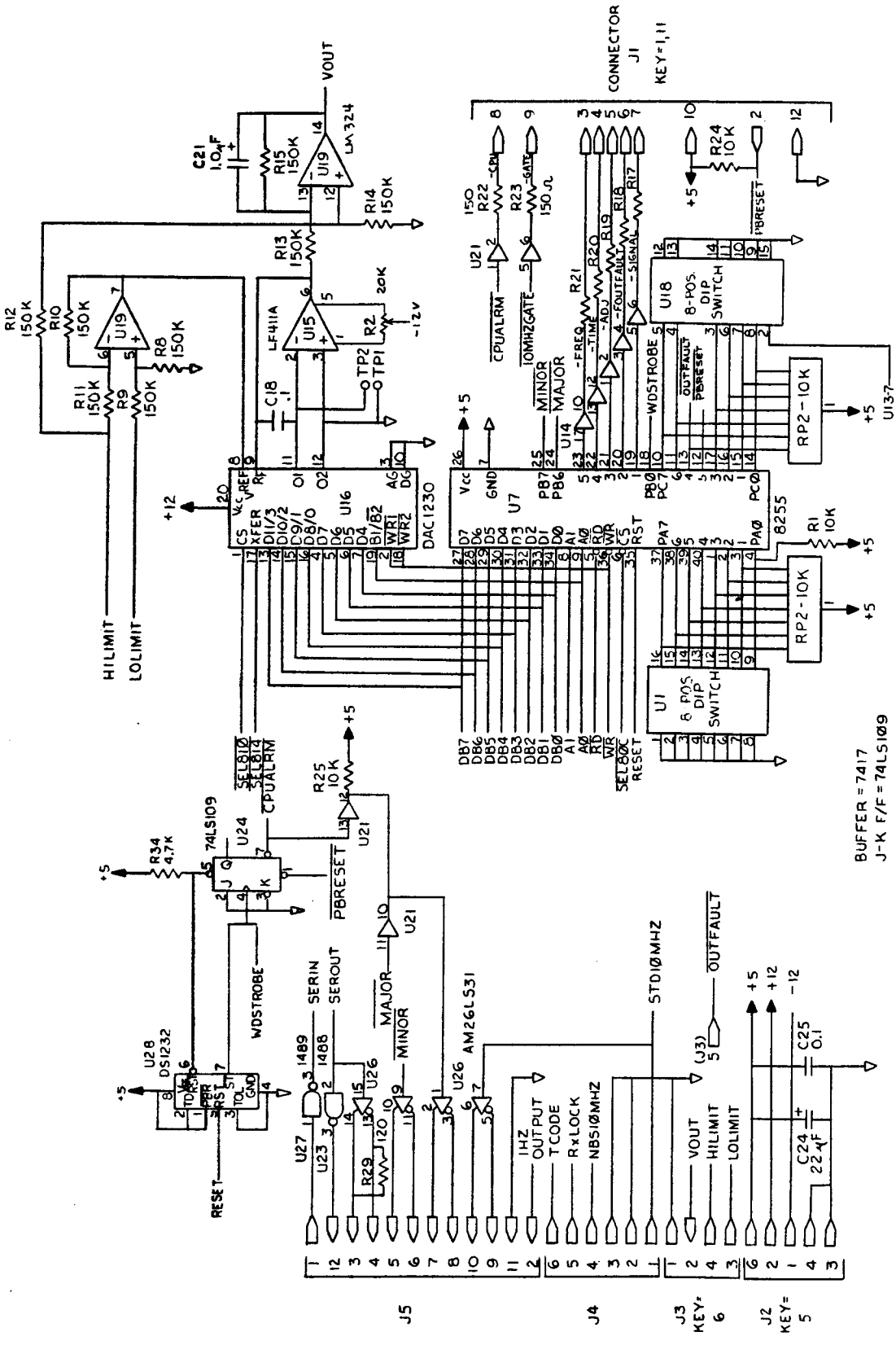


FIGURE 4-11 FTC A6 SCHEMATIC DIAGRAM SHEET 2 OF 2

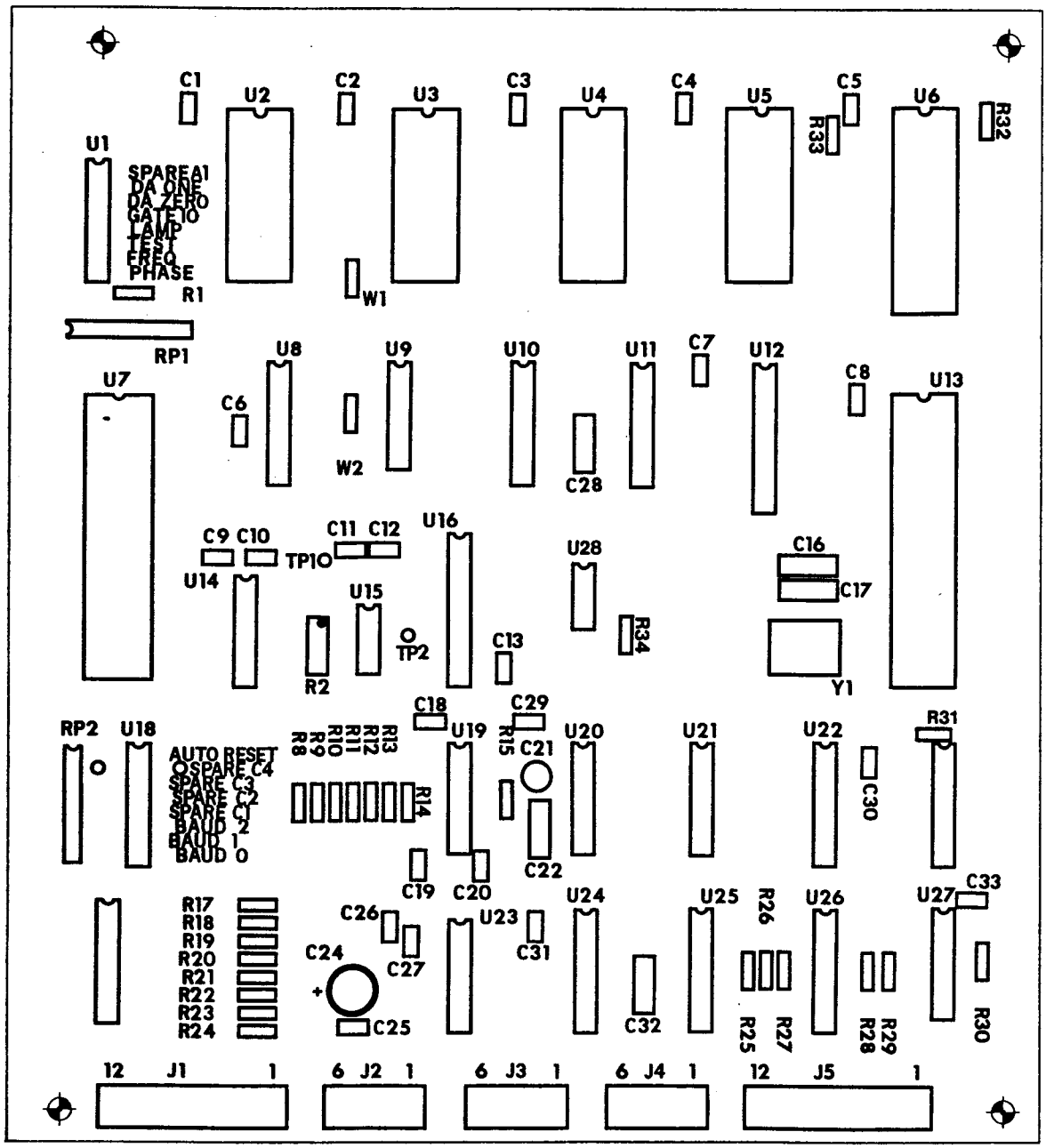


FIGURE 4-12 FTC A6 COMPONENT LOCATION DIAGRAM

There are two interrupt inputs to the CPU: NBS-5MS and PHASE DIFF INTR. The NBS-5MS is the Real-time Clock input which provides software with a time reference. PHASE DIFF INTR indicates each time a phase difference measurement has been completed between the NBS-1Hz and the STD-1Hz. This will occur twice per second, once for each half cycle of the NBS-1Hz and STD-1Hz.

The CPU directly reads the NBSHIGH (U13-3) and STDHIGH (U13-4) signals from the Phase Difference circuit. The NBSHIGH is high when the NBS-1Hz leads, in phase, the Time Code (TCODE) received from the WWVB receiver for the last sample. The STDHIGH is high when the NBS-1Hz leads the STD-1Hz for the last sample.

The CPU also reads the TCODE from the WWVB receiver for the purposes of determining the TCODE symbols received. This is input to the CPU at U13-2. The WWVB receiver locked condition is sensed by the CPU at U13-1.

Three outputs are provided by the CPU for Frequency Counter control: GATE (U13-8), LDCONTR (U13-5), and LDSTR (U13-6).

4.5.2 REAL-TIME CLOCK

The Real-time Clock (RTC) provides time reference information for the frequency counter. The NBS 10-MHz is first divided by two by the J-K F/F (U25). The resultant 5-MHz signal is fed to the 8254 Counter (U2-18) where it is divided by 25,000 to provide a 5-millisecond square wave output at U2-17.

4.5.3 FREQUENCY COUNTER

The Frequency Counter provides for the measurement of the STD 10-Mhz output frequency. The counter itself consists of an 8254 Counter (U4) with its three internal counting elements cascaded in series. The 10-MHz pulses are gated to the counter chain via the dual F/F arrangement of U22. To enable counting, the CPU activates the GATE line (U13-8) to J-K inputs, U22-2 and 3. Synchronous with the leading edge of the RTC, the GATE will be clocked to the outputs, U22-6 and 7. The CPU will hold the GATE open for the desired period, measured in units of 5 milliseconds. When the GATE is closed, the outputs will change with the subsequent leading edge of RTC.

When U22-14 is high and U22-13 is low, the J-K F/F output U22-10, is allowed to toggle with each leading edge of the STD 10-MHz provided to U22-12. The resultant 5-MHz wave-form when applied to the three inverters U21 and the EX-OR gate, U9, will cause a 10-MHz series of pulses to be output from U9. A pulse is generated for each transition of U22-10. Their width is defined by the propagation delay of the three inverters plus the added delay imposed by C22. This pulse shaping circuit is included pursuant to the clock shaping requirements of the 8254 when counting at a 10-MHz rate.

The output pulses of U9 are fed to the AND-OR multiplexer, U11-2. The multiplexer enables the three 8254 counters to be cascaded together or connected to the LDSTR (U13-6) output from the CPU. In order to zero the counters before opening the GATE to count the pulses, the CPU must load the counters with zero. The 8254's, however, will not load the zero count

until the first clock pulse. To satisfy this requirement, the CPU initializes the counters by placing a high on the LDCONTR line (U13-5) and pulsing the LDSTR (U13-6) line low. This provides the initializing clock pulse. The LDCONTR is then returned low, returning the counters to the cascaded configuration for counting the 10-MHz pulses.

4.5.4 NBS 1-HZ CLOCK

The NBS 1-Hz Clock is derived by dividing the NBS 10-MHz from the WWVB receiver. The phase of the NBS 1-Hz is continuously adjusted by the CPU to reflect an in-phase relationship with the "on-time" pulse transmitted by WWVB and received by the receiver. The NBS 10-MHz is fed through a J-K F/F (U25) where it is divided by two. The resultant 5-MHz clock is fed to a pre-scaling divider (U2-9) where it is further divided by 100 to provide a 50-kHz output at U2-10. The 50 kHz is fed to a final divider (U2-15) where it is divided by 50,000 to provide the NBS 1-Hz output at U2-13. The phase is adjusted under software control by periodically adjusting the 50,000 division factor up or down for one cycle of the divider.

4.5.5 PHASE DIFFERENCE COMPARATOR

The Phase Difference Comparator provides for the evaluation of phase differences between NBS 1-Hz/TCODE and NBS 1-HZ/STD 1-Hz.

The comparison between NBS 1-Hz and TCODE is only on the basis of their overall relationship (i.e. leading/lagging). This is accomplished by TCODE clocking a J-K F/F (U10-12) with the NBS 1-Hz as data input (U10-13 and 14). When the F/F output (U10-10) is high, NBS 1-Hz is leading, in phase, the TCODE sample.

The comparison between NBS 1-Hz and STD 1-Hz includes both the sign (leading/lagging) and the magnitude. The sign is derived by STD 1-Hz clock in a J-K F/F (U10-4) with the NBS 1-Hz serving as the data input (U10-2 and 3). A high at the F/F output, U10-6, indicates that NBS 1-Hz is leading. The magnitude is derived by EX-ORing the NBS-1Hz and the STD 1-Hz through U9-12 and 13. The resultant output, U9-11, is used at a gate for a counter, U3-16, and also as an interrupt to notify the CPU of available measurements. The counter receives 20 microsecond pulses at U3-18. Each time the gate goes high, the count is zeroed and the incoming pulses are counted. When the gate goes low, counting is disabled and the CPU is interrupted. The counter then reflects the magnitude of phase difference in 20 microsecond units.

4.5.6 D/A CONVERTER

The STD 10-MHz oscillator's frequency is voltage controlled. The frequency is controlled under software direction by programming an output voltage (VOUT) to the oscillator through the D/A Converter. The actual voltage range over which the CPU can program the voltage is established by two inputs to the FTC: LOLIMIT and HILIMIT. LOLIMIT serves as the lower voltage limit of adjustment while HILIMIT serves as the higher limit. These two inputs are fed to a differential amplifier (U19-5 through 7) which provides a negative voltage output to the DAC reference (U16-8) equal to the differential between LOLIMIT and HILIMIT. The DAC (U16) is

operated in the current mode. The Op Amp (U15) provides for the conversion of the DAC current into a voltage. The current-to-voltage conversion inverts the DAC output providing positive voltages at U15-6. The output of U15 is fed to a differential amplifier (U19-12 thru 14) which provides the VOUT as the differential between the programmed DAC voltage and the HILIMIT. Therefore, when the DAC is at its minimum numeric value, VOUT is equal to HILIMIT and when the DAC is at its maximum numeric value, VOUT is equal to LOLIMIT.

4.5.7 WATCHDOG TIMER

The Watchdog Timer and power monitor functions are performed by U28. Whenever Vcc falls below 4.75 volts, the reset outputs (Pins 5 and 6) become active. The reset signals also become active at power-on when Vcc reaches 4.75 volts.

As part of the FTC software, U7-18 provides the periodic pulses, WDSTROBE, to the strobe input U28-7. If a pulse is not received by U28-7 within 1.2 seconds, the last strobe the reset outputs will become active. When this occurs, the CPU alarm lamp will be latched on by F/F U24. Depressing the pushbutton reset will clear the CPU alarm.

4.5.8 MISCELLANEOUS I/O

There are a variety of miscellaneous I/O signals provided for by the parallel I/O interface, U7, and the open-collector buffers, U14 and U21. These signals fall into three categories: status inputs, status outputs, and switch options.

There are two status input: an oscillator output fault indication (OUTFAULT) and a pushbutton status reset (PBRESET). OUTFAULT is introduced to the FTC to indicate a failure in the STD 10-MHz. It is sampled at U7-13. A low level indicates a fault. The PBRESET is sampled at U7-12. A low level will cause status lamps to be reset under software control. This signal is also presented to U24-1 to reset the CPUALRM F/F.

The FTC provides a number of status output indications. The front panel indications include: CPU Alarm, GATE, SIGNAL, OUTFAULT, ADJOSC, TIME, and FREQ. The CPU Alarm is directly derived from the CPUALRM F/F (U24) and is buffered by U21 at pin 1 for open collector output on pin 2. GATE is directly driven by the frequency counter gate (U22-7) and buffered for output at U21-6. SIGNAL, OUTPUT FAULT, ADJ OSC, TIME, and FREQ are all derived by software and output via U7 pins 19 through 23, respectively.

These outputs are buffered by U14 with open collector outputs and current limiting resistors. Rear panel indications include: MAJOR Alarm and MINOR Alarm. Both of these signals are derived by software and output via U7 pins 24 and 25, respectively. The MAJOR Alarm is wire-ORed with the CPUALRM via U21 pins 10 and 12. U26 provides RS-422 level outputs for MAJOR and MINOR.

The FTC includes a number of option switches which enable the user to control various operational characteristics of the FTC through its software. These switches (U1 and U18) are input to U7. Resistor packs,

RP1 and RP2, serve as pull-ups. The FTC response to each of these switches is under the control of the software. (Note: U18-1 and 2 are not input to U7.)

MODEL 8164

SECTION 5

OPTIONS AND ACCESSORIES

5.0 INTRODUCTION

This section describes the following options and accessories that are available for the Model 8164.

* Distribution Amplifier - Option 03
* Line Taps - Model 8140T and 8140TTL
* Line Extender Amplifier - Model 8140TA
* VersaTap™ Frequency Synthesizer Model 8140VT
* 10 Hz Channel Offset - Option 31
* SmartStart™ - Option 34
* Paging Offsets - Option 36
* Smaller Paging Offsets - Option 56
* WWVB Synchronized Clock - Model 8171A

Rack Mount (Option 01), Slides (Option 11), Antenna (Model 8206), Antenna Mount (Model 8211), and Preamplifier (Model 8207) are described in Section 1 of this manual.

5.1 OPTION 03 BUILT IN DISTRIBUTION AMPLIFIER

Option 03 allows counters and synthesizers throughout a facility to use the WWVB disciplined outputs from a Model 8164 as a common time base. Because equipment can share a common time base, there is no need to buy expensive, high stability time bases for each instrument or remove them from service for periodic calibration.

Units equipped with Option 03 may drive up to 25 remote stations. Multiple outputs are provided on the rear panel so that signals may be sent in several different directions. A line tap at each remote station receives DC power and the 10 MHz standard from the main coaxial trunk line cable. The signal is buffered then divided to the frequency needed at that station. After filtering, the signal is available at the line tap output. New stations are easily added to the system by inserting additional line taps.

5.1.1 SYSTEM COMPONENTS

A frequency distribution system may use Model 8140T or 8140TTL Line Taps, Model 8140VT VersaTap™s or an 8140TA Line Extender Amplifier. The following paragraphs describe each of these units.

5.1.1.1 MODEL 8140T AND MODEL 8140TTL LINE TAPS

These devices, powered by DC on the coaxial feed line, are attached to the coaxial distribution network and provide an output at one of 3 specified frequencies: 1, 5, or 10 MHz. The frequencies of 500 and 100 kHz are available at somewhat higher costs.

INPUT - Buffered high input impedance causes negligible mismatch on main trunk line distribution cable. Accepts signal levels provided by the base station equipped with Option 03.

OUTPUT LEVEL - Standard unit (Model 8140T) provides 600 mV rms sine wave into 50 ohms. When used without termination, the output is TTL compatible. Optional unit (Model 8140TTL) provides TTL compatible signals into loads greater than 100 ohms.

OUTPUT FREQUENCIES - 10, 5.0, 1.0, 0.5 or 0.1 MHz. Specify frequency for each Line Tap ordered.

HARMONIC DISTORTION OF OUTPUT - -40 dB for standard unit with sine wave output.

CROSSTALK (ISOLATION) - 80 dB minimum.

OUTPUT PHASE NOISE - Typically less than -130 dB/Hz 1 kHz from carrier for 10 MHz input to base station amplifier.

LINE TAP SIZE - In inches - 5.25 L x 2.63 W x 1.71 H. (In mm: 133 L x 67 W x 43 H). Mounting hole pattern: 4.75 x 1.75 inches (121 x 44 mm).

Each line tap bears a label showing its output frequency. Should this label be lost, the frequency can easily be determined using a frequency counter or oscilloscope.

5.1.1.2 MODEL 8140VT VERSATAP™ FREQUENCY SYNTHESIZER

The VersaTap™ is a single-frequency synthesizer whose output is factory-set to any frequency between 1 kHz and 16 MHz in 1-kHz increments and up to 20 MHz in 2 kHz increments. Some special frequencies can be furnished, such as the 3.5795454...MHz TV color sub-carrier. Exact frequencies must be specified at time of order.

INPUT - Buffered high impedance input. Accepts 10.0 MHz with signal level between 100 millivolts and 5.5 Vp-p on a DC voltage of 7 to 12 VDC. The DC current requirement is 150 milliamps at +12 VDC.

OUTPUT A - A sine wave of 600 mV rms at the specified frequency into a 50-ohm load for frequencies greater than 56 kHz. A TTL output for frequencies below 56 kHz.

OUTPUT B - A TTL output at the specified frequency. If the internal jumper, W6, is moved to location W5, Output B is HIGH when the VersaTap™ is phase locked to the incoming reference and LOW when it is unlocked.

LOCK LED - The LED will light when the VersaTap™ is locked to the incoming reference. The LED will blink if the DC input is low, which may cause the VersaTap™ to malfunction. The LED will be unlit when the VersaTap™ is not locked to the incoming reference.

VERSATAP™ SIZE - In inches 8.3 L x 4.2 W x 1.7 H. (In mm: 211 L x 107 W x 43 H). Mounting hole pattern 8.88 x 2.75 inches (225.4 x 69.9 mm).

5.1.1.3 MODEL 8140TA LINE EXTENDER AMPLIFIER

The Line Extender Amplifier must be used to boost the output signal when the coaxial distribution network is more than 1500 feet (457 m) long. The Line Extender will drive an additional 1500-feet (457 m) of RG-58 coaxial cable with Model 8140T Line Taps installed along its length.

Two DC-isolated 50-ohm terminators must be used: one at the input tee connector of the Line Extender Amplifier and one at the far end of the cable connected to the output of the Line Extender Amplifier.

See the "Typical Interconnection Diagram" Figure 5-2, for an approved method of interconnection.

5.1.2 DESIGN OF DISTRIBUTION NETWORKS

This section provides guidelines for using the Option 03 distribution outputs. In planning a system installation follow the guidelines listed below:

1. A maximum of 25 line tap loads may be driven from one base station. More than 25 loads is not permitted due to power supply limitations and impedance matching. Table 5-1, Line Tap Loads, lists the equivalent number of loads and current each distribution device consumes. The receiver may provide up to 1.2 amps total to the distribution network.

DEVICE	LOADS	CURRENT (mA)
8140T All Versions	1	45
8140TA	1	45
8140VT Standard	3	150
8140VT w/Opt 45	5	250
8140VT w/Opt 48	4	200
8140VT w/Opt 58	4	200

TABLE 5-1 LINE TAP LOADS

If more than 25 line tap loads are required you may:

Add a Model 8140 Frequency Distribution Amplifier. The Model 8140 contains an internal power supply and will feed an additional 25 line tap loads. A line tap is required (typically 10 MHz) to provide the input frequency source to the Model 8140. This "Daisy Chaining" may be continued indefinitely.

2. Because of voltage drops and signal attenuation the longest trunk line using RG-58 cable is 1500 feet (457 m). Figure 5-1, Line Tap Number and Distance Chart, is used to calculate the number of line tap loads that may be used at various distances from the base station.

For example, if 25 line taps are used, their average distance from the amplifier is limited to 750 feet (228 m), using RG-58. Up to 12 line taps may be placed at 1500 feet (457 m) on any one trunk line.

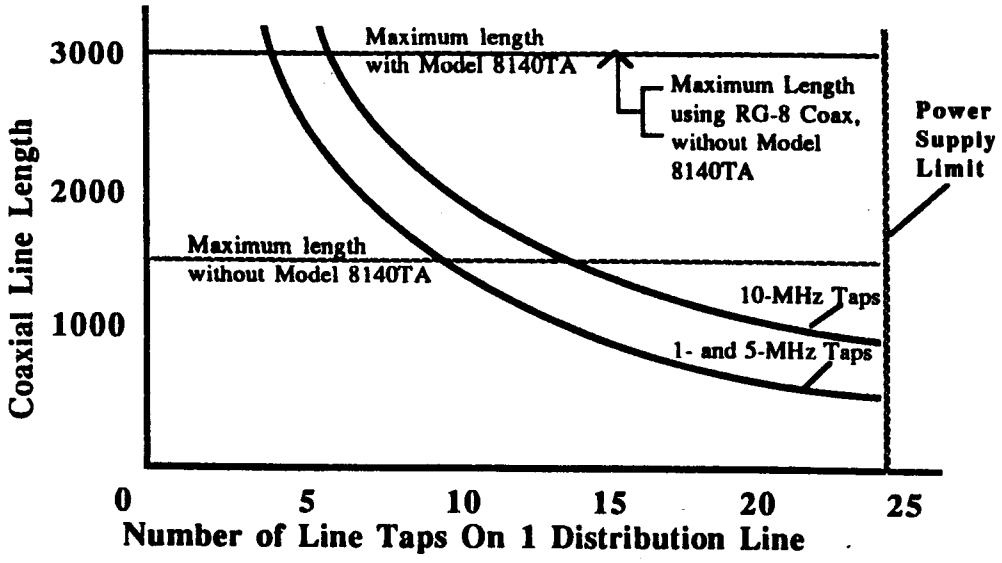


FIGURE 5-1 LINE TAP NUMBER AND DISTANCE CHART - OPTION 03

If longer runs are required, you may:

A. Locate the Model 8164 in the geographical center of the installation, running distribution lines in both directions and achieving a coverage of 3000 linear feet (914 m).

B. Use a Model 8140TA Line Extender Amplifier at 1500 feet, allowing a further 1500-foot (457 m) extension of the distribution line. The Model 8140TA counts as one line tap load towards the total number allowed. Use a 50 ohm DC isolated terminator, part number 004490, at the input tee connector and at the end of the extended line section as shown in the "Typical Interconnection Diagram", Figure 5-2.

C. Use a Model 8140 Frequency Distribution Amplifier.

3. Each distribution line must be continuous from the base station to the DC isolated 50 ohm load that must be used at the far end. Line taps are inserted along the distribution line by using the supplied input tee connector. No branching or "Y" configurations may be used as this causes impedance mismatch on the line. Anything other than a 50 ohm line impedance may cause reflections which can cancel the output wave-form at the receiver triggering the OUTPUT FAULT lamp. Refer to the Typical Interconnection Diagram, Figure 5-2 for an approved method of interconnection.

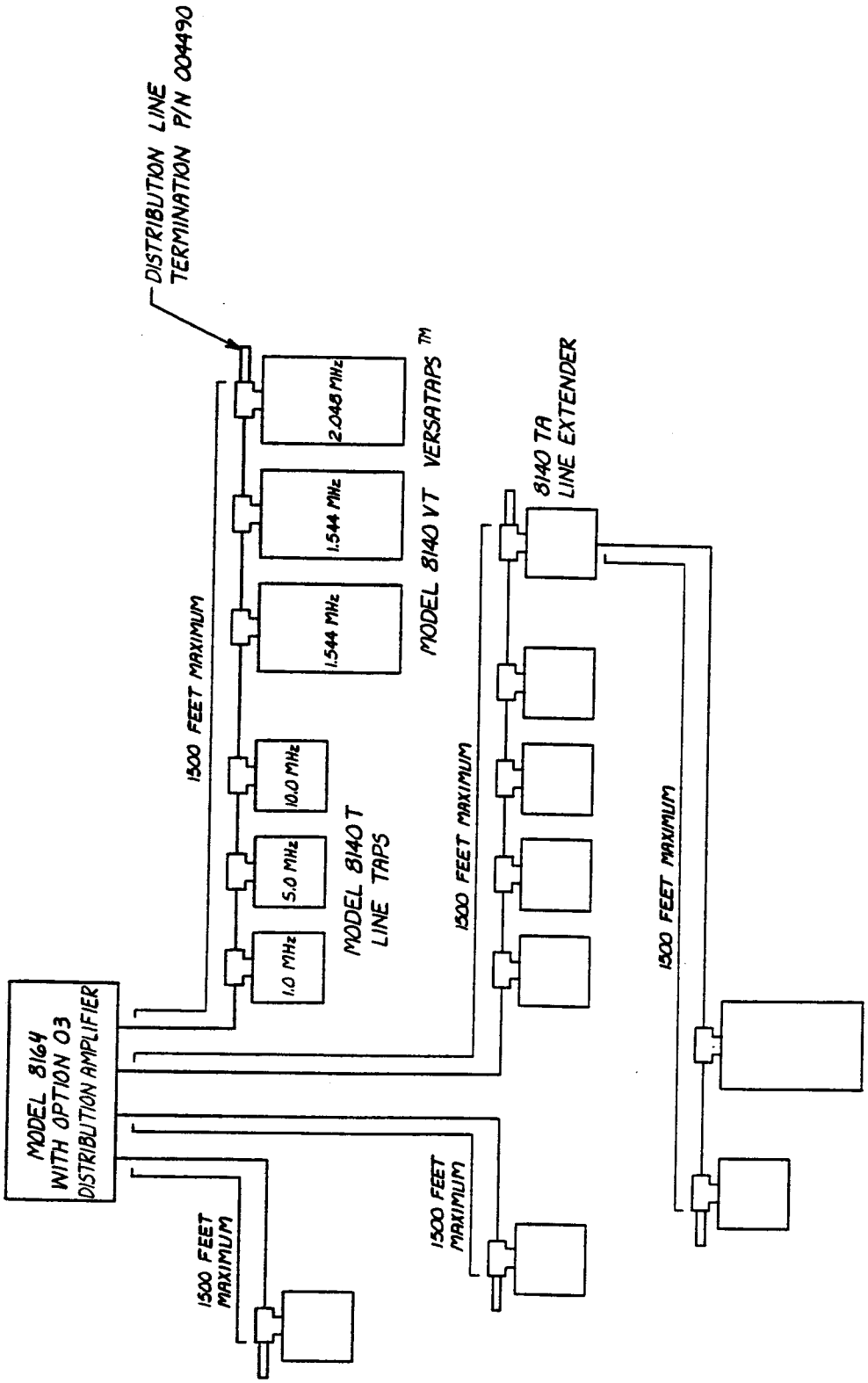


FIGURE 5-2 TYPICAL INTERCONNECTION DIAGRAM

4. Four DC-isolated 50 ohm loads are furnished with each unit equipped with Option 03. They may be found in the ancillary kit that is packed with each unit when it leaves the factory. If any of these loads are lost, spares may be purchased from Spectracom. The part number to order is 004490. Terminators may be placed on any unused distribution output connector to prevent loss.

5. We recommend that, wherever practical, the line taps be permanently mounted to a lab bench or wall nearby. This avoids their loss or misplacement and discourages people from occasionally disconnecting them, thus cutting off the signal to stations further down the line.

6. Never directly connect a distribution line to an instrument; always use a line tap or VersaTap™. Doing so may damage the instrument or cause an impedance mismatch on the distribution line.

5.1.3 PRINCIPLES OF OPERATION

The schematic for Option 03 is shown in Figure 5-3, "Distribution Amplifier A4 Schematic Diagram." The Component Location Diagram is Figure 5-4. The board is located on the rear panel behind the ovenized oscillator assembly. The distribution amplifier assembly is referred to as the A4 board.

The distribution output frequency source is the hi-stability ovenized oscillator. The 10 MHz output from the ovenized oscillator is fed to the A4 board on J1 Pin 10. The signal is first buffered and amplified by Q1 and Q2. The signal then passes through gates U1A and U1B where the signal is split in two directions. One direction is through the dividers U5, U6 and U7. The divided outputs are fed to gates U4, U3, and U2 and are selectively fed to the font panel standard output jack, according to the front panel pushbutton selector switches.

The other direction is through U4C and into line drivers U8 and U9. The signal is then filtered to a sine wave and a 12 volt DC offset added. The signal is then fed to each of the rear panel connectors.

The presence of output signal at each of these rear panel jacks is detected by a diode/capacitor combination at each output jack and used as a signal for front panel indication of output fault. Detector outputs at all four jacks are gated together through diodes CR5, CR9, CR13, CR17 and fed to a transistor switch consisting of Q5, Q4, and Q3 which lights the OUTPUT FAULT lamp in the absence of output signal.

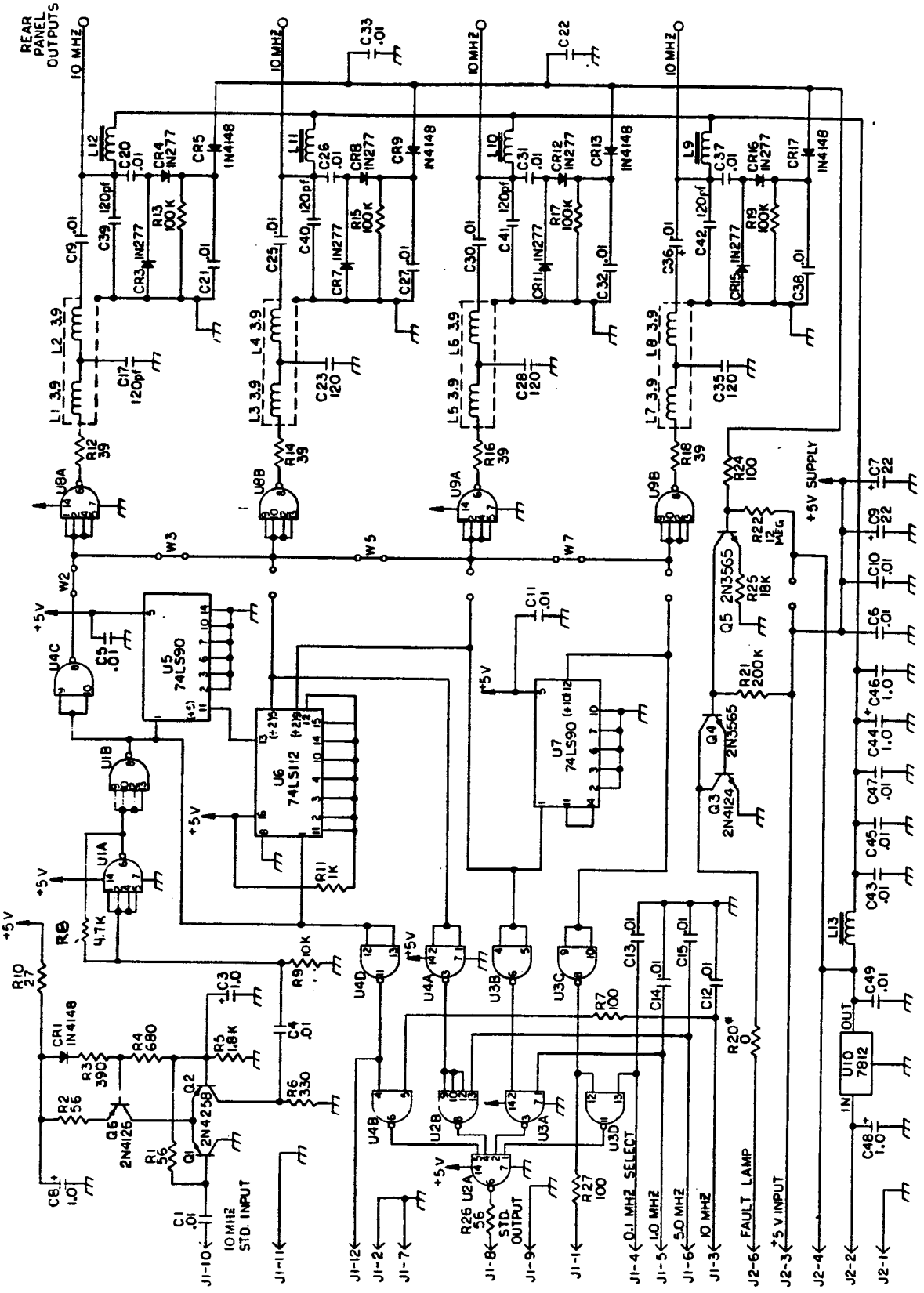


FIGURE 5-3 DISTRIBUTION AMPLIFIER A4 SCHEMATIC DIAGRAM

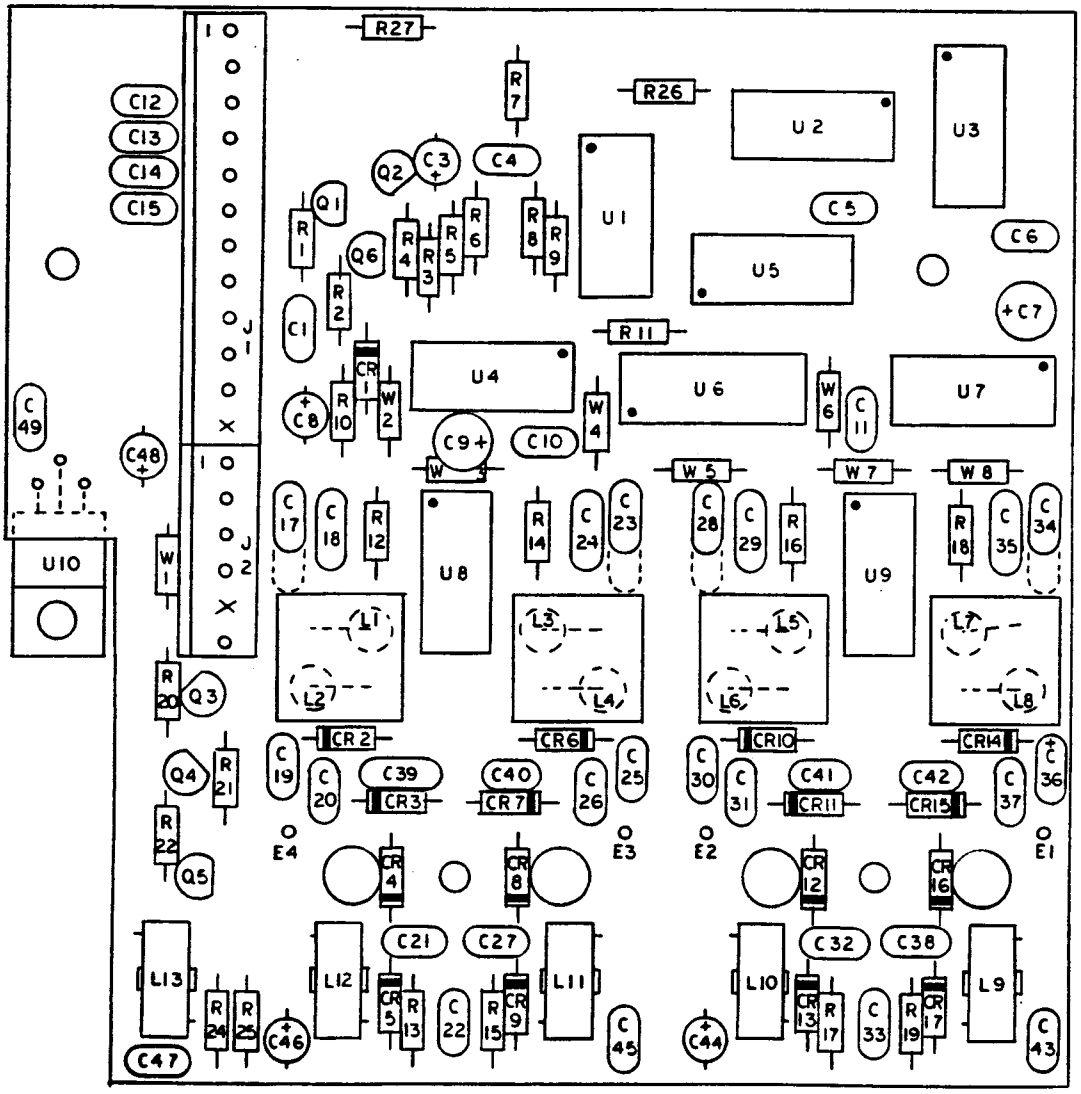


FIGURE 5-4 DISTRIBUTION AMPLIFIER A4 COMPONENT LOCATION DIAGRAM

5.2 OPTION 31 - 10-HZ CHANNEL OFFSET

To avoid interference between TV stations operating on the same frequency, geographical separation and radiated powers are carefully selected. Nevertheless, considerable co-channel interference has been encountered.

Co-channel interference between TV stations appears to viewers as a horizontal pattern of alternating light and dark bars much like the shadows cast by venetian blinds. The visibility of these bars varies cyclically as a function of the difference frequency of the interfering carriers.1

Co-channel interference can be minimized if the transmitter frequencies are tightly controlled. To minimize the interference, the visual carrier of an interfering station is offset by either plus or minus 10,010 Hz. The 10-kHz offset and the direction (i.e. plus or minus) is assigned by the FCC. This offset is normally provided in the transmitter. The Model 8164 Disciplined Oscillator with Option 31 provides a precise 10 MHz standard with offset control that, when translated to the visual carrier frequency results in an additional 10 Hz offset.

5.2.1 OPERATION

The internal dip switches A6U1-1 labeled Spare A1 and A6U18- 2,3,4,5 labeled Spare C4, Spare C3, Spare C2, and Spare C1, control the 10 MHz offset. Table 5-2 Frequency Offset Table, lists the frequency as a function of switch setting for each of the VHF-TV channels.

For TV Channel 2 with a plus 10 kHz offset, place A6U1-1 Spare A1 and A6U18-4 Spare C2 in the ON position and A6U18-2, 3 and 5 in the OFF position. This selects a frequency of 10,000,001.810 Hz for the 10 MHz standard, providing an additional 10 Hz offset at visual carrier frequency.

When shipped from the factory, the unit is set to the frequency specified on the serial number tag. If a different selection is required, remove the top cover and select the new frequency.

The frequency correcting switch, A6U1-7, must be on to allow the unit to frequency lock. An offset may be entered without removing power. Once an offset is entered, the FREQ lamp will latch on. The RESET button will clear the frequency alarm lamp when the unit synchronizes to within 1.0 E-8 of the expected frequency. This typically takes 3-4 hours under good signal conditions.

The offset frequency is available on the four rear panel outputs and the front panel STANDARD OUTPUT. The outputs provided are 0.1, 1.0, 5.0, and 10 MHz. Each is derived from the Disciplined 10 MHz Oscillator and is offset proportionally. A positive channel 6 offset yields 10,000,001.201 Hz on the 10 MHz output and 5,000,000.600 on the 5 MHz output.

1. "Precise Frequency Control, Theory and Practice" by J.L. Klecker and A.H. Bott, Engineering Report, Harris Corporation, Broadcast Division, 123 Hampshire Street, Quincy, Illinois 62301.

Units equipped with Option 03, Built-In Distribution Amplifier, change the four rear panel outputs to provide the offset 10 MHz signal on a 12 VDC level.

NOTE: The strip chart recorder displays the phase comparison of the Disciplined Oscillator to the received WWVB signal. The offset frequencies of Option 31 are too large for the chart recorder to obtain a meaningful recording. To conserve on chart paper, turn the recorder off.The strip chart recorder can still be used to calibrate a local input to the WWVB reference.

TABLE 5-2 FREQUENCY OFFSET TABLE

	SWITCH A6U18				FREQUENCY - Hz		
CHNL	-2 C4	-3 C3	-4 C2	-5 C1	PLUS OFFSET A6U1-1 = ON	MINUS OFFSET A6U1-1 = OFF	RELATIVE FREQUENCY
2	0	0	1	0	10,000,001.810	9,999,998.190	181.0 X 10^{-9}
3	0	0	1	1	10,000,001.632	9,999,998.367	163.2 X 10^{-9}
4	0	1	0	0	10,000,001.487	9,999,998.513	148.7 X 10^{-9}
5	0	1	0	1	10,000,001.294	9,999,998.706	129.4 X 10^{-9}
6	0	1	1	0	10,000,001.201	9,999,998.799	120.1 X 10^{-9}
7	0	1	1	1	10,000,000.571	9,999,999.429	57.1 X 10^{-9}
8	1	0	0	0	10,000,000.552	9,999,999.448	55.2 X 10^{-9}
9	1	0	0	1	10,000,000.534	9,999,999.466	53.4 X 10^{-9}
10	1	0	1	0	10,000,000.517	9,999,999.483	51.7 X 10^{-9}
11	1	0	1	1	10,000,000.502	9,999,999.498	50.2 X 10^{-9}
12	1	1	0	0	10,000,000.487	9,999,999.513	48.7 X 10^{-9}
13	1	1	0	1	10,000,000.473	9,999,999.527	47.3 X 10^{-9}

SWITCH A6U1 & A6U18
1 = ON; 0 = OFF

5.2.2 PRINCIPLES OF OPERATION

The Model 8164 operates on a "frequency locking" principal. The frequency of the 10 MHz standard oscillator is measured and control voltage corrections applied to bring it to the desired frequency. The time base for the measurement is derived from the received WWVB signal. The measurement interval is 1000 seconds. The measurement resolution is 1.0 E-10 . The adjustment resolution is 2.4 E-10. The long term accuracy is typically ±1.0 E-9.

5.2.3 OFFSET PERFORMANCE TEST

Place the comparator switch on the front panel in the STANDARD OUTPUT position. The chart recorder on the front panel measures phase drift of the internal 10 MHz standard relative to the NBS phase-locked 10 MHz. With the front panel switch labeled Recorder EXP not depressed, the full scale represents 50 microseconds.

Table 5-3, Phase Comparator Movements, lists the time it takes for the needle to move 50 microseconds for each of the channel settings. The needle will move left to right for positive offsets and right to left for negative offsets.

Prior to performing this test, the Model 8164 must be phase-locked to WWVB and in continuous operation for at least 24 hours.

TABLE 5-3 PHASE COMPARATOR MOVEMENTS

CHANNEL	PHASE COMPARATOR MOVEMENTS MIN/50 MICROSECONDS
2	4:36
3	5:07
4	5:35
5	6:28
6	6:56
7	14:35
8	15:06
9	15:37
10	16:07
11	16:36
12	17:07
13	17:37

The needle will travel the 50 microseconds right to left (full-scale) in 17 minutes and 7 seconds for Channel 12 minus. The absolute frequency is 9,999,999.513 Hz, resulting in an additional negative 10 Hz offset at the visual carrier frequency. The other channels can also be easily checked.

Perform this measurement a few times to obtain an average value. The relative frequency is determined from the formula:

$$F = \frac{\Delta t}{T}$$

Where: F = Relative Frequency

Δt = Amount of phase change expressed in seconds. The full-scale deflection represents 50 microseconds (50 E-6 seconds).

T = Time interval expressed in seconds over which the the phase change occurred.

Compare the relative frequency obtained with the average time measurement with values in Table 5-2.

5.3 OPTION 34 - SMARTSTART™

Option 34, SmartStart™, enables the Model 8164 to quickly recover after a power loss. A non-Option 34 unit would require a 1-3 hour re-synchronization period after a power failure. This is because the oscillator control value is lost and defaulted to an average value at power on. Also, the oscillator requires a warm-up period whenever the oscillator power is interrupted. Option 34 provides a non-volatile RAM to retain the oscillator control value and a back-up oscillator supply to allow the unit to be "ON" frequency when line power returns.

5.3.1 BATTERY CONSIDERATIONS

5.3.1.1 NON-VOLATILE STATIC RAM

The non-volatile static RAM in location A6U5 contains a lithium battery with an expected life of ten years from date of manufacture. The four digit date code, YYWW, is located on top of the chip. The manufacture year is designated by YY, the manufacture week is designated by WW.

If the lithium battery is depleted, the lamp labeled FREQ STATUS ALERT will illuminate on the front panel after unit power-on. The unit will function as a standard Model 8164 without Option 34. When this occurs, replace the non-volatile RAM, Spectracom part number U01220.

5.3.1.2 OSCILLATOR BACK-UP SUPPLY

With this option, the oscillator will continue to run for up to 36 hours after power line failure. This prevents the oscillator from ever being turned off and avoids settling and retrace aging problems when the power returns. The battery contained in the option is float-charged continuously as long as the power line is connected to the unit. The battery pack contains sealed lead-acid cells that require no maintenance. Note that although the oscillator and oven are kept running by the battery during power failures, the signal is not available for use because the amplifier stages are turned off to conserve battery power.

The battery power supply has capacity for 36 hours of minimum standby operation. Recharge rates, 33% in 6 hours, 66% in 12 hours, 100% in 36 hours. The batteries have an eight year float life expectancy.

> NOTE: The internal battery has been disconnected for shipment by placing the rear panel battery selector switch in the "EXT" position. To re-connect the battery, return the switch to the "INT" position.
>
> The internal battery will maintain power to the oscillator for 36 hours. If the unit will be disconnected from AC power for more than 36 hours, place the rear panel selector switch in the "EXT" position.
>
> If the unit is returned to the factory for repair, place the rear panel battery select switch in the "EXT" position.

5.3.2 PRINCIPLES OF OPERATION

The control voltage for the voltage-controlled ovenized oscillator is provided by a 12-bit D/A converter on printed circuit board A6. The 12-bit D/A word is stored in non-volatile RAM (A6U5), along with a 32-bit pseudo-random bit pattern. At power-on, the 32-bit pattern is compared against a stored replica to verify that the RAM has not lost data. The D/A word is read and the control voltage to the oscillator is returned to the value prior to power failure.

If the power has been maintained to the oscillator oven by the oscillator battery, then the oscillator will remain on frequency during long power failures. During long power failures, there will be a small frequency offset due to crystal aging. This will be automatically corrected in one to three hours.

If at power-on, the 32-bit pseudo-random pattern read does not match the stored replica, then a default value for the D/A converter will be read from the EPROM. The STATUS ALERT lamp labeled FREQ will be illuminated.

The battery charging circuit is described Section 4.4.2 of this manual.

5.4 OPTION 36 - PAGING TRANSMITTER OFFSETS

In radio paging systems, it is desirable to cover large geographic areas with multiple radio paging transmitters. To operate such systems, a technique, referred to as "simulcasting," is generally employed. Simulcasting requires precise control of transmitter frequencies to reduce interference between adjacent transmitters on the same radio paging channel.

Ineffective transmitter frequency control can reduce system coverage and cause "dead spots," "false pages," and message distortion. These adverse effects are reduced or eliminated by providing a carrier frequency offset between adjacent transmitters. The offset values are selected to minimize co-channel interference. To assure maximum performance of the paging system, the effects of transmitter oscillator "aging" must be neutralized by periodically checking and adjusting the transmitter oscillators to maintain the desired frequency offsets.

The SPECTRACOM MODEL 8164 with Option 36, PAGING TRANSMITTER OFFSETS provides an accurate, controlled frequency reference which is "frequency locked" to the National Bureau of Standards. This reference can be used by synthesized paging transmitters to provide "ageless" frequency control, including offsets, to within one part per billion.

5.4.1 OPERATION

A frequency offset is entered into the Model 8164 by dip switches A6U1-1 and A6U18-2,3,4,5. Table 5-4, Frequency Offsets, lists the frequency of the 10-MHz standard as a function of switch settings.

The frequency correction switch, A6U1-7, must be on to allow the unit to frequency lock. An offset may be entered without removing power. Once an offset is entered, the FREQ lamp will latch on. The reset button will clear the lamp when the unit synchronizes to within 1.0 E-8 of the expected frequency. This typically takes 3-4 hours under good signal conditions.

The offset frequency is available on the four rear panel outputs and the front panel standard output. The outputs provided are 0.1, 1.0, 5.0 and 10 MHz. Each is derived from the Discipline 10 MHz Oscillator and is offset proportionally. A positive channel 5 offset yields 10,000,000.397 Hz on the 10 MHz connector and 5,000,000.198 on the 5 MHz output.

Units equipped with Option 03, Built-In Distribution Amplifier change the four rear panel outputs to provide the offset 10 MHz signal on a 12 VDC level.

> NOTE: The strip chart recorder displays the phase comparison of the Disciplined Oscillator to the received WWVB signal. The offset frequencies of Option 36 are too large for the chart recorder to obtain a meaningful recording. Channel 1 and 2 should produce usable recordings but the other channels will not and the chart recorder should be turned off to conserve chart paper. The strip chart recorder can still be used to calibrate a local input to the WWVB reference.

TABLE 5-4 FREQUENCY OFFSETS

CHNL	SWITCH A6U18 -2 -3 -4 -5 C4,C3,C2,C1	FREQUENCY (in hertz) POS. OFFSET A6U1-1 = ON	NEG. OFFSET A6U1-1 = OFF	RELATIVE FREQUENCY ΔfS
0	0000	10,000,000.000	10,000,000.000	0.0
1	0001	10,000,000.066	9,999,999.934	6.6×10^{-9}
2	0010	10,000,000.132	9,999,999.868	13.2×10^{-9}
3	0011	10,000,000.199	9,999,999.801	19.2×10^{-9}
4	0100	10,000,000.265	9,999,999.735	26.5×10^{-9}
5	0101	10,000,000.331	9,999,999.669	33.1×10^{-9}
6	0110	10,000,000.397	9,999,999.603	39.7×19^{-9}
7	0111	10,000,000.464	9,999,999.536	46.4×10^{-9}
8	1000	10,000,000.530	9,999,999.470	53.0×10^{-9}
9	1001	10,000,000.596	9,999,999.404	59.6×10^{-9}
10	1010	10,000,000.662	9,999,999.338	66.2×10^{-9}
11	1011	10,000,000.728	9,999,999.272	72.8×10^{-9}
12	1100	10,000,000.795	9,999,999.205	79.5×10^{-9}
13	1101	10,000,000.861	9,999,999.139	86.1×10^{-9}
14	1110	10,000,000.927	9,999,999.073	92.7×10^{-9}
15	1111	10,000,000.993	9,999,999.007	99.3×10^{-9}

5.4.2 FREQUENCY OFFSET AT THE CARRIER FREQUENCY

The frequency offset at the carrier frequency is determined by the formula

$$\Delta fc = Fc \times \Delta fs$$

where: Δfc = carrier offset

Fc = carrier frequency

Δfs = offset of 10-MHz standard (from Table 5-4)

Table 5-5, OFFSET AT VHF AND UHF BANDS, lists the frequency offset in Hertz as a function of switch setting for the VHF and UHF bands.

TABLE 5-5 OFFSET AT VHF AND UHF BANDS (IN HERTZ)

NOTE: Offset is positive when A6U1-1 is on, and offset is negative when A6U1-1 is off.

	SWITCH A6U18	OFFSET (in hertz)			
	-2 -3 -4 -5	-------VHF-------		-------UHF------	
CHANNEL	C4,C3,C2,C1	132 MHz	170 MHz	440 MHz	480 MHz
0	0000	0	0	0	0
1	0001	0.87	1.12	2.90	3.17
2	0010	1.74	2.24	5.80	6.34
3	0011	2.63	3.38	8.76	9.55
4	0100	3.50	4.50	11.66	12.72
5	0101	4.37	5.63	14.57	15.89
6	0110	5.24	6.75	17.47	19.06
7	0111	6.12	7.89	20.42	22.27
8	1000	7.00	9.01	23.32	25.44
9	1001	7.87	10.13	26.22	28.61
10	1010	8.74	11.25	29.13	31.78
11	1011	9.61	12.38	32.03	34.94
12	1100	10.49	13.52	34.98	38.16
13	1101	11.37	14.64	37.88	41.33
14	1110	12.24	15.76	40.79	44.50
15	1111	13.11	16.88	43.69	47.66

5.4.3 PRINCIPLES OF OPERATION

The Model 8164 operates on a "frequency locking" principal. The frequency of the 10 MHz standard oscillator is measured and control voltage corrections applied to bring it to the desired frequency. The time base for the measurement is derived from the received WWVB signal. The measurement interval is 1000 seconds. The measurement resolution is 1.0 E-10. The adjustment resolution is 2.4 E-10. The long term accuracy is typically $\pm$1.0 E-9.

5.4.4 OFFSET PERFORMANCE TEST

Place the comparator switch on the front panel in the STANDARD OUTPUT position. The chart recorder on the front panel measures phase shift of the internal 10 MHz standard relative to the NBS phase-locked 10 MHz. With the front panel labeled Recorder EXP not depressed, the full scale represents 50 microseconds.

Table 5-6, Phase Comparator Movements, lists the time it takes for the needle to move 50 microseconds for each of the channel settings. The needle will move slowly from left to right for positive offsets and from right to left for negative offsets. When the end of the scale is reached, the needle will return to the other end and resume its slow travel in the same direction.

Prior to performing this test, the Model 8164 must be phase-locked to WWVB and in continuous operation for at least 24 hours.

TABLE 5-6 PHASE COMPARATOR MOVEMENTS
(50 microseconds full-scale setting)

CHANNEL	HH:MM:SS
0	--
1	02:06:26
2	01:03:08
3	00:41:53
4	00:31:27
5	00:25:11
6	00:20:59
7	00:17:58
8	00:15:43
9	00:13:59
10	00:12:35
11	00:11:27
12	00:10:29
13	00:09:41
14	00:08:59
15	00:08:24

The needle will travel the 50 microseconds from left to right (full-scale), in 20 minutes and 59 seconds for positive offset channel 6. The absolute frequency is 10,000,000.397 Hz. The other channels can be checked in a similar manner.

Perform this measurement a few times to obtain an average value. The relative frequency is determined from the formula:

$$F = \frac{\Delta t}{T}$$

Where: F = Relative Frequency

Δt = Amount of phase change expressed in seconds. The full-scale deflection represents 50 microseconds (50 E-6 seconds).

T = Time interval expressed in seconds over which the the phase change occurred.

Compare the relative frequency obtained with the average time measurement with values in Table 5-4.

5.5 OPTION 56 - SMALLER PAGING OFFSETS

In radio paging systems, it is desirable to cover large geographic areas with multiple radio paging transmitters. To operate such systems, a technique, referred to as "simulcasting," is generally employed. Simulcasting requires precise control of transmitter frequencies to reduce interference between adjacent transmitters on the same radio paging channel.

Ineffective transmitter frequency control can result in reduced system coverage and cause "dead spots," "false pages," and message distortion. These adverse effects are reduced or eliminated by providing a carrier frequency offset between adjacent transmitters. The offset values are selected to minimize co-channel interference. To assure maximum performance of the paging system, the effects of transmitter oscillator "aging" must be neutralized by periodically checking and adjusting the transmitter oscillators to maintain the desired frequency offsets.

The SPECTRACOM NBS RECEIVER-DISCIPLINED OSCILLATOR MODEL 8164 with Option 56, PAGING TRANSMITTER OFFSETS, provides maximum maintenance. The Model 8164 provides an accurate, controlled frequency reference which is "frequency locked" to the National Bureau of Standards. This reference can be used by synthesized paging transmitters to provide "ageless" frequency control, including offsets, to within one part per billion.

5.5.1 OPERATION

A frequency offset is entered into the Model 8164 by dip switches A6U1-1 and A6U18-2,3,4,5. Table 5-7, Frequency Offsets, lists the frequency of the 10 MHz standard as a function of switch settings. The positive offset column shows that for Channel 0, a precise 10.0 MHz frequency is provided. For Channel 1, the frequency is 10,000,000.011 Hz. For Channel 15, the frequency is 10,000,000.166 Hz.

The frequency correction switch, A6U1-7, must be on to allow the unit to frequency lock. An offset may be entered without removing power. Once an offset is entered, the FREQ lamp will latch on. The RESET button will clear the lamp when the unit synchronizes to within 1.0 E-8 of the expected frequency. This typically takes 3-4 hours under good signal conditions.

The OFFSET FREQUENCY is available on the four rear panel outputs and the front panel STANDARD OUTPUT. The outputs provided are 0.1, 1.0, 5.0, and 10 MHz. Each is derived from the Disciplined 10 MHz Oscillator and is offset proportionally. A positive channel 6 offset yields 10,000,000.066 Hz on the 10 MHz connector and 5,000,000.033 on the 5 MHz output.

Units equipped with Option 03, Built-In Distribution Amplifier, change the four rear panel outputs to provide the offset 10 MHz signal on a 12 VDC level.

> NOTE: The strip chart recorder displays the phase comparison of the Disciplined Oscillator to the received WWVB signal. The offset frequencies of Option 56 will cause the resultant chart recording to slope from left to right for positive offsets and right to left for negative offset. The slope becomes more pronounced with the higher channel offsets.

TABLE 5-7 FREQUENCY OFFSETS

CHANNEL	SWITCH A6U18 -2 -3 -4 -5 C4,C3,C2,C1	FREQUENCY (in hertz) POSITIVE OFFSET A6U1-1 = ON	NEGATIVE OFFSET A6U1-1 = OFF	RELATIVE FREQUENCY ΔfS
0	0000	10,000,000.000	10,000,000.000	0.0
1	0001	10,000,000.011	9,999,999.989	1.1×10^{-9}
2	0010	10,000,000.022	9,999,999.978	2.7×10^{-9}
3	0011	10,000,000.033	9,999,999.967	3.3×10^{-9}
4	0100	10,000,000.044	9,999,999.956	4.4×10^{-9}
5	0101	10,000,000.055	9,999,999.945	5.5×10^{-9}
6	0110	10,000,000.066	9,999,999.934	6.6×10^{-9}
7	0111	10,000,000.077	9,999,999.923	7.7×10^{-9}
8	1000	10,000,000.088	9,999,999.912	8.8×10^{-9}
9	1001	10,000,000.099	9,999,999.901	9.9×10^{-9}
10	1010	10,000,000.111	9,999,999.889	11.1×10^{-9}
11	1011	10,000,000.122	9,999,999.878	12.2×10^{-9}
12	1100	10,000,000.133	9,999,999.867	13.3×10^{-9}
13	1101	10,000,000.144	9,999,999.856	14.4×10^{-9}
14	1110	10,000,000.155	9,999,999.845	15.5×10^{-9}
15	1111	10,000,000.166	9,999,999.834	16.6×10^{-9}

5.5.2 FREQUENCY OFFSET AT THE CARRIER FREQUENCY

The frequency offset at the carrier frequency is determined by for formula:

$$\Delta fc = Fc \times \Delta fs$$

where: Δfc = carrier offset

Fc = carrier frequency

Δfs = offset of 10 MHz standard (from Table 5-7)

Table 5-8, offset at 450 MHz carrier frequency, lists the frequency offset in Hertz as a function of switch setting.

TABLE 5-8 OFFSET AT 450 MHz CARRIER FREQUENCY

NOTE: Offset is positive when A6U1-1 is on, and negative when A6U1-1 is off.

CHANNEL	SWITCH A6U18 -2 -3 -4 -5 C4,C3,C2,C1	OFFSET (IN HERTZ) AT 450 MHz
0	0000	0.0
1	0001	0.5
2	0010	1.0
3	0011	1.5
4	0100	2.0
5	0101	2.5
6	0110	3.0
7	0111	3.5
8	1000	4.0
9	1001	4.5
10	1010	5.0
11	1011	5.5
12	1100	6.0
13	1101	6.5
14	1110	7.0
15	1111	7.5

5.5.3 PRINCIPLES OF OPERATION

The Model 8164 operates on a "frequency locking" principal. The frequency of the 10 MHz standard oscillator is measured and control voltage corrections applied to bring it to the desired frequency. The time base for the measurement is derived from the received WWVB signal. The measurement interval is 1000 seconds. The measurement resolution is 1.0 E-10. The adjustment resolution is 2.4 E-10. The long term accuracy is typically ±1.0 E-9.

5.5.4 OFFSET PERFORMANCE TEST

The Model 8164 must be phase-locked to WWVB and in continuous operation for at least 24 hours prior to testing the offsets. The Option 56 offsets may be verified by determining the relative frequency from the strip chart recording. Refer to Section 2.6.2 of this manual for detailed information on frequency calculation from a chart recording. Compare measured relative frequency with the values found in Table 5-7.

> NOTE: The measurement resolution for channels 7 through 15 can be improved by increasing the chart paper speed. Substitute the factory installed 20 mm/hr chart speed cam with the supplied 60 mm/hr cam. The 60 mm/hr cam and installation instructions are found in the Simpson Operators Manual.

5.6 MODEL 8171A, SYNCHRONIZED CLOCK

The Spectracom Model 8171 Synchronized Clock uses the WWVB time code and translated carrier frequency from the 8164 Receiver to provide precise time. A microprocessor performs digital filtering, decoding, phase-locking, and time-keeping functions, and provides the front panel time display and rear panel data outputs.

After the receiver has phase-locked to the carrier, the Model 8171 decodes the time from the WWVB signal modulation. After checking successive data streams to eliminate errors, the clock sets itself and displays correct time (UTC), adjusted for time zone and propagation delay by rear panel switches. Time data are fed to the outputs, and a panel lamp indicates "time sync." Accuracy of ±1.0 millisecond may be achieved. Computer interfaces are RS-232 and parallel BCD.

For more information, contact Spectracom Corporation or the nearest sales representative.

MODEL 8164

SECTION 6

SERVICE INFORMATION

6.0 INTRODUCTION

Periodic calibration of a WWVB Receiver, in the usual sense that an instrument must be sent to the Bureau of Standards or calibrated against a traceable standard, is unnecessary. Time and frequency are the only two measurable quantities that can be transmitted via a radio signal. Because of this, it is possible to be "connected" directly to the Bureau of Standards via a radio signal for calibration of both time and frequency.

We can draw a simple analogy by considering a secondary voltage standard, or standard cell, which is used for voltage calibration. Standard cells are usually returned to the Bureau of Standards or a secondary standards laboratory where they are calibrated and certified traceable to the Bureau of Standards. If it were possible to have a pair of wires connected from your laboratory directly to the "standard volt" at the Bureau of Standards, it would be unnecessary to return your voltage cell periodically to the Bureau of Standards for calibration. This is exactly the situation that we find with time and frequency being received by radio signal directly from the Bureau of Standards. Periodic "calibration" of the instrument is unnecessary because its output is being derived directly from the Bureau of Standards. The only periodic checks that are necessary are ones to determine that the receiver is operating properly and that the correct signal is being received.

6.1 PERFORMANCE CHECK

Spectracom recommends an abbreviated procedure for verifying proper equipment operation. For those users concerned about formal establishment of calibration traceability, the following monthly checks will be sufficient, especially if formally recorded in a log book.

1. Check to see that the green lock light is lit on the front panel of the receiver. This establishes that the receiver is phase locked to a 60 kHz signal being received via the antenna.

2. Check to see that the hourly offset of 2.1 microseconds is occurring at 10 minutes after the hour. These offsets occur due to the 45° phase shift that is applied to the signal at the transmitter at 10 minutes after the hour, returning to normal 15 minutes after the hour. The presence of those offsets both identifies the station and gives hourly "time ticks" on a chart recorder trace of the phase comparator output. Their presence indicates that the signal is from the National Bureau of Standards.

3. Depress the V/Ø lock voltage switch on the front panel to the "lock voltage" position, V, and observe that the front panel meter reading is at or near center scale. If this reading is reaching the outer boundaries of the middle one-third of the scale when the green lock light is on, a trimmer adjustment should be made on the A2 circuit board in the receiver to re-center the meter reading. To obtain a center scale reading, first verify that the green lock light is lit due to an antenna signal, then adjust A2C10 to obtain a center scale reading. This is a sensitive adjustment, and must be made very slowly in extremely small increments. The long time constant in the phase locked loop will prevent the meter reading from changing rapidly, and at least 30 seconds must be allowed

between adjustments for the phase locked loop to settle down. This adjustment compensates for the long-term aging of the 10 MHz crystal A2Y1 which is phase locked to the WWVB carrier frequency. In a properly functioning receiver, this adjustment should not be required more often than every 2 years.

If the answers to the three items on the checklist are yes, then the receiver is operating properly. Calibrations made with it are traceable directly to the Bureau of Standards.

CHECK LIST

	YES	NO
1. LOCK LAMP LIT	____	____
2. OFFSET (PHASE SHIFT) OF 2.1 USEC AT 10 AND 15 MINUTES AFTER EACH HOUR.	____	____
3. LOCK VOLTAGE NEAR CENTER	____	____

Receiver operating unsatisfactorily may require calibration. This section contains information on receiver realignment and performance checks.

6.2 TEST EQUIPMENT

Table 6-1 lists the recommended test equipment for checking the performance of the Model 8164.

Test equipment with equivalent characteristics may be substituted.

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED
WWVB Antenna	60 kHz Active Antenna	Spectracom Model 8206
Oscilloscope	2-Channel	Tektronix Model 455
Voltmeter	4-1/2 Digit Multimeter	Data Precision Model 255
Counter	Accuracy $\pm 1 \times 10^{-7}$	HP 5315B Universal Counter
Signal Generator	60 kHz, $\pm 1 \times 10^{-7}$ Accuracy. Output less than 0.2 μV.	Wavetek Model 3002 Synthesizer
Computer Terminal	RS-232C Interface 300 Baud	Teletype Model 43

TABLE 6.1 RECOMMENDED TEST EQUIPMENT

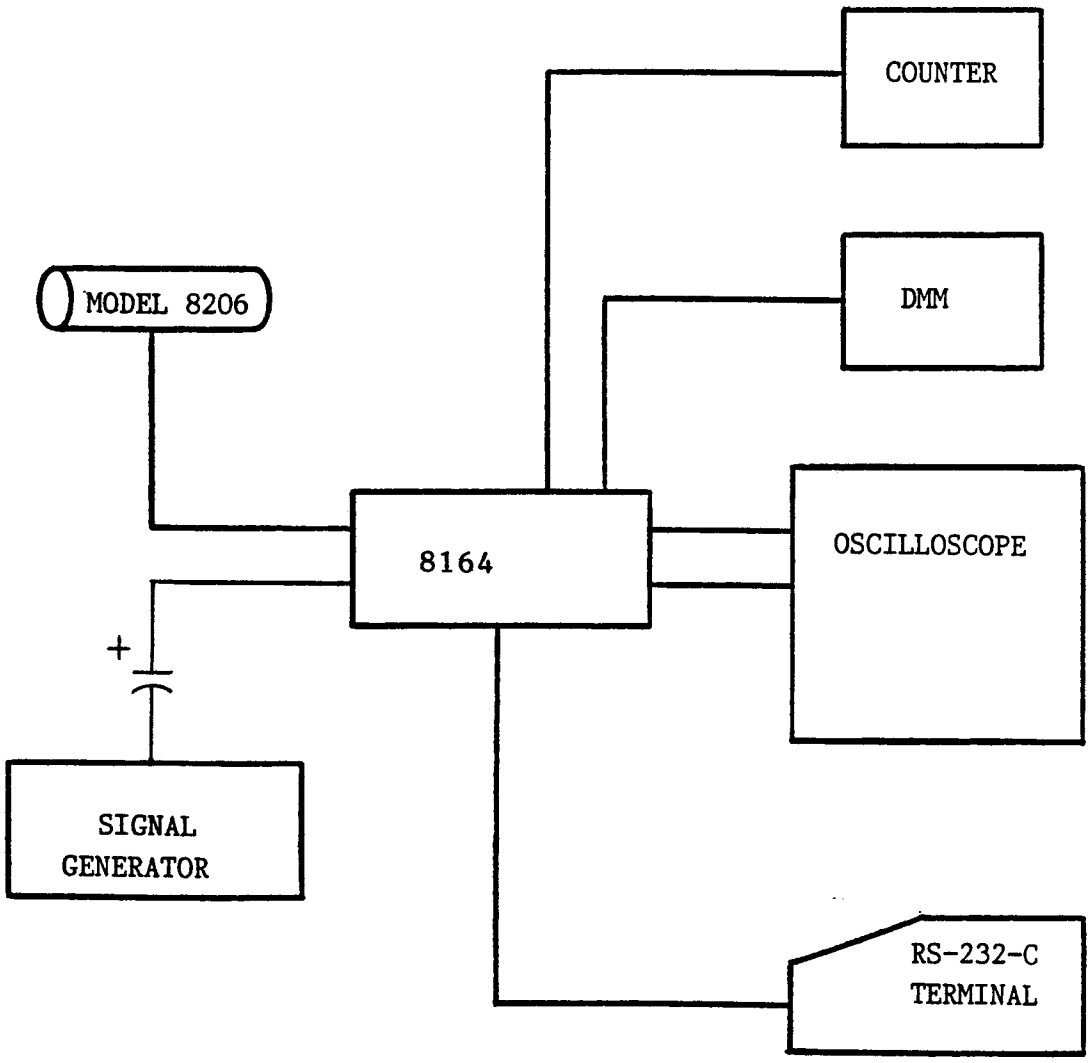


FIGURE 6-1 TEST SET-UP

6.3 BENCH SET-UP

Figure 6-1 shows the Model 8164 Test Set-Up. The signal generator is used to simulate the 60 kHz transmitted by WWVB.

> CAUTION: There is 12 VDC at the antenna input connector. This is used to power the Model 8206 Loop Antenna and Model 8207 Line Amplifier. Some signal generators may require a capacitor to be installed as shown in Figure 6-1 to block this DC level.

6.4 RECEIVER ALIGNMENT AND PERFORMANCE CHECKS

6.4.1 POWER SUPPLIES

This test checks the power supply voltages.

+5 Volts (±.25) A2J3-1 _____V
+12 Volts (±0.5) A2J4-4 _____V
-12 Volts (±0.5) A2J4-1 _____V

6.4.2 RF AMPLIFIER A1 CHECKS

The purpose of these checks is to verify that input transformer T1 and crystal filter C8, C9, and Y1 have been tuned.

Disconnect the AGC wire (violet) from connector A1P2, pin 6.

Connect the oscilloscope probe to A2E1.

Set the signal generator and attenuator to provide an unmodulated 1.0 μV rms signal at exactly 60 kHz.

Apply power to the receiver and adjust the signal generator level to provide a 1 volt peak-to-peak output signal on the oscilloscope.

Adjust the slug in the transformer, A1T1, for a peak on the oscilloscope, while reducing the signal generator to maintain a 1 volt peak-to-peak output.

INPUT VOLTAGE AT 1V P-P OUTPUT _____ μV (< 1.6 μV rms)

Adjust capacitor A1C8 for maximum output on the oscilloscope.

TUNE CRYSTAL FILTER A1C8 _____

Change the signal generator frequency to 100 kHz and output level of 1.0 mV rms. Adjust capacitor A1C9 for minimum output on the oscilloscope.

TUNE STOP BAND NULL A1C9 _____

Change the signal generator frequency to 60 kHz at a 1 mV rms input level. The output wave-form (A2E1) should be a square wave with a 50% ±10% duty cycle and 3 volts peak-to-peak ±20%.

OUTPUT
50% duty cycle ±10% _____

OUTPUT
3V P-P ±20% _____

Change the signal generator so the input to the 8164 is 5 μV rms. The output amplitude should be equal to or greater than 1.5V peak-to-peak. The output will be a sine wave until the clipping point is reached at approximately 3 volts peak-to-peak.

OUTPUT SIGNAL, A2E1, 1.5V p-p _____V

NOTE: This completes the alignment of the RF Amplifier. The AGC potentiometer adjustment is described in test 6.4.9.

6.4.3 QUADRATURE DETECTOR AND PHASE DETECTOR BALANCE

This checks the adjustment of potentiometers A2R30 and A2R5. Remove the input signal to the antenna input.

Adjust the panel meter to zero using the zero adjust on the meter.

Connect a clip lead from A2E2 to A2E3. Connect the negative lead of the DVM to A2TP3, and the positive lead to A2TP4. Set the DVM to ±2V full scale. Make no connection to the antenna input.

Apply power to the receiver and adjust A2R30 for a zero reading on the DVM. Slight digit changes may be noticed, but should be less than ±5 mV. Move the positive DVM lead from A2TP4 to A2TP6. The reading should be less than ±500 mV.

QUAD DETECTOR BALANCE _____

Connect the negative DVM lead to A2TP1 and the positive lead to A2TP2. Adjust A2R5 for a zero reading on the DVM. Changes of ±5 mV or less may be noticed.

PHASE DETECTOR BALANCE _____

6.4.4 LOCK VOLTS METER ADJUST

This test adjusts A2R14. Move the clip lead from A2E3 to A2E4. Set the front panel meter switch to read lock volts (V position). Adjust A2R14 for a meter reading of 80% full scale. Glyptol A2R14.

LOCK VOLTS (80% full scale) _____

6.4.5 OSCILLATOR ADJUST

Connect the frequency counter to the NBS OUTPUT on the front panel. Adjust A2C10 for a counter reading of 9,999,900 Hz.

OSCILLATOR PRESET (9,999,900 Hz) _____Hz

6.4.6 OSCILLATOR SYMMETRY

Disconnect the clip lead from A2E2 to A2E4. Connect the front panel NBS OUTPUT to the oscilloscope. Select 10 MHz output frequency. Adjust A2R23 so the 10 MHz signal is a symmetrical square wave. Glyptol A2R23.

OSCILLATOR SYMMETRY _____

6.4.7 FINAL ADJUST 10 MHZ OSCILLATOR

Adjust the signal generator to 60.000 kHz unmodulated and 1 mV RMS when connected to the receiver antenna. The receiver should lock, indicated by a green lock light and a lock voltage meter reading near center scale. Adjust A2C10 very slowly until the lock voltage is exactly center scale.

6.4.8 FINAL ADJUST PHASE DETECTOR BALANCE

Disconnect the signal generator from the antenna and note the lock voltage meter reading drift. Disregard any sudden small jump at the moment of disconnect. If a downward drift is observed, then turn A2R5 clockwise by very small amounts until the drift is stopped. Small jumps may occur as A2R5 is adjusted, disregard these and only note the slow drift. If an upward drift is observed, then turn A2R5 counter-clockwise by very small amounts. This is a very fine adjustment and is completed when no perceptible drift is evident after one minute of observation. Glyptol A2R5.

6.4.9 AGC VOLTAGE CONTROL ADJUST A1R19

Connect the negative lead of the DVM to A2TP3 and the positive lead to A2TP6. Adjust the signal generator to 60.000 kHz and 1 μV when connected to the ANTENNA input. The meter is reading the AGC voltage with the AGC feedback loop open (the AGC wire, A1P2-6, was disconnected during the testing of the RF Amplifier). Lock-up may take several minutes at 1 μV input. The voltage at A2TP6 may continue to rise after the green lock light comes on.

Adjust the signal generator in small amounts (less than 1 dB) until the voltage is approximately +2.38 V. Wait one or more minutes between level changes. The voltage read on the DVM is delayed by a long time constant in the AGC loop. A 2.38 V reading is normally reached with an antenna input level between 0.25 and 1.0 μV.

AGC VOLTS A2TP3 TO A2TP6 (2.38V) _____V

Reconnect the violet AGC wire to A1P2-6. The DVM reading will slowly decrease to a lower value. Adjust the AGC control A1R19 in very small

amounts until the DVM stabilizes 1V lower or approximately +1.38V. Because of the long time constant in the AGC loop, wait one or more minutes between adjustments. Glyptol A1R19.

AGC VOLTS A2TP3 TO A2TP6 (1.38V) _____V

6.4.10 RECEIVER SENSITIVITY

This test measures the receiver sensitivity. Increase the signal generator level to 10 μV and wait a minute for the receiver to stabilize. Decrease the signal generator level to 1.0 μV and allow one minute for the receiver to stabilize. The green LOCK light should be on. Slowly decrease the signal generator level until the red UNLOCK light comes on. Do not exceed 1 dB per 10 seconds. The signal generator level should be between 0.1 and 0.4 μV.

UNLOCK SENSITIVITY (0.1-0.4 μV) _____μV

Slowly increase the signal generator level until the green LOCK light comes on. Do not exceed 1 dB per 10 seconds. The level will typically be 6 dB above the unlock level and should be between 0.25 and 1.0 μV.

LOCK LEVEL (0.25-1.0 μV) _____μV

6.4.11 PHASE COMPARATOR FULL SCALE ADJUSTMENT

This test calibrates the full scale deflection of the front panel meter.

Turn off the receiver and recheck the mechanical zero adjustment of the front panel meter. This procedure is discussed in the Simpson Operators Manual.

Turn on the receiver, set the front panel RECORDER switch to read phase difference. Depress the EXP switch on the front panel for 10 microsecond full-scale deflection. Select 0.1 MHz input frequency on the front panel FREQUENCY select switch. Connect the NBS OUTPUT to the LOCAL INPUT. Adjust A2R78 for full scale deflection of the front panel meter. Glyptol A2R78.

CALIBRATE FRONT PANEL METER (A2R78) _____

6.4.12 MEASURE LOCAL INPUT SENSITIVITY

This test measures the sensitivity of the LOCAL INPUT amplifier. Install the Model 8206 and achieve phase lock with WWVB. Depress the 1 MHz select FREQUENCY switch on the front panel. Connect the signal generator to the LOCAL INPUT. Set the input signal to 1.0 MHz at 100 mV RMS. The meter will show the relative phase drift between the two signals.

Decrease the signal level into the LOCAL INPUT until the phase comparator operation becomes erratic. Increase the level until stable operation is attained. Record the level of the input signal.

LOCAL INPUT SENSITIVITY _____mV

6.4.13 NBS OUTPUT

Connect the oscilloscope to the NBS OUTPUT connector through a short coax cable. Depress the 0.1 MHz FREQ select switch and observe that the waveform is a TTL-compatible rectangular square wave. Repeat by selecting 1.0, 5.0, and 10.0 MHz. Perform this check on the STANDARD OUTPUT also.

NBS OUTPUT 0.1 MHZ (>2.7V) _____V
1.0 MHz (>2.7V) _____V
5.0 MHz (>2.7V) _____V

10.0 MHz (>2.7V) _____V

6.4.14 ANTENNA VOLTAGE MEASUREMENT

Connect the antenna to the receiver through a BNC T-connector. With the antenna connected to the receiver, measure the DC voltage at the ANTENNA input.

ANTENNA VOLTAGE (2.0V ±0.2) _____V

6.4.15 SIGNAL STRENGTH MEASUREMENT

After the antenna has been installed and connected to the Model 8164, measure the AGC voltage. Connect the negative lead of the DVM to A2TP3 and the positive lead to A2TP6. Record the voltage. Maximize this voltage by experimenting with antenna location and orientation. The receiver will lock on the signal when the AGC voltage is greater than 1.0 volts.

AGC VOLTS (>1.0 V) _____V

6.5 OSCILLATOR AND POWER SUPPLY A5 CHECKS

These checks verify that the power supplies on the A5 assembly are operational.

Connect the negative lead of a DMM to the chassis. Select the +200 VDC range and connect the positive lead to J6-3 on the rear panel. Place the rear panel selector switch in the EXT position. The DMM should read +27.6 V at 25°C ambient. This voltage will vary by -0.05 volts per degree C for room temperatures other than 25°C. If the temperature corrected voltage is not correct, adjust potentiometer A5R18 for the correct reading, and glyptol the potentiometer.

A5R18 set for +27.6 V _____V

Disconnect the positive lead of the DMM and set it for a range greater than +0.5 Amperes. Reconnect the meter to J6-3 note the reading should be .25A ±.05 A. This measurement checks the maximum charge current limiting at the EXT battery terminal by shorting the power supply through the ammeter to ground. THIS CHECK ALSO CAUSES THE LINE INTERRUPT LIGHT TO TURN ON. PRESS THE RESET SWITCH TO TURN OFF THE LIGHT.

CHARGE CURRENT .25A ±.05 _____A

Disconnect the DMM and set it to read volts on a range to read 200 volts.

Connect the positive lead to the collector of A5Q9 (the metal side of the package). The DMM should read +21.0 volts. If it does not adjust A5R25 for +21.0 volts.

A5Q9-C READS 21.0 V _____V

NOTE: IF THE INTERNAL BATTERY PACK IS TO BE USED SET THE REAR PANEL SWITCH TO THE **INT** POSITION.

6.5.1 OSCILLATOR ALIGNMENT

Allow the oscillator to operate with uninterrupted oven and oscillator power for at least 24 hours before performing the alignment. The alignment procedure is described in Section 6.6.14, Frequency-Time Comparator checks.

6.6 FREQUENCY-TIME COMPARATOR CHECKS

These checks verify the operation of the frequency-time comparator assembly. Before starting this section of test procedure, record the dip switch settings of U1 and U18.

The Antenna should be connected to the Model 8164. A cable should be prepared to connect a data terminal to the RS-232 DATA connector on the rear panel.

The RS-232 interface is:

Pin 5	Data from 8164
Pin 4	Data into 8164
Pin 9	Ground

The mating connector is a 9-pin series D male.

6.6.1 POWER SUPPLIES

Apply power to the unit and record the following voltages:

J2-6	+5 volts	(±0.25)	_____Volts
J2-2	+12 volts	(±0.50)	_____Volts
J2-1	-12 volts	(±0.50)	_____Volts

6.6.2 RECEIVER LOCK

Set up the oscilloscope for DC coupling, auto-trigger at 1 volt/division and 10 milliseconds/division. Connect the probe ground to the chassis. The LOCK lamp on the front panel should be illuminated.

LOCK lamp illuminated _____
J4-5 RXLOCK (> +3.0 Volts) _____

Remove the antenna from the unit. Within 30 seconds the unlock lamp should illuminate.

UNLOCK lamp illuminated _____
J4-5 RXLOCK (< +0.6 Volts) _____

RECONNECT THE ANTENNA

6.6.3 PUSH BUTTON RESET

Place the oscilloscope probe on PBRESET (J1-2).

J1-2 PBRESET (> 3.0 Volts) _____

Hold front panel RESET button depressed.

J1-2 PBRESET (< 0.6 Volts) _____

6.6.4 OUTFAULT INPUT TEST

Place oscilloscope probe on OUTFAULT (J3-5).

J3-5 OUTFAULT (> 3.0 Volts) _____

Short the 10 MHz standard output on the rear panel.

J3-5 OUTFAULT (< 0.6 Volts) _____

6.6.5 10 MHZ CLOCK INPUTS

Set up the oscilloscope for DC coupling, positive-trigger at 1 volt/division and 100 nanoseconds/division. Leave the probe ground on the chassis.

At NBS 10 MHz (J4-4) should be a square wave:
Period (100 ±10 nanoseconds) _____
High Level (> 3.0 Volts) _____
Low Level (< 0.6 Volts) _____

At STD 10 MHz (J4-1) should be a square wave:
Period (100 ±10 nanoseconds) _____
High Level (> 3.0 Volts) _____
Low Level (< 0.6 Volts) _____

6.6.6 TIME CODE INPUT

Change the oscilloscope time base to 200 milliseconds per division. The oscilloscope should trigger approximately every three seconds. Place probe at TCODE (J4-6). More than one half of the wave-forms observed should transition low within the first five divisions and re-transition high at 1.00 ±0.02 seconds and 2.00 ±0.02 seconds.

Low-High Transition Period
(1.00 ±0.02 seconds) _____
High Level (> 3.0 Volts) _____
Low Level (< 0.6 Volts) _____

6.6.7 ALARM LAMP TEST

Turn on the LAMP and TEST switches on dip switch U1. All remaining switches on U1 and U18 should be turned off. Note that the CPU lamp flashes alternate of the FREQ, SIGNAL, OUTPUT, TIME and ADJ OSC alarms.

LED CHECK _____

Turn off the TEST and LAMP switches and depress the RESET button to clear any alarms.

6.6.8 1-Hz OUTPUT

Change the oscilloscope time base to 200 milliseconds/division. Change the trigger to positive edges. Place the probe on Pin 7 of the rear panel DATA connector. A 1-Hz square-wave should be observed with a high level greater than 3.0 volts and a low level less than 0.6 volts.

1-Hz OUTPUT _____

6.6.9 SIGNAL FUNCTION TEST

Remove the power from the unit. Connect the data terminal to the rear panel connector. Move U1 switches TEST and GATE to the ON position. Apply power to the unit. Initially, the UNLOCK and SIGNAL lamps will be illuminated. Within 30 seconds, the LOCK lamp should illuminate, extinguishing the UNLOCK and SIGNAL lamps.

Ten seconds after the lock lamp illuminates, a frequency printout at the data terminal should begin.

6.6.10 TIME CODE FUNCTION TEST

Within 30 seconds of the illumination of the LOCK lamp a phase printout at the computer terminal should begin.

6.6.11 GATE10 SWITCH TEST

Move the GATE10 switch to the OFF position. One more frequency printout should occur at the end of the regular 10 second gate period. The only automatic printouts for the subsequent 1000 seconds should be phase printouts.

6.6.12 TERMINAL COMMANDS

Type the letter "D" on the keyboard. "DA=500" should be printed out. Type "500" followed by a carriage return. The D/A Set Record should be printed.

Type the letter "R" on the keyboard. "Restart at" should be printed out.

Type the letter "L" on the keyboard. All records since the application of power should be reprinted.

6.6.13 D/A SWITCH TEST

Using the DVM, measure HILIMIT (J3-4). It should read 6.5 ±0.5 volts. (Chassis ground is sufficient for the ground probe.)

Adjust LOLIMIT (J3-3), by turning R4 on the A5 board, to 3.0 ±0.3 volts.

Move the TEST and DA-ZERO switches to the ON position. Using the DVM, measure the voltage at U16-9. It should read an average of 0 ±0.2 volts.

Move the DA-ZERO switch to the OFF position and move the DA-ONE switch to the ON position. The voltage at U15-6 should change to 3.5 ±0.5 volts.

6.6.14 FREQUENCY RANGE ADJUSTMENT

Before performing the oscillator alignment the unit must be connected to an uninterrupted power source a minimum of 24 hours in advance.

The antenna must be connected and the receiver must be phase locked.

Move the TEST, GATE10, and DA-ZERO switch to the ON position. Type "R" on the data terminal. Approximately every ten seconds, a frequency record will be printed. The frequency printouts are in hexadecimal. Adjust the coarse frequency trim on the ovenized oscillator until three consecutive frequency printouts of 000005F5E119 ±1 are achieved. (Counter-clockwise rotation of the trimmer will increase frequency.)

000005F5E119 ±1 _____

Units equipped with Option 31, 10-Hz TV Offset only, set oscillator to:

000005F5E123 ±1 _____

Move the DA-ZERO switch to the OFF position and move the DA-ONE switch to the ON position. Similarly, adjust R4 on the A5 board until three consecutive printouts of 000005F5E0B5 ±2 are achieved. (Counter-clockwise rotation will increase frequency.)

000005F5E0B5 ±2 _____

Option 31 Units only

000005F5EBF ±2 _____

The receiver alignment and performance tests are now complete. Return DIP switches U12 and U18 to their original positions. The unit will require a 3 to 4 hour re-synchronization period.

6.7 ACCESSORY TESTS

This section provides information on testing the following:

* Model 8206 Antenna
* Model 8207 Preamp
* Model 8140T Line Tap

6.7.1 MODEL 8206 ANTENNA

This test verifies the proper operation of the Model 8206 Loop Antenna.

Figure 6-2, MODEL 8206 TEST SET-UP shows the test set-up for testing the antenna. Connect a coax cable to the signal generator. Wrap 2 turns of wire around the antenna. Connect one side of the wire to the center conductor of the coax through a 1K resistor. Connect the other side to the shield.

Adjust the signal generator for an output of .014 V rms into the 1K load. If the signal generator has a calibrated output that expects a 50-ohm load, then adjust the output level to .007 V rms. Feed +12V to the antenna through a 27K resistor. AC couple the antenna to the scope.

Find the resonant frequency of the antenna by adjusting the signal generator frequency for maximum output signal. The resonant frequency should be 60.0 ±.3 kHz.

RESONANT FREQUENCY 60.0 ±.3 kHz_____kHz

The amplitude of the output signal should be approximately 0.01 Vp-p.

ANTENNA OUTPUT (.010 Vp-p) _____V

Determine the antenna bandwidth. Increase the signal generator frequency until the output amplitude is 3 dB below the resonant frequency amplitude. Decrease the signal generator frequency until the output amplitude is 3 dB down. Make sure that the amplitude of the input signal remains constant during this test. The antenna bandwidth is the difference in the two frequencies.

ANTENNA BANDWIDTH (1 kHz)_____kHz

WARNING: ALL OTHER ANTENNAS EXCEPT UNIT UNDER TEST MUST BE KEPT AT LEAST 6 FEET AWAY TO PREVENT STRAY DETUNING! DO NOT PLACE ANTENNA ON OR NEAR METAL SURFACES OR OBJECTS.

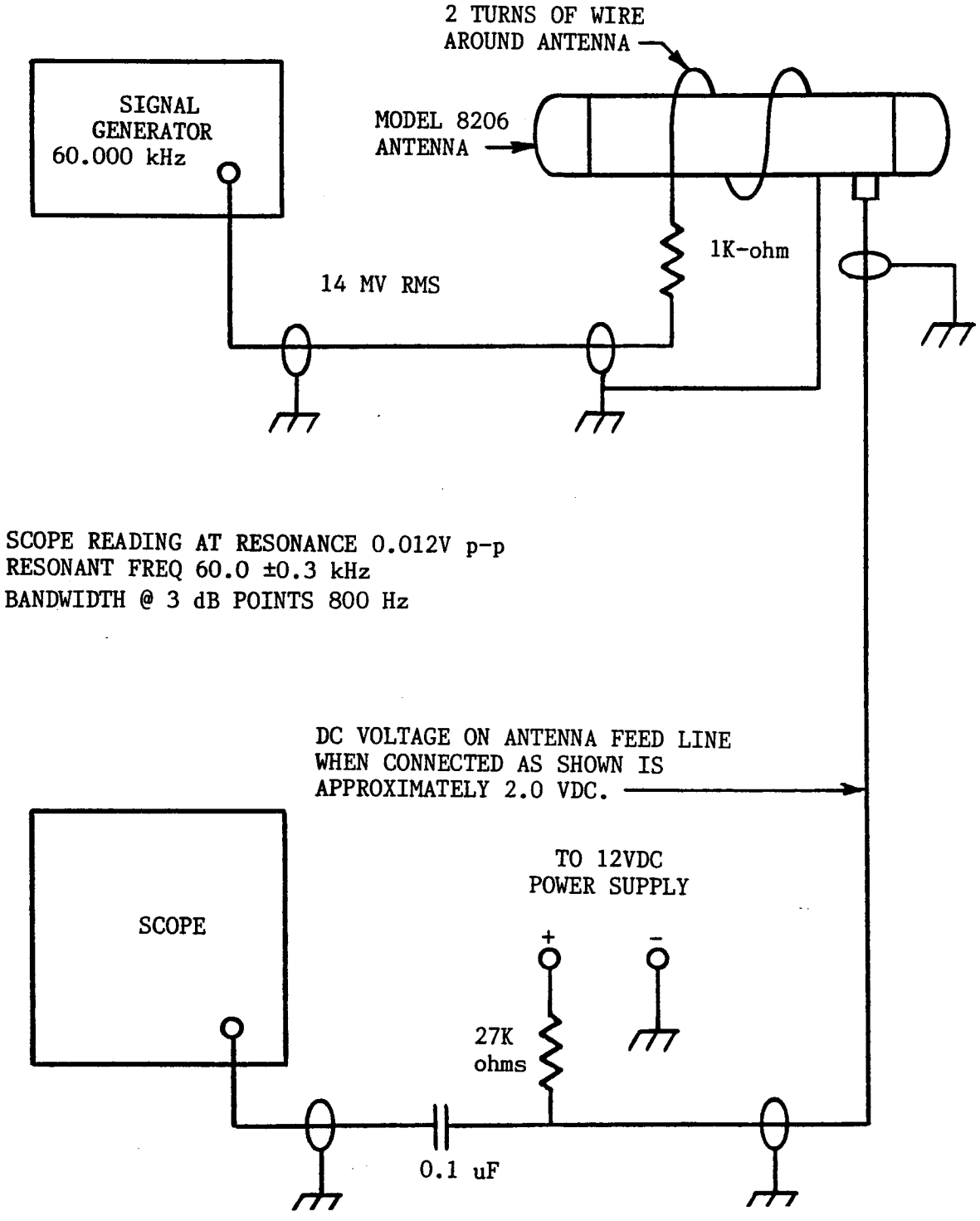


FIGURE 6-2 ANTENNA MODEL 8206 TEST SET-UP

6.7.2 MODEL 8207 PREAMP ALIGNMENT

The Model 8207 Antenna Preamplifier is a low noise, tuned, 60 kHz line amplifier used in the antenna feed line wherever the WWVB signal strength is less than 0.4μV at the receiver antenna connector.

The purpose of this test is to tune the preamp to 60 kHz.

Perform the receiver alignment as described in this section.

Set the receiver A1S1 switch to the preamp (P) position.

Use RG-58 coax to connect the preamp between the signal generator and the WWVB receiver as shown in Figure 6-3.

Physically separate the preamp from the receiver by at least 10 feet. Keep the cable from the signal generator to the preamp away from the vicinity of the receiver to prevent signal regeneration.

In the receiver, disconnect the AGC wire (violet) from connector A1P2, Pin 6, but leave the remaining wires in place and the connector mated.

Connect an oscilloscope probe to A1E3. Set the scope for AC coupling. The ground lead is connected to the chassis.

Set the generator to provide a 1.0 μV signal at exactly 60.000 Hz, unmodulated.

Apply power to the receiver and adjust the signal generator level as necessary to provide a 1 Vp-p output signal on the oscilloscope.

Adjust the slug in transformer A1T1 in the Model 8207 for a peak on the oscilloscope, while reducing the signal generator level to maintain the 1 Vp-p output.

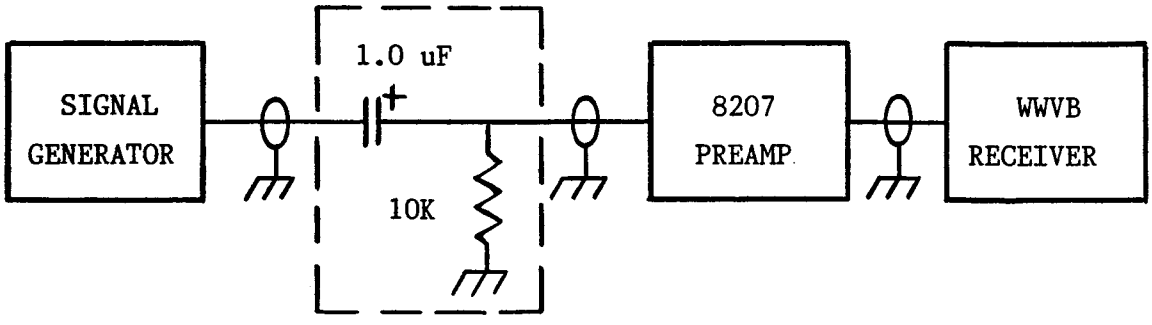


FIGURE 6-3 MODEL 8207 PREAMPLIFIER ALIGNMENT

6.7.3 MODEL 8140T LINE TAP TEST PROCEDURE

Refer to Figure 6-4 Line Tap Model 8140T Test Setup. Connect a coaxial BNC tee to the output of the line tap under test. Connect the 50-ohm (use the DC isolated 50 ohm terminators P/N 004490) load to one output of the tee and connect the oscilloscope to the other tee output.

Set the scope for DC coupling and set the sweep at 1 cycle/cm.

The oscilloscope presentation should be a 1.4 Vp-p minimum. (2.0 Vp-p typical) sine wave symmetrical around the 0 volt reference.

Remove the 50-ohm output termination. The scope should show 3.0 Vp-p minimum (4.0 Vp-p typical) sine wave with a DC offset as shown.

NOTE: At frequencies of 5 or 10 MHz, a 10:1 oscilloscope probe must be used to prevent loading.

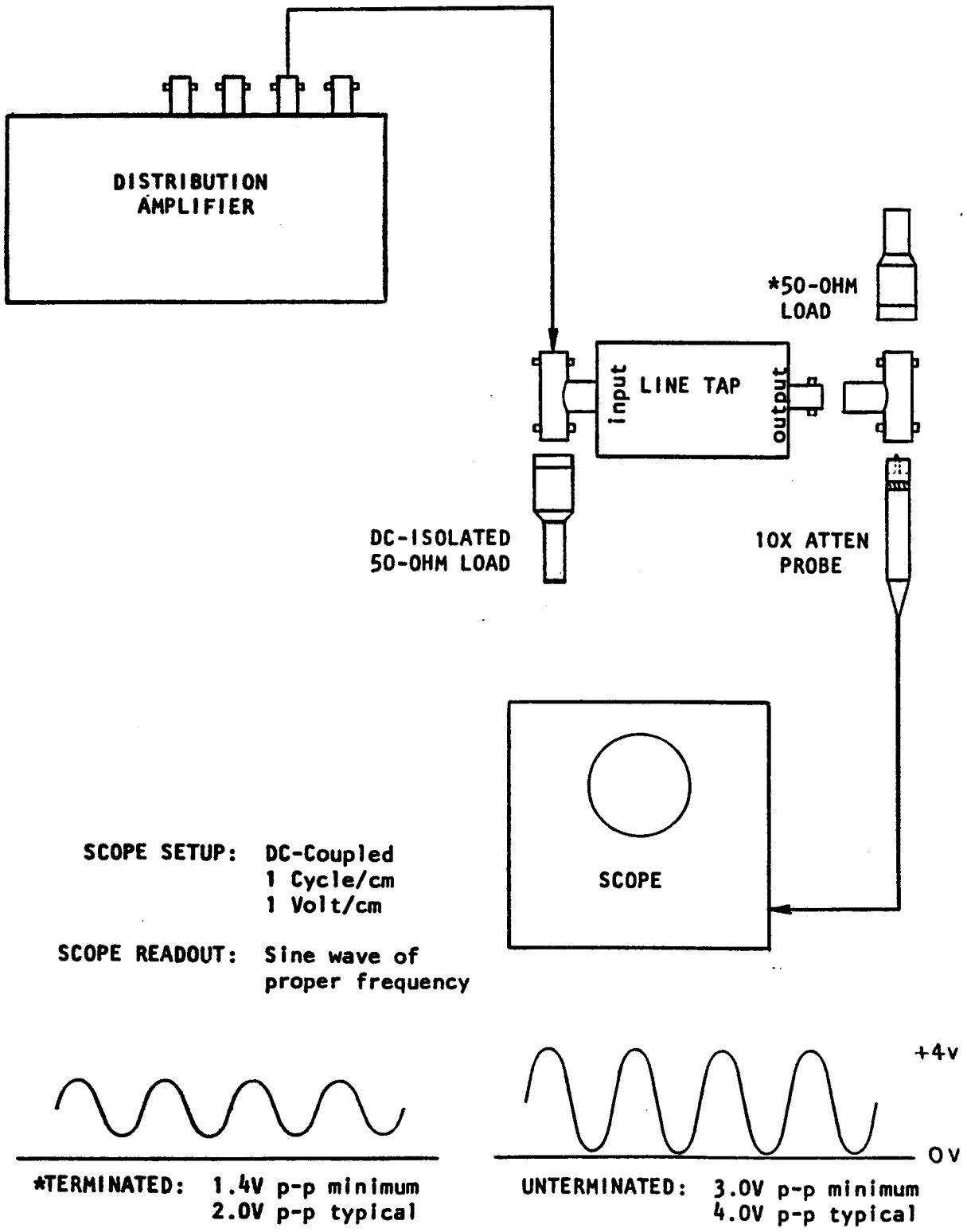


FIGURE 6-4 LINE TAP MODEL 8140T TEST SET-UP

6.8 TROUBLESHOOTING

If trouble occurs with a WWVB receiver, some simple checks can isolate the problem to specific areas of the receiver. Some of the more likely problems and the procedures for solving them are as follows:

6.8.1 RECEIVER DOES NOT LOCK

Improper reception. The most efficient way of solving this type of problem is to isolate the problem to one of the three major receiver system components. These are antenna, A1 RF amplifier assembly, and A2 receiver board assembly.

A. Antenna DC check. Measure the DC voltage on the antenna line with a DVM. With the antenna connected to the receiver and the receiver turned on, the DC voltage on the coaxial line should be approximately 2.0 volts ±10%. This can be measured by inserting a coaxial tee in the line at the rear of the receiver and measuring the antenna voltage with the antenna connected. With the antenna disconnected, the DC voltage at the antenna terminal of the receiver should be approximately 11.5 volts DC ±10%. If both these measurements are satisfactory, proper DC conditions are verified in both the antenna and its power supply in the receiver.

   If the 11.5 volt level is not present with the antenna disconnected, the fault is in either the A1 Rf Amplifier assembly or in the A2 Receiver assembly. Disconnect the A1 board and check for +12 VDC at pin 1 of the connector A1P2. If the voltage is not present, the problem is in the power supply on the A2 board assembly (diodes CR12 through CR14, capacitors C53 through C57, or regulator U22.) If the 12 volt level is present, the problem is in the A1 board assembly.

B. Check the receiver without the antenna connected. Using a signal generator set at 60.000 kHz with an accuracy of ±1.0 E-6, feed a 1.0 microvolt signal from the generator to the antenna input of the receiver. Apply power to the receiver and see if the receiver locks. If it does lock under this condition, the problem is most likely with the RF performance of the antenna or with the antenna placement or installation. If the receiver does not lock with 1.0 microvolts applied, the fault is in the receiver.

   Check the 60 kHz signal at E3 of RF amplifier board A1. If the signal is present, the RF amplifier is operating satisfactorily and the problem is in Receiver assembly board A2. If the 60 kHz signal is not present at E3, the fault is in the A1 board assembly.

6.8.2 NO NBS OUTPUT AT THE FRONT PANEL CONNECTOR

Check pin 11 of U5A on the A2 board to see that the oscillator stage containing A2Y1 is operating properly, and oscillating at 10.0 MHz. If this oscillator, which gets phase locked to WWVB, is not oscillating then the most likely problem is with the crystal Y1, which may need to be replaced. Another possibility is oscillator alignment. If this oscillator stage is not performing properly, the NBS output will not be present, and

the receiver will not phase lock, or alternatively the phase lock lamp may remain on continuously even though the receiver is not operating properly. This condition can be checked by removing the antenna signal and checking to see that the phase lock lamp is extinguished after approximately 30 seconds.

6.8.3 NO STANDARD OUTPUT

If the front panel output from the internal frequency standard oscillator is not present, the fault can lie with either assemblies A4 or A5. The A5 oscillator assembly is the source of this signal and contains both the oscillator and its power supply. If any of these are malfunctioning, the frequency standard outputs will be missing. Assembly A4 is the output amplifier which feeds the appropriate frequencies from the A5 assembly to both the front and rear panels. Signal tracing from the input of this board to the outputs which feed the front and rear panels can establish whether or not this board is performing properly.

6.8.4 FUSE BLOWS

This problem is most likely caused by power supply malfunction in the A2 board or in the chassis power supply components such as power transformers, filter capacitors, etc. The problem may be isolated to on or off-board causes by disconnecting all of the connectors from the A2 board and turning the unit on again. If the fuse still blows, the cause is not on the A2 board. If the fuse does not blow with the connectors removed from the A2 board, reconnect them in the following order, turning power on after each connector is reattached:

A. Reattach the connector from the cable harness to A2J2. This connects the power transformers to the power supply rectifier circuits. If this causes the fuse to blow, the problem is most likely a power supply short on the A2 board itself. Check the voltage regulators U21, U22, and U23 for proper operation. Check to see that Zener diode VR2 is not shorted to ground. This diode provides over-voltage protection on the +5 VDC line and will fuse, shorting to ground causing a fuse to blow if U21 fails and lets the +5 volts go high. Before replacing VR2, disconnect it and check U21 for proper operation. If connecting the cable at A2J2 does not cause the fuse to blow after power is reapplied, proceed to the next step.

B. Connect the A1 assembly to A2J5. Reapply power.

C. Connect the cable harness connector to A2J1. Reapply power. If this causes the fuse to blow, the problem is most likely in the A4 or A5 assemblies, perhaps a power supply short circuit on one of these boards.

D. Reconnect the cables at A2J3 and A2J4. A2J3 provides +5 volts DC to the other parts of the receiver, including the front panel and a short on one of these lines will cause a fuse to blow.

6.8.5 OUTPUT FAULT LIGHT ON

The output fault lamp indicates that a rear panel output is not present. First check that the outputs are not being loaded down by a device using the standard outputs. Impedance mismatch can cause reflections which will cancel the signal. Terminate the end of any coaxial line with a 50 ohm load to prevent reflections.

6.8.6 TERMINAL COMMANDS

If there is no response to letters typed at the terminal, repeatedly type characters and look for ASCII data at U27-1 and U13-10. If data is present, suspect the processor chip.

If the "L" command does not produce a replication of the previous records, suspect the RAM chip, U5.

6.8.7 D/A SWITCH TEST

If HILIMIT does not have 6.5 volts, check A5, Oscillator Assembly.

If LOLIMIT cannot be adjusted to 3.0 volts, check A5, Oscillator Assembly.

If the DA-ZERO switch does not produce zero volts at U15-6, verify that the DA-ZERO switch is operative by checking for a low at U7-39 when the switch is ON and a high when the switch is OFF. Also verify that the DA-ONE switch is not defective by checking for a high at U7-38. If the switches check out, then the PPI (U7), the D/A unit (U16), or the Op Amp (U15) may be at fault.

If the DA-ONE switch does not produce the expected results, verify that the switch is operative by checking for a low at U7- 38 when the switch is ON and a high when the switch is OFF. Also check the DA-ZERO switch at U7-39. If the switches check out, measure the voltage at U16-8, it should be approximately -3.5 volts. If not, check the preceding differential amplifier. If U16-8 was satisfactory, then the PPI (U7), the D/A unit (U16), or the OpAmp (U15) may be at fault.

6.8.8 FREQUENCY RANGE ADJUSTMENT

If 000005F5E119 coarse adjustment cannot be achieved, check U19- 14 for approximately 6.5 ±0.3 volts. If this voltage is not present, check the associated differential amplifier.

If difficulty is encountered in adjusting R4 on the A5 board for 000005F5E0B5, measure the voltage at J3-3. U19-14 should be equal to that voltage ±0.5 volts. If not, check the associated differential amplifier.

6.8.9 PROCESSOR CHECK

The central control element of the FTC is a microprocessor subsystem including a microprocessor, a read-only memory (ROM), and a random-access memory (RAM). To provide for the FTC functions, the processor utilizes a variety of hardware devices including counter/timers and basic input/output

variety of hardware devices including counter/timers and basic input/output lines.

The rational behavior of the FTC relative to these various input/output sources is determined by instructions stored in the ROM.

The inner workings of the processor subsystem are rather complex, so the following procedures have been constructed to aid in troubleshooting the processor subsystem.

Remove the power from the unit. Move all switches on U1 and U18 to the OFF position. Move the PHASE, FREQ, TEST, and GATE10 switches to the ON position. Apply power to the unit. Verify the following measurements after LOCK condition:

Logic level	50 kHz	wave-form at U3-10	_____
Logic level	1 Hz	wave-form at U3-13	_____
Logic level	50 kHz	wave-form at U2-10	_____
Logic level	1 Hz	wave-form at U2-13	_____
Logic level	200 Hz	wave-form at U2-17	_____

If the above conditions exist, the internals of (CPU) U13, U12, U2, and U3 are probably good.

If none of the above are functional, check U13-18 for a low level 11 MHz signal. This verifies the CPU oscillator circuit and crystal. Check for a high going pulse at U12-11 every 1 to 2 microseconds for approximately 100 nanoseconds. Check for a low going signal of 200 nanoseconds at U6-20. This verifies the CPU instruction fetch cycle. Connect the oscilloscope to U5-21. Set for negative triggering with a sweep of 2 microseconds/division. Momentarily turn the power off and back on again. Pulses should appear here every 3 to 6 microseconds for more than 100 milliseconds. If so, U6 and U12 are probably good. U8 is probably faulty.

If U2 readings above are good but the U3 readings are not, check for a 200+ nanosecond low going pulse at U8-14 at least 10 times per second. If it is present, U3 is probably faulty, otherwise U8 is probably faulty.

If U3 readings above are good but the U2 readings are not, check for 200+ nanosecond low going pulses at U8-13 at least 10 times per second. If present, U2 is probably faulty, otherwise U8 is probably faulty.

Check for 200+ nanosecond low-going pulses at U8-12 at least 10 times per second. If they are not present, U8 is probably faulty.

If switches or lamps do not behave normally at this point, U7 is probably faulty.

MODEL 8164

SECTION 7

REPLACEABLE PARTS LIST

7.0 INTRODUCTION

The parts lists on the following pages include ancillary components, circuit board assemblies and PC board components that are replaceable. Refer to the schematic diagrams to determine which optional parts are used in the equipment you have. To order a complete PC board assembly, list the PC board assembly number followed by the appropriate option numbers.

7.1 RF AMPLIFIER ASSEMBLY

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
A1	001100	PC BOARD ASSEMBLY, RF AMPLIFIER
C001	C07220	CAP, 22 uF 25V LITIC
C002	C06182	CAP, 1800pF MICA
C003	C09010	CAP, 1.0 uF 50V LITIC
C004	C09010	CAP, 1.0 uF 50V LITIC
C005	C09010	CAP, 1.0 uF 50V LITIC
C006	C07220	CAP, 22 uF 25V LITIC
C007	C05820	CAP, 82pF MICA
C008	C00040	CAP, 4.5-20 pF CER. TRIM
C009	C00040	CAP, 4.5-20 pF CER. TRIM
C010	C05050	CAP, 5pF MICA
C011	C09010	CAP, 1.0 uF 50V LITIC
C012	C07220	CAP, 22 uF 25V LITIC
C013	C09010	CAP, 1.0 uF 50V LITIC
C014	C18103	CAP, 10000 pF 65V POLYSTYRENE
C015	C18103	CAP, 10000 pF 65V POLYSTYRENE
C016	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C017	C09010	CAP, 1.0 uF 50V LITIC
C018	C07220	CAP, 22 uF 25V LITIC
C019	C09010	CAP, 1.0 uF 50V LITIC
C020	C09010	CAP, 1.0 uF 50V LITIC
C021	C09010	CAP, 1.0 uF 50V LITIC
C022	C07220	CAP, 22 uF 25V LITIC
C023	C06182	CAP, 1800pF MICA
L001	L03102	CHOKE, 1000 uH
L002	L03102	CHOKE, 1000 uH
L003	L03331	CHOKE, 330 uH
P001	J00002	RECEPTACLE, BNC
P002	P04014	PLUG, 6 PIN
P02E	P00300	KEY, MOLEX
Q001	Q04126	TRANSISTOR, PNP, 2N4126
Q002	Q04124	TRANSISTOR, NPN, 2N4124
Q003	Q04124	TRANSISTOR, NPN, 2N4124
R001	R01562	RES, 5.6K OHMS 1/4W 5% C.FILM
R002	R01273	RES, 27K OHMS 1/4W 5% C.FILM
R003	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R004	R01183	RES, 18K OHMS 1/4W 5% C.FILM
R005	R01153	RES, 15K OHMS 1/4W 5% C.FILM

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
R006	R01152	RES, 1.5K OHMS 1/4W 5% C.FILM
R007	R01123	RES, 12K OHMS 1/4W 5% C.FILM
R008	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R009	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R010	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R011	R01183	RES, 18K OHMS 1/4W 5% C.FILM
R012	R01183	RES, 18K OHMS 1/4W 5% C.FILM
R013	R01123	RES, 12K OHMS 1/4W 5% C.FILM
R014	R01683	RES, 68 K OHMS 1/4W 5% C.FILM
R015	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R016	R01681	RES, 680 OHMS 1/4W 5% C.FILM
R017	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R018	R01100	RES, 10 OHMS 1/4W 5% C.FILM
R019	R05503	POT, 50K OHM TRIM
R020	R01222	RES, 2.2K OHMS 1/4W 5% C.FILM
S001	S00420	SWITCH, SLIDE
T001	T00020	TRANSFORMER, INPUT
U001	U01350	IF AMP, 1350
U002	U01350	IF AMP, 1350
Y001	Y00000	XTAL, 60 KHZ

7.2 RECEIVER ASSEMBLY

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
A2	001200	PC BOARD ASSEMBLY, RECEIVER
C001	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C002	C09010	CAP, 1.0 uF 50V LITIC
C003	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C004	C00100	CAP, 120 uF 15V TANT
C005	C02103	CAP, .01 uF 25V DISC CERAMIC
C006	C07220	CAP, 22 uF 25V LITIC
C007	C15685	CAP, 6.8 uF 35V TANT
C008	C05560	CAP, 56pF MICA
C009	C05200	CAP, 20pF MICA
C010	C00040	CAP, 4.5-20 pF CER. TRIM
C011	C05121	CAP, 120pF MICA
C012	C05301	CAP, 300pF MICA
C013	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C014	C18472	CAP, 4700 pF 65V POLYSTYRENE
C015	C18472	CAP, 4700 pF 65V POLYSTYRENE
C016	C09010	CAP, 1.0 uF 50V LITIC
C017	C07220	CAP, 22 uF 25V LITIC
C018	C07220	CAP, 22 uF 25V LITIC
C019	C09010	CAP, 1.0 uF 50V LITIC

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
C020	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C021	C15105	CAP, 1 uF 35V TANT
C022	C10157	CAP, 150 uF 6V TANT
C023	C07220	CAP, 22 uF 25V LITIC
C024	C02103	CAP, .01 uF 25V DISC CERAMIC
C025	C02103	CAP, .01 uF 25V DISC CERAMIC
C026	C02103	CAP, .01 uF 25V DISC CERAMIC
C027	C02103	CAP, .01 uF 25V DISC CERAMIC
C028	C02103	CAP, .01 uF 25V DISC CERAMIC
C029	C02103	CAP, .01 uF 25V DISC CERAMIC
C030	C02103	CAP, .01 uF 25V DISC CERAMIC
C031	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C032	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C033	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C034	C07220	CAP, 22 uF 25V LITIC
C035	C07220	CAP, 22 uF 25V LITIC
C036	C02103	CAP, .01 uF 25V DISC CERAMIC
C037	C02103	CAP, .01 uF 25V DISC CERAMIC
C038	C02103	CAP, .01 uF 25V DISC CERAMIC
C039	C05910	CAP, 91pF MICA
C040	C05910	CAP, 91pF MICA
C041	C02103	CAP, .01 uF 25V DISC CERAMIC
C042	C02103	CAP, .01 uF 25V DISC CERAMIC
C043	C02103	CAP, .01 uF 25V DISC CERAMIC
C044	C18392	CAP, 3900 pF 65V POLYSTYRENE
C045	C18751	CAP, 750 pF 65V POLYSTYRENE
C046	C18392	CAP, 3900 pF 65V POLYSTYRENE
C047	C07222	CAP, 2200 uF 25V LITIC
C048	C07222	CAP, 2200 uF 25V LITIC
C049	C07222	CAP, 2200 uF 25V LITIC
C050	C07222	CAP, 2200 uF 25V LITI
C051	C09010	CAP, 1.0 uF 50V LITIC
C052	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C053	C08102	CAP, 1000 uF 35V LITIC
C054	C08102	CAP, 1000 uF 35V LITIC
C055	C09010	CAP, 1.0 uF 50V LITIC
C056	C09010	CAP, 1.0 uF 50V LITIC
C057	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C058	C01104	CAP, 0.1 uF 25V DISC CERAMIC
C059	C09010	CAP, 1.0 uF 50V LITIC
C060	C09010	CAP, 1.0 uF 50V LITIC
CR01	CR04148	DIODE, IN4148
CR02	CR00209	VARICAP,29 pF,3V
CR03	CR05059	RECTIFIER,1A,200 PIV
CR04	CR04148	DIODE, IN4148
CR06	CR04148	DIODE, IN4148
CR07	CR04148	DIODE, IN4148
CR08	CR05624	RECTIFIER,3A,200 PIV
CR09	CR05624	RECTIFIER,3A,200 PIV

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
CR10	CR05624	RECTIFIER,3A,200 PIV
CR11	CR05624	RECTIFIER,3A,200 PIV
CR12	CR05059	RECTIFIER,1A,200 PIV
CR13	CR05059	RECTIFIER,1A,200 PIV
CR14	CR05059	RECTIFIER,1A,200 PIV
CR15	CR05059	RECTIFIER,1A,200 PIV
CR16	CR04148	DIODE, IN4148
J001	J10014	HEADER, 6 PIN (4)
J002	J10014	HEADER, 6 PIN (2)
J003	J10014	HEADER, 6 PIN (2)
J004	J10014	HEADER, 6 PIN (2)
J005	J10014	HEADER, 6 PIN
L001	L03152	CHOKE, 1500 uH
L002	L03152	CHOKE, 1500 uH
L003	L03152	CHOKE, 1500 uH
Q001	Q04126	TRANSISTOR, PNP, 2N4126
Q002	Q04126	TRANSISTOR, PNP, 2N4126
Q003	Q04124	TRANSISTOR, NPN, 2N4124
Q004	Q04258	TRANSISTOR, PNP, PN 4258-18
Q005	Q04126	TRANSISTOR, PNP, 2N4126
Q006	Q04258	TRANSISTOR, PNP, PN 4258-18
Q007	Q04258	TRANSISTOR, PNP, PN 4258-18
Q008	Q04126	TRANSISTOR, PNP, 2N4126
Q009	Q04124	TRANSISTOR, NPN, 2N4124
R001	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R002	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R003	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R004	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R005	R05202	POT, 2K OHM TRIM
R006	R21512	RES, 5.1K OHMS 1/4W 2% M.FILM
R007	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R008	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R009	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R010	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R011	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R012	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R013	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R014	R05502	POT, 5K OHM TRIM
R015	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R016	R01562	RES, 5.6K OHMS 1/4W 5% C.FILM
R017	R01562	RES, 5.6K OHMS 1/4W 5% C.FILM
R018	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R019	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R020	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R021	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R022	R01330	RES, 33K OHMS 1/4W 5% C.FILM
R023	R05102	POT, 1K OHM TRIM
R024	R01331	RES, 33 OHMS 1/4W 5% C.FILM
R025	R01471	RES, 470 OHMS 1/4W 5% C.FILM

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
R026	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R027	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R028	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R029	R01152	RES, 1.5K OHMS 1/4W 5% C.FILM
R030	R05202	POT, 2K OHM TRIM
R031	R21512	RES, 5.1K OHMS 1/4W 2% M.FILM
R032	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R033	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R034	R01473	RES, 47K OHMS 1/4W 5% C.FILM
R035	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R036	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R037	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R038	R21154	RES, 150K OHMS 1/4W 2% M.FILM
R039	R21153	RES, 15K OHMS 1/4W 2% M.FILM
R040	R21154	RES, 150K OHMS 1/4W 2% M.FILM
R041	R01122	RES, 1.2K OHMS 1/4W 5% C.FILM
R042	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R043	R01475	RES, 4.7M OHMS 1/4W 5% C.FILM
R044	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R045	R01473	RES, 47K OHMS 1/4W 5% C.FILM
R046	R01563	RES, 56K OHMS 1/4W 5% C.FILM
R047	R01394	RES, 390K OHMS 1/4W 5% C.FILM
R048	R01105	RES, 1 M OHMS 1/4W 5% C.FILM
R049	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R050	R01221	RES, 220 OHMS 1/4W 5% C.FILM
R051	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R052	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R053	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R054	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R055	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R056	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R057	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R058	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R059	R01682	RES, 6.8K OHMS 1/4W 5% C.FILM
R060	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R061	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R062	R01391	RES, 390 OHMS 1/4W 5% C.FILM
R063	R01152	RES, 1.5K OHMS 1/4W 5% C.FILM
R065	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R066	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R067	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R068	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R069	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R070	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R071	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R072	R01822	RES, 8.2K OHMS 1/4W 5% C.FILM
R073	R01822	RES, 8.2K OHMS 1/4W 5% C.FILM
R074	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R075	R01104	RES, 100K OHMS 1/4W 5% C.FILM

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
R076	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R077	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R078	R05502	POT, 5K OHM TRIM
R079	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R080	R05502	POT, 5K OHM TRIM
R081	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R082	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R083	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R085	R01682	RES, 6.8K OHMS 1/4W 5% C.FILM
R086	R01182	RES, 1.8K OHMS 1/4W 5% C.FILM
R087	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R088	R01152	RES, 1.5K OHMS 1/4W 5% C.FILM
R089	R21153	RES, 15K OHMS 1/4W 2% M.FILM
U001	U01496	BALANCED MOD/DEMOD, LM1496
U002	U00324	QUAD OP AMP, LM324
U003	U01496	BALANCED MOD/DEMOD, LM1496
U004	U00339	QUAD COMPARATOR, LM339
U005	U4LS37	QUAD 2 INPUT NAND, 74LS37
U006	U4S140	4 INPUT DRIVER, 74S140
U007	U4LS37	QUAD 2 INPUT NAND, 74LS37
U008	U4LS90	DECADE COUNTER, 74LS90
U009	U4LS90	DECADE COUNTER, 74LS90
U010	U4LS90	DECADE COUNTER, 74LS90
U011	U4S132	QUAD SCHMITT NAND, 74S132
U012	U4S140	4 INPUT DRIVER, 74S140
U013	U4LS90	DECADE COUNTER, 74LS90
U014	U4LS90	DECADE COUNTER, 74LS90
U015	U4LS37	QUAD 2 INPUT NAND, 74LS37
U016	U4LS90	DECADE COUNTER, 74LS90
U017	ULS153	DUAL 4 INPUT MULTIPLEXER, 74LS153
U018	U4LS37	QUAD 2 INPUT NAND, 74LS37
U020	U4LS90	DECADE COUNTER, 74LS90
U021	U07805	REGULATOR, 5V 1.5 AMP, TL780-05CKC
U022	U78M12	REGULATOR, +12V 0.5 AMP, 78M12CT
U023	U79M12	REGULATOR, -12V 1 AMP, 7912CKC
VR02	VR04735	ZENER DIODE, 6.2V
W001	R01000	JUMPER, 0 OHMS
W002	R01000	JUMPER, 0 OHMS
W003	R01000	JUMPER, 0 OHMS
Y001	Y00011	XTAL, 10 MHZ

7.3 OUTPUT AMPLIFER ASSEMBLY

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
A4	002400	PC BOARD ASSEMBLY, OUTPUT
C001	C02103	CAP, .01 uF 25V DISC CERAMIC
C003	C09010	CAP, 1.0 UF 50V LITIC
C004	C02103	CAP, .01 uF 25V DISC CERAMIC
C005	C02103	CAP, .01 uF 25V DISC CERAMIC
C006	C02103	CAP, .01 uF 25V DISC CERAMIC
C007	C07220	CAP, 22 uF 25V LITIC
C008	C09010	CAP, 1.0 uF 50V LITIC
C009	C07220	CAP, 22 uF 25V LITIC
C010	C02103	CAP, .01 uF 25V DISC CERAMIC
C011	C02103	CAP, .01 uF 25V DISC CERAMIC
C012	C02103	CAP, .01 uF 25V DISC CERAMIC
C013	C02103	CAP, .01 uF 25V DISC CERAMIC
C014	C02103	CAP, .01 uF 25V DISC CERAMIC
C015	C02103	CAP, .01 uF 25V DISC CERAMIC
C017	C05121	CAP, 120PF MICA
C019	C02103	CAP, .01 uF 25V DISC CERAMIC
C020	C02103	CAP, .01 uF 25V DISC CERAMIC
C021	C02103	CAP, .01 uF 25V DISC CERAMIC
C022	C02103	CAP, .01 uF 25V DISC CERAMIC
C023	C05121	CAP, 120PF MICA (OPT 03)
C023	C05241	CAP, 240PF MICA
C025	C02103	CAP, .01 uF 25V DISC CERAMIC
C026	C02103	CAP, .01 uF 25V DISC CERAMIC
C027	C02103	CAP, .01 uF 25V DISC CERAMIC
C028	C05102	CAP, 1000PF MICA
C028	C05121	CAP, 120PF MICA (OPT 03)
C029	C05241	CAP, 240PF MICA
C030	C02103	CAP, .01 uF 25V DISC CERAMIC
C031	C02103	CAP, .01 uF 25V DISC CERAMIC
C032	C02103	CAP, .01 uF 25V DISC CERAMIC
C033	C02103	CAP, .01 uF 25V DISC CERAMIC
C034	C21123	CAP, 12000 pF 250V POLYCARB.
C035	C05121	CAP, 120 pF MICA (OPT 03)
C035	C05391	CAP, 390 pF MICA
C036	C02103	CAP, .01 uF 25V DISC CERAMIC (OPT 03)
C036	C09010	CAP, 1.0 uF 50V LITIC
C037	C02103	CAP, .01 uF 25V DISC CERAMIC
C038	C02103	CAP, .01 uF 25V DISC CERAMIC
C039	C05121	CAP, 120 pF MICA
C040	C05121	CAP, 120 pF MICA (OPT 03)
C040	C05201	CAP, 200 pF MICA
C041	C05102	CAP, 1000 pF MICA
C041	C05121	CAP, 120 pF MICA (OPT 03)
C042	C02103	CAP, .01 uF 25V DISC CERAMIC
C042	C05121	CAP, 120 pF MICA (OPT 03)
C043	C02103	CAP, .01 uF 25V DISC CERAMIC

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
C044	C09010	CAP, 1.0 uF 50V LITIC
C045	C02103	CAP, .01 uF 25V DISC CERAMIC
C046	C09010	CAP, 1.0 uF 50V LITIC
C047	C02103	CAP, .01 uF 25V DISC CERAMIC
C048	C09010	CAP, 1.0 uF 50V LITIC
C049	C02103	CAP, .01 uF 25V DISC CERAMIC
CR01	CR04148	DIODE, IN4148
CR02	CR00277	DIODE, IN277
CR03	CR00277	DIODE, IN277
CR04	CR00277	DIODE, IN277
CR05	CR04148	DIODE, IN4148
CR06	CR00277	DIODE, IN277
CR07	CR00277	DIODE, IN277
CR08	CR00277	DIODE, IN277
CR09	CR04148	DIODE, IN4148
CR10	CR00277	DIODE, IN277
CR11	CR00277	DIODE, IN277
CR12	CR00277	DIODE, IN277
CR13	CR04148	DIODE, IN4148
CR14	CR00277	DIODE, IN277
CR15	CR00277	DIODE, IN277
CR16	CR00277	DIODE, IN277
CR17	CR04148	DIODE, IN4148
J01A	J10014	HEADER, 6 PIN
J01B	J10014	HEADER, 6 PIN
J002	J10014	HEADER, 6 PIN
L001	L023R9	CHOKE, 3.9 uH
L002	L023R9	CHOKE, 3.9 uH
L003	L023R9	CHOKE, 3.9 uH (OPT 03)
L003	L028R2	CHOKE, 8.2 uH
L004	L023R9	CHOKE, 3.9 uH (OPT 03)
L004	L028R2	CHOKE, 8.2 uH
L005	L02390	CHOKE, 39 uH
L005	L023R9	CHOKE, 3.9 uH (OPT 03)
L006	L02390	CHOKE, 39 uH
L006	L023R9	CHOKE, 3.9 uH (OPT 03)
L007	L023R9	CHOKE, 3.9 uH (OPT 03)
L007	L03391	CHOKE, 390 uH
L008	L023R9	CHOKE, 3.9 uH (OPT 03)
L008	L03391	CHOKE, 390 uH
L009	L04000	INDUCTOR, TOROID (OPT 03)
L010	L04000	INDUCTOR, TOROID (OPT 03)
L011	L04000	INDUCTOR, TOROID (OPT 03)
L012	L04000	INDUCTOR, TOROID (OPT 03)
L013	L04000	INDUCTOR, TOROID (OPT 03)
Q001	Q04258	TRANSISTOR, PNP, PN 4258-18
Q002	Q04258	TRANSISTOR, PNP, PN 4258-18
Q003	Q04124	TRANSISTOR, NPN, 2N4124
Q004	Q03565	TRANSISTOR, NPN, 2N3565

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
Q005	Q03565	TRANSISTOR, NPN, 2N3565
Q006	Q04126	TRANSISTOR, PNP, 2N4126
R001	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R002	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R003	R01391	RES, 390 OHMS 1/4W 5% C.FILM
R004	R01681	RES, 680 OHMS 1/4W 5% C.FILM
R005	R01182	RES, 1.8K OHMS 1/4W 5% C.FILM
R006	R01331	RES, 330 OHMS 1/4W 5% C.FILM
R007	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R008	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R009	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R010	R01270	RES, 27 OHMS 1/4W 5% C.FILM
R011	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R012	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R013	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R014	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R015	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R016	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R017	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R018	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R019	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R020	R01000	JUMPER, 0 OHMS
R021	R01224	RES, 220K OHMS 1/4W 5% C.FILM
R022	R01126	RES, 12M OHMS 1/4W 5% C.FILM(OPT 03)
R022	R01475	RES, 4.7M OHMS 1/4W 5% C.FILM
R024	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R025	R01183	RES, 18K OHMS 1/4W 5% C.FILM
R026	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R027	R01101	RES, 100 OHMS 1/4W 5% C.FILM
U001	U4LS20	DUAL NAND, 74LS20
U002	U4S140	4 INPUT DRIVER, 74S140
U003	U4LS37	QUAD 2 INPUT NAND, 74LS37
U004	U4LS37	QUAD 2 INPUT NAND, 74LS37
U005	U4LS90	DECADE COUNTER, 74LS90
U006	ULS112	DUAL J-K F/F, 74LS112
U007	U4LS90	DECADE COUNTER, 74LS90
U008	U4S140	4 INPUT DRIVER, 74S140
U009	U4S140	4 INPUT DRIVER, 74S140
U010	U78T12	REGULATOR, 78T12ACT (OPT 03)
W001	R01000	JUMPER, 0 OHMS
W002	R01000	JUMPER, 0 OHMS
W003	R01000	JUMPER, 0 OHMS
W004	R01000	JUMPER, 0 OHMS
W005	R01000	JUMPER, 0 OHMS
W006	R01000	JUMPER, 0 OHMS
W007	R01000	JUMPER, 0 OHMS
W008	R01000	JUMPER, 0 OHMS

7.4 OSCILLATOR, POWER SUPPLY ASSEMBLY

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
A5	002500	PC BOARD ASSY, OSC/PWR SUPPLY
C001	C12226	CAP, 22 uF 15V TANT
C003	C02103	CAP, .01 uF 25V DISC CERAMIC
C004	C15685	CAP, 6.8 uF 35V TANT
C005	C12226	CAP, 22 uF 15V TANT
C006	C22105	CAP, 1 uF 100V POLYESTER
C007	C02103	CAP, .01 uF 25V DISC CERAMIC
C008	C09471	CAP, 470 uF 50V LITIC
C009	C09471	CAP, 470 uF 50V LITIC
C010	C15685	CAP, 6.8 uF 35V TANT
C011	C05102	CAP, 1000 pF MICA
CR01	CR05059	RECTIFIER,1A,200 PIV
CR02	CR05059	RECTIFIER,1A,200 PIV
CR03	CR05059	RECTIFIER,1A,200 PIV
CR04	CR05059	RECTIFIER,1A,200 PIV
CR05	CR04148	DIODE, IN4148
CR06	CR05059	RECTIFIER,1A,200 PIV
CR07	CR05059	RECTIFIER,1A,200 PIV
CR08	CR04148	DIODE, IN4148
J001	J10014	HEADER, 6 PIN
J002	J10014	HEADER, 6 PIN (2)
Q001	Q03563	TRANSISTOR, NPN, 2N3563
Q002	Q04126	TRANSISTOR, PNP, 2N4126
Q003	Q04124	TRANSISTOR, NPN, 2N4124
Q004	Q00L51	TRANSISTOR, PNP, MPS-L51
Q005	Q04126	TRANSISTOR, PNP, 2N4126
Q006	Q00L51	TRANSISTOR, PNP, MPS-L51
Q007	Q04126	TRANSISTOR, PNP, 2N4126
Q008	Q04124	TRANSISTOR, NPN, 2N4124
Q009	Q00034	TRANSISTOR, PNP, TIP34A
Q010	Q00033	TRANSISTOR, NPN, TIP33A
R002	R01221	RES, 220 OHMS 1/4W 5% C.FILM
R003	R01330	RES, 33K OHMS 1/4W 5% C.FILM
R004	R07203	POT, 20K OHM 18 TURN TRIM
R005	R11363	RES, 36K OHMS 1/4W 5% M.FILM
R006	R21823	RES, 82 K OHMS 1/4W 2% M.FILM
R009	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R010	R01182	RES, 1.8K OHMS 1/4W 5% C.FILM
R011	R01333	RES, 33K OHMS 1/4W 5% C.FILM
R012	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R013	R03182	RES, 1.8K OHMS 1W 5% C.COMP
R014	R022R4	RES, 2.4 OHMS 1/2W 5% C.FILM
R015	R01273	RES, 27K OHMS 1/4W 5% C.FILM
R016	R01273	RES, 27K OHMS 1/4W 5% C.FILM
R017	R01222	RES, 2.2K OHMS 1/4W 5% C.FILM
R018	R05103	POT, 10K OHM TRIM
R019	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
R020	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R021	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R022	R11123	RES, 12K OHMS 1/4W 5% M.FILM
R023	R03182	RES, 1.8K OHMS 1W 5% C.COMP
R024	R01470	RES, 47 OHMS 1/4W 5% C.FILM
R025	R05102	POT, 1K OHM TRIM
R026	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R027	R11392	RES, 3.9K OHMS 1/4W 5% M.FILM
R028	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R029	R01512	RES, 5.1K OHMS 1/4W 5% C.FILM
U001	002590	OSCILLATOR
U002	U00723	VOLTAGE REGULATOR, 723
VR01	VR05242	ZENER DIODE, 12V
W001	R01000	JUMPER, 0 OHMS
W002	R01000	JUMPER, 0 OHMS
W003	R01000	JUMPER, 0 OHMS
W004	R01000	JUMPER, 0 OHMS

7.5 FREQUENCY TIME COMPARATOR ASSEMBLY

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
A6	018100	PC BOARD ASSEMBLY, FTC
C001	C26104	CAP, .1 uF 50V CERAMIC MONO
C002	C26104	CAP, .1 uF 50V CERAMIC MONO
C003	C26104	CAP, .1 uF 50V CERAMIC MONO
C004	C26104	CAP, .1 uF 50V CERAMIC MONO
C005	C26104	CAP, .1 uF 50V CERAMIC MONO
C006	C26104	CAP, .1 uF 50V CERAMIC MONO
C007	C26104	CAP, .1 uF 50V CERAMIC MONO
C008	C26104	CAP, .1 uF 50V CERAMIC MONO
C009	C26104	CAP, .1 uF 50V CERAMIC MONO
C010	C26104	CAP, .1 uF 50V CERAMIC MONO
C011	C26104	CAP, .1 uF 50V CERAMIC MONO
C012	C26104	CAP, .1 uF 50V CERAMIC MONO
C013	C26104	CAP, .1 uF 50V CERAMIC MONO
C016	C05150	CAP, 15 pF MICA
C017	C05100	CAP, 10 pF MICA
C018	C26104	CAP, .1 uF 50V CERAMIC MONO
C019	C26104	CAP, .1 uF 50V CERAMIC MONO
C020	C26104	CAP, .1 uF 50V CERAMIC MONO
C021	C09010	CAP, 1.0 uF 50V LITIC
C022	C05500	CAP, 50 pF MICA
C024	C07220	CAP, 22 uF 25V LITIC
C025	C26104	CAP, .1 uF 50V CERAMIC MONO
C026	C26104	CAP, .1 uF 50V CERAMIC MONO

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
C027	C26104	CAP, .1 uF 50V CERAMIC MONO
C028	C05101	CAP, 100 pF MICA
C029	C26104	CAP, .1 uF 50V CERAMIC MONO
C030	C26104	CAP, .1 uF 50V CERAMIC MONO
C031	C26104	CAP, .1 uF 50V CERAMIC MONO
C032	C05101	CAP, 100 pF MICA
C033	C26104	CAP, .1 uF 50V CERAMIC MONO
J01A	J02006	HEADER, 6 PIN
J01B	J02006	HEADER, 6 PIN
J002	J02006	HEADER, 6 PIN
J003	J02006	HEADER, 6 PIN
J004	J02006	HEADER, 6 PIN
J05A	J02006	HEADER, 6 PIN
J05B	J02006	HEADER, 6 PIN
R001	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R002	R07203	POT, 20K OHM 18 TURN TRIM
R008	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R009	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R010	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R011	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R012	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R013	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R014	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R015	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R017	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R018	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R019	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R020	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R021	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R022	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R023	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R024	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R025	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R029	R01121	RES, 120 OHMS 1/4W 5% C.FILM
R030	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R031	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R032	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R033	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R034	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
RP01	R36103	RES NETWORK 10K OHM SIP
RP02	R36103	RES NETWORK 10K OHM SIP
U001	S00336	SWITCH, 8 POS DIP
U002	U08254	PROGRAM INTERVAL TIMER, 8254
U003	U08254	PROGRAM INTERVAL TIMER, 8254
U004	U82542	PROGRAM INTERVAL TIMER, 8254-2
U005	U01220	2K X 8 RAM, DS1220AB
U006	EP0006	EPROM, FTC 3.11, 27C64
U006	EP0007	EPROM, FTC 3.21, 27C64
U006	EP0015	EPROM, FTC 3.31, 27C64

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
U007	U08255	PROGRAMMABLE INTERFACE, 8255A-5
U008	ULS138	3 INPUT MULTIPLEXER, 74LS138
U009	U4LS86	QUAD EXCLUSIVE OR, 74LS86
U010	ULS109	DUAL J-K F/F, 74LS109A
U011	ULS158	QUAD 2 INPUT MULTIPLEXER, 74LS158
U012	ULS373	OCTAL D-LATCH, 74LS373
U013	U08031	8-BIT MICROCOMPUTER, P8031
U014	U07417	HEX O.C. BUFFER, 7417
U015	U00411	OP AMP/LOW OFFSET, LF411
U016	U01230	12 BIT D/A, DAC1230
U018	S00336	SWITCH, 8 POS DIP
U019	U00324	QUAD OP AMP, LM324
U020	U4LS14	HEX SCHMITT INVERTER, 74LS14
U021	U07417	HEX O.C. BUFFER, 7417
U022	ULS109	DUAL J-K F/F, 74LS109A
U023	U01488	QUAD LINE DRIVER, 1488
U024	ULS109	DUAL J-K F/F, 74LS109A
U025	ULS109	DUAL J-K F/F, 74LS109A
U026	U6LS31	QUAD RS422 DRIVER, 26LS31
U027	U01489	QUAD LINE RECEIVER, 1489
U028	U01232	POWER MONITOR, DS1232
W001	R01000	JUMPER, 0 OHMS
W002	R01000	JUMPER, 0 OHMS
Y001	Y00014	XTAL, 11.059 MHz

7.6 ANCILLARY KIT

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
0001	W01000	LINE CORD
0002	P01115	PLUG, 15 PIN MOLEX
0003	P01100	PIN, MOLEX CRIMP (TOTAL 15 PINS)
0004	004490	TERMINATOR, 50 OHM, DC ISOLATED (TOTAL 4, OPT 03)
0005	P00002	PLUG, BNC, UG-88/U
0006	MAN8164	MANUAL 8164
F001	F00R75	FUSE, 3/4A, 3AG
F001	F001R2	FUSE, 1-1/4A, 3AG, (OPT 03)
F002	F00R38	FUSE, 3/8A, 3AG

MODEL 8164

MANUAL ERRATA

THIS SECTION CONTAINS MANUAL CORRECTIONS OR CHANGES MADE TO THE INSTRUMENT AFTER THE PRINTING OF THIS MANUAL.

ERRATA VERSION 3.1 - 08/93

The Model 8206 Loop Antenna and the Model 8211 Antenna Mount are discontinued. Spectracom now offers two antennas, the Model 8206A Loop Antenna and the Model 8208 Whip Antenna. The antenna mount is now available as Model 8213.

Please replace Sections 1.4 through 1.8 of the installation section of the manual with the following paragraphs.

The Model 8206A is a direct replacement for the Model 8206 Loop Antenna. Any reference to the Model 8206 other than the following errata sections may be substituted with the Model 8206A.

1.4 MODEL 8206A LOOP ANTENNA

The Model 8206A Loop Antenna reliably receives the 60 kHz WWVB transmission in field strengths of 50 μV/meter or greater. The majority of the United States exceeds 50 μV/meter as shown in Figure 1-3 Measured Field Intensity Contours. In locations having less than 50 μV/meter field strength, the Model 8207 Preamplifier is required. Refer to Section 1.8 for additional information. The equivalent electrical height of the Model 8206A is 5.0 cm.

The Model 8206A consists of a wound ferrite core surrounded by a Faraday shield which aids in noise rejection. The received signal is amplified by an internal preamplifier and output to the receiver. The preamp is powered by the receiver over the antenna coax. The antenna is packaged in a PVC housing measuring 10 inches long and 2.8 inches in diameter. The assembled antenna weight is 2.5 pounds.

The Model 8206A is a directional antenna. The tubular housing must be positioned broadside to Fort Collins, Colorado, (See Figure 1-4) and horizontal to the ground to allow maximum signal reception. No signal will be received if the tube points directly toward the transmitter site, as the antenna pattern nulls are located off the ends of the tube. The great circle map shown in Figure 1-3 is used to determine the correct antenna orientation per receiver location. The antenna position may be optimized using the AGC measurement described in Section 2.8, Signal Strength Measurement.

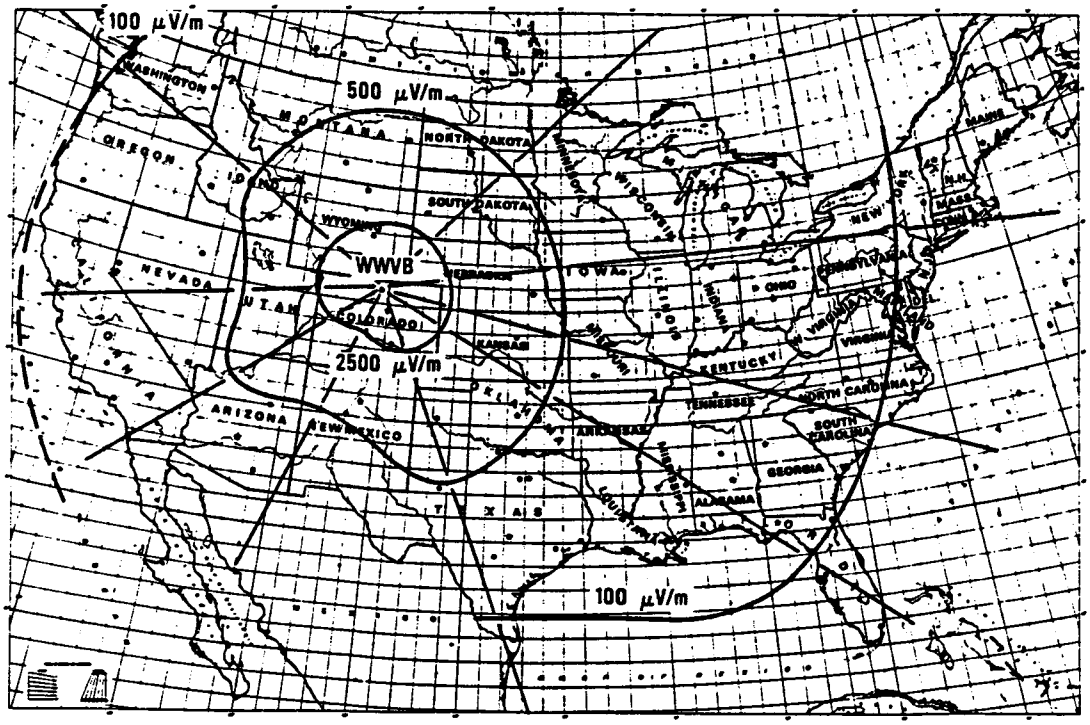
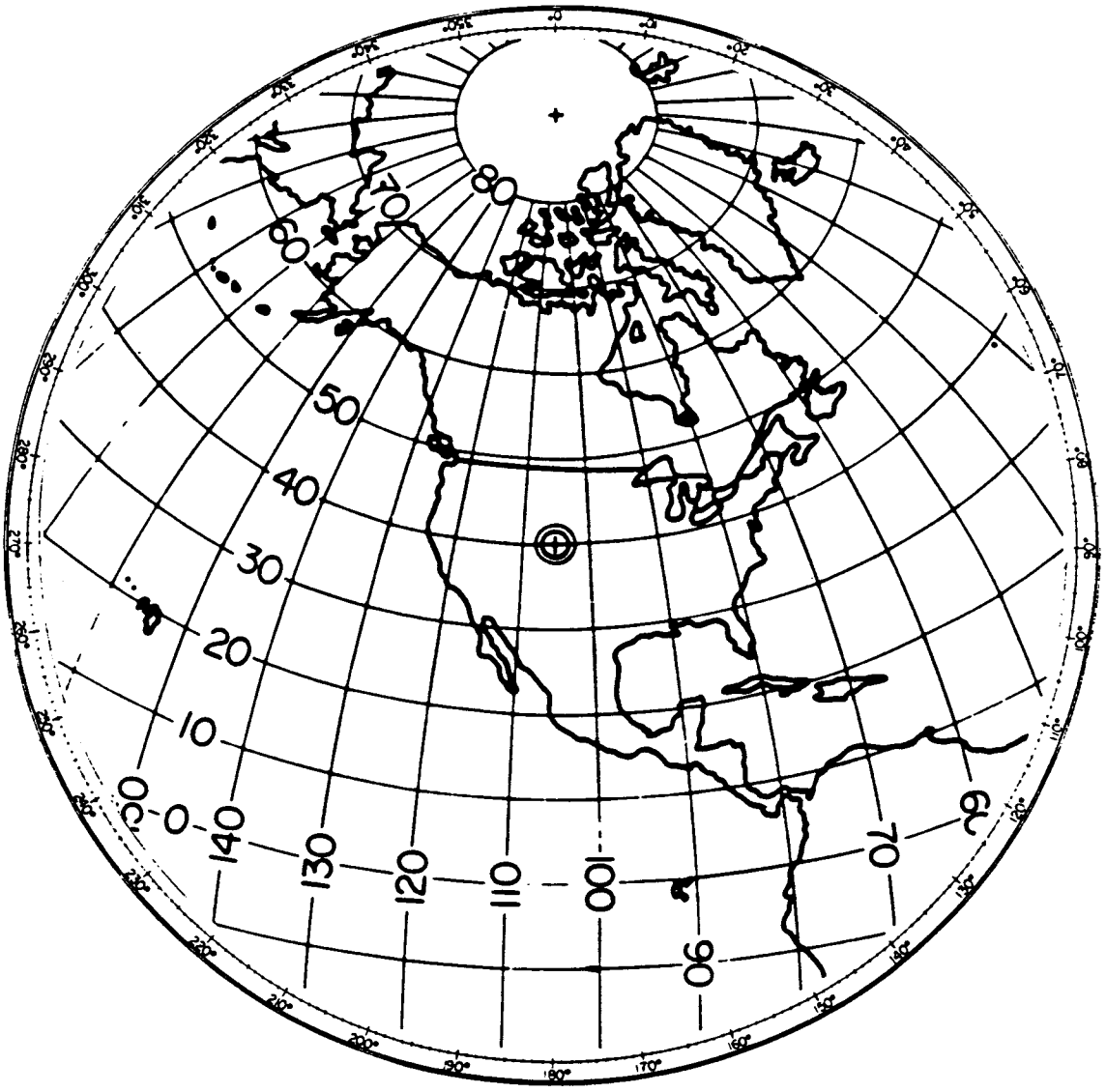


FIGURE 1-2 MEASURED FIELD INTENSITY CONTOUR WWVB @ 13 KW ERP



TO AIM ANTENNA AT FORT COLLINS, COLORADO, DETERMINE COMPASS HEADING FROM THIS MAP.

Draw a straight line from the receiver location through Fort Collins, Colo. at the center of the map. Continue until the line intersects the outer ring. The point at which the line intersects the outer ring indicates the compass heading for Fort Collins from your location.

FIGURE 1-3 GREAT CIRCLE MAP CENTERED ON FORT COLLINS, COLORADO

1.5 MODEL 8208 WHIP ANTENNA

The Model 8208 Whip Antenna provides performance equal to the Model 8206A Loop Antenna at a reduced cost. The Model 8208 may be used in field strengths of 50 μV/meter or greater. The Model 8208 contains a preamplifier housed in a weather-proof enclosure. The preamplifier is powered by the receiver over the antenna coax cable. The Model 8208 is 58.5 inches long and weighs 1.3 pounds.

1.6 ANTENNA LOCATION

The antenna should be mounted a minimum of 25 feet from the receiver to prevent regeneration. The antenna MUST NOT be positioned next to the receiver or on top of it. Doing so will make the results obtained with the equipment meaningless even though the green lock lamp on the receiver front panel may be lit.

In system installations where more than one Spectracom antenna is used, a minimum separation of 10 feet between antennas is recommended.

The antenna must be at least three feet from any steel beams, roof decking, pipes, etc., as metal will detune the antenna and can cause as much as 20 dB degradation of the signal-to-noise ratio. The antenna must not be mounted under a metal roof or inside a building with heavy steel structural supports, as these shield the antenna from the signal. Roof tops are generally good if a clear shot toward Fort Collins is available without being blocked by a large steel structure. Attics are ideal sites if the roof and rafters are not metallic. The signal-to-noise ratio will be optimized if the antenna is located as far as possible from local RF noise sources such as TV sets, or fluorescent or neon lamps that blink or sputter on and off. Any equipment containing a switching power supply is a probable cause of interference.

1.7 ANTENNA INSTALLATION

Mount the antenna where it will not be disturbed. Antenna height is not critical as the 60 kHz signal is primarily a ground wave. Holding the antenna two to three feet off the ground or rooftop is adequate. Each antenna includes a two-foot mast assembly and two hose clamps to simplify installation. A typical roof-top installation is illustrated in Figure 1-4. Spectracom offers an aluminum base, Model 8213, for installations where vent pipe mounting is not practical or desired.

NOTE: THE MODEL 8206A IS A DIRECTIONAL ANTENNA. FOLLOW THE INSTRUCTIONS FOUND ON FIGURE 1-3 TO AIM THE ANTENNA CORRECTLY.

HANDLE THE ANTENNA WITH CARE. DROPPING OR ROUGH HANDLING MAY CRACK THE FERRITE CORE, POSSIBLY DETUNING THE ANTENNA, RENDERING IT USELESS.

Spectracom recommends RG-58C/U coax for the antenna cable, though any 50-ohm coax with superior specifications may be used. The antenna coax is used to provide the antenna with its DC operating voltage and the receiver with the amplified WWVB signal. Because of low attenuation characteristics at 60 kHz and the very low power requirement of the antenna (10 mW), cable lengths up to 1,500 feet are possible if care is taken to avoid routing the cable near noise sources.

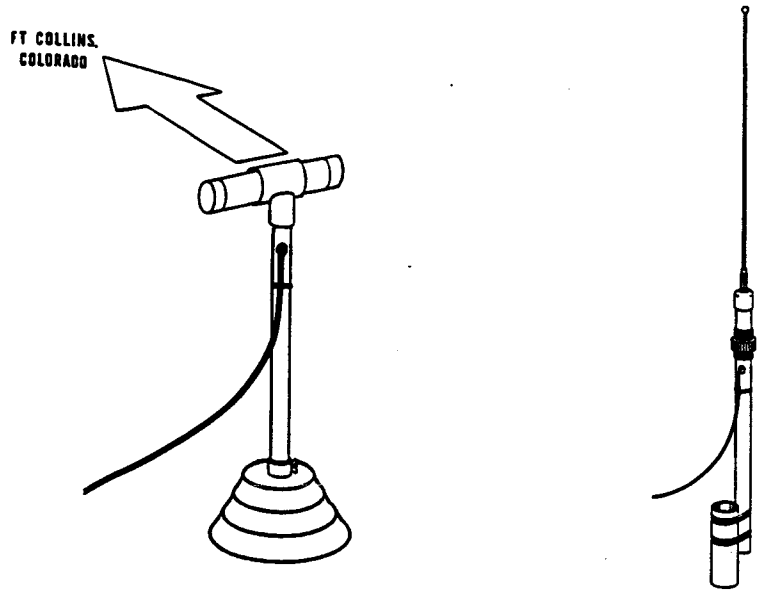


FIGURE 1-4 ANTENNA MOUNTING

1.8 MODEL 8207 PREAMPLIFIER INSTALLATION

The Spectracom Model 8207 Preamplifier is a low noise, tuned, 60-kHz line amplifier used in the antenna feed line wherever the WWVB signal strength is less than 50 μV/meter at the Antenna or less than 0.4 μV at the receiver antenna terminal. Typical locations where the preamplifier is probably required are Hawaii, Alaska, Puerto Rico, and the Canal Zone. Figure 1-2 shows the measured average signal strength for the contiguous 48 states. Atmospheric conditions may cause short term degradation of field intensity. The Model 8207 Preamplifier provides approximately 40 dB of gain between the antenna and receiver increasing sensitivity to 4.0 nanovolts.

The preamplifier is connected in the antenna feed line with **INPUT** connected to the antenna and **OUTPUT** connected to the receiver. Because of the high gain of the system, it is recommended that the preamplifier be located at least 10 feet away from the receiver. The antenna must be least 25 feet beyond the preamplifier. Switch A1S1 of the receiver RF Amplifier must be set at its right-hand position, marked PREAMP or P, prior to equipment turn-on, to apply DC voltage to the Model 8207 on the antenna feed line. If the preamplifier is removed from the system, the switch must be placed in the left-hand position, marked ANT or A prior to turn-on.