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COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

7A42
LOGIC TRIGGERED VERTICAL AMPLIFIER

SERVICE (VOLUME 1)

For Qualified Service Personnel Only

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

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Product Group 42

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT)

TABLE OF CONTENTS (CONT)

TABLE OF CONTENTS (CONT)

RELATED DOCUMENTATION

For information on related 7A42 documentation refer to General Information, Section 1 of this manual under Technical Manuals and Standard Accessories.

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (CONT)

The illustrations in section 7 are located near their associated diagrams on the foldout page.

LIST OF TABLES

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL


Static-Sensitive Devices


This symbol indicates where applicable cautionary or other information is to be found.

AS MARKING ON EQUIPMENT


DANGER—High voltage


Protective ground (earth) terminal.


ATTENTION—refer to manual.

WARNINGS

POWER SOURCE

This product is intended to operate in a mainframe connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, plug the mainframe power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective-ground connection by way of the grounding conductor in the mainframe power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating), can render an electric shock.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gasses.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary

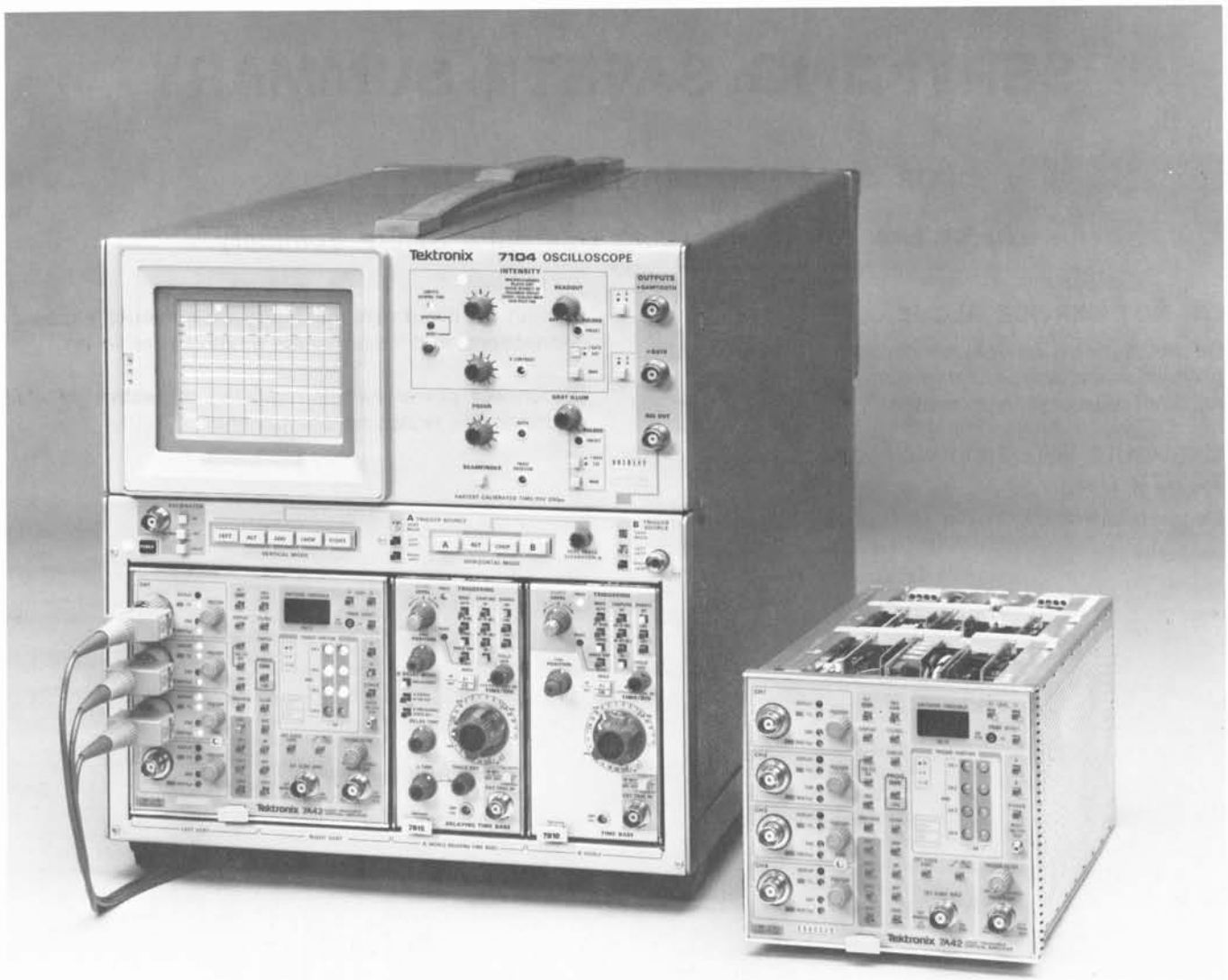
DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.



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7A42 FEATURES

The 7A42 Logic Triggered Vertical Amplifier is a four channel, wide bandwidth, plug-in unit, compatible with Tektronix 7000-series Oscilloscopes. It was specifically designed to display and make measurements on digital logic signals in the TTL, ECL and CMOS logic families. While the display output from the 7A42 is analog, the trigger output is digital and is comprised of a user selectable Boolean function of the four input channels. A fifth TRIGGER VIEW trace depicts either the trigger function output or the external clock input.

GENERAL INFORMATION

This section contains a basic content description of both the Operators and Service manuals, information on instrument installation, power requirements, packaging for shipment, Standard Accessories, Optional Accessories, Specifications and a dimensional drawing of the 7A42. The specification portion consists of three tables: Electrical, Environmental, and Physical Characteristics.

TECHNICAL MANUALS

An operators and two service manuals are supplied with your 7A42 as standard accessories. The following information outlines the content of these manuals.

Operators Manual

The Operators Manual is divided into the following four sections:

Section 1—GENERAL INFORMATION contains content descriptions of the Operators and Service manuals, instrument description, mainframe and plug-in compatibility, packaging instructions and instrument specifications.

Section 2—OPERATING INSTRUCTIONS contains a block diagram description, a front-panel drawing and brief description of controls, connectors and indicators. Get-Acquainted Exercises provide a basic operating procedure for the first-time user followed by a systematic demonstration of all front-panel controls. A detailed description of all front-panel controls is also given in this section.

Section 3—APPLICATIONS gives examples of how to use the 7A42 to make some difficult measurements.

Section 4—INSTRUMENT OPTIONS contains a description of available options.

Service Manual

WARNING

The following service instructions are for use by qualified personnel only. To avoid personal injury, do not perform any service other than that contained in the operating instructions unless you are qualified to do so. Refer to Operators Safety Summary and Service Safety Summary prior to performing any service.

The service manual is divided into 2 volumes. Volume 1 contains the following:

Section 1—GENERAL INFORMATION contains content descriptions of the Operators and Service manuals, mainframe and plug-in compatibility, packaging instructions, instrument specifications, and operating instructions.

Section 2—THEORY OF OPERATION contains basic and general circuit analysis that is useful for servicing the instrument.

Section 3—MAINTENANCE describes preventive maintenance procedures, conventional troubleshooting and diagnostic troubleshooting procedures with detailed instructions for replacing assemblies, subassemblies, and individual components.

Section 4—CHECKS AND ADJUSTMENT contains procedures to check the operational performance and electrical characteristics of the instrument. Procedures also include methods for adjustment of the instrument to meet specifications.

Section 5—INSTRUMENT OPTIONS contains a description of available options.

Section 6—REPLACEABLE ELECTRICAL PARTS contains information necessary to order replaceable parts and assemblies related to the electrical functions of the instrument.

Section 7—DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS includes detailed circuit schematics, locations of assembled boards within the instrument, voltage and waveform information and circuit board component locators.

Section 8—REPLACEABLE MECHANICAL PARTS includes information necessary to order replaceable mechanical parts and shows exploded drawings which identify assemblies.

Volume 2 of the service manual contains signature analysis tables to be used with the diagnostic information provided in the Maintenance section of the Volume 1 service manual.

INSTALLATION

INITIAL INSPECTION

This instrument was inspected both mechanically and electrically before shipment. It should be free of mars or scratches and should meet or exceed all electrical specifications. To confirm this, inspect the instrument for physical damage incurred in transit and check the basic instrument functions by performing the Performance Check Procedure in the Checks and Adjustment section of this manual. If there is damage or deficiency, contact your local Tektronix Field Office or representative.

OPERATING TEMPERATURE

The 7A42 can be operated where the ambient air temperature is from 0° to +50° C and can be stored in ambient temperatures from −55° to +75° C. After storage at temperatures outside the operating limits, allow the chassis temperature to reach operating limits before applying power.

INSTALLING THE 7A42 IN THE MAINFRAME

The 7A42 is designed to operate in the two center or the two left plug-in compartments of a Tektronix 7000-series oscilloscope mainframe.

NOTE

Switch off the mainframe power before installing or removing the 7A42.

To install the 7A42 in the mainframe, align the grooves in the top and bottom of the instrument with the guides at the top and bottom of the plug-in compartment. Then push the 7A42 in until its front panel is flush with the front panel of the mainframe.

To remove the 7A42 from its host mainframe, pull the release latch (see Fig. 1-1) to disengage the unit from the mainframe, then pull the 7A42 straight out from the plug-in compartment leaving the mainframe on the bench.

MAINFRAME COMPATIBILITY

The 7A42 is compatible with all Tektronix 7000 series mainframes. In four-wide plug-in compartment mainframes, it can be installed in either the two left or two center plug-in compartments. When used in the two left compartments, select the Left Vertical Mode to display the analog signals. The associated time base plug-in Trigger Source should be Left Vertical with the time-base trigger controls set to Auto or Norm, Dc, Internal, Slope to +, with the Level control centered. The A Then B Gate Output can be picked off from the RIGHT VERTICAL TRIGGER SOURCE by a 7D11 or 7D15 from either horizontal compartment. In three-wide plug-in compartment mainframes, the 7A42 must be used in the two left compartments in a similar way.

When the 7A42 is installed in the center two plug-in compartments of a four compartment mainframe; set the

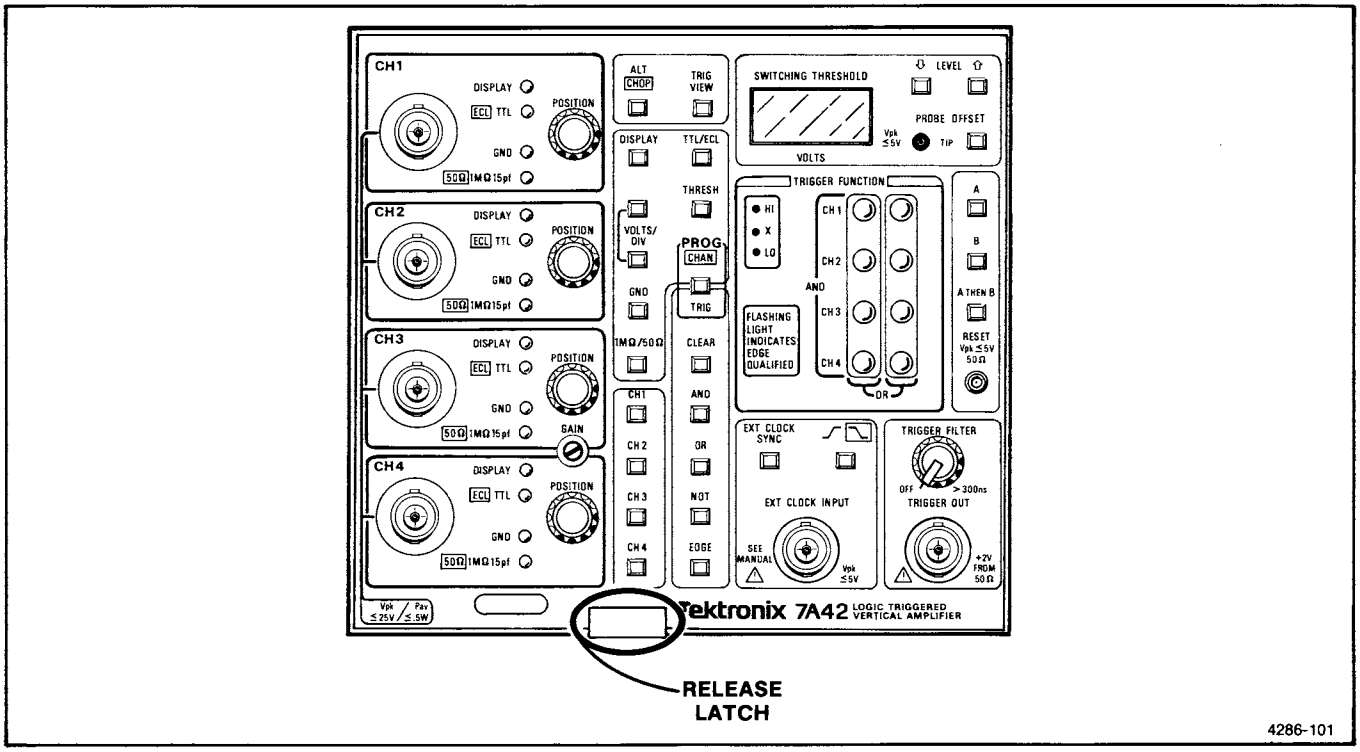

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Figure 1-1. 7A42 release latch.

mainframe Vertical Mode and Trigger Source to Right Vertical. The mainframe A Then B Gate Output can not be used in this configuration, however, the A Then B Gate is still available at the front-panel TRIGGER OUT bnc connector.

Since all analog channels are sent out the 7A42's left interface connector, it cannot use the full capabilities of a dual beam oscilloscope such as the 7844, R7844, and the 7612D. However, it has full compatibility with these mainframes in a single beam configuration.

Since the 7A42 uses the mainframe crt readout to display the channel volts per division and error warning messages, the 7A42 is not recommended for use in mainframes without readout.

If the 7A42 is used with two time-base units in a four compartment mainframe where Chop has been selected as the Horizontal Mode, and if exactly four traces are to be displayed by the 7A42, two of the traces may synchronize to one time base while the other two traces synchronize to the other time base. To prevent this from happening, one trace should be removed, or a fifth trace should be added to the mainframe crt display (even if it is positioned off screen so it cannot be seen). With one, two, three, or five traces, the channel display will not synchronize to the horizontal chop frequency.

The 7A42 is compatible with the 7854 Oscilloscope mainframe when the 7854 is operated in real-time. However, when the 7854 is operated in digital storage, and waveform and readout acquisition is desired, the 7A42-7854 mode should be selected by moving jumper P540 to the 7854 mode. To locate P540 refer to Figure 3-7 in the Maintenance section of this manual. Once the 7A42-7854 mode has been selected, proper readout and waveform acquisition can be guaranteed with the following 7A42 display conditions:

1. Any single channel displayed alone (CH1, CH2, CH3, CH4, or TRIG VIEW).

2. Channels 1 and 2 only displayed together, ALT display mode selected.

3. Channels 3 and 4 only displayed together, ALT display mode selected.

Refer to the Applications section in the Operators manual for further information.

PACKAGING FOR SHIPMENT

If this instrument is to be shipped by commercial transportation, we recommend that the instrument be packaged in the original manner. The carton and packaging material in which your instrument was shipped should be saved and used for this purpose.

NOTE

Package and ship Plug-Ins and Mainframes separately.

If this instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: Owner of the instrument (with address), the name of a person at your firm who can be contacted, complete instrument type and serial number, and a description of the service required.

If the original package is unfit for use or not available, package the instrument as follows:

1. Obtain a corrugated cardboard shipping carton having inside dimensions at least six inches greater than the instrument dimensions; refer to Table 1-1 for carton test strength requirements.

2. Enclose the instrument with polyethylene sheeting or equivalent to protect the finish of the instrument.

3. Cushion the instrument on all sides by tightly packaging dunnage or urethane foam between the carton and the instrument, allowing three inches of packaging on each side.

4. Seal the carton with shipping tape or with an industrial stapler.

5. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

TABLE 1-1
Shipping Carton Test Strength

Gross Weight (lb)	Carton Test Strength (lb)
0	200
10-30	275
30-120	375
120-140	500

SPECIFICATION

The electrical characteristics listed in Table 1-2 apply when the following conditions are met: (1) Adjustment of the instrument must have taken place at an ambient temperature between +20° and +30° C, (2) the instrument is allowed a 20-minute warm-up period, (3) specifications are valid at an ambient temperature of 0° to +50° C, unless otherwise stated, (4) the instrument must be in an environment that meets the limits described in Table 1-3, (5) the instrument must be operated in a calibrated 7000-series mainframe.

Any applicable conditions not listed above may be stated as part of the characteristic. Environmental characteristics are listed in Table 1-3 and Physical characteristics are listed in Table 1-4.

TABLE 1-2
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
DISPLAY		
Deflection Factor		
Calibrated Range at Input BNC Connector		
TTL (CMOS) Family	0.1, 0.2, 0.5 V/div.	
ECL Family	20, 50, 100 mV/div.	
Calibrated Range through a 10X Probe		
TTL (CMOS) Family		1, 2, 5 V/div.
ECL Family		0.2, 0.5, 1 V/div.
Channel to Channel Gain Match	Within 2% in ECL Logic Family, 20 mV/div, 1 Megohm input impedance.	
Gain Ratio Accuracy within the same Channel	Within 2% of indicated deflection factor relative to ECL Logic Family, 20 mV/div, 1 Megohm input impedance.	
GAIN Range		Permits adjustment of deflection factor for calibrated operation with any calibrated 7000-series mainframe. Adjustable at least +4% to -4% from calibrated setting.
Frequency Response		
Bandwidth	350 MHz in 7104, 0°-35°C mainframe ambient temperature. Refer to Tektronix Product Catalog 7000-Series Oscilloscope System Specification for system bandwidths.	

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
DISPLAY (CONT)		
Input Signal Dynamic Range		
Maximum Signal Voltage at tip of 10X Probe		
TTL (CMOS) Family		±30 V.
ECL Family		±6 V.
Output Dynamic Range		Limited to the CRT display area. Mainframe Vertical Trace Separation should not be used to bring an off-screen signal onto screen.
Maximum Input Voltage		
1 Megohm		25 V (dc + peak ac) 36 MHz or less, derated linearly to 3 V (peak ac) at 300 Mhz.
50 Ohm		5 V RMS during any 1 ms time interval. Active internal protection opens all inputs if overvoltage is applied to any channel.
50-Ohm Input Protection Reaction Time		
Maximum time to open input with applied overvoltage of:		
10 V DC	10 seconds.	
15 V DC	1 second.	
20 V DC	0.5 second.	
Input Characteristics		
Input Coupling		
DC		Incoming signal is dc-coupled to the amplifier.
GND		A grounded input is actually open at the input BNC, (i.e., 1 Megohm or 50 Ohm termination is disconnected). Internally, the amplifier input is grounded to provide a zero-volt input reference.
High Impedance	1 Megohm ±1%, in parallel with approximately 15 pF.	
Low Impedance	50 ohms ±1 ohm at dc.	
VSWR		≤1.15:1, dc to 300 MHz.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
DISPLAY (CONT)		
VOLTS/DIV Shift	0.2 divisions or less shift when VOLTS/DIV is changed in either TTL or ECL Families or between Families.	
POSITION Range		At least +7 divisions to −7 divisions but less than +9 divisions to −9 divisions from graticule center with gain calibrated.
Displayed Noise		Grounded input at maximum sensitivity, 7A42 triggered on another channel, tested at 1 ms/div and 10 ns/div, not more than 0.02 divisions RMS, as measured in a 7854.
DC Drift		
Drift with Time		Not more than 0.2 divisions in any 10 minutes after twenty minute warm-up (ambient temperature and line voltage constant).
Drift with Temperature		Not more than 0.2 divisions for 10° C ambient change (line voltage constant).
Differential Delay Between Any Two Channels, set to Same Logic Family and VOLTS/DIV	200 ps maximum.	
Plug-in Delay Time		Typically 25 ns from channel input to A11 and B11 of mainframe interface connector.
Channel to Channel Crosstalk		Typically less than 0.05 divisions with logic signal inputs applied through a 10X probe.
Chop Frequency		See mainframe manual for specifications.
TRIG VIEW or External Clock View		
Amplitude	0.35 divs ±0.1 div.	
Position		Baseline to be set 3 divisions (±0.5 divisions) below graticule center. Internally adjustable approximately ±4 divisions from graticule center. See Section 4 for adjustment procedure.
Risetime		2 ns or less.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
DISPLAY (CONT)		
TRIG VIEW or External Clock View (cont)		
Time Coincidence with Channel Display		
TRIG VIEW	Within 3 ns.	
External Clock View	Within 5 ns.	
Readout		Displayed on crt, see detailed operating information.
TRIGGER		
SWITCHING THRESHOLD		
Voltage Range		
At Input BNC		
TTL (CMOS) Family	+1.28 V to -1.27 V.	
ECL Family	+256 mV to -254 mV.	
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		+12.8 V to -12.7 V.
ECL Family		+2.56 V to -2.54 V.
Resolution		
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		100 mV.
ECL Family		20 mV.
Accuracy, at Center Value of Hysteresis Window		
At Input BNC		
TTL (CMOS) Family	±5 mV ±2% of setting.	
ECL Family	±1 mV ±2% of setting.	
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		±50 mV ±2% of setting.
ECL Family		±10 mV ±2% of setting.
Hysteresis, Centered at Threshold, 50kHz (sine-wave)		
At Input BNC		
TTL (CMOS) Family	40 mV +20%, -50%.	

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
SWITCHING THRESHOLD (cont)		
Hysteresis, Centered at Threshold, 50kHz (sine-wave)		
ECL Family	8 mV +20% -50%.	
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		400 mV +20%, -50%
ECL Family		80 mV +20% -50%
Presets		
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		+1.4 V.
ECL Family		−1.30 V.
PROBE OFFSET Activated		0 V.
TIP (PROBE OFFSET) Input		
Maximum Voltage Range	+5.10 V to −5.10 V, dc only.	
Input Resistance		≥100 KΩ.
DVM Resolution		20 mV.
DVM Accuracy	±20 mV ±2% of reading.	
TRIGGER FILTER		
Range	Off, or adjustable from <15 ns to >300 ns.	The trigger filter cannot be activated if the EXT CLOCK is turned on, nor will it operate with any trigger function that contains an edge sensitive channel.
Match, Function A to Function B	Within 20%, at maximum setting.	
⚠ EXT CLOCK Input		
Maximum Voltage Range		+5V to −5V (DC + peak AC).
Threshold		Two EXT CLOCK INPUT modes are available, TTL or ECL; for selection of either mode see Figure 1-11.
TTL Level		
Logic Zero	≤0.8 V.	
Logic One	≥2 V.	

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
EXT CLOCK Input (cont)		
Maximum Voltage Range (cont)		
ECL Level		
Logic Zero	≤-1.5 V.	
Logic One	≥-1.1 V.	
Input Impedance		The EXT CLOCK INPUT may be connected directly to the clock source, or through a 1X probe (TTL only). The EXT CLOCK Input is not compatible with a 10X probe.
TTL Level		Approximately 10K ohm in parallel with approximately 55 pF, terminated to +5 V.
ECL Level		Approximately 50 ohms, terminated to -2 V.
Minimum Input Slew Rate		
TTL Level		None.
ECL Level		100 mV/ns.
Pulse Width		
TTL Level	20 ns minimum.	Either pulse transition selected.
ECL Level	5 ns minimum.	Leading pulse transition selected.
	10 ns minimum.	Trailing pulse transition selected.
Set-up Time	10 ns minimum.	Time that level sensitive channels must be valid before EXT CLOCK INPUT transition.
Hold Time	10 ns minimum.	Time that level sensitive channels must remain valid after EXT CLOCK INPUT transition.
Channel EDGE Sensitivity		
Set-up Time, Channel to Channel	5 ns minimum.	Time that level sensitive portion of trigger function must be true before EDGE sensitive channel transition.
Hold Time, Channel to Channel	5 ns minimum.	Time that level sensitive portion of trigger function must remain true after EDGE sensitive channel transition.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
Channel EDGE Sensitivity (cont)		
Set-up Time, EDGE Sensitive Channel	10 ns minimum.	Time that level of EDGE sensitive channel must be stable before transition.
Hold Time, EDGE Sensitive Channel	5 ns minimum.	Time that level of EDGE sensitive channel must remain stable after transition.
Mainframe Trigger Output		
Amplitude, 1 MHz square wave		300 mV ±50 mV p-p differential, into A13 and B13 of main interface connection on left side of plug-in.
Centering, 1 MHz square wave		Mean value of square wave within one division of graticule center.
Risetime, 10% to 60%		2 ns ±1 ns.
Falltime, 90% to 40%		2 ns ±1ns.
⚠ TRIGGER OUT Connector		
Output Voltage		
Logic Zero	≤0.2 V into 50 ohm load.	
Logic One	≥0.8 V into 50 ohm load.	
Output Impedance		Approximately 50 ohms.
Toggle Frequency	125 MHz maximum.	A Mode or B Mode, with displayed input signal of 60mV p-p in ECL or 300mV p-p in TTL Logic Family, centered at threshold.
Propagation Delay		
Channel Input to Trigger Output		25 ns or less.
Differential Propagation Delay from Channel Input to Trigger Output through any Trigger Function		5 ns or less.
A THEN B Mode		
Time Between A and B	5 ns minimum.	Minimum set-up time from event A to event B to insure that trigger output occurs with event B.
Time From B to A	5 ns minimum.	Minimum time after event B to next event A to insure proper arming.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
TRIGGER OUT Connector (cont)		
Event Duration		Minimum time to insure proper arming and triggering.
Event A	5 ns minimum.	
Event B	5 ns minimum.	
Front-Panel A THEN B Gate Output		The front-panel A THEN B Gate Output is active only if selected and in the A THEN B mode; see Figure 1-15 for selection.
Voltage		
Logic Zero		≤0.2 V into 50 ohm load.
Logic One		≥0.8 V into 50 ohm load.
Output Impedance		Approximately 50 ohms.
Timing		
Time from Event A Recognition to Rising Edge of Gate	25 ns or less.	
Mainframe A THEN B Gate Output		Active only in A THEN B Mode.
Amplitude, 1 MHz Square Wave		300 mV ±50 mV p-p differential, into A13 and B13 of main interface connector on right side of plug-in.
Centering, 1 MHz Square Wave		Mean value of square wave within one division of graticule center.
Risetime, 10% to 60%		2 ns ±1 ns.
Falltime, 90% to 40%		2 ns ±1 ns.
Timing		
Time from Event A Recognition to Rising Edge (50% point) of Gate Output		Approximately 15 ns.
Time from Event B Recognition to Falling Edge (50% point) of Gate Output		Approximately 15 ns.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
Mainframe A THEN B Gate Output (cont)		
Pulse Width		
Gate Output width, Measured at the 50% Points	Greater than the time between event A and event B by 5 ns ±2 ns.	
RESET Input		
Maximum Input Voltage		+5 V to -5 V (DC + peak AC).
Input Impedance		Approximately 50 ohms.
Levels		
Logic Zero	≤0.2 V.	
Logic One	≥0.8 V.	
Pulse Width	100 ns minimum.	
Timing, Post-RESET Inhibit Time to Next Trigger	10 ns minimum.	Time from falling edge of RESET to next recognizable event.
Response Time	RESET pulse must lead or be coincident with event recognition, to inhibit trigger output. Event recognition must lead the RESET pulse by 10 ns to guarantee trigger output.	
BATTERY BACK-UP		
Ni-Cad Battery (3.75 V)		Provides power to preserve front-panel control status a minimum of 200 hours while main power is off. Battery requires about 24 hours to fully charge from discharged condition.

TABLE 1-3
Environmental Characteristics

Characteristics	Information
Temperature (External Ambient Mainframe) Temperature	
Operating	0 to +40° C in 7403N/7603 without fan (fan kit is available). 0 to +50° C in other 7000-series mainframes.
Storage	−55° C to +75° C.
Altitude	
Operating	15,000 feet (4.6 Km).
Nonoperating	To 50,000 feet (15.2 Km).
EMC	Tested to MIL-T-28800C, MIL-STD-461A (excluding RE-01).
Vibration	
Operating and Nonoperating	Tested to MIL-T-28800C, SECT. 4.5.5.3.1 Type III, Class 5.
Shock	Tested to MIL-T-28800C, SECT. 4.5.5.4.1 Type III, Class 5.
Bench Handling	Tested to MIL-T-28800C, SECT. 4.5.5.4.4 Type III, Class 5.
Transportation	National Safe Transit Association, Preshipment Test Procedure.
Vibration and Bounce (packaged product)	NSTA, PROJECT 1 A-B-1.
Drop (packaged product)	NSTA, PROJECT 1 A-B-2.

TABLE 1-4
Physical Characteristics

Characteristics	Information
Net Weight	Approximately 6.2 lb, 2.8 Kg.
Dimensions	See dimensional drawing Figure 1-2.

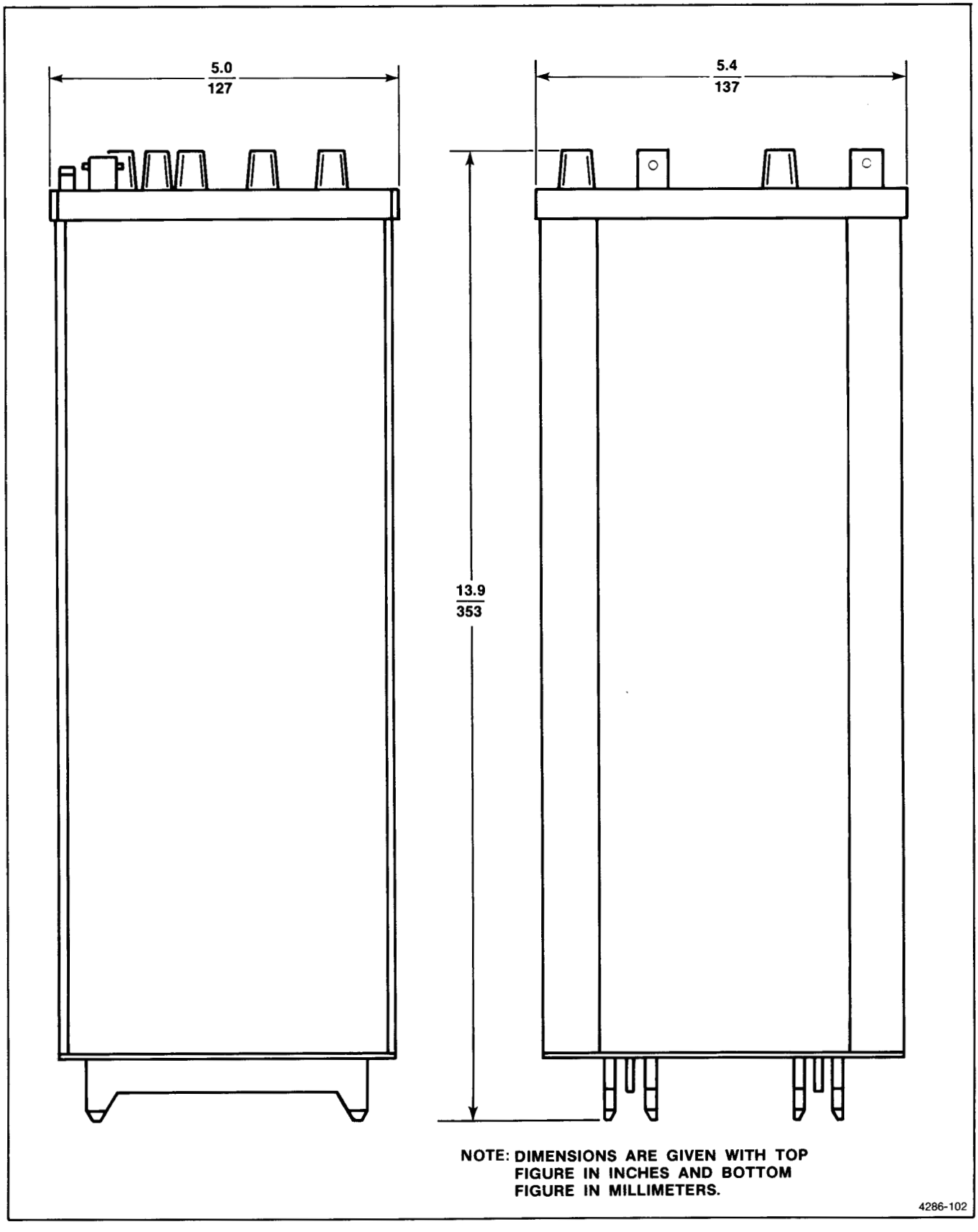


Figure 1-2. 7A42 dimensional drawing.

STANDARD ACCESSORIES

1 ea	Operators Manual
1 ea	Service Manual (Volume 1)
1 ea	Service Manual (Volume 2)
1 ea	SMB to BNC Cable

For part numbers, refer to the tabbed Accessories page at the rear of this manual.

OPTIONAL ACCESSORIES (not included)

The following accessories have been selected from our catalog specifically for your instrument. They are listed as a convenience to help you meet your measurement needs. For detailed information and prices, refer to a Tektronix Products Catalog or contact your local Tektronix Field Representatives.

PROBES

The P6131 10X passive probe (10 Megohm, 10.8 pF) has a 1.3 meter cable, a narrow barrel and variety of probe tips (hooks, IC grabbers, and ground leads) available.

The P6230 is an active 450 ohm variable bias/offset probe, which is an excellent ECL logic probe due to its low capacitances and minimal loading (because of the variable bias/offset feature). The 7A42's PROBE OFFSET feature is designed to work with the P6230. The P6131 accessories will also fit the P6230. (See ECL Probing Techniques in the Application section of the 7A42 Operators manual.)

Passive probes such as the P6131, require low-frequency compensation into the inputs of the 7A42, as with any vertical amplifier. The mainframe calibrator provides a signal suitable for making this adjustment. For optimum high-frequency performance, the probe high-frequency compensation should also be adjusted directly into the 7A42 inputs. See the probe manual for instructions to perform this adjustment.

OPERATING INSTRUCTIONS

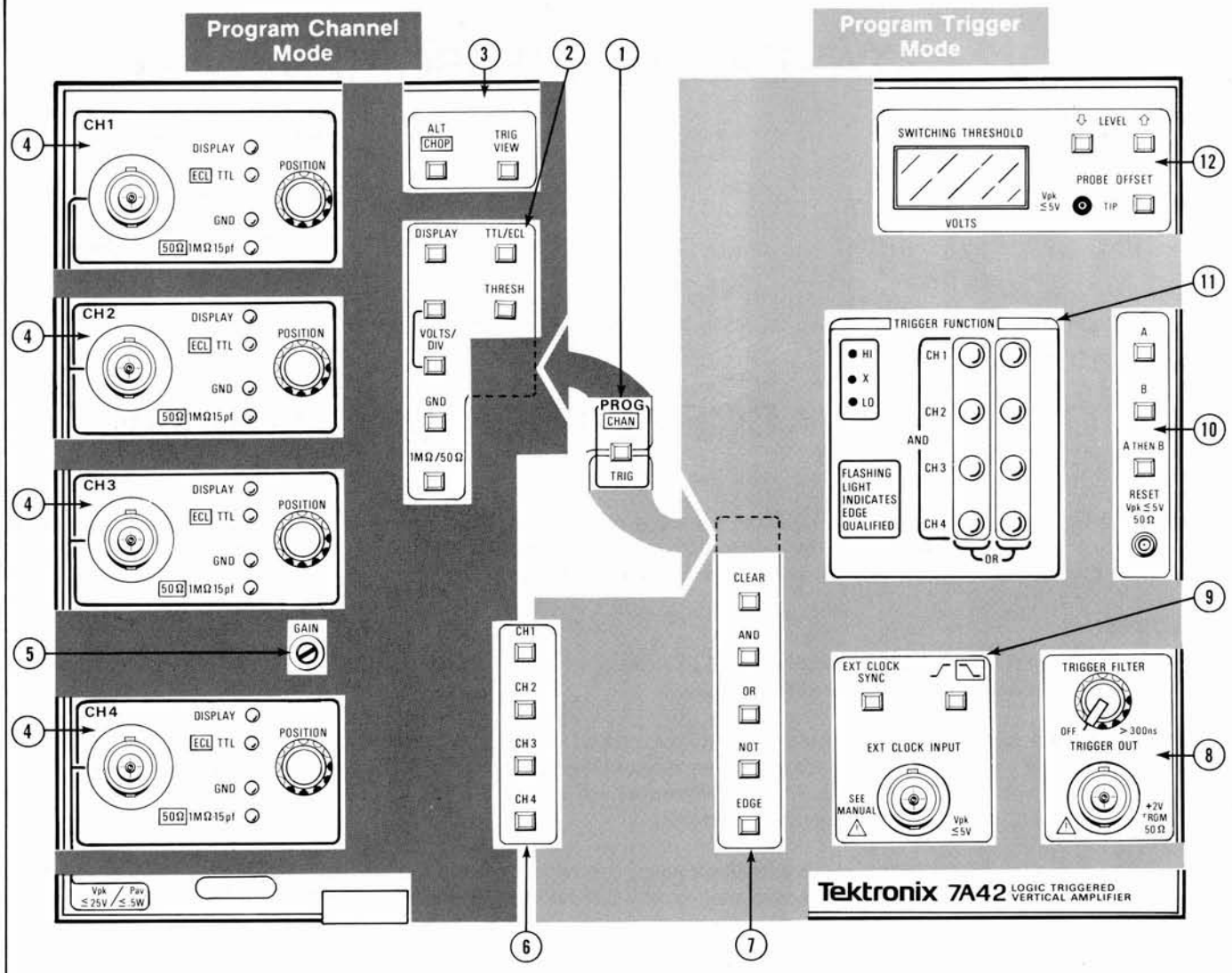
This section will familiarize you with the capabilities and operation of the 7A42. A thorough understanding of this information will remove later uncertainty when operating your 7A42.

OPERATION

For operation, your 7A42 Logic Triggered Vertical Amplifier must be properly installed in a Tektronix 7000-series mainframe. Installation is explained in the General Information section of this manual.

CONTROLS, CONNECTORS, AND INDICATORS

All controls, connectors, and indicators required for the normal operation of the 7A42 Logic Triggered Vertical Amplifer unit are located on the front panel. Figure 1-3 shows an exploded front panel and gives a brief functional description of each control, connector, and indicator.



1 **PROG CHAN or TRIG**—Pushbutton selects one of two modes; when light is on, those controls associated with programming the TRIGGER FUNCTION are operable (see **6**, **7** and **10**). When light is out, those controls associated with CH1, CH2, CH3, CH4 setup conditions are operable (see **6** and **2**).

2 **DISPLAY**—Pushbutton turns on or off the display of the incoming signal selected by controls listed under number **6**[1]. Nondisplayed channels may still contribute to the TRIGGER FUNCTION.

VOLTS/DIV—Two pushbutton switches increase or decrease vertical deflection factor of the channel selected by controls listed under number **6**[1].

GND—Pushbutton grounds the selected channel amplifier input and disconnects the incoming signal, of the channel selected by controls listed under number **6**[1].

1MΩ/50Ω—Pushbutton switch selects input impedance to be either one megohm or 50 ohms of the channel selected by controls listed under number **6**[1].

TTL/ECL—Pushbutton switch selects the deflection factor range and preset threshold to be compatible with either TTL or ECL logic families of the channel selected by controls listed under number **6**[1].

THRESH—Pushbutton switch activates the LEVEL pushbuttons and SWITCHING THRESHOLD VOLTS display, allowing operator to set the threshold voltage of the channel selected by controls listed under number **6**[1].

4286-103A

Figure 1-3. 7A42 controls, connectors, and indicators.

(3) **ALT/CHOP**—Pushbutton switch, determines whether the displayed channel(s) are displayed alternately, after each sweep of the time base, or are displayed simultaneously in a chopped mode.

TRIG VIEW—Pushbutton to display TRIGGER FUNCTION output signal or EXT CLOCK signal on crt.

(4) The following controls, connectors, and indicators are common to CH1, CH2, CH3, and CH4.

Input Connector—Bnc for signal connection.

POSITION—Vertically positions the incoming signal. Clockwise rotation moves displayed trace upward.

DISPLAY—When DISPLAY indicator light is on, channel is selected for display.

ECL/TTL—When indicator light is on the preset threshold voltage and range of deflection factors are compatible with TTL logic levels; when off they are compatible with ECL Logic levels.

GND—When indicator light is on, the amplifier input is grounded and the input signal is electrically disconnected from the amplifier.

50Ω/1MΩ—When indicator light is on, the input impedance is one megohm, 15 picofarads; when off, input impedance is 50Ω.

(5) **GAIN**—Screwdriver control adjusts display gain of channels CH1, CH2, CH3, and CH4.

(6) **CH1, CH2, CH3, and CH4**—Operate in either the PROG CHAN or the PROG TRIG modes. In the PROG CHAN mode the self-cancelling pushbutton switches determine which channel is affected by the controls listed under number **2**[1]. In the PROG TRIG mode the CH1 through CH4 pushbutton switches determine which channel is programmed into the TRIGGER FUNCTION, as selected by the controls listed under number **10**[2].

(7) **CLEAR**—Pushbutton switch clears the programmed TRIGGER FUNCTION selected by the controls listed under **10**[2].

AND, OR, NOT—Pushbutton switches used with controls listed under number **6** to program the TRIGGER FUNCTION selected by the controls listed under **10**[2].

EDGE—Pushbutton selects edge sensitivity for the channel being programmed into the TRIGGER FUNCTION[2].

(8) **TRIGGER FILTER**—*Variable control sets* minimum duration of TRIGGER FUNCTION output before it is sent to the time base or TRIGGER OUTput connector.

TRIGGER OUT—Provides a front-panel output of the trigger signal.

(9) **EXT CLOCK INPUT**—Provides external clock input for synchronizing triggers to an external clock signal source (EXT CLOCK SYNC light must be on).

EXT CLOCK SYNC—Pushbutton switch allows an external clock to qualify the TRIGGER FUNCTION.

 —*Pushbutton switch selects positive going* or negative going edge of the external clock signal which qualifies TRIGGER FUNCTION.

(10) **A, B, A THEN B**—Two independent TRIGGER FUNCTION programs are available (A and B). The A THEN B is a nested combination where A must occur to arm triggering before B is allowed to produce a trigger output.

RESET—External input to disable the TRIGGER FUNCTION output and disarm the A THEN B nested triggering; no arming or triggering can occur while a high level is applied.

(11) **TRIGGER FUNCTION**—LED display indicates the Boolean function which will produce a TRIGGER FUNCTION output. Number **6**, **7**, and **10** controls are used to program TRIGGER FUNCTION lights[2].

(12) **SWITCHING THRESHOLD VOLTS**—LED display indicates threshold voltage of the channel selected by controls listed under number **6** or displays probe offset[3].

LEVEL—Two pushbutton switches set threshold voltage of channel selected by the controls listed under number **6**[3].

PROBE OFFSET—Measures offset voltage of probe connected to the channel selected by controls listed under number **6**[3].

[1]PROG CHAN/TRIG must be set to CHAN.
[2]PROG CHAN/TRIG must be set to TRIG.
[3]PROG CHAN/TRIG must be set to CHAN, and THRESH must be active.

4286-103B

Figure 1-3 (cont). 7A42 controls, connectors, and indicators.

DETAILED OPERATING INFORMATION

Detailed information concerning the controls and operation of the 7A42 is given in the following pages.

SELF-TEST

When power is applied to the 7A42 an internal self-test sequence is automatically performed. While the self-test sequence is in progress the mainframe crt readout shows 7A42 TEST BUSY, see Figure 1-4. When the self-test sequence is finished, the message 7A42 TEST COMPLETE appears momentarily on the mainframe oscilloscope crt, as shown in Figure 1-5. During the self-test sequence some of the front-panel pushbuttons and all of the indicators are illuminated.

The SWITCHING THESHOLD VOLTS indicator will display 8.8.8.8. during the first part of the self-test sequence to verify that all segments operate. If there are no self test failures, the Firmware Version number will then be displayed for a few seconds before the self test is completed.

Self-test failures are indicated by three different methods: 1. on the mainframe crt, 2. on the 7A42 SWITCHING THRESHOLD display, and 3. on the TRIGGER FUNCTION indicators. Figure 1-6 illustrates a typical self-test failure, indicated by the three display methods. Displaying the self-test failure messages in three different ways increases the chance that the failure message will be displayed, even if the failure affects the operation of two of the three display methods.

The TRIGGER FUNCTION display indicates a self-test failure with the color red and self-test passed with the color green. If a failure occurs, the self-test sequence will stop.

The SWITCHING THRESHOLD VOLTS indicator and mainframe crt readout display indicate a self-test failure with a numeric code. All of the self-test code numbers are listed in Table 1-5, along with the nature of the failure and an explanation of the severity of the failure. The severity information is helpful in determining if the 7A42 can still be used for the intended purpose or whether repair is necessary. To continue the self-test sequence, press any of the 7A42 front-panel pushbuttons.

NOTE

Before the 7A42 Self Test feature can verify that the 7A42 readout circuitry is operating properly, mainframe crt readout system must be set to the "Freerun" (non-Gated) mode.

FRONT-PANEL INITIALIZATION

While getting acquainted with the 7A42, it might be desirable to begin operation with the front-panel controls set to a known state (initialized). The front panel will initialize to the control settings listed in Table 1-6. To initialize the 7A42 front-panel controls to a known state, perform the procedure of Figure 1-7.

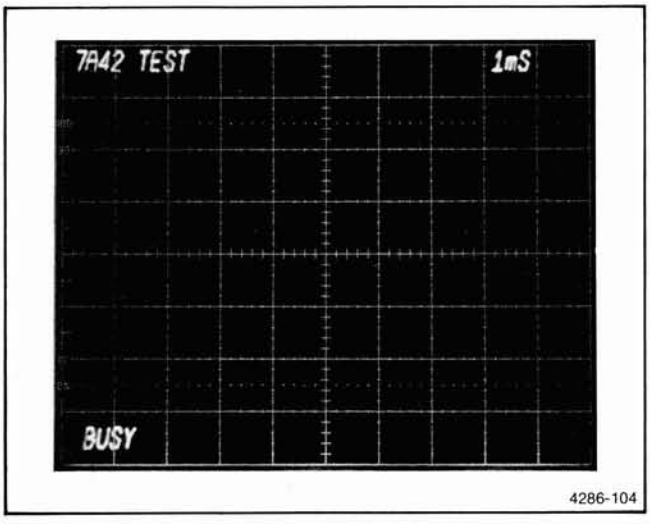


Figure 1-4. Self-test in progress.

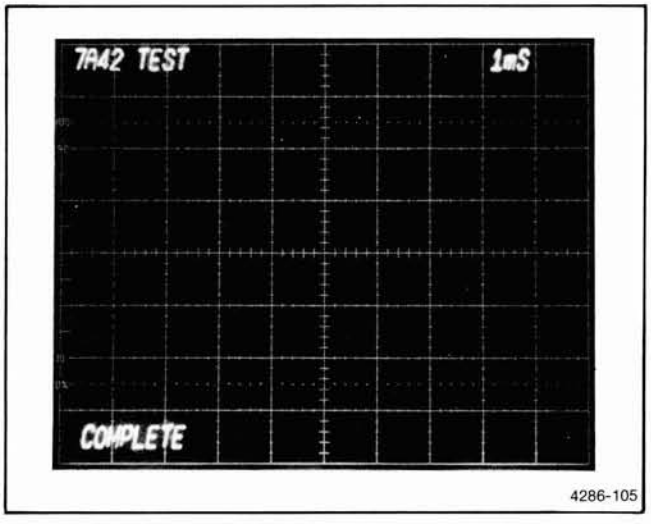
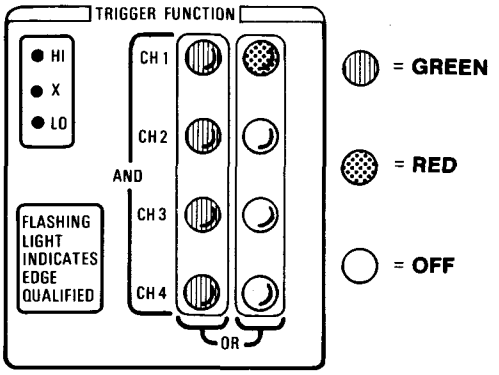
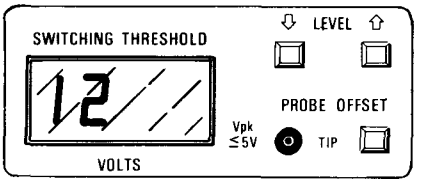
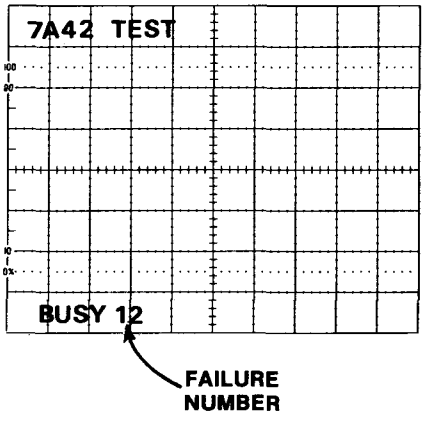


Figure 1-5. Self-test finished.

DISPLAY MEDIA	TYPICAL MEDIA
TRIGGER FUNCTION LEDS **GREEN = TEST PASSED** **RED = TEST FAILED**	
SWITCHING THRESHOLD VOLTAGE MONITOR (Numeric Display)	
CRT READOUT (Numeric Display) **NOTE: During some self tests, the crt readout is unstable; this condition is normal.**	

4286-106

Figure 1-6. Typical self-test failure display.

BATTERY BACKUP

The 7A42 battery backup feature restores the 7A42 front-panel control settings to the same settings that were present when the power was turned off.

The battery-backup feature can be defeated if so desired. If the battery-backup feature has been disabled, the 7A42 front-panel control settings will return, at power up, to the settings listed in Table 1-6. To disable the battery back up feature disconnect J747 from the MPU Board, see Figure 1-8.

OPERATOR MESSAGES

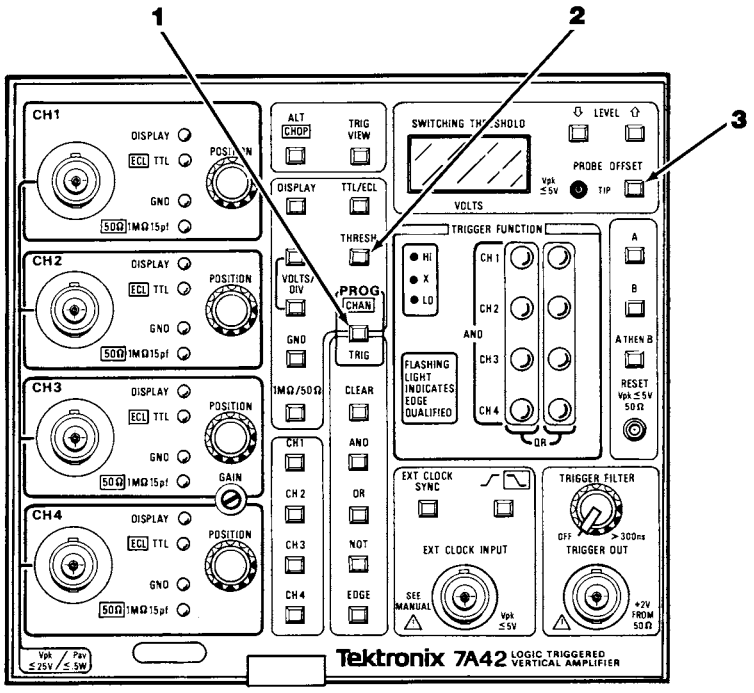
Operator Messages occur under several operating conditions and are accompanied by an audible beep. When they occur, the mainframe readout will display a mnemonic at the top of the crt and a number code at the bottom. The mnemonic is an abbreviated explanation of the operating condition which caused the message to be displayed. The code number references the message to Table 1-7 which gives a more complete explanation of the operating condition.

TABLE 1-5
7A42 Self-Test Failure Messages

TRIGGER FUNCTION (LED display)		SWITCHING THRESHOLD VOLTS and crt readout display		Severity of failure; functional usability of instrument
Indication	**Test**	**Indication**	**Test**	
CH1, first column	ROM	01 to 04	ROM	Possible loss of front-panel control; repair before use.
CH2, first column.	RAM	05 to 06	RAM	
CH3, first column.	Microprocessor control logic.	07 to 09	Microprocessor control logic.	
CH4, first column.	PROBE OFFSET	10	PROBE OFFSET	Avoid use of probe offset feature. 7A42 otherwise fully functional. Repair when convenient.
CH1, second column.	Crt display and readout	11	Crt trace display.	Channels 1 through 4 may not be displayable. Repair before use.
		12,13	Crt readout.	Crt readout may not be functioning. Cause could be lack of mainframe readout. Repair when convenient.
CH2, second column.	Trigger	14	Trigger control.	Some or all trigger functions may not be operational. Repair before use.
		15	Trigger logic.	Some channels may not trigger properly. Repair before use.
		23	Boolean logic.	Some trigger functions may not be operational. Repair before use.
		26	A THEN B	Avoid use of A THEN B mode. Repair when convenient.
CH3, second column.	Edge detectors.	34	Edge detectors.	Avoid use of Edge-qualified triggering mode and external clock. Repair when convenient.
CH4, second column.	EXT CLOCK	70	EXT CLOCK	Avoid use of external clock. Repair when convenient.

NOTE

For more detailed information, see Table 3-6, extended test failure messages, in this manual.



a. Set the PROG pushbutton **1** to the CHAN mode (pushbutton light out).

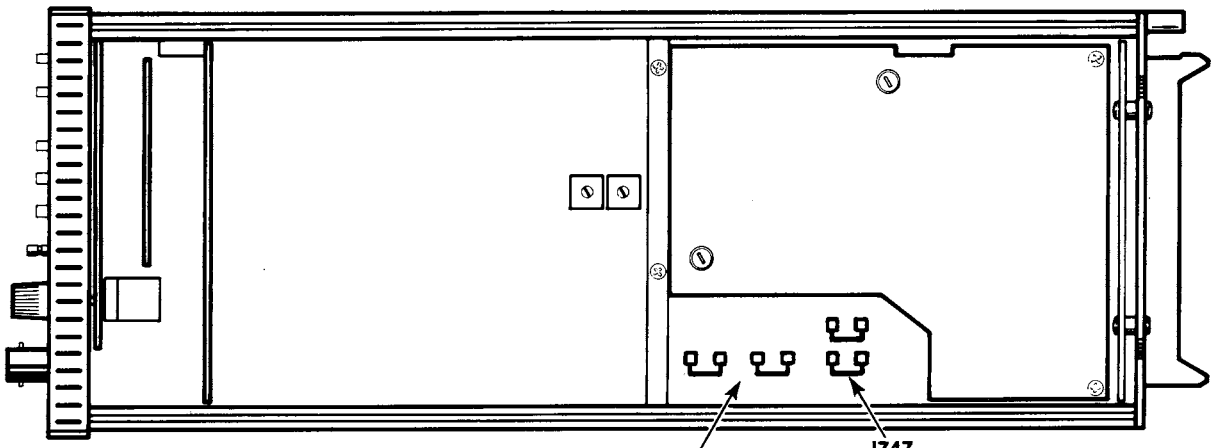
b. Press the THRESH pushbutton **2** so that the pushbutton light is on (Threshold Mode).

c. Press the PROBE OFFSET pushbutton **3** until it illuminates red (Acquire Mode).

d. Turn the oscilloscope mainframe Power off and then on again.

4286-113

Figure 1-7. Initialization of the 7A42 front-panel controls.



4286-406

Figure 1-8. Location of J747 Battery Enable link plug.

NOTE

The audible beep can be turned off, by installing a link plug on P730. See Figure 3-8 in the Maintenance section of this manual for the location of P730.

SIGNAL CONNECTIONS

Generally, probes offer the most convenient means of connecting input signals to the instrument. Probes are shielded to prevent electromagnetic interference. The

TABLE 1-6
7A42 Front-Panel Control Settings When Initialized

Control	Control Setting
PROG CHAN/TRIG	Program Channel (light off)
Programmable Channel	CH1 only
DISPLAY	CH1 only
VOLTS/DIV (CH1 through CH4)	Preset to 0.5 V/Div at bnc input
TTL/ECL (CH1 through CH4)	TTL
GND (CH1 through CH4)	Ungrounded
1MΩ/50Ω (CH1 through CH4)	1MΩ
ALT/CHOP	ALT
TRIG VIEW	Off
SWITCHING THRESHOLD voltage (CH1 though CH4)	Preset TTL (+1.4V); display off
THRESH	Off
PROBE OFFSET	Off
A TRIGGER FUNCTION	CH1 (HI)
B TRIGGER FUNCTION	Cleared
TRIGGER MODE TRIGGER FUNCTION A THEN B	 A Off
EXT CLK SYNC	Off
External Clock Slope	Off

NOTE

Controls not listed above are not preset.

TABLE 1-7
7A42 Operator Message Summary

Code	Mnemonic	Description and Corrective Action
1	OVERLOAD	A channel input is overloaded. Remove the overvoltage and unground the channels to continue operation.
2	OFFSET ACQ	A key was pressed while Probe Offset acquisition was in progress. Push PROBE OFFSET once to lock in acquired value, or twice to turn PROBE OFFSET off, before continuing operation.

TABLE 1-7 (CONT)
7A42 Operator Message Summary

Code	Mnemonic	Description and Corrective Action
3	PUSH PROG	Key(s) pressed is/are active only in PROG CHAN mode. To use key, first press PROG CHAN.
4	PUSH PROG	Key(s) pressed is/are active only in PROG TRIG mode. To use key, first press PROG TRIG.
5	AND/OR REQ	While programming a trigger function, a CH1, CH2, CH3, CH4, NOT, or EDGE was pressed when an AND or an OR key was expected.
6	CH KEY REQ	While programming a trigger function, two Boolean operator keys (AND or OR) were pressed without pressing a channel key (CH1, CH2, CH3, or CH4) in between. Channel keys and Boolean operator keys should be pressed alternately, e.g., CH1 AND NOT CH2 OR CH3 EDGE.
7	OR IS FULL	The OR key was pressed again. Only one TRIGGER FUNCTION OR is allowed.
8	EXTCLK ON	The EDGE key was pressed while in the EXT CLOCK SYNC mode. The selection of an EDGE sensitive channel and the EXT CLOCK SYNC mode are mutually exclusive. If EDGE sensitivity is desired, first turn off the EXT CLOCK SYNC mode.
9	EXTCLK REQ	The EXT CLOCK slope key was pressed when the EXT CLOCK SYNC button was turned off. The EXT CLOCK SYNC slope key is operational only when the EXT CLOCK SYNC button is turned on.
10	EDGE IS ON	The EXT CLOCK SYNC key was pressed when one of the trigger functions (either A, B, or both) already have an EDGE sensitive channel. Channel EDGE sensitivity and EXT CLOCK are mutually exclusive. If EXT CLOCK SYNC operation is desired, first CLEAR the channel EDGE sensitive trigger function.
11	THRESH REQ	Either a LEVEL key or the PROBE OFFSET key was pressed without pressing the THRESH key first. The THRESH key must be lit to change a threshold level or acquire a probe offset.

TABLE 1-7 (CONT)
7A42 Operator Message Summary

Code	Mnemonic	Description and Corrective Action
12	NO FUNC A	The A THEN B key was pressed without having programmed function A; or while in A THEN B mode function A was CLEARed. Both trigger functions (A and B) must be programmed for proper A THEN B operation. Program function A; then proceed.
13	NO FUNC B	The A THEN B button was pressed without having programmed function B; or while in A THEN B mode function B was CLEARed. Both trigger functions (A and B) must be programmed for proper A THEN B operation. Program function B; then continue.

WARNING BEEPS: Although no messages are displayed, short warning beeps are issued to indicate "out of range." A beep will sound when the VOLTS/DIV keys are pushed beyond the available selections or when the variable threshold level reaches its limits.

NOTE

The audible beep can be turned off, by installing a link plug on P730. See Figure 3-8 in the Maintenance section of this manual for location of P730.

10X probe offers a high input impedance to minimize circuit loading when measurements are made; signal amplitude is attenuated by a factor of 10 by the probe, so the scale-factor readout is switched to indicate the correct scale factor.

The limited TTL/ECL VOLTS/DIV ranges require that attenuation be used to obtain useful signal levels at the 7A42 channel inputs. Ten times probes are recommended on the channel inputs to attenuate TTL and ECL signals; otherwise 10X attenuators should be used. When 10X probes are used the VOLTS/DIV and SWITCHING THRESHOLD are automatically compensated to reflect the characteristics at the probe tip.

RECOMMENDED PROBES

The Tektronix P6131 and P6230 probes are recommended for use with the 7A42. The Tektronix P6131 is a 10X passive probe with 10 megohm at 10.8 picofarads. A variety of probe tips (hooks, IC grabber and ground leads) are available with this probe.

The Tektronix P6230 is an active 450 ohm bias/offset probe which is especially useful with ECL logic circuits due to its minimal circuit loading characteristics. For information on how to use the P6230 probe, refer to the Application section in the 7A42 Operators manual.

Probe Compensation

Maladjustment of probe compensation is one source of measurement error. Most 10X passive high impedance probes are equipped with a compensation adjustment. To ensure optimum measurement accuracy, always compensate the oscilloscope probe before making measurements. Refer to the probe instruction manual for probe adjustment procedure.

For optimum 7A42/P6131 performance the P6131 should be high-frequency compensated while connected to the 7A42; see the P6131 probe manual for high-frequency compensation adjustment procedure.

COAXIAL CABLES

Although the 7A42 input channel VOLT/DIV ranges are intended to be used with 10X probes, coaxial cables may be used for signal connections. When coaxial cables are used a 10X attenuator must be used to reduce TTL/ECL signals to usable levels. When 10X attenuators are used the VOLTS/DIV and SWITCHING THRESHOLD readings are not automatically compensated and will indicate values a factor of 10 lower than actual.

Cables also may be used to connect signals to the input connectors, but they may have considerable effect on the accuracy of the displayed waveform. To maintain the original frequency characteristics of an applied signal, use only low-loss, 50 ohm, high-quality coaxial cable. Cables should be terminated into 50 ohms. The 7A42 has an internal 50 ohm termination for each input channel which can be selected from the front-panel.

CRT READOUT

Figures 1-9 and 1-10 show the 7A42 scale factor readout location. Figure 1-10 was taken with X10 probes attached to the channel inputs. Figure 1-9 was taken without probes attached to the channel inputs and without changing the channel VOLTS/DIV settings from those of Figure 1-10.

NOTE

Improper crt readout operation may be caused by the 7A42-7854 mode being selected when the 7A42 is operated in other 7000-series mainframes. See Figure 3-7 in the Maintenance section of this manual to determine if the 7A42-7854 mode is selected.

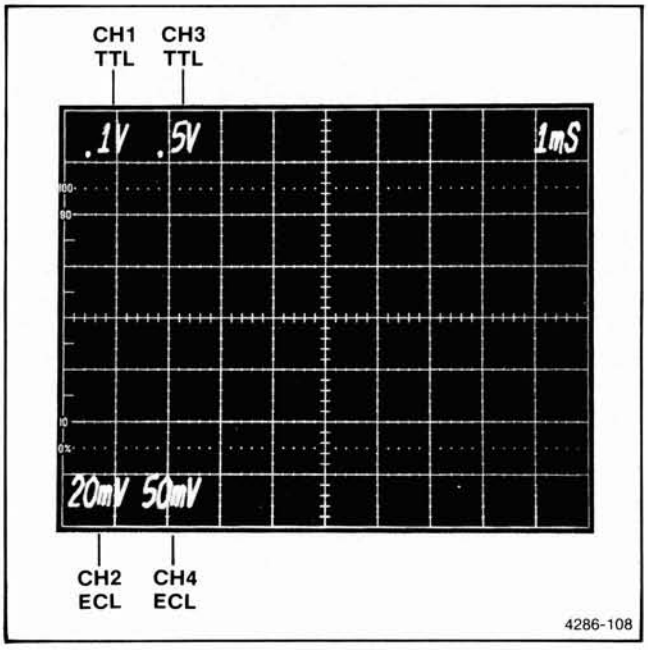


Figure 1-9. Channel readout display.

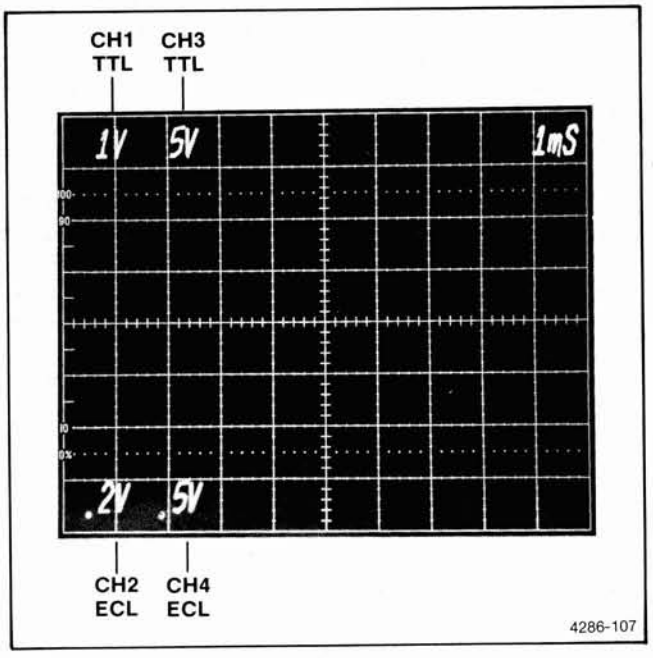


Figure 1-10. Channel readout display with 10X probes attached to inputs of CH1, CH2, CH3, and CH4.

POSITION

A POSITION control is provided for each of the four channels. The control vertically positions the displayed trace on the host mainframe crt (clockwise rotation moves the trace upward).

GAIN

This screwdriver control adjusts the 7A42 display output (of all four channels) to match the vertical gain tolerance of any Tektronix 7000-series mainframe.

STATUS INDICATORS (CH1, CH2, CH3, CH4)

Each channel has four status indicators (DISPLAY, ECL/TTL, GND and 50Ω/1MΩ). These indicators show the status of each individual channel. A description of each indicator is given below.

DISPLAY

When the DISPLAY indicator is lit, the associated channel is displayed on the mainframe crt. If the indicator is extinguished, any signal applied to the channel input will still be routed to the TRIGGER FUNCTION circuitry, providing the GND indicator is not lit.

ECL/TTL

When the ECL/TTL indicator is lit, the channel threshold voltage range and deflection factors match the voltage levels and signal amplitudes of the TTL logic family. When the indicator is extinguished the threshold voltage range and deflection factors are in accord with the ECL logic family.

GND

When the GND indicator is lit, the input to the selected channel amplifier is grounded and the signal path from the front-panel bnc connector to the amplifier is open. An external signal applied to this channel is not terminated (it is open). Grounded channel traces are still displayed to enable the ground reference position to be established.

50Ω/1MΩ

When the 50Ω/1MΩ indicator is lit, the input impedance of the associated channel is one megohm. When the indicator is extinguished the input impedance is 50 ohms.

ALT/CHOP

The ALT/CHOP pushbutton selects either alternate or chopped as the display mode (for all channels). When the ALT/CHOP indicator is lit, the channels selected for display are alternately displayed on the mainframe oscilloscope crt after each sweep of the time base. When the ALT/CHOP indicator is extinguished, the display is electronically switched between channels at about a one-megahertz rate. In general, the ALT mode provides the best display at sweep rates of 100

microseconds/division and faster while the CHOP mode provides the best display at sweep rates slower than about 200 microseconds/division or whenever multiple single-shot signals are to be photographed.

TRIGGER FUNCTION

The two-color TRIGGER FUNCTION indicators display the Boolean trigger function. The color red indicates a HI (logic 1, or higher than threshold voltage) condition. Green indicates LO (logic Ø, or lower than threshold voltage) condition. An indicator that is not lit represents the X (don't care) condition. A red flashing or green flashing indicator signifies that the channel is edge sensitive (rising, red; or falling, green) as opposed to being level sensitive.

The TRIGGER FUNCTION indicators are arranged in two columns of four each. Each column represents a logical AND function, (a Boolean product of the four input channels). After the AND functions are performed, the columns are ORed together to form the complete Boolean TRIGGER FUNCTION. Thus each TRIGGER FUNCTION is equivalent to two four-bit word recognizers ORed together.

There is one exception to this convention. While an extinguished indicator represents the "don't care" condition, an entire column that is not lit is considered to be inactive. If an unlit column were interpreted as a don't care, that column ORed with any other column would always be true.

A TRIGGER FUNCTION AND B TRIGGER FUNCTION

There are two separate TRIGGER FUNCTIONS available, A and B. They are identical; either may be used. One pushbutton will always be lit to indicate which function is displayed by the TRIGGER FUNCTION indicators and therefore, the function that will produce the trigger output. The other function is stored in memory and may be called up by pressing that pushbutton. The programming or clearing of the function displayed will not affect the other function.

A THEN B NESTED TRIGGERING

One level of nested triggering is available when this mode is used. The trigger output to the mainframe time base occurs only after the triggering is first armed by the occurrence of function A. The trigger output then takes place with the next occurrence of function B. After this cycle, the 7A42 will begin to look for another occurrence of function A, to begin the next nested trigger cycle.

TRIG VIEW

The TRIG VIEW trace provides a visible replica of the trigger output signal as it is processed by the 7A42 according to the programmed TRIGGER FUNCTION. This trigger signal is also sent to the time base. When the EXT CLOCK SYNC pushbutton switch is lit, the TRIG VIEW trace displays the external clock input signal.

The TRIG VIEW trace is normally located near the bottom of the crt display. There is an internal provision for repositioning the trace; refer to the Performance Check and Adjustment section of this manual, for a procedure to reposition the TRIG VIEW trace. If all of the channel displays are turned off the TRIG VIEW trace will be on and cannot be turned off.

TRIGGER FILTER

The TRIGGER FILTER control provides a selectable amount of delay between the time that the TRIGGER FUNCTION is recognized as true, and the time that the Trigger Output is sent to the time base to trigger the sweep. Thus the TRIGGER FILTER will inhibit trigger events that are shorter in duration than those for which the control is set. A longer trigger event will pass through the TRIGGER FILTER and can cause a triggered sweep as well as a signal at the front-panel TRIG OUT connector. The TRIGGER FILTER control can be used only with level-sensitive trigger functions (it is inactive with any TRIGGER FUNCTION that contains an edge-sensitive channel). The TRIGGER FILTER operates independently on TRIGGER FUNCTION A and TRIGGER FUNCTION B. In the A THEN B mode, the TRIGGER FILTER may be inactive on function A because of an edge sensitive channel, while at the same time be active on function B. The TRIGGER FILTER is not active when in the EXT CLOCK SYNC mode or when the control is in the counterclockwise detent (OFF) position.

EXT CLOCK SYNC

The EXT CLK SYNC pushbutton allows the 7A42 to be used in a synchronous mode of operation. The trigger output (in either A, B, or A THEN B mode) will occur only on the selected edge of an external clock signal, providing the TRIGGER FUNCTION is also true at that time. If TRIG VIEW is selected, a replica of the external clock input signal having a fixed amplitude and position will be displayed on the TRIG VIEW trace.

SLOPE SELECT

Either the rising or falling edge of an external clock signal can be used to qualify the TRIGGER FUNCTION. When the Slope Select pushbutton is lit the TRIGGER FUNCTION is qualified on the rising transition of the external clock signal.

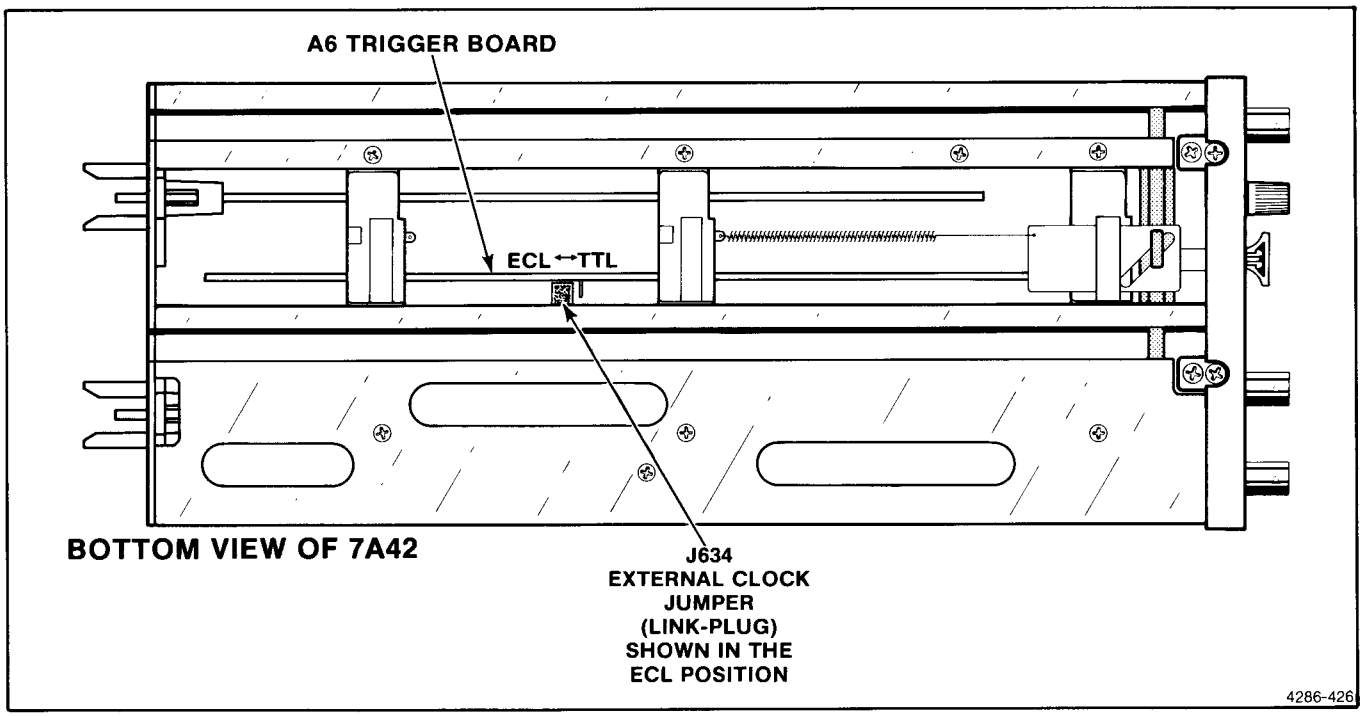


Figure 1-11. Location of J634, External Clock Jumper, on A6 Trigger Board.

EXT CLOCK INPUT

The EXT CLOCK INPUT is directly compatible with either TTL or ECL logic families. The instrument is shipped from the factory in the TTL mode.

For selection of the ECL or TTL mode see Figure 1-11. The EXT CLOCK INPUT can be used with a 1X probe in TTL mode, or can be directly connected to the logic circuit in either TTL or ECL mode; 10X probes should not be used with this input.

RESET INPUT

The RESET INPUT allows the operator to apply a signal to inhibit the trigger output. Applying a positive 0.8 volt level to the RESET input will prevent the programmed TRIGGER FUNCTION from being recognized as true. The result is that no trigger output signal will occur until the reset voltage is removed.

If the A THEN B nested-trigger mode is selected, TRIGGER FUNCTION A has occurred, and TRIGGER FUNCTION B has not occurred; the RESET signal will reset function A (the armed condition) as well as inhibit function B. Therefore, the RESET input can be used to enhance the A THEN B nested trigger operation by providing an "A THEN B unless RESET" feature.

TRIGGER OUT

The TRIGGER OUT bnc connector is a trigger output signal source. This signal can be used to synchronize other equipment with the 7A42 TRIGGER FUNCTION. The output of the TRIGGER FUNCTION is determined by the setting of the A, B, or A THEN B pushbuttons, the programming of the A and B functions, and the channel input signals. Timing diagrams for a typical set of conditions are shown in Figures 1-12 and 1-13.

Two modes of operation can be selected for the TRIGGER Out connector; Normal, and A THEN B Gate. In Normal Mode, the A THEN B Trigger Out is a pulse, regardless of the duration of Trigger Function B. A typical timing diagram depicting the Normal and A THEN B Gate modes, is shown in Figure 1-14. For selection of either mode see Figure 1-15. The TRIGGER OUT signal levels are compatible with the RESET input levels.

PROG CHAN/TRIG

The PROG CHAN/TRIG pushbutton selects one of two modes, PROG CHAN (program channel) or PROG TRIG (program trigger). In the PROG CHAN mode the DISPLAY, VOLTS/DIV, GND, 1MΩ/50Ω, TTL/ECL, and THRESH pushbuttons are activated. These controls are used with the CH1, CH2, CH3 and CH4 pushbuttons to individually set the channel status. In the PROG TRIG mode CLEAR, AND, OR, NOT, and EDGE pushbutton controls are activated and are used with the CH1, CH2, CH3, and CH4 pushbutton controls to program a Boolean equation into the A TRIGGER FUNCTION or B TRIGGER FUNCTION. The following text discusses first the PROG CHAN controls and then the PROG TRIG controls.

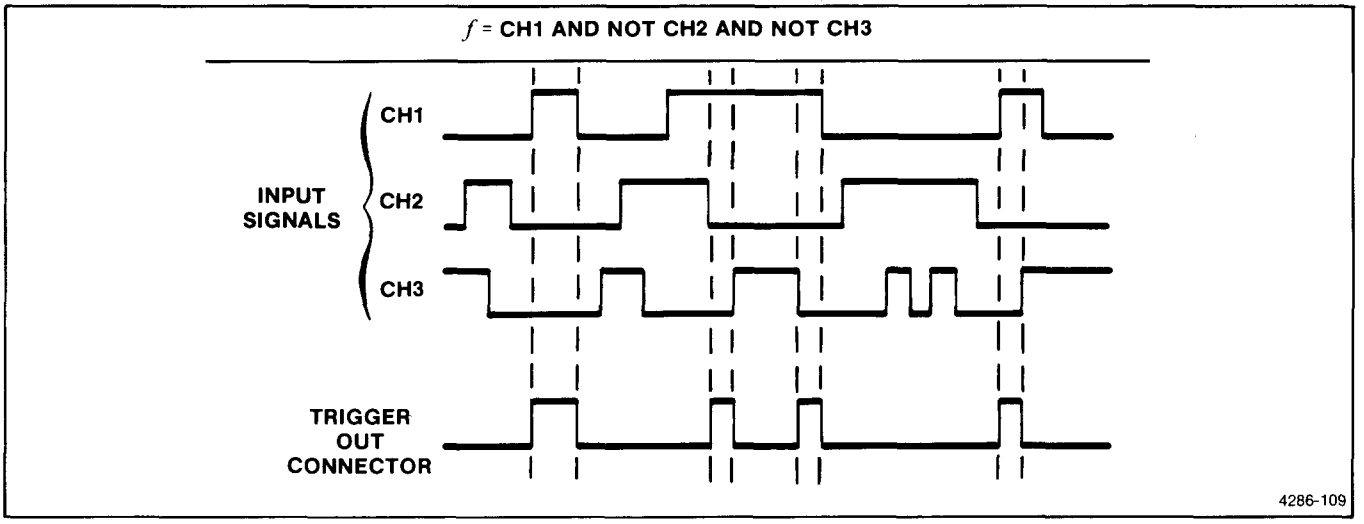


Figure 1-12. Timing diagram showing the relationship of the TRIGGER OUT waveform to the input signals.

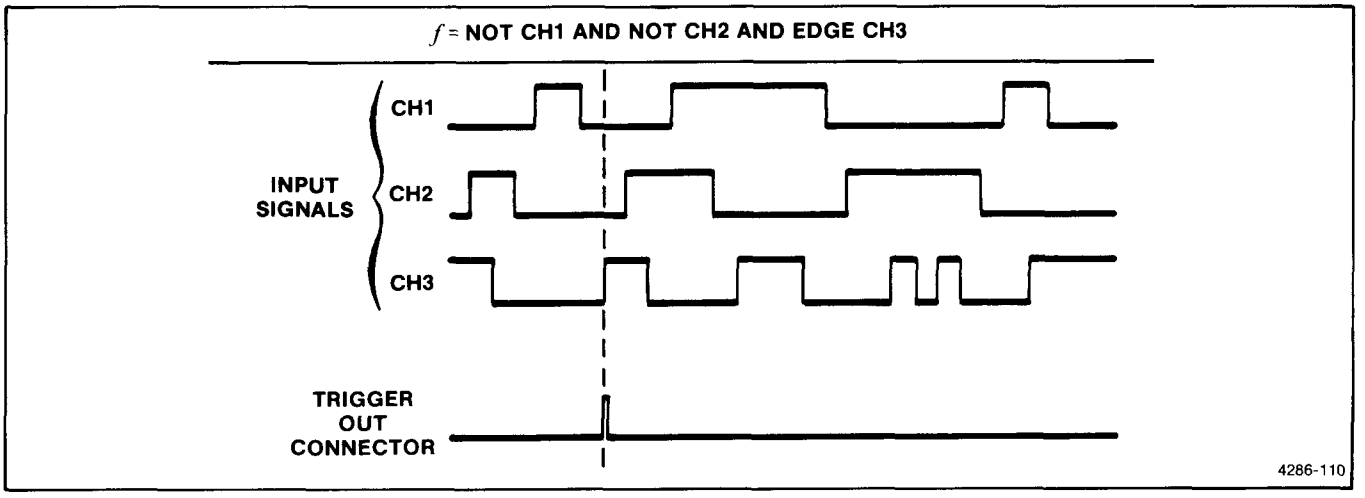


Figure 1-13. Timing diagram depicting the TRIGGER OUT waveform, as a result of the TRIGGER FUNCTION reacting to the input signals.

PROGRAM CHANNEL MODE

The TTL/ECL, VOLTS/DIV, GND, 1MΩ/50Ω, and DISPLAY, controls are active in the PROG CHAN mode. These controls are used with the CH1, CH2, CH3, and CH4 pushbuttons to set the status of each channel.

CH1, CH2, CH3, CH4. In the PROG CHAN mode the CH1, CH2, CH3, and CH4 pushbuttons are used to select and indicate the channel which will respond to the TTL/ECL, VOLTS/DIV, GND, 1MΩ/50Ω, DISPLAY and THRESH pushbutton controls.

DISPLAY. The DISPLAY pushbutton turns the selected channel display on or off. In the off position the trace is removed from the crt display. However, the signal applied to that channel is still routed to the TRIGGER FUNCTION circuitry, providing the channel GND indicator is not lit.

TTL/ECL. The TTL/ECL pushbutton offers a threshold range and selection of display sensitivities appropriate for either TTL or ECL logic families.

VOLTS/DIV. The VOLTS/DIV pushbuttons set the scale factor of the selected channel. The scale factor is displayed on the mainframe crt readout; refer to CRT Readout in this section. Three sensitivities are available in each logic family; see Table 2-4. To increase the sensitivity (display size) press the upper button.

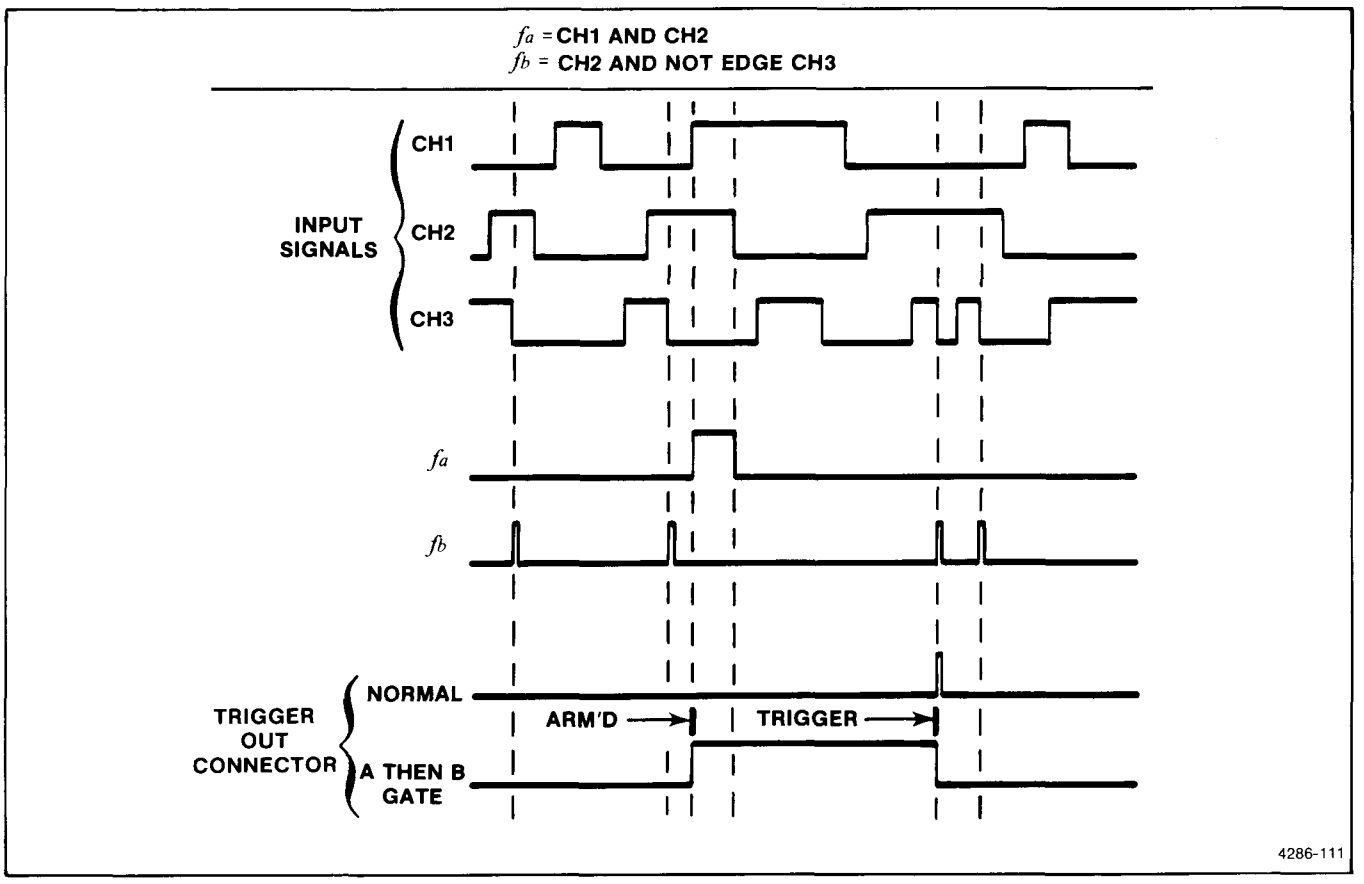


Figure 1-14. Example of A THEN B, level and EDGE sensitive TRIGGER FUNCTION, showing the Normal and A THEN B Gate waveform alternatives.

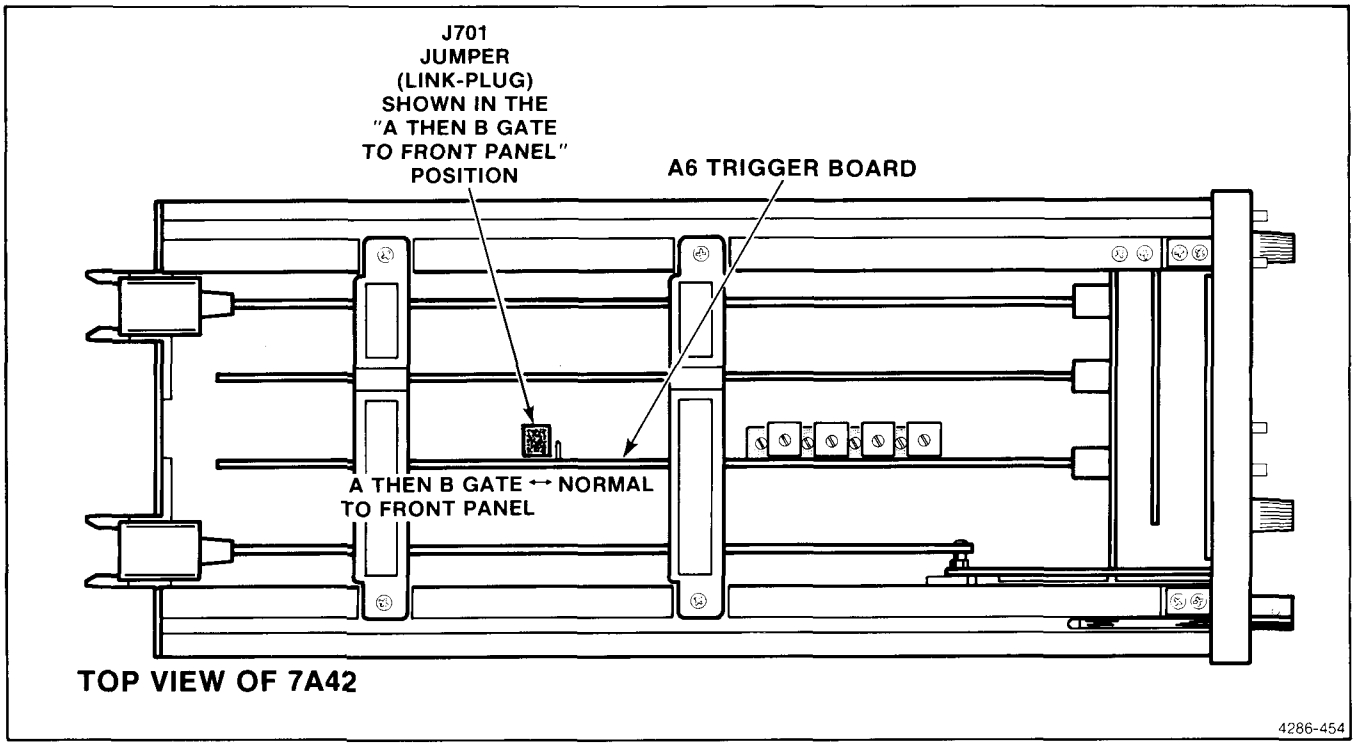


Figure 1-15. Location of J701, on A6 Trigger Board.

TABLE 1-8
Channel Volts/Division Ranges

Logic Family	At The BNC	Through a 10X Probe
TTL (CMOS)	.1, .2, .5 V/Div	1, 2, 5 V/Div
ECL	20, 50, 100 mV/Div	.2, .5, 1 V/Div

GND. The GND pushbutton connects the selected channel amplifier input to ground as a reference for trace positioning. However, the incoming signal is not grounded; it is disconnected from the amplifier input.

1MΩ/50Ω. The 1MΩ/50Ω pushbutton selects the input impedance of the selected channel. The available impedances are 1 megohm in parallel with about 15 pF, or 50 ohms.

THRESH. Each of the four input channels have two possible preset threshold voltages, +1.4 volts for the TTL mode and -1.30 volts for the ECL mode. In addition, these threshold voltages can be altered using the LEVEL⇧ or LEVEL⇩ pushbuttons. The SWITCHING THRESHOLD VOLTS display will indicate the threshold voltage present at each of the channel inputs. To turn the SWITCHING THRESHOLD VOLTS display on, press the THRESH pushbutton (the light should be on).

The SWITCHING THRESHOLD VOLTS display corresponds to the channel pushbutton that is lit (CH1, CH2, CH3, or CH4). While the button is lit, the actual threshold voltage for the channel is indicated in the seven-segment LED display. For each logic family there are internally preset thresholds that can be altered by pressing either the LEVEL⇧ or LEVEL⇩ button. A single push changes the threshold by one increment. When either LEVEL button is held down the rate accelerates. Each channel's threshold level is maintained when THRESH is pushed again to turn off the seven-segment display and button light. However, for a particular channel, the variable setting (if any) will be cancelled (reverts to the preset value) when the TTL/ECL selection is changed.

PROBE OFFSET. The PROBE OFFSET control provides a means of acquiring the offset voltage introduced into the signal path by the P6230 (500 ohm) active probe. In order to minimize circuit loading, it is desirable to set the probe offset/bias near the logic zero level or the termination voltage of the ECL circuit being probed. To acquire the PROBE OFFSET, THRESH must be selected and the channel (1 through 4) to which the P6230 is connected must be selected. When the PROBE OFFSET pushbutton is pressed it will light red. The SWITCHING THRESHOLD VOLTS display then becomes a DVM which reads the amount of probe offset. To measure and acquire the probe offset voltage, touch the probe tip to the front-panel jack labeled TIP, then set the offset adjustment on the probe case to the voltage desired. While still holding the probe tip to the TIP jack, push the PROBE OFFSET button once again to acquire this offset measurement into the 7A42. The probe offset button will now light green and the probe tip may now be removed. The offset measurement remains in the display. Altering the 7A42 trigger threshold (independent of the probe offset) may be done using the LEVEL buttons. Pushing the PROBE OFFSET button once more turns off the lit button and clears the acquired offset measurement. The 7A42 PROBE OFFSET feature is appropriate for use only with the P6230 probe.

The acquired PROBE OFFSET voltage, whether zero or otherwise, is maintained when the THRESH button is turned off or while threshold information of another channel is being displayed. That value is also maintained if the logic family is changed, adding to the preset threshold levels as expected. If a channel has a non-zero offset and THRESH (with that channel selected) is turned on, the PROBE OFFSET button will be lit green (a reminder of the offset status).

LEVEL. The LEVEL⇧ and LEVEL⇩ controls are used to set the threshold voltage of each channel to a value other than the preset threshold voltage. These controls are active only in the PROG CHAN mode and when the THRESH pushbutton switch is lit.

When either the LEVEL⇧ or LEVEL⇩ button is held, the variable threshold changes at an accelerating rate, pausing momentarily at the preset value.

The SWITCHING THRESHOLD VOLTS display indicates the preset threshold voltage or the variable threshold voltage set by the LEVEL⇧ and LEVEL⇩ controls. The CH1, CH2, CH3, and CH4 pushbuttons indicate which channel's threshold voltage is being monitored.

PROGRAM TRIGGER MODE

The CH1, CH2, CH3, CH4, CLEAR, AND, OR, NOT, and EDGE pushbuttons are active in the PROG TRIG mode. These controls are explained next.

CH1, CH2, CH3, and CH4. The CH1, CH2, CH3, and CH4 pushbutton switches are used with the AND, OR and NOT pushbuttons to program the TRIGGER FUNCTION, (e.g., keystroke sequence; CH1 AND CH2 AND CH3 OR CH4).

AND. The AND pushbutton enters the logical AND operator into the Boolean TRIGGER FUNCTION. AND serves as a delimiter for the CH1 through CH4, NOT, and EDGE pushbuttons.

OR. The OR pushbutton enters the logical OR operator into the Boolean TRIGGER FUNCTION. OR also serves as a delimiter for the CH1 through CH4, NOT, and EDGE pushbuttons.

CLEAR. The CLEAR pushbutton erases the TRIGGER FUNCTION program currently displayed by the TRIGGER FUNCTION indicators. The other stored TRIGGER FUNCTION program remains unaffected by the CLEAR operation (see A, B and A THEN B).

NOT. The NOT pushbutton is used to negate a variable in the Boolean TRIGGER FUNCTION. For example, if CH1 is entered into the TRIGGER FUNCTION display (that is, CH1 is an active HI, red), pressing the NOT key will change it to an active LO (green). Successively pressing the NOT key will alternately change the CH1 indicator from HI to LO; this sequence will continue until a delimiter is entered (AND or OR).

EDGE. The EDGE pushbutton is used to change a level sensitive variable in a Boolean TRIGGER FUNCTION from level to edge sensitive. The NOT pushbutton is used with the EDGE pushbutton to select falling edge sensitivity. For example, the keystroke sequence CH1 EDGE programs the 7A42 to trigger on the rising transition of CH1; the keystroke sequence CH3 NOT EDGE sets it to trigger on the falling transition of CH3. Pressing the EDGE key twice changes the channel to edge-sensitive and back to level-sensitive, similar to the operation of the NOT key.

The 7A42 allows one independent EDGE-sensitive channel per product in each TRIGGER FUNCTION (A and B).

NOTE

The channel (CH1, CH2, CH3 or CH4), EDGE, and NOT keys can be entered in any order. For instance, the keystroke sequences CH1 NOT EDGE, NOT CH1 EDGE, and EDGE NOT CH1 are equivalent.

If the product already contains one edge-sensitive channel at the time a second edge-sensitive channel is entered into the same product, the last entered channel will receive the edge-sensitive status. The previous edge-sensitive channel will become level-sensitive only. This is because only one edge-sensitive channel per product is allowed. If the last entered channel is converted back to level-sensitive, the previous edge-sensitive channel will again become edge-sensitive.

THEORY OF OPERATION

This section describes the circuitry in the 7A42 Logic Triggered Vertical Amplifier. The description starts with a discussion of the instrument, using the block diagram shown in Figure 2-1. Next, each circuit is described in detail with supporting illustrations, where appropriate, to show the relation between the stages in each major circuit. Detailed schematic diagrams of each circuit are located in the Diagrams and Circuit Board Illustrations section at the back of this manual. Refer to these schematics throughout the following description for specific values and relationships.

BLOCK DIAGRAM

The following discussion presents an overview of the 7A42 before discussing the individual circuits in detail. In the simplified block diagram shown in Figure 2-1, each major circuit has a block. The number(s) in each block refer(s) to the schematic diagram(s) that show(s) the complete circuitry. The schematic diagrams are located at the back of this manual.

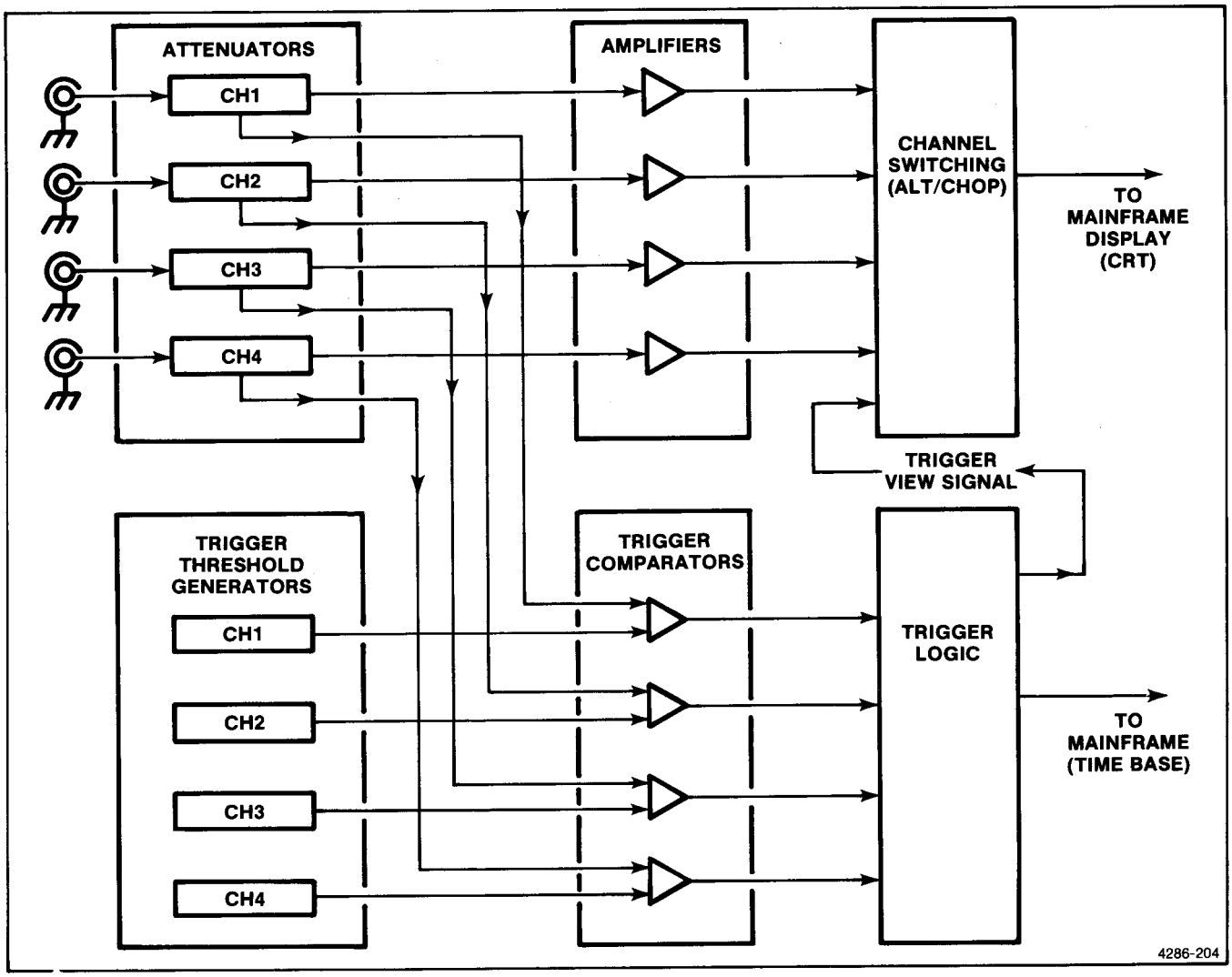


Figure 2-1. Simplified Block Diagram.

DESCRIPTION

The 7A42 has six functional blocks of circuitry; attenuators, amplifiers, channel-switching, trigger-threshold generators, trigger comparators, and trigger logic (see Fig. 2-1).

Each channel (Ch1 through Ch4) has its own attenuator, amplifier, trigger-threshold generator, and trigger comparator. Impedance selection (50 ohms or 1 megohm) and gain switching (volts/div) are accomplished by the attenuator. Each channel's attenuator has two signal outputs, one for the trigger comparator and another for the amplifier.

The amplifiers provide the gain necessary to drive the vertical amplifiers in the host oscilloscope. The channel-switching stage provides vertical signal processing to display the channel traces and the trigger-view trace on the host oscilloscope crt. This is accomplished by either chopping between the channels selected for display, or by displaying them alternately after each sweep.

The trigger comparator compares the signal from the attenuator with the voltage from the trigger-threshold generator. When the signal from the attenuator exceeds the threshold voltage, the trigger comparator produces an output which is applied to the trigger-logic stage.

The trigger-logic stage accepts outputs from the comparator and compares them with the programmed logic level of each channel. When the applied input signal(s) match the programmed trigger-logic conditions, a trigger pulse is produced. The user sets the trigger-logic conditions via the 7A42 front panel.

TABLE 2-1
Signal Name Dictionary

Signal Name	Description	Located on Diagram
+15B	+15 volt power supply—Decoupled mainframe power supply from right side of 7A42.	1, 2, 4, 10, 11
+5B	+5 volt power supply—Decoupled power supply from right side of 7A42.	1, 2, 4, 10, 11
+5C	+5 volt power supply—Decoupled mainframe supply from left side of 7A42.	1, 2, 4, 10, 11
+5D	+5 volt power supply—Digital power supply from Power Supply Board.	1, 2, 4, 10, 11
-15B	-15 volt power supply—Decoupled mainframe power supply from left side of 7A42.	4, 5, 6, 7, 8, 9, 10
-15C	-15 volt power supply—Decoupled power supply from left side of 7A42.	3, 4, 7, 10, 11
-2D	-2 volt power supply—Source is Power Supply Board.	1, 5, 6, 7, 8, 9, 11
-5D	-5 volt power supply—Source is Power Supply Board.	1, 5, 6, 7, 8, 9, 11
-5V1--5V4	Separate -5 volt power supplies to CH1-CH4 attenuator hybrids.	2, 11
-11V1--11V4	Separate -11 volt supplies to CH1-CH4 attenuator hybrids.	2, 11
1AXON, ...4BYON	Channel (1), Function (A), First Product (X), On—Control lines from the trigger logic control shift register level shifters to the Boolean logic. These lines gate the desired signals into the Boolean logic.	5
$\overline{\text{1AXINV}}$, ...$\overline{\text{4BYINV}}$	Channel (1), Function (A), First Product (X), Invert—Control lines from the trigger logic control shift register level shifters to the Boolean logic. These lines selectively invert the input signals.	5
1CW-4CW	Clockwise—Connections to CH1 position control pot. There is 0 ohms between 1W (wiper) and this pin when the knob is rotated to the clockwise (CW) position.	3, 12

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
1CCW-4CCW	Counterclockwise—Connections to CH1 position control potentiometer. There is 0 ohms between this pin and pin 1W (wiper) when the knob is rotated to the counterclockwise (CCW) position.	3, 12
1W-4W	Wiper—Wiper connection of CH1 position control potentiometer.	3, 12
$\overline{7854}$	7854—Decoded read strobe used to determine the location of link-plug jumper 540.	9
A9-A11	Address—Address lines to an address decoder on the Digital Board.	4, 9
$\overline{\text{A MODE}}$	A MODE—When low, enables trigger function A.	7, 8
$\overline{\text{A THEN B}}$	A THEN B—A control signal to enable the A THEN B latch.	7, 8
ALE	Address Latch Enable—Decodes the multiplexed AD bus from the microprocessor.	9
ALT	ALT—Selects ALT display mode.	4
ALT DRIVE	Mainframe ALT DRIVE—A6 of Main Interface connector.	4
ALTSN	ALT Sync—When high, this signal synchronizes the displayed channel to the ALT DRIVE signal.	4
$\overline{\text{AT COL}}$	Attenuator Column—An address decoded write select which clocks the Attenuator Column latch (part of the armature relay driver circuit).	2, 4
$\overline{\text{AT ROW}}$	Attenuator Row—An address decoded write select which clocks the Attenuator Row latch (part of the armature relay driver circuit).	2, 4
BD0-BD7	Buffered Data—Buffered Data Bus lines zero through seven (external to kernal).	1, 2, 4, 5, 8, 9, 10, 12
BEXTCLK	Buffered External Clock—This is the external clock signal from the clock buffer to the edge detector.	6, 7
BUSCLR	Bus Clear—This signal (in the XBUSX diagnostic test) lights a LED if the External Bus is operational.	9
$\overline{\text{CATS}}$	Not implemented.	9
$\overline{\text{CATSRD}}$	Not implemented.	9
$\overline{\text{CH13}}$, $\overline{\text{CH24}}$	Control lines to the (CH1, CH2) and (CH3, CH4) channel switches (M211s).	3, 4
$\overline{\text{CH12}}$, $\overline{\text{CH34}}$	Control lines to the (CH1, CH2) or (CH3, CH4) channel switch (M211).	3, 4
CH1 COL	Channel 1 Column—7K-series CH1 column readout information.	10
CH1 ROW	Channel 1 Row—7K-series CH1 row readout information.	10
CH1-CH4 SIG	Input lines from the hybrid attenuator impedance converter to the trigger amplifier.	3
$\overline{\text{CH1-CH4}}$	CH1-CH4—Indicates currently displayed channel when low.	4

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
CH2 COL	Channel 2 Column—7K-series CH2 column readout information.	10
CH2 ROW	Channel 2 Row—7K-series CH2 row readout information.	10
CHOP	CHOP—Selects CHOP display mode.	4
CHOP DRIVE	CHOP DRIVE—A5 of Main Interface connector.	4
$\overline{\text{DSPC}}$	Display Control—An address decoded write select which clocks the Display Control latch.	4
$\overline{\text{DSPT}}$	Display Test—An address decoded write select which clocks the Display Test latch.	4
$\overline{\text{DSPV}}$	Display View—Channel Switch signal controlling Trigger View display.	3, 4
DVD0-DVD3	DVM Digit—Probe Offset DVM display Digit drivers (active low).	1, 12
$\overline{\text{DVM LED}}$	Digital Volt Meter LED—An address decoded write select which clocks the Probe Offset DVM display driver IC (7218B).	1, 4
DVS0-DVS7	DVM Segment—Probe Offset DVM display Segment drivers (active high).	1, 12
$\overline{\text{ERRTRG}}$	Error Trigger—When used in the diagnostics mode, is pulsed by diagnostic firmware whenever an error is detected (active low).	9
$\overline{\text{ETST}}$	Enable Test—Used to enable the Wait State Test circuit.	9
$\overline{\text{EXEDGEN}}$	External Edge Enable—When low enables external clock. See Theory of Operation for more details.	6, 7
EXT CLK EXER	External Clock Exercise—This signal is high during some diagnostics to control the state of the External Clock Input.	7, 8
EXT CLK SLOPE	External Clock Slope—A control signal which selects the desired external clock edge.	7, 8
EXT CLK SYNC	External Clock Sync—A control signal which enables the external clock buffer when external clock synchronization is desired.	7, 8
EXT CLOCK INPUT	External Clock Input—This input is from a peltola connector on the front panel jack to the Trigger Board.	7
FD0-7	Filtered Data bus—The buffered data bus after passing through some series resistors that slow the transistions.	5
FILTER OFF	Filter Off—A control signal used to disable the trigger filter.	6
FNA, FNB	Function A, Function B—The output of the Boolean logic. These lines go high when the function is true.	5, 7
FPLC0-FPLC7	Front Panel LED Column—Front panel LED column drivers zero through seven.	1, 12
$\overline{\text{FP LED}}$	Front Panel LED—An address decoded write select which clocks the display driver IC (7218A) of the Front Panel LEDs.	1, 4
FPLR0-FPLR4	Front Panel LED Row—Front Panel LED row drivers zero through four.	1, 12
$\overline{\text{GENIN}}$	General Input—An address decoded read select (active low) used to read the General Input latch onto the data bus.	9

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
$\overline{\text{GENOUT}}$	General Output—Address decoded write select (active low) used to write data into the General Output latch.	9
$\overline{\text{INTAC}}$	Interrupt Acknowledge—Resets the RST5.5 latch (real time interrupt).	9
KPD1-4	Relay Pull Down—Pull-down lines in armature drive circuit.	2, 12
KPU1-4	Relay Pull Up—Pull-up lines in armature drive circuit.	2, 12
KPUD1-5	Relay Pull Up-Down—Pull-up/down lines in armature drive circuit.	2, 12
$\overline{\text{KYCD}}$	Key Code—An address decoded read select (active low) used to read keycode data.	1, 9
$\overline{\text{LO READ}}$	Lower Readout—An address decoded write select which clocks the lower readout latch.	4, 10
$\overline{\text{MATRIX}}$	Matrix—Address decoded write select (active low) to LED matrix driver IC.	1, 9
$\overline{\text{MENAX-MENBY}}$	Multiplexer Enable, Function (A), First Product (X)—Control lines from the trigger logic control shift register level shifters to the Edge Detectors. These lines enable the multiplexer for an edge sensitive channel.	6, 8
MS0AX, ...MS2BY	Multiplexer Select, Channel (0), Function (A) First Product (X)—Control lines from the trigger logic control shift register level shifters to the Edge Detectors. These lines select the desired edge sensitive channel.	6, 8
MXCX, MXCY	Matrix Column X and Matrix Column Y—Matrix LED column driver lines (active low).	1, 12
MXR0-MXR7	Matrix Rows—Matrix LED row driver lines (active high) zero through seven.	1, 12
PC1-4	Probe Coding—Probe coding channels one through four.	2, 9, 12
PIM	Plug-In Mode—TTL version of Plug-In Mode, B35 of 7K-series interface.	4
$\overline{\text{PODAC}}$	Probe Offset DAC—Address decoded select (active low) used to write data to the Probe Offset DAC which is used to do an analog to digital conversion of the Probe Offset voltage.	9
POG	Probe Offset Green—A signal which lights the green Probe Offset LED.	4, 12
POR	Probe Offset Red—A signal which lights the red Probe Offset LED.	4, 12
$\overline{\text{PUPCK}}$	Power Up Clock—Clock signal indicates instrument power up.	9
$\overline{\text{PUST1}}$	Pull Up Strobe 1—Strobe which clocks the armature relay drive circuitry.	2
$\overline{\text{PUST2}}$	Pull Up Strobe 2—Strobe which clocks the armature relay drive circuitry.	2
PUST/$\overline{\text{PDST}}$	Pull Up Strobe/Pull Down Strobe—Strobe which clocks the armature relay drive circuitry.	2

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
QWR	Qualified Write—This is the qualified WR of the 8085 (active high) with A12 ∧ A13 ∧ A14.	4, 9, 12
$\overline{\text{RAM}}$	Random Access Memory—An address decoded select (active low) which is further decoded to produce RAM chip select.	9
RD	Read—Read strobe.	9
$\overline{\text{RD}}$	Read—Compliment of Read strobe.	9
RD+WR	Read OR Write—Signal is high during Read OR Write operation.	9
$\overline{\text{RELN}}$	Relay Enable—This signal is used to disable the attenuator relay drivers at power-up until the processor can initialize the system. It also disables the piezo speaker in a similar fashion.	2, 4, 9, 12
$\overline{\text{RESET INPUT}}$	Reset Input—This input is a peltola connector from the LED Board to the Trigger Board.	7
RL0-RL7	Return Lines—Keyboard switch Return Lines (active low) zero through seven.	1, 12
RSAX, RSAY	Reset, Function (A), First Product (X)—Reset signal for trigger function A.	6, 7
RST 5.5	RST 5.5—Interrupt to 8085 which occurs with the real time clock.	1, 9
RST 6.5	RST 6.5—Interrupt to 8085 from the keyboard decoder.	1, 9
RST 7.5	RST 7.5—Interrupt to 8085 which occurs with each timeslot.	9, 10, 12
$\overline{\text{ARST}}$	Restart—No automatic restart when low.	9
SA START	Signature Analysis Start—Signature Analysis Start bit.	9
SA STOP	Signature Analysis Stop—Signature Analysis Stop bit.	9
SACK	Signature Analysis Clock—Signature Analysis Clock bit.	9
SID	Serial Input Data—Serial input to 8085. This signal is an inverted TTL representation of TS1 (Time Slot one).	9, 10, 12
$\overline{\text{SINGCH}}$	Single Channel—When low this line indicates only a single channel is displayed.	4
SL0-SL3	Scan Lines—Keyboard switch Scan Lines (active high) zero through three.	1, 12
SOD	Serial Output Data—Serial output data from 8085. This is used as a control to the 7218 Display driver chips.	1, 9
STAX, ...STBY	Strobe, Function (A), First Product (X)—Strobe trigger function.	5, 6
$\overline{\text{SYNCAX}}$, ...$\overline{\text{SYNCBY}}$	Sync, Function (A), First Product (X)—Control lines from the trigger logic control shift register level shifters to the Edge Detectors. The line is low when edge sensitivity or external clock is active.	5, 6
TB0	Test bit 0—Used in Self Test and Diagnostics from Trigger Board.	6, 7, 9
TB1	Test Bit 1—Used in Self Test and Diagnostics from Digital Board.	4, 9, 12

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
TB2	Test bit 2—Used in Self Test and Diagnostics from Trigger Board.	6, 9, 12
TB3	Test bit 3—Used in Self Test and Diagnostics from Trigger Board.	5, 6, 9, 12
TB4	Test bit 4—Used in Self Test and Diagnostics from Trigger Board.	5, 6, 9, 12
TB5	Test bit 5—Used in Self Test and Diagnostics from Trigger Board.	8, 9, 12
TEST	Test—When active, this line causes the PAL to be in test mode, e.g., setup for LSSD (Level Sensitive Scan Design).	4
TFP1-TFP2	Trigger Filter Pot—The two connections to the trigger filter potentiometer.	5, 12
TFS1-TFS2	Trigger Filter Switch—The two connections to the trigger filter switch.	6, 12
TIP	Tip—Front panel Probe Offset jack.	9, 12
TRAP	Trap—A nonmaskable interrupt to the 8085. It will occur when any of the 50 ohm input resistors are over dissipated. This interrupt is rising edge sensitive.	2, 9, 12
TRAP1-TRAP4	Trap—The source of these signals is the attenuator hybrid. These analog signals represent the power dissipation of the 50 ohm input resistors.	2, 12
TRIG VIEW OUT	Trigger View Output—The Trigger View output signal to the display channel switch on the Amplifier Board.	7
TRIGEN	Trigger Enable—A control signal which enables the trigger logic output and releases reset to the A THEN B flip flop.	7, 8
$\overline{\text{TRSH1}}$-$\overline{\text{TRSH4}}$	Threshold 1-Threshold 4—Address decoded write lines (active low) used to write the trigger threshold DACs.	5, 9, 12
TS1	Time Slot One—7K-series readout.	10
TSX	Time Slot X—This signal is the result of diode ORing Time Slot lines one through ten.	10
$\overline{\text{UP READ}}$	Upper Readout—An address decoded write select which clocks the upper readout latch.	4, 10
$\overline{\text{WRKB}}$	Write Keyboard—An address decoded write select (active low) to keyboard controller IC.	1, 9
$\overline{\text{WRMD}}$	Write Mode—An address decoded write select line (active low) used to clock the trigger mode latch on the Trigger Board.	8, 9, 12
$\overline{\text{WRTL}}$	Write Trigger Logic—An address decoded write line (active low) used to clock the trigger function into the trigger control shift registers.	8, 9, 12
$\overline{\text{XBUSX}}$	External Bus Exercise—An address decoded select (active low) used to determine if the XBUSX strap is installed.	9
$\overline{\text{XWR}}$	X Write—A system write strobe which becomes a read strobe during signature analysis.	9

DETAILED CIRCUIT OPERATION

Complete schematic diagrams are provided in Section 7, Diagrams and Circuit Board Illustrations. The number inside the diamond preceding a heading in the following discussions refers to the schematic diagram for that circuit. The schematic diagrams contain wide shaded borders around the major stages of the circuit to conveniently locate the components mentioned in the following discussions. The name of each stage is given in a shaded box on the diagram, and appears as a subheading in the discussion of that schematic diagram.

All logic functions are described using the positive logic convention. Positive logic is a system of notation where the more positive of two levels (HI) is called the true or 1-state; the more negative level (LO) is called the false of 0-state. The HI-LO method of notation is used in this logic description. The specific voltages that constitute a HI or LO state vary between individual devices. Whenever possible, the input and output lines are named to indicate the function that they perform when in the HI (true) state.

1 FRONT PANEL DISPLAY AND CONTROL

KEYBOARD DECODER

The keyboard decoder IC decodes the keyboard switch array, informs the MPU (Microprocessor Unit) when a key is pressed, and sends a binary code to the MPU indicating which key was pressed.

The keyboard is continually scanned by U205. When a key is pressed, U205 interrupts the MPU (via RST 6.5) and loads the corresponding eight-bit code onto an internal first-in/first-out register which is then read by the MPU.

Detailed information about the internal functioning of the keyboard decoder IC may be obtained from the manufacturer's data books.

CHANNEL STATUS AND SWITCH LED DRIVER

The 7218 LED driver (U320) accepts binary data from the MPU and drives the Channel Status LEDs and the Switch LEDs. The 7218 LED driver is set in 'no decode' mode to drive the LEDs directly with the binary data from the MPU. Refer to the manufacturer's data for detailed information on the internal functioning and programming of the 7218 LED driver.

THRESHOLD DISPLAY DRIVER

The Threshold Display Driver (U110) accepts BCD data from the MPU and drives the Threshold Display array. The 7218 LED driver is configured to store and decode the input data from the MPU and produce the appropriate outputs to drive the seven-segment LED displays.

MATRIX LED DRIVER

The Matrix LED Driver circuit (U105) is essentially the same as the Channel Status and Switch LED Driver (U320) described above, except that the output of U105 drives the Matrix LEDs. (Also, U105 is designed to drive a common-cathode array, where U320 drives a common-anode array.)

2 ATTENUATORS AND CONTROL

ARMATURE RELAY DRIVERS

Figure 2-2 shows a simplified block diagram of the Armature Relay Matrix used in the 7A42. The relays are arranged in this matrix to minimize the total number of drives and interconnects.

Each series pair of coils represents a single relay. The nomenclature beside each coil shows the function invoked when current is pulsed in the indicated direction.

The KPU (Pull Up) and KPD (Pull Down) drive lines are unidirectional. The KPUD (Pull Up Down) lines are bidirectional (able to source or sink current).

While idle, all outputs of AT COL latch (ATtenuator COLumn latch) A7 U421 are high, as are pins 15 and 16 of AT ROW latch (ATtenuator ROW latch) A7 U420. This results in all relay drive lines being high impedance.

To activate a relay, the drive signal must be present for about 15 ms.

As an example, the following is the sequence of events which take place to insert the CH1 2.5X attenuator. ($ indicates a hexadecimal number.)

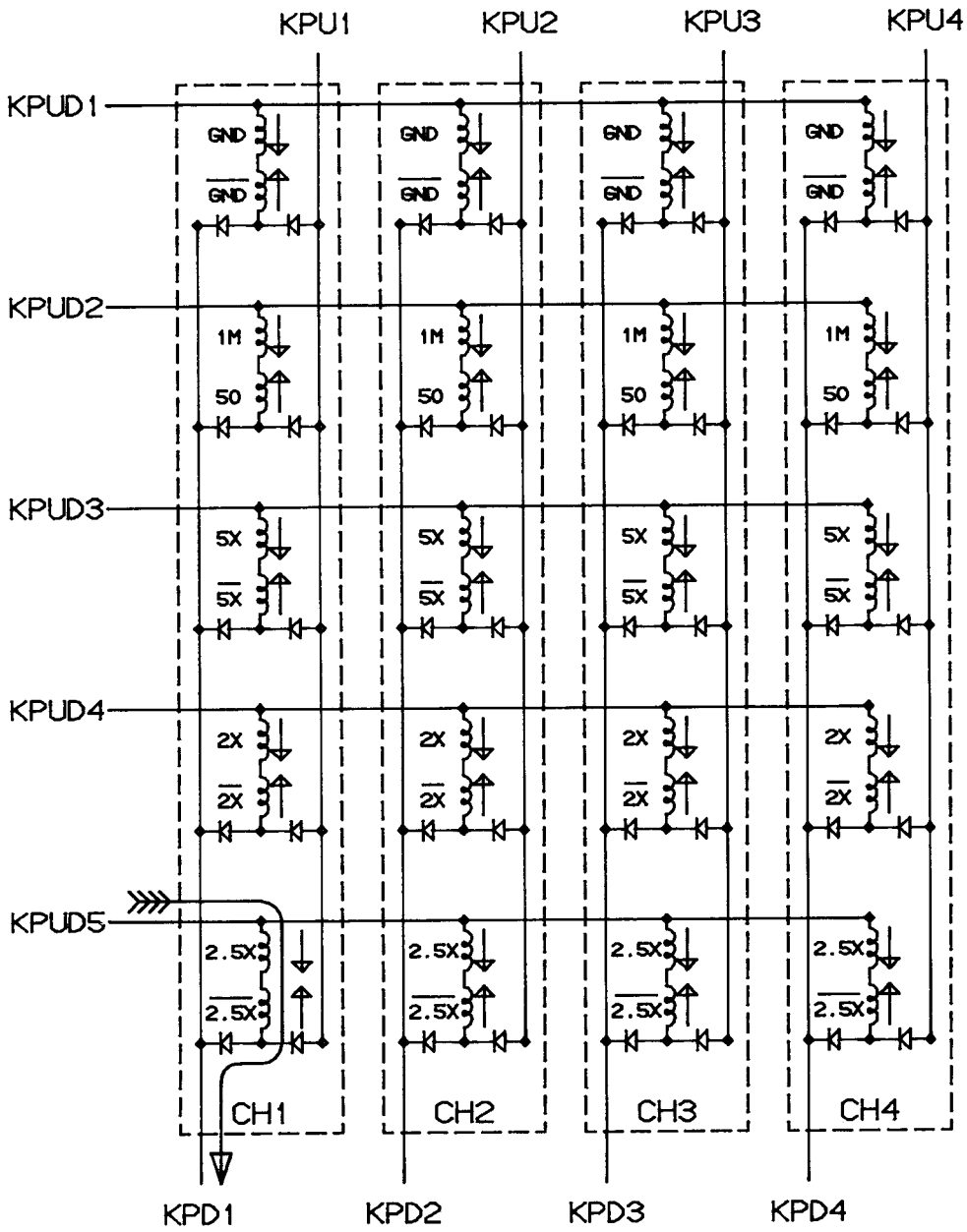


Figure 2-2. Armature Relay Matrix (Actuating the CH1 2.5X attenuator).

1. Write $FD to AT COL latch: selects KPD1 (only one output of this latch will be low at a time to insure that KPU and KPD drives are never activated simultaneously).

2. Write $70 to the AT ROW latch: set PUST/$\overline{\text{PDST}}$ low to enable KPD1; select KPUD5 to pull up, all other KPUD lines to pull low; $\overline{\text{PUST1}}$, $\overline{\text{PUST2}}$ are set high (same as idle state).

3. Write $10 to AT ROW latch: same data as step 2, but this time with $\overline{\text{PUST1}}$ and $\overline{\text{PUST2}}$ set low to enable KPUD drives.

4. Wait approximately 15 ms.

5. Write $FF to the AT COL latch: disables all KPU, KPD lines.

6. Wait 5 ms for transients to decay. (see below)

7. Write XX11XXXX (binary) to the AT ROW latch to disable the KPUD lines. Diodes CR520, CR521, CR530, and CR630 on the KPU lines protect the 75325 from voltage spikes when these lines turn off. There is similar protection internal to the 75325's on the KPD lines. Step 6 above insures that relay coil current has decayed before releasing the KPUD drive.

Jumper A7 J401, RELN, is provided to disable the relay drives in times of trouble (e.g., processor out of control).

The dc resistance of the relay coils is about 40 ohms each. This resistance along with the 18 ohm collector resistance on pin 1 of the 75325's results in about 12 volts across the pair of relay coils being activated.

OVERLOAD COMPARATORS

Four identical voltage comparator circuits are used to monitor the TRAP lines from the Attenuator hybrids. Their open collector outputs are wire-ORed at pull-up resistor R236. If any of the four attenuator 50-ohm termination resistors is over-dissipated, it's associated negative temperature coefficient sensing network will drive the comparator's + input below the reference voltage set by R234, R235, CR230, and CR231. This drives the output low, which is inverted through U830 to cause a high priority TRAP interrupt to the processor. The processor then disconnects all inputs using relay control.

The feedback resistors, along with the 1K resistors and 0.1μF capacitors provide hysteresis and noise filtering.

Trigger Pickoff

The attenuator modules send the trigger output signal through the attenuator control board and a series resistance to the trigger board comparators.

CHANNEL SWITCHING AND AMPLIFIERS

CHANNEL AMPLIFIERS

Channels 1 through 4 each have an independent amplifier stage which provides voltage gain between the attenuator output and the channel switch input. All four of these stages are identical, therefore, only channel 1 will be described.

The input signal from the attenuator module enters the amplifier board through two interconnect pins. The single ended signal (with an offset of -5 volts) then goes through a small balun transformer to convert the high-frequency component into a true differential signal. The -5 volt offset was chosen at this point so that no further level shifting in the amplifier path would be necessary. The balun output is connected to the input bases of a differential amplifier IC. After looping through the bases it is terminated by R1011. Capacitors integral to the ECB and the inductance of the amplifier IC leadframe and bondwires form bridged, tee-coil peaking, at the bases to offer a resistive load impedance to the attenuator and improve the bandwidth of the stage.

The amplifier stages use hybrid thick-film resistor networks as bias and 'long tails'. The resistor networks are placed between the channel amplifiers and are shared between adjacent channels. A total of five networks are needed; the networks above channel 1 and below channel 4 are only partially used. Within the network are three resistors in a series divider configuration from ground to -5 volts. Taps at -3 volts and -4 volts set the bias inside the amplifier to ensure that the signal is sent through the proper pair of output transistors. For a given amplifier IC, the network located physically below that IC provides these bias voltages.

The resistor network located above an amplifier IC serves as a long-tail current source to the amplifier emitters. The long tail is divided into two sections by a tap. Low-frequency (thermal) compensation is connected between the taps. High-frequency compensation is connected directly between the emitters. The total resistance is set to provide a 12.5 mA current source at each emitter.

The outputs of the amplifiers are connected to the channel switches through 75-ohm microstrip transmission lines on the ECB. The individual channel gain adjustment is made with a trimmer potentiometer that shunts a portion of the differential signal. Diodes to ground provide protection to the channel switches if the amplifier IC inadvertently becomes disconnected.

Position Control

The position control circuit provides 6.5 mA of the 12.5 mA standing current needed by the amplifier stage. The

trace is positioned by adding additional current to one side and taking an equal amount from the other. For each channel, the two PNP transistors serve as these position control current sources. They are controlled by the front-panel POSITION control and a long-tail network chosen to minimize the common mode positioning current variation over the entire position range. Diodes CR900 and CR910 protect the channel switch inputs if the position control potentiometer should inadvertently become disconnected.

The position control circuit is isolated from the analog signal lines by series resistors R910 and R911 and balun transformer T800 that has been installed backwards. The transformer will pass common mode signals but will reject differential signals. Series resistor, R800, and capacitor, C700, shunting the position control transistors, provide mid-frequency compensation.

CHANNEL SWITCHES

The 7A42 uses three hybrid channel switches. Channel switch U600 combines the channel 1 amplifier output with that of channel 2. Channel switch U640 combines the outputs of channels 3 and 4. The outputs of U600 and U640, after passing through delay lines, are combined by a third channel switch, U240, which also introduces the trigger view signal.

The channel switches select one output signal from four input signals. The desired input signal is selected via four TTL-compatible control lines (pins 13, 14, 24, and 25). The output is intended to drive a 150-ohm load and provide reverse termination for a delay line.

Inputs A and B require a current source drive and have a transimpedance of 300 ohms from input to output. Inputs C and D require a voltage drive from a 150-ohm source and have a voltage gain of 0.75.

The control lines are active low, i.e., when low the associated input signal will appear at the output.

The outputs from the channel 1 through channel 4 amplifier stages are connected to the A and B inputs of the first two channel switches. These inputs supply the remaining 6 ma of standing current required by the amplifier stage output.

Two bias networks are required to support these channel switches. The 1.24 K resistor provides an accurate 4 mA bias, while the variable resistance to ground is used to optimize the front corner of the step response. The pair of 75-ohm resistors connect an unused portion of the circuit to ground.

The channel switch output impedance is 75 ohms per side. The outputs drive two matched 15.5 ns, 150-ohm delay lines, DL600 and DL640. The delay lines are terminated by the third channel-switch's inputs (C and D). The trigger view signal is injected through input B.

The resistor network across the channel switch outputs, along with the channel switch output impedance, provides a 50-ohm reverse termination (per side) and a small amount of front-panel gain adjustment.

The trigger view signal arrives at the A5 Amplifier board as a differential signal. The associated resistors set the trigger view display amplitude, and the TRIGGER VIEW POSITION control allows it to be moved to any location on screen.

4 DISPLAY CONTROL

ADDRESS DECODER AND LATCH

The QWR (Qualified WRite) and processor address lines A9, A10, and A11 are used to generate eight write strobes on the A7 Digital board using an LS138 address decoding chip. The write strobes are the same width as the processor $\overline{WR}$ signal (700 ns) and are active low.

DISPLAY CONTROL

Channel switching is predominantly controlled by U800, a PAL16R6, which contains a fuse pattern configuring it as a synchronous state machine. Channels to be displayed are presented to the PAL as the input vector via Display Control latch outputs D1 through D5. Here D1 corresponds to CH1, D2 to CH2, etc. and D5 to Trigger View.

With each clock to the PAL on pin 9, the output vector on pins 14 ($\overline{CH5}$) through 18 ($\overline{CH1}$) advances to display the next channel. The outputs are active low and mutually exclusive.

As an example, assume that the desired display selected from the front panel is CH1, CH3, and Trigger View. With each clock pulse to the PAL the outputs would change as follows:

D1	D2	D3	D4	D5	CH1	CH2	CH3	CH4	CH5
1	0	1	0	1	0	1	1	1	1
1	0	1	0	1	1	1	0	1	1
1	0	1	0	1	1	1	1	1	0
1	0	1	0	1	0	1	1	1	1
	etc.								

The PAL is clocked on both rising and falling edges of either the Chop Drive or Alt Drive signals which are supplied by the mainframe and selected through analog switch U820.

The voltage levels of CHOP and ALT Drive are typically -0.6 to 1.1 volts and are not suitable to drive the TTL inputs of the PAL directly. Transistors Q810 and Q811, and their surrounding components, form a comparator with hysteresis and variable reference level to decrease propagation delay from Chop Drive's edge to channel switch settling time. The varying reference level is necessary because of the slow rise and fall times of Chop Drive.

In "test" mode, when TEST is high on pin 7 of the PAL, the PAL's internals are reconfigured so that it can be tested using Level Sensitive Scan Design techniques. Psuedo random data is entered to the PAL by the processor on D1 of the Display Control latch, and clocked in with $\overline{\text{BUSCK}}$ of the Display Test latch. Output data from the PAL is read back by the processor via TB1 and entered into a Signature Analysis routine.

Other outputs on the Display Test latch include $\overline{\text{HORN}}$, used to activate the piezo speaker; MODE, used as an input to U110 and U320 when writing their control words, $\overline{\text{POG}}$ and $\overline{\text{POR}}$; Probe Offset Green and Probe Offset Red LED drivers.

The negative bias for U820 is set by CR810, CR811, and R811.

HORN

Timer U730 is wired as an astable multivibrator which freeruns at about 4 kHz. The oscillator is disabled by pulling the Discharge line, pin 7 to ground. The software controls the horn through the Display Test latch and saturating switch Q720D. It is also disabled at power up by Q720B, until the processor has initialized the hardware.

5

TRIGGER COMPARATORS, BOOLEAN LOGIC, AND FILTERS

THRESHOLD DACs

The trigger threshold voltages for channels 1 through 4 are determined independently by threshold DACs U1020, U1030, U1022, and U1032 respectively. The DACs are controlled by the buffered data bus, BD0-BD7, which passes through series resistances to form the filtered data bus, FD0-FD7. Slower transition times on the filtered data bus requires that writes to the A6 Trigger board include a wait state. A low level on select lines $\overline{\text{TRSH1}}$-$\overline{\text{TRSH4}}$ latches data into the DACs. The analog output voltage range of the DACs is from 0 volts to +2.55 volts. A resistive divider network shifts this range down to -0.48 volts to +0.48 volts at the comparator inputs and provides gain and offset adjustment.

COMPARATORS

The channel 1 through 4 comparators, U200, U210, U220, and U230, convert the analog signals from the channel 1 through 4 attenuators to ECL level complementary digital signals. The 24.3K resistors from the inverted output to the negative inputs supply positive feedback and provide a fixed amount of hysteresis. The comparator outputs drive the Boolean Logic and Edge Detectors.

BOOLEAN LOGIC

The Boolean Logic is divided into two parts, function A and function B. Each function consists of two products of four bits (CH1-CH4). Each product is implemented with AND gates from U300, U302, U332, and U330 which select the channels forming the product, and with EXOR gates from U400, U410, U420, and U430, which set those channels to be active high or active low. The AND function which forms the product is a negative logic wired-AND of the EXOR gate outputs. The Boolean Logic gates are controlled by 32 lines from the Trigger Control hardware.

There are several rules regarding the control of the Boolean Logic gates. The ON lines (1AXON, 3BYON, etc.) must be low for any unused channels in a product. The $\overline{\text{INV}}$ lines ($\overline{\text{1AXINV}}$, $\overline{\text{3BYINV}}$, etc.) must be manipulated depending upon the state of the rest of the channels in the product. If any channel in a particular product is used, the $\overline{\text{INV}}$ lines of unused channels in that product (if any) must be set low. If the entire product is unused, $\overline{\text{INV}}$ must be set high for at least one channel. If a given product is edge sensitive and contains no level sensitive channels, $\overline{\text{INV}}$ must be set low for all channels in that product.

TRIGGER FILTERS

The signal path is from the wired-AND of each product through gates U402A, U412A, U422A, and U432A where the two products of each function are wire-ORed together forming signals FNA and FNB. These signals are active high (high when the function is true). The function A and B trigger filters are separate but identical, and provide amounts of time delay which track one another. The trigger filter for a given function is not operational if either product in that function contains an edge-sensitive channel or if the trigger filter is turned off. The following description for function A applies to function B as well. If both products in function A are level sensitive and the trigger filter is turned on, the control lines STAX, and STAY will be low; $\overline{\text{SYNCAX}}$ and $\overline{\text{SYNCAY}}$ will be high. The output of U500A will be high until either product becomes true. At that time it will begin to go low at a rate determined by the 470 pF capacitor and the current source from U532. As soon as it is low enough to cross the switching threshold of U500D, positive feedback from U500Ds output speeds the transition and sends a positive going signal to U402B and U412B and then a negative going signal to

U402A and U402B. This negative level enables that gate and allows the waiting signal at the other input to pass through. The principal of the trigger filter is that if the delay time caused by the capacitor between U500A and U500D exceeds the time that the product is true, the resultant function, FNA, will not become true.

When the products become false (both high), the output of U500A will go high and rapidly charge the capacitor, readying it for the next cycle.

When the trigger filter is turned off from the front panel, the lines STAX and STAY from the edge detectors will go high. This presents low levels to U402A and U412A, enabling them continuously.

If, for example, the first product contains an edge sensitive channel and the second does not, $\overline{\text{SYNCAX}}$ will go low, $\overline{\text{SYNCAY}}$ will remain high. The trigger filter is now prevented from working with the first product by U500B. The signal STAX will strobe high corresponding to the edge sensitive channel transition in the first product. The level sensitive portion of that product will be gated through at this time only.

Transistor array Q532A-E provides twin tracking dc current sources to the function A and function B trigger filters. Each current source is twice the magnitude of the current flowing into the circuit through the 330 ohm resistor and therefore dependent upon the position of the front panel potentiometer. The base-emitter voltage for U532A, B, D, and E is set by U532C. Since all transistors are closely matched, their collector currents will be equal with equal base-emitter voltages.

6 EDGE DETECTORS

There are four independent edge detector circuits, one for each product in functions A and B. The following description for the one associated with the first product of function A applies to all the others as well. The channel 1 through 4 signals and their complements are presented to the input of the multiplexer, U310. If the product contains an edge sensitive channel, the control line $\overline{\text{MENAX}}$ will be low to enable the multiplexer output; lines MS0AX, MS1AX, and MS2AX will be high or low to select the proper channel and polarity so that the multiplexer output will make a negative going transition corresponding to the channel edge to which sensitivity has been programmed. Since $\overline{\text{MENAX}}$ is low, the output of U800B is low as is pin 3 of U700B. The signal $\overline{\text{SYNCAX}}$ goes low to disable the trigger filter. With BEXTCLK high, output of U510A is low, allowing U402C and U402D to be driven by the output of U310. Before the qualifying edge comes along, the output of U310 will be high, setting the output of U402C low. When the edge arrives, U310 output will go low and the output of U402D will go high momentarily until a high level has propagated to U402C's output, at which time it will return low. The width of this pulse is determined by the propagation delay of U402C and the added delay of the series resistor and shunt capacitor between U310 and U402C. This pulse becomes the STAX signal which strobes the level sensitive portion of the trigger function on to the output. When the output of U310 goes high, the circuitry is restored to its initial state.

All four edge detectors work in unison when the external clock circuitry is activated. In this mode, $\overline{\text{MENAX}}$, $\overline{\text{MENAY}}$, $\overline{\text{MENBX}}$, and $\overline{\text{MENBY}}$ are all high but the signal $\overline{\text{EXEDGEN}}$ is low. The external clock comes in with the signal BEXTCLK. When BEXTCLK goes high the output of U510A goes low and produces a STAX pulse and the falling edge of BEXTCLK restores the circuitry as above.

When the trigger filter is turned off from the front panel, the signal FILTER OFF goes high. If, for instance, function A contains no edge sensitive channels and the external clock is not being used, $\overline{\text{SYNCAX}}$ and $\overline{\text{SYNCAY}}$ will be high. With FILTER OFF high, the outputs of U700A and U700B will go high forcing the outputs of U510A, U510B, U402C, and U412C low, and therefore STAX and STAY will be high to prevent the trigger filter from functioning.

The function B edge detectors have several minor differences from those in function A. The outputs of U422C and U432C are not wire-ORed with signals from the reset circuitry as is function A. Finally, a test bit is picked off the output of U322 through a relatively high resistance for use in self test and extended diagnostics.

7 A THEN B LOGIC AND TRIGGER I/O

A THEN B LOGIC

The A THEN B Logic passes the trigger signal from the trigger filters to the trigger outputs in one of three modes: A mode, B mode, or A THEN B mode. The mode is determined by the control lines $\overline{\text{A THEN B}}$ and $\overline{\text{A MODE}}$. In A mode, $\overline{\text{A THEN B}}$ will be high and $\overline{\text{A MODE}}$ will be low. The FNA signal from the function A trigger filter can propagate through U600B and U610D to the trigger outputs. This is possible because U520B's output is high, U520A and U610B's outputs are low, preventing U600A from latching. In B mode, operation is similar

except the signal propagates from FNB through U600C and U610D to the trigger outputs. Both control lines must be high in this mode. FNA is blocked from getting through by U600B.

In A THEN B mode, control line $\overline{\text{A THEN B}}$ will be low and $\overline{\text{A MODE}}$ will be high. An occurrence of function A will arm the trigger. The next occurrence of function B causes a trigger output pulse and resets the armed condition. In this mode, the output of U610B is initially held high. When FNA goes high, this high state is latched by U600A. Gate U600B prevents this signal from reaching the trigger outputs. However, U600C becomes enabled so that when FNB goes high, a trigger output occurs. When this happens, the output of U600C goes high, causing the outputs of U520A and 610B to go low, and resets latch U600A in preparation for the next cycle. The width of the resulting trigger output pulse is set by the propagation delays of U520A and U610B. In this mode the A THEN B GATE OUTPUT is also active. Pin 15 of U600D goes high when high when function A occurs and back low again when function B occurs. By moving a jumper on the A6 Trigger Board, a representation of the A THEN B GATE will be piped to the Front-panel TRIGGER OUTPUT connector via U610A and U620B.

TRIGGER OUT AMPLIFIER

The trigger output signal is sent to a front-panel bnc connector (as well as to the time base). With its pin 7 normally low, U620A makes the trigger output signal into complementary ECL level signals to drive the front-panel Trigger Output Amplifier. The circuit consists of one differential amplifier stage with a single-ended output whose levels are about 2 volts high, and 0 volts low from a 50-ohm source impedance.

RESET BUFFER

The function of RESET differs slightly if the 7A42 is in A THEN B mode rather than A mode or B mode. In the latter modes, when the reset input is driven high, the trigger output is simply inhibited. In A THEN B mode, in addition to inhibiting the trigger output while high, RESET causes the armed condition to be reset if it has previously been set by function A being true. After reset terminates, normal triggering can resume.

A reset input signal more positive than about 0.5 volts causes the comparator stage (Q720, Q620) to switch, pulling signals RSAX, RSAY, and pin 10 of U520D high. When the collector of Q720 goes low, trigger output is immediately inhibited by U610D. That same signal propagates through U610B to reset the A THEN B latch U600A, assuming that the signal FNA is low. This is assured by RSAX and RSAY which act on U402C and U412C to force signals STAX and STAY low. The low signal at the collector of Q720 also forces $\overline{\text{EXEDGEN}}$ low and $\overline{\text{SYNCAX}}$ and $\overline{\text{SYNCAY}}$ (on diagram 6) low to disable the trigger filter path and guarantee a false FNA.

EXT CLOCK

If the external clock is active, the control line EXT CLK SYNC will be high to present an ECL low level to U520C which enables the external clock buffers, a low to U610C which enables the edge detectors, and a low to U630 which allows the trigger view multiplexer to pass the external clock signal to the A6 Amplifier Board.

The external clock can be selected to either TTL or ECL logic levels by an internal jumper. The TTL threshold is about +1.4 volts where the ECL threshold is about -1.3 volts. The external clock signal from the front-panel bnc goes to the TTL buffer and the internal jumper. If the jumper is in the TTL position, the ECL buffer (U520C) is disconnected. The TTL buffer consists of a differential amplifier stage with some positive feedback and hysteresis. The input to the stage is clamped to +5 volts and ground to prevent overdrive. The output has ECL level voltage swings. With the ECL buffer disconnected, the output of U520C is not pulling high so the TTL buffer can drive U620A. If the jumper is in the ECL position, the external clock input is now terminated by about 50 ohms to -2 volts to be compatible with ECL logic levels. Since the ECL high and low levels are both more negative than ground, the TTL buffer is always clamped in its low input state which results in a low output from Q724, thus allowing U520C to drive U620A. The input of U520C is clamped to ground and -5V to prevent damage from overdrive. The control line EXT CLK EXER is used in self test and extended diagnostics to synthesize a low level TTL clock level. If the jumper is in ECL, the input level is already low, so EXT CLK EXER will have no effect.

The slope of the external clock is controlled by line EXT CLK SLOPE. The edge detectors are sensitive to a rising edge of the signal BEXTCLK, so U620A is set to either invert or not invert to select the desired clock edge. EXT CLK SLOPE is set high for a rising clock edge and low for a falling. If EXT CLK SYNC is not active (low), the output of U520C is forced high, and EXT CLK SLOPE is set high to assure that BEXTCLK will be high so as not to interfere with the edge detectors in channel edge sensitivity. The BEXTCLK signal is driven into the edge detectors by U510A, B, C, and D on diagram 6.

TRIGGER VIEW SELECT

If the trigger view is turned on at the front panel, the trigger view trace will be a representation of the trigger out signal sent to the time base and to the front-panel output connector, unless the external clock is active. If the external clock is on, the trigger view trace will display a representation of that signal. The selection is made by multiplexer U630D which is controlled by the EXT CLK SYNC line. If the external clock is active, the signal on route to the multiplexer is delayed by U630A, B, and C to make the external clock trace on screen line up with the other analog traces.

8 TRIGGER CONTROL

TRIGGER CONTROL LATCH

The trigger control latch is set by the filtered data bus FD0-FD7 on a rising edge of select line $\overline{\text{WRMD}}$. In most cases, its outputs are level shifted to drive ECL inputs as described above. The only exceptions are EXT CLK EXER and TRIGEN. When TRIGEN is driven low it causes an internal reset. This is used to inhibit false trigger outputs during the loading of trigger functions into the trigger control shift registers. After the load is complete, TRIGEN is returned high.

TRIGGER CONTROL SHIFT REGISTERS

The trigger control shift registers consist of a serial string of 48 bits which are loaded from FD7 of the filtered data bus on a rising edge of select line $\overline{\text{WRTL}}$. The TTL outputs of the registers are level shifted down to ECL levels by resistive-divider networks and sent on to the Boolean Logic and Edge Detectors. The output of the register string is buffered and sent back to the A8 MPU Board as a test bit for self test and extended diagnostics.

9 CPU

The 7A42 contains two separate data bus structures; an internal bus, and an external bus. The internal bus is located completely on the A8 MPU Board, and is the main data bus for the 8085A microprocessor. The external bus is used by the rest of the 7A42 and is accessed as a block of memory-mapped I/O ports. The data buses are separated in this way to minimize noise propagation through the instrument by isolating the bulk of the data I/O (i.e., RAM and ROM access) to the A8 MPU Board. This data 'traffic' is blocked from the rest of the instrument by the External Bus Buffers. The external bus also provides fault isolation so that the MPU can still run diagnostic routines if there is a fault on the external bus.

DIAGNOSTIC CONTROL

The diagnostic control circuit determines the operating mode of the 7A42; diagnostic mode (for signature analysis), or normal operation. In normal operation, the jumper selects the readout mode.

The Mode selector jumper (P540) should be in the Norm position when the 7A42 is used with any 7000-series mainframe except the 7854. If the 7A42 is being used in a 7854 mainframe, the jumper should be in the 7854 position due to the particular readout requirements of the 7854.

The other three positions of the jumper are for diagnostics purposes only; their use is described in the Maintenance section of this manual.

MPU

The 7A42 uses an 8085A microprocessor to control the low-frequency functions of the instrument (e.g., attenuator control, readout, etc.). A detailed description of the functions and command set of the 8085A microprocessor is beyond the scope, and intent, of this manual. Please refer to the appropriate data books for detailed information.

On power up, R531 and C337 hold the $\overline{\text{RESET IN}}$ input of U305 low until the power supplies have stabilized. Diode CR530 discharges C337 quickly when the $\overline{\text{RESET IN}}$ line is pulled low by the Auto Restart circuit, or in case of momentary power failure.

ADDRESS LATCH

The address latch de-multiplexes the lower eight bits of the address information from the address/data lines of the 8085A. The information on the address/data lines is latched and transferred to the lower eight address lines by the ALE signal from the 8085A.

ROM DECODER

The ROM Decoder generates the chip-select signals for the ROMs.

ROM

The ROM consists of three 8k-byte EPROMs and a socket for an additional 4k-byte EPROM (for future expansion).

RAM

The two RAM ICs provide 1k-byte of static read-write memory. This memory has an associated battery backup circuit to maintain it's contents when the mainframe power is off.

BATTERY BACKUP

This circuit ensures that valid data is maintained in the RAM by disabling the chip-select signal to the RAM chips as soon as a power-down condition is detected, and providing power from the rechargable battery to the RAM until normal power is restored.

A fully charged battery will provide back-up power to the RAM for at least 200 hrs.

EXTERNAL BUS BUFFERS

The external bus buffers provide a data path between the internal and external data buses. Latch U300 allows data on the internal bus to be transferred to the external

bus, and latch U320 transfers the data on the external bus to the internal bus. When the external bus is not being addressed, the output of U320 is disabled (three-state output) and U300 latches the external-bus data on it's output to reduce the number of transitions on the external data bus. Latch U300 also provides the extra current drive required by the additional load on the external bus.

ADDRESS DECODER

This circuit produces various enable signals based on the addresses and control signals generated by the MPU.

I/O

The I/O circuit is an eight-bit latch which holds control signals for use during the diagnostic routines.

POWER-UP RELAY DRIVE DISABLE

The output of U900A ($\overline{\text{RELN}}$) is set high on power-up or reset to disable the armature relay drives until the MPU and relay drive signals have been initialized.

AUTO RESTART

This circuit causes a hardware auto reset to the microprocessor whenever it detects that Real Time Interrupts are not being serviced in a regular manner. This should occur only when there are hardware or firmware problems in the kernel.

Refer to Figure 2-3 during the following discussion.

During normal operation, Real Time Interrupts are generated when the rising edge of astable multivibrator A8 U815 clocks D flip flop A8 U900. Shortly after the RST 5.5 interrupt is recognized by the processor, the Interrupt Acknowledge line is pulsed low to reset the flip flop.

Gates A8 U927A and U927B are cross coupled to form a set-reset flip flop. Because the output duty factor of U815 is 50%, the outputs of the set-reset flip flop will also be 50% data factor. Components R924, R925, C1000, and C1005 take the average value of the Q and Q outputs which are then diode OR-ed, and presented to the comparator. With the $\overline{\text{ARST}}$ link-plug removed (auto restart circuit enabled), the noninverting input rests about 0.7 volts above the inverting input, so that $\overline{\text{RESET IN}}$ is high, and RESET OUT is low.

If a failure or temporary fault occurs, Interrupt Acknowledge will no longer match the frequency of the astable. It may be locked low, or locked high, or occur too frequently, but in any case, the average value of either the Q or Q output of the set-reset flip flop will begin to rise. When the V- input becomes greater than the reference voltage on the V+ input, the open collector output of the comparator will pull low to −15 volts, and cause the processor to be reset.

The RESET OUT signal is fed back to the inverting input of the comparator through R1002 (for hysteresis) to ensure stable operation.

With RESET OUT high, C1005 eventually charges to a voltage greater than the V- comparator input, and $\overline{\text{RESET IN}}$ returns to a high level.

If the fault persists, the above sequence repeats, and will continue to cycle at about a 2 Hz rate until the fault is removed.

WAITSTATE GENERATOR

The waitstate generator provides a low pulse of one CLK period (approximately 0.5 μS) duration on the READY line to the MPU. This circuit is enabled (by U630, pin 11) only when the filtered data bus is addressed.

REAL TIME CLOCK

Timer U815 is wired as an astable multivibrator with a period of approximately 15 ms. The output of U815 clocks D flip flop U900B to produce the RST 5.5 signal to the MPU.

GENERAL INPUT LATCH

Latch U605 provides a means to latch signals from other circuits, and transfer them to the external data bus for inspection by the MPU.

PROBE OFFSET ACQUISITION

During probe offset acquisition, an analog-to-digital conversion of the TIP voltage is performed by the processor using successive approximation. See Figure 2-4. The processor makes a first guess at the TIP voltage by setting the output of D/A converter (U600) to it's midrange value. This is done by setting the MSB of the DAC equal to 1, and all other data bits to 0. Whether the guess is too high or too low is determined by comparator U505A, and the outcome is read by the processor on data bit 4 of the General Input Latch (U605). If the D/A output is too high, the MSB (bit 7) of the DAC is reset to 0; if it was too low, it will remain set.

Next, bit 6 is set high, with all lower-order bits remaining low, and the comparison is again checked by the processor. Bit 6 will remain set, or be reset, according to the same criteria as above.

This continues for the remaining bits, and after 8 iterations, the processor will have the 8-bit digital representation of the TIP voltage.

The usable input range at the TIP jack is ±5 volts, which is attenuated to approximately ±3.75 volts at the comparator by a resistive divider.

The output range of the DAC is 0 to 10 volts. This is level shifted and attenuated to give a range of approximately ±3.75 volts at the comparator.

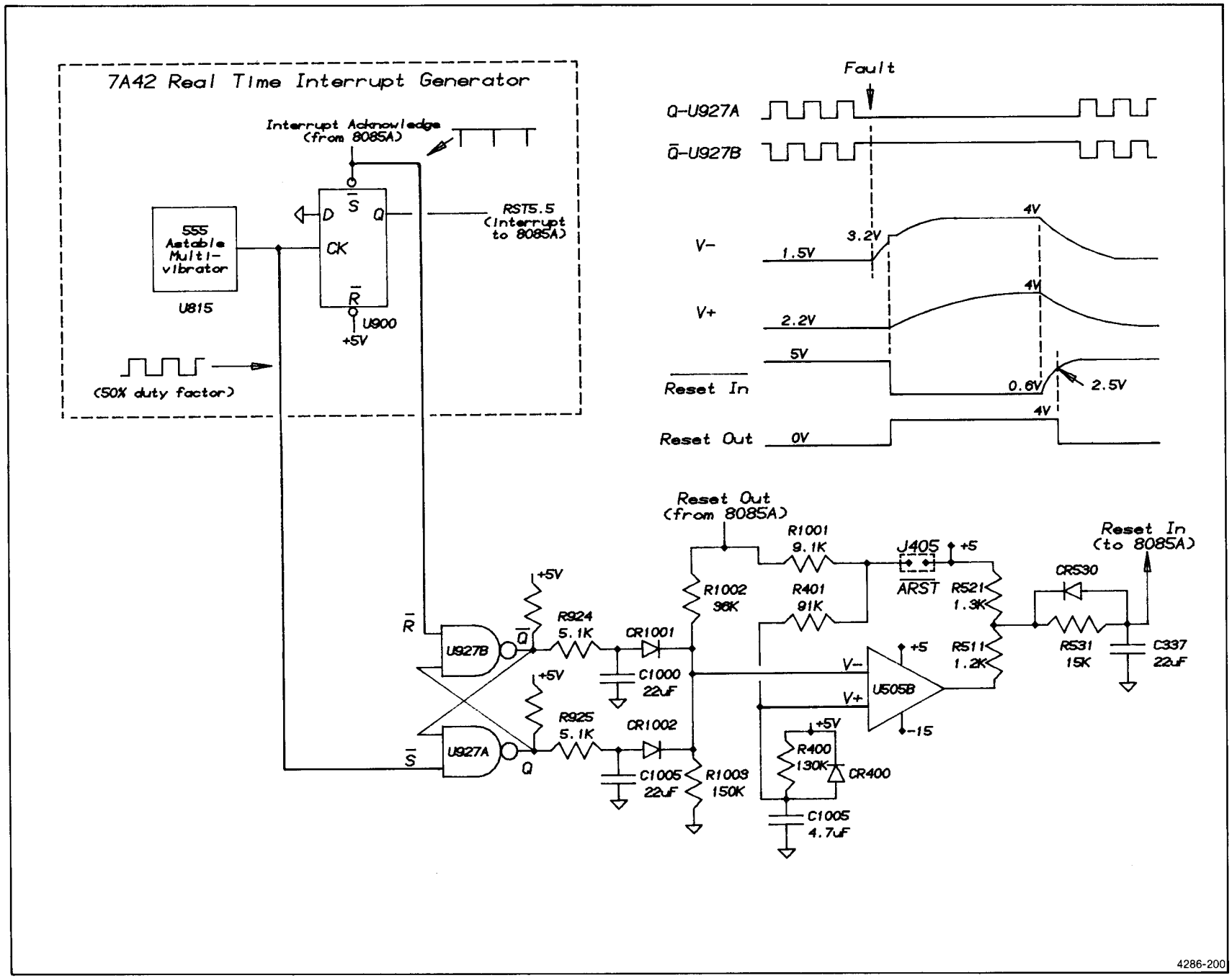


Figure 2-3. Partial A8; Auto Restart Circuit.

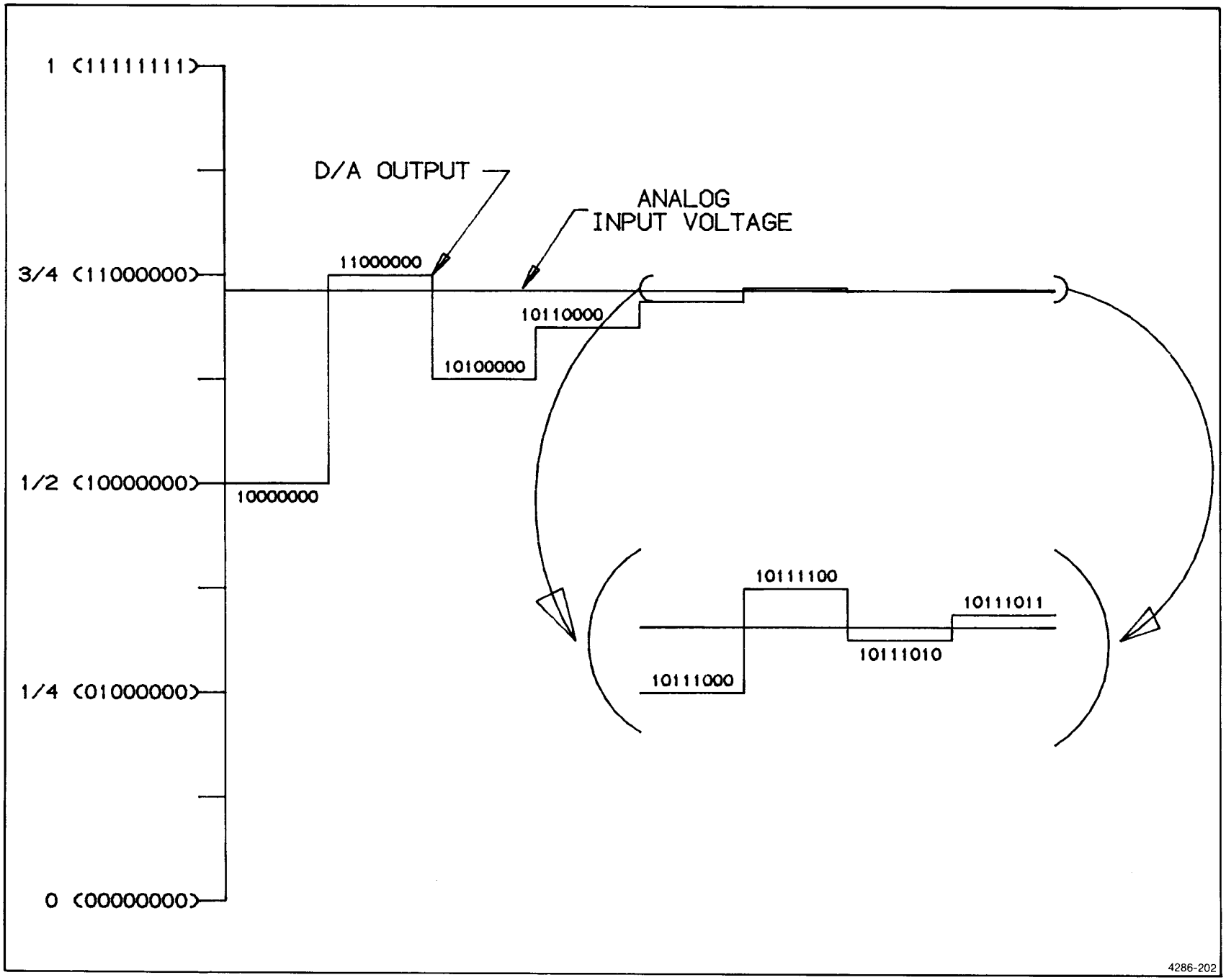


Figure 2-4. Successive Approximation Example.

Diodes CR505 and CR508 protect the comparator against over voltage. Zener diode VR510 shifts the comparator output to TTL levels.

PROBE CODING AND DIAGNOSTIC HOOKS MUX

Multiplexer U700 selects one of eight input signals to be connected to pin 13 of U605 (General Input Latch).

DIAGNOSTIC HOOKS

Quad op-amp U800 acts as a low-speed ECL-to-TTL signal translator while the diagnostic routines are running.

10 READOUT

This discussion assumes an understanding of the 7000-series readout system. Refer to a suitable mainframe service manual for background information.

The 7A42 uses the CH1 and CH2 mainframe readout positions associated with the left side of the plug-in to display vertical deflection information and error messages.

Figure 2-5 shows a timing diagram of the 7A42 readout signals.

The CH1 and CH2 readout circuitry are identical; only CH1 will be discussed here. TSX is the result of diode OR-ing the ten timeslot lines together on the A5 Amplifier board. With each falling timeslot edge, a 1.5 μs pulse (RST 7.5) is produced at the output of U830A.

The rising edge of RST 7.5 interrupts the processor, and a short time later data for the next timeslot is written to data registers U601, U600, U401, and U400. As an example, the RST 7.5 at the beginning of timeslot 9 signifies to the processor the time has come to write timeslot 10 data. This scheme of writing the next timeslots data instead of the current timeslot's data is necessary because of the high rate at which timeslots occur, relative to processor speed.

Timeslot 1 is transformed into TTL levels by Q720C and wired to the SID (Serial Input Data) input of the processor where it is used for synchronization. It is also used as an address line to the registers, and to synchronize the WA1, RA1 flip-flop.

With the exception of timeslot 1, data is always alternately written to and read from locations 0 and 1 of the registers (WA2 and RA2 = 0). Addressing is performed by D flip-flop U630 which is wired so that RA1 and WA1 will always be 180 degrees out of phase.

A complication arises when a "jump" is issued either by the mainframe or by another plug-in unit. Rather than timeslots occurring in an orderly manner, timeslot 1 may repeated up to 4 times, if three consecutive jumps occur. The 7A42 accommodates this in the following way.

During timeslot 10, the processor writes timeslot 1's data into location 2 of the registers by lifting WA2 via latch U500. With RA2 wired to SID, anytime timeslot 1 occurs, data will be read from register location 2.

The processor keeps a history of the SID line so that new timeslot data (timeslot 2 data) is written only on the first occurrence of timeslot 1 (i.e., it checks for a low SID line before writing timeslot 3 data).

Digital to Analog converters present the analog row and column currents to the mainframe.

11 POWER SUPPLY AND DISTRIBUTION

The 7A42 uses a switching power supply to develop output voltages of +5 volts, -2 volts, and -5 volts from the mainframe ±50-volt supplies. This type of power supply is used because of it's compactness and high efficiency.

POWER STAGE

This section is composed of the flyback transformer T1, and the Darlington switch (Q402 and Q500).

For high efficiency, the transistor combination must exhibit low storage time, low current rise and fall time, and low saturation voltage.

At turn-on time, Q402 saturates, Q500 is held at the edge of saturation, and approximately 100 volts is applied to the primary of T1. Current ramps-up at a rate determined by the applied voltage and the transformer primary inductance, which is about 2 mh. Switch closure duration is typically 20 μs, giving a peak current of 1 ampere.

When the switch is opened, the collector current falls and the collector voltage rises according to the transformer leakage inductance and the snubbing network. The final value of the voltage on the primary side of the transformer is the output voltage reflected through the transformer by the turns ratio.

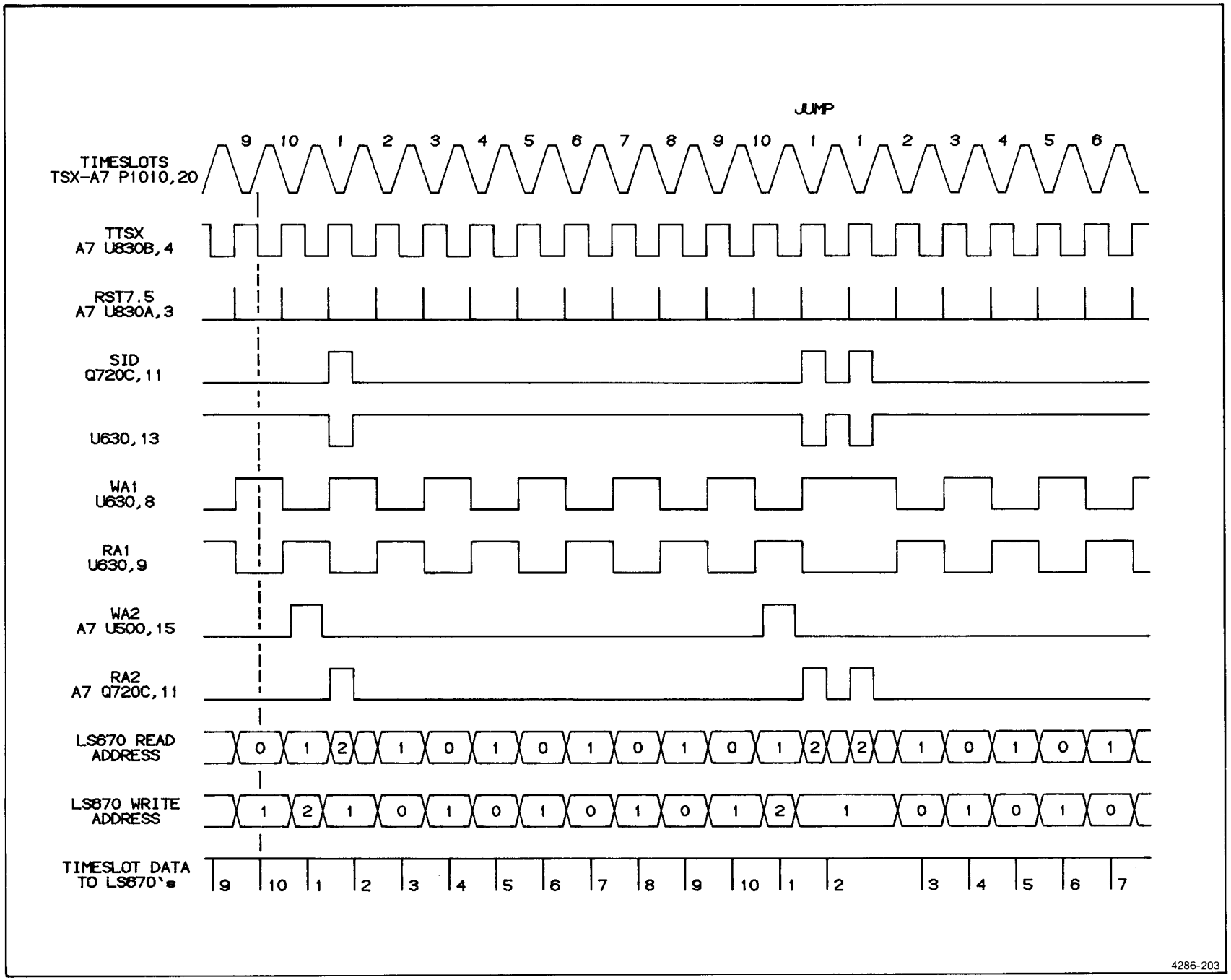


Figure 2-5. 7A42 Readout Timing.

Resistors R405 and R401 discharge the base storage capacitance of Q402 and Q500 to reduce turn-off time.

RECTIFIERS AND FILTERS

Diodes CR410, CR520, and CR620 are used to rectify the square-wave output. Schottky diodes are used here because of their low forward-voltage drop and low storage time.

The output pi filters reduce the ac component of the rectifier output voltage and reduce supply output impedance at higher frequencies where regulator loop gain begins to fall.

Special consideration is given to the selection of C410, C530, and C630 regarding equivalent series resistance (ESR). Peak current values of 1 to 5 amperes are typical and without low values of ESR, excessive heating will occur.

CURRENT LIMIT

The current limit circuit senses excess primary current. When a fault is detected, it clamps the PWM comparator input to ground, causing the supply to shut down for about 100 ms. It then releases the comparator and allows the supply to attempt to recover. With a short circuit on the secondary side, the Current Limit will cycle at about 10 Hz.

Current limiting occurs when the primary current through R410 exceeds about 1.2 amperes. Transistors Q100 and Q200 are turned on by Q313 and Q317 when the maximum primary current is exceeded. When Q100 turns on, Q300 also turns on, pulling the base of Q100 high. This keeps Q200 saturated, and the supply down, while C200 charges.

INPUT FILTER

Because the transformer primary current is discontinuous and contains some high-amplitude, high-frequency harmonics, the ±50-volt mainframe power supplies are decoupled from the 7A42 switcher by C220, C330, C325, and L220.

Due to the highly capacitive load on the ±50-volt supplies, surge current may cause the mainframe power supply to current limit when the instrument is turned on initially. Diode CR230 keeps C220 from discharging between attempts to start the mainframe power supply.

PULSE WIDTH MODULATION (PWM) CONTROLLER

The primary function of the PWM integrated circuit is to monitor the -5 volt output and adjust the duty cycle of the power stage so that the secondary output voltages are maintained at constant values under varying load conditions.

The -5 volt output is level shifted through R119, R122, and R125 to +2.5 volts and presented to the noninverting input of the error amplifier where it is compared to the +2.5 volt reference level. The reference is determined by the +5 volt reference from the PWM IC and the 2X divider R120 and R121. The output of the error amplifier is compared to the 20 kHz free-running oscillator output which is a ramp whose frequency is set by R218 and C105. It is the output of this comparator which determines the duty cycle of the power stage. Under normal operating conditions, the duty cycle is about 38 percent. (The Darlington switch is ON about 38% of the time, and OFF about 62% of the time.)

Stability of the regulator is ensured by R109 and C108 at the error-amplifier output.

Components R105, C115, CR110, and CR111 are used to "soft start" the switcher when mainframe power is initially applied. This prevents excessively high current in the power stage.

When power is initially applied to the 7A42 through it's host mainframe, C115 is fully discharged and the output of the error amplifier is clamped to ground through CR110, thus disabling the regulator. As C115 is charged through R105, the duty cycle slowly increases until it reaches it's steady state value. The capacitor is charged to a final value of +5 volts and under normal operation is disconnected from the error-amplifier output by CR110. In the event that mainframe power momentarily drops, or cycles, CR111 quickly discharges C115 to ensure soft start when power returns.

DRIVERS

These three transistors provide the necessary current drive during ON and OFF times to control the power stage.

At turn-on, the PWM output transistor saturates, resulting in C2 (pin 13 of U210) and E2 (pin 14 of U210) being at about 3 volts. Transistor Q315, in a common base configuration, supplies about 15 ma of base drive to Q402 throughout ON time. Additional current drive is provided by Q305 through C301 to quickly turn the Darlington on. Resistor R301 discharges C301 to 0 volts during the OFF time.

Previous to the turn-off signal from pin 13 of U210, Q312 is off, and it's collector is biased to approximately -42 volts by divider R225, R226. Capacitor C122 is charged to about 7 volts through CR406 and CR407. When turn-off occurs, Q312 saturates and the base of Q402 is pulled to about -55 volts through the capacitor. This causes the stored charge in the base of Q402 to be removed quickly, decreasing the total turn-off time. The capacitor is tied to the base of Q402 through CR121, which prevents the divider from turning the Darlington on during the OFF time.

SNUBBER

Because the transformer is non-ideal and contains leakage inductance, some means to protect the Darlington pair, Q402 and Q500, against avalanche and secondary breakdown is needed. The reactive snubber is used to limit the flyback voltage to prevent breakdown, and to shape the switch's load line during current fall time to minimize it's power dissipation.

First, assume Q402 and Q500 are saturated and receive a turn-off signal at the base of Q402. A storage-time delay later, the collector current begins to decrease and the current in C405 begins to increase an equal amount. Over this time frame, the transformer's primary current remains approximately constant. As the collector of the Darlington rises to a peak value of approximately 150 volts, C405 is charged to about 100 volts and remains at that value until turn-on time. Note that during the time C405 is charging, not only does the snubber control the manner in which the collector voltage rises, but also, a portion of the energy stored in the transformer's leakage inductance, which would otherwise be lost, is returned to the +50V supply.

At the switch's turn-on time, C405 and L310 are paralleled through Q500 and the voltage at the cathode of CR402 is −150 volts. This voltage rises to a peak value of nearly +50 volts when the current through L310 and C405 attempts to reverse, but is blocked by CR402. During this portion of the cycle, the voltage on C405 is always restored to a value of something less than 100 volts.

Notice that, had the voltage stored on C405 during flyback been greater than 100 volts (at the switch turn-on time), the LC tank would have tried to ring higher than +50 volts but would be clamped by CR400.

ATTENUATOR SUPPLIES

Operational amplifiers U300 and U310 form an individual set of −5 and −11 volt power supplies for each of the four attenuator modules. The supplies are separate from each other to help minimize crosstalk, and to provide individual offset adjustment as needed.

The −5 volt supply is generated at the output of an operational amplifier with a gain of −1, by using +5 volts as a reference. The −11 volt supply is adjustable to compensate for any variations in the +5 volt and −5 volt supplies. This is done to prevent drift in the attenuator impedance converter, caused by power-supply variations. Since all the supplies track each other, drift from this source is reduced.

MAINTENANCE

This section contains information for performing preventive maintenance, troubleshooting, corrective maintenance, and testing and diagnostics for the 7A42 Logic Triggered Vertical Amplifier. All support-related items mentioned in this manual are listed in Table 3-1.

PREVENTIVE MAINTENANCE

Preventive maintenance performed regularly can prevent or forestall instrument breakdown and may improve instrument reliability. The severity of the environment to which the instrument is subjected determines the frequency of maintenance. A convenient time to perform preventive maintenance is before electrical adjustment of the instrument.

PLUG-IN PANEL REMOVAL

WARNING

Dangerous voltages (about 250 V peak) are present at several points on the Power Supply Board. When the 7A42 is operated with its covers removed, do not touch exposed connections or parts. Some transistors have voltages present on their cases. Disconnect the 7A42 from its power source before cleaning or replacing parts.

The side panels, top-and-bottom frame rails, and front panel reduce radiation of electromagnetic interference from the instrument. The side panels are held in place by grooves in the frame rails. To remove a panel, pry out with the fingers, beginning at the rear of the appropriate side cover. To install a cover, position it over the frame rail grooves, then press down with the fingers until the cover snaps into place. Pressure must be exerted along the full length of the rails to secure the panel.

NOTE

The 7A42 will not slide into the mainframe if the side panels are not fully seated in the rails.

CLEANING

The 7A42 should be cleaned as often as operating conditions require. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation, which can cause overheating and component breakdown. Dirt also provides an electrical conduction path that can result in instrument failure.

NOTE

The cabinet panels of the mainframe in which the 7A42 is installed reduce the amount of dust reaching the interior of the instrument. Operation without the panels in place necessitates more frequent cleaning.

CAUTION

Avoid the use of chemical cleaning agents which might damage the materials used in this instrument. Use only Isopropyl alcohol or totally denatured ethyl alcohol. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

EXTERIOR

Loose dust accumulated on the outside of the instrument can be removed with a soft cloth or small brush. The brush is particularly useful for dislodging dirt in and around the side-panel ventilation holes and front-panel switches.

NOTE

Remove the side panels before cleaning them.

INTERIOR

Cleaning the interior of the instrument should be necessary only occasionally. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air (approximately 5 lb/in^2). Remove any dirt that remains with a soft brush or a cloth dampened with a mild solution of detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces, or for cleaning more delicate circuit components.

TABLE 3-1
Part Number Reference For Support Items

Purpose	Item	Quantity Required	Location
Standard Accessories	Operators Manual	1	Section 1—General Information "STANDARD ACCESSORIES"
	Service Manual	1	
Discharge Static Voltage to Prevent Damage of Static-Sensitive Components	Static Control Mat, Tektronix Part 006-3414-00.	1	Section 3—Maintenance "STATIC-SENSITIVE DEVICE CLASSIFICATION"
	Wrist strap, Tektronix Part 006-3415-00.	1	
Test Equipment for General Troubleshooting	TEKTRONIX 7704A Oscilloscope with 7A26 Dual Trace Amplifier and 7B80 Time Base, or equivalent	1	"TROUBLESHOOTING EQUIPMENT"
	TEKTRONIX 577/177 Curve Tracer. TEKTRONIX 576 Curve Tracer. TEKTRONIX 7CT1N Curve Tracer Plug-in unit and a 7000-series oscilloscope. TEKTRONIX 5CT1N Curve Tracer Plug-in unit and a 5000-series oscilloscope.	1	
	TEKTRONIX DM501A Digital Multimeter	1	
	TEKTRONIX 067-1112-00 7A42 Service Kit. Includes: 1 Extender board 670-7334-00. 4 Extender cables, three-conductor, 9-inch, 175-1754-00. 3 Extender cables, three-conductor, 15-inch, 175-2904-00. 1 Extender cable, 20-conductor, 175-7373-00. 4 Terminations, 200 Ω, 317-0201-03. 7A42 Signature Analysis TTL-to-ECL Level Converter, 670-8210-00.	1	
	TEKTRONIX 067-0616-00 Flexible extender.	2	
	TEKTRONIX 067-1090-00 Signature Analyzer. SONY/TEKTRONIX 308 Data Analyzer	1	

TABLE 3-1 (CONT)
Part Number Reference For Support Items

Purpose	Item		Quantity Required	Location
Integrated Circuit Extracting Tool	Tektronix Part 003-0619-00.		1	REMOVING AND REPLACING PARTS, AND REPLACEMENT"
Sockets for Integrated Circuits	Number of Pins	Tektronix Part Number		
	8	136-0727-00		
	14	136-0728-00		
	16	136-0729-00		
	20	136-0752-00		
Circuit Board Removal Tools	Philips screwdriver, #1		1	REMOVING AND REPLACING PARTS, CIRCUIT BOARDS
	Philips screwdriver, #2		1	
	Torx screwdriver, #10		1	
	Vacuum desoldering equipment, Pace PPS-4A or equivalent.		1	
	Soldering iron, 15 W		1	
	Alcohol & fine-bristle brush		1	
	Hex-key wrench, 3-32-inch		1	
	Needle-nose pliers.		1	
	Nutdriver, 3/16-inch		1	
	Small straight-slot screwdriver.		1	
	Torque wrench, 0-10 inch-pound range		1	
	Spacer post, 4-40 internal thread, 3/16-inch hexagonal stock		1	
Replacement Kit for Circuit-Board Pins	Tektronix Part 040-0542-00.		1	REMOVING AND REPLACING PARTS
Pressure Pad	Tektronix Part 348-0759-00.		1	REMOVING AND REPLACING PARTS ARMATURE RELAYS
Test Equipment for Checks and Adjustment Procedures	Refer to Table 4-2, Test Equipment.			Section 4—Checks and Adjustment "TABLE 4-2, TEST EQUIPMENT"

CAUTION

Circuit boards and components must be dry before applying power to prevent damage from electrical shorts.

LUBRICATION

Generally, there are no parts in this instrument that require a regular lubrication program during the life of the instrument.

VISUAL INSPECTION

The 7A42 should be inspected occasionally for loosely seated semiconductors or heat-damaged parts. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged parts are found. Overheating usually indicates other trouble in the instrument; therefore, correcting the cause of overheating is important to prevent recurrence of the damage.

SEMICONDUCTOR CHECKS

Periodic checks of semiconductors are not recommended. The best check of semiconductor performance is actual operation in the instrument. More details on semiconductors are given under Troubleshooting later in this section.

ELECTRICAL ADJUSTMENT

To ensure accurate measurements, check the electrical adjustment of this instrument after each 2000 hours of operation, or annually if used infrequently. In addition, replacement of components may necessitate adjustment of the affected circuits. Complete adjustment instructions are given in Section 4, Checks and Adjustment. This procedure can be helpful in localizing certain troubles in the instrument, and in some cases, may correct them.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of other closely related circuits. The Performance Check procedure in Section 4, Checks and Adjustment, provides a quick and convenient means of checking instrument operation. In some cases, minor troubles may be revealed or corrected by adjustment. Also see Table 3-4 after replacing any parts on the A6-Trigger Board. (Table 3-4 is located in the Integrated Circuit part of 7. CHECK INDIVIDUAL COMPONENTS, in this section.)

TROUBLESHOOTING

The following information is provided to facilitate troubleshooting of the 7A42 Logic Triggered Vertical Amplifier. Information contained in other sections of this manual should be used in conjunction with the following data to aid in locating a defective component. An understanding of the circuit operation is helpful in locating troubles. See Section 2, Theory of Operation, for this information.

TROUBLESHOOTING AIDS

WARNING

Dangerous voltages (about 250 V peak) are present at several points on the A9. Power Supply Board. When the 7A42 is operated with its covers removed, do not touch exposed connections or parts. The power transistor has voltage present on its case. Disconnect the 7A42 from its power source before cleaning or replacing parts.

DIAGRAMS

Complete schematic diagrams are given on the pullout pages in Section 7, Diagrams and Circuit Board Illustrations. The component circuit number and electrical value of each component in the 7A42 are shown on these diagrams. (See the first page of the Diagrams and Circuit Board Illustrations section for definitions of the reference designators and symbols used to identify components in the 7A42.) Important voltages and numbered waveform test points are also shown on the diagrams. Important waveforms, and numbered test points where they were obtained, are located adjacent to or preceding some diagrams. The portions of circuits mounted on circuit boards are enclosed with heavy, solid-black lines.

CIRCUIT BOARD ILLUSTRATIONS

To aid in locating circuit boards, an illustration showing the circuit board location appears on the back of the foldout page facing the schematic diagram. An illustration of the circuit board(s) is also included here to identify the physical location of components and

waveform test points that appear on the respective schematic diagram. Each circuit board illustration and diagram is arranged in a grid locator with an index to facilitate rapid location of components contained in the corresponding schematic diagram.

COMPONENT COLOR CODING

This instrument contains composition resistors, metal-film resistors, and wire-wound resistors. The resistance values of wire-wound resistors are usually printed on the component body. The resistance values of composition resistors and metal-film resistors are color coded on the components, using the EIA color code (some metal-film resistors may have the value printed on the body). The color code is read starting with the stripe nearest the end of the resistor. Composition resistors have four stripes, which consist of two significant figures, a multiplier, and a tolerance value (see Fig. 3-1).

Metal-film resistors have five stripes consisting of three significant figures, a multiplier, and a tolerance value.

The values of common disc capacitors and small electrolytics are marked on the side of the component body.

The cathode end of glass-encased diodes is indicated by a stripe, a series of stripes, or a dot. The cathode and anode ends of metal-encased diodes can be identified by the diode symbol marked on the body.

WIRING COLOR CODE

Most internal wiring is done with multi-conductor ribbon cables. These ribbon cables are gray with a colored stripe on the number 1 conductor, which goes to pin 1 on the associated connector.

Some wiring is done with multi-conductor ribbon cables with differently colored conductors. The colors of these cables follow the EIA color code, and the brown conductor should connect to pin 1 of the associated connector.

Three coaxial cables connect the A6 Trigger Board to the RESET, EXT CLOCK INPUT, and TRIGGER OUT connectors on the front panel. Table 3-2 lists the color codes of the coaxial cables.

TABLE 3-2
Color Codes of Coaxial Cables

Front Panel Connector	Color Code of Cable	A6 Trigger Board Connector
J47	blue on white	J632
J49	red on white	J602
J710 (on LED Board)	green on white	J700

SEMICONDUCTOR LEAD CONFIGURATIONS

Lead configurations and index locators for semiconductor devices used in the 7A42 are shown in Figure 3-2.

STATIC-SENSITIVE DEVICE CLASSIFICATION

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 3-3 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

TABLE 3-3
Relative Susceptibility to Damage from Static Discharge

Semiconductor Classes	Relative Susceptibility Levels[1]
MOS or CMOS microcircuits, and discrete or linear microcircuits with MOS inputs (most sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear Microcircuits	7
Low-power Schottky TTL	8
TTL (least sensitive)	9

[1]**Voltage equivalent for levels.**

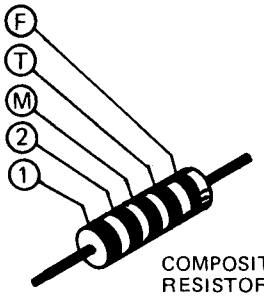
1 = 100 to 500 V
2 = 200 to 500 V
3 = 250 V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V (est.)
8 = 900 V
9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 ohms).

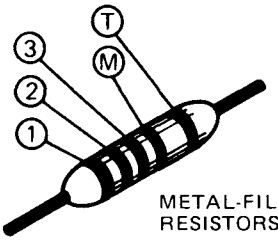
Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers on a metal rail, or conductive foam. Label any package that contains static-sensitive assemblies or components.

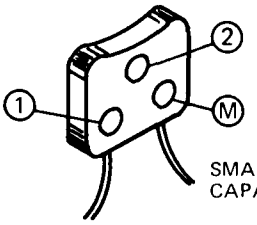
COLOR CODE



COMPOSITION RESISTORS



METAL-FILM RESISTORS



SMALL DISC CAPACITORS

(1) (2) and (3) - 1ST, 2ND, AND 3RD SIGNIFICANT FIGS.

(M) - MULTIPLIER

(T) - TOLERANCE

(F) - FAILURE RATE LEVEL

COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS		
		MULTIPLIER (OHMS)	TOLERANCE	MULTIPLIER (pF)	TOLERANCE	
					OVER 10pF	UNDER 10pF
BLACK	0	1	---	1	±20%	± 2pF
BROWN	1	10	±1%	10	±1%	±0.1pF
RED	2	10^2 or 100	±2%	10^2or 100	±2%	---
ORANGE	3	10^3or 1 K	±3%	10^3 or 1000	±3%	---
YELLOW	4	10^4 or 10K	±4%	10^4 or 10,000	+100% −0%	---
GREEN	5	10^5 or 100 K	±1/2%	10^5or 100,000	±5%	±0.5pF
BLUE	6	10^6 or 1 M	±1/4%	10^6 or 1,000,000	---	---
VIOLET	7	---	±1/10%	10^7 or 10,000,000	---	---
GRAY	8	---	---	10^{-2} or 0.01	+80% −20%	±0.25pF
WHITE	9	---	---	10^{-1} or 0.1	±10%	±1pF
GOLD	---	10^{-1} or 0.1	±5%	---	---	---
SILVER	---	10^{-2} or 0.01	±10%	---	---	---
NONE	---	---	±20%	---	±10%	±1pF

4286-301

Figure 3-1. Color code for resistors and capacitors.

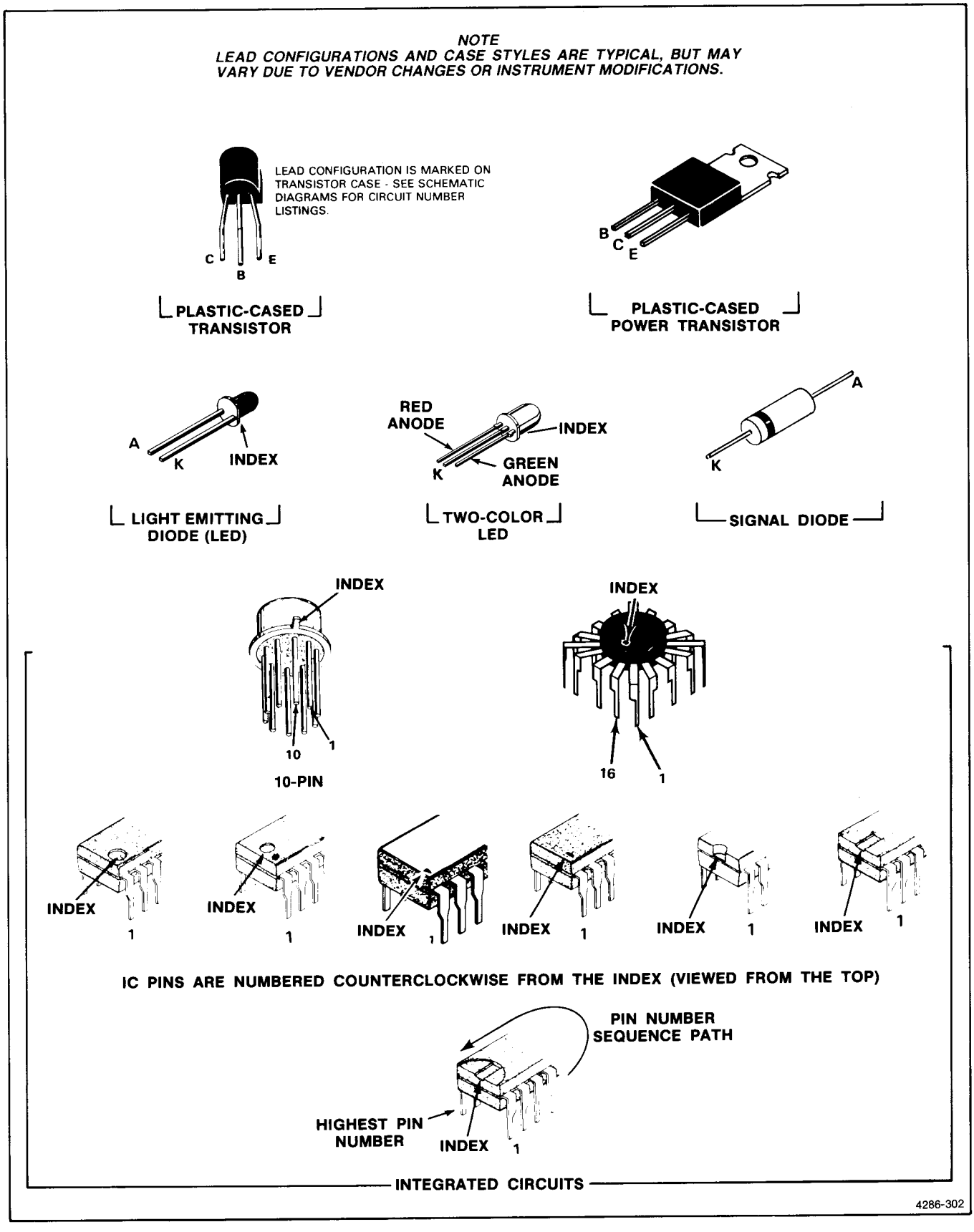


Figure 3-2. Semiconductor lead configuration.

3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static free work station by qualified service personnel. We recommend use of the Static Control Mat, Tektronix Part 006-3414-00, and Wrist Strap, Tektronix Part 006-3415-00.

4. Allow nothing capable of generating or holding a static charge on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only special antistatic suction type desoldering tools.

MULTI-PIN CONNECTOR IDENTIFICATION

A triangle on the holder identifies pin 1 of multi-pin connector holders. When connecting the holder to its row of pins on the circuit board, orient the holder to align its triangle with the triangle on the circuit board (see Fig. 3-3).

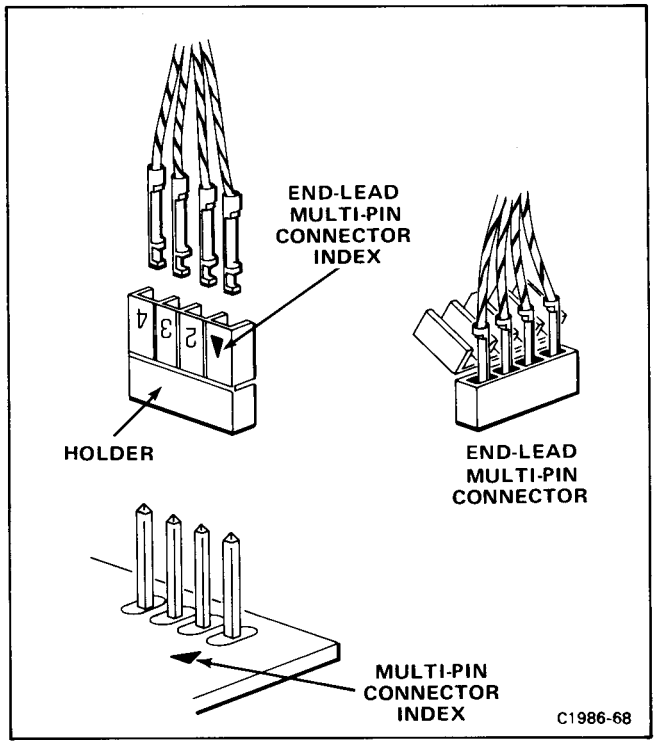


Figure 3-3. Orientation of multi-pin connectors.

TROUBLESHOOTING EQUIPMENT

The following equipment is useful for troubleshooting the 7A42 Logic Triggered Vertical Amplifier:

1. Transistor Tester

   Description: Dynamic-type tester.

   Purpose: Test semiconductors.

   Recommended type: TEKTRONIX 577/177 Curve Tracer, TEKTRONIX 576 Curve Tracer, 7CT1N Curve Tracer plug-in unit and a 7000-series oscilloscope system, or a 5CT1N Curve Tracer plug-in unit and a 5000-series oscilloscope system.

2. Digital Multimeter

   Description: 10 megohm input impedance and 0 to 1 kilovolt range, ac and dc; ohmmeter, accuracy, within 0.1%. Test probes must be insulated to prevent accidental shorting.

   Purpose: Check voltages and resistances.

   Recommended type: TEKTRONIX DM501A Digital Multimeter.

3. Test Oscilloscope

   Description: Frequency response, dc to 150 megahertz minimum; deflection factor, 10 millivolts to 5 volts/division. A 10X, 10-megohm voltage probe should be used to reduce circuit loading for voltage measurements.

   Purpose: Check operating waveforms.

   Recommended type: TEKTRONIX 7704A Oscilloscope with 7A26 Dual-Trace Amplifier and 7B80 Time Base, or equivalent.

4. Calibration Fixtures

   (A) Extender Set

   Purpose: Troubleshooting the circuit boards.

   Recommended type: Tektronix 067-1112-00 7A42 Service Kit.

(B) Extender Set (plug-in)

Purpose: Troubleshooting with 7A42 extended.

Recommended type: Tektronix 067-0616-00. (two required).

(C) Signature Analyzer

Description: Start/Stop gating inputs, four-digit hexadecimal readout, logic level indicator. TTL and ECL logic capability.

Purpose: Troubleshooting digital circuits.

Recommended types:

a. Tektronix 067-1090-00 Signature Analyzer.

b. Sony/Tektronix 308 Data Analyzer

TROUBLESHOOTING TECHNIQUES

This troubleshooting procedure is arranged to check the simple trouble possibilities before proceeding with extensive troubleshooting. The first few checks ensure proper connection and operation of associated equipment. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located, replace it using the replacement procedures given under Corrective Maintenance.

1. CHECK CONTROL SETTINGS

Incorrect control settings can indicate a nonexistent trouble. If there is any question about the correct function or operation of any control on the 7A42, refer to the Operators Manual.

2. CHECK ASSOCIATED EQUIPMENT

Before proceeding with troubleshooting, check that the equipment used with this instrument is operating correctly. Also, check that the input signals are properly connected and that the interconnecting cables are not defective. Check the line-voltage source.

3. VISUAL CHECK

Visually check any part of the instrument where the trouble may be located. Many troubles can be found by visible indications such as unsoldered connections, broken wires, damaged circuits, and damaged components. Especially check that all cables are properly installed.

4. ISOLATE TROUBLE TO A CIRCUIT

To isolate the trouble to a circuit, refer to "Diagnostics and Troubleshooting," later in this section.

5. CHECK INSTRUMENT ADJUSTMENT

Check the electrical adjustment of the 7A42, or of the affected circuit if the trouble appears in one circuit. If the apparent trouble cannot be isolated to a defective component, the trouble may only be a result of maladjustment. Complete adjustment instructions are given in Section 4, Checks and Adjustment.

6. CHECK VOLTAGES

Often the defective component can be located by checking for the correct voltages in the circuit. Typical voltages are given in Section 7, Diagrams and Circuit Board Illustrations.

NOTE

Voltages given in Section 7, Diagrams and Circuit Board Illustrations, are not absolute and may vary slightly among different 7A42s. To obtain operating conditions used to take these readings, see the Voltage Conditions adjacent to the schematic diagram.

7. CHECK INDIVIDUAL COMPONENTS

The following procedures describe methods of checking individual components in the 7A42. Components that are soldered in place (excluding integrated circuits) are best checked by first disconnecting one end. This isolates the measurement from the effects of surrounding circuitry.

CAUTION

To avoid electric-shock hazard, always turn off the mainframe power switch before removing or replacing components.

Transistors

A good check of transistor operation is actual performance under operating conditions. A transistor can most effectively be checked by substituting a new component for it (or one which has been previously checked). However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic tester. Static type testers are not recommended, because they do not check operation under simulated operating conditions.

Integrated Circuits

Integrated circuits can be checked with a test oscilloscope, signature analyzer, digital tester or by direct substitution.

CAUTION

Direct substitution must not be attempted with soldered-in integrated circuits. The I.C., circuit board, or both, could be damaged due to the heat required to melt the solder from the connections. Refer to Soldering Techniques later in this section. Use care when checking voltages and waveforms around the integrated circuits so that adjacent leads are not shorted together. The integrated circuit test clip provides a convenient means of clipping a test probe to the in-line, multi-pin integrated circuits.

A good understanding of the circuit operation is essential to troubleshooting circuits using integrated circuits if a signature analyzer is not available. Operating conditions and other information for the integrated circuits are given in Section 2, Theory of Operation and Section 7, Diagrams and Circuit Board Illustrations.

When any IC on the A6 Trigger Board is replaced, it is important that the 7A42 meet all performance specifications with the new IC in the circuit. Table 3-4 is a guide to show which performance checks should be made to verify that the 7A42 meets its specifications with the new IC. Aspects of circuit performance which are not affected by the replaced IC need not be checked.

The performance checks should be made with the A6 Trigger Board installed in the 7A42, and the 7A42 installed in a mainframe. Self-test should run and pass. The trigger threshold gain and offset should be recalibrated, and amplifier gain should be properly adjusted.

Diodes

A diode can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter on a scale having a low internal source current, such as the R × 1k scale. The resistance should be very high in one direction and very low in the other direction.

CAUTION

When checking diodes, do not use an ohmmeter scale setting that has a high internal current, because high currents may damage the diodes under test.

Resistors

Check the resistors with an ohmmeter. Resistor tolerances are given in Section 6, Replaceable Electrical Parts. Normally, resistors need not be replaced unless the measured value varies widely from the specified value.

Capacitors

A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter on the highest scale. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after initial charge of the capacitor. An open capacitor can best be detected with a capacitance meter or by checking that the capacitor passes ac signals.

8. REPAIR AND ADJUST THE CIRCUIT

If any defective parts are located, follow the replacement procedures given under Component Replacement in this section. Check the performance of any circuit that has been repaired or that has had any electrical components replaced. Adjustment of the circuit may be necessary.

TABLE 3-4
What To Check After Replacing Components on The A6 Trigger Board

Component Number	Device Type	Check These Steps (see "Part II—Performance Check Procedure" in Section 4)
U1020	AD558	C2, C3, C4; CH1 only.
U1030	AD558	C2, C3, C4; CH2 only.
U1022	AD558	C2, C3, C4; CH3 only.
U1032	AD558	C2, C3, C4; CH4 only.
U200	9685	B3, C2, C4; CH1 only.
U210	9685	B3, C2, C4; CH2 only.
U220	9685	B3, C2, C4; CH3 only.
U230	9685	B3, C2, C4; CH4 only.
U300	10H104	B3, F4, F5; CH1 only, F2, F3; CH1 to CH2, to CH3, and to CH4.
U302	10H104	B3, F4, F5; CH2 only, F2, F3; CH2 to CH1, to CH3, and to CH4.
U332	10H104	B3, F4, F5; CH3 only, F2, F3; CH3 to CH1, to CH2, and to CH4.
U330	10H104	B3, F4, F5; CH4 only, F2, F3; CH4 to CH1, to CH2, and to CH3.
U400	10113	B3, F4, F5; CH1 only, F2, F3; CH1 to CH2, to CH3, and to CH4.
U410	10113	B3, F4, F5; CH2 only, F2, F3; CH2 to CH1, to CH3, and to CH4.
U420	10113	B3, F4, F5; CH3 only, F2, F3; CH3 to CH1, to CH2, and to CH4.
U430	10113	B3, F4, F5; CH4 only, F2, F3; CH4 to CH1, to CH2, and to CH3.
U500	10H104	E2
U530	10H104	E2
Q532	CA3086	E2
U402	10H102	B3, F2, F3; first product in function A only (all channels).
U412	10H102	B3, F2, F3; second product in function A only (all channels).
U422	10H102	B3, F2, F3; first product in function B only (all channels).
U432	10H102	B3, F2, F3; second product in function A only (all channels).
U310	10H164	B3, F4, F5; CH1 only, F2, F3; CH1 to CH2, to CH3, and to CH4.
U312	10H164	B3, F4, F5; CH2 only, F2, F3; CH2 to CH1, to CH3, and to CH4.
U320	10H164	B3, F4, F5; CH3 only, F2, F3; CH3 to CH1, to CH2, and to CH4.
U322	10H164	B3, F4, F5; CH4 only, F2, F3; CH4 to CH1, to CH2, and to CH3.
U510	10H102	D3, D5, D6.
U700	10104	E2, D3.
U800	10104	D3; entire procedure, F4; CH1 only.
U520	10H102	B3; CH1 only, D3; first trigger function, ECL level only, G3.
U600	10H104	B3; CH1 only, G2, G3, G5.
U610	10H104	D3; first trigger function, ECL level only, B3; CH1 only, E3, E4, G3.
U620	10H104	B3. D3; first trigger function, ECL level only, E3, E4.
U630	10173	B3, D2.
U828	74LS164	Run self test.
U912	74LS164	Run self test.
U838	74LS164	Run self test.
U818	74LS164	Run self test.
U922	74LS164	Run self test.
U932	74LS164	Run self test.
U1010	74C374	Run self test.

The transistors can also be checked with the procedures.
Q722, Q726, Q1002, Q1004, Q1010, Q1012 and Q1014 are checked by self test.

Q622, Q724	151-0220-00	D3, D4; TTL level only.
Q620, Q720	151-0220-00	H2, H5.
Q600, Q610	151-0221-00	E3, E4.

DIAGNOSTICS AND TROUBLESHOOTING

The 7A42 Logic Triggered Vertical Amplifier is designed so that if a trouble occurs, it can be quickly diagnosed with a minimum of test equipment.

The extensive internal diagnostics built into the 7A42 provide broad coverage of much of the instrument. The diagnostics have two forms, Self-Test and Extended Diagnostics. Self-Test runs automatically at power-up and reports if a functional block in the instrument has failed. Service personnel can then use the Extended Diagnostics to troubleshoot and correct the problem.

Circuits that are not covered by the internal diagnostics are described in a separate section, Troubleshooting Circuits Not Covered By Diagnostics.

If the 7A42 has no sign of life, refer to What to Do if The 7A42 Does Not Respond to Front-Panel Controls before attempting to use the Extended Diagnostics.

This part of the Maintenance Section describes the 7A42's self-contained system for diagnosing troubles. Signature tables, for use with signature analysis, are located in Volume 2 of the 7A42 Service Manual, 7A42 Signature Analysis Tables, Tektronix Part 070-4654-00.

SELF TEST

Each time the 7A42 is turned on in normal operating mode, it tests itself comprehensively with a series of 72 "self-tests." After the self-test sequence has been performed, the result will be displayed as shown in Table 3-5.

During a self-test the crt of the host oscilloscope will display 7A42 TEST BUSY. During the first part of self-test, the SWITCHING THRESHOLD VOLTS indicator will display 8.8.8.8. to test all its indicator segments. Then it will display the firmware version number (e.g., 1.00) until self-test is complete, or until a self-test fails.

When the oscilloscope crt displays 7A42 TEST COMPLETE for about one second, and no self-test failure occurs, the operator can use the 7A42 with confidence that it is operating correctly.

In order for the self-test to verify operation of the 7A42 readout circuitry, the mainframe Readout control should be set to freerun (non-Gated or non-Pulsed) mode.

EXTENDED DIAGNOSTICS

The Extended Diagnostic tests use the same test routines that Self-Test uses. However, when an Extended Diagnostic test is started it will run continuously until it is manually terminated. Extended Diagnostic tests are selected via the front panel. See Figure 3-4 for the redefined key functions in the Extended Test mode, which are valid only in the Extended Test mode. The keys defined on the right side select the calibration and troubleshooting tests. Refer to Table 3-7 for the jumper locations for Extended Test mode. (Table 3-7 is located in What to Do if The 7A42 Does Not Respond to Front-Panel Controls, under Forced Instruction Freerun, later in this section.)

To select a specific self-test for exercise, refer to Figure 3-4 and press the appropriate key. For example, if you want to exercise self-test 7, Real-Time Interrupt, press the upper VOLTS/DIV button. The 7A42 will start performing self-test 7, and the SWITCHING THRESHOLD VOLTS Indicator will display 07 in its left-most two digits. The right-most two digits will display the number of failures the test reveals.

TABLE 3-5
CRT And SWITCHING THRESHOLD VOLTS Displays

Result of Self Test	TRIGGER FUNCTION LEDs	Display On	
		Crt of Host Oscilloscope	SWITCHING THRESHOLD VOLTS
Passed	All green	7A42 TEST COMPLETE	None
Failed	Any one red	7A42 TEST BUSY with failure code	Number of test which found trouble

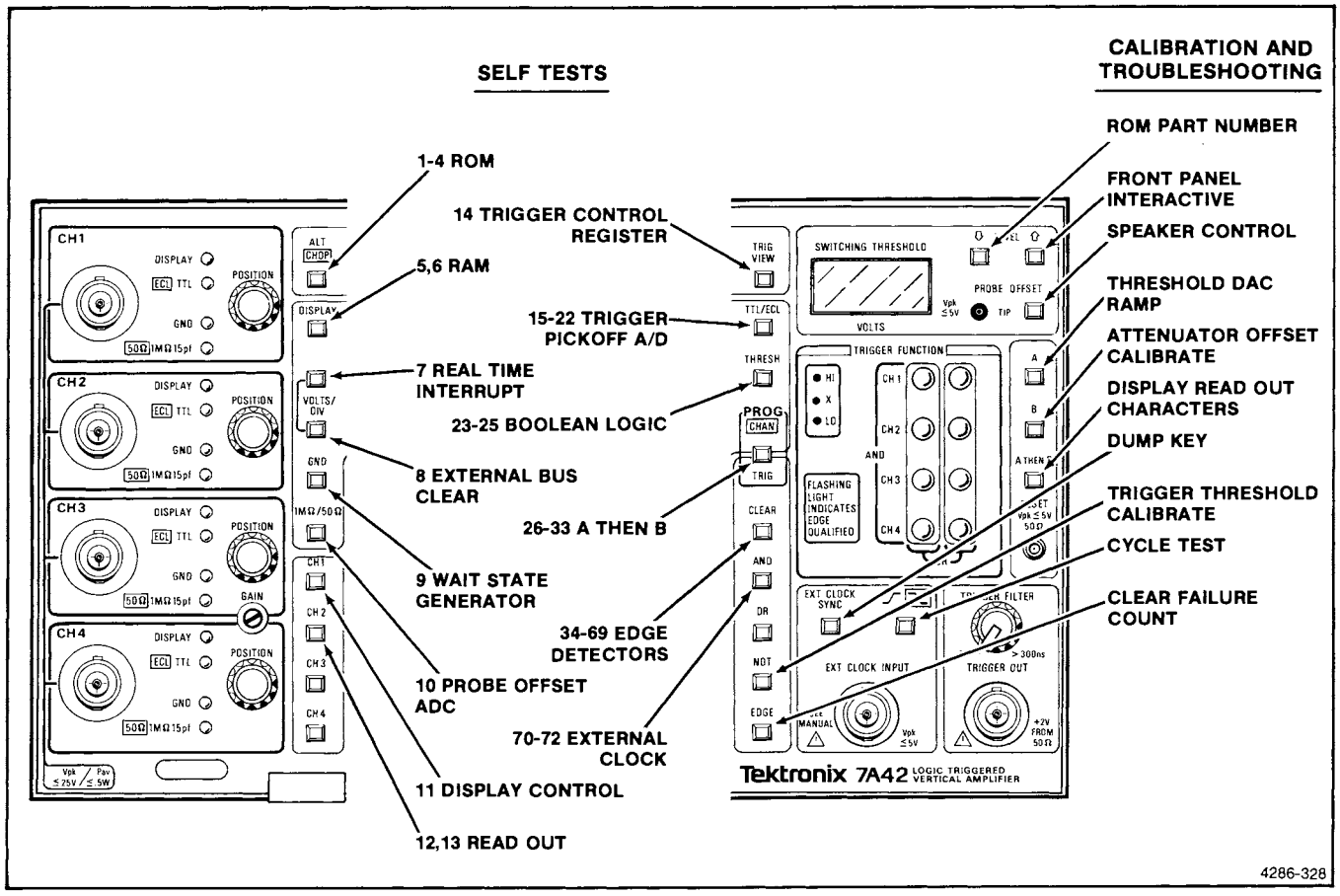


Figure 3-4. Functions of front-panel keys with 7A42 in extended diagnostic test mode.

NOTE

The response to a front-panel key-press sometimes lags that press by up to a second—this is normal. In some cases, two front-panel key-presses may be needed to stop one Extended Test and start another.

Tests that are grouped together are tested sequentially. They cannot be tested individually. For example, self-tests 1 through 4 test the ROMs. When the 7A42 is in extended diagnostic test mode and the ALT CHOP key is pressed, self-tests 1 through 4 will be performed in a repetitive sequence. The left-most two digits of the SWITCHING THRESHOLD VOLTS indicator will display 01, the number of the first test in the sequence, and the right-most two digits will display the total number of failures all tests reveal. To find the number of failures for the individual tests, press the EXT CLOCK SYNC (DUMP KEY) key once. The SWITCHING THRESHOLD VOLTS indicator will display 01XX, where 01 means test 1 and XX is the number of failures Test 1 detected. Press the EXT CLOCK SYNC key once again to find the failures for test 2, and advance the readout through all individual test results by pressing the EXT CLOCK SYNC key once for each test. There is one exception—the DUMP key cannot be used to display individual failures of RAM tests 05 and 06.

The Extended Diagnostics also contain several routines useful as circuit exercises for troubleshooting or calibrating the 7A42. Refer to Calibration and Troubleshooting Aids, in this section, for a description of these features.

When the 7A42 is powered-up in Extended Test mode, ROM and RAM tests are performed. If these tests pass, the mainframe crt will display "ENTER TEST" and the user may then select another test.

If a ROM fails, the CH 1 (column 1) TRIGGER FUNCTION LED will light red and the SWITCHING THRESHOLD VOLTS indicator will display the number of the ROM that failed. If ROM fails, use Forced Instruction Freerun (described in What to Do if The 7A42 Does Not Respond to Front-Panel Controls, later in this section) and SA Test #1, Starting Point #2, #3, and #4 to locate the problem.

If a RAM fails, the Extended RAM test will begin automatically. The CH 2 (column 1) TRIGGER FUNCTION LED will indicate the result of this test each time the test is made. The SWITCHING THRESHOLD VOLTS indicator will display 0501 (pass is 0500). Use SA Test #5, Starting Point #1 and #2 to locate the problem.

Although it is not recommended because the Extended Test program depends on RAM, the user may attempt to continue by pushing any key.

While a test is running, the front-panel TRIGGER FUNCTION LEDs and the SWITCHING THRESHOLD VOLTS indicator displays the status (passing or failing) of that test. The same TRIGGER FUNCTION LED that lights during the Self-Test now lights. Table 3-6 cross-references the LEDs to particular tests. The LED first lights green to indicate "passing test." If the test fails the LED will light red and stay red as long as the test fails. Thus an intermittent failure will cause the LED to light red whenever the test is failing, and green when it is passing.

If you are running a test continuously, you might want to reset the failure count when the display reaches 99. To do this, press the CLEAR FAILURE COUNT (EDGE) key. The current test will continue to run, but the failure count for all tests in that Test Category will be reset to zero, and the associated TRIGGER FUNCTION LED will turn green until another test fails.

The Extended Diagnostics offers a mode which executes the self-test repetitively. This mode can continuously check the instrument while it is unattended. This is useful during a reliability or temperature-cycle test, or if an intermittent failure is suspected. To initiate this mode, enter Extended Diagnostics and press the CYCLE TEST (SLOPE) key. After the cycle test has started, a push of any key will stop the cycling self-test.

In the Cycle Test mode, the series of self-tests is run continuously, and running sums of the number of failures for each test are tabulated. After each test the TRIGGER FUNCTION LEDs are updated green or red to signify whether the test passed or failed, respectively.

TABLE 3-6
Extended Test Failure Messages

TRIGGER FUNCTION (LED Display)	First Two Digits Of SWITCHING THRESHOLD VOLTS And Crt Readout Display	Extended Test
CH1, first column	01	ROM1
	02	ROM2
	03	ROM3
	04	ROM4
CH2, first column	05	RAM1
	06	RAM1
CH3, first column	07	Real Time Interrupt
	08	External Bus Clear
	09	Wait State Generator
CH4, first column	10	Probe Offset ADC
CH1, second column	11	Display Control
	12	Readout; RST 7.5
	13	Readout; SID
CH2, second column	14	Trigger Control Register
	15, 19	Trigger Pickoff A/D; CH1
	16, 20	Trigger Pickoff A/D; CH2
	17, 21	Trigger Pickoff A/D; CH3
	18, 22	Trigger Pickoff A/D; CH4
	23 through 25	Boolean Logic
	26 through 33	A Then B
CH3, second column	34 through 65	Edge Detectors
	66 through 69	Buffered External Clock
CH4, second column	70 through 72	External Clock

Pushing a key other than EXT CLOCK SYNC will abort the test. The 7A42 will then await the selection of another Extended Test or Troubleshooting and Calibration Aid.

Pressing the EXT CLOCK SYNC (DUMP) key will halt the test, and show the total failure count for failure code 01 on the SWITCHING THRESHOLD VOLTS indicator. Successive pushes will advance the SWITCHING THRESHOLD VOLTS indicator to subsequent failure codes.

Each time the Cycle Test is restarted by pushing the SLOPE key, all failure counts are cleared, and previous data is destroyed.

Two special cases where the Cycle Test will function differently than previously stated are ROM and RAM failures. If a ROM fails, the Cycle Test will stop, the TRIGGER FUNCTION LED associated with the ROM will light red. At this point, pressing any key will cause the Cycle Test to proceed.

If a RAM fails the Cycle Test will abort, and the Extended RAM test will commence.

BACKGROUND INFORMATION ON SIGNATURE ANALYSIS

Signature analysis is a troubleshooting method for isolating faults, usually to the component level, in complex logic circuits. Signature analysis testing relies on exercising circuit nodes in a repeatable fashion. The type of exercise is relatively unimportant, as long as the events at the node under test are repeatable. For example, a microprocessor system can easily be made to repeatedly increment (loop) through its address fields, exercising a good portion of the instrument's circuitry. In most cases, exercise routines are stored in ROM, then retrieved and run to exercise circuitry.

Once a means of exercising the circuitry has been implemented, actual signatures at circuit nodes can be taken. Individual signatures are taken over a specific number of system clock cycles (gate time), determined by how the signature analyzer is electrically connected into the system. The actual signature is presented to the user as a four-digit hexadecimal number that is a numerical representation of the complex sequence of events occurring at the node under test. Individual signatures may be composed of the characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, C, F, H, P and U.

The signatures taken at various nodes are compared to the "signature sets" containing known good signatures for each particular test node. (All signatures for these procedures were taken with a Tektronix 067-1090-00 Signature Analyzer.) An incorrect signature indicates a problem. Bad signatures can be traced (in terms of data flow) to the point of error in much the same way a bad waveform can be traced to its source in analog circuitry.

However, there is an important difference between analog signal tracing and digital signature tracing. In analog signal tracing, clues to faults are indicated by deviations from the desired waveshape (clipping, oscillations, power supply noise, etc.). In signature tracing, however, subtle differences in signatures from those desired mean nothing. A wrong signature just indicates trouble, not a particular type of trouble.

There are several cases where certain wrong signatures may provide clues, though. A signature of 0000 may be an indication that a TTL signal is shorted to ground (0000 is the low state signature). Likewise, a node with a faulty signature the same as the V_{cc} signature may be shorted to the positive supply. When two or more nodes have the same bad signature, they may be shorted together.

EXTENDING CIRCUIT BOARDS FOR TROUBLESHOOTING

Some troubleshooting may require that the A6 Trigger board or A7 Digital Board be installed in an extended position to gain access to components. Refer to Figures 3-5 and 3-6.

How To Extend The A6 Trigger Board

1. Remove the A6 Trigger Board assembly as described in the Corrective Maintenance section under Removing and Replacing Parts.

2. Install the 670-7334-00 right-angle Extender Board (part of 067-1112-00 7A42 Service Kit) into socket J500 on the A3 Interconnect Board where the A6 Trigger Board was connected.

3. Replace the upper circuit-board support immediately behind the Extender Board to prevent it from coming unplugged.

4. Remove the Trigger Shields from the front and back of the A6 Trigger Board.

5. Install the A6 Trigger Board in the socket of the Extender Board. Viewed from the front of the 7A42, the A6 Trigger Board components should be on the right side of the board.

6. In place of the standard wire, install a 15-inch, 3-conductor ribbon wire (175-2904-00, part of 067-1112-00) from P600 of the A6 Trigger Board to P910 of the A8 MPU Board. Be sure that pin 1 is correctly oriented at both ends of the wire.

7. In place of the standard wire, install a 15-inch, 3-conductor ribbon wire (175-2904-00, part 067-1112-

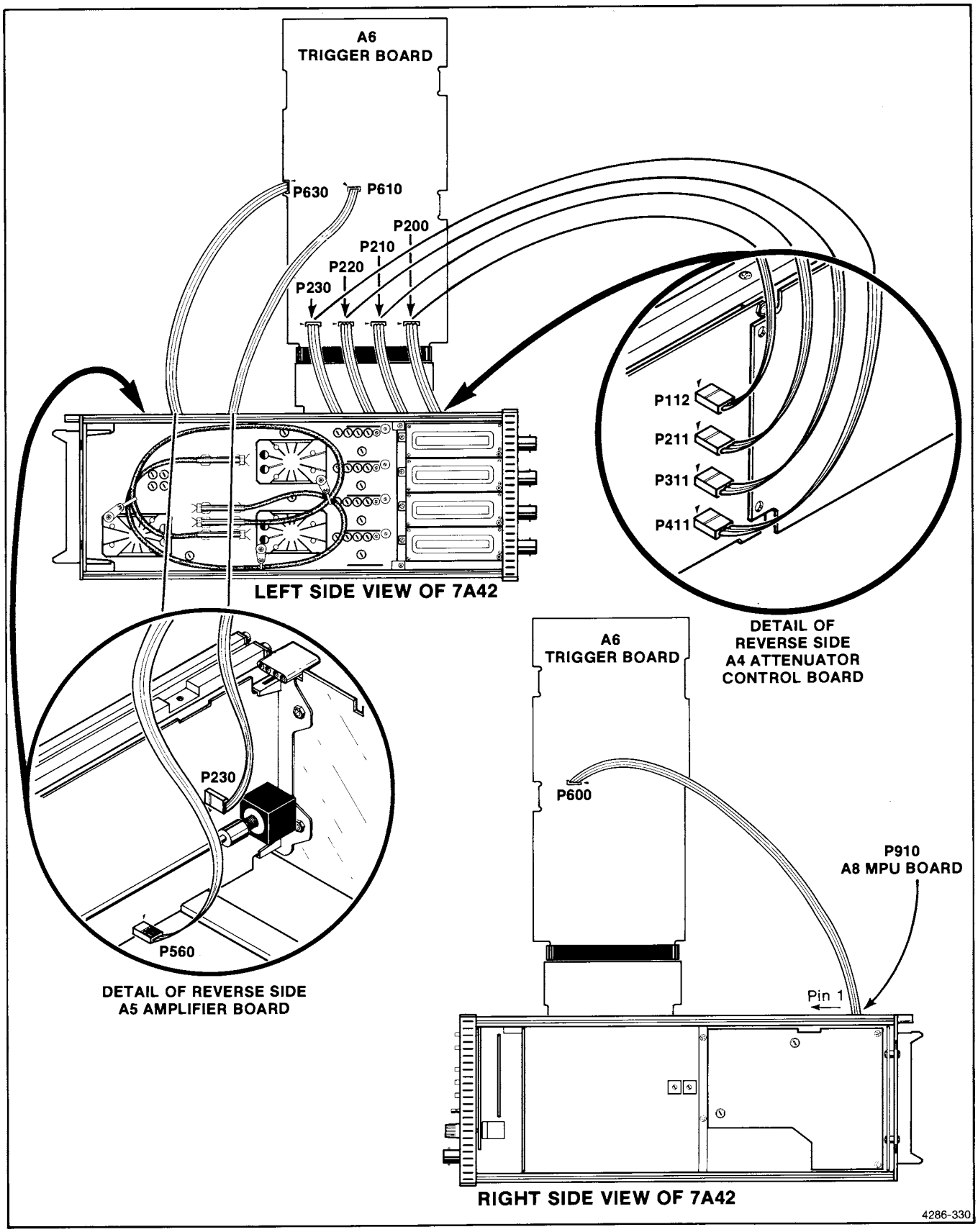


Figure 3-5. Right and left views of extended A6 Trigger Board and its connections.

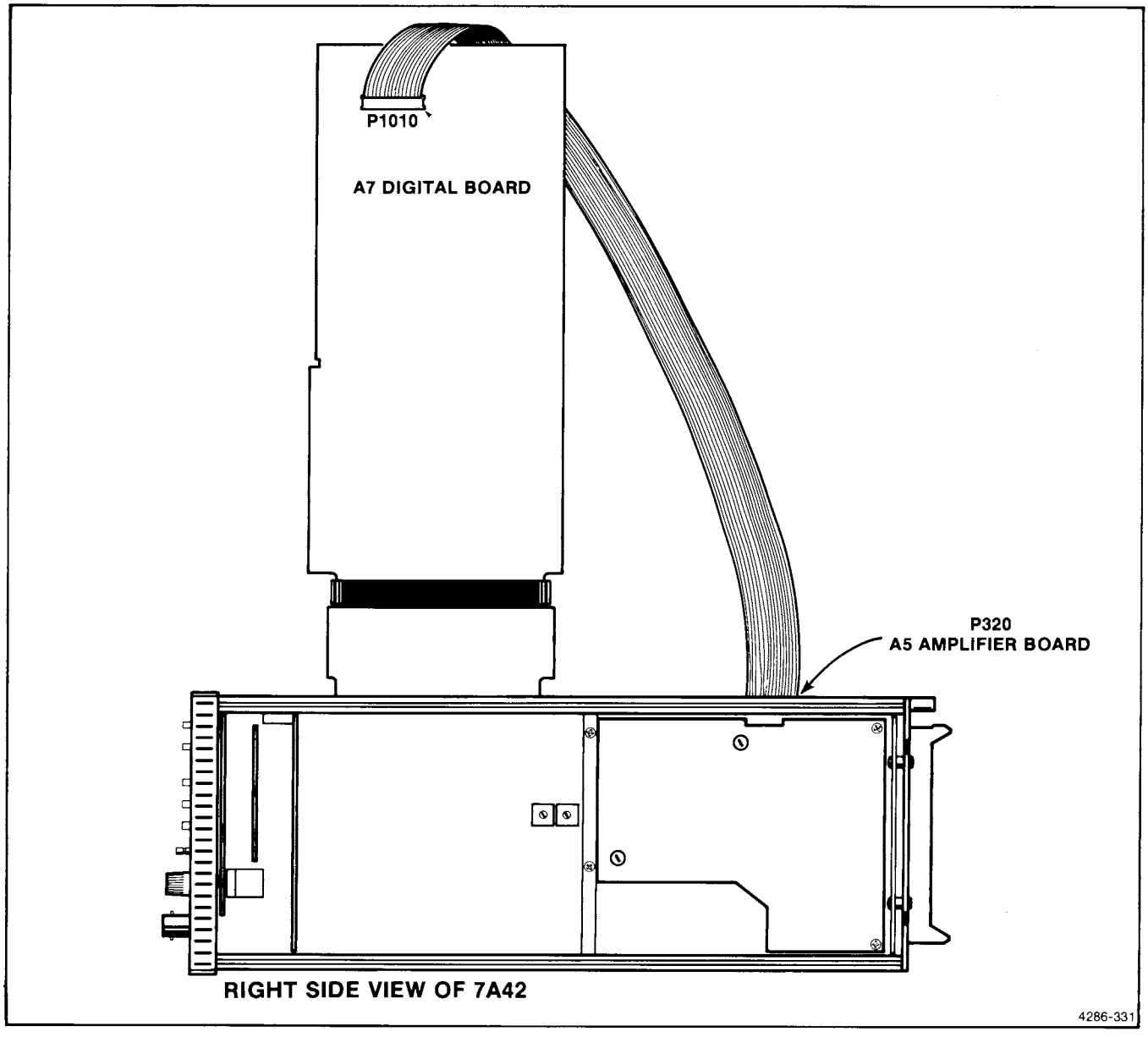


Figure 3-6. Extended view of A7 Digital Board and its connections.

00) from P610 of the A6 Trigger Board (pins on back side) to P230 of the Amplifier Board. Be sure that pin 1 is correctly oriented at both ends of the wire.

8. In place of the standard wire, install a 15-inch, 3-conductor ribbon wire (175-2904-00, part 067-1112-00) from P630 of the A6 Trigger Board (pins on back side) to P560 of the A5 Amplifier Board. Be sure that pin 1 is correctly oriented at both ends of the wire.

9. Some troubleshooting procedures suggest that four 317-0201-03 Trigger Input Terminations be installed. If so, there is no need to install the four ribbon wires as described in step 10.

10. In place of the standard wires, install four 9-inch, 3-conductor ribbon wires (175-1754-00, part of 067-1112-00) from P411, P311, P211, and P112 of the A4 Attenuator Control Board to P200, P210, P220, and P230 respectively of the A6 Trigger Board. Be sure that pin 1 is correctly oriented at both ends of the wire.

11. After troubleshooting, perform the above steps in reverse order to reinstall the A6 Trigger Board in its original location.

How To Extend The A7 Digital Board

1. Remove the A7 Digital Board assembly as described in the Corrective Maintenance section under Removing and Replacing Parts.

2. Install the 670-7334-00 right-angle Extender Board (part of 067-1112-00 7A42 Service Kit) into socket J400 on the A3 Interconnect Board where the A7 Digital Board was connected.

3. Replace the upper circuit-board support immediately behind the Extender Board to prevent it from coming unplugged.

4. Install the A7 Digital Board in the socket of the Extender Board. Viewed from the front of the 7A42, the Digital Board components should be on the right side of the board.

5. In place of the standard wire, install the long 20-conductor gray ribbon cable (175-7373-00, part of 067-1112-00) from P1010 of the A7 Digital Board to P320 of the A5 Amplifier Board.

6. After troubleshooting, perform the above steps in reverse order to reinstall the A7 Digital Board in its original location.

WHAT TO DO IF THE 7A42 DOES NOT RESPOND TO FRONT-PANEL CONTROLS

Before the diagnostics can be used, the kernel (the MPU, EPROM, address lines and data lines) must be up and running, able to read front-panel key-pushes, and report the pass/fail status of each test to the front-panel LEDs. There are two jumper-selectable tests on the MPU Board which will aid a technician in troubleshooting the kernel and the external bus; Forced Instruction Freerun (FR), and External Bus Exercise (XBUSX). Forced Instruction Freerun is used to troubleshoot the kernel. XBUSX aids in clearing the data bus external to the kernel, and exercises the keyboard controller IC and the front-panel LED Driver ICs.

FORCED INSTRUCTION FREERUN

In this mode, eight jumpers are removed to disconnect the 8085 A/D-bus from all circuitry except the pull-up resistors and the collector of a transistor attached to AD7. During the time the processor does an opcode fetch, the transistor pulls AD7 low, resulting in the machine code for a MOVA,A (the equivalent of a NOP). This forces the processor to "freerun," with the program counter sequencing the address lines through the entire addressable range. During this time a signature analyzer (SA) or an oscilloscope can be used to check the lines, ROMs, internal data bus (RAMs and External Bus receiver are disabled by removing jumpers), and the address-decoded read selects. A jumper, in the address-decoded write select circuitry, causes $\overline{WR}$ to be replaced with $\overline{RD}$. This lets these selects be signature analyzed (only the $\overline{RD}$ line will be active during freerun). On the MPU Board, the A15 line and the EPROM chip selects are on square pins to provide SA-start/stop. The accessible rising edge of $\overline{RD}$ will be used as SA-clock. Pull-up resistors are provided, on both sides of the A/D bus jumper and on the external bus, to ensure stable signatures with analyzers that do not have integral pull-up or pull-down resistors. During Forced Instruction Freerun, the Auto Restart Circuit must be disabled.

Using FR, everything in the kernel can be tested except the RAMs.

To start the Forced Instruction Freerun, proceed as follows:

1. Turn off power in host mainframe.

2. Remove the 7A42 from the host mainframe.

3. Remove two screws at the rear of the A9 Power Supply Board and loosen the two screws that attach the power-supply mounting post to the upper and lower rails. This allows the A9 Power Supply Board to be swung out to gain access to the A8 MPU Board.

4. Remove the eight P420 link-plug jumpers located to the right of A8U305 (8085A). See Figure 3-7.

5. Move the Mode link-plug jumper, P540, to the FR—freerun position. This jumper is located near the left end of the NiCad battery (A8BT650).

6. Rotate the P645 link-plug jumper, located below A8U635, to "SA" position to substitute $\overline{RD}$ signals for $\overline{WR}$ signals.

7. Remove the RE link-plug jumper, P742, to disable RAMs from writing. This jumper is located below A8U730.

8. Remove the XBE link-plug jumper, P900, located to the right of A8U900, to prevent external bus from writing on internal bus.

9. Install the $\overline{ARST}$ link-plug jumper, P405, which is located to the right of A8U305. This will prevent automatic restarts to the processor. Figure 3-7 shows the jumpers on the A8 MPU Board.

10. Install the $\overline{SPKR}$ link-plug jumper, A7P730, to disable the speaker. See Figure 3-8 for link-plug jumper location. Use long-nose pliers to access A7P730 through the hole in the bottom rail.

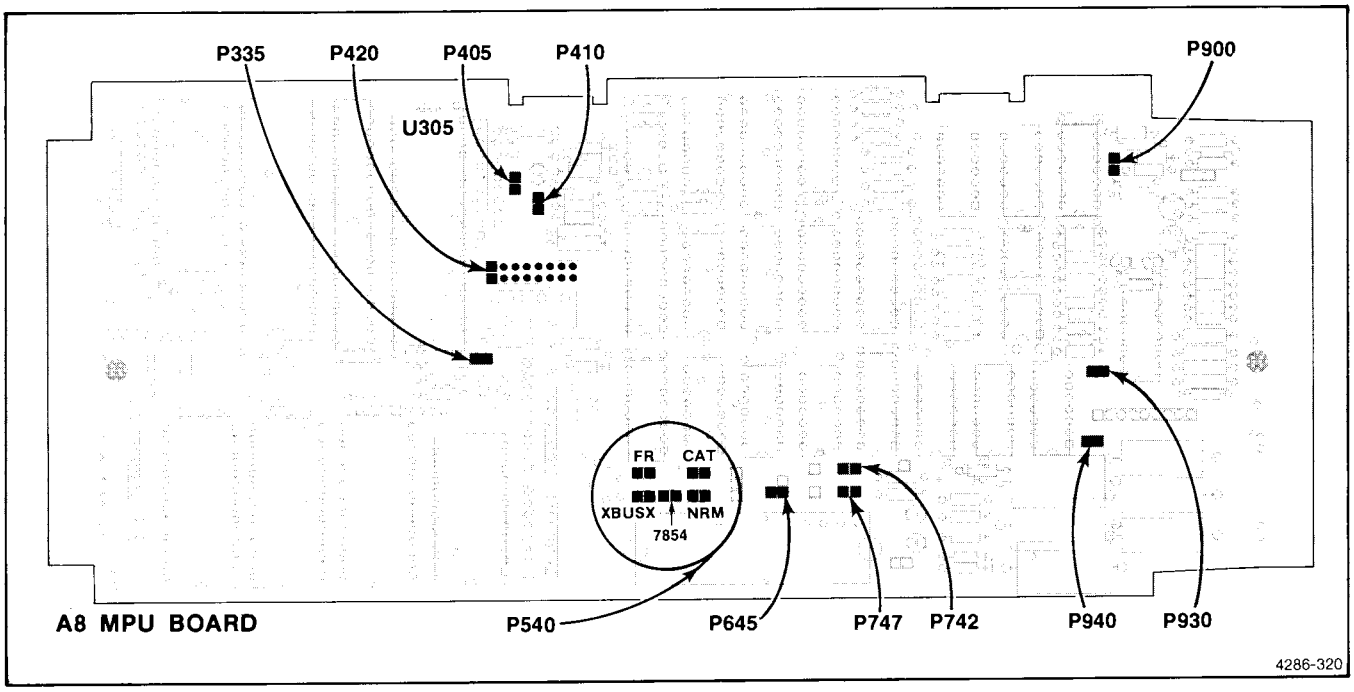


Figure 3-7. Location of jumpers on A8 MPU Board.

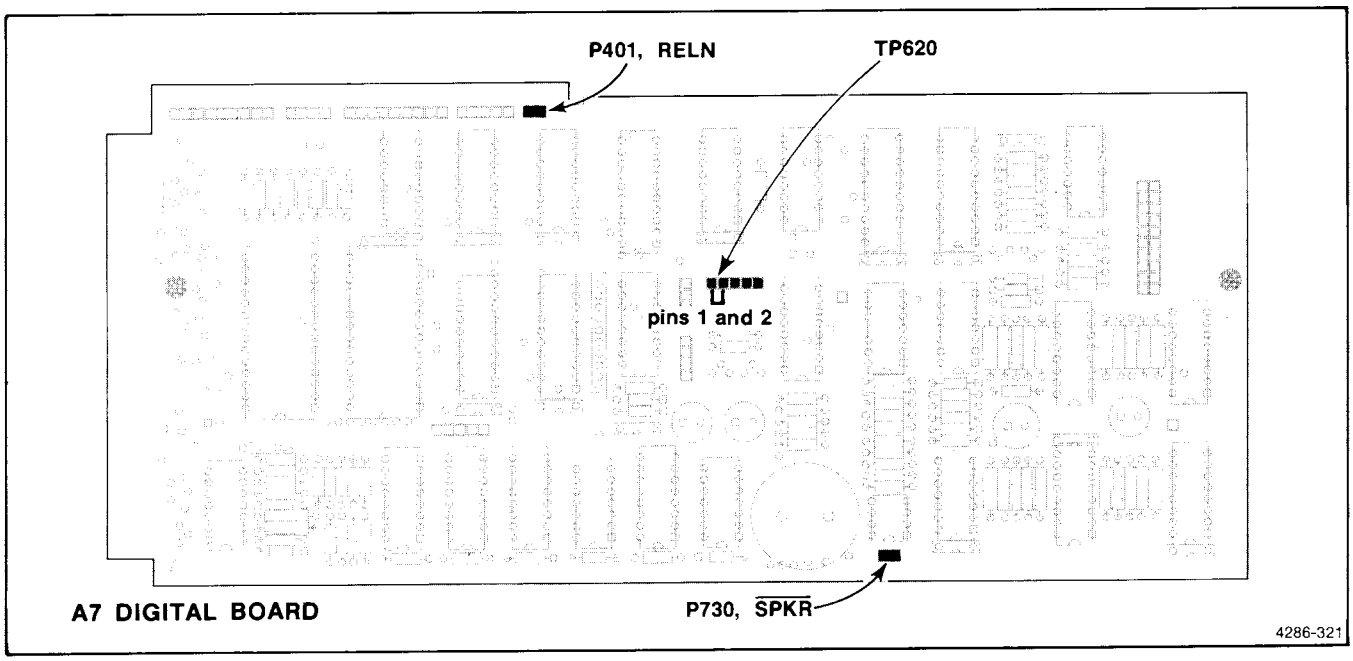


Figure 3-8. Location of jumpers on the A7 Digital Board.

11. Remove the RELN link-plug jumper, A7J401, to disable armature relay drive.
12. Use two Flexible Plug-in Extenders (Tektronix Part 067-0616-00) to connect the 7A42 to the host oscilloscope.
13. Turn on the host oscilloscope.
14. Use Signature Analysis Test #1, Starting Points #1 through #5, to ascertain if the kernel is operating properly.

To return to the Normal mode of operation, refer to Table 3-7 for link-plug jumper locations. Table 3-8 lists the purposes of the jumpers.

TABLE 3-7
Alphabetical List of Link-Plug Jumpers on Digital and MPU Boards

Board	Name & Component # of Jumper	Mode				
		Normal		Extended Test	Freerun	XBUSX
		7XXX	7854			
Digital	RELN A7P401	I	I	R	R	R
	$\overline{\text{SPKR}}$ A7P730	R	R	R	I	I
MPU	ABT A8P335	R	R	R	R	R
	AD BUS A8P420	I	I	I	R	I
	BE A8P747	I	I	I	X	X
	NRM/$\overline{\text{TST}}$ A8P410	I	I	R	X	X
	RE A8P742	I	I	I	R	X
	$\overline{\text{ARST}}$ A8P405	R	R	R	I	I
	$\overline{\text{RTI}}$ A8P930	R	R	R	X	R
	SA/NRM A8P645	NRM	NRM	NRM	SA	NRM
	$\overline{\text{WAIT}}$ A8P940	R	R	R	R	R
	$BE A8P900	I	I	I	R	I

Legend: I = jumper installed
R = jumper removed
X = don't care
Other = Jumper installed by this mark on circuit board

TABLE 3-8
Purposes of Link-Plug Jumpers on Digital and MPU Boards

Jumper Name	Purpose of Jumper
ABT	Automatic Board Test; used in manufacturing only.
AD-BUS	Removed during Forced Instruction Freerun to isolate the processor's data bus.
BE	Battery Enable; if jumper is installed, 7A42 will save front panel status at power down, and restore this status at the subsequent power up.
MODE P540	Used to select Read-Out format, Forced Instruction Freerun, and External Bus Exercise modes.
NRM/$\overline{\text{TST}}$	Selects Normal Operating Mode or Extended Test Mode (diagnostic).
RE	RAM Enable; when installed enables the RAMs to be selected. Removed while using Signature Analysis to troubleshoot the kernel.
RELN	Relay Enable; when removed, disables attenuator armature-latch-relay drive circuitry. This should be done during abnormal microprocessor code execution, i.e., during Forced Instruction Freerun, External Bus Exercise.
$\overline{\text{RTI}}$	No Real Time Interrupts; prevents RST 5.5's from occurring. Note that if this is installed, $\overline{\text{RSTRT}}$ must also be installed to prevent the microprocessor from being restarted.
$\overline{\text{ARST}}$	No Restarts; when installed, prevents the Auto Restart Circuit from issuing a hardware RESET IN to the 8085.
SA/NRM	If in SA position, wires $\overline{\text{RD}}$ to the address decoders rather than $\overline{\text{WR}}$. This is done while using Signature Analysis in Forced Instruction Freerun.
$\overline{\text{SPKR}}$	No Speaker; when installed disables the speaker.
$\overline{\text{WAIT}}$	No WAIT state; when installed disables the Wait State Generator. If installed, may cause problems on the Trigger board.
XBE	External Bus Enable; removed while using signature analysis to troubleshoot the kernel.

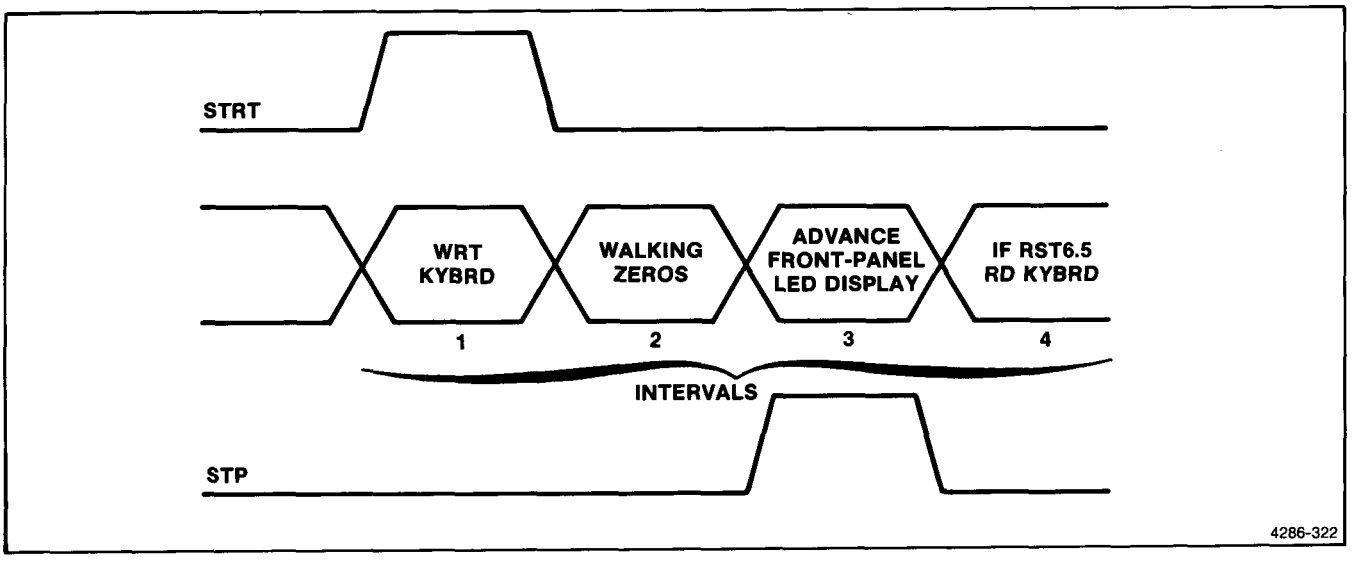


Figure 3-9. Timing of XBUSX operation.

EXTERNAL BUS EXERCISE (XBUSX)

At power up, the processor will read data bit 7 at the memory mapped location "XBUS" to determine if the External Bus Exercise link-plug jumper is installed. The cycle shown in Figure 3-9 will be repeated until the jumper is removed.

Interval 1 (see Fig. 3-9)

During this segment, the "mode word" is written to the keyboard controller IC, configuring it to match the 7A42 Switch Board hardware.

The only RAM available external to kernel is concealed in the display portion of the 8279 Keyboard Controller IC. At the beginning of interval 1, the processor writes, then reads the 8279 RAM to determine if the external bus is clear. It reports the result to an LED labeled BUSCLR, which is mounted on the A8 MPU Board.

Interval 2

The processor's internal and external buses are isolated with tri-state transparent latches. Walking zeros are latched to the external bus so that an oscilloscope triggered by STRT can be used to find lines shorted to ground, to +5 V, or to each other. Also, signatures may be taken during XBUSX interval 2 by using the negative transition of STRT as SA-start and the positive transition of STP as SA-stop. Each time the pattern advances, all latches on the Digital and Trigger Boards are also written so that their outputs will walk zeros and can be checked with an oscilloscope or a signature analyzer. The walking-zero pattern is repeated 47 times during interval 2.

Interval 3

With every cycle of XBUSX, the front-panel LED display will be updated. The user will see the LEDs go on and off in an orderly fashion. The display driver outputs are self-scanning and can best be checked with an oscilloscope.

Interval 4

During interval 4, if RST6.5 is high (a key-push has been detected by the 8279, and keycode data is waiting in its RAM) the processor will read the keycode data and modify the front-panel LEDs and front-panel status LEDS to confirm recognition of a key-push. The two-digit keycode is also displayed on the SWITCHING THRESHOLD VOLTS indicator.

To start the External Bus Exercise, proceed as follows:

1. Turn off power in host mainframe.
2. Remove the 7A42 from the host mainframe.
3. Move the MODE link-plug jumper A8P540 to XBUSX position. See Figure 3-7.
4. Install the $\overline{\text{SPKR}}$ link-plug jumper A7P730 to disable the speaker. See Figure 3-8 for jumper location.
5. Use two Flexible Plug-in Extenders (Tektronix Part 067-0616-00) to connect the 7A42 to the host oscilloscope.
6. Turn on the host oscilloscope.
7. Use SA Test #2, Starting Point #1 when in XBUSX mode.
8. Examine the following:

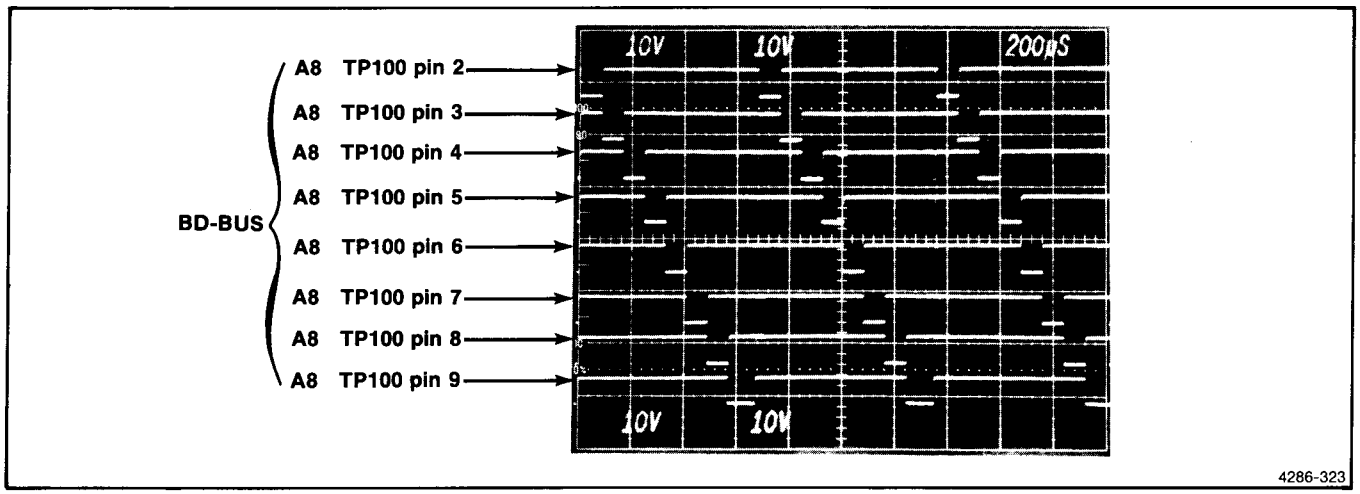


Figure 3-10. A typical "walking-zeros" waveform.

External Bus Operation

Check that the $\overline{\text{BUSCLR}}$ LED is not lit. The $\overline{\text{BUSCLR}}$ LED is located on the A8 MPU Board to the right of NiCad battery BT650. If it is on, use an oscilloscope to check the "walking-zeros" pattern on pins 2-9 of the external bus at A8TP100 (located at the upper left hand corner of A8). Use STRT and STP on A8U715 for triggering. Figure 3-10 shows a typical walking-zeros waveform.

Front-Panel LED Operation

Check that the LEDs are individually lit to confirm no opens, shorts, LED failures, drive failures, or interconnect problems. LEDs should light all keys except the following: DISPLAY, VOLTS/DIV(2), GND, 1MΩ/50Ω, TTL/ECL, CLEAR, AND, OR, NOT, EDGE, LEVEL⇧, LEVEL⇩. See Table 3-9.

Front Panel Keys and DVM Display

Press each key and check the DVM display for its distinct key-code. Table 3-9 gives the key codes. This is also a good way to examine the DVM display for problems. If the DVM display will not light, you can verify that the microprocessor recognizes a switch-closure by observing a change from a regular to an erratic sequence of front-panel LED display when the front-panel key is pressed.

Probe Offset DAC and Comparator

During XBUSX the "walking zeros" pattern is also written to A8U600 (Probe Offset DAC). Trigger the test oscilloscope on the positive transition of "STRT" (A8P740) and observe that the waveforms on A8U505A pins 1, 2, and 3 are similar to those shown in Figure 3-11. Also, check that level shifter VR510 and R515 is functioning.

TABLE 3-9
Front-Panel Interactive Keys, Codes, and LEDs

Key	Code	Front-Panel LED
ALT/CHOP	0000	Back-lit
DISPLAY	0001	CH1 DISPLAY
VOLTS/DIV-upper	0002	TRIG. FUNC. COL2 CH1
VOLTS/DIV-lower	0003	TRIG. FUNC. COL2 CH2
GND	0004	CH1 GND
1MΩ/50Ω	0005	CH1 1M/50 OHM
CH1	0006	Back-lit
CH2	0007	Back-lit
CH3	0015	Back-lit
CH4	0014	Back-lit
TRIG VIEW	0008	Back-lit
TTL/ECL	0009	CH1 TTL/ECL
THRESH	0010	Back-lit
PROG	0011	Back-lit
CLEAR	0012	TRIG. FUNC. COL2 CH3
AND	0013	TRIG. FUNC. COL1 CH1
OR	0021	TRIG. FUNC. COL1 CH2
NOT	0023	TRIG. FUNC. COL1 CH3
EDGE	0022	TRIG. FUNC. COL1 CH4
EXT CLOCK SYNC	0020	Back-lit
Ext Clock Slope	0019	Back-lit
LEVEL⇧	0024	TRIG. FUNC. COL2 CH4
LEVEL⇩	0025	**EXIT EXERCISE**
PROBE OFFSET	0026	Back-lit
A	0027	Back-lit
B	0028	Back-lit
A THEN B	0029	Back-lit

Auto Restart Circuit

Background Information—This circuit causes a hardware reset to the microprocessor when it detects that real-time interrupts are not being serviced in a regular manner. This should occur only when there are hardware or firmware problems in the kernel. In normal operating conditions, real-time interrupt RST5.5 occurs and is immediately followed by a pulse on the $\overline{\text{INTAC}}$ line. This repeats approximately every 12 ms as determined by astable multivibrator U815.

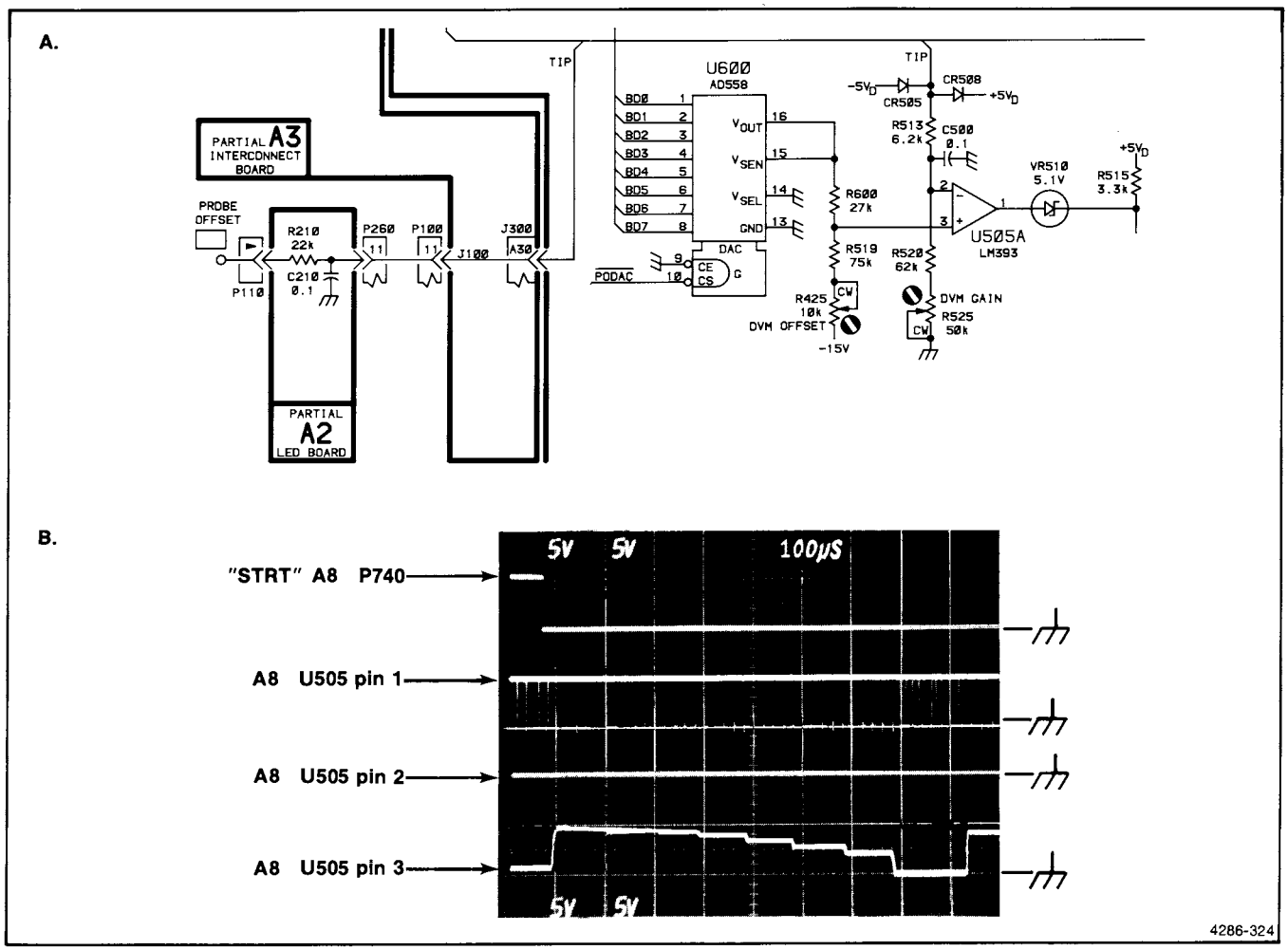


Figure 3-11. (A) Partial A8 CPU diagram: probe-offset DAC and (B) waveforms when operating.

If the circuit is working properly and detecting a defect in the kernel, RESET IN will be cycling at about 2 Hz.

To enable the Auto Restart Circuit, remove the A8P405 link-plug jumper located to the right of A8U305. Symptoms of Auto Restarts in XBUSX include:

1. RESET-IN of the 8085 (A8U320 pin 36) will be pulled low at a frequency of about 2Hz, and

2. The front-panel LED display will run only partially through its sequential pattern before the microprocessor is restarted.

The cause of a restart problem could be one or more of the following:

a. Kernel failure—if this is suspected, use Forced Instruction Freerun to isolate the problem.

b. A8U815 Real Time Interrupt Astable Failure—the output of this IC should be free-running, have a 50% duty cycle, LSTTL levels, with a period of about 12 ms. Note that A8J930 $\overline{\text{RTI}}$, which disables Real Time Interrupts (RST 5.5), should not be installed.

c. Auto Restart Circuit Failure—refer to Figure 3-12 for typical circuit operation.

To return to the Normal mode of operation, refer to Table 3-6 for correct link-plug jumper locations.

DIAGNOSTIC TEST DESCRIPTIONS

This section lists the Diagnostic Tests by code number. The first 13 tests are closely related to specific components or small functional groups of components. To help isolate problems, specific troubleshooting tips accompany the test descriptions. The remainder of the tests (14 through 72) cover the trigger circuitry but do not correspond directly with the individual components. Instead, a number of different codes will likely be reported if an individual component fails. This pattern of

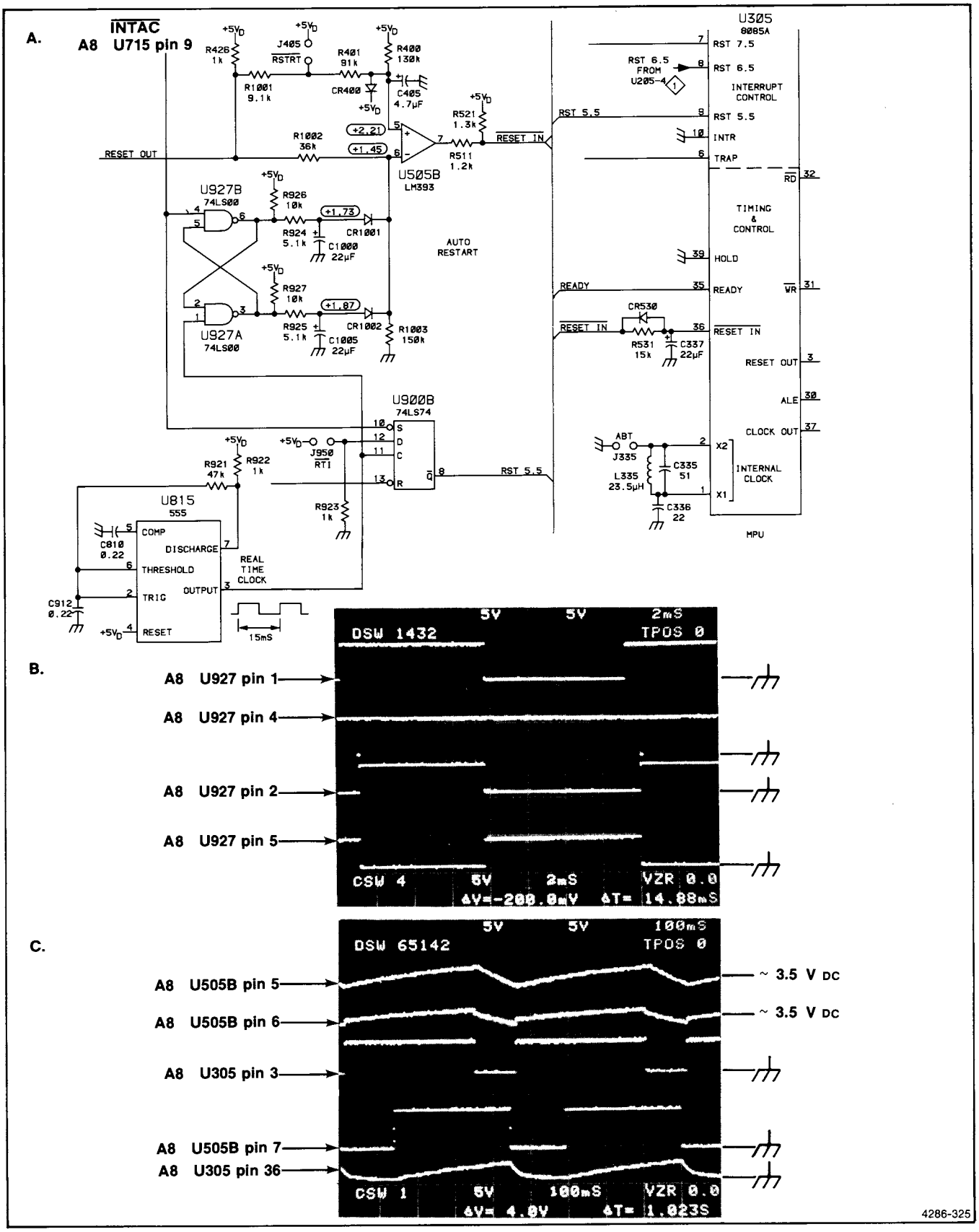


Figure 3-12. (A) Partial A8 CPU diagram: auto-restart circuit, (B) waveforms when operating normally, and (C) waveforms when kernel has failed.

codes provides the key to finding the problem through the use of the Trigger Diagnostic Charts, which then leads to a specific troubleshooting procedure.

ROMs

1—ROM A8U145

The ROM version number and its complement are read from the ROM trailer to verify that the data bus can transmit both logic levels.

A check-sum is computed and compared to the value stored in the ROM trailer.

If the test fails, use Forced Instruction Freerun and signature analysis to locate the problem. Refer to SA Test #1, Starting Point #3 and verify the control line setups for each table before proceeding.

2—ROM A8U245

The ROM version number and its complement are read from the ROM trailer to verify that the data bus can transmit both logic levels.

A check-sum is computed and compared to the value stored in the ROM trailer.

If the test fails, use Forced Instruction Freerun and signature analysis to locate the problem. Refer to SA Test #1, Starting Point #4 and verify the control line setups for each table before proceeding.

3—ROM A8U340

The ROM version number and its complement are read from the ROM trailer to verify that the data bus can transmit both logic levels.

A check-sum is computed and compared to the value stored in the ROM trailer.

If the test fails, use Forced Instruction Freerun and signature analysis to locate the problem. Refer to SA Test #1, Starting Point #5 and verify the control line setups for each table before proceeding.

4—ROM A8U345

If installed, the ROM version number and its complement are read from the ROM trailer to verify that the data bus can transmit both logic levels.

A check-sum is computed and compared to the value stored in the ROM trailer.

If the test fails, use Forced Instruction Freerun and signature analysis to locate the problem. Refer to SA Test #1, Starting Point #6 and verify the control line setups for each table before proceeding.

RAMs

5—RAM A8U615

Pseudo-random nibbles and their complements are written to and read from RAM1. If the data written to RAM does not match that which is read back, a failure is indicated.

If this test fails in Extended Test mode, select Test 5 (use the DISPLAY key) and use signature analysis to locate the problem. Use SA Test #5, Starting Point #1 and verify control line setup before proceeding.

Tips:

a. Be sure that the RAM Enable link-plug jumper ("RE," A8J742, located below U730) is installed.

b. Check that the Battery Backup Circuit is not causing the problem. If A8U825 pin 1 is stuck low, investigate this circuit.

6—RAM A8U710

Pseudo-random nibbles and their complements are written to and read from RAM2. If the data written to RAM does not match that which is read back, a failure is indicated.

If this test fails in Extended Test mode, select Test 5 (use the DISPLAY key) and use signature analysis to locate the problem. Use SA Test #5, Starting Point #2 and verify control line setup before proceeding.

Tips:

a. Be sure that the RAM Enable link-plug jumper ("RE," A8J742, located below U730) is installed.

b. Check that the Battery Backup Circuit is not causing the problem. If A8U825 pin 1 is stuck low, investigate this circuit.

MPU BOARD MISCELLANEOUS

7—Real Time Interrupt Circuit (RST5.5) A8U815, A8U900B

The microprocessor uses a timing loop to measure the period of the Real Time Interrupt, RST5.5. If the period is out of the range of the stored limits, a failure is indicated.

Symptoms include: Auto Restart Circuit resets the microprocessor (if enabled), audible warning beeps fail to time out, or Trigger Function LEDs fail to blink to indicate an edge-sensitive Trigger Function.

If this test fails in Extended Test mode, select Test 7 (use the upper VOLTS/DIV key) and use an oscilloscope to troubleshoot the circuit. Refer to the typical waveforms shown in Figure 3-13.

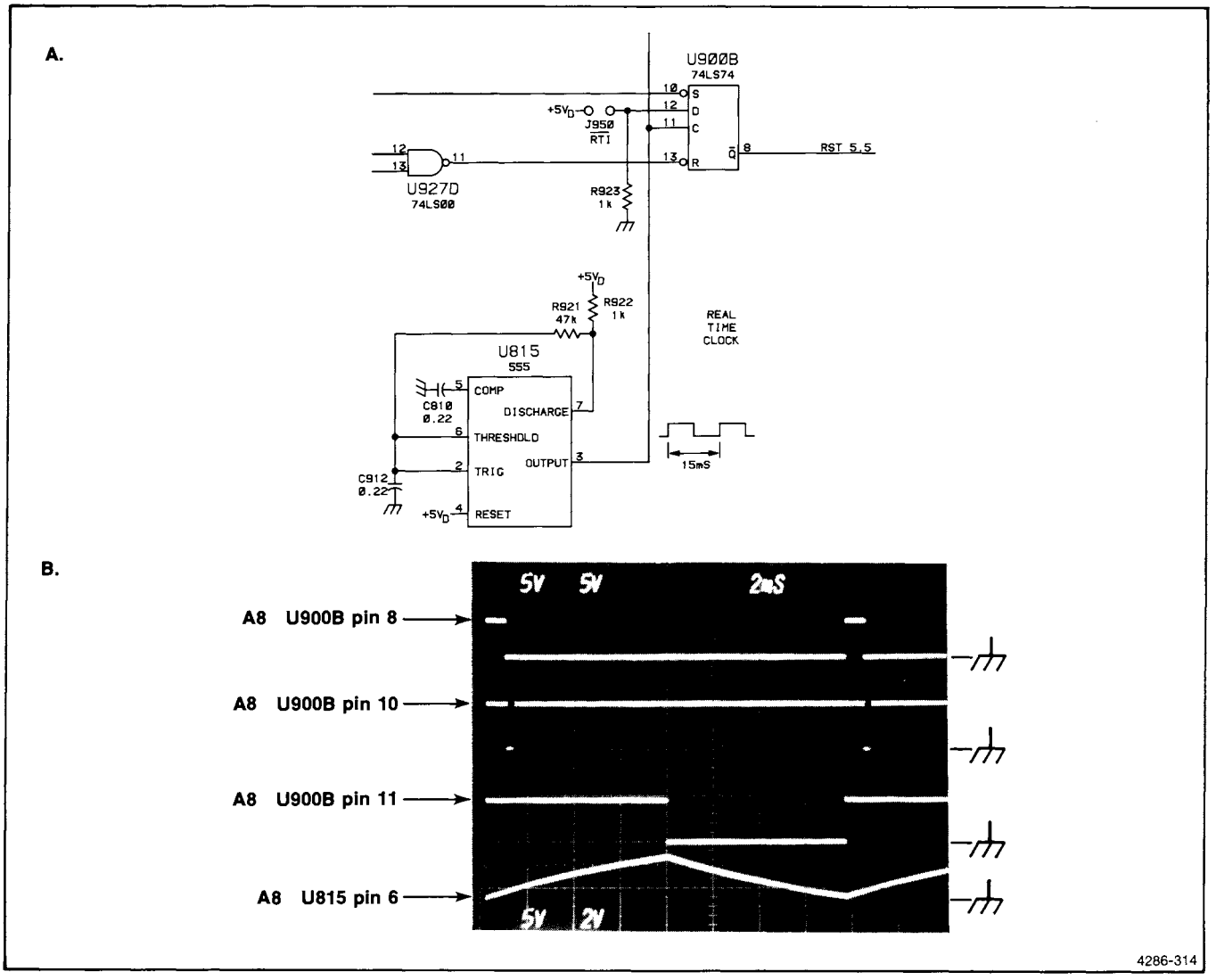


Figure 3-13. Waveforms in real-time interrupt circuit.

Tips:

Check that Real Time Interrupts are not disabled by a link-plug jumper installed in A8J930 "$\overline{\text{RTI}}$."

8—External Bus Clear

This test checks that the External Bus is clear by writing to and reading from the RAM of the 8279 keyboard controller IC.

If this test fails, refer to "What To Do If The 7A42 Does Not Respond To Front-Panel Controls," in this section, and use External Bus Exercise to clear the external bus.

Symptoms include irregular front-panel LED displays, erratic readout on the host oscilloscope, speaker remaining on, etc.

9—Wait State Generator A8U835

Pin 2 of the general output latch A8U715 asserts a high on the enable test (ETST) line. In this condition when a write to the Trigger Board is performed, the Wait State Generator will set the RST5.5 latch, allowing the microprocessor to determine whether a Wait State pulse has occurred.

If this test fails, in Extended Test mode select Test 9 (use the GND key) and use an oscilloscope to troubleshoot the circuit. Refer to the typical waveforms shown in Figure 3-14. Use the positive transition at pin 12 of A8U927D trigger the oscilloscope.

10—Probe Offset ADC A8U600, A8U505A

The open circuit TIP jack voltage is A-D converted via the successive-approximation method. If it is outside predetermined limits, a failure is indicated.

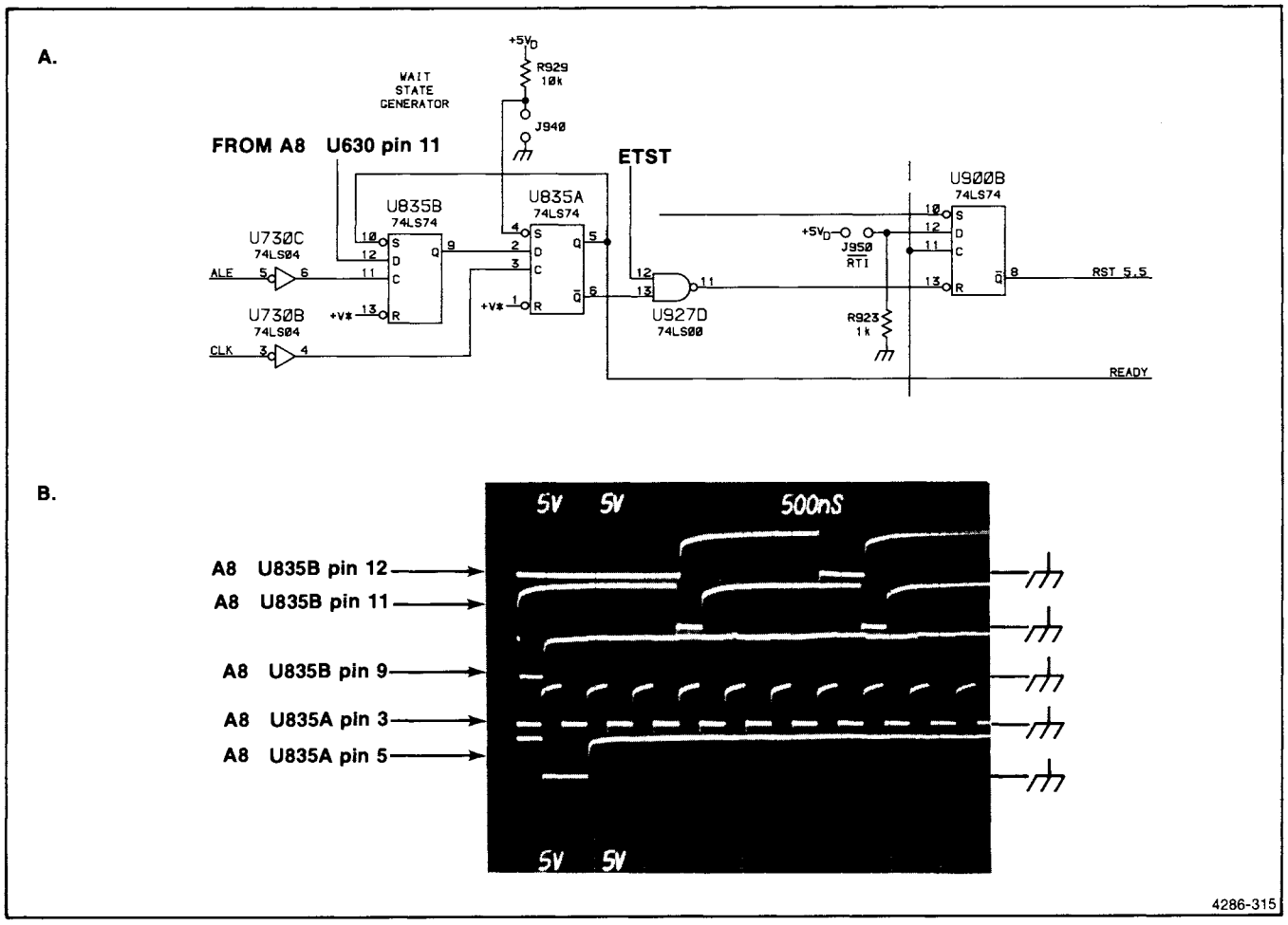


Figure 3-14. Waveforms in wait-state generator.

If this test fails, select test 10 (push the 1MΩ/50Ω button) and use an oscilloscope to troubleshoot the circuit. Refer to the waveforms shown in Figure 3-15b. Also refer to XBUSX in "What To Do if the 7A42 Does Not Respond to Front-Panel Controls," in this section.

Tips:

a. It may be helpful to connect an ac signal to the TIP jack to see that the pin 16 output of DAC A8U600 can follow it. The input should be a 10 Hz sine wave, about 10 V p-p, centered at zero volts.

b. Be sure the TIP jack interconnect is intact, especially the square-pin connection on the LED board - A2P110.

DIGITAL BOARD MISCELLANEOUS

11—Display Control A7U700, A7U800, A7U820, A7U900

Control lines to the programmable array logic (PAL) IC, U800, are set to reconfigure it for the level-sensitive scan design (LSSD) via U700 (Display Control Latch). Pseudo-random data is generated by the microprocessor and passed through the PAL (U800). Output data from the PAL is read back to the processor via the TB1 line where a signature is computed and compared to a stored value. If the signatures differ, a failure is indicated.

If this test fails, in Extended Test mode select test 11 and use signature analysis to isolate the problem. Refer to SA Test #11, Starting Point #1.

12—Readout; RST7.5 A8U830A, B, D and A8Q720A

The time between successive RST7.5 pulses is measured by the microprocessor using a timing loop. If this time is not within the values stored in ROM, a failure is indicated.

If this test fails, in Extended Test mode select Test 12 (use the CH2 key) and use an oscilloscope to isolate the problem. Refer to Figure 3-16 below. Be sure that all interconnections are intact.

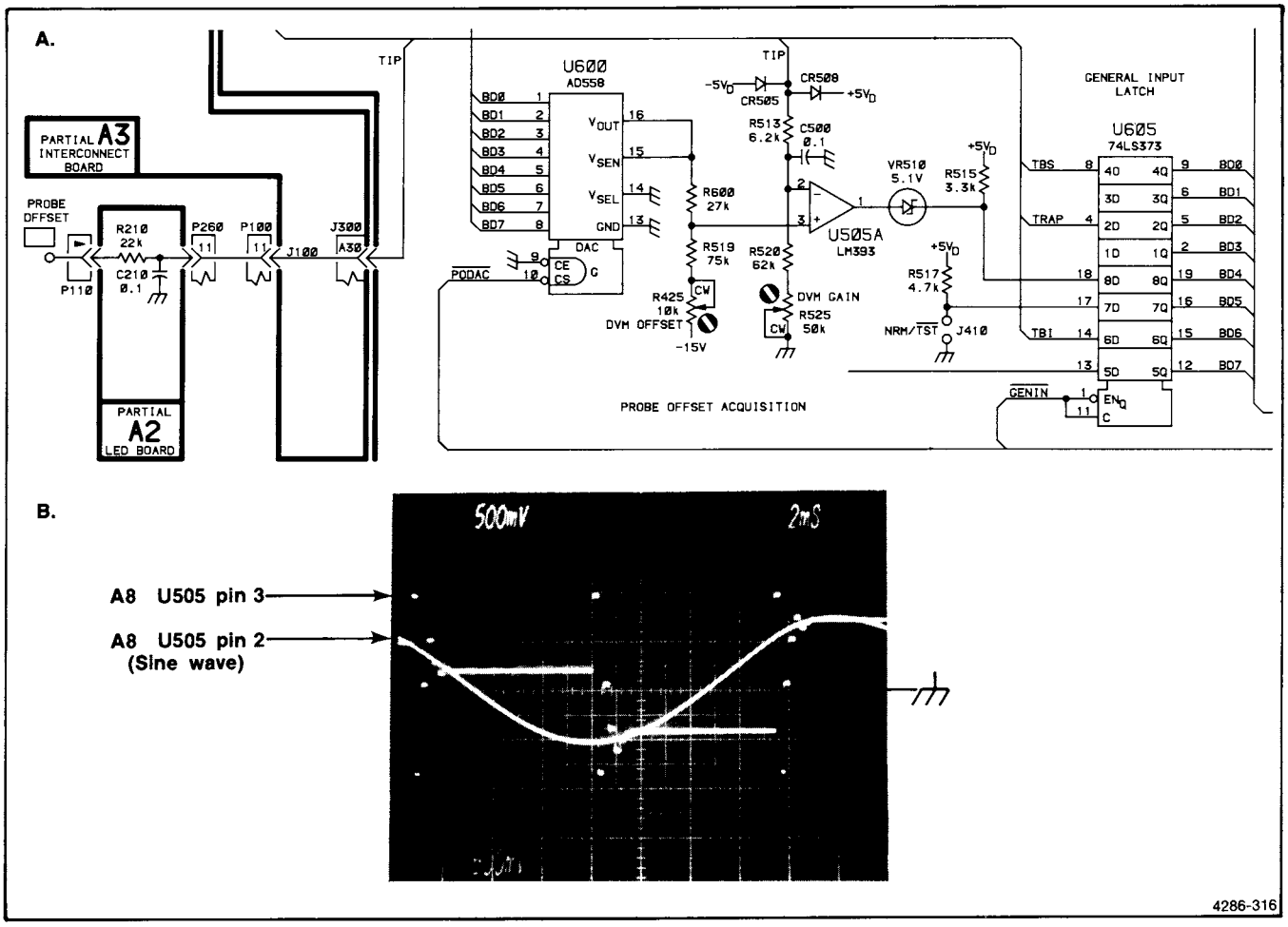


Figure 3-15. (A) Probe offset A/D converter and (B) its waveforms.

In order for this test to verify operation of the 7A42 readout circuitry, the mainframe Readout control should be set to freerun (non-Gated or non-Pulsed) mode.

Check that the gray ribbon cable from P320 on the A5 Amplifier Board to P1010 on the A7 Digital Board is fully engaged at both ends.

Refer to Troubleshooting circuits Not Covered by Diagnostics, in this section, for more information about troubleshooting the readout.

13—Readout; SID A7Q720C

This test counts the number of RST7.5 pulses that occur between occurrences of SID. If there are fewer than seven or more than 10, a failure is indicated.

If this test fails, in Extended Test mode select Test 12 (use the CH2 key), and use an oscilloscope to troubleshoot the circuit. Refer to Figure 3-14 in test 12. Be sure that all interconnections are intact.

In order for this test to verify operation of the 7A42 readout circuitry, the mainframe Readout control should be set to freerun (non-Gated or non-Pulsed) mode.

Check that the gray ribbon cable from P320 on the A5 Amplifier Board to P1010 on the A7 Digital Board is fully engaged at both ends.

Refer to Troubleshooting circuits Not Covered by Diagnostics, in this section, for more information about troubleshooting the readout.

A6 TRIGGER BOARD DIAGNOSTICS

The 7A42 Trigger Diagnostics provide broad coverage of the trigger circuitry and are capable of isolating faults down to small functional groups and, in some cases, to the component level. After running the diagnostic tests, the reported failure codes will translate into specific A6 Trigger Board component groups where conventional troubleshooting should be performed. This translation is

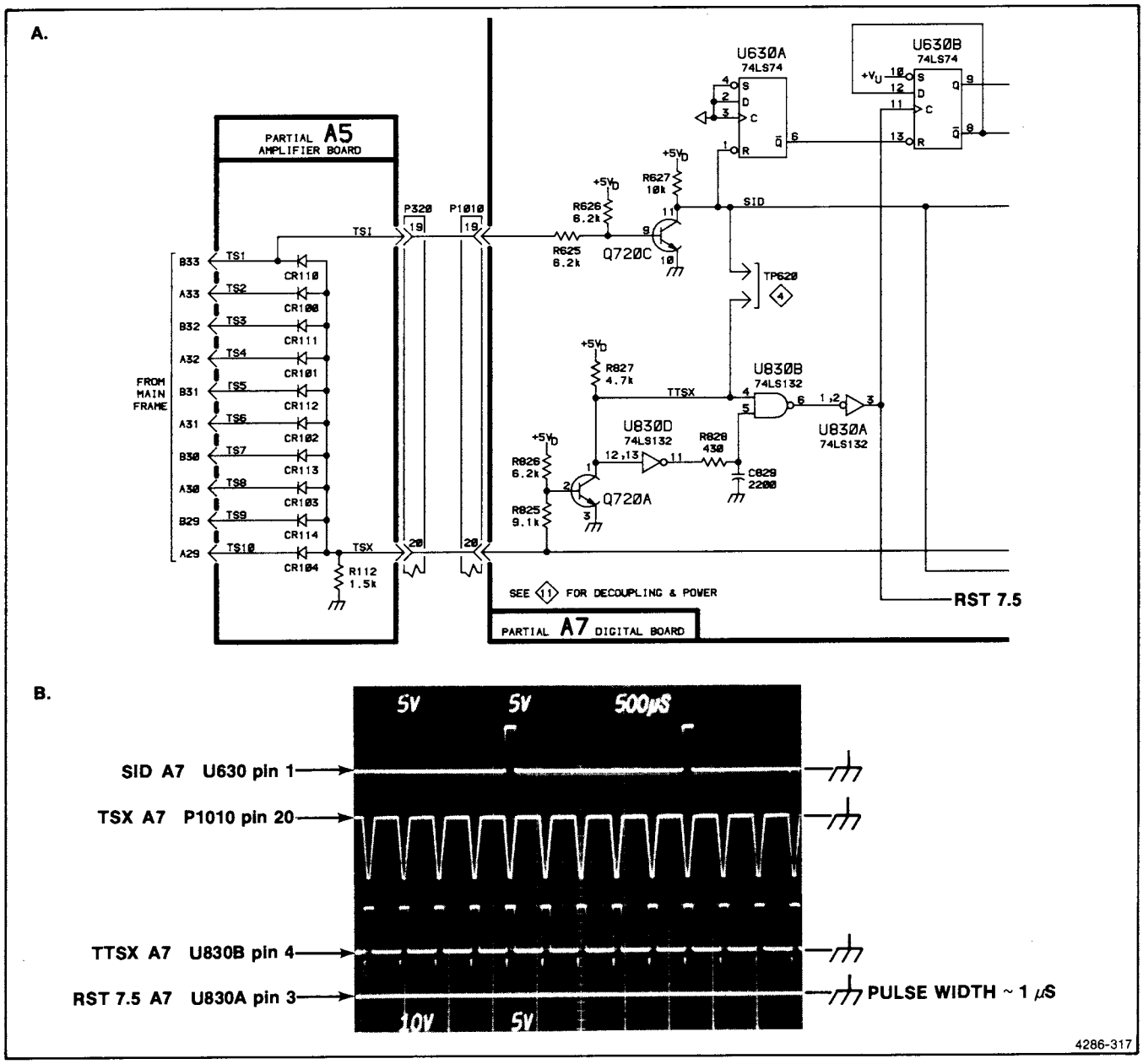


Figure 3-16. (A) Readout circuitry and (B) waveforms at 50 µs/div., (C) 500 µs/div.

aided graphically with the Trigger Diagnostic Charts, which follow.

These charts are intended as guides for interpreting extended diagnostic failure codes associated with the A6 Trigger Board. They show possible failure codes which could be reported if a given part of a component group has failed. They also graphically show the interdependency of some component groups, that is, the parts of the trigger circuitry which must work to detect problems in another part.

The component groups are arranged in a sequence from those most likely to affect the testability of other components (and therefore most likely to cause a broad range of failure code indications) to those most isolated (where a specific failure code indication is possible).

If a given box within the table is filled in, it indicates that parts in that component group could be defective when the associated failure code is displayed. However, because of interdependences among the component groups, they are not necessarily defective.

Patterns of failure codes within a given Test Category can provide insight when determining the source of a problem. If a pattern of failure codes within a category is reported, it often means that the defective component is

one on which the test depends rather than one that the test has been designed to isolate. For example, if every odd-numbered EDGE DETECTOR test fails, the edge-detector circuits are probably not at fault; first check the circuitry on which the edge detectors depend for proper operation. These circuits can be found by finding component groups where the odd-numbered edge-detector tests have been shaded and where any other failure codes indicated by the diagnostics are also filled in on the chart.

For a particular component group to be suspect, not all the failure codes associated with the filled in boxes need be reported by the diagnostics. One failure mode of a given gate might cause one set of failure codes, while another type of failure of the same part could cause an entirely different set of codes. However, if a failure code is indicated by the diagnostics, but that code is not filled in on the chart, the associated component group can be eliminated from suspicion under normal circumstances.

The chart was made with the following assumptions in mind:

1. Only one component has failed. Multiple component failures will cause overlapping failure code indications, and could also cause indications that do not appear with either individual component group.

2. Except where noted otherwise, the front-panel TRIGGER FILTER control is in the OFF (detent) position.

3. If the A6 Trigger Board is being operated in its extended position, and the four Trigger Board input terminations (Tektronix Part 317-0201-03) are installed.

4. Digital IC inputs fail open. They have not failed in a manner which would force the output of another circuit to which they are connected to a high or low state. Internally, however, the input may functionally assume either the high or low state.

5. Digital IC outputs can fail in either the high or low state, but not shorted directly to a power supply or ground. In other words, a defective output might still be pulled to another state by circuitry to which it is connected in the case of wire-AND and wire-OR configurations.

LEGEND

A filled-in box indicates that the parts in its component group could be defective if the associated failure code is reported. The words "Test Category" as used below are defined as the group of failure codes listed under a test title, ie, the BOOLean LOGIC Test Category encompasses failure codes 23, 24, and 25.

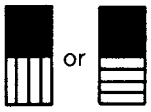
A solid-colored box indicates a failure code which is the only code reported within a given Test Category. This box indicates a strong link between a unique failure indication (not part of a pattern) and the associated component group.

The following shadings indicate that any failure code indication within a given Test Category must be accompanied by other failure code indications in the form of a pattern. Three types of shading are used to distinguish patterns.

Within a Test Category, all failure codes with this shading must occur together.

Within a Test Category, all failure codes with this shading must occur together.

This shading represents failure codes that appear in patterns which differ greatly depending on the failure mode of the defective component. Within a Test Category, the pattern usually consists of only a portion of the shaded failure codes.



A half-solid, half-shaded box indicates a failure code which can be the only indication within a particular Test Category for some failure modes of the defective component. For other failure modes, it might appear as part of a pattern with others of like shading within the Test Category.

EXAMPLE #1

Suppose the trigger diagnostics report failure code 32 and every odd code from 35 to 65 (inclusive). One can immediately look for component groups where the box under test 32 is filled in solid. This is because test 32 was the only code within the Test Category A THEN B which was reported. To further narrow the candidates, look now for one of the above component groups which also has every odd box from 35 to 65 shaded in the same way, i.e., either all vertical or all horizontal lines (not mixed). This indicates that the possible defective component is among the following: A FILTER - U500B, U500C, U402B, U412B SYNCAX, SYNCAY - U800A, U800B STAX, STAY - U402D, U412D, U700B, U402C

The last column in the charts refers to a Troubleshooting Tip(s) which should help identify the specific problem. In this case, a signature analysis loop will be specified, and the fault should be easily isolated.

EXAMPLE #2

The diagnostics report failure codes 26, 27, 33, and every fourth code from 34 to 66 inclusive (34, 38, 42,... 62, 66). This strong pattern is easily recognizable next to the A FILTER components U402A and U402B. The AX BOOL. LOGIC group might also be suspected, but the failure code 23 was not reported. This does not completely eliminate the AX BOOL. LOGIC from suspicion, but because code 23 is in the Boolean Logic test category, which is specifically designed to find troubles in the Boolean Logic circuitry, and because code 23 was not reported, one would do well to look elsewhere first.

INSTRUCTIONS

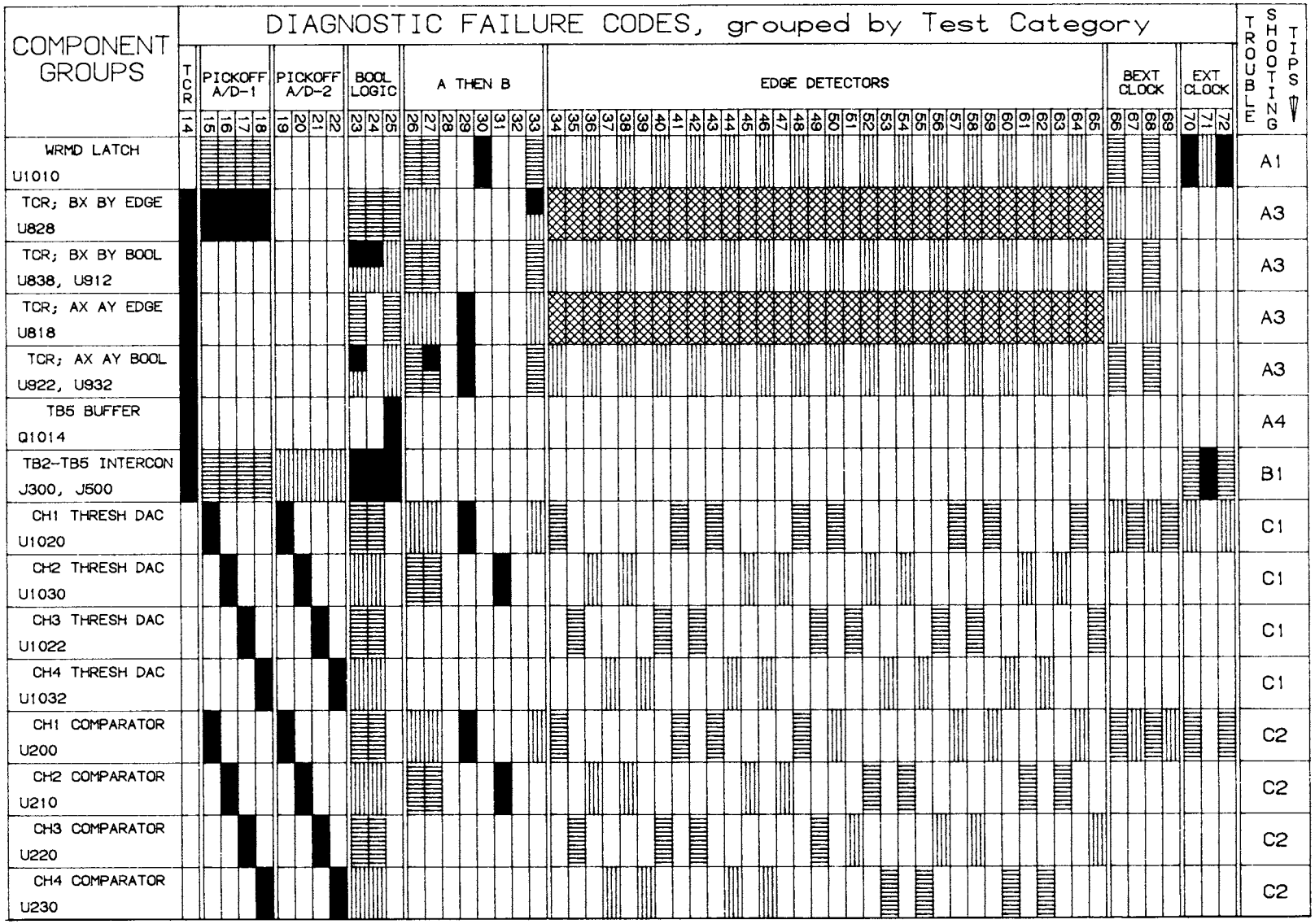
1. Start the trigger diagnostic tests listed in Table 3-10. The diagnostic key definition map (see Fig. 3-4) shows which front-panel buttons to push. The tests run very quickly; in a second or two each set of tests will run many times. If a particular failure is intermittent or temperature-sensitive, the tests can be run indefinitely while the board is heated or cooled.

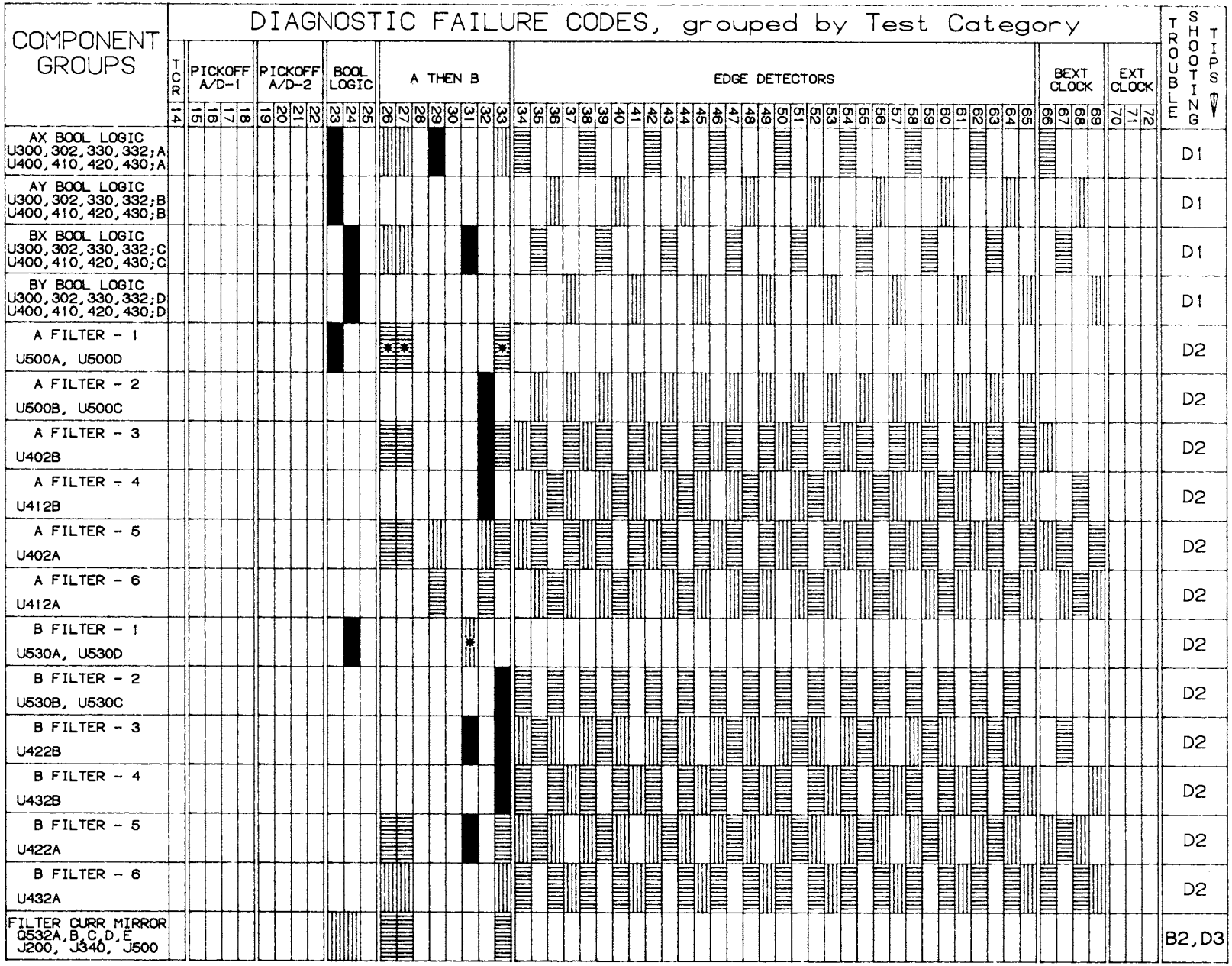
2. After the tests have run, use the DUMP key to single-step the self-tests and thereby find which tests failed. Record these code numbers.

TABLE 3-10
Names and Codes of Trigger Diagnostic Tests

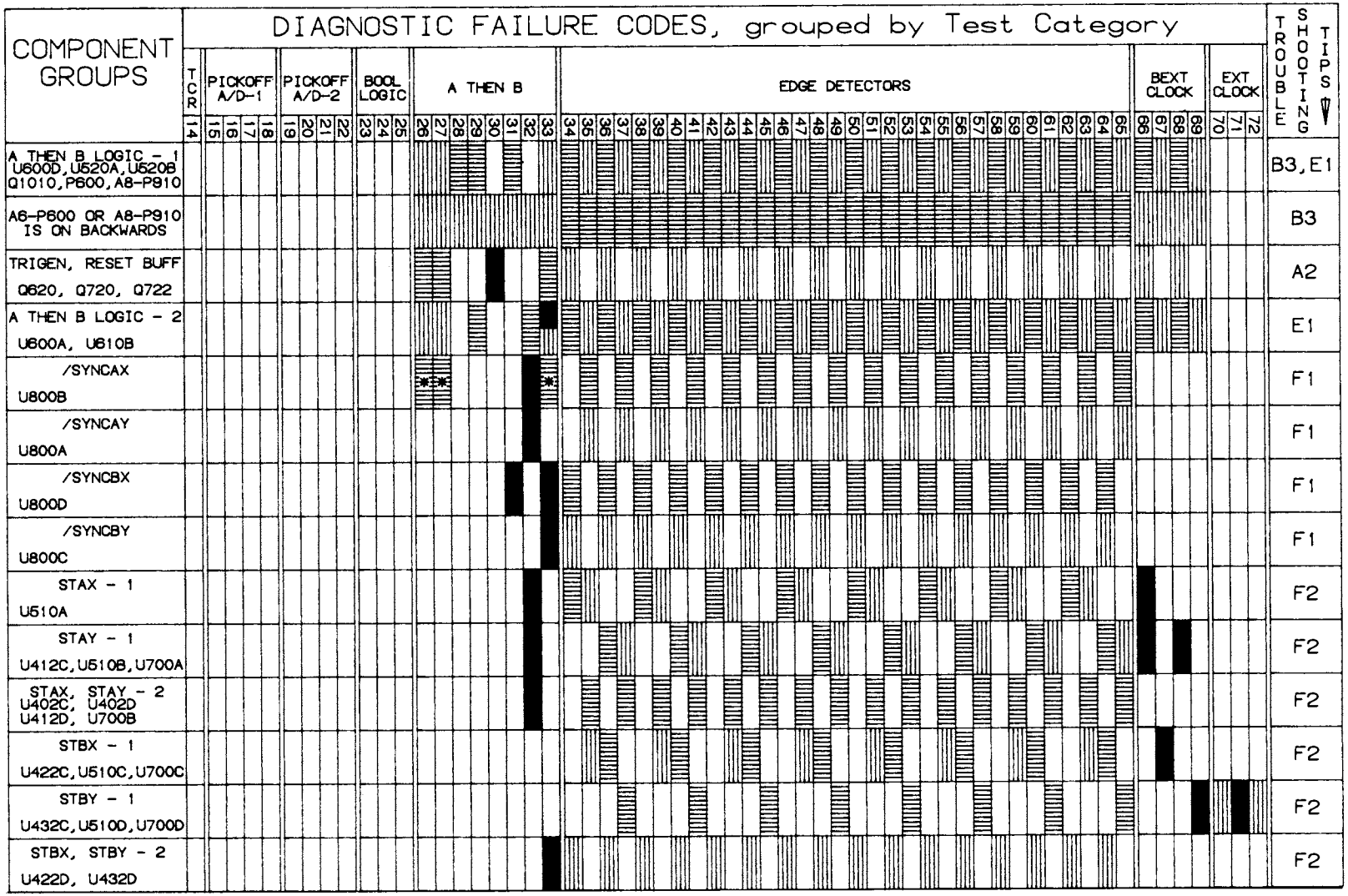
Trigger Diagnostic Test	Reports Codes
Trigger Control Register	14
Trigger Pickoff A/D	15 - 22
Boolean Logic	23 - 25
A THEN B	26 - 33
Edge Detectors and Buffered Ext Clk	34 - 69
External Clock	70 - 72

3. Refer to the following Trigger Diagnostic Charts to determine the component group or groups where the fault probably exists. The last column on the charts contains a reference to a particular troubleshooting procedure which can be found in the part entitled A6 Trigger Board Troubleshooting Tips. For each identified component group, perform the recommended troubleshooting procedure.

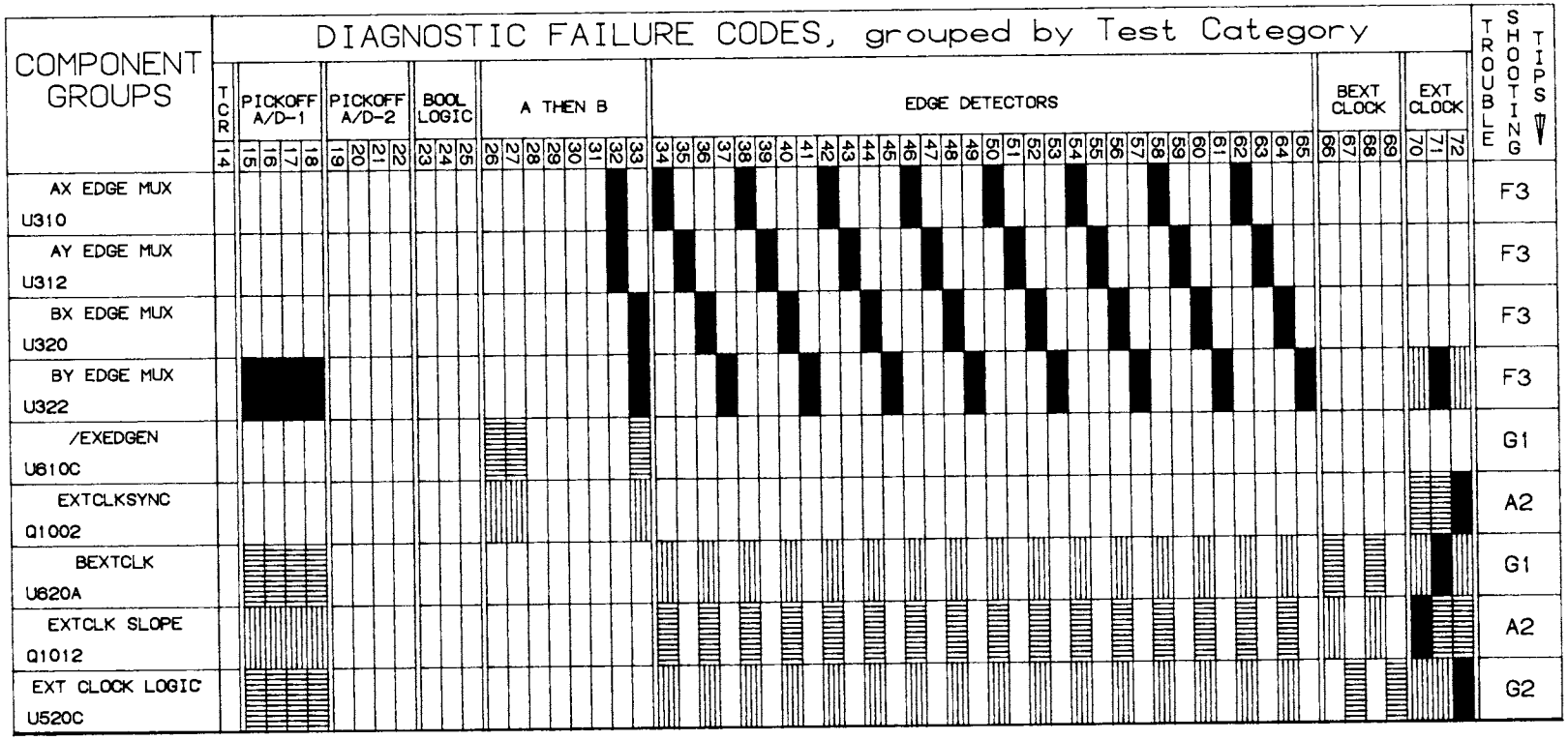




*This shading is valid only with the Trigger Filter Control in the on position.



*This shading is valid only with the Trigger Filter Control in the on position.



TROUBLESHOOTING TIPS FOR THE TRIGGER BOARD

These troubleshooting tips assist service personnel in isolating specific component failures on the A6 Trigger Board. The tips are organized by functional groups of circuitry. The identification codes (A2, D5, etc) are used in the Trigger Diagnostic Charts to refer to information in this section. There is no relation between these codes and similar ones used elsewhere in this manual (Checks and Adjustments, for example).

To perform most A6 Trigger Board troubleshooting, the board will have to be extended from the instrument. However, if trigger failure codes are indicated, before removing the board check that all the cable connections between boards are fully engaged. Pay particular attention to the four ribbon wires connecting the A4 Attenuator Control Board to the back of the A6 Trigger Board. If the Troubleshooting Procedure requires access to individual components, use the instructions given in Extending Circuit Boards For Troubleshooting, which is located in the Extended Diagnostics part of this section, just after Background Information On Signature Analysis. The Trigger Board input terminations should be installed in place of the cables from the A4 Attenuator Control Board.

When signature analysis is used to troubleshoot the ECL sections of the trigger circuitry, the 7A42 Signature Analyzer TTL to ECL Converter (Tektronix Part 670-8210-00) is needed to translate the SA start, stop, and clock signals from TTL levels to ECL levels. This converter is part of the 067-1112-00 7A42 Service Kit. Connect the converter to the A8 MPU Board as shown in Figure 3-17. The signature analyzer control probe then connects to the square-pin outputs on the Converter Board. Set the signature analyzer thresholds to ECL levels. If your signature analyzer will accept mixed logic families, set the control probe to TTL levels (connect it directly to the A8 MPU Board), and set the data probe to ECL levels. The 670-8210-00 is then unnecessary.

TRIGGER CONTROL LOGIC

A1. Trigger Control (WRMD) Latch, A6U1010

NOTE

If failure code 09 (Wait State Generator) has been reported, the lack of wait states could cause the Trigger Control Latch to malfunction. Refer to Test #9, Wait State Generator, in FAILURE CODES AND DESCRIPTION OF SELF-TESTS in this section.

a. The XBUSX diagnostic is useful for pinpointing problems with latch A6U1010. Refer to the External Bus Exercise procedure in the part entitled What to Do If The 7A42 Does Not Respond to Front-Panel Controls to start this diagnostic. Use an oscilloscope triggered on the negative transition of STR (from the A8 MPU Board) to probe U1010. A "walking zero" should be observed at the U1010 outputs in the pin sequence: 2, 5, 6, 9, 12, 15, 16, and 19. If this is found, U1010 is working properly; then perform the procedure given in A2, which follows.

b. While still running the XBUSX diagnostic, trigger the oscilloscope on the positive transition of the $\overline{\text{WRMD}}$ signal (TP1000 on the Trigger Board). If the oscilloscope will not trigger, the $\overline{\text{WRMD}}$ signal is probably not reaching the Trigger Board. If the oscilloscope triggers properly, compare the inputs and outputs of the latch for each data bit to verify that they are at the same level for several hundred microseconds after the positive transition of $\overline{\text{WRMD}}$. For example, the input pin 3 should match the output pin 2 during this time. The Data line should be low on every eighth trace. If an input and its corresponding output do not match, U1010 is defective. If the data line does not go low every eighth time the oscilloscope triggers, the Filtered Data Bus could be bad.

c. Probe both sides of resistors R200, R201, and R202 while still triggering as in part b. Verify that each data line on both the Filtered Data Bus (FD0-FD7) and the Buffered Data Bus (BD0-BD7) sides of the resistors goes low every eighth time the oscilloscope triggers. If the correct bus signals are not reaching the A6 Trigger Board, the A3 Interconnect Board may have a defect. Trace the signal from its source on the A8 MPU Board.

A2. Trigger Control Level Shifting Transistors, Reset Buffer

While running the XBUSX diagnostic as described in A1, part a, use an oscilloscope to trace the suspected trigger control lines from their sources at U1010 through the appropriate resistors and transistors. Verify that the outputs of these level shifters are reasonable ECL levels, (-0.6V > high > -1.0V; -1.5V > low > -5.2V). The Reset Buffer can be checked in the same way.

A3. Trigger Control Shift Registers

Start the Trigger Control Register diagnostic test (code 14). With an oscilloscope, verify that the $\overline{\text{WRTL}}$ signal is reaching the A6 Trigger Board and has acceptable TTL levels. Use a signature analyzer to trace the problem. Refer to SA Test #14, Starting Point #1.

TRIGGER INTERCONNECT

B1. Trigger Test Bit Interconnect

The diagnostic tests rely on test bits from the A6 Trigger Board which feed back to the A8 MPU Board. Test bits TB2, TB3, TB4, and TB5 pass through the edge connector, through the A3 Interconnect Board, and

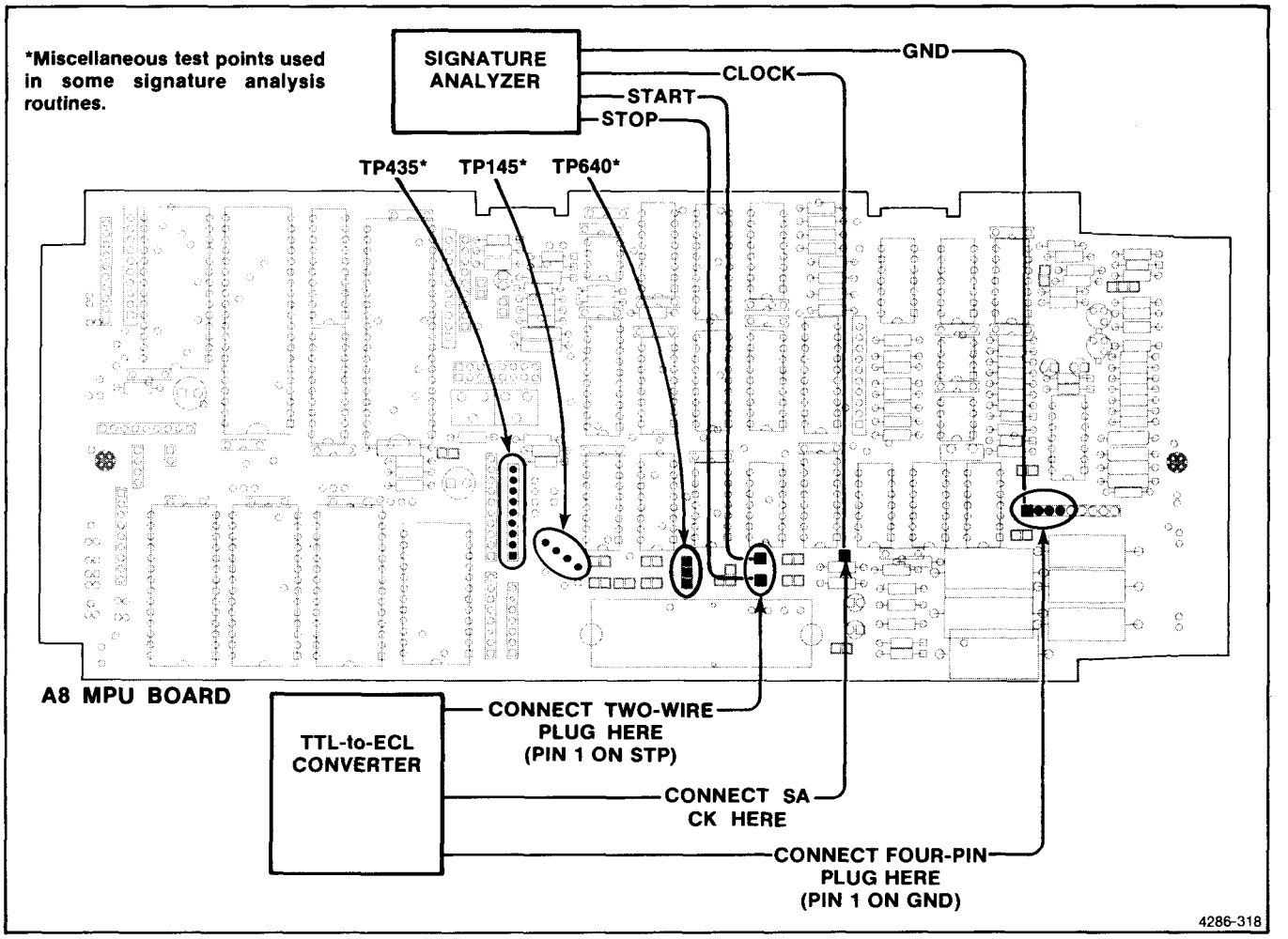


Figure 3-17. How to connect a signature analyzer or the 7A42 Signature Analyzer TTL-to-ECL Converter to the A8 MPU Board.

finally through the A8 MPU Board's edge connector. Trace suspect signals from their sources to their destinations with an ohmmeter.

B2. Trigger Filter Interconnect

The interconnect between the trigger filter current sources and the front-panel control passes through the A6 Trigger Board edge connector, the A3 Interconnect Board to J200, then a gray ribbon cable to the A2 LED Board entering at J340. Check that these connectors are installed properly and are fully engaged. If the trouble persists, use a DVM to measure the voltage at the end of R234 closest to C234. If this voltage reads about -5 V regardless of the position of the front-panel TRIGGER FILTER control, some point in the interconnect to the potentiometer R39, or perhaps R39 itself, is open. Connect the DVM to the end of R901 nearest the back edge of the A6 Trigger Board. If this voltage reads +5 V regardless of the setting of the TRIGGER FILTER control (off position or not), something in the connection to S39, or S39 itself, is bad.

B3. A Then B Gate Output Cable

Test bit TB0 reaches the A8 MPU Board through the three-conductor ribbon cable from P600 (Trigger) to P910 (MPU). Check that there are no open conductors and that the cable is not installed backwards on either end. The signals on pin 1 and 3 should be about 200 mV p-p amplitude with a dc offset of about -1.4 V.

THRESHOLD DACS AND COMPARATORS

C1. Threshold DACs

Before extending the A6 Trigger Board, check the integrity of the four ribbon wire connections between the A4 Attenuator Control Board and the back of the A6 Trigger Board. If these cable connections look good, remove the A6 Trigger Board but do not reinstall it in its extended position. An improper output voltage level from any of the attenuators could cause the same failure code indications as a defective threshold DAC. Check that with the channel inputs grounded and instrument power turned on, the voltages at pins 1 and 3 of each of the three-conductor ribbon wires from the A4 Attenuator

Control Board are within a few millivolts of ground. After checking this, install the A6 Trigger Board in its extended position and install the four input Terminations (317-0201-03) rather than the cables from the A4 Attenuator Control Board.

If the attenuator trigger output voltage levels were not correct, refer to the section entitled Troubleshooting Circuits Not Covered by Diagnostics for a procedure to further identify the problem.

Start the Threshold DAC Ramp exercise by pushing the "A" button. Set an oscilloscope to trigger on the positive transition of the STR signal (available on the A8 MPU Board square pin). The Channel 1 through Channel 4 threshold DACs should have repetitive ramp signals on each of their outputs. The ramps are 90 degrees out of phase from each other to allow detection of shorts between them. At the DAC outputs (pin 16) the ramps should start at zero volts and go to +2.55 V. Verify that the ramps also pass through the resistive level shifters to the comparator inputs. At pin 3 of each comparator, the levels should ramp from -0.48 V to +0.48 V.

If a DAC output signal is not moving, probe the appropriate write signal ($\overline{\text{TRSH1}}$, $\overline{\text{TRSH2}}$, etc.) to verify that the DAC is receiving data. If the output signal is nonlinear, check that all the data inputs are reaching the DAC and that its output is not shorted to another line on the board.

C2. Threshold Comparators

While running the circuit exercise from C1, probe the comparator outputs. Each comparator should switch when its input ramp reaches the midpoint. The comparators have complementary outputs; check that both outputs are switching and are opposite polarities.

BOOLEAN LOGIC AND TRIGGER FILTERS

D1. Boolean Logic

a. Start the Boolean Logic diagnostic test (code 23). A bad gate or connection in this circuitry can be found using signature analysis. Set the data and control probe thresholds to ECL levels. Connect the SA start, stop and clock inputs through the 7A42 Signature Analysis TTL-to-ECL Converter (Tektronix Part 670-8210-00) to the square pins marked STR, STP, and SACK, respectively, on the A8 MPU Board. Set all control inputs for positive transitions. Use SA Test #23, Starting Point #1. If bad signatures are found at both nodes in Starting Point #1, the problem is likely to be in circuitry on which the Boolean Logic depends (Trigger Control, Comparators, etc.). Double-check the indicated failure codes to see if this is possible.

   Spot checking with an oscilloscope, all inputs and outputs of the gates in the Boolean Logic section and U500A, U500D, U530A, U530D of the Trigger Filters should be moving (going high and low) during this test. The only exception is pin 9 of the 10113 gates, an enable connected to -2 V. This check may aid in isolating a bad gate. Pay particular attention to the logic levels at the gate inputs driven by the TTL-to-ECL resistive level shifter networks. These voltages should be valid ECL logic levels. If the problem seems to originate at the output of gates U500A or U530A, refer to the procedure in D3, which follows.

b. If the fault appears to originate at a wire-AND junction such as pin 2 of U400, it can be difficult to determine exactly which gate is bad. The easiest way is to reconfigure the 7A42 into normal operating mode, then enter specific trigger functions that exercise the paths through each of the suspected gates. Input signals to the A6 Trigger Board can be supplied through the attenuator if the extra-length cables are installed in place of the trigger input terminations.

c. If the wire-AND node appears to be stuck in a high state no matter what trigger function is programmed, a temporarily applied short circuit can usually "smoke out" the bad part. Reinstall the trigger input terminations if they have been removed. Adjust each channel's switching threshold to the maximum negative level (- 0.254 V or -1.27 V depending on the selected logic family). Enter the following trigger function into *both* function A and function B (all LEDs in both columns lit red):

   CH1 AND CH2 AND CH3 AND CH4 OR
   CH1 AND CH2 AND CH3 AND CH4

   With this trigger function all the wire-AND junctions should be in the low state. If the suspected one is still high, make a temporary connection between that wire-AND node and the -2 V test point TP802 while constantly feeling the the cases of ICs U400, U410, U420, and U430. The part that is trying to pull high will heat up and give itself away. Remove the short immediately as soon as this heating is detected and replace the bad component.

D2. Trigger Filters

a. All the gates in the trigger filter circuit can be checked with SA Test #23, Starting Point #2. If the problem seems to be at the output of U500A or U530A, refer to part D3. There are two wire-OR junctions that need special consideration if the source of the fault originates there.

b. The wire-OR junction at the output of U402A and U412A also includes the outputs of U520D and U600A. If the wire-OR node is stuck high (never goes low), proceed as follows: U520D should not be pulling high because its pin 10 input is held high

during this test. Verify this level at pin 10 of U520. If pins 6 and 7 of U520 are shorted together the pin 5 input of gate U600A will be held low, which should release its influence on the wire-OR node. If the wire-OR is still stuck high, pull pin 5 of U402A and pin 5 of U412A to the high state by connecting them to ground through a signal diode (such as Tektronix Part 152-0141-02). The anode should go to ground; the cathode goes to the gate inputs. If the wire-OR node is still high, temporarily short it to -2 V while constantly feeling the cases of U402, U412, U520 and U600. The package that heats up is the one with an output stuck high. Replace the part and remove all temporary connections made in this procedure.

c. If the wire-OR junction at the output of U402A, etc., is moving up and down during the Boolean Logic diagnostic but has a wrong signature, one of the gate inputs or outputs is probably open. The easiest way to isolate the faulty gate is to connect an oscilloscope probe to the wire-OR junction. Watch the oscilloscope trace while temporarily forcing each gate's output to the high state by overriding its inputs. Overriding the bad gate's inputs will not force the wire-OR junction to a steady high level. To override the inputs of U402A, U412A, or U520D, temporarily (for just a fraction of a second at a time) short both inputs to -2 V. If the short is applied indefinitely, permanent damage could occur to any other gates trying to drive these inputs high. An override of very short duration is not destructive. The output of U600A can be forced to the high state with no risk of damage by simply pulling its pin 5 input to the high state through a diode, as described in part b.

d. The wire-OR junction at the outputs of U422A and U432A is easier to troubleshoot because only those two gates drive it. Use the methods outlined in parts b and c above to isolate the problem.

D3. Trigger Filter Current Sources

a. Be certain that the trigger filter interconnect is functioning properly, as described in B2. The function A and function B filter circuits are identical; a procedure to fix function A's filter applies to function B as well. With a DVM, check that pins 3, 7, 10, and 13 of Q532 are connected to the -5 V supply. With the trigger filter turned on, the voltage at pins 2, 4, 6, 8, 9 and 12 of Q532 should be about 0.7 V more positive than the -5 V supply. The voltages on pins 1, 5, 11, and 14 should be about -2 V or greater and moving high and low with the gate outputs to which they are connected.

b. If the output of U500A at pin 2 appears stuck in the high state, it could be the fault of the gate or the lack of any pull-down current from Q532. To check the gate, temporarily connect a resistor in the 100 to 1000 ohm range from pin 2 of U500A to the -2 V supply. If the gate output then goes high and low while the Boolean Logic diagnostic is running, the gate is good; replace Q532. If the gate output is still stuck, replace U500A.

c. It is possible that the trigger filter current sources could fail in some way that the diagnostics cannot detect. If one of the collectors of Q532 attached to pin 2 of U500A were internally open, the current source would function at only half the correct magnitude. Each collector supplies an equal contribution to the current drawn from pin 2. The symptoms of this problem are excessive trigger filter range. The minimum filter time would not meet specifications and the maximum filter time would be about twice its normal value. If this situation occurs, replace Q532.

A THEN B LOGIC

E1. A Then B Logic

The A Then B logic circuitry can be troubleshot using the A Then B diagnostic as a circuit exercise. The test consists of setting and resetting A Then B latch U600A by various means. Read the descriptions of tests 26 through 33, in A6 Trigger Board Test Descriptions, for a description of the test.

Figure 3-18 is a timing diagram of the sequence of events with the active signals identified. An oscilloscope triggered on the positive transition of STR (from the A8 MPU Board) can be used to verify the actual circuit timing. The important thing is the relationship of the signal transitions relative to each other rather than the exact width or period of the pulses.

If the oscilloscope display is not stable enough to show the transitions distinctly, proceed as follows:

a. Install a jumper on the $\overline{\text{RTI}}$ pins, which are located at the rear of the A8 MPU Board behind the A9 Power Supply Board. To gain access, you must first remove the screws that retain the rear of the A9 Power Supply Board and loosen the two screws that fasten the post that supports the front of the board in order to swing the A9 Power Supply Board outward.

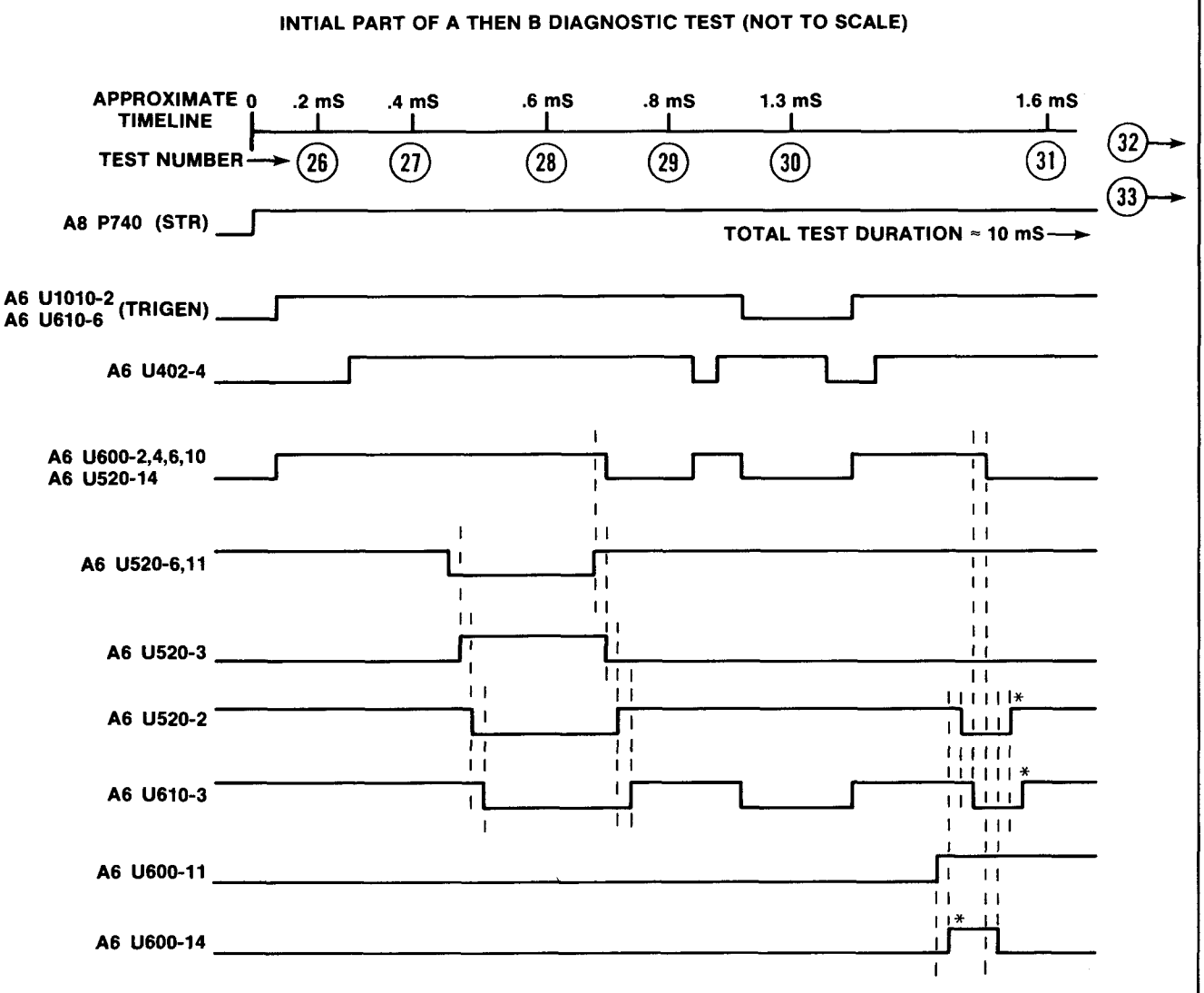
b. Disconnect the gray ribbon cable that connects P320 of the A5 Amplifier Board to P1010 of the A7 Digital Board.

Use the A Then B diagnostic test (code 26) to verify the waveforms in Figure 3-18.

EDGE DETECTORS

F1. $\overline{\text{SYNC}}$ Control Lines

Start the Boolean Logic diagnostic test (code 23). U800 can be tested with signature analysis using SA Test #23,



This diagram shows the operation of key gates during the first part of the A Then B diagnostic test. The entire test takes about 10 ms. Only the first 1.6 ms are shown here; the last two tests performed in the remaining 8.4 ms require loading additional trigger information and would not make a meaningful display.

Although not drawn to scale, an approximate time-line is given to help identify the test events. The times where the test bits are sampled for tests 26 through 31 are shown. The A Then B test starts when STR goes high; use STR to trigger the oscilloscope.

To show the time dependence of signals, dashed lines indicate transition times that are shifted by the propagation delays of gates. At a sweep speed of 0.2 ms/division, these transitions will appear time-coincident. The pulses marked with asterisks (*) are formed entirely by gate propagation delays and are very narrow. A fast delayed sweep and a viewing hood will probably be necessary to see them.

4286-319

Figure 3-18. Timing of waveforms in A Then B Logic test.

Starting Point List #3. Because the $\overline{\text{SYNC}}$ lines are static control lines, an alternate way to test them is to reconfigure the 7A42 to normal operating mode. Refer to Tables 3-7 and 3-8 for the link-plug jumper locations to do this. (Tables 3-7 and 3-8 are located in What to Do if The 7A42 Does Not Respond to Front-Panel Controls in this section.) While monitoring the U800 outputs, program the 7A42 with the necessary trigger functions to exercise the U800 inputs. The $\overline{\text{MEN}}$ lines can be controlled by entering an edge-sensitive channel into the associated product of the trigger function. For example, an edge-sensitive channel in the second product (column) of function A will drive $\overline{\text{MENAY}}$ low. The $\overline{\text{EXEDGEN}}$ line is driven low when the EXT CLOCK SYNC button is lit.

F2. Edge-Detector Circuits

a. Start the Boolean Logic diagnostic test (code 23) to test U700 with signature analysis. Use SA Test #23, Starting Point #4. The signatures that occur with the TRIGGER FILTER control in the on and off positions are listed.

b. Start the Trigger Control diagnostic test (code 14) to test U510 with signature analysis. Use SA Test #14, Starting Point #2.

c. The Edge-Detector circuits can be checked with an oscilloscope. Start the Edge Detector diagnostic test (code 34) to exercise the Edge-Detector circuits. To test the circuit associated with the first product in function A, set the oscilloscope to trigger on the negative transition of the pin 15 output of multiplexer U310. Check that the pin 15 output of U402D produces the strobe signal STAX. The STAX signal should be about 4 or 5 nanoseconds in width and occur immediately after the negative transition at U310 pin 15. There will be an occasional negative transition at U310 pin 15 for which no strobe is generated; this is normal. The repetition rate of the signals is low so a viewing hood may be needed to see the signals. Use low-capacitance probes to prevent degradation of the high-speed signals.

F3. Multiplexers

Start the Boolean Logic diagnostic test and use signature analysis to check the multiplexers U310, U312, U320, and U322. The proper signatures are listed in Signature Test #23, Starting Point #5. If an incorrect signature appears at any multiplexer data input, select, or enable, the problem lies further upstream. If the output pin 15 is held high, check U510 (see F2, part b).

EXTERNAL CLOCK

G1. Clock Control Lines

a. Configure the 7A42 in normal operating mode; refer to Table 3-7 for the proper link-plug jumper positions. The $\overline{\text{EXEDGEN}}$ signal can be controlled through two paths. First push the EXT CLOCK SYNC button (lit) to see that the signal goes low. Press the EXT CLOCK SYNC button again (light now out). The signal should return to the high state. Now apply a dc voltage from 1 to 5 volts to the center conductor of J700 on the A6 Trigger Board. The $\overline{\text{EXEDGEN}}$ signal should go low during this time.

G2. External Clock Logic

Configure the 7A42 in normal operating mode; refer to Table 3-7 for the proper link-plug jumper positions. Place the EXT CLOCK jumper, located on the bottom edge of the A6 Trigger Board, in the ECL position. Push the EXT CLOCK SYNC button (key lit) to enable U520C. Check the levels at the output of U520C (pin 9) while momentarily shorting the two pins of P632 on the A6 Trigger Board. (This shorts the EXT CLOCK INPUT connector.) When the pins are shorted, U520 pin 9 should be high.

TRIGGER BOARD TEST DESCRIPTIONS

TRIGGER CONTROL

14—Trigger Control Register

A pseudo-random bit string is shifted through the 48-cell Trigger Control Shift Register and sampled by the processor at TB5.

15—Trigger Pickoff A/D-1

An A/D conversion is performed on the output voltage of the CH1 trigger pickoff. The feedback path to the processor is through the B-Y Edge Multiplexer and TB2.

16—Trigger Pickoff A/D-1

An A/D conversion is performed on the output voltage of the CH2 trigger pickoff. The feedback path to the processor is through the B-Y Edge Multiplexer and TB2.

17—Trigger Pickoff A/D-1

An A/D conversion is performed on the output voltage of the CH3 trigger pickoff. The feedback path to the processor is through the B-Y Edge Multiplexer and TB2.

18—Trigger Pickoff A/D-1

An A/D conversion is performed on the output voltage of the CH4 trigger pickoff. The feedback path to the processor is through the B-Y Edge Multiplexer and TB2.

19—Trigger Pickoff A/D-2

An A/D conversion is performed on the output voltage of the CH1 trigger pickoff. The feedback path to the processor is through the "AX" section of the Boolean Logic to TB3. This test is performed only if Error Code 15, 16, 17, or 18 has occurred.

20—Trigger Pickoff A/D-2

An A/D conversion is performed on the output voltage of the CH2 trigger pickoff. The feedback path to the processor is through the "AX" section of the Boolean Logic to TB3. This test is performed only if Error Code 15, 16, 17, or 18 has occurred.

21—Trigger Pickoff A/D-2

An A/D conversion is performed on the output voltage of the CH3 trigger pickoff. The feedback path to the processor is through the "AX" section of the Boolean Logic to TB3. This test is performed only if Error Code 15, 16, 17, or 18 has occurred.

22—Trigger Pickoff A/D-2

An A/D conversion is performed on the output voltage of the CH4 trigger pickoff. The feedback path to the processor is through the "AX" section of the Boolean Logic to TB3. This test is performed only if Error Code 15, 16, 17, or 18 has occurred.

23—Boolean Logic-Function A

Pseudo-random data is written to the Boolean Logic Section and to the Trigger Threshold DACs via the Trigger Control shift register. The firmware signatures TB3, which is the result of shifting data through the AX and AY sections of the boolean logic.

24—Boolean Logic-Function B

Pseudo-random data is written to the Boolean Logic Section and to the Trigger Threshold DACs via the Trigger Control shift register. The firmware signatures TB4, which is the result of shifting data through the BX and BY sections of the boolean logic.

25—Boolean Logic-TCR

A pseudo-random bit string is shifted through the 48-cell Trigger Control Shift Register and sampled by the processor at TB5.

26—A Then B Logic

The output of the A Then B latch should follow the output of the CH1 Trigger Comparator, which is channeled through the AX section of the Boolean Logic. The result of the test may depend on the front-panel Trigger Filter control if there is a failure in the A Filter Logic.

27—A Then B Logic

This test is an extension of test #26; it checks that the A Then B latch remains set when FNA is set low.

28—A Then B Logic

The A Then B latch should be set from the previous test. This test checks part of the reset circuitry by asserting a high on the A Then B line. The reset circuitry forces TB0 low; this check verifies that condition.

29—A Then B Logic

Continuation of the previous test. The A Then B line is set high with FNA low. The latch resets and TB0 is checked to verify that it is low.

30—A Then B Logic

The A Then B latch is set using the same path as in test #26. The Function A (FNA) line is then set low, and the latch is reset by setting TRIGEN low.

31—A Then B Logic

The A Then B latch is set using the same path as in test #26. FNB is set high via the Ch 2 Trigger Threshold DAC, Ch 2 comparator, and BX Boolean logic. This should reset the A Then B latch and cause a low on the TB0 line.

32—A Then B Logic

This test loads the trigger function; AX=CH1*CH4∧, AY=CH2*CH4∧. With CH1 and CH2 high, but no CH4 positive transition, the A Then B latch should not be set. That is, this test checks to see that STAX and STAY qualify FNA.

33—A Then B Logic

First the A Then B latch is set through the path used in test #26. With the following trigger function; AX=C1, AY=off, BX=CH2*CH4∧, BY=CH3*CH4∧, and the Trigger Threshold DACs such that CH1=0, CH2=1, CH3=1, CH4=no transition, STBX and STBY should prevent FNB from going high. TB0 is checked to see that the latch is not reset.

34-65—Edge Detectors

In these tests the A Then B latch is repeatedly set and reset using all possible combinations of channels and their complements through each of the products AX, AY, BX, and BY. Table 3-11 relates the failure code to the channel and product being used to set and reset the latch.

66—Buffered External Clock

The following trigger function is loaded; AX=$\overline{\text{CH1}}$, BX=CH1 and CH1 is set high. External Clock is activated by a high on the Ext Clk Sync line. Using EXT CLK EXER (external clock exercise), the latch is set. If TB0 is low, a failure is indicated.

67—Buffered External Clock

The A Then B latch should remain set if test #66 passed. Using the same trigger function as in test #66, and CH1 set low, this test attempts to reset the latch using EXT CLK EXER. If TB0 remains high a failure is indicated.

68—Buffered External Clock

The following trigger function is loaded; AY=$\overline{\text{CH1}}$, BY=CH1 and CH1 is set high. Using EXT CLK EXER

TABLE 3-11
Failure Codes, Sets, And Resets For Edge Detectors

Failure Code	Set		Reset		Comment
	AX	AY	BX	BY	
34	1↑				Set through U310 pin 14
35			3↑		Reset through U320 pin 12
36		2↑			
37				4↑	
38	2↑				Note: ↑ means positive transition
39			4↑		↓ means negative transition
40		3↑			
41				1↑	
42	3↑				
43			1↑		
44		4↑			
45				2↑	
46	4↑				
47			2↑		
48		1↑			
49				3↑	
50	1↓				Negative transitions start here
51			3↓		
52		2↓			
53				4↓	
54	2↓				
55			4↓		
56		3↓			
57				1↓	
58	3↓				
59			1↓		
60		4↓			
61				2↓	
62	4↓				
63			2↓		
64		1↓			
65				3↓	

(external clock exercise), the latch is set. If TB0 is low, a failure is indicated.

69—Buffered External Clock

The A Then B latch should remain set if test 68 passed. Using the same trigger function as in test 68, and CH1 set low, this test attempts to reset the latch using EXT CLK EXER. If TB0 remains high a failure is indicated.

70—External Clock

The control lines are set to allow the BEXTCLK signal to be monitored via TB2. For this test, EXT CLK EXER=1, EXT CLK SYNC=0, and EXT CLK SLOPE=1. This should result in TB2 being equal to 0; if not, a failure is indicated.

71—External Clock

The control lines are set to allow the BEXTCLK signal to be monitored via TB2. For this test, EXT CLK EXER=1, EXT CLK SYNC=0, EXT CLK SLOPE=0. This should result in TB2 being equal to 1; if not, a failure is indicated.

72—External Clock

The control lines are set to allow the BEXTCLK signal to be monitored via TB2. For this test, EXT CLK EXER=1, EXT CLK SYNC=1, EXT CLK SLOPE=0. If this test passes, TB2 will be 0.

TROUBLESHOOTING CIRCUITS NOT COVERED BY DIAGNOSTICS

MAINFRAME SUPPLY CURRENT LIMITED

If the 7A42 is overloading the host mainframe power supply, the mainframe supply will cycle in current-limit mode until the fault is removed. The mainframe will repetitively power up and then shut down with a frequency of about 1 Hz.

If the overload is of low enough impedance, it may be possible to probe the supplies with an oscilloscope and determine which supply is shorted. Higher resistance shorts will dissipate power and may be detected by temperature rise.

Perform the following setup to determine whether the fault path is through the left or right side of the 7A42.

Turn off the host mainframe and place the 7A42 on a flexible extender (Tektronix Part 067-0616-00), connecting only the right side of the 7A42 (the A8 MPU Board).

CAUTION

The H842 channel switches on the A5 Amplifier Board require that both +5 Va and -5 Va be present simultaneously to avoid possible damage.

Therefore, when connecting only the right side of the 7A42 to the mainframe interface, and when +5 Va is not available to the channel switches, P600 must be disconnected from the A5 Amplifier Board to eliminate -5 Va.

Turn on the host mainframe. If the supplies come up normally, assume the fault is upstream from the left interconnect.

If under these conditions the mainframe is still in current limit, circuit boards may be disconnected from the A3 Interconnect Board in various combinations to further isolate the problem. The A9 Power Supply Board may also be disconnected from the A8 MPU Board by disconnecting two ribbon cables.

7A42 +5 V_D, -2 V_D, -5 V_D Failures

CAUTION

Use caution when troubleshooting the 7A42 power supply. Permanent damage to the power stage could result if component leads or IC pins are momentarily shorted together, or to ground.

These supplies may fail due to overload conditions at the supply outputs, which will force current-limit to cycle, or may fail because of a failure on the A9 Power Supply Board.

If the waveform at pin 9 of A9 U210 is similar to the waveform shown on diagram 11 (opposite the schematic), the majority of the supply is probably good and the problem is most likely a shorted secondary. The short can be anywhere downstream from the transformer secondaries. Boards may be disconnected from the A3 Interconnect Board to isolate the problem to the board level.

To aid troubleshooting, the A9 Power Supply Board can be run with external loads. Disconnect the eight-wire ribbon cable between A8 and A9 which connects to the supply outputs, then connect the following resistors to the supply outputs to approximate the typical load. +5 Vd : 5 ohms-5W min; -2 Vd : 4 ohms-1W min, -5 Vd : 4 ohms-7W min. Connections can most easily be made to the output side of filter inductors L420, L530, and L640.

The primary current-limit point is adjustable; if set too low, the current-limit may cause erroneous indications of fault.

AMPLIFIER BOARD

Most problems on this board can be found by comparing the dc voltages given on the schematic to measured values. Some typical problems and their symptoms are listed here.

No position control—single trace at center screen.

No readout on screen—check P500, P600, P320, and J100 connections.

Any position control affects more than one trace—check for shorts in P320 interconnect.

TRIGGER BOARD

The 7A42 internal diagnostics can detect problems on most, but not all, of the A6 Trigger Board. For those circuits in which the diagnostics cannot detect faults, the diagnostic routines can be used as circuit exercises to aid troubleshooting.

Trigger Out to Mainframe

If the Trig Out signals from pins A13 and B13 of the A5 Amplifier Board are missing or are too small, check that the three-conductor cable from P610 on the back of the A6 Trigger Board to P230 on the back of the A5 Amplifier Board is fully engaged with both connectors. Invoke the Boolean Logic diagnostic test to exercise the trigger output. The differential signal reaching the A5 Amplifier Board should be about 500 mV p-p between sides with a common-mode offset of about -1.3 V. The buffer stage on the A5 Amplifier Board changes the signal to about 300 mV p-p with zero offset. If there is no signal at the input of the A5 Amplifier Board, put the A6 Trigger Board on an extender and check the source of that signal at A6P610. If the problem still exists, invoke the Boolean Logic diagnostic test. Use SA Test 23, Starting Point #6 (U610D), and trace the signal with a signature analyzer.

Trigger View Output

If the Trig View Out to A5 Amplifier Board signal is missing or is too small, check that the ribbon cable that connects between P630 of the A6 Trigger Board and P560 of the A5 Amplifier Board. Check that, when the TRIG VIEW button is lit, pin 6 of TP420 on the A5 Amplifier Board goes low. If the trigger view display is still absent, rotate A6R460, Trig View Position, through its range. When exercised with Boolean Logic diagnostic test (code 23), the input to P560 should be a differential signal of about 25 mV p-p with a common-mode offset of about -0.5 V (see diagram 3).

Use SA Test #23, Starting Point #7 (U620C) to trace to the source of the problem on the A6 Trigger Board with a signature analyzer.

Front Panel TRIGGER OUT

If there is no signal at the TRIGGER OUT connector, check that the coaxial cable from A6 J602 on the A6 Trigger Board to J49 on the front panel is properly installed at both ends. If an output exists but is not at the correct levels, compare voltages in the circuit with those shown on diagram 7.

Signature analysis can be used to verify the ECL gate driving the Trigger Out Buffer. Put link-plug jumper A6 J701 on the NORM position and refer to SA Test #23, Starting Point #8.

ATTENUATORS

The 7A42 input attenuators consist of active and passive circuitry on a ceramic hybrid substrate which is not serviceable by the Tektronix Field Service Centers or by customers. If you suspect a problem with an attenuator, the voltages at the hybrid substrate pins can be measured with a DVM if the proper precautionary measures are taken. *The hybrid attenuator is a fragile component; be extremely careful to avoid damage.*

A symptom of an attenuator problem is an off-center trace, or one that cannot be positioned onto the screen. With no input, check the voltages at pins 1 and 13 of the associated amplifier IC (U1010, U1020, U1040, U1060 on A5 Amplifier Board). The voltages at these pins (see diagram 3) should be within a few millivolts of each other. If the pin 1 voltage is normal but the pin 13 voltage is abnormal, the attenuator is supplying an improper output level. Check the three-conductor ribbon cable that connects the back of the A4 Attenuator Control Board to the back of the A6 Trigger Board. If a connector is plugged on backward at either end, the displayed trace will be positioned off center. Try disconnecting this cable to see if the problem goes away.

If the voltage at pin 1 is not -5 V ±0.2 V, check the -5 V source at TP200 or TP400 on the A5 Amplifier Board. All the -5 V and -11 V supplies should be at nearly the same voltages for each channel.

If the -5 V and -11 V supplies are correct at the A5 Amplifier board, check that the gray ribbon cable that connects P320 on the A5 Amplifier Board to J600 on the A3 Interconnect Board is fully engaged. Also, check that the pins from the back of the A4 Attenuator Control Board are properly and fully inserted into the sockets of J700 on the A3 Interconnect Board. If the problem persists, remove the cover of the suspect attenuator module. Refer to "How to Remove and Replace Attenuator Modules," in this section, for the proper procedure. Figure 3-19 shows the pins that connect the attenuator substrate to the A4 Attenuator Control Board and the voltages that should exist on each pin, with no input signal. Use extreme care when probing the substrate. Use a clean, sharp probe and touch only the points where the pin is soldered to the substrate. To avoid scratching or cracking the substrate, take care not to touch the ceramic substrate. Be careful not to contaminate the interior of the attenuator with dust or moisture. If a supply voltage is not present on the substrate, trace the interconnect problem to the source. If all supply voltages are correct, but the input, trigger output, or signal output voltages are incorrect, the substrate is defective and the entire module must be replaced.

DIGITAL BOARD

Armature Relay Drive Circuitry

The armature relays in the Attenuator Modules make audible clicks when they transfer from one position to the other. Relay transfers occur in response to the

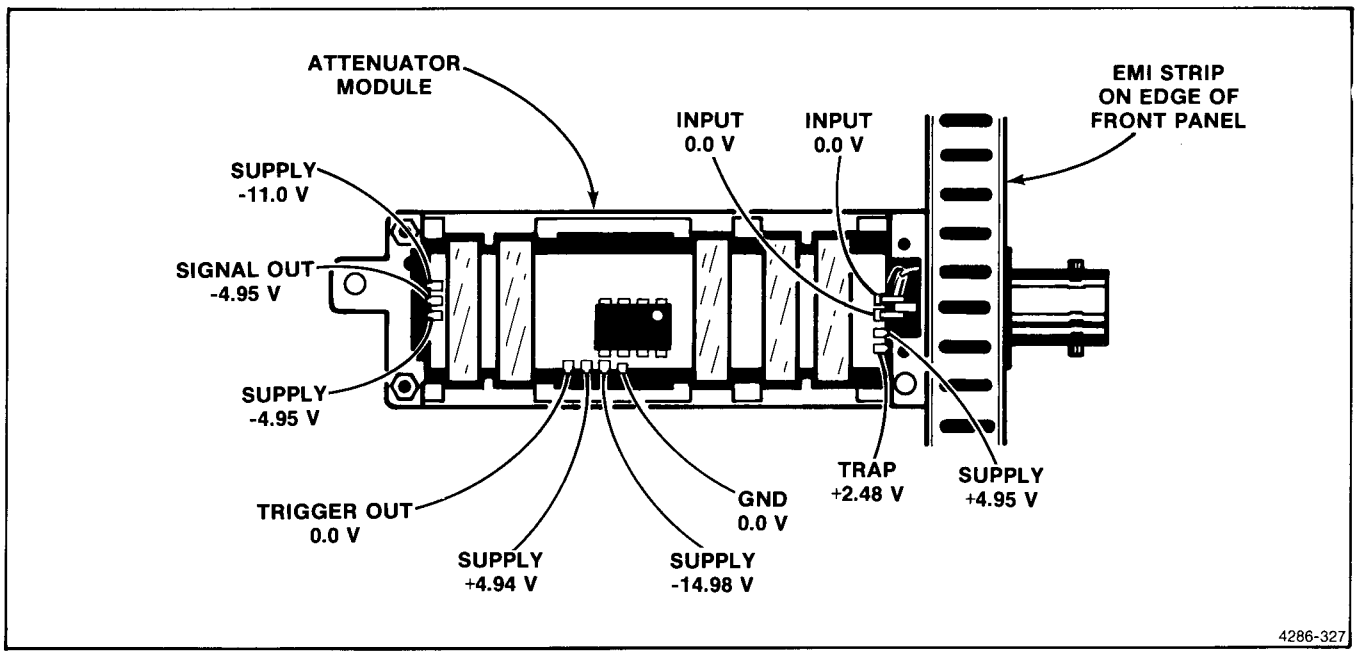


Figure 3-19. Voltages at 10 pins on attenuator module.

following front-panel key presses with the 7A42 in Program Channel mode:

1. When the TTL/ECL button is pressed,
2. When the upper or lower VOLTS/DIV button is pressed as long as the audible beep does not sound,
3. When the GND button is pressed while the associated channel's input impedance is 50 ohms, or
4. When the 1MΩ/50Ω button is pressed when the associated channel is ungrounded.

NOTE

If the GND button is pressed when the associated channel's input impedance is 1MΩ, the relays should click twice. If the 1MΩ/50Ω button is pressed when the associated channel is grounded, no click should occur.

Check each input channel for the above armature relay transfer (clicks). Do not confuse the sound of a relay transfer click with the sound the speaker makes when it acknowledges each keystroke. If there is any confusion, disable the speaker by installing the $\overline{\text{SPKR}}$ link-plug jumper A7P730. See Figure 3-8 for jumper location. Repeat each test several times.

If sometimes no click or an abnormal (weak sounding) click is heard, take note when that happens. If you fail to hear a distinct click in only one of the situations with only one channel, the problem probably lies in the Armature Relay itself. See Diagram 2 to identify the problem relay. Try exchanging the suspect relay with one of its neighbors which is known to function properly. Refer to "How to Remove and Replace Armature Relays," later in this section. If the problem changes locations with the suspect relay, replace it. If the problem remains in the same location, the steering diode(s) may be at fault. Remove the A4 Attenuator Control Board and check the steering diodes with an ohmmeter. Another indication of steering diode problems is that several relays attempt to transfer when only one should transfer (one will click distinctly and the others seem to clatter).

If multiple problems (lack of transfers) are found, it is unlikely that the Armature Relays have failed; there is likely a problem in the relay drive circuitry or the relay control lines between the A7 Digital Board and the relays. The failure pattern makes the following implications:

a. If the same problem appears in each channel, for instance situation 1 above (no transfer when the TTL/ECL button is pressed), the signal KPUD3, responsible for driving K13, K23, K33, and K43 should be investigated. This is the only signal common to these relays.

b. If all the relays in a particular channel (e.g., CH2), fail to operate (they may operate once but not repetitively), the signals KPU2 and KPD2 common to K12, K22, K32, K42, and K52 would be suspect.

c. If no relay transfers can be heard, the relay-drive circuitry is probably defective. Check that the RELN jumper is installed. See Figure 3-8 for jumper location.

Signature Analysis may be helpful in troubleshooting the relay-drive circuitry. Refer to SA Test #2, Starting Point #2 to trace the problem. If all the signatures in the starting point list are correct, check the 75325 driver ICs in normal operating mode with the set-up conditions listed opposite diagram 2. The voltages should be as shown on the schematic. By exercising the suspect relay-drive line, the problem should be found using conventional troubleshooting techniques.

Readout

The Self-Test and Extended Diagnostics can detect problems in parts of the Readout circuitry involving the timeslots, RST7.5 generator, and SID signal. However, the remainder of the Readout circuitry is not covered by Diagnostics. The Display Readout Characters circuit exercise can be helpful in troubleshooting a readout problem using signature analysis. If Extended Tests 12 or 13 fail, first troubleshoot the problem using the tips provided in Diagnostic Test Descriptions. If both tests 12 and 13 pass their Extended Tests, proceed with the steps below.

Select the Display Readout Characters circuit exercise from the Extended Test mode. If there are no readout characters on the crt, check the mainframe Readout controls for proper adjustment. If readout is displayed for another plug-in unit (for instance, the time base) but not the 7A42, the fault probably lies within the 7A42. See the Theory of Operation section for thorough description of the readout circuitry.

While the Display Readout Characters circuit exercise is executing, use signature analysis to check the readout circuits. Refer to SA Test #13, Starting Point #1.

If all the signatures in this starting point list are found to be correct, and the waveforms in the circuit match those shown opposite diagram 10, the problem must be in the reaodut DACs or the row and column interconnect to the mainframe. Most mainframes provide an internal test point where the row and column currents can be monitored; see the oscilloscope mainframe Service Manual for more information.

CALIBRATION AND TROUBLESHOOTING AIDS

The following exercises may be selected after the instrument has been powered up in Test mode. Also see Figure 3-4 (in the EXTENDED TESTS part of this section) for key functions in test mode.

ROM PART NUMBER (LEVEL ⇩ KEY)

When this key is pushed, a ROM number (1,2,3,4) followed by the last six digits of its Tektronix part number is displayed on the crt readout. (The first three digits of Tektronix IC part numbers are 160.) After a delay of about one second, the display advances to the next ROM. This continues until another test or exercise is selected. This exercise verifies that the correct ROMs (part type and firmware version) are installed.

FRONT-PANEL INTERACTIVE (LEVEL ⇧ KEY)

This exercise verifies that the front-panel keys are correctly recognized by the microprocessor. Each time a key is pushed, its associated code (see Table 3-12) is displayed on the crt readout and the SWITCHING THRESHOLD VOLTS display. Keys with LED backlighting are lit and then extinguished when the key is pushed. A front-panel LED will be lit for those keys without LED backlighting and will respond in the same manner. Table 3-12 lists the key, its code, and the corresponding front-panel LED. Pushing the "LEVEL⇧" key at any time will exit this exercise.

TABLE 3-12
Front-Panel Interactive Keys, Codes, and LEDs

Key	Code	Front-Panel LED
ALT/CHOP	0000	Back-lit
DISPLAY	0001	CH1 DISPLAY
VOLTS/DIV-upper	0002	TRIG. FUNC. COL2 CH1
VOLTS/DIV-lower	0003	TRIG. FUNC. COL2 CH2
GND	0004	CH1 GND
1MΩ/50Ω	0005	CH1 1M/50 OHM
CH1	0006	Back-lit
CH2	0007	Back-lit
CH3	0015	Back-lit
CH4	0014	Back-lit
TRIG VIEW	0008	Back-lit
TTL/ECL	0009	CH1 TTL/ECL
THRESH	0010	Back-lit
PROG	0011	Back-lit
CLEAR	0012	TRIG. FUNC. COL2 CH3
AND	0013	TRIG. FUNC. COL1 CH1
OR	0021	TRIG. FUNC. COL1 CH2
NOT	0023	TRIG. FUNC. COL1 CH3
EDGE	0022	TRIG. FUNC. COL1 CH4
EXT CLOCK SYNC	0020	Back-lit
Ext Clock Slope	0019	Back-lit
LEVEL ⇩	0024	TRIG. FUNC. COL2 CH4
LEVEL ⇧	0025	**EXIT EXERCISE**
PROBE OFFSET	0026	Back-lit
A	0027	Back-lit
B	0028	Back-lit
A THEN B	0029	Back-lit

SPEAKER CONTROL (PROBE OFFSET KEY)

When pressed, this key activates the piezo speaker-drive circuit. The speaker will continue to sound until the key is pushed again.

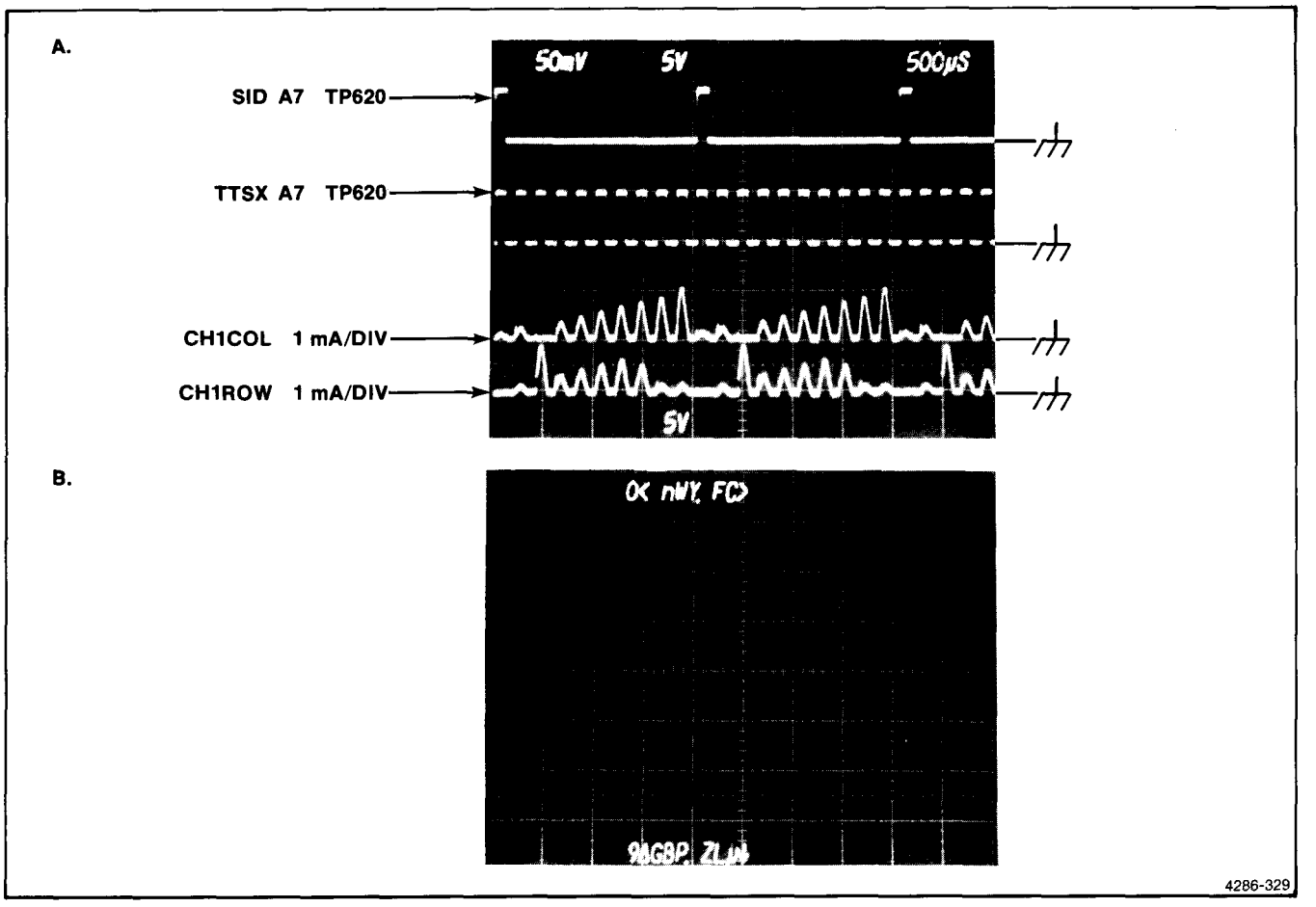


Figure 3-20. (A) Row and column currents and (B) readout during Display Readout Characters test.

THRESHOLD DAC RAMP (A KEY)

This test is used to troubleshoot the trigger threshold D/A Converters and Comparators. The CH1 through CH4 DAC outputs will repetitively ramp through their ranges. The ramps are 90 degrees out of phase so that shorts between them can be detected. A8—P745 "START" can be used as a convenient oscilloscope trigger.

ATTENUATOR OFFSET CALIBRATOR (B KEY)

In this exercise each channel's 2X and 2.5X attenuators are inserted to give 0X, 2X, and 5X attenuation. During this time the Offset Adjust potentiometers on the A5 Amplifier Board can be adjusted to minimize attenuator offset which causes trace shift. (Also see Checks and Adjustment section of this manual.)

DISPLAY READOUT CHARACTERS (A THEN B KEY)

Selecting this exercise causes the upper and lower crt readout positions to be filled with characters taken from the "Character selection matrix for 7000-series Readout System" (refer to an appropriate 7000-series mainframe service manual for further details). This can confirm that the 7A42 Readout DACs (A7-U920, U930, U1020, U1030) are capable of sinking current through their entire range of values. Figure 3-20 shows CH1 Row and Column currents and the readout characters displayed during this test.

TRIGGER THRESHOLD CALIBRATION (NOT KEY)

This test acts as an aid in calibrating the gain and offset of each of the four trigger threshold DAC circuits.

When the NOT key is first pushed to enter this calibration routine, the instrument status is set so that CH1 trigger threshold offset is ready for adjustment (refer to the A6 Trigger Board part of the Checks and Adjustment section of this manual). With the CH1 input grounded, CH1 and Trigger View are displayed on the crt. The trigger function is set to A=CH1 with the Switching Threshold displayed and set to .000 VOLTS.

With each successive push of the NOT key, the next channel is set up for trigger threshold offset calibration (i.e., on the second push of the NOT key, CH2 and

Trigger View displayed, CH2 input grounded, trigger function set to A=CH2...etc.).

The fifth push of the NOT key readies the 7A42 for CH1 trigger offset gain calibration. Trigger View and CH1 are displayed with CH1's input ungrounded and input impedance set to 1MΩ. The trigger function is set to A=CH1 with the Switching Threshold set to .250 Volts. With a .250 Volt reference connected to the CH1 input, the trigger threshold gain is ready to adjust.

Pushing the NOT key again readies the next channel for calibration.

A NOT key push following CH4 trigger threshold gain calibration restarts the sequence with CH1 trigger threshold offset ready for adjustment.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of replacing parts and repairing assemblies. Special techniques required to replace parts in the 7A42 Logic Triggered Vertical Amplifier are given here.

WARNING

Dangerous voltages (about 250 V peak) are present at several points on the A9 Power Supply Board. When the 7A42 is operated with its covers removed, do not touch exposed connections or parts. Some transistors have voltages present on their cases. Disconnect the 7A42 from its power source before cleaning or replacing parts.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office. However, you should be able to obtain many of the standard electronic parts from a local commercial source. Before you purchase or order a part from any source other than Tektronix, Inc., check the Replaceable Electrical Parts list for the proper value rating, tolerance and description.

SPECIAL PARTS

Some parts are manufactured or selected by Tektronix, Inc., to satisfy particular requirements, or are made for Tektronix, Inc., to our specifications. Most of the mechanical parts used in this instrument were made by Tektronix, Inc. To determine the manufacturer of parts, refer to Parts List, Cross Index Mfr. Code Number to Manufacturer.

ORDERING PARTS

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type.
2. Instrument serial number.
3. A description of the part; if it is an electrical part, include circuit number.
4. Tektronix Part Number.

SOLDERING TECHNIQUES

WARNING

To avoid electric-shock hazard and instrument damage, disconnect the 7A42 from the power source before soldering.

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used when repairing or replacing parts.

The desoldering and removal of parts is especially critical and should be done only with a vacuum solder extractor; further, one approved by a Tektronix, Inc., Service Center.

Use wire solder with rosin core, 63% tin, 35% lead. Contact your local Tektronix, Inc. representative or field office for approved solders.

Most circuit boards used in the 7A42 are multilayer. Conductive paths between the top and bottom board layers may connect with one or more inner layers. If this inner conductive path is broken (due mainly to poor soldering practices) between the layers, the board is unusable and must be replaced. Damage can void warranty.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum type desoldering equipment, should attempt repair of any board in this instrument.

When soldering on circuit boards or small wiring, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron can cause the etched circuit wiring to separate from the board base material, and metl the insulation from small wiring. Always keep the soldering-iron tip properly tinned for best heat transfer. Apply only enough heat to make a good solder joint. To protect heat-sensitive components, hold the component lead with a pair of long-nose pliers between the component body and the solder joint.

The following technique should be used to replace a component on any of the circuit boards.

Touch the tip of the vacuum desoldering tool directly to the solder to be removed.

CAUTION

Excessive heat can cause the etched circuit wiring to separate from the board base material.

Never allow the solder extractor to remain on the board for more than three seconds. Solder wick, spring-actuated or sqeeze-bulb solder suckers, and heat blocks (for multi-pin components) must not be used. Damage can void warranty.

NOTE

Some components are difficult to remove from the circuit boards due to a bend placed in each lead during machine insertion of the component. The bent leads held the component in position during a flow-solder manufacturing process which soldered all components at once. To make removal of machine-inserted components easier, first remove the solder from the joint, then straighten the leads of the component on the back of the circuit board, using a small screwdriver or pliers.

When removing multi-pin components, do not heat adjacent conductors consecutively (see Fig. 3-21). Allow a moment for the circuit board to cool before proceeding to the next pin.

Bend the leads of the replacement components to fit the holes in the circuit board. Insert the leads into the holes in the board, or as originally positioned.

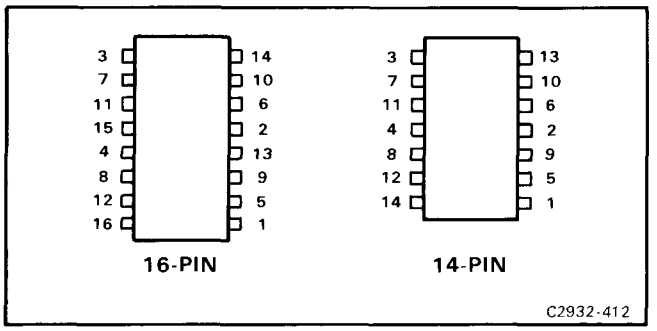


Figure 3-21. Recommended desoldering sequence.

Touch the iron to the connection and apply enough solder to make a firm solder joint.

Cut off any excess lead protruding through the board.

Clean the areas around the solder connection with a flux remvoing solvent. Be careful not to remove the information printed on the circuit board.

REMOVING AND REPLACING PARTS

CAUTION

To avoid component damage, always disconnect the assembly from the power source before removing or replacing components.

The exploded-view drawing associated with the Replaceable Mechanical Parts list (located at the rear of this manual) may be helpful in the disassembly procedures that follow.

SEMICONDUCTORS

Semiconductors should not be replaced unless actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement of semiconductors may affect the adjustment of the instrument. When semiconductors are replaced, check the operation of circuits which may be affected.

Replacement semiconductors should be of the original type or a direct replacement. Lead configurations of the semiconductors used in this instrument are shown in Figure 3-2, Semiconductor Lead Configurations, at the beginning of this section.

CAUTION

Do not remove stickers affixed to the top of EPROMs. Removing of this sticker will allow light into the chip, and may cause partial erasure of its data.

An extracting tool should be used to remove the in-line integrated circuits to prevent damaging the pins. This tool is available from Tektronix, Inc.; order Tektronix Part 003-0619-00. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the integrated circuit. Try to avoid disengaging one end from the socket before the other end.

Once an in-line integrated circuit is removed, a socket should be installed to prevent damage to the circuit board due to repeated soldering and desoldering. Do not install sockets for the ECL devices on the A6 Trigger Board or behind the power supply on the A8 MPU Board. Recommended part numbers are as follows:

8-pin	136-0727-00
14-pin	136-0728-00
16-pin	136-0729-00
20-pin	136-0752-00

CHASSIS PARTS

How to Remove the Front-Panel Assembly

To remove the front-panel assembly, proceed as follows:

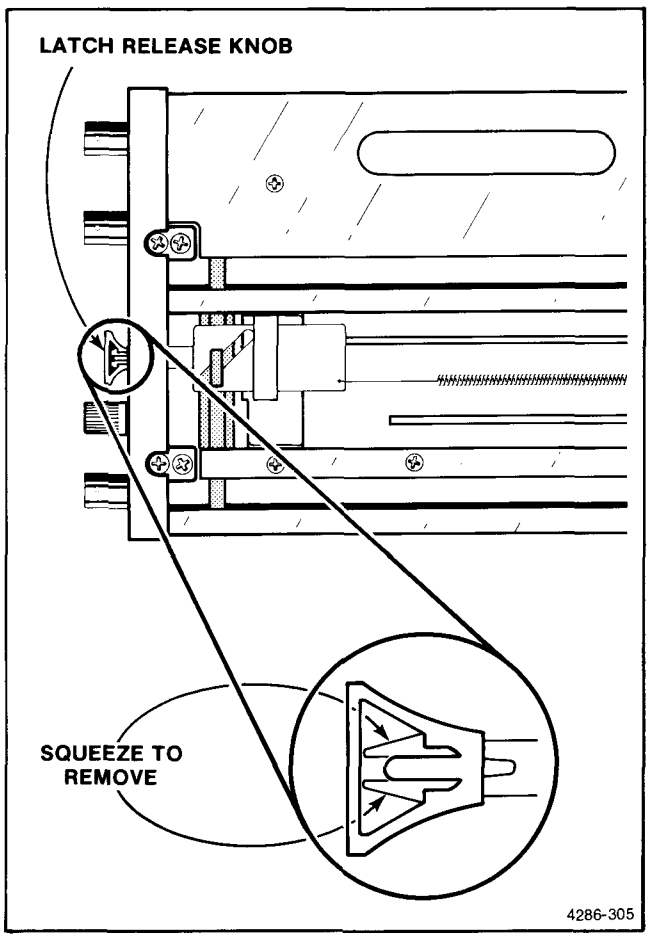


Figure 3-22. How to remove the latch-release knob.

1. Remove the latch release knob. See Figure 3-22.
2. Remove the socket-head capscrew from the front of each attenuator assembly (total of four screws).
3. Remove the eight screws that fasten the front panel to the chassis rails.
4. Set the 7A42 right-side up on a work area, then pull the front panel outward, away from the chassis, and swing it to the right.
5. Unplug J340 and J260 from the LED Board, and J140 from the A1 Switch Board.
6. Make a note of the cable colors, then unplug the coaxial cables from the rear of the TRIG OUT and EXT CLOCK front-panel connectors.
7. Unplug P710 from J710 on the front of the A2 LED Board.

How to Replace the Front Panel

1. Hold the front-panel assembly near the front of the 7A42, then plug in the three coaxial cables as follows:

Color	Cable Whose Other End Connects to	Connect Front-Panel End to
blue/white	J632 on A6 Trigger Board	EXT CLOCK, J47
red/white	J602 on A6 Trigger Board	TRIG OUT, J49
green/white	J700 on A6 Trigger Board	J710 on A2 LED LED Board (Center conductor to top pin)

2. Plug P240 and P260 onto J240 and J260 on the A2 LED Board, then plug P140 onto J140 on the A1 Switch Board.
3. Align the front panel with the chassis rails, then slide it into position while guiding the latch release and the GAIN adjust shaft into their respective holes.
4. Start, but do not tighten, two of the screws that hold the front panel to the chassis rails.
5. Start the four socket-head capscrews that fasten the front of the attenuators to the front panel.
6. Install the other six front-panel to chassis rail screws, then tighten all eight of them.
7. Tighten (but not too much) the four socket-head capscrews.

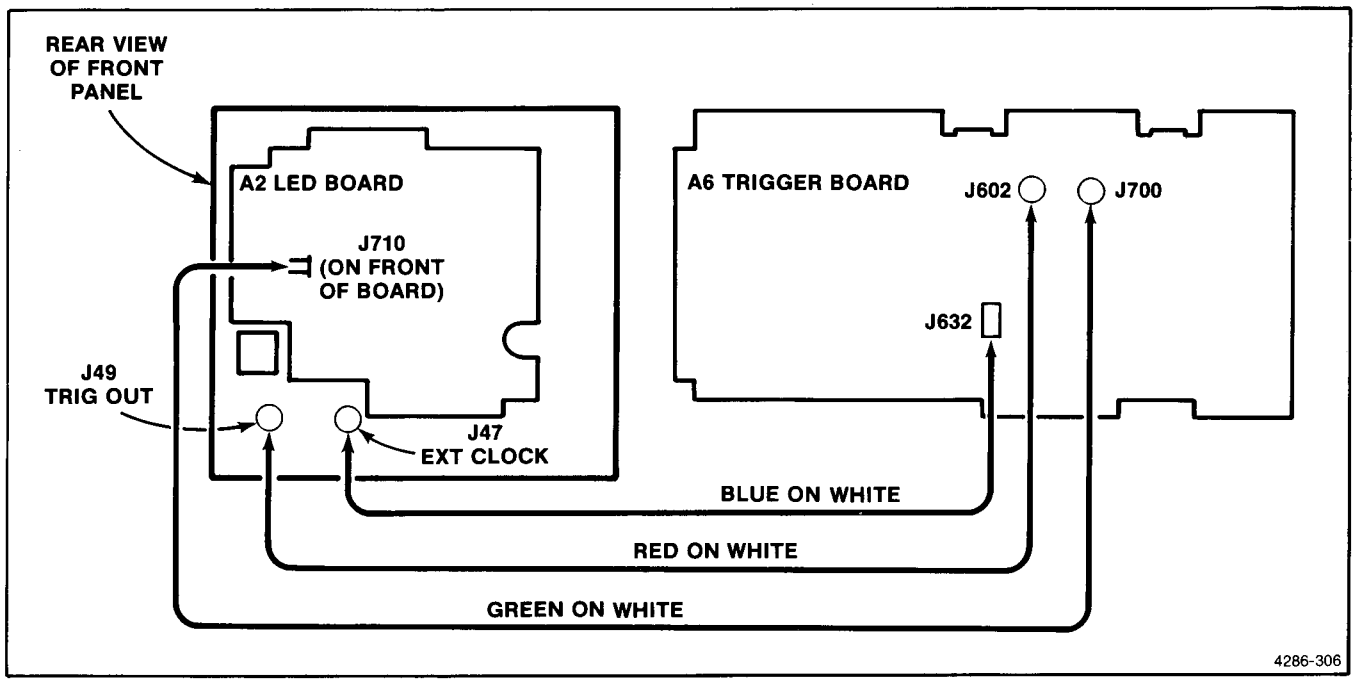


Figure 3-23. Interconnections between front panel and A6 Trigger Board.

8. Install the latch release knob.

How to Replace Front-Panel Components

LEDs

1. Remove the front panel as outlined in "How to Remove the Front Panel," in this section.

2. Remove the A1 Switch Board—A2 LED Board assembly from the front panel, and separate it, as outlined in "How to Remove the A1 Switch Board—A2 LED Board Assembly," in this section.

3. Cut the leads of the defective LED with diagonal cutting pliers.

4. Unsolder and remove the lead ends from the circuit board.

5. Use a vacuum desoldering tool to remove the solder from the holes.

6. Orient the new LED correctly, then insert its leads into the pads on the circuit board.

NOTE

The LED and Switch Boards each have LED-orientation diagrams, as shown in Figure 3-24.

Also, the initial letter of the LED color is noted next to each LED (R for red, Y for yellow, etc.).

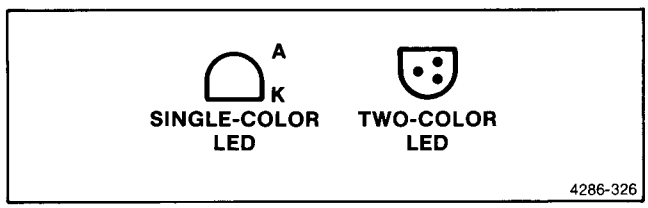


Figure 3-24. Pins of single-color and two-color LEDs.

7. Place the LED at the correct installed height, then solder one lead only.

8. Check the height of the LED; if necessary, heat the solder joint and adjust the installed height.

9. Solder the other lead(s) and cut off the excess.

10. Guide the five potentiometers and eight LEDs through holes in the A1 Switch Board, then install the flat washers and nuts on the potentiometers.

11. Install the two-board assembly on the front panel as outlined in "How to Install the A1 Switch Board—A2 LED Board Assembly," in this section.

Potentiometers

1. Remove the front panel as outlined in "How to Remove the Front Panel," in this section.

2. Remove the A1 Switch Board—A2 LED Board assembly from the front panel, and separate it, as outlined in "How to Remove the A1 Switch Board—A2 LED Board Assembly," in this section.

3. Cut the leads of the defective potentiometer.

4. Unsolder and remove the lead ends from the circuit board.

5. Use a vacuum desoldering tool to remove the solder from the holes.

6. Bend the leads of the new potentiometer to fit the holes in the LED Board.

7. Install the potentiometer leads in the appropriate holes (do not solder yet) and orient the potentiometer in correct position.

8. Assemble the A1 Switch Board to the A2 LED Board, install the five flat washers and nuts, then tighten the nuts.

9. Solder the potentiometer leads to the A2 LED Board, then cut off the excess leads.

10. Install the two-board assembly on the front panel as outlined in "How to Install the A1 Switch Board—A2 LED Board Assembly," in this section.

Switches

1. Remove the front panel as outlined in "How to Remove the Front Panel," in this section.

2. Remove the A1 Switch Board—A2 LED Board assembly from the front panel, and separate it, as outlined in "How to Remove the A1 Switch Board—A2 LED Board Assembly," in this section.

   Each switch is held to the circuit board by two mounting posts which are a press fit in the board. To remove a switch, proceed as follows:

3. Locate the mounting posts of the switch to be replaced.

4. Working from the back of the circuit board, use a flat object to press the two mounting posts in until they are flush with the board surface.

NOTE

Do not pry the switch from the front of the board. Doing so could damage the circuit board parts and runs.

5. Grasp the switch assembly firmly and pull it out of the board.

6. Orient the new switch so that the contacts line up with the contact pads on the circuit board.

7. Insert the mounting posts into the holes in the circuit board.

8. Press the switch toward the board until it seats firmly.

9. Install the two-board assembly on the front panel as outlined in "How to Install the A1 Switch Board—A2 Lead Board Assembly," in this section.

How to Remove and Replace the Front-Panel Overlay and/or the A10 DVM Board

The A10 DVM Board is captive between the front-panel overlay and the sub-panel. The overlay must be removed for access to the A10 DVM Board. To remove the front-panel overlay, proceed as follows:

1. Remove the front-panel assembly as outlined in this section.

2. Remove the four POSITION knobs and the TRIG FILTER knob.

3. Remove the four screws that fasten the A1 Switch Board—A2 LED Board assembly to the front panel.

4. Grasp the A2 LED Board at its top and bottom, then pull it directly away from the front panel to disengage the A2 LED Board from the pins of the A10 DVM Board on the front panel. Be careful not to stress P110's wire as it comes through its hole in the A1 Switch Board.

The rear of the front panel is now accessible.

5. Remove the four nuts that fasten the front panel overlay to the sub-panel.

6. Gently press the four studs to separate the overlay from the sub-panel.

7. If desired, remove the A10 DVM Board from the front of the sub-panel.

8. To replace the A10 DVM Board, insert it in the recess in the front of the sub-panel with its pins offset toward the top of the sub-panel.

9. Install the front-panel overlay over the A10 DVM Board, then install the four retaining nuts and tighten them carefully (do not overtighten). After replacing the A1 Switch Board—A2 LED Board assembly, check that all DVM pins are properly installed in their sockets.

10. To complete the replacement process, follow the removal procedure in reverse order, starting with part 4.

How to Remove and Replace the Rear Panel

To remove the rear panel, proceed as follows:

1. Set the 7A42 right-side up on the workbench with the rear panel facing you.

2. Remove the two screws that fasten the rear end of the A9 Power Supply Board to the bracket attached to the rear panel.

3. Remove the two screws and nuts that fasten the A6 Trigger Board grounds to the rear panel.

4. Remove the eight screws that fasten the rear panel to the chassis rails.

5. Withdraw the rear panel from the 7A42 chassis.

To replace the rear panel, use the removal procedure in reverse order.

CIRCUIT BOARDS

If a circuit board is damaged beyond repair, replace the entire board assembly. Part numbers are listed in Section 6, Replaceable Electrical Parts, for completely wired boards.

Refer to the "Diagrams and Circuit Board Illustrations" section for the location of each circuit board.

Some parts mounted on the board, such as extension shafts, support posts, switch pushbutton knobs, lamps and board to front-panel wiring, must be retained for use with the new assembly.

NOTE

Refer to Adjustment After Repair in this section.

How to Remove the A1 Switch Board—A2 LED Board Assembly

NOTE

When working with the A1 Switch Board and A2 LED Board, be careful not to bend the LEDs. They should all be oriented correctly, standing up straight and at equal heights, before the board assembly is installed.

1. Remove the 7A42 front panel as outlined in this section.

2. Remove the four POSITION knobs and the TRIG FILTER knob. This is accomplished by firmly grasping each knob and pulling it straight out from the front panel.

3. Unplug P110 from J110 on the A2 LED Board. P110 is on the end of the wire that connects to the PROBE OFFSET TIP connector on the front panel.

4. Unplug P720 from J720 on the A2 LED Board. P720 connects to the RESET connector on the front panel.

5. Remove the four screws that fasten the A1 Switch Board—A2 LED Board assembly to the front panel.

6. Grasp the A2 LED Board at the top and bottom, then pull it directly away from the front panel to disengage the A2 LED Board from the pins of the A10 DVM Board on the front panel. Take care not to stress the wire to P110 (from the PROBE OFFSET TIP connector) as it comes out of its hole in the A1 Switch Board.

7. Pull the five plastic knob inserts from the shafts of the POSITION controls (four) and the TRIGGER FILTER control.

8. Remove the five nuts and washers that fasten the POSITION controls and TRIGGER FILTER control to the A1 Switch Board.

9. Carefully separate the A1 Switch Board from the A2 LED Board.

How to Install the A1 Switch Board—A2 LED Board Assembly

NOTE

When working with the A1 Switch Board and A2 LED Board, be careful not to bend the LEDs. They should all be oriented correctly, standing up straight and at equal heights, before the board assembly is installed.

1. Insert P110 through the hole in the A1 Switch Board, then plug it on to J110 on the A2 LED Board. P110 is on the end of the wire connected to the PROBE OFFSET TIP connector on the 7A42 front panel.

2. Connect P720 to J720 on the A2 LED Board. P720 is on the end of the wire connected to the RESET connector on the 7A42 front panel, and J720 is the single pin next to J710. Install washers and nuts on each potentiometer, then tighten the nuts.

3. Install the five knob inserts on the POSITION controls (four) and the TRIGGER FILTER control. Orient the inserts so that they slide all the way on to the shafts.

4. Carefully place the two-board assembly so that the pins on the A10 DVM Board align with the appropriate receptacles on the A2 LED Board, then fully engage the connector. Double check that all DVM pins have been properly installed in their sockets.

5. Install the four retaining screws and tighten them.

6. Install the knobs on the five knob inserts that protrude through the front panel.

How to Remove the A4 Attenuator Control Board

1. Remove the latch release knob, as shown in "How to Remove the Front Panel."

2. Remove the two screws that fasten the two nut blocks, at the rear of the A4 Attenuator Control Board, to the chassis rails. Do not remove the screws that hold the nut blocks to the A4 Attenuator Control Board.

3. Remove the socket-head capscrew from the front of each attenuator module, a total of four screws.

4. Remove the eight screws that fasten the front panel to the chassis rails.

5. Pull the front panel outward, away from the chassis, until it clears the chassis rails, then swing it to the right.

6. Remove the screw that fastens the rear of each attenuator module, through the A4 Attenuator Control Board, to the A5 Amplifier Board (a total of four screws).

7. Pull the A4 Attenuator Control Board directly away from the A5 Amplifier Board to disengage the connector pins. Then swing the A4 Attenuator Board to the left to make the trigger signal connectors accessible.

8. Disconnect the four trigger signal connectors from the back of the A4 Attenuator Control Board.

How to Replace the A4 Attenuator Control Board

1. Connect the four trigger signal connectors to the back of the A4 Attenuator Control Board.

2. Align the pins on the A4 Attenuator Control Board with their connectors on the A5 Amplifier and A3 Interconnect Boards, then engage them.

3. Start, but do not fully tighten, the four screws that fasten the A4 Attenuator Control Board to the A5 Amplifier Board.

4. Place the front panel in position, then guide the GAIN adjust shaft and the plug-in release bar into their respective holes in the front panel.

5. Start, but do not tighten, two of the screws that fasten the front panel to the chassis rails.

6. Start, but do not tighten, the four socket-head capscrews that fasten the front of the attenuator modules to the front panel.

7. Install the other six front-panel to chassis-rail screws, then tighten all eight of them.

8. Install the two screws that fasten the nut blocks (on the A4 Attenuator Control Board) to the chassis rails.

9. Tighten (but not too much) the four socket-head capscrews.

10. Tighten the four screws that hold the rear of the A4 Attenuator Control Board to the A5 Amplifier Board.

How to Remove the A5 Amplifier Board

1. Remove the rear panel as outlined in this section.

2. Remove the two top circuit-board supports.

3. Remove the three screws and nuts that fasten ground straps from the A5 Amplifier Board heat sinks.

4. Remove the ribbon cable that connects J600 on the A3 Interconnect Board to J500 on the A5 Amplifier Board.

5. Disconnect the four input plugs that connect the signals from the attenuator modules to the A6 Trigger Board at the A6 Trigger Board ends (P200, P210, P220, and P230).

6. Unplug P230 from the back of the A5 Amplifier Board.

7. Remove the ribbon cable that connects J560 to J630 on the A6 Trigger Board.

8. Disconnect P320 from the back of the A5 Amplifier Board.

9. Remove the four screws that fasten the A5 Amplifier Board to the A4 Attenuator Control Board.

10. Use a blunt instrument to push the front end of the A5 Amplifier Board away from the A4 Attenuator Control Board enough to disengage the eight pins that connect the input signals.

11. Hold the front of the A5 Amplifier Board away from the pins from the A4 Attenuator Control Board, then gently pull the A5 Amplifier Board toward the rear of the 7A42. Be careful not to bend any parts.

How to Replace the A5 Amplifier Board

1. Set the A5 Amplifier Board in the grooves in the bottom circuit board support, then slide it forward far enough so you can insert the gain-adjust shaft into the hole in the A3 Interconnect Board.
2. Wiggle the gain-adjust shaft while slowly moving the A5 Amplifier Board forward to its installed position (in installed position, the eight pins from the A4 Attenuator Control Board will align with the receptacles on the A5 Amplifier Board). Use care not to bend any parts.
3. Use the flat side of a screwdriver to press the A5 Amplifier Board toward the A4 Attenuator Control Board and engage the pins.
4. Connect the Channel 2, 3, and 4 inputs to the A6 Trigger Board.
5. Install the gray ribbon cable between J600 on the A3 Interconnect Board and J500 on the A5 Amplifier Board.
6. Connect the Channel 1 input (P200) to the A6 Trigger Board. The cable should be routed over the gray ribbon cable.
7. Install the three-wire ribbon cable between J560 of the A5 Amplifier Board and J630 of the A6 Trigger Board.
8. Connect P320 to J320 on the back of the A5 Amplifier Board.
9. Install the four screws that fasten the front of the A5 Amplifier Board to the attenuator modules.
10. Install the rear panel.
11. Install the two screws and nuts that fasten the ground leads from the Trigger Shields to the rear panel.
12. Install the two upper circuit-board guides. Be sure that the circuit boards fit in the slots in both the upper and lower circuit-board guides.
13. Install the three screws and nuts that fasten the heat sink ground straps to the chassis rail.
14. Install the two screws and spacers that attach the rear of the power-supply chassis to the rear panel.

How to Remove and Replace the A6 Trigger Board Assembly

1. Remove the two upper circuit-board supports.
2. Remove the two screws and nuts that fasten the two ground leads to the rear panel. See Figure 3-25.
3. Unplug the Trig Out (red on white) and Reset (green on white) cables, the A Then B Gate Out connector, and the Ext Clk connector from the right side of the A6 Trigger Board.
4. Unplug the Trigger Out (P602) and Trigger View Output (P630) connectors, and the four trigger inputs from the Attenuators (P200, P210, P220, and P230) from the back of the A6 Trigger Board.
5. Rock the board up and down while pulling it toward the rear of the 7A42.
6. When the board clears its receptacle, lift it carefully out of the 7A42. Be careful not to bend or damage any parts.
7. To replace the A6 Trigger Board assembly first hold it close enough to the 7A42 to plug the Ext Clk connector, P632, to J632 on the A6 Trigger Board.
8. Lower the A6 Trigger Board assembly about halfway into the 7A42 chassis, then plug in the following connectors:

Connector	Signal	Side of Board (front view)
P602	Trig Out to front panel	R
P700	Reset to front panel	R
P600	A then B Gate to MPU	R

9. Lower the A6 Trigger Board assembly fully into the 7A42 chassis.
10. Use a pair of long-nose pliers to plug P610 on to J610 on the back of the A6 Trigger Board. (The other end of this cable connects to J230 on the A5 Amplifier Board.)
11. Connect P200, P210, and P220, the Ch 1, Ch 2, and Ch 3 inputs to the A6 Trigger Board.
12. Turn the 7A42 upside down.
13. Connect P230, the Ch 4 input, to J230 on the A6 Trigger Board.
14. Connect P630, the Trig View Out to Amplifier signal, to J630 on the A6 Trigger Board.
15. Check that the three coaxial cables do not go between the A6 Trigger Board and its shield, lest they prevent the A6 Trigger Board assembly from fitting correctly in the slots in the lower circuit-board guides.
16. Set the Trigger Board in the slots in the lower circuit-board supports.

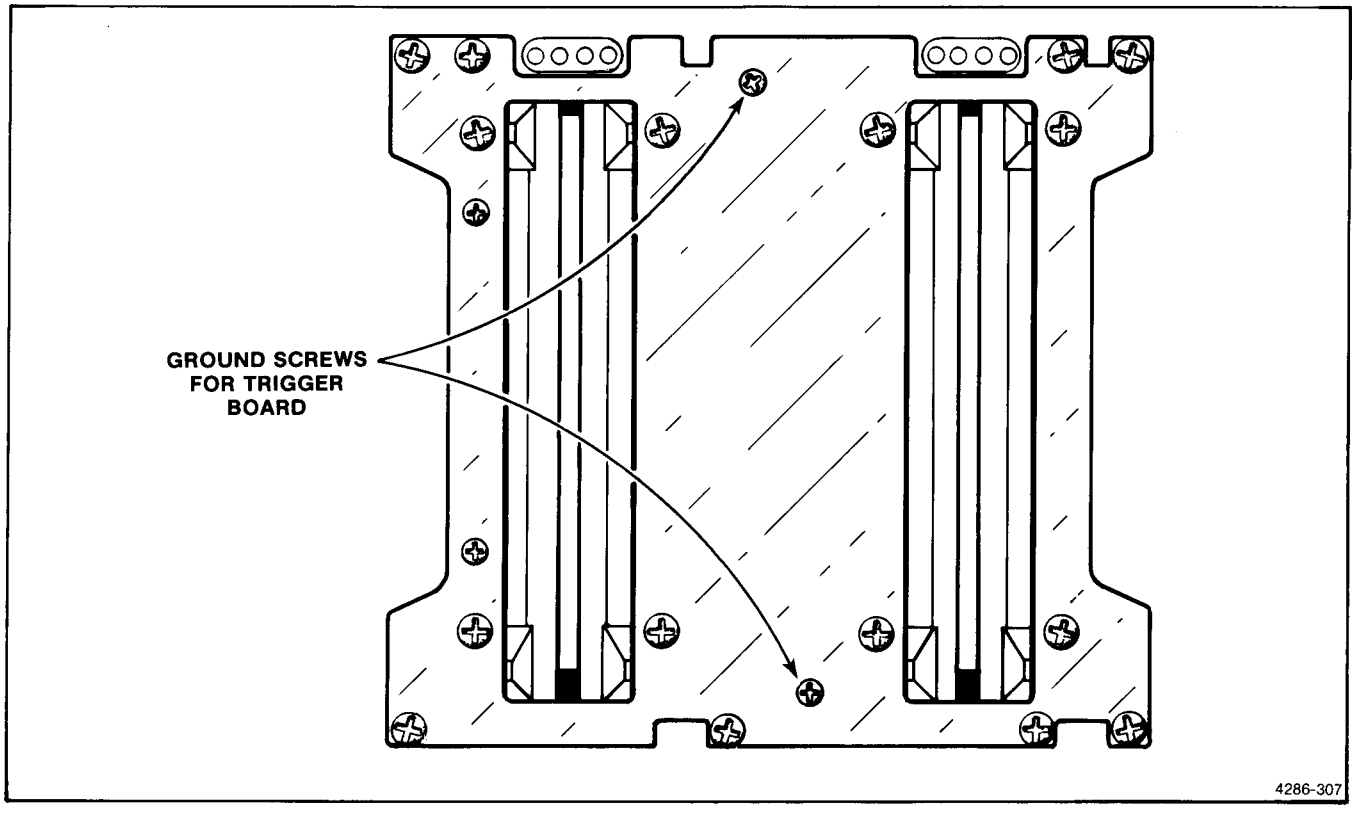


Figure 3-25. Trigger Board ground screws.

17. Insert the A6 Trigger Board into its socket.

18. Replace the two screws and nuts that fasten the ground leads to the rear panel.

19. Replace the upper circuit-board guides (be sure that the circuit boards are in their slots in both upper and lower circuit-board guides).

How to Remove and Replace the A7 Digital Board

1. Remove the two upper circuit-board guides.

2. Unplug P1010 from the upper rear of the A7 Digital Board.

3. Rock the board up and down while pulling it toward the rear of the 7A42.

4. When the board clears the receptacle, lift it out of the 7A42. Be careful not to bend or damage any parts.

5. To replace the A7 Digital Board, hold the back of the board so that P1010 can be connected to J1010.

6. Lower the board into the 7A42 and set it in the slots in the lower guide.

7. Insert the board into its socket.

8. Replace the upper circuit-board guides (be sure that the circuit boards are in their slots in both upper and lower circuit-board guides).

How to Remove and Replace the A8 MPU Board

1. Remove the power supply as outlined in this section.

2. Remove the rear panel as outlined in this section.

3. Remove the two upper circuit-board guides.

4. Unplug power-supply connectors P440 and P445.

5. Unplug P910 from the back of the board.

6. Pull the A8 MPU Board out of its socket, then carefully withdraw it from the 7A42 chassis.

7. To replace the A8 MPU Board, use the removal procedure in reverse order.

How to Remove the A9 Power Supply Board

The A9 Power Supply Board is attached to the chassis rails and to the rear panel via an angle bracket. To remove the A9 Power Supply Board, proceed as follows:

1. Loosen the two screws that fasten the ends of the post spacer to the chassis rails about 1/2 turn each.

2. Remove the two screws that fasten the rear of the A9 Power Supply Board to the angle-bracket.

3. Swing the rear of the A9 Power Supply Board out from the 7A42 chassis.

4. Unplug P445 and P440 from the A9 Power Supply Board.

5. Remove the two screws which were loosened in part 1.

To replace the A9 Power Supply Board, follow the removal procedure in reverse order. When replacing the A9 Power Supply Board, be sure to fully tighten the two screws that fasten the hinge post to the chassis rails. If they protrude they could catch on the EMI strip when the 7A42 is removed.

How to Remove and Replace Attenuator Modules

To remove an attenuator module, proceed as follows:

1. Remove the A4 Attenuator Control Board as outlined in this section.

2. On the opposite side of the board from the attenuator modules, the front and rear ends of each module are fastened to the board with a 4-40 by 1/4-inch screw and a 3/16-inch hex nut, respectively. Remove these two fasteners on the module(s) to be removed.

3. Use the vacuum desoldering tool to unsolder the ten pins shown in Figure 3-26.

4. After removing solder from these 10 holes, make sure that each pin is actually unsoldered from the hole. The unsoldered pins should be free to move.

5. Gently work the module away from the circuit board, being careful to move the front and rear evenly so that the module remains parallel to the board during its departure. When the slender gold pins leave their sockets the module will be free.

To replace an attenuator module, proceed as follows:

1. Inspect the A4 Attenuator Control Board to verify that the 10 holes where the module pins will fit are free and clear of any solder from a previous installation. See Figure 3-26.

2. Check that the pins on the attenuator module(s) are straight; carefully straighten any that need it.

3. Remove any excess solder from the 10 pins which will be soldered. See Figure 3-26.

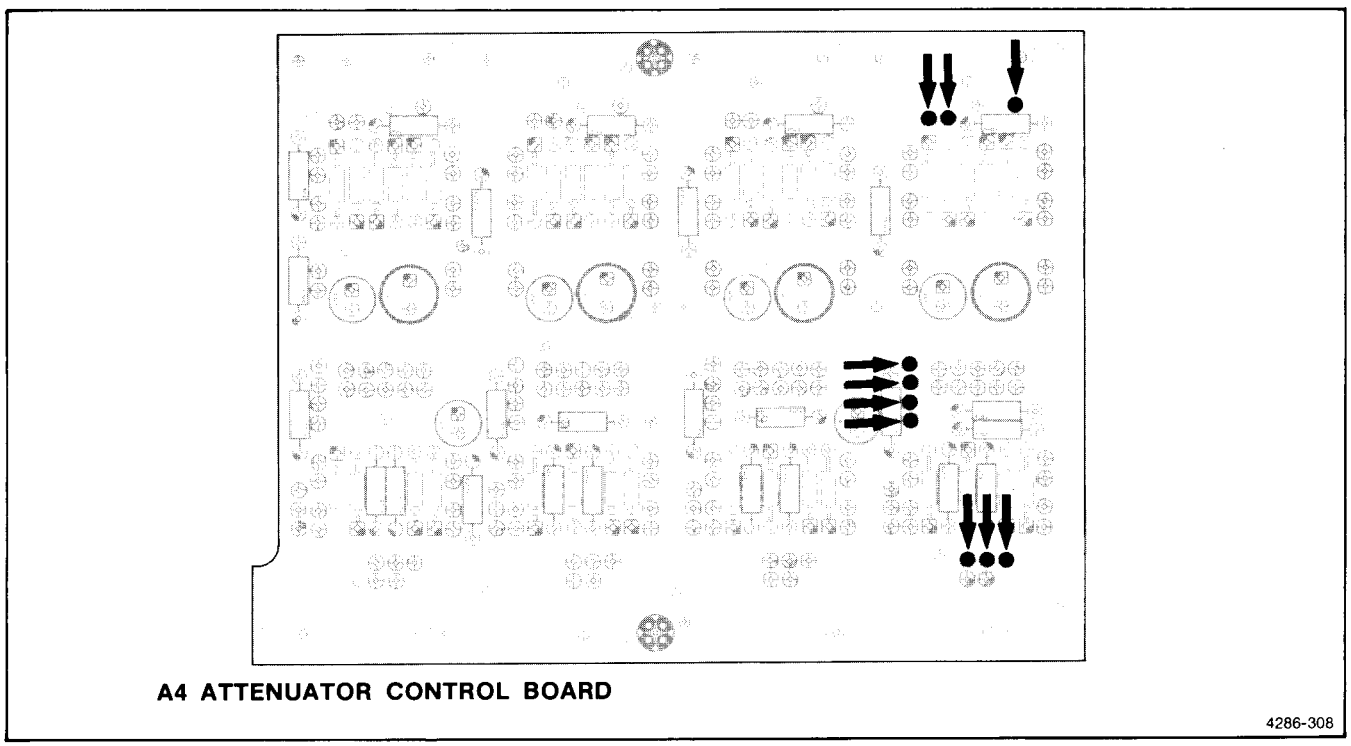


Figure 3-26. The 10 pins that must be unsoldered to remove an attenuator module.

4. Check that the hex nut is removed from the stud on the bottom of the attenuator module.

5. Check that the mounting screw is not screwed into the bottom of the attenuator module.

6. Align the attenuator module with the A4 Attenuator Control Board so that:

   a. the threaded stud goes into its hole,

   b. the slender relay pins are started (but not yet inserted) into the silicone rubber seals in the sockets, and

   c. the other 10 pins are aligned with their holes.

7. By applying slight pressure, the silicone rubber seals should provide a "cushiony" feel because the relay pins are contacting them instead of the sockets underneath them. This shows that the relay pins are in the correct locations. An improperly located pin will result in a stiff feel, which will alert you that a pin is not located correctly.

8. When you are satisfied that the pins are correctly located in the sockets, apply a gentle pressure to insert the pins in their sockets. The pins should enter the sockets far enough to allow the attenuator module to rest against the circuit board.

9. Look beneath the attenuator module to see if all the relay pins entered their sockets straight. A bent pin indicates interference, which should be corrected.

10. Install the 4-40 by 1/4-inch screw to fasten the connector end of the module to the board, and the hex nut to fasten the back end of the attenuator to the board. Do not overtighten these fasteners because excessive stress could crack the substrate in the attenuator module.

11. Install the 4-40 by 1-1/8-inch screw through the other hole in the front of the attenuator module adjacent to the bnc connector. (Be sure to use the correct length screw here to avoid damage to the A1 Switch Board.)

12. Start the spacer post on the other end of the long screw installed in step 11, then tighten to "finger tightness" only. (Do not use a nutdriver or other tool on the spacer post.) Overtightening will warp the board. These three fasteners must be installed before the 10 pins are soldered to the board. They seat the attenuator firmly against the board.

13. Solder the 10 pins (see Fig. 3-26) to the board. Do not use excessive solder.

14. Remove the long screw and the spacer post.

15. Complete the process by installing the A4 Attenuator Control Board as outlined in this section.

How to Remove and Replace Armature Relays

The attenuator modules need not be removed from the A4 Attenuator Control Board, nor must the board be removed from the 7A42, to remove or replace armature relays. To remove a relay, proceed as follows:

1. Remove the four screws that secure the cover, then remove the cover.

2. Grasp the relay across its short dimension with a pair of needle-nose pliers and gently pull it straight out of the attenuator module.

When the attenuator covers are removed, use care to prevent particles of any foreign material, or even solder smoke, from entering the attenuator.

The armature relays can be installed in either direction. To install a relay, proceed as follows:

1. Check that the four relay pins are straight and parallel to one another, that is, all perpendicular to the bottom surface of the relay housing.

2. Hold the relay in position so that its four pins enter the holes in the attenuator housing next to the A4 Attenuator Control Board.

3. Press gently on the top of the relay and notice the response. Silicone rubber seals in the pin sockets will cause a "cushiony" feel when the pins are located properly in the sockets.

4. Gently press the relay into its sockets until the relay bottom seats fully into the attenuator housing.

5. Remove the pressure pad from the inside of the attenuator cover.

6. Install a new pressure pad (Tektronix Part 348-0759-00) in the attenuator cover.

7. Gently blow the inside of the attenuator out with clean pressurized air.

8. Install the cover on the attenuator.

When ordering armature relays, it is a good time to order pressure pads for the inside of the attenuator covers (Tektronix Part 348-0759-00). The pressure pads should be replaced when more than one attenuator cover is removed, when relays are substituted, or when new relays are installed.

How to Replace the Delay Lines

The 7A42 delay lines are a matched pair; if defective

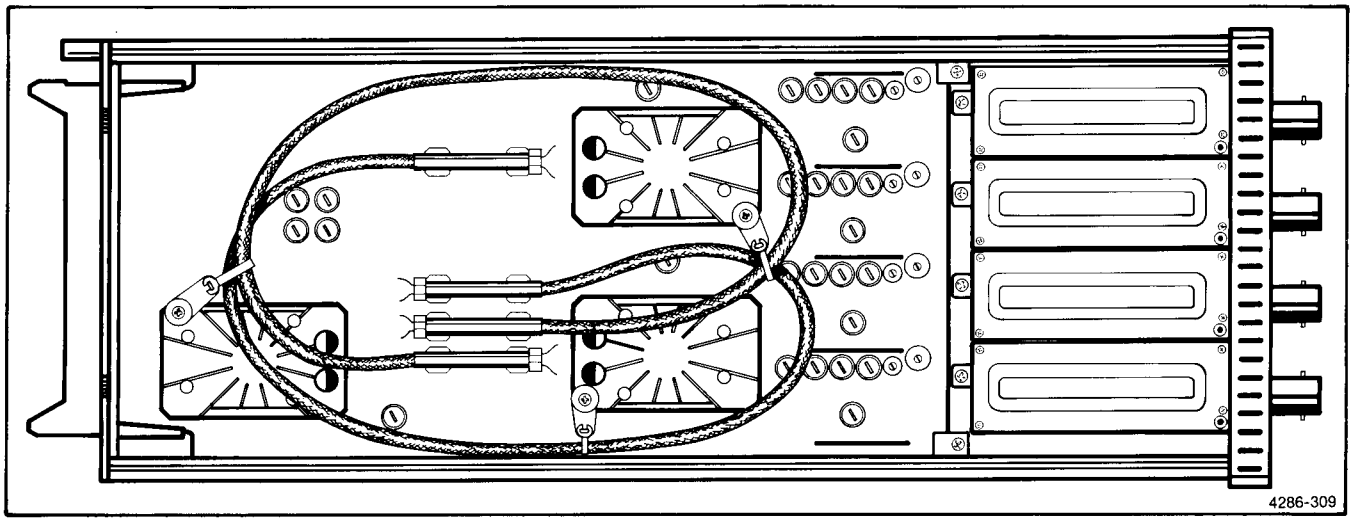


Figure 3-27. Placement of delay lines.

they should be replaced as a pair. The pair of delay lines should be routed and clamped as shown in Figure 3-27.

When replacing a pair of delay lines, observe the following guidelines:

1. Do not cut any of the leads shorter.
2. The red lead goes in the terminal marked +.
3. Some parts of the delay lines may need to be pre-formed to clear the vertical channel switches. Check the contours of the old delay line as a guide.
4. When soldering the leads to the board, place the lead in the circuit board pad so that the end is flush with the back of the board. The lead should not protrude through the board.
5. Do not pull any lead out of the delay-line housing.

How to Replace Vertical Channel Switch Microcircuits

The vertical channel switch (VCS) microcircuits have integral heat sinks. Three locator posts, two at one end and one at the other, index the VCS for correct installation.

To replace the VCS, proceed as follows:

1. Remove the retaining nuts and cable clamp from the VCS.
2. Lift the VCS from its socket.
3. Orient the replacement VCS to fit the socket.
4. Be sure the locator pins fit in their respective locations.
5. Press the VCS toward the board to feel the spring tension of the contacts.
6. Hold the VCS in place, install the four retaining nuts and tighten them finger tight.
7. Use a torque wrench to tighten the retaining nuts to 3-1/2 to 4 inch pounds.
8. Install the spacer posts and cable clamps as shown in Figure 3-27.

Plug-in Latch

1. Using needle-nose pliers, squeeze the lock mechanism and pull the knob off the latch shaft. See Figure 3-28.
2. Remove the latch shaft return spring.
3. Remove the front-panel assembly as outlined in this section.
4. Remove the clips that hold the latch crossbar in place.
5. Lift the crossbar out of its groove, then out of the 7A42.
6. To replace, insert the crossbar and shaft into the grooves, re-install the clips, and press the latch knob on to the shaft until it snaps into place.
7. Attach the spring to the shaft.
8. Re-install the front-panel assembly on the 7A42.

INTERCONNECTING PINS

Two methods of interconnection are used in the 7A42 to electrically connect the circuit boards with other boards

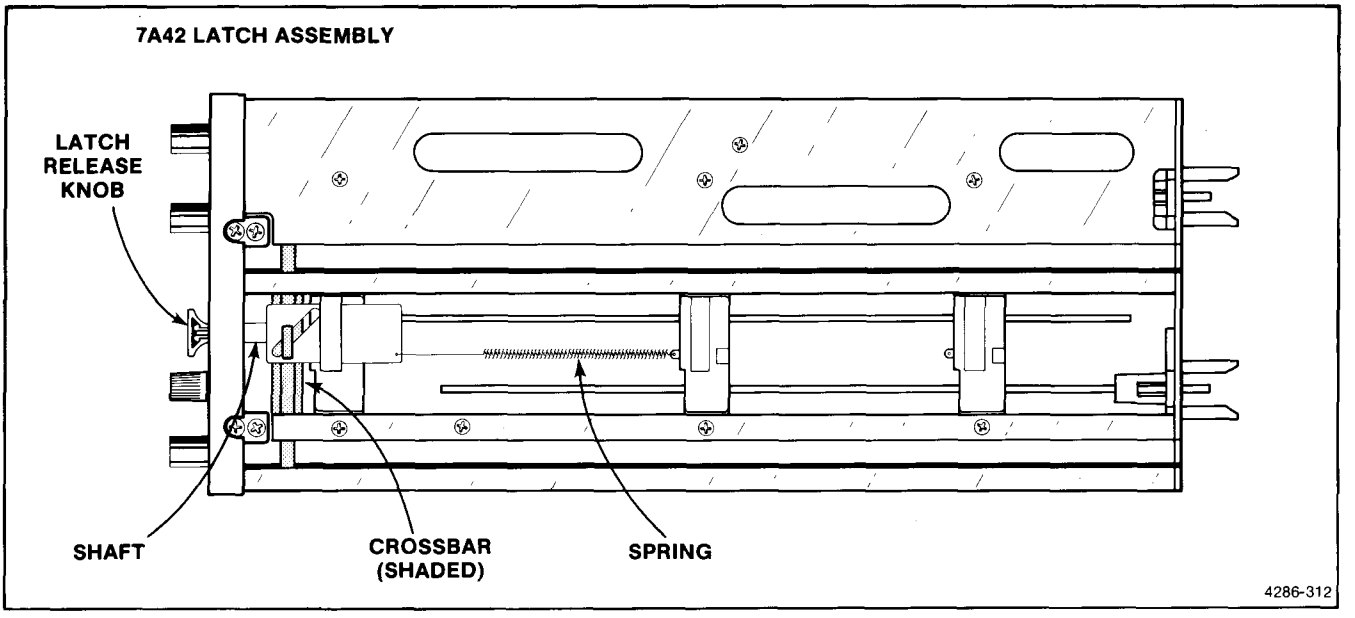


Figure 3-28. Latch assembly.

and components. When interconnection is made with a coaxial cable, a special end-lead connector plugs into a socket on the board. Other interconnections are made with a pin soldered into the board. Two types of mating connectors are used for these interconnecting pins. If the mating connector is mounted on a plug-on circuit board, a special socket is soldered into the board. If the mating connector is on the end of a lead, an end-lead pin connector is used that mates with the interconnecting pin. The following information provides the removal and replacement procedure for the various types of interconnecting methods.

Coaxial-Type End-Lead Connectors

Replacement of the coaxial-type end-lead connectors requires special tools and techniques; only experienced maintenance personnel should attempt to remove or replace these connectors. We recommend that the damaged cable or wiring harness be replaced as a unit. For cable or wiring harness part numbers, see Section 8, Replaceable Mechanical Parts. An alternative solution is to refer the replacement of the defective connector to your local Tektronix Field Office or representative. Figure 3-29 shows the parts of a coaxial end-lead connector assembly.

Circuit-Board Pins

A circuit-board pin replacement kit (including necessary tools, instructions, and replacement pins with attached ferrules) is available from Tektronix, Inc. Order Tektronix Part. 040-0542-01. Replacing circuit-board pins on multi-layer boards is not recommended. (The multi-layer boards in this instrument are listed under Soldering Techniques in this section.)

To replace a damaged pin, first disconnect any pin connectors. Then remove the solder from the connection using a vacuum desoldering tool. (See Soldering Techniques.) Remove the damaged pin from the board with a pair of pliers, leaving the ferrule (see Fig. 3-30) in the circuit board if possible. If the ferrule remains in the circuit board, remove the spare ferrule from the replacement pin and press the new pin into the hole in the circuit board. If the ferrule is removed with the damaged pin, then press the replacement pin, with attached spare ferrule, into the circuit board. Position the replacement pin in the same manner as the original. Solder the pin to the circuit board on each side of the board. If the original pin was bent at an angle to mate with a connector, carefully bend the new pin to the same angle. Replace the pin connector.

Circuit-Board Pin Sockets

The pin sockets on the circuit boards are soldered to the back of the board. To remove or replace one of these sockets, first unsolder the pin (see Soldering Techniques). Then straighten the tabs on the socket and remove the socket from the board. Place the new socket in the circuit board hole and press the tabs down against the board. Solder the tabs of the socket to the circuit board; be careful not to get solder inside the socket.

NOTE

The spring tension of the pin sockets ensures a good connection between the circuit board and the pin. This spring tension can be destroyed by using the pin sockets as a connecting point for spring-loaded probe tips, alligator clips, etc.

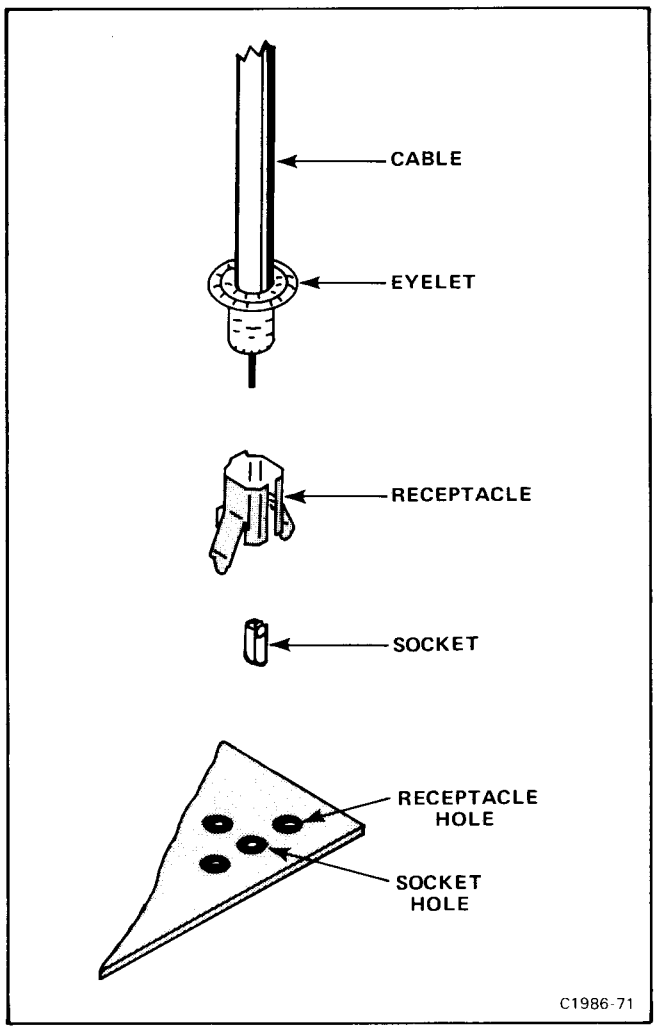


Figure 3-29. Coaxial-end lead connector assembly.

Multi-Pin Connectors

The pin connectors used to connect the wires to the interconnecting pins are clamped to the ends of the associated leads. To remove or replace damaged multi-pin connectors, remove the old pin connectors from the end of the lead and clamp the replacement connector to the lead.

NOTE

Some multi-pin connectors are equipped with a special locking mechanism. These connectors cannot be removed by pulling the wire(s). To remove the connectors from the pin(s) grasp the plastic holder and pull.

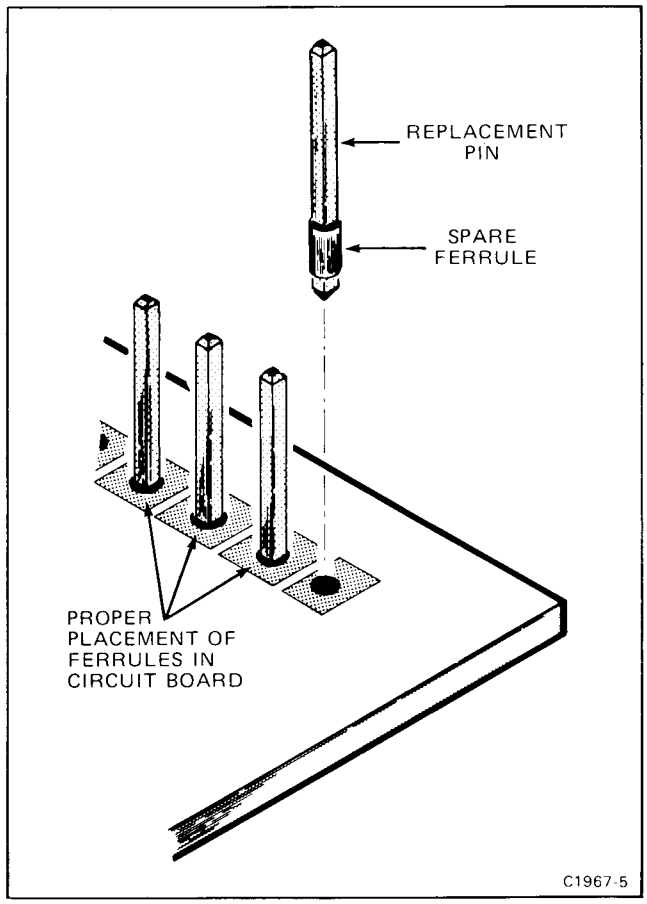


Figure 3-30. Exploded view of circuit-board pin and ferrule.

To remove an individual wire from the holder insert a scribe in the hole on the side of the holder and slide the extended portion under the holder. This will allow the wire to be removed from the holder.

Some of the pin connectors are grouped together and mounted in a plastic holder; the overall result is that these connectors are removed and installed as a multi-pin connector (see Troubleshooting Aids). If the individual end-lead pin connectors are removed from the plastic holder, note the order of the individual wires for correct replacement in the holder.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of any closely related circuits. See section 4 for a complete adjustment procedure.

CHECKS AND ADJUSTMENT

This section provides procedures for checking and adjusting this instrument. These procedures are designed to compare the performance of this instrument with measurement instruments of known accuracy to detect, correlate, or eliminate by adjustment, any variation from the electrical specifications. Also, the functional check procedure verifies that the major functions of the instrument perform properly.

This section has three separate parts: Part I—Functional Check Procedure verifies that the major functions of the instrument perform properly. Part II—Performance Check Procedure verifies that this instrument meets the applicable electrical specifications in Section 1. Part III—Adjustment Procedure provides adjustment instructions to ensure that this instrument is performing at peak capabilities and meets or exceeds the listed electrical specifications at the time of adjustment under the conditions specified. These three parts provide for verification of the qualitative integrity of the product, its performance relating to specifications in Section 1, and the optimization of its performance respectively.

USING THESE PROCEDURES

NOTE

In these procedures, capital letters within the body of the text identify front-panel controls, indicators, connectors and readout information on the 7A42 (e.g., POSITION). Initial capitals identify all the associated test equipment and their controls, connectors and indicators (e.g., Triggering) used in the procedures. Initial capitals also identify adjustments internal to the 7A42 (e.g., Current Limit).

The Part I—Functional Check procedure should be followed in the sequence in which it is written, starting with step 1, and continuing through to its conclusion. Typically, the Functional Check Procedure is a front-panel check, but in some cases it may be necessary to open the instrument covers to change jumper positions, set switches, or make connections.

The Part II—Performance Check and Part III—Adjustment procedures are divided into subsections by major functional circuits (e.g., A. Power Supply, B. Attenuator Offset, etc.). The order in which the subsections and procedures appear is the recommended sequence for a complete performance check or adjustment of the instrument.

The first step in each subsection (A1, B1, etc.) contains reference information and Setup Conditions that must be performed before proceeding.

The Setup Conditions provide equipment connection information and control settings for both this instrument and any associated test equipment. Also, the Setup Conditions are written so that if desired, each subsection (A, B, C, etc.) or step (A2, A3, B2, B3, etc.) can be performed independently.

When used as the first word of an instruction, the terms CHECK, EXAMINE, ADJUST, and INTERACTION are defined as follows:

1. **CHECK**—indicates that the instruction accomplishes an electrical specification check. Each electrical specification check is listed in Table 4-1, Performance Check and Adjustment Summary.

2. **EXAMINE**—usually precedes an ADJUST instruction and indicates that the instruction determines whether adjustment is necessary. If no ADJUST instruction appears in the same step, the EXAMINE instruction concerns measurement limits that do not have a related adjustment. Measurement limits following the word EXAMINE are not to be interpreted as electrical specifications. They are provided as indicators of a properly functioning instrument and to aid in the adjustment process.

3. **ADJUST**—describes which adjustment to make and the desired result. It is recommended that adjustments not be made if a previous EXAMINE instruction indicates that no adjustment is necessary.

4. **INTERACTION**—indicates that the adjustment described in the preceding instruction interacts with other circuits. The nature of the interaction is described and reference is made to the step(s) affected.

PERFORMANCE CHECK AND ADJUSTMENT SUMMARY

Table 4-1 lists the electrical specifications that are checked in Part II, and the related adjustment (when applicable) in Part III. Table 4-1 is intended to provide a convenient means of locating the steps that check the electrical specifications of the product.

TABLE 4-1
Performance Check and Adjustment Summary

Characteristic	Performance Requirement	Part II-Performance Check Procedure Title	Part III-Adjustment Procedure Title
DISPLAY			
Deflection Factor Calibrated Range at Input BNC's TTL (CMOS) Family	0.1, 0.2, 0.5 V/div.	A2. Check Deflection Factor Accuracy and Trace Shift.	C2. Adjust Amplifier Gain (R1010, R1030, R1040, R1060).
ECL Family	20, 50, 100 mV/div.		
Channel-to-Channel Gain Match	Within 2% in ECL logic family, 20 mV/div, 1 MΩ input impedance.	A3. Check Channel-to-Channel Gain Match.	C2. Adjust Amplifier Gain (R1010, R1030, R1040, R1060).
Gain Ratio Accuracy Within the Same Channel	Within 2% of indicated deflection factor relative to ECL logic family, 20 mV/div, 1 MΩ input impedance.	A2. Check Deflection Factor Accuracy and Trace Shift.	Not applicable.
Frequency Response Bandwidth	350 MHz in 7104, 0°-35°C mainframe ambient temperature. Refer to 7000-series Oscilloscope system Specifications, in the Tektronix Product Catalog, for System Specifications.	A4. Check Bandwidth.	C3. Adjust Amplifier Compensation (R903, R902, R700, R901, R1000, C1100, C1000, R922, R921, R920, R1020, C1120, C1020, R935 R934, R730, R933, R1031, C1130, C1031, R953, R952, R951, R1050, C1150, C1050).
Protection Reaction Time 50Ω Input Impedance Only	APPLIED OVER-VOLTAGE / MAXIMUM TIME TO OPEN INPUT 10 V dc — 10 seconds 15 V dc — 1 second 20 V dc — 0.5 second	Specification applicable under fault conditions; therefore, this specification does not have a procedural check.	Not applicable.
Input Characteristics High Impedance	1 MΩ, ±1%, in parallel with approximately 15 pF.	A5. Check High-Impedance Inputs.	Not applicable.
Low Impedance	50Ω, ±1Ω at dc.	A6. Check Low-Impedance Inputs.	Not applicable.
Volts/Division Shift	0.2 div or less shift when volts/div is changed in either TTL or ECL families, or between families.	A2. Check Deflection Factor Accuracy and Trace Shift.	B2. Adjust Attenuation Offset (R320, R321, R322, R323).
Differential Delay Between Any Two Channels Set to Same Logic Family and Volts/Division	200 ps maximum.	A7. Check Differential Delay Between Channels.	Not applicable.

TABLE 4-1 (CONT)
Performance Check and Adjustment Summary

Characteristic	Performance Requirement	Part II-Performance Check Procedure Title	Part III-Adjustment Procedure Title
DISPLAY (CONT)			
TRIG VIEW or External Clock View		B2. Check Trigger View Amplitude.	Not applicable.
Amplitude	0.35 div ±0.1 div.		
Time Coincidence with Channel Display		B3. Check Trigger View-Time Coincidence With Channel Display.	Not applicable.
TRIG VIEW	Within 3 ns.		
External Clock View	Within 5 ns.	D2. Check Ext Clock View-Time Coincidence With Channel Display.	Not applicable.
TRIGGER			
Threshold		C2. Check Threshold Voltage Range.	Not applicable.
Voltage Range			
TTL (CMOS) Family	+1.28 V to −1.27 V, as observed at input connector.		
ECL Family	+256 mV to −254 mV, as observed at input connector.		
Accuracy (At Center Value of Hysteresis Window)		C3. Check Threshold Accuracy.	D3. Adjust Trigger Thresholds (R300, R302, R301, R303, R400, R402, R401, R403).
TTL (CMOS) Family	±5 mV, ±2% of reading, as observed at input connector.		
ECL Family	±1 mV, ±2% of reading, as observed at input connector.		
Hysteresis (Centered at Threshold, 50kHz sine-wave)		C4. Check Threshold Hysteresis.	Not applicable.
TTL (CMOS) Family	40 mV +20%, -50%, as observed at input connector.		
ECL Family	8 mV +20%, -50%, as observed at input connector.		
Probe TIP Input		C5. Check Probe-Tip Input Voltage Accuracy.	D4. Adjust Probe Offset (R425, R525).
Voltage Range (Maximum)	+5.10 to −5.10 V, dc only.		
DVM Accuracy	±20 mV, ±2% of reading.		

TABLE 4-1 (CONT)
Performance Check and Adjustment Summary

Characteristic	Performance Requirement	Part II-Performance Check Procedure Title	Part III-Adjustment Procedure Title
TRIGGER (CONT)			
TRIGGER FILTER		E2. Check Trigger Filter.	Not applicable.
Range	OFF, or adjustable from <15 ns to >300 ns.		
Match, Function A to Function B	Within 20% at maximum setting.		
EXT CLOCK INPUT		D4. Check External Clock Input Thresholds.	Not applicable.
Threshold			
TTL Level			
Logic zero	≤0.8 V.		
Logic one	≥2 V.		
ECL Level			
Logic zero	≤-1.5 V.		
Logic one	≥-1.1 V.		
Pulse Width		D3. Check Minimum External Clock Width.	Not applicable.
TTL Level	20 ns minimum.		
ECL Level	5 ns minimum.		
Set-Up Time	10 ns minimum.	D5. Check External Clock Setup Time.	Not applicable.
Hold Time	10 ns minimum.	D6. Check External Clock Hold Time.	Not applicable.
Channel Edge Sensitivity		F2. Check Edge Setup Time (Channel-to-Channel).	Not applicable.
Set-Up Time (Channel to Channel)	5 ns minimum.		
Hold Time (Channel to Channel)	5 ns minimum.	F3. Check Edge Hold Time (Channel-to-Channel).	Not applicable.
Set-Up Time (Edge Sensitive Channel)	10 ns minimum.	F4. Check Edge Setup Time (Edge-Sens-Chan).	Not applicable.
Hold Time (Edge Sensitive Channel)	5 ns minimum.	F5. Check Edge Hold Time (Edge-Sens-Chan).	Not applicable.
TRIGGER OUT Connector		E4. Check Trigger Output Voltage.	Not applicable.
Output Voltage			
Logic Zero	≤0.2 V into 50Ω.		
Logic One	≥0.8 V into 50Ω.		
Toggle Frequency (Displayed Input Signal of 60 mV p-p in ECL, or 300 mV p-p in TTL Logic Family, Centered at Threshold)	125 MHz maximum.	E3. Check Maximum Toggle Frequency.	Not applicable.

TABLE 4-1 (CONT)
Performance Check and Adjustment Summary

Characteristic	Performance Requirement	Part II-Performance Check Procedure Title	Part III-Adjustment Procedure Title
TRIGGER (CONT)			
A THEN B Mode		G2. Check Time Between Event A And Event B.	Not applicable.
Time Between A and B	5 ns minimum.		
Time From B to A	5 ns minimum.	G3. Check Time From Event B to Event A.	Not applicable.
Event Duration		G4. Check Minimum Event Duration.	Not applicable.
Event A	5 ns minimum.		
Event B	5 ns minimum.		
Mainframe A THEN B Gate Output		G5. Check A Then B Gate Output Width.	Not applicable.
Pulse Width	Gate output width, measured at the 50% points, is greater than time between Event A and Event B by 5 ns, ±2 ns.		
Front Panel A THEN B Gate (at TRIGGER OUT connector)		E4. Check Trigger Output Voltage.	Not applicable.
Voltage			
Logic zero	≤0.2 V into 50 Ω.		
Logic one	≥0.8 V into 50 Ω.		
Timing (From Event A Recognition to Rising Edge of Gate)	25 ns or less.	G6. Check Gate Output *Timing.*	Not applicable.
RESET Connector		H2. Check Reset Input Thresholds.	Not applicable.
Levels			
Logic zero	≤0.2 V.		
Logic one	≥0.8 V.		
Pulse Width	100 ns minimum.	H3. Check Reset Input Pulse Width.	Not applicable.
Timing (Post-Reset Inhibit Time to Next Trigger)	10 ns minimum, from falling edge of RESET to next recognizable event.	H4. Check Post-Reset Inhibit Time.	Not applicable.
Response Time	RESET pulse must lead or be coincident with event recognition, to inhibit trigger output. Event recognition must lead the RESET pulse by 10 ns to guarantee trigger output.	H5. Check Reset Activation Window.	Not applicable.

TEST EQUIPMENT

The test equipment listed in Table 4-2 is required for completing Part II—Performance Check Procedure and Part III—Adjustment procedure.

If only a Performance Check is desired, not all equipment is necessary and is indicated by footnote 1. The remaining test equipment is common to both Parts II and III.

The Adjustment procedure is based on the first item of equipment given in Table 4-2. If other equipment is substituted, control settings or setups may need to be altered. If the exact item of equipment given as an example is not available, refer to the Minimum Specifications column to determine if other equipment may be substituted. Then check the Purpose column. If you determine that your measurement requirements will not be affected, the item and corresponding step(s) can be deleted.

TEST EQUIPMENT ALTERNATIVES

Completing both Part II and III may not always be necessary or desirable. You may desire to only check selected characteristics, and thereby substantially reduce the amount of test equipment required.

TABLE 4-2
Test Equipment

Description	Minimum Specification	Purpose	Example of Applicable Test Equipment
1. Oscilloscope Mainframe	Compatible with Tektronix 7000-series plug-in units. Bandwidth, dc to 1 GHz.	Used throughout procedure with the 7A42, as a system.	a. TEKTRONIX 7104 Oscilloscope. b. Refer to Tektronix catalog for compatible oscilloscope.
2. Time-Base Unit	1 ns/div sweep speed.	Used throughout procedure with the Oscilloscope Mainframe and 7A42, as a system.	a. TEKTRONIX 7B10 Time Base. b. TEKTRONIX 7B80 Time Base.
3. Calibration Generator	Amplitude calibrator frequency, 1 kHz; amplitude, 5 V into 50 Ω; accuracy, 0.25% into 1 MΩ. Pulse Mode, period, 1 μs to 10 ms; accuracy, within 5%.	Provides calibrated signal for checking the A. Channel Amplifiers C. Threshold and Probe Offset, G. Trigger—A then B, and for adjusting the C. Amplifier and D. Trigger Threshold and Probe Offset.	a. TEKTRONIX PG 506 Calibration Generator, with Power Module.
4. Digital Multimeter	Voltage range, 0-20 V; accuracy, within 0.05%. Resistance range, 200 Ω; accuracy, 0.05%, Display, 3-1/2 digit.	Used to check the A. Channel Amplifiers, C. Threshold and Probe Offset, and to adjust the D. Trigger Threshold and Probe Offset.	a. TEKTRONIX DM 502A Autoranging DMM, with power module. b. TEKTRONIX DM 501A, with power module.
5. HF Pulse Generator	Risetime, 1 ns; pulse duration variable, 2 ns; amplitude, 5 V into 50 Ω; internal termination, 50 Ω or 1 MΩ.	Used to check the B. Trigger View Trace, D. External Clock, E. Trigger-Level Sensitivity, F. Trigger-Edge Sensitivity G. Trigger—A then B, and H. Trigger-Reset.	a. TEKTRONIX PG 502 250 MHz Pulse Generator, with power module.
6. Function Generator	Sine-wave output; offset voltage, variable; amplitude, 10 V into 50 Ω load; frequency 100 kHz; accuracy, 5%.	Used to check the C. Threshold and Probe Offset, D. External Clock, and H. Trigger-Reset.	a. TEKTRONIX FG 503 Function Generator, with power module.

TABLE 4-2 (CONT)
Test Equipment

Description	Minimum Specification	Purpose	Example of Applicable Test Equipment
7. LF Leveled Sine-Wave Generator	Reference frequency, 50 kHz; Maximum frequency, 125 MHz; amplitude, 1 volt into 50 Ω.	Used to check the E. Trigger-Level Sensitivity.	a. TEKTRONIX SG 503 Leveled Sine Wave Generator.
8. HF Leveled Sine-Wave Generator	Sine-wave output; frequency 6 MHz to 350 MHz; amplitude, 4 V into 50 Ω.	Used to check the A. Channel Amplifiers.	a. TEKTRONIX SG 504 Leveled Sine Wave Generator, with Power Module.
9. LF Pulse Generator	Variable risetime and falltime, 5 ns; amplitude, 10 V into 50 Ω.	Used to check the D. External Clock, and H. Trigger-Reset.	a. TEKTRONIX PG 508 50 MHz Pulse Generator, with Power Module.
10. Power Supply	0 to 20 V continuously variable @ 500 mA.	Used to check the C. Threshold and Probe Offset, and to adjust the D. Trigger Threshold and Probe Offset.	a. TEKTRONIX PS 503A Dual Power Supply, with power module.
11. Flexible Plug-In[1] Extender (Calibration Fixture, Two Required)	For use with 7000-series plug-in units.	Used throughout the Part III—Adjustment Procedure.	a. Tektronix Part 067-0616-00 Flexible Plug-In Extender.
12. Normalizer (Calibration Fixture)	Input RC time constant, 1 MΩ X 15 pF; Connectors, bnc.	Used to check the A. Channel Amplifiers.	a. Tektronix Part 067-0537-00 15 pF Input Normalizer.
13. Dual-Input Cable (Calibration Fixture)	Connectors, bnc-female to dual-bnc-male; the two lengths of RG58 coaxial cable must be matched to less than 0.1 inch.	Used to check the A. Channel Amplifiers, B. Trigger View Trace, D. External Clock, F. Trigger-Edge Sensitivity, and G. Trigger—A then B.	a. Tektronix Part 067-0525-02 Dual Input Cable.
14. Coaxial Cable (Three required)	Impedance, 50 Ω; Connectors, bnc; Length, 42 inches.	Used throughout the Performance Check and Adjustment procedure for signal connections.	a. Tektronix Part 012-0057-01.
15. Adapter Cable	Impedance, 50 Ω; connectors, bnc to right-angle sealectro; length, 44 inches.	Used to check the H. Trigger Reset.	a. Tektronix Part 012-0403-00.
16. Precision Cable	Precision cut to 36.0 inches long; impedance, 50 Ω; connectors, bnc male.	Used to check the F. Trigger-Edge Sensitivity, and G. Trigger—A then B.	a. Tektronix Part 012-0482-00.
17. Patch Cords (Two Required)	Single conductor, length, 18 inches; connectors, banana plug to banana plug.	Used to check the C. Threshold and Probe Offset, and to adjust the D. Trigger Threshold and Probe Offset.	a. Tektronix Parts Red: 012-0031-00. Black: 012-0039-00.

[1]**Used for Adjustment ONLY; not used for Performance Check.**

TABLE 4-2 (CONT)
Test Equipment

Description	Minimum Specification	Purpose	Example of Applicable Test Equipment
18. Meter Leads (For Digital Multimeter)	Single conductor; connectors, banana plug to probe tip.	Used throughout procedures with digital multimeter.	a. Tektronix Part 003-0120-00.
19. Adapter, BNC T	Connectors, bnc male to dual bnc female.	Used to check the D. External Clock, and H. Trigger Reset.	a. Tektronix Part 103-0030-00.
20. Adapter, Female-To-Female (Two Required)	Connectors, bnc, female-to-female.	Used to check the D. External Clock, G. Trigger—A then B, and the H. Trigger Reset.	a. Tektronix Part 103-0028-00.
21. 2X Attenuator (Two Required)	Connectors, bnc male to bnc female; attenuation, 2X; impedance, 50 Ω; power rating, 2 watts.	Used to check the D. External Clock.	a. Tektronix Part 011-0069-02.
22. 10X Attenuator (Two Required)	Impedance, 50 Ω; attenuation, 10X; power rating, 2 watts; connectors, bnc.	Used throughout the Performance Check for signal attenuation.	a. Tektronix Part 011-0059-02.
23. 50 Ω Feedthrough Terminator	Impedance, 50 Ω; frequency, dc to 500 MHz; connectors, bnc male to bnc female.	Used to check the C. Threshold and Probe Offset, D. External Clock, E. Trigger-Level Sensitivity, and H. Trigger-Reset.	a. Tektronix Part 011-0049-01.
24. Alignment tool[1]	Low capacitance adjustment tool.	Used throughout the Part III—Adjustment Procedure.	a. Tektronix Part 003-0675-00.

[1]**Used for Adjustment ONLY; not used for Performance Check.**

PART I—FUNCTIONAL CHECK PROCEDURE

The Part I—Functional Check Procedure verifies that the major functions of the instrument perform as described in the Operators Manual. The procedure exercises the main user interfaces of the device to verify their operation and checks the main internal features.

This procedure is not intended to fully check instrument specifications, but may serve as a brief instrument check of functional specifications, or nonquantified characteristics.

7A42 FUNCTIONAL CHECK

Performing this functional check procedure will ensure that your 7A42 is functionally operational but it will not determine if the instrument is properly adjusted for performance. Built-in self diagnostics greatly simplifies the functional check of the 7A42 by automatically exercising a majority of the functions. You will, however, need to perform the following procedure to thoroughly verify proper operation.

1. SELF TEST

a. Install the 7A42 into the two vertical compartments of a Tektronix 7000-series oscilloscope mainframe.

b. Install a time-base plug-in unit into the right horizontal compartment of the Tektronix 7000-series oscilloscope mainframe.

c. Select the oscilloscope mainframe Left Vertical Mode and B Horizontal Mode buttons. Set the B Trigger Source to Left Vert.

d. Set the time-base unit Triggering Mode, Coupling, and Source switches to Auto, DC, and Internal, respectively.

e. Turn the oscilloscope mainframe Power on. The Self Test will run automatically at power up.

f. When the Self Test is successfully completed, the message "SELF TEST COMPLETE" will appear on the crt for approximately two seconds. Then the front-panel controls will be initialized to the settings they were in at the last power down.

If the Self Test fails, a pattern of LEDs in the TRIGGER FUNCTION matrix will remain lighted, and failure codes will be displayed in the SWITCHING THRESHOLD monitor and crt readout displays; refer to Section 3, Maintenance and Diagnostics, for troubleshooting information.

To continue the Self Test when a failure is indicated, just press any button. At the completion of the last test, control is returned to the normal operating firmware.

2. INITIALIZING THE 7A42

a. Press the PROG CHAN button, if necessary, to extinguish the button light.

b. Press the THRESH button, if necessary, to turn the button light on.

c. Press the PROBE OFFSET button, if necessary, to turn the red button light on.

d. Turn the oscilloscope mainframe Power off, then back on again. The 7A42 should perform all the Self Tests as described previously, and then initialize the front-panel settings to the configuration shown in Table 4-3.

3. DISPLAY AND TRIGGER FUNCTIONS

a. Observe that the red CH1 DISPLAY light is on. Rotate the CH1 POSITION control and note the channel 1 trace can be moved off the screen in both directions.

b. Press the upper VOLTS/DIV button twice to set the deflection factor to .1 V/division (readout display on crt).

c. Connect a coaxial cable from the oscilloscope mainframe Calibrator output connector to the 7A42 CH1 input connector. Set the Calibrator for an output amplitude of 0.4 V (into 1 MΩ) at 1 kHz.

d. Set the time-base unit Time/Div for a sweep speed of 200 μs/division. A square-wave amplitude of 4 divisions should be displayed on the crt. Adjust the time-base unit Triggering Level control as necessary for a stable display.

e. Press the lower VOLTS/DIV button once, and note the crt readout display changes from .1 V to .2 V/division. Press the button again and note the readout changes to .5 V. Return the display to .1 V with two pushes of the upper VOLTS/DIV button.

f. The effect of switching the 7A42 input impedance from 1 MΩ to 50 Ω can be observed, however it depends upon the output impedance of the

TABLE 4-3
7A42 Front-Panel Power-Up Control Settings

Control	Control Setting (Button Light)
PROG CHAN/TRIG	CHAN (off)
Programmable Channel	
CH1	On
CH2	Off
CH3	Off
CH4	Off
DISPLAY	
CH1	On
CH2	Off
CH3	Off
CH4	Off
VOLTS/DIV (Ch1 through CH4)	Preset to 0.5 V/Div at bnc input.
TTL/ECL (CH1 through CH4)	TTL
GND (CH1 through CH4)	Off (ungrounded)
1MΩ/50Ω (CH1 through CH4)	On (1MΩ)
ALT/CHOP	On (ALT)
TRIG VIEW	Off
SWITCHING THRESHOLD voltage (CH1 through CH4)	Preset TTL (+1.4V); display off.
THRESH	Off
PROBE OFFSET	Off
A TRIGGER FUNCTION	CH1 (HI)
B TRIGGER FUNCTION	Clear
Trigger Mode A	On
Trigger Mode B	Off
Trigger Mode A THEN B	Off
EXT CLK SYNC	Off
External Clock Slope	Off

NOTE
Controls not listed above are not preset.

oscilloscope mainframe Calibrator. Most mainframes have a 450 Ω output impedance resulting in 0.4 V amplitude when the 4 V output is selected. Select the 4 V calibrator output amplitude. Push the 1 MΩ/50Ω button to change the 7A42 input impedance to 50 Ω (50Ω 1MΩ 15pf light off). The 4 division signal should still be displayed on screen. Push the 1MΩ/50Ω button again (50Ω 1MΩ 15pf light on) and return the Calibrator output amplitude to 0.4 V.

g. Press the GND button (CH1 GND light on) to see the effect of grounding the channel. The display goes to a ground reference and the triggering stops. Press the GND button again (CH1 GND light off) and note the Calibrator signal is again displayed on the crt.

h. Press the THRESH button (button light on). Now vary the 7A42 trigger threshold throughout its range by pushing (and holding) the LEVEL⇧ and LEVEL⇩ buttons. The trace should become untriggered when the SWITCHING THRESHOLD readout exceeds about 0.40 V, or when it becomes less than about 0.00 V. Return the SWITCHING THRESHOLD readout to 0.14 V.

i. Set the Time-base unit Time/Div for 500 ns/div. With the oscilloscope mainframe Intensity turned up, the rising edge of the Calibrator signal can be viewed. Turn the 7A42 TRIGGER FILTER on (turn clockwise) and observe that the point of triggering is increasingly delayed. Return the control to the OFF (fully counterclockwise) position. Set the time-base unit Time/Div for 200 μs/div.

j. The effects of several trigger functions can be observed with this input signal. Press the TRIG VIEW button to turn on the trigger view trace. Press the PROG TRIG button (green button light on) and press the CLEAR button. Press the CH1 button. Note that the display is the same as it was before. Now push the NOT button; the TRIGGER FUNCTION is now channel 1 low level (green light on). Note that the low level of the channel 1 trace corresponds in time with the high level (true) of the trigger view trace. Push the NOT button again. The trigger function is channel 1 high level again (red TRIGGER FUNCTION light on). Push the EDGE button. The display should remain triggered (if not, a slight adjustment of the time-base unit Triggering Level control may be necessary). The trigger function is now "CH1 EDGE" (the rising edge of channel 1). Change the sweep speed to 100 ns/div. With the intensity turned up a small pulse in the trigger-view trace corresponds with the point on the rising edge where triggering occurs. Push the NOT button to change the trigger function to channel 1 falling edge and observe the displayed result. Edge-

sensitive trigger functions are indicated by a pulsing light in the TRIGGER FUNCTION matrix. Press the NOT and EDGE buttons each several more times to observe their interaction and to compare the crt display to the TRIGGER FUNCTION matrix. Return the sweep speed to 200 μs/div and press the CLEAR button.

k. Press the PROG CHAN button (button light off) and turn off the CH1 display with a press of the DISPLAY button.

l. Operation of Channels 2 through 4 are identical to that of Channel 1. Parts 3a through 3k may be repeated for each channel by substituting the channel under test for all references to CH1 in the procedure.

4. A THEN B NESTED TRIGGERING

a. A simple case of nested triggering can be checked with the oscilloscope mainframe Calibrator signal. Initialize the 7A42 front-panel settings as described in part 2 earlier.

b. Press the upper VOLTS/DIV button twice to set the deflection factor to .1 V/division (readout display on crt).

c. Press the PROG TRIG button (green button light on). Check that the "A" button light is on (right edge of the instrument). The display should be triggered on channel 1 high level. Now push the "B" button (right hand edge of instrument). Press the NOT button, and the CH1 button, respectively. The display should now be triggered on the channel 1 low level. Pushing the "A" button again returns the trigger to channel 1 high level (function B is channel 1 low level). Both trigger functions can be independently programmed and recalled at will. Now push the A THEN B button. The 7A42 is now performing a nested trigger with both functions A and B. Function A first arms the trigger circuitry. Triggering can then occur after the next occurrence of function B. While in A THEN B mode, either of the A or B trigger functions can be displayed in the TRIGGER FUNCTION matrix by selecting the A or B buttons. To exit A THEN B mode, press that button again (button light off).

5. EXT CLOCK OPERATION

a. The functionality of the EXT CLOCK input can be checked if an internal jumper which selects either ECL or TTL clock input levels is in the TTL position. The position of this jumper may be determined from the front panel. Press the PROG CHAN button (button light off). Press the TRIG VIEW button. A triggered square wave should be displayed. Now push the EXT CLOCK SYNC button while watching the trigger view trace. The waveform will become untriggered and the trigger view trace will either go to a steady high, or low level. If it goes low, the External Clock jumper is in ECL mode. Refer to Figure 4-6 in the Performance Check procedure for the location of the External Clock jumper. If the trace goes high, the EXT CLOCK levels are TTL and will be compatible with the oscilloscope mainframe Calibrator output.

b. Set the oscilloscope mainframe Calibrator output amplitude to 4 V and connect a coaxial cable from it to the EXT CLOCK input connector. Check that the EXT CLOCK SYNC button light is on. The clock slope button light should also be on, indicating rising edge sensitivity. Press the PROG TRIG button (button light on), and the CLEAR button. Press the CH1 button, the OR button, the NOT button, and the CH1 button, respectively. There should be a stable trigger view trace on the crt. The trigger view trace display (when the EXT CLOCK SYNC is on) is a digital representation of the clock signal. Push the slope button to falling edge (button light off). Now the trace should be triggered on the falling edge of the external clock signal. Now press the CLEAR button. The trace should become untriggered even through the external clock signal is present, because trigger output will not occur when the trigger function is cleared.

This completes the Part I—Functional Check Procedure.

PART II—PERFORMANCE CHECK PROCEDURE

The Part II—Performance Check Procedure verifies electrical specifications without removing instrument covers or changing internal adjustments. The steps in this procedure check the Performance Requirement statements in Table 4-1, Performance Check and Adjustment Summary. Performance Check Procedure step numbers listed in Table 4-1 reference each Performance Requirement to a specific check in this procedure, and cross-reference to the proper adjustment step in Part III—Adjustment Procedure.

INDEX TO PART II— PERFORMANCE CHECK PROCEDURE

PERFORMANCE CHECK INITIAL SETUP PROCEDURE

NOTE

The specifications are valid at an ambient temperature of 0° to +40° C when used in a 7400/7600-series mainframe without a fan, or at an ambient temperature of 0° to +50° C when used in any other 7000-series mainframe, unless otherwise stated.

CAUTION

To avoid instrument damage, it is recommended that the oscilloscope mainframe POWER switch be turned off before removing or replacing the 7A42.

1. Remove the internal J747 BE (Battery Enable) link plug to disable the battery backup feature. Refer to Figure 4-1. The removal of J747 permits the front-panel settings to be initialized to a known condition each time the oscilloscope mainframe power is turned off, then on. For this reason, the "power off, then on" routine is used frequently throughout the following procedure.

2. Install the 7A42 in the oscilloscope mainframe Left and Right Vertical compartments.

3. Install the time-base unit in the B Horizontal Compartment of the oscilloscope mainframe.

4. Set the oscilloscope mainframe controls:

   Power ..... On
   Intensity ..... Visible display
   Focus ..... Well-defined display
   B Trigger Source ..... Left Vert
   Vertical Mode ..... Left
   Horizontal Mode ..... B

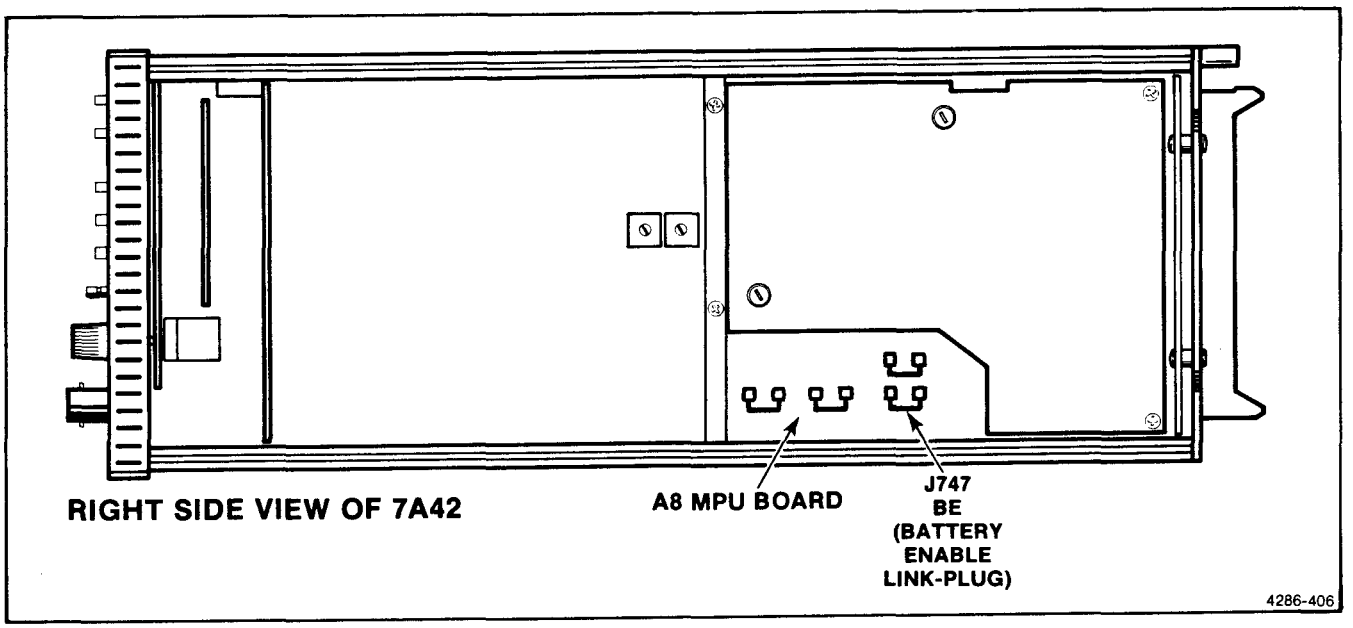


Figure 4-1. Location of the J747 Battery Enable link plug.

A. CHANNEL AMPLIFIERS

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
2. Time-Base Unit
3. Calibration Generator
4. Digital Multimeter
8. HF Leveled Sine-Wave Generator
12. Normalizer (Calibration Fixture)
13. Dual-Input Cable (Calibration Fixture)
14. Coaxial Cable (Two Required)
18. Meter Leads

A1. PRELIMINARY SETUP

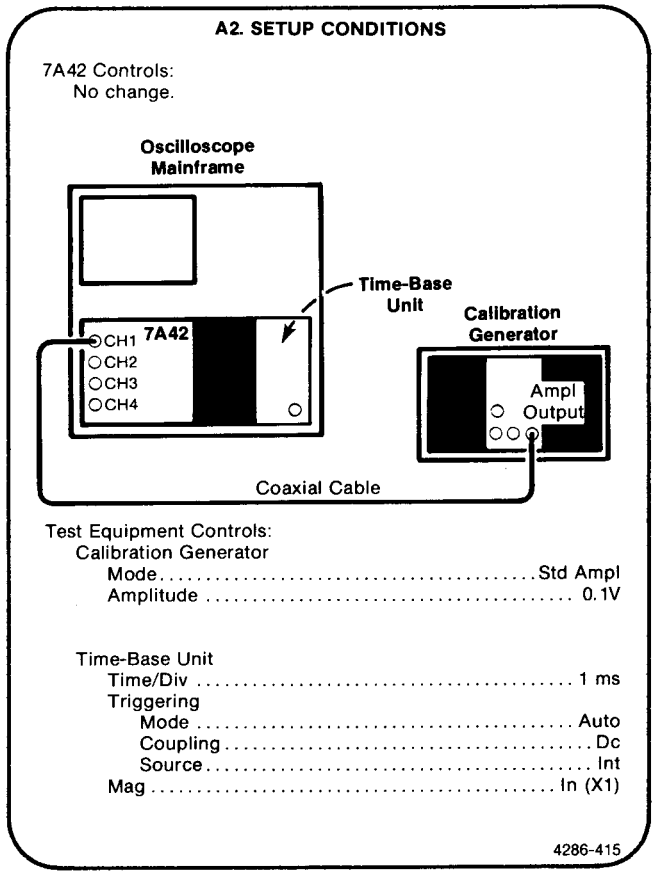
a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

A2. CHECK DEFLECTION FACTOR ACCURACY AND TRACE SHIFT

NOTE

First perform step A1, then proceed.



a. Initialize the 7A42 front-panel settings, by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button to select the first Logic Family indicated in Table 4-4 (i.e., ECL TTL light off to select ECL).

TABLE 4-4
Calibrated Range At Input Connectors

Logic Family	VOLTS/DIV	Input Impedance	Calibration Generator Amplitude	Displayed Amplitude	Calibration Generator Deflection Error Readout
ECL	20 mV	1 MΩ	100 mV	5 div	± 2%
ECL	50 mV	1 MΩ	200 mV	4 div	± 2%
ECL	0.1 V	1 MΩ	500 mV	5 div	± 2%
TTL	0.5 V	1 MΩ	2 V	4 div	± 2%
TTL	0.2 V	1 MΩ	1 V	5 div	± 2%
TTL	0.1 V	1 MΩ	500 mV	5 div	± 2%
ECL	0.1 V	50 Ω	1 V	5 div	± 2%
ECL	50 mV	50 Ω	500 mV	5 div	± 2%
ECL	20 mV	50 Ω	200 mV	5 div	± 2%
TTL	0.5 V	50 Ω	5 V	5 div	± 2%
TTL	0.2 V	50 Ω	2 V	5 div	± 2%
TTL	0.1 V	50 Ω	1 V	5 div	± 2%

c. Press the appropriate VOLTS/DIV button to display the VOLTS/DIV setting indicated in Table 4-4.

d. Press the 1MΩ/50Ω button to provide the Input Impedance indicated in Table 4-4.

e. Set the calibration generator Amplitude control to the value given in Table 4-4.

f. Press the calibration generator Variable control (knob out) and adjust it to display exactly 5 divisions of signal amplitude on the crt.

g. **CHECK**—for the displayed amplitude and Deflection Error given in the last two columns of Table 4-4.

h. Repeat parts b through g for each set of conditions listed in Table 4-4.

i. Repeat parts b through g for CH2, CH3, and CH4; for each successive channel to be checked, first press the DISPLAY button, the channel button of the channel to be checked, the DISPLAY button, and the TRIG VIEW button respectively. Then, proceed with part b.

j. Remove the coaxial cable from the 7A42 CH 4 input connector.

k. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

l. Press the GND button (CH1 GND light on).

m. **CHECK**—for 0.2 divisions or less vertical trace shift while stepping the VOLTS/DIV buttons through the three ranges (0.5 V, 0.2 V, and 0.1 V).

n. Press the TTL/ECL button (CH1 ECL TTL light off).

o. **CHECK**—for 0.2 divisions or less vertical trace shift while stepping the VOLTS/DIV buttons through the three ranges (0.1 V, 50 mV, and 20 mV).

p. Press the DISPLAY button (CH1 DISPLAY light off).

q. Press the CH2 button (button light on).

r. Press the DISPLAY button (CH2 DISPLAY light on).

s. Press the TRIG VIEW button (button light off).

t. Repeat parts k through s for CH2, CH3, and CH4.

u. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

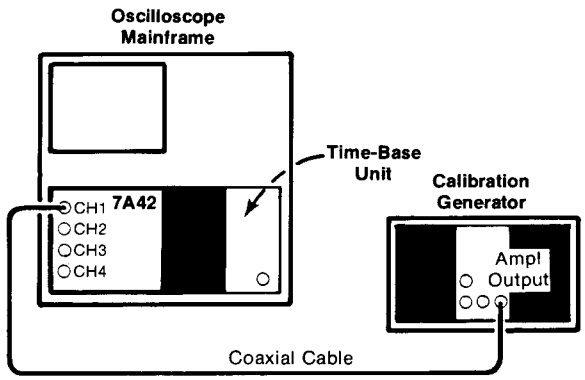
A3. CHECK CHANNEL-TO-CHANNEL GAIN MATCH

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A3. SETUP CONDITIONS

7A42 Controls:
No change.



Test Equipment Controls:
Calibration Generator
Mode ..... Std Ampl
Amplitude 0.1V

Time-Base Unit
Time/Div ..... 1 ms
Triggering
Mode ..... Auto
Coupling ..... Dc
Source ..... Int
Mag ..... In (X1)

4286-416

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the upper VOLTS/DIV button until a crt readout of 20 mV is displayed.

d. **CHECK**—for a displayed signal amplitude of 5 divisions, ±0.1 division.

e. Move the input signal from CH1 to the CH2 input connector.

f. Press the DISPLAY button (CH1 DISPLAY light off).

g. Press the CH2 button (button light on).

h. Press the DISPLAY button (CH2 DISPLAY light on).

i. Press the TRIG VIEW button (button light off).

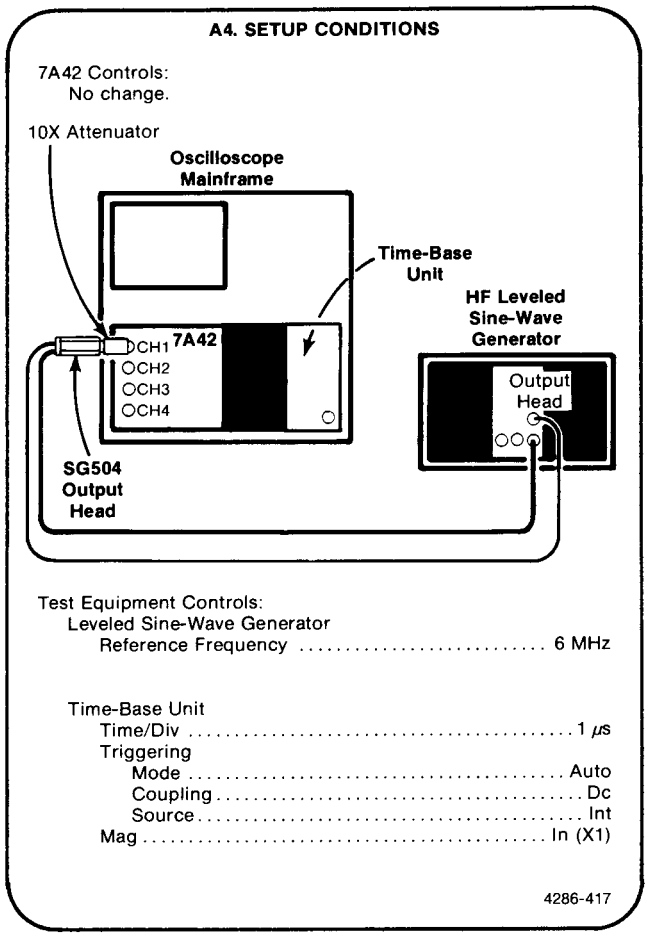
j. Repeat parts b through i for the CH2, CH3, and CH4 inputs.

k. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

A4. CHECK BANDWIDTH

NOTE

If the preceding step was not performed, first perform step A1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the TTL/ECL button (CH1 ECL/TTL light off).

d. Press the upper VOLTS/DIV button twice until a crt readout of 20 mV is displayed.

e. Set the leveled sine-wave generator Amplitude control to display a signal amplitude of 6 divisions at 6 MHz.

f. Set the leveled sine-wave generator Frequency control for 350 MHz output.

g. **CHECK**—for at least 4.2 divisions of signal amplitude on the crt.

h. Remove the 10X attenuator and connect the leveled sine-wave generator output head directly to the CH1 input connector.

i. Press the TTL/ECL button (CH1 ECL/TTL button light on).

j. Press the upper VOLTS/DIV button once to display a crt readout of .2 V.

k. Set the leveled sine-wave generator Amplitude control to display a signal amplitude of 6 divisions at 6 MHz.

l. Set the leveled sine-wave generator Frequency control for 350 MHz output.

m. **CHECK**—for at least 4.2 divisions of signal amplitude on the crt.

n. Move the output head from the CH1 input and reconnect it through the 10X attenuator to the CH2 input connector.

o. Press the DISPLAY button (CH1 DISPLAY light off).

p. Press the CH2 button (CH2 button on).

q. Press the DISPLAY button (CH2 DISPLAY light on).

r. Press the TRIG VIEW button (button light off).

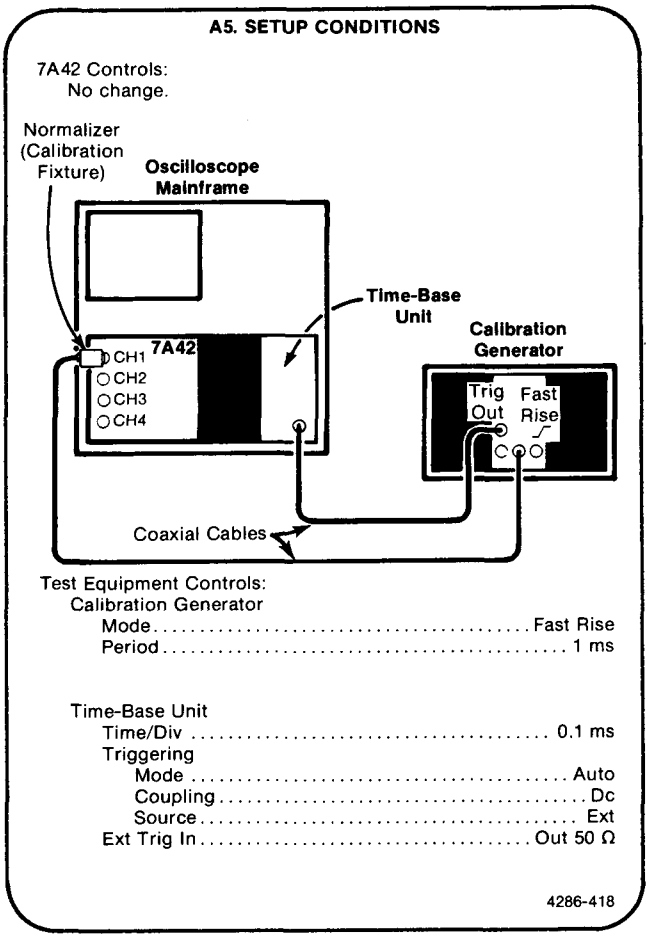
s. Repeat parts b through r for CH2, CH3, and CH4.

t. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

A5. CHECK HIGH-IMPEDANCE INPUTS

NOTE

If the preceding step was not performed, first perform step A1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on.

b. Press the upper VOLTS/DIV button for a readout display of 0.1 V on the crt.

c. Rotate the calibration generator Pulse Amplitude control to display a signal amplitude of 4 divisions, centered on the graticule.

d. **CHECK**—that the top of the pulse is flat to within 0.1 division.

e. Move the normalizer signal from the CH1 to the CH2 input connector.

f. Press the DISPLAY button (CH1 DISPLAY light off).

g. Press the CH2 button (button light on).

h. Press the DISPLAY button (CH2 DISPLAY light on).

i. Press the TRIG VIEW button (button light off).

j. Repeat parts b through i for CH2, CH3, and CH4.

k. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

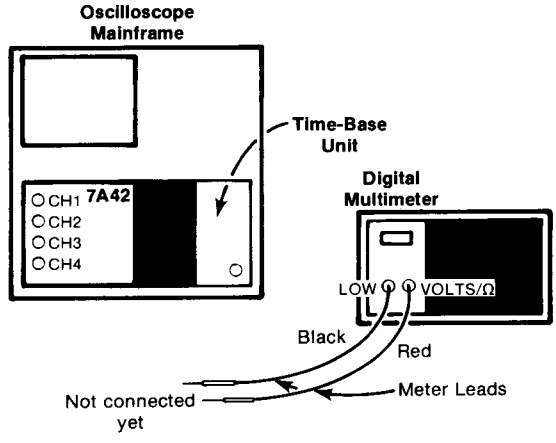
A6. CHECK LOW IMPEDANCE INPUTS

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A6. SETUP CONDITIONS

7A42 Controls:
No change.



Test Equipment Controls:
Digital Multimeter
Range/Function..... 200 Ω

4286-419

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Connect the meter leads to the CH1 input connector (black to ground, and red to center conductor).

d. **CHECK**—for a digital multimeter reading of 50 ohms, within the limits of 49 to 51 ohms.

e. Press the CH2 button (button light on).

f. Repeat parts b through e for CH2, CH3, and CH4; for each successive channel to be checked, first press the DISPLAY button, the channel button of the channel to be checked, the DISPLAY button, and the TRIG VIEW button, respectively. Then proceed to part b.

g. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

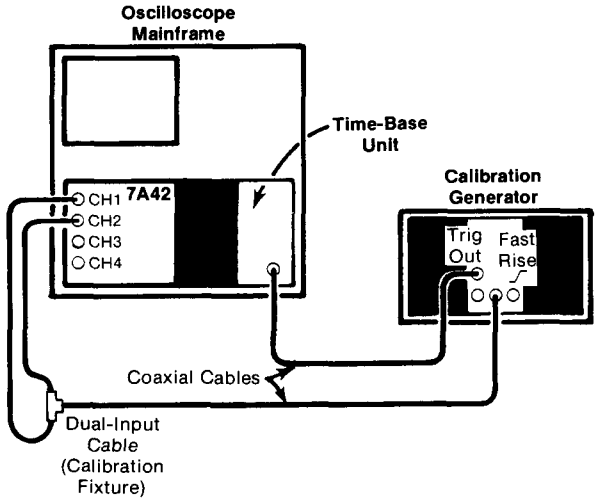
A7. CHECK DIFFERENTIAL DELAY BETWEEN CHANNELS

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A7. SETUP CONDITIONS

7A42 Controls:
No change.



NOTE
Mark the CH1 leg of the Dual-Input Cable with a piece of tape for future reference.

Test Equipment Controls:

Calibration Generator
- Mode ..... Fast Rise
- Period ..... 1 μs

Time-Base Unit
- Time/Div ..... 5 ns
- Triggering
  - Mode ..... Auto
  - Coupling ..... Dc
  - *Source* ..... Ext
- Mag ..... In (X1)
- Ext Trig In ..... Out 50 Ω

4286-420

NOTE

The amplifiers gain and compensation must be properly adjusted for this check to pass the performance requirement.

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the upper VOLTS/DIV button until a readout of 20 mV is displayed on the crt.

e. Press the PROG TRIG button (button light on).

f. Press the CLEAR button to extinguish all TRIGGER FUNCTION lights.

g. Press the PROG CHAN button (button light off).

h. Press the CH2 button (button light on).

i. Press the TTL/ECL button (CH2 ECL TTL light off).

j. Press the DISPLAY button (CH2 DISPLAY light on).

k. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

l. Press the upper VOLTS/DIV button until a readout of 20 mV is displayed on the crt.

m. Set the time-base unit Triggering Level control for a stable display, centered on the screen.

n. Set the calibration generator Pulse Amplitude control to display 5 divisions of signal amplitude on both displayed signals. Rotate the CH1 and CH2 POSITION controls to superimpose the two traces (one over the other) at the 0% and 100% points of the pulse.

o. Release the time-base unit Mag button to the Out X10 position (500 ps sweep speed).

p. Note the time (in divisions) at the 50% amplitude level that the CH1 trace leads or lags the CH2 trace (i.e., if the CH1 trace leads by 0.2 div, record +0.2; if CH1 lags by that amount, record -0.2).

q. Reverse the two legs of the dual-input cable, so that the leg previously marked with tape is on the CH2 input connector.

r. Repeat part p.

s. **CHECK**—the differential delay; first add the two values noted, then divide the sum by 2. The computed value should be 0.4 division or less.

t. Repeat parts b through s for all combinations of all channels (six combinations total).

u. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

B. TRIGGER VIEW TRACE

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
2. Time-Base Unit
5. HF Pulse Generator
13. Dual-Input Cable (Calibration Fixture)
14. Coaxial Cable
22. 10X Attenuator

B1. PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

c. Set the time base unit controls:

Triggering
Mode ..... Auto
Coupling ..... Dc
Source ..... Int
Mag ..... In (X1)

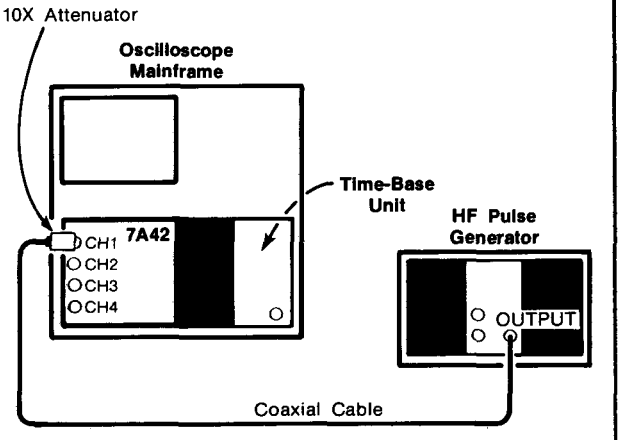
B2. CHECK TRIGGER VIEW AMPLITUDE

NOTE

First perform step B1, then proceed.

B2. SETUP CONDITIONS

7A42 Controls:
TRIGGER FILTER ..... OFF
TRIG VIEW ..... Press (button light on)



Test Equipment Controls:
HF Pulse Generator
Pulse Duration ..... Sq Wave (Int Period)
Variable X1
Period ..... 1 μs
Variable X1

Time-Base Unit
Time/Div ..... 0.2 μs

4286-421

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the GND button (CH1 GND light on). Set the CH1 trace 1 division above the center horizontal graticule line.

e. Press the GND button (CH1 GND light off).

f. Set the HF pulse generator High Level Output control to position the top of the square wave 0.8 division below the GND Reference Level. Refer to Figure 4-2.

g. Set the HF pulse generator Low Level Output Control to position the bottom of the square wave 1.7 divisions below the GND Reference Level. Refer to Figure 4-2.

h. Set the time-base unit Triggering Level control as necessary for a stable display.

i. **CHECK**—the trigger view waveform for an amplitude of 0.35 division, within the limits of 0.25 to 0.45 division.

j. Move the 10X Attenuator signal from the CH1 input to the CH2 input connector.

k. Press the DISPLAY button (CH1 DISPLAY light off).

l. Press the PROG TRIG button (button light on).

m. Press the CLEAR button.

n. Press the CH2 button (CH2 button light on).

o. Press the PROG CHAN button (button light off).

p. Press the CH2 button (CH2 button light on).

q. Press the DISPLAY button (CH2 DISPLAY light on).

r. Rotate the CH2 POSITION control to position the trace on the screen.

s. Press the TTL/ECL button (Ch2 ECL TTL button light off).

t. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

u. **CHECK**—the trigger view waveform for an amplitude of 0.35 division, within the limits of 0.25 to 0.45 division.

v. Repeat parts j through u for CH3 and CH4.

w. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

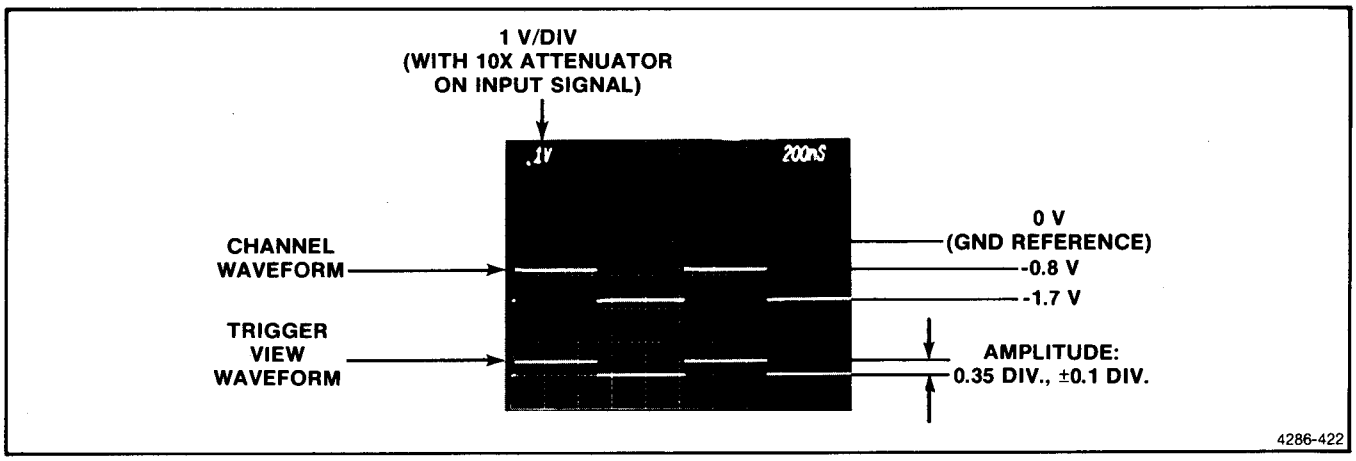


Figure 4-2. Trigger view waveform amplitude with ECL input signal.

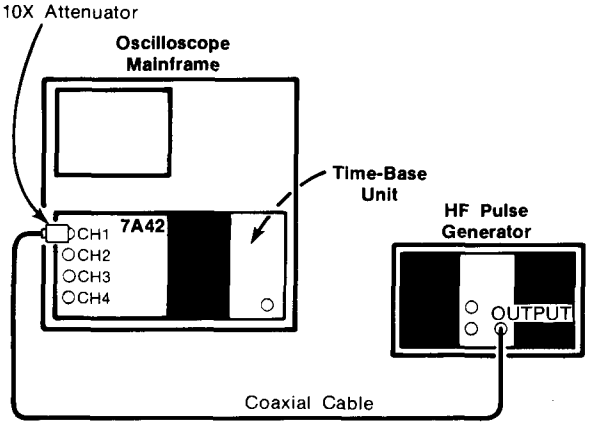
B3. CHECK TRIGGER VIEW-TIME COINCIDENCE WITH CHANNEL DISPLAY

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B3. SETUP CONDITIONS

7A42 Controls:
TRIGGER FILTER ..... OFF



Test Equipment Controls:
HF Pulse Generator
Pulse Duration ..... Sq Wave (Int Period)
Variable X1
Period ..... 0.1 μs
Variable X1
Back Term ..... On (pull button out)

Time-Base Unit
Time/Div ..... 20 ns
Mag ..... Out (X10)

4286-423

NOTE

The Amplifier Gain and Trigger Threshold adjustments must be properly adjusted for this check to pass the performance requirements.

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the CH2 button (button light on).

e. Press the TTL/ECL button (CH2 ECL TTL light off).

f. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

g. Press the CH3 button (button light on).

h. Press the TTL/ECL button (CH3 ECL TTL light off).

i. Press the 1MΩ/50Ω button (CH3 50Ω 1MΩ 15pf light off).

j. Press the CH4 button (button light on).

k. Press the TTL/ECL button (CH4 ECL TTL light off).

l. Press the 1MΩ/50Ω button (CH4 50Ω 1MΩ 15pf light off).

m. Press the CH1 button (button light on).

n. Press the TRIG VIEW button (button light on).

o. Press the GND button (CH1 GND light on). Set the CH1 trace 1 division above the center horizontal graticule line.

p. Press the GND button (CH1 GND light off).

q. Set the HF pulse generator High Level Output control to position the top of the square wave 0.8 division below the GND Reference Level. Refer to Figure 4-3.

r. Set the HF pulse generator Low Level Output control to position the bottom of the square wave 1.7 divisions below the GND Reference Level. Refer to Figure 4-3.

s. Set the time-base unit Triggering Level control as necessary for a stable display.

t. Set the time-base unit Time/Div to 2 ns.

u. Set the time-base unit Position control to position the 50% amplitude level of the Trigger View Transition to the center vertical graticule line. Refer to Figure 4-3.

v. Press the PROG TRIG button (button light on).

w. Press the CLEAR button.

x. Press the CH1 button.

y. **CHECK**—that the channel transition 50% amplitude level is within 1.5 divisions of the 50% amplitude level on the trigger view transition. Refer to Figure 4-3.

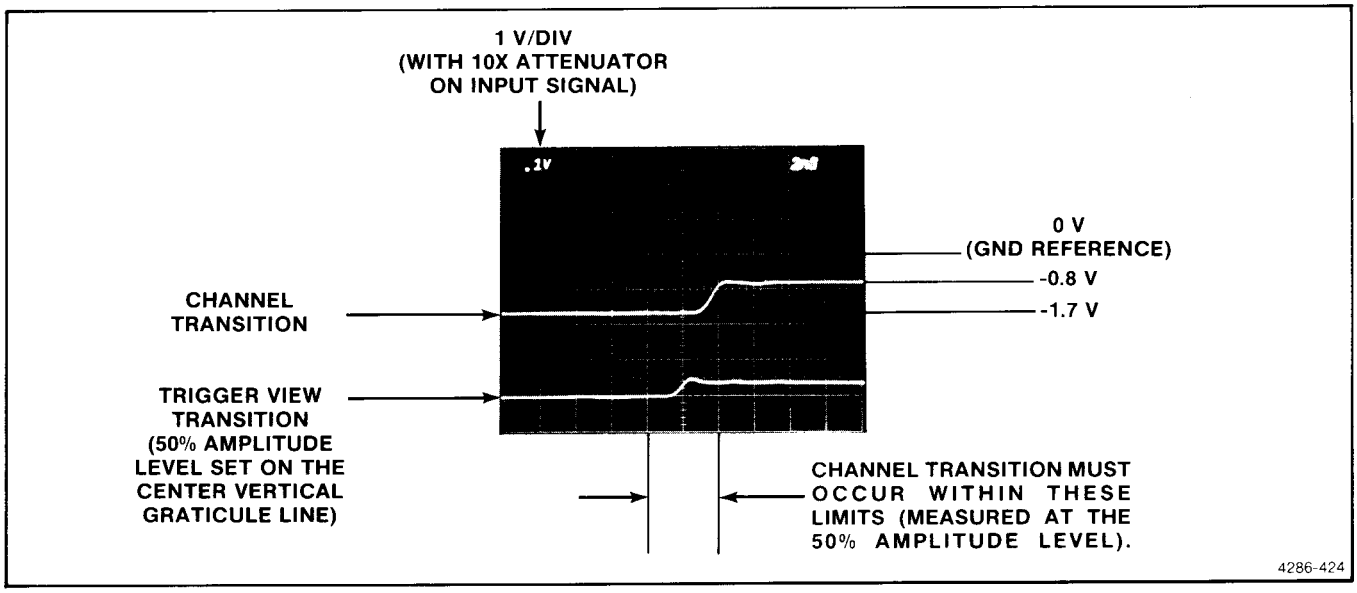


Figure 4-3. Trigger view and channel transition time coincidence.

z. Press the NOT button.

aa. **CHECK**—repeat part y.

bb. Press the EDGE button.

cc. **CHECK**—repeat part y.

dd. Press the NOT button.

ee. **CHECK**—repeat part y.

ff. Press the CLEAR button.

gg. Press the CH2 button.

hh. Press the NOT button, the OR button, and the CH1 button respectively.

ii. **CHECK**—repeat part y.

jj. Press the NOT button.

kk. **CHECK**—repeat part y.

ll. Press the EDGE button.

mm. **CHECK**—repeat part y.

nn. Press the NOT button.

oo. **CHECK**—repeat part y.

pp. Press the CLEAR button.

qq. Press the B button (button light on).

rr. Repeat parts x through pp.

ss. Move the HF pulse generator Output signal from the CH1 input to the CH2 input connector.

tt. Press the PROG CHAN button (button light off).

uu. Press the DISPLAY button (CH1 DISPLAY light off).

vv. Press the CH2 button (button light on).

ww. Press the DISPLAY button (button light on).

xx. Press the PROG TRIG button (button light on).

yy. Press the CLEAR button, and the CH2 button (red CH2 TRIGGER FUNCTION light on).

zz. Press the PROG CHAN button (button light off).

aaa. Repeat parts o through ss for CH2, CH3 and CH4.

bbb. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

C. THRESHOLD AND PROBE OFFSET

Equipment Required: (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
2. Time-Base Unit
3. Calibration Generator
4. Digital Multimeter
6. Function Generator
10. Power Supply
14. Coaxial Cable
17. Patch Cords (Two Required)
18. Meter Leads
22. 10X Attenuator
23. 50Ω Feedthrough Terminator

C1. PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

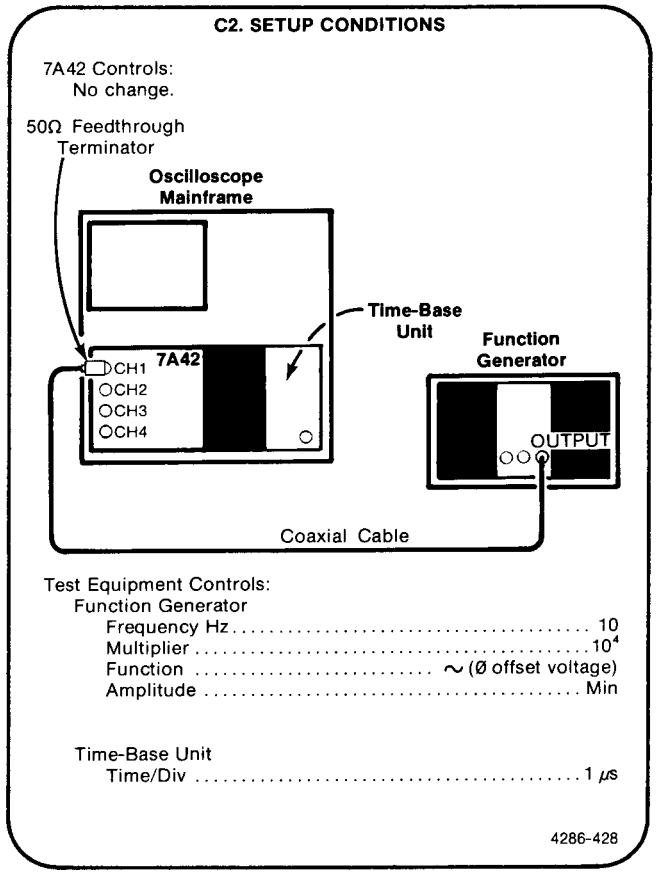
c. Set the time-base unit controls:

Triggering
Mode ..... Auto
Coupling ..... Dc
Source ..... Int
Mag ..... In (X1)

C2. CHECK THRESHOLD VOLTAGE RANGE

NOTE

First perform step C1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the GND button (CH1 GND light on).

e. Center the trace (zero-volt level) exactly on the center horizontal graticule line.

f. Press the GND button (CH1 GND light off).

g. Set the function generator Amplitude control to display 5 divisions of amplitude, centered on the graticule.

h. Press the THRESH button (button light on).

i. Press the LEVEL⇧ button to display .000 on the SWITCHING THRESHOLD readout; the sine wave should now be triggered at the zero-volt level. See Figure 4-4.

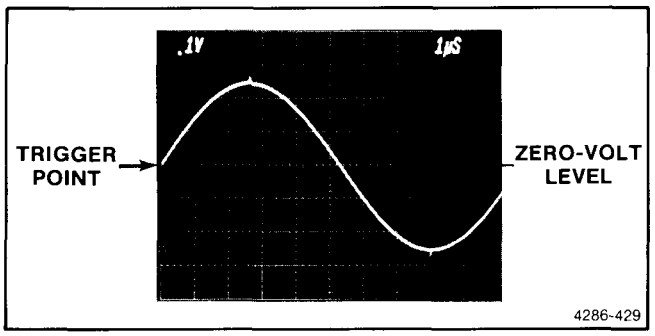


Figure 4-4. 100 kHz sine-wave signal triggered at the zero-volt level.

j. Press the LEVEL⇧ button, and note the Trigger Point moves up the sine wave.

k. **CHECK**—that the trace freeruns (does not trigger) just as the SWITCHING THRESHOLD readout reaches the limit of .256. NOTE: the zero-volt level must be exactly on the center horizontal graticule line.

l. Press the LEVEL⇩ button, and note the Trigger Point moves down the sine wave.

m. **CHECK**—that the trace freeruns (does not trigger) just as the SWITCHING THRESHOLD readout reaches the limit of -.254. NOTE: The zero-volt level must be exactly on the center horizontal graticule line.

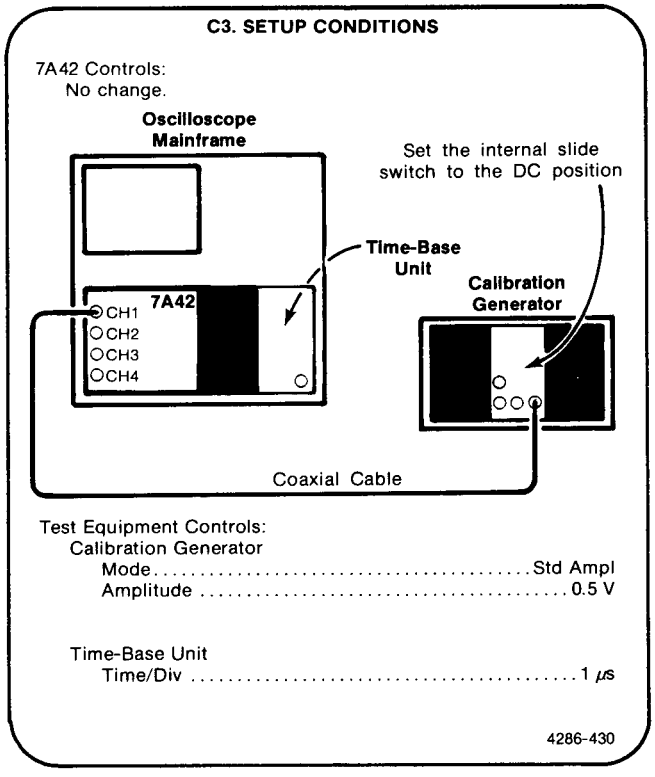
n. NOTE: It is not necessary to check the threshold voltage range of the TTL family. Satisfactory verification of the ECL family threshold voltage range adequately verifies TTL family performance.

o. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

C3. CHECK THRESHOLD ACCURACY

NOTE

If the preceding step was not performed, first perform step C1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the GND button (CH1 GND light on).

e. Press the THRESH button (button light on).

f. Press the LEVEL buttons for a SWITCHING THRESHOLD readout of .000.

g. Press the TRIG VIEW button (button light on).

h. Move the SWITCHING THRESHOLD voltage level up and down from the .000 volt level, using the LEVEL buttons, and note that the trigger view trace dc level shifts.

i. Record the SWITCHING THRESHOLD voltage levels at which the two shifts occur.

j. **CHECK**—the average of the two values recorded in part i should be .000 volt within the limits of ±.001 volt.

k. Press the GND button (CH1 GND light off).

l. Press the LEVEL button to move the SWITCHING THRESHOLD readout to .250 VOLTS.

m. Move the SWITCHING THRESHOLD voltage level up and down from the .250 volt level, using the LEVEL buttons.

n. **CHECK**—that the trigger view trace dc level shifts between high and low at .250 volts, within the limits of .244 and .256 volts, as read on the SWITCHING THRESHOLD readout display.

o. Press the DISPLAY button (CH1 DISPLAY light off).

p. Press the CH2 button (button light on).

q. Press the DISPLAY button (CH2 DISPLAY light on).

r. Press the TTL/ECL button (CH2 ECL TTL light off).

s. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

t. Press the GND button (CH2 GND light on).

u. Press the PROG TRIG button (button light on).

v. Press the CLEAR button.

w. Press the CH2 button (red CH2 TRIGGER FUNCTION light on).

x. Press the PROG CHAN button (button light off).

y. Move the coaxial cable input signal to the CH2 input connector.

z. Repeat parts f through m for CH2, CH3, and CH4.

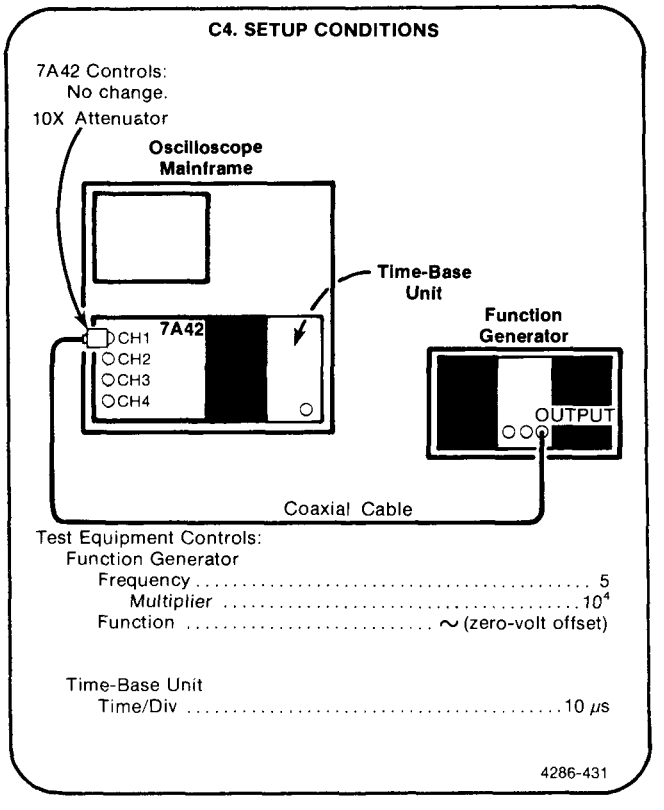
aa. NOTE: It is not necessary to check the threshold accuracy of the TTL family. Satisfactory verification of the ECL family threshold accuracy adequately verifies TTL family performance.

bb. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

C4. CHECK THRESHOLD HYSTERESIS

NOTE

If the preceding step was not performed, first perform step C1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the upper VOLTS/DIV button for a readout display of .1 V on the crt.

d. Set the function generator Amplitude control to display exactly 4 divisions of signal amplitude, centered on the crt graticule.

e. Set the time-base unit Time/Div to 1 μs.

f. Press the THRESH button (button light on).

g. Press the TRIG VIEW button (button light on).

h. Press the LEVEL buttons to display 0.00 on the SWITCHING THRESHOLD readout.

i. Set the 7A42 CH1 POSITION control and the time-base Position control to position the start of the trace as shown in Figure 4-5.

j. Set the time-base unit Variable Time/Div control to position the falling edge of the trigger view trace to a vertical graticule line. Refer to Figure 4-5.

k. **CHECK**—that the hysteresis level (see Fig. 4-5) is 0.4 division, within the limits of 0.2 to 0.48 division.

l. Move the 10X attenuator signal from the CH1 input to the CH2 input connector.

m. Press the DISPLAY button (CH1 DISPLAY light off).

n. Press the PROG TRIG button (button light on).

o. Press the CLEAR button.

p. Press the CH2 button (red CH2 TRIGGER FUNCTION light on).

q. Press the PROG CHAN button (button light off).

r. Press the CH2 button (button light on).

s. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

t. Press the DISPLAY button (CH2 DISPLAY light on).

u. Press the upper VOLTS/DIV button for a readout display .1 V on the crt.

v. Set the function generator Amplitude control to display exactly 4 divisions of signal amplitude, centered on the crt graticule.

w. Press the LEVEL buttons to display 0.00 on the SWITCHING THRESHOLD readout.

x. Set the 7A42 CH1 POSITION control and the time-base Position control to position the start of the trace as shown in Figure 4-5.

y. Set the time-base unit Variable Time/Div control to position the falling edge of the trigger view trace to a vertical graticule line. Refer to Figure 4-5.

z. **CHECK**—that the hysteresis level (see Fig. 4-5) is 0.4 division, within the limits of 0.2 to 0.48 division.

aa. Repeat parts l through z for CH3 and CH4.

bb. NOTE: It is not necessary to check the hysteresis level of the ECL family. Satisfactory verification of the TTL family hysteresis levels adequately verifies ECL family performance.

cc. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

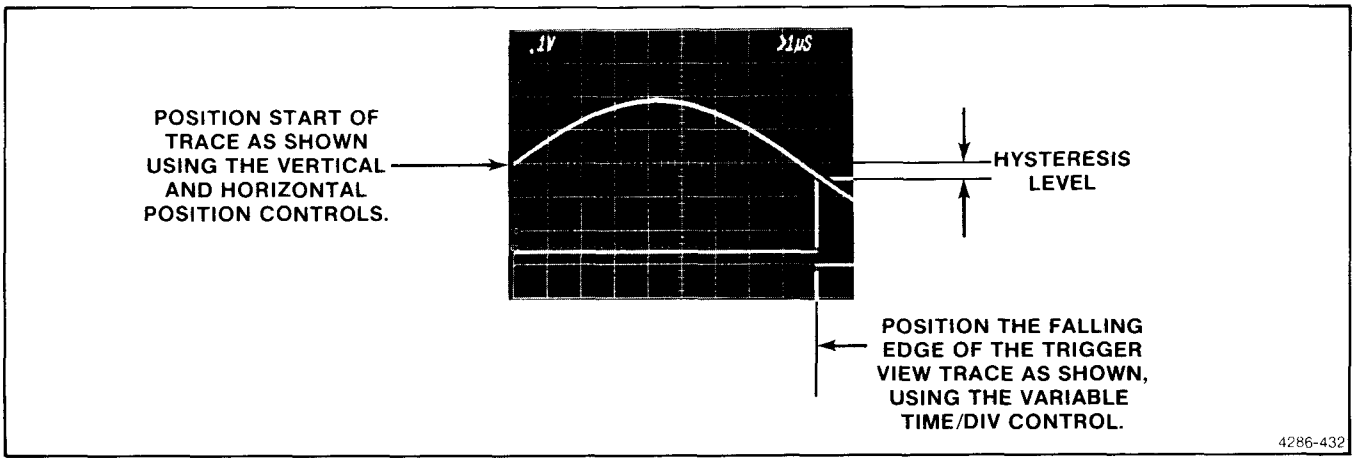


Figure 4-5. Typical waveform display for measuring the hysteresis level.

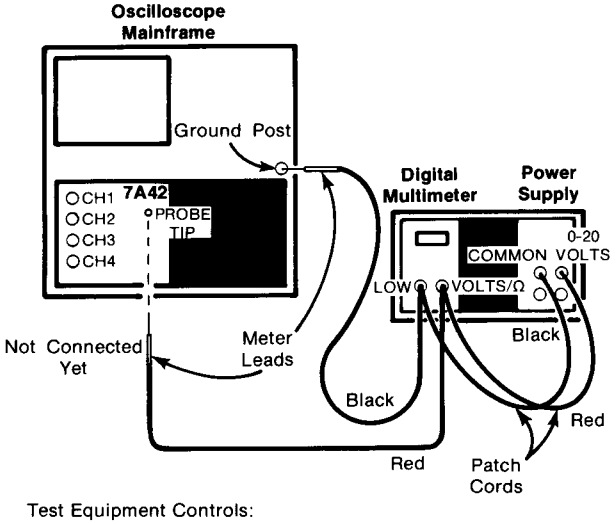
C5. CHECK PROBE-TIP INPUT VOLTAGE ACCURACY

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C5. SETUP CONDITIONS

7A42 Controls:
No change.



Test Equipment Controls:
Digital Multimeter
Range/Function ..... 20 V dc

Power Supply
Output ..... On (pressed in)
+ Volts ..... Ø
Current Limit ..... Min
-Volts ..... Ø
Current Limit ..... Min

4286-433

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the THRESH button (button light on).

c. Press the PROBE OFFSET button (red button light on).

d. Set the power supply +Volts control for a reading of +2.00 volts on the digital multimeter.

e. Connect the red meter lead to the PROBE TIP connector.

f. **CHECK**—the SWITCHING THRESHOLD readout display for a reading of +1.94 to +2.06 volts.

g. Set the power supply +Volts control for a reading of +5.00 volts on the digital multimeter.

h. **CHECK**—the SWITCHING THRESHOLD readout display for a reading of +4.88 to +5.12 volts.

i. Move the red patch cord from the +dc voltage source, to the -dc voltage source on the power supply.

j. Repeat parts d through h using the -Volts control on the power supply.

k. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

D. EXTERNAL CLOCK

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
2. Time-Base Unit
5. HF Pulse Generator
6. Function Generator
9. LF Pulse Generator
13. Dual-Input Cable
14. Coaxial Cable (Three Required)
19. Adapter, BNC T
20. Adapter, Female-to-Female (Two Required)
21. 2X Attenuator (Two Required)
22. 10X Attenuator
23. 50Ω Feedthrough Terminator

D1. PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

c. Set the time-base unit controls:

Triggering
- Mode ..... Auto
- Coupling ..... Dc
- Source ..... Int

Mag ..... In (X1)

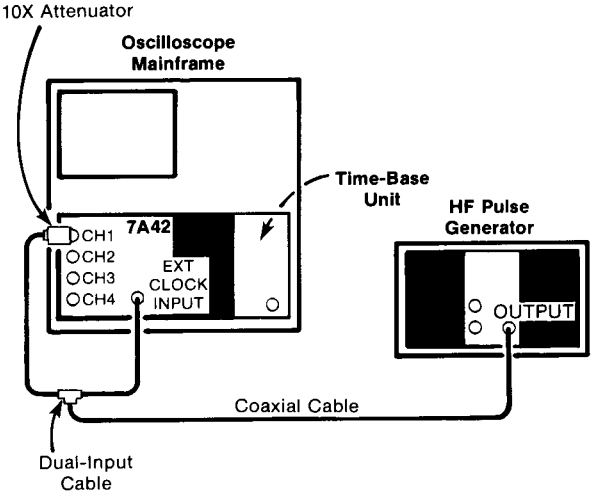
D2. CHECK EXT CLOCK VIEW-TIME COINCIDENCE WITH CHANNEL DISPLAY

NOTE

First perform step D1, then proceed.

D2. SETUP CONDITIONS

7A42 Controls:
First, remove the 7A42 from the oscilloscope mainframe. Then move the J634 External Clock Jumper (link-plug) to the "ECL" position, as shown in Figure 4-6. Replace the 7A42 in the oscilloscope mainframe.



Test Equipment Controls:

HF Pulse Generator
- Pulse Duration ..... Sq Wave (Int Period)
- Variable X1
- Period ..... 0.1 μs
- Variable X1
- Back Term ..... On (pull button out)

Time-Base Unit
- Time/Div ..... 5 ns

4286-425

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the TRIG VIEW button (button light on).

e. Press the GND button (CH1 GND light on). Set the CH1 trace 1 division above the center horizontal graticule line.

f. Press the GND button (CH1 GND light off).

g. Set the HF pulse generator High Level Output control to position the top of the square wave 0.8 division below the GND Reference Level. Refer to Figure 4-7.

h. Set the HF pulse generator Low Level Output control to position the bottom of the square wave 1.7 divisions below the GND Reference Level. Refer to Figure 4-7.

i. Set the time-base unit Triggering Level control as necessary for a stable display.

j. Press the PROG TRIG button (button light on).

k. Press the CLEAR button.

l. Press the CH2 button (red CH2 TRIGGER FUNCTION light on).

m. Press the OR button, the NOT button, and the CH2 button (green CH2 TRIGGER FUNCTION light on).

n. Press the EXT CLOCK SYNC button (button light on).

o. **CHECK**—that the Ext Clock View Transition (measured at the 50% amplitude levels) occurs simultaneously with the Channel Transition, within 1 division. Refer to Figure 4-7.

p. Press the ⌥ button (button light off).

q. **CHECK**—that the Ext Clock View Transition (measured at the 50% amplitude levels) occurs simultaneously with the Channel Transition, within 1 division.

r. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

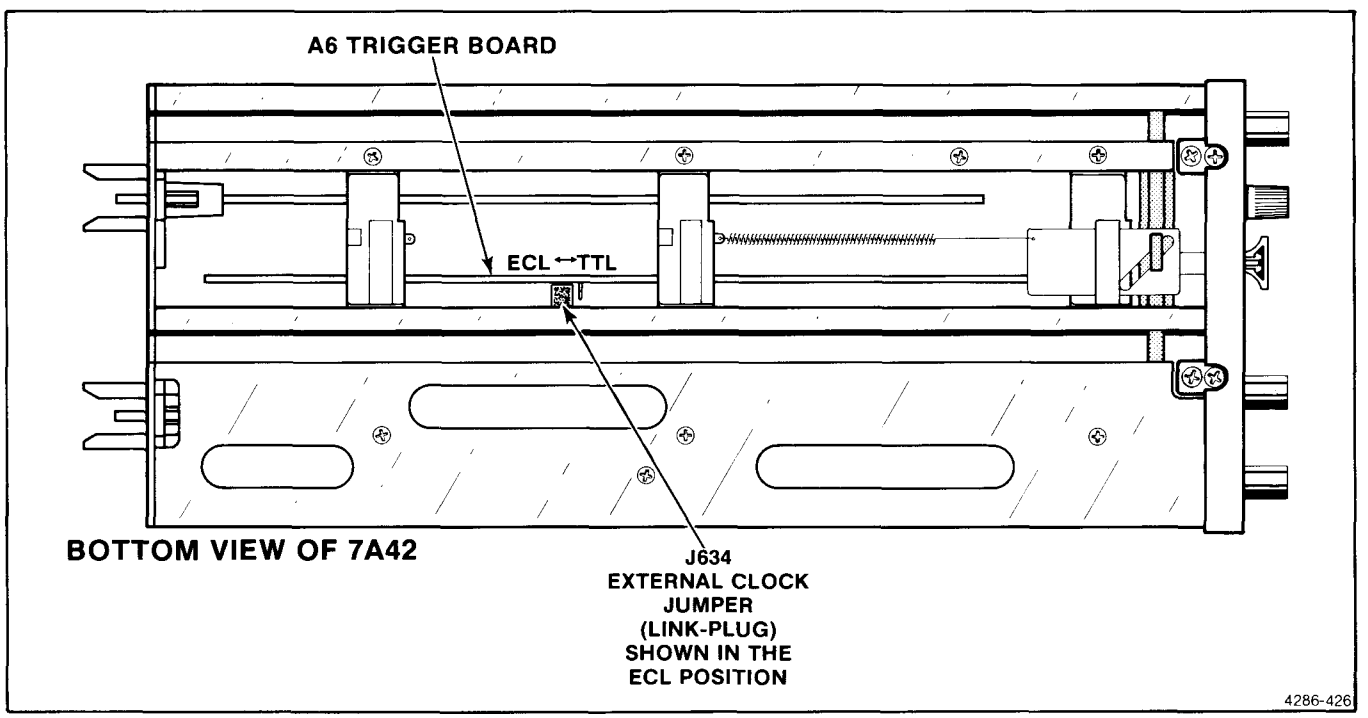


Figure 4-6. Location of J634 External Clock Jumper (link-plug) on the A6 Trigger Board.

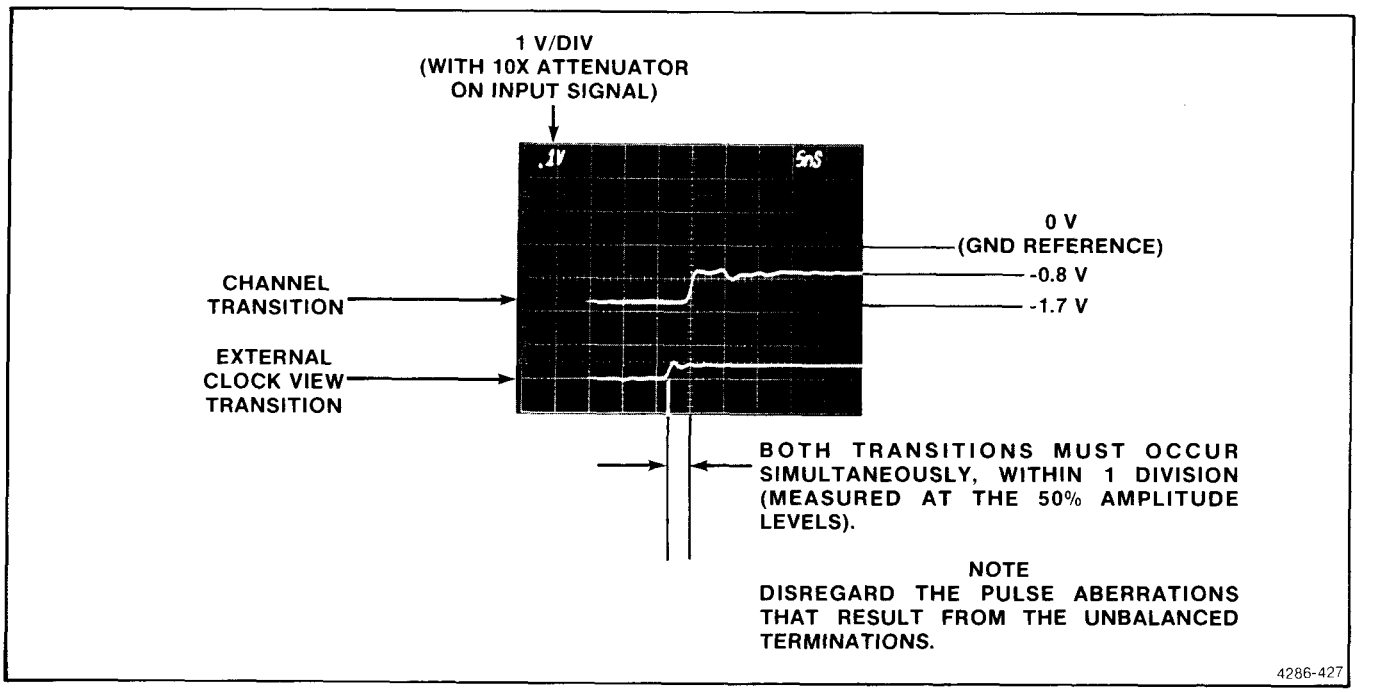


Figure 4-7. External clock view and channel transition time coincidence.

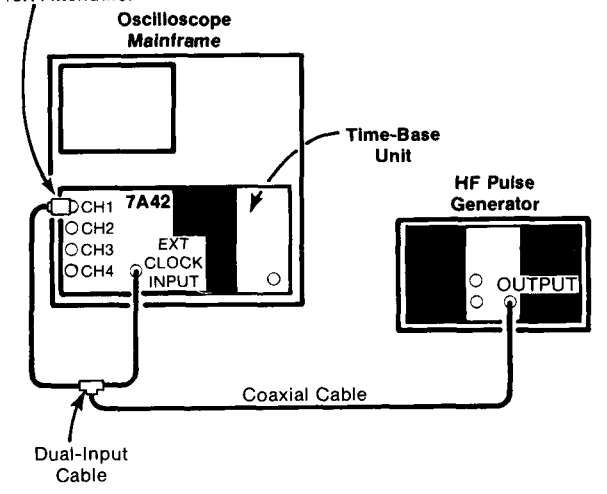
D3. CHECK MINIMUM EXTERNAL CLOCK WIDTH

NOTE

If the preceding step was not performed, first perform step D1, then proceed.

D3. (ECL) SETUP CONDITIONS

7A42 Controls:
First, remove the 7A42 from the oscilloscope mainframe. Then move the J634 External Clock Jumper (link-plug) to the "ECL" position, as shown in Figure 4-6. Replace the 7A42 in the oscilloscope mainframe.



Test Equipment Controls:

HF Pulse Generator
- Pulse Duration ..... 5 ns
- Variable X1
- Period ..... 1 μs
- Variable ..... X5 (midrange)
- Back Term ..... On (pull button out)
- Output ..... Norm + (complement button out)

Time-Base Unit
- Time/Div ..... 10 ns

4286-436

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe off, then back on again.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the TTL/ECL button (CH1 ECL TTL light off).

d. Press the TRIG VIEW button (button light on).

e. Press the PROG TRIG button (button light on).

f. Press the B button (button light on).

g. Press the CH2 button (red CH2 TRIGGER FUNCTION light on).

h. Press the OR button, the NOT button, and the CH2 button (green CH2 TRIGGER FUNCTION light on).

i. Press the A button (button light on).

j. Press the PROG CHAN button (button light off).

k. Press the GND button (CH1 GND light on).

l. Set the CH1 trace 1 division above the center horizontal graticule line.

m. Press the GND button (CH1 GND light off).

n. Set the HF pulse generator High Level Output control to position the top of the pulse to 0.8 division below the GND Reference Level. Refer to Figure 4-8.

o. Set the HF pulse generator Low Level Output control to position the bottom of the pulse 1.7 divisions below the GND Reference Level. Refer to Figure 4-8.

p. Press the B button (button light on).

q. Press the EXT CLOCK SYNC button (button light on).

r. **CHECK**—that the waveform display remains triggered.

s. Press the CH2 button (button light on).

t. Press the TTL/ECL button (CH2 ECL TTL light off).

u. **CHECK**—that the waveform display remains triggered.

v. Press the A button (button light on).

w. Press the PROG TRIG button (button light on).

x. Press the CLEAR button.

y. Press the CH2 button, the OR button, the NOT button, and the CH2 button, respectively.

z. Press the PROG CHAN button (button light off).

aa. **CHECK**—that the waveform display remains triggered.

bb. Press the TTL/ECL button (CH2 ECL TTL light on).

cc. **CHECK**—that the waveform display remains triggered.

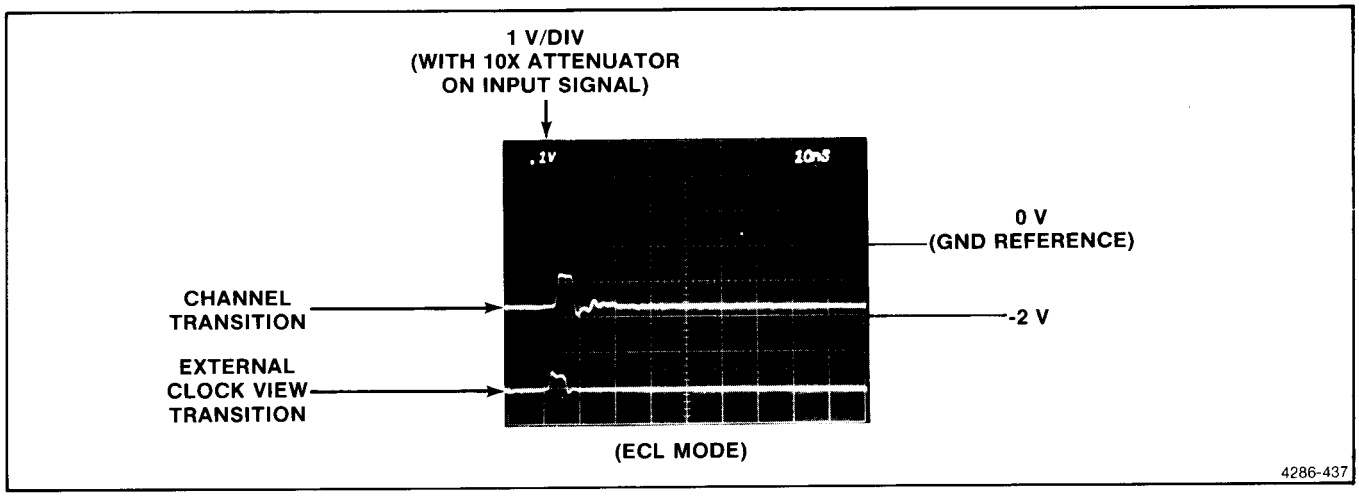


Figure 4-8. Typical external clock transition display in the ECL mode.

dd. Turn the mainframe oscilloscope Power off.

ee. Disconnect the dual-input cable from the 7A42.

ff. Remove the 7A42 from the oscilloscope mainframe and move the J634 External Clock Jumper (link-plug) from the ECL position to the TTL position. Refer to Figure 4-6. Reinstall the 7A42 in the oscilloscope mainframe, and turn the oscilloscope mainframe Power back on.

gg. Perform the setup instructions as shown in the D3. (TTL) Setup Conditions.

hh. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

ii. Press the TRIG VIEW button (button light on).

jj. Press the PROG TRIG button (button light on).

kk. Press the B button (button light on).

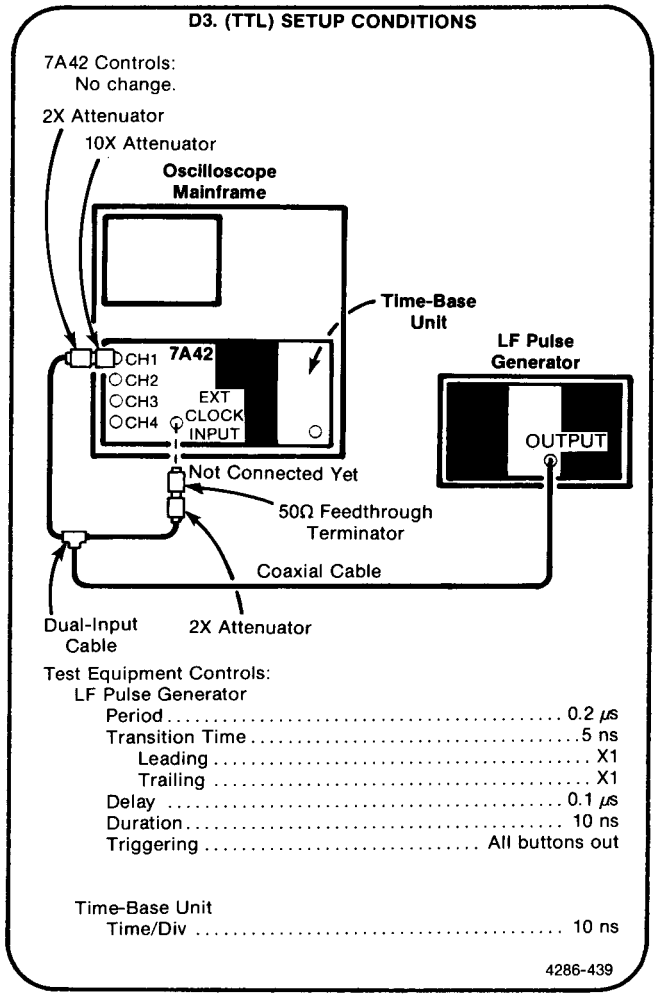
ll. Press the CH2 button (red CH2 TRIGGER FUNCTION light on).

mm. Press the OR button, the NOT button, and the CH2 button, respectively (green CH2 TRIGGER FUNCTION light on).

nn. Press the A button (button light on).

oo. Press the PROG CHAN button (button light off).

pp. Press the upper VOLTS/DIV button for a readout display of .1 V on the crt.



qq. Press the GND button (CH1 GND light on).

rr. Set the CH1 POSITION control to position the trace to the center horizontal graticule line.

ss. Press the GND button (CH1 GND light off).

tt. Set the LF pulse generator Low Level Output control to position the pulse baseline to the center horizontal graticule line.

uu. Set the LF pulse generator High Level Output control to position the top of the pulse to the third horiozntal graticule line above the GND Reference Level. Refer to Figure 4-9.

vv. Set the LF pulse generator Duration Cal control to display a trigger view pulse width of 2 divisions (20 ns), measured at the 50% amplitude points.

ww. Connect the open-leg of the dual-input cable to the EXT CLOCK INPUT.

xx. Press the EXT CLOCK SYNC button (button light on).

yy. Press the B button (button light on).

zz. **CHECK**—that the waveform display remains triggered.

aaa. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

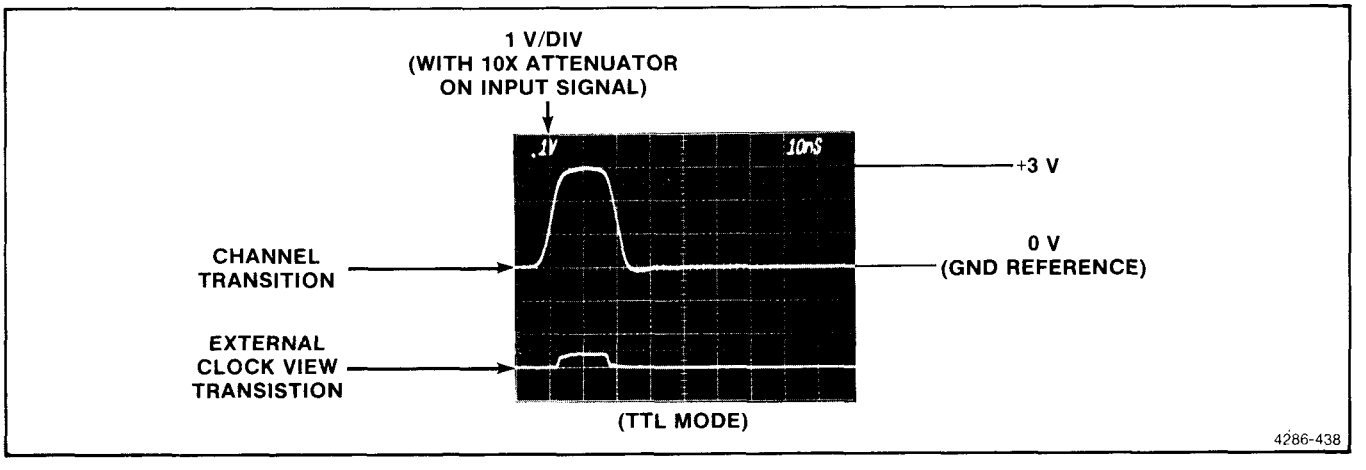


Figure 4-9. Typical external clock transition display in the TTL mode.

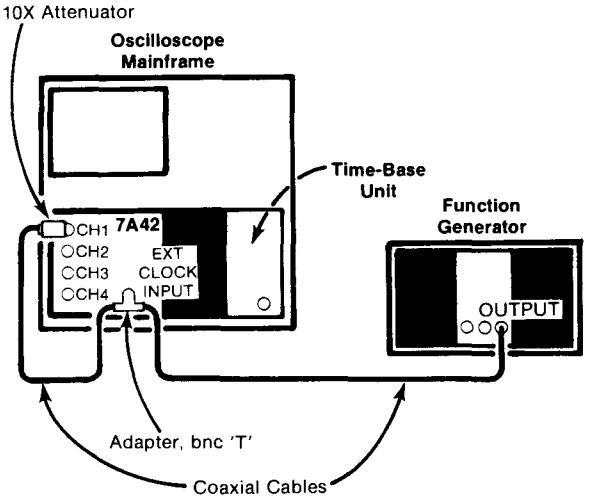
D4. CHECK EXTERNAL CLOCK INPUT THRESHOLDS

NOTE

If the preceding step was not performed, first perform step D1, then proceed.

D4. SETUP CONDITIONS

7A42 Controls:
First, remove the 7A42 from the oscilloscope mainframe. Then move the J634 External Clock Jumper (link-plug) to the "ECL" position, as shown in Figure 4-6. Replace the 7A42 in the oscilloscope mainframe, and turn the Power on.



Test Equipment Controls:

Function Generator
- Function (DC Offset) ..... ~
- Offset ..... Midrange
- Frequency (Hz) 10
- Multiplier ..... 10^4
- Amplitude ..... Min

Time-Base Unit
- Time/Div ..... 1 μs

4286-440

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the upper VOLTS/DIV button to display 50 mV on the crt readout.

e. Press the THRESH button (button light on, with a SWITCHING THRESHOLD readout of -.130 VOLTS).

f. Press the PROG TRIG button (button light on).

g. Press the B button (button light on).

h. Press the CH2 button, the OR button, the NOT button, and the CH2 button, respectively.

i. Press the A button (button light on).

j. Press the PROG CHAN button (button light off).

k. Press the TRIG VIEW button (button light on).

l. Press the GND button (CH1 GND light on).

m. Set the CH1 trace 2 divisions above the center horizontal graticule line.

n. Press the GND button (Ch1 GND light off).

o. Set the function generator Amplitude and Offset controls to display a sine-wave signal from 0 volt (GND Reference) to -2 volts on the crt. Refer to Figure 4-10.

p. Press the B button (button light on).

q. Press the EXT CLOCK SYNC button (button light on).

r. **CHECK**—that the waveform display remains triggered, and that the transition on the trigger view waveform occurs when the channel waveform voltage is within the limits of the -1 V to -1.5 V window. Refer to Figure 4-10.

s. Turn the oscilloscope mainframe Power off. Remove the 7A42 from the oscilloscope mainframe. Move the J634 External Clock Jumper (link-plug) to the TTL position. Refer to Figure 4-6. Replace the 7A42 in the oscilloscope mainframe, and turn the Power on.

t. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

u. Press the upper VOLTS/DIV button to display .1 V on the crt readout.

v. Press the THRESH button (button light on, with a SWITCHING THRESHOLD readout of 0.14 VOLTS.

w. Press the PROG TRIG button (button light on).

x. Press the B button (button light on).

y. Press the CH2 button, the OR button, the NOT button, and the CH2 button, respectively.

z. Press the A button (button light on).

aa. Press the PROG CHAN button (button light off).

bb. Press the TRIG VIEW button (button light on).

cc. Press the GND button (CH1 GND light on).

dd. Set the CH1 trace to the center horizontal graticule line.

ee. Press the GND button (CH1 GND light off).

ff. Set the function generator Amplitude and Offset controls to display a sine-wave signal from 0 volt (GND Reference) to +3 volts on the crt. Refer to Figure 4-11.

gg. Press the B button (button light on).

hh. Press the EXT CLOCK SYNC button (button light on).

ii. **CHECK**—that the waveform display remains triggered, and that the transition on the trigger view waveform occurs when the channel waveform voltage is within the limits of the +0.8 V to +2 V window. Refer to Figure 4-11.

jj. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

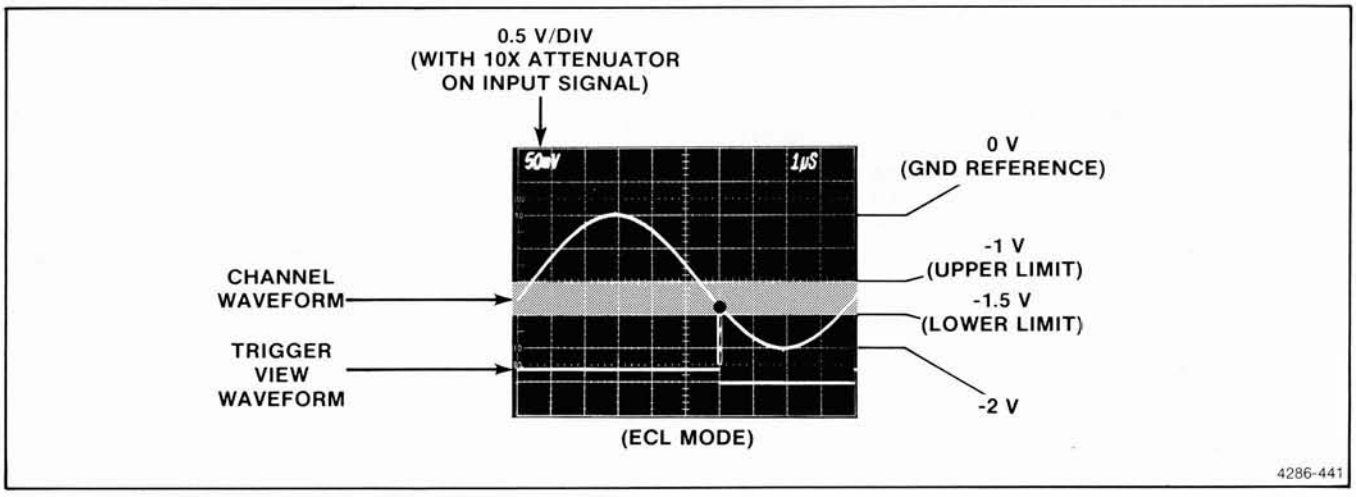


Figure 4-10. Threshold voltage range of the external clock input, in the ECL mode.

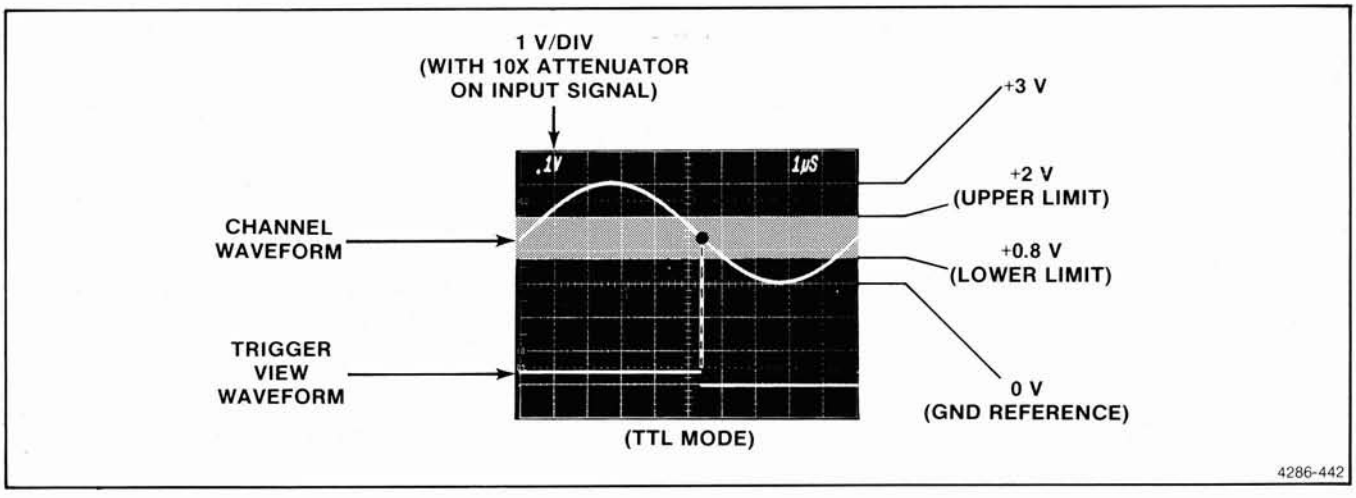


Figure 4-11. Threshold voltage range of the external clock input, in the TTL mode.

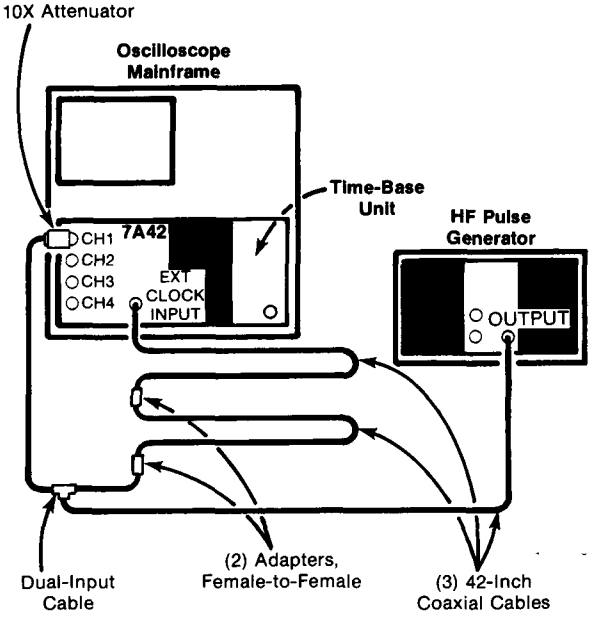
D5. CHECK EXTERNAL CLOCK SETUP TIME

NOTE

If the preceding step was not performed, first perform step D1, then proceed.

D5. SETUP CONDITIONS

7A42 Controls:
First, remove the 7A42 from the oscilloscope mainframe. Then move the J634 External Clock Jumper (link-plug) to the "ECL" position, as shown in Figure 4-6. Replace the 7A42 in the oscilloscope mainframe, and turn the Power on.



Test Equipment Controls:

HF Pulse Generator
- Pulse Duration ..... Sq Wave (Int Period)
- Variable X1
- Period ..... 1 μs
- Variable X1
- Back Term ..... On (pull button out)
- Output ..... Norm + (complement button out)

Time-Base Unit
- Time/Div ..... 1 μs

4286-443

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the TTL/ECL button (CH1 ECL TTL light off).

d. Press the GND button (CH1 GND light on).

e. Set the CH1 trace 1 division above the center horizontal gratiucle line.

f. Press the GND button (CH1 GND light off).

g. Set the HF pulse generator High Level Output control to position the top of the square wave 0.8 division below the GND Reference level.

h. Set the HF pulse generator Low Level Output control to position the bottom of the square wave 1.7 divisions below the GND Reference level.

i. Press the TRIG VIEW button (button light on).

j. Press the EXT CLOCK SYNC button (button light on).

k. **CHECK**—that the displayed waveform remains triggered.

l. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

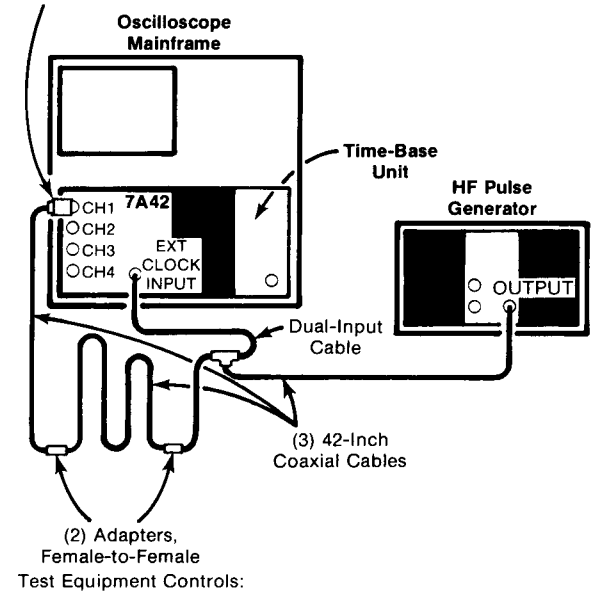
D6. CHECK EXTERNAL CLOCK HOLD TIME

NOTE

If the preceding step was not performed, first perform step D1, then proceed.

D6. SETUP CONDITIONS

7A42 Controls:
First, remove the 7A42 from the oscilloscope mainframe. Then move the J634 External Clock Jumper (link-plug) to the "ECL" position, as shown in Figure 4-6. Replace the 7A42 in the oscilloscope mainframe, and turn the Power on.



Test Equipment Controls:

HF Pulse Generator
- Pulse Duration ..... Sq Wave (Int Period)
- Variable X1
- Period ..... 1 μs
- Variable X1
- Back Term ..... On (pull button out)
- Output ..... Norm + (complement button out)

Time-Base Unit
- Time/Div ..... 0.2 μs

4286-444

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the TTL/ECL button (CH1 ECL TTL light off).

d. Press the PROG TRIG button (button light on).

e. Press the CLEAR button, the NOT button, and the CH1 button, respectively (green CH1 TRIGGER FUNCTION light on).

f. Press the PROG CHAN button (button light off).

g. Press the GND button (CH1 GND light on).

h. Set the CH1 trace 1 division above the center horizontal graticule line.

i. Press the GND button (CH1 GND light off).

j. Set the HF pulse generator High Level Output control to position the top of the square wave to the GND Reference level.

k. Set the HF pulse generator Low Level Output control to posiiton the bottom of the square wave 2 divisions below the GND Reference level.

l. Press the TRIG VIEW button (button light on).

m. Press the EXT CLOCK SYNC button (button light on).

n. **CHECK**—that the displayed waveform remains triggered.

o. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

E. TRIGGER-LEVEL SENSITIVITY

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
2. Time-Base Unit
5. HF Pulse Generator
7. LF Leveled Sine-Wave Generator
14. Coaxial Cable (Two Required)
22. 10X Attenuator
23. 50Ω Feedthrough Terminator

E1. PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

c. Set the time-base unit controls:

Triggering
Mode ..... Auto
Coupling ..... Dc
Source ..... Int
Mag ..... In (X1)

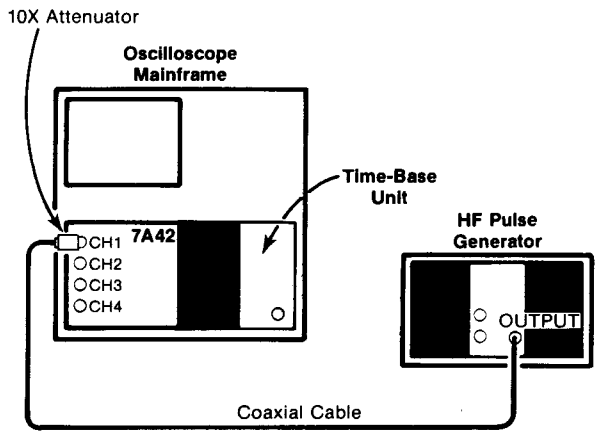
E2. CHECK TRIGGER FILTER

NOTE

First perform step E1, then proceed.

E2. SETUP CONDITIONS

7A42 Controls:
TRIGGER FILTER ..... OFF



Test Equipment Controls:
HF Pulse Generator
Pulse Duration ..... 50 ns
Variable X1
Period ..... 1 μs
Variable X1
Back Term ..... On (pull button out)
Output ..... Norm + (complement button out)

Time-Base Unit
Time/Div ..... 20 ns

4286-434

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

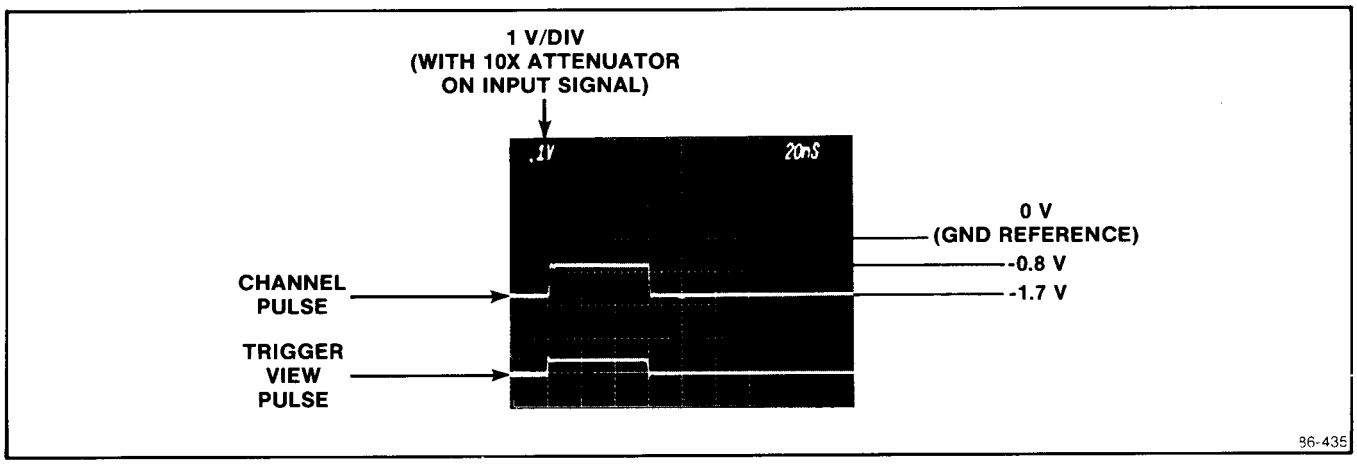


Figure 4-12. Typical trigger view and channel pulse display for checking the trigger filter range.

d. Press the TRIG VIEW button (button light on).

e. Set the HF pulse generator Variable Period control to display 1 pulse per division on the crt graticule.

f. Set the time-base unit Time/Div to 20 ns.

g. Press the GND button (CH1 GND light on).

h. Position the CH1 trace 1 division above the center horizontal gratiucle line.

i. Press the GND button (CH1 GND light off).

j. Set the HF pulse generator High Level Output control to position the top of the pulse 0.8 division below the GND Reference Level. Refer to Figure 4-12.

k. Set the HF pulse generator Low Level Output control to position the bottom of the pulse 1.7 divisions below the GND Reference Level. Refer to Figure 4-12.

l. Set the HF pulse generator Variable Pulse Duration control to display a trigger view pulse width of 3 divisions (60 ns). Refer to Figure 4-12.

m. Turn the TRIGGER FILTER control on, just out of the detent position (minimum on position).

n. **CHECK**—that the trigger view pulse width is reduced not more than 15 ns.

o. Turn the TRIGGER FILTER control OFF (in detent).

p. Set the time-base unit Time/Div to 0.2 μs.

q. Set the HF pulse generator Variable Pulse Duration control to display a trigger view pulse width of 3 divisions (600 ns).

r. Turn the TRIGGER FILTER control out of the detent, to the maximum clockwise position.

s. **CHECK**—that the trigger view pulse width is reduced by at least 300 ns. Record the exact amount of reduction.

t. Press the B button (button light on).

u. Press the PROG TRIG button (button light on).

v. Press the CH1 button (red CH1 TRIGGER FUNCTION light on).

w. Turn the TRIGGER FILTER control OFF (in detent).

x. Set the HF pulse generator Variable Pulse Duration control to display a trigger view pulse width of 3 divisions (600 ns).

y. Turn the TRIGGER FILTER control out of the detent, to the maximum clockwise position.

z. **CHECK**—that the trigger view pulse width is reduced by at least 300 ns. Record the exact amount of reduction.

aa. **CHECK**—find the difference between the values recorded in part s and part y. The difference between these two values must be less than 10% of the sum of the two recorded values.

bb. Turn the TRIGGER FILTER control OFF (in detent).

cc. Set the time-base unit Time/Div to 20 ns.

dd. Set the HF pulse generator Variable Pulse Duration control to display a trigger view pulse width of 3 divisions (60 ns).

ee. Turn the TRIGGER FILTER control on, just out of the detent position (minimum on position).

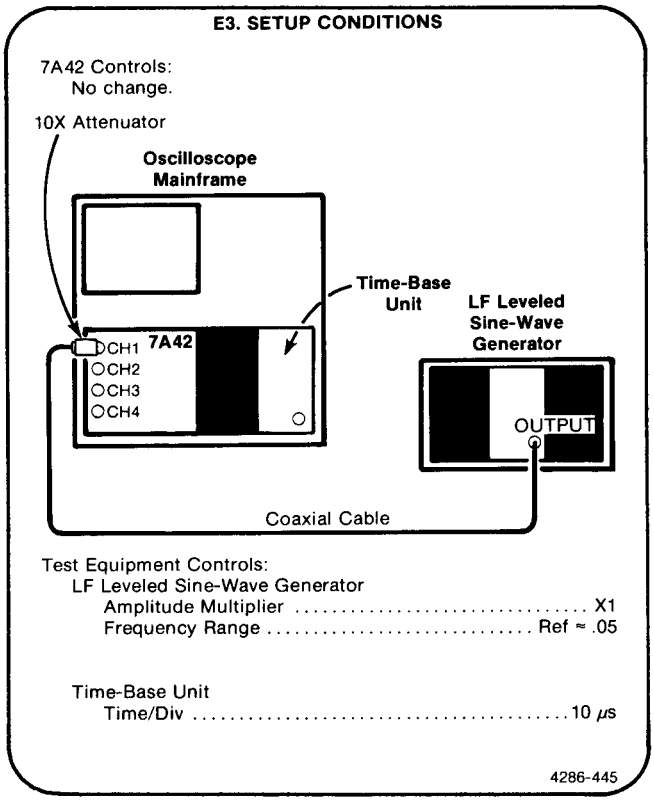
ff. **CHECK**—that the trigger view pulse width is reduced not more than 15 ns.

gg. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

E3. CHECK MAXIMUM TOGGLE FREQUENCY

NOTE

If the preceding step was not performed, first perform step E1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the upper VOLTS/DIV button to display 20 mV on the crt readout.

e. Press the THRESH button (button light on).

f. Press the LEVEL buttons to display .000 on the SWITCHING THRESHOLD readout display.

g. Press the CH2 button (button light on).

h. Press the DISPLAY button (CH2 DISPLAY light on).

i. Press the 1MΩ/50Ω button (50Ω 1MΩ 15pf light off).

j. Press the GND button (CH2 GND light on).

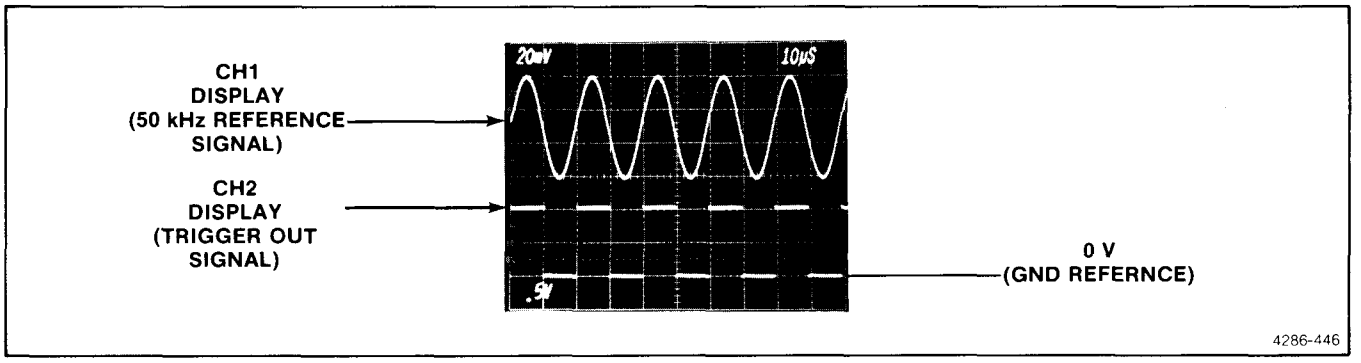


Figure 4-13. Typical waveform display of the 50 kHz reference signal and the resultant trigger output signal.

k. Set the CH2 POSITION control to position the CH2 trace 3 divisions below the center horizontal graticule line.

l. Press the GND button (CH2 GND light off).

m. Set the LF leveled sine-wave generator Output Amplitude control to display 3 divisions of signal on the crt.

n. Connect a coaxial cable from the TRIGGER OUT connector to the CH2 input connector. The trigger output signal should now be displayed in CH2. Refer to Figure 4-13.

o. Increase the LF leveled sine-wave generator frequency to 125 MHz.

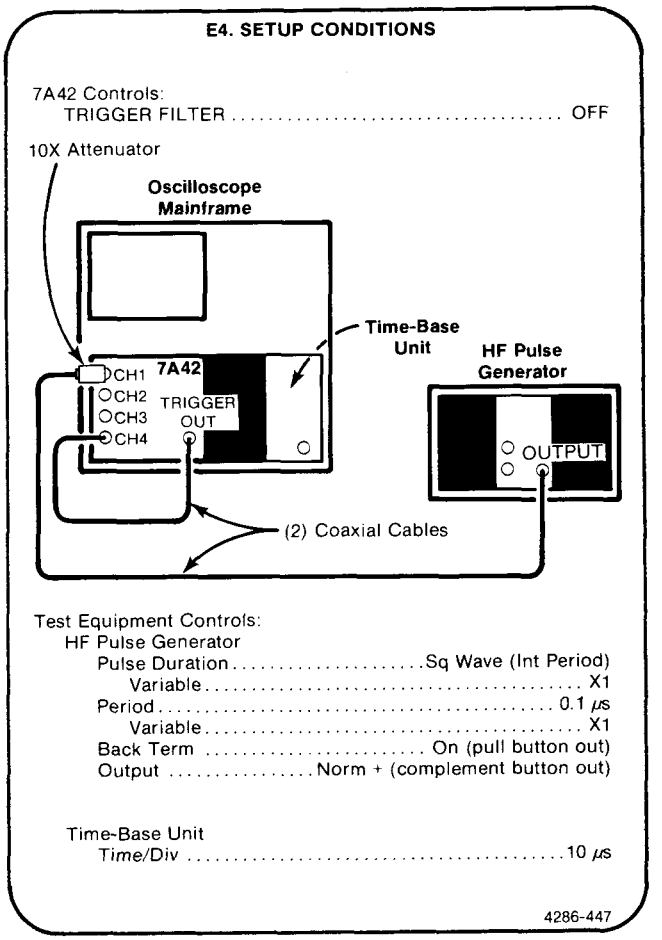
p. **CHECK**—that the waveform display remains triggered, and the triggered output display amplitude remains the same throughout the frequency range of 250 kHz to 125 MHz.

q. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

E4. CHECK TRIGGER OUTPUT VOLTAGE

NOTE

If the preceding step was not performed, first perform step E1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the GND button (CH1 GND light on).

e. Set the CH1 trace 1 division above the center horizontal graticule line.

f. Press the GND button (CH1 GND light off).

g. Set the HF pulse generator High Level Output control to position the top of the pulse 0.8 division below the GND Reference level.

h. Set the HF pulse generator Low Level Output control to position the bottom of the pulse 1.7 divisions below the GND Reference level.

i. Press the CH4 button (button light on).

j. Press the 1MΩ/50Ω button (CH4 50Ω 1MΩ 15pf light off).

k. Press the DISPLAY button (CH4 DISPLAY light on).

l. Press the GND button (CH4 GND light on).

m. Position the CH4 display baseline (zero volts) 3 divisions below the center horizontal graticule line.

n. Press the GND button (CH4 GND light off).

o. **CHECK**—that the trigger output pulse amplitude level ranges from less than +0.2 V to greater than +0.8 V.

p. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

F. TRIGGER-EDGE SENSITIVITY

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
2. Time-Base Unit
3. Calibration Generator
5. HF Pulse Generator
13. Dual-Input Cable
14. Coaxial Cable
16. Precision Cable
20. Adapter, Female-to-Female
22. 10X Attenuator

F1. PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

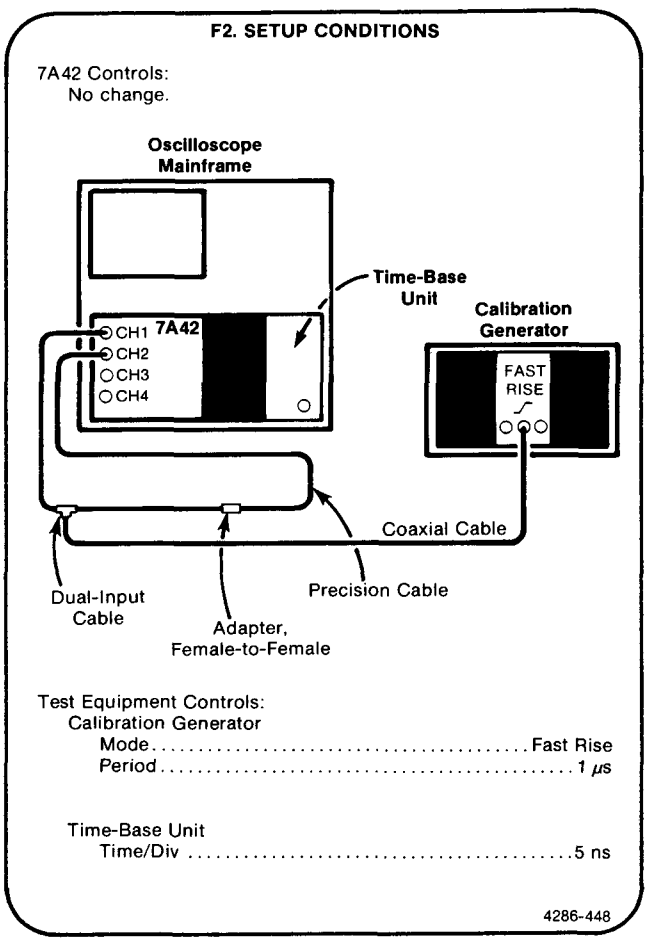
c. Set the time-base-unit controls:

Triggering
Mode ..... Auto
Coupling ..... Dc
Source ..... Int
Mag ..... In (X1)

F2. CHECK EDGE SETUP TIME (CHAN-TO-CHAN)

NOTE

First perform step F1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the TTL/ECL button (ECL TTL light off).

d. Press the CH2 button (button light on).

e. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

f. Press the TTL/ECL button (CH2 ECL TTL light off).

g. Press the DISPLAY button (CH2 DISPLAY light on).

h. Set the calibration generator Pulse Amplitude control to display a signal amplitude of 2 divisions on the two channels. The two signals should be triggered on the screen, with the CH2 signal delayed about 5 ns behind the CH1 signal.

i. Press the TRIG VIEW button (button light on).

j. Press the PROG TRIG button (button light on).

k. Press the CLEAR button.

l. Press the CH1 button, the AND button, the CH2 button, and the EDGE button, respectively.

m. **CHECK**—that the waveform display is triggered.

n. Press the CLEAR button.

o. Press the NOT button, the CH1 button, the AND button, the NOT button, the CH2 button, and the EDGE button, respectively.

p. **CHECK**—that the waveform display is triggered.

q. Reverse the signal connections on the CH1 and CH2 input connections.

r. Press the CLEAR button.

s. Press the CH1 button, the EDGE button, the AND button, and the CH2 button, respectively.

t. **CHECK**—that the waveform display is triggered.

u. Press the CLEAR button.

v. Press the NOT button, the CH1 button, the EDGE button, the AND button, the NOT button, and the CH2 button, respectively.

w. **CHECK**—that the waveform display is triggered.

NOTE

The "Channel-to-Channel Edge Setup Time" performance requirement applies for all combinations of channels in A and B trigger functions. To completely verify this specification would require performing the preceding checks 24 times. This specification was completely checked at the factory. Because of this, if you make performance checks on a routine basis we feel that completing the preceding checks "once" will give a high confidence level that all combinations will meet specifications, unless:

1. the trigger self-test (performed at power-up) fails, or

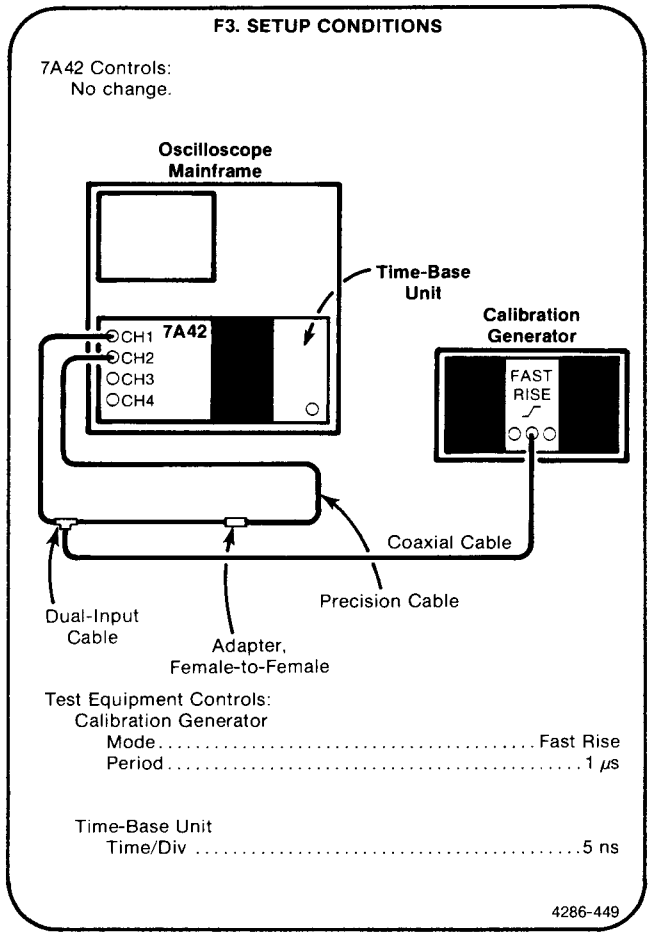
2. any ICs on the Trigger Board have been replaced. (Refer to the Maintenance section for a list of checks to perform when specific ICs have been replaced.)

x. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

F3. CHECK EDGE HOLD TIME (CHAN-TO-CHAN)

NOTE

If the preceding step was not performed, first perform step F1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the TTL/ECL button (ECL TTL light off).

d. Press the CH2 button (button light on).

e. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

f. Press the TTL/ECL button (CH2 ECL TTL light off).

g. Press the DISPLAY button (CH2 DISPLAY light on).

h. Set the calibration generator Pulse Amplitude control to display a signal amplitude of 2 divisions on the two channels. The two signals should be triggered on the screen, with the CH2 signal delayed about 5 ns behind the CH1 signal.

i. Press the TRIG VIEW button (button light on).

j. Press the PROG TRIG button (button light on).

k. Press the CLEAR button.

l. Press the CH1 button, the EDGE button, the AND button, the NOT button, and the CH2 button, respectively.

m. **CHECK**—that the waveform display is triggered.

n. Press the CLEAR button.

o. Press the NOT button, the CH1 button, the EDGE button, the AND button, and the CH2 button respectively.

p. **CHECK**—that the waveform display is triggered.

q. Reverse the signal connections on the CH1 and CH2 input connectors.

r. Press the CLEAR button.

s. Press the NOT button, the CH1 button, the AND button, the CH2 button, and the EDGE button, respectively.

t. **CHECK**—that the waveform display is triggered.

u. Press the CLEAR button.

v. Press the CH1 button, the AND button, the NOT button, the CH2 button, and the EDGE button, respectively.

w. **CHECK**—that the waveform display is triggered.

NOTE

The "Channel-to-Channel Edge Hold Time" performance requirement applies for all combinations of channels in A and B trigger functions. To completely verify this specification would require performing the preceding checks 24 times. This specification was completely checked at the factory. Because of this, if you make performance checks on a routine basis we feel that completing the preceding checks "once" will give a high confidence level that all combinations will meet specifications, unless:

1. the trigger self-test (performed at power-up) fails, or

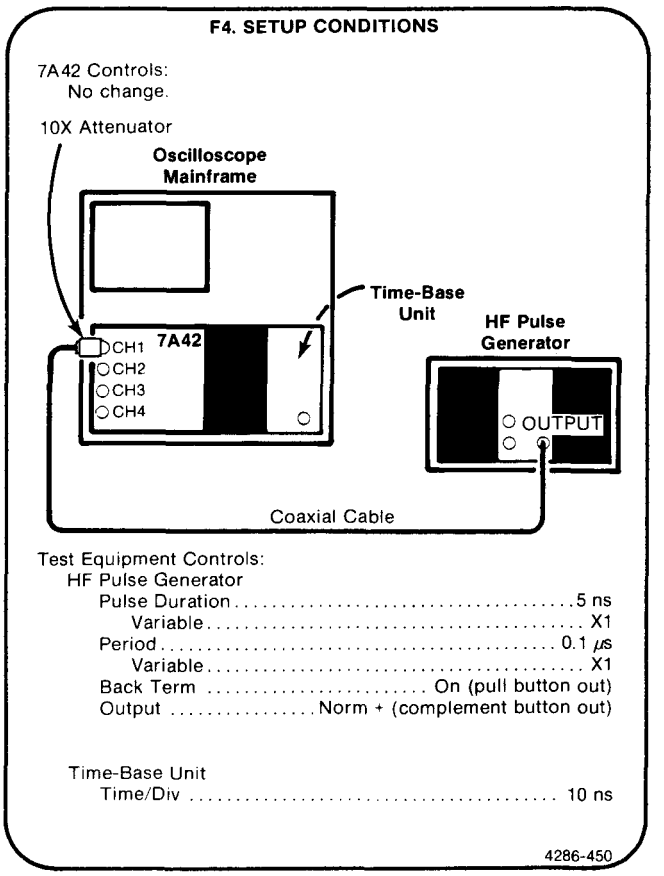
2. any ICs on the Trigger Board have been replaced. (Refer to the Maintenance section for a list of checks to perform when specific ICs have been replaced.)

x. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

F4. CHECK EDGE SETUP TIME (EDGE-SENS CHAN)

NOTE

If the preceding step was not performed, first perform step F1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the CH2 button (button light on).

e. Press the TTL/ECL button (CH2 ECL TTL light off).

f. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

g. Press the CH1 button (button light on).

h. Press the GND button (CH1 GND light on).

i. Set the CH1 trace 1 division above the center horizontal graticule line.

j. Press the GND button (CH1 GND light off).

k. Set the HF pulse generator High Level Output control to position the top of the pulse 0.8 division below the GND Reference level.

l. Set the HF pulse generator Low Level Output control to position the bottom of the pulse 1.7 divisions below the GND Reference level.

m. Set the time-base unit Triggering Level control as necessary for a stable display.

n. Set the HF pulse generator Variable Pulse Duration control for a displayed pulse width of 1 division (10 ns) measured at the 50% amplitude levels.

o. Press the PROG TRIG button (button light on).

p. Press the CLEAR button.

q. Press the TRIG VIEW button (button light on).

r. Press the NOT button, the EDGE button, and the CH1 button, respectively.

s. **CHECK**—that the pulse display remains triggered (falling edge of pulse aligned with the leading edge of the trigger view pulse).

t. Press the CLEAR button.

u. Press the NOT button, the CH2 button, the OR button, the NOT button, the EDGE button, and the CH1 button, respectively.

v. **CHECK**—that the pulse display remains triggered (falling edge of pulse aligned with the leading edge of the trigger view pulse).

w. Press the CLEAR button.

x. Press the B button (button light on).

y. Press the NOT button, the EDGE button, and the CH1 button, respectively.

z. **CHECK**—that the pulse display remains triggered (falling edge of pulse aligned with the leading edge of the trigger view pulse).

aa. Press the CLEAR button.

bb. Press the NOT button, the CH2 button, the OR button, the NOT button, the EDGE button, and the CH1 button, respectively.

cc. **CHECK**—that the pulse display remains triggered (falling edge of pulse aligned with the leading edge of the trigger view pulse).

dd. Press the CLEAR button.

ee. Press the HF pulse generator Complement (-) button in.

ff. Press the EDGE button, and the CH1 button.

gg. **CHECK**—that the inverted pulse remains triggered (rising edge of pulse aligned with the leading edge of the trigger view pulse).

hh. Press the CLEAR button.

ii. Press the NOT button, the CH2 button, the OR button, the EDGE button, and the CH1 button, respectively.

jj. **CHECK**—that the inverted pulse remains triggered (rising edge of pulse aligned with the leading edge of the trigger view pulse).

kk. Press the CLEAR button.

ll. Press the A button (button light on).

mm. Press the EDGE button, and the CH1 button.

nn. **CHECK**—that the inverted pulse remains triggered (rising edge of pulse aligned with the leading edge of the trigger view pulse).

oo. Press the CLEAR button.

pp. Press the NOT button, the CH2 button, the OR button, the EDGE button, and the CH1 button, respectively.

qq. **CHECK**—that the inverted pulse remains triggered (rising edge of pulse aligned with the leading edge of the trigger view pulse).

rr. Press the CLEAR button.

ss. Release the HF pulse generator Complement button (button out).

NOTE

The "Edge-Sensitive Channel Edge Setup Time" performance requirement applies for all combinations of channels in A and B trigger functions. To completely verify this specification would require performing the preceding checks 4 times. This specification was completely checked at the factory. Because of this, if you make performance checks on a routine basis we feel that completing the preceding checks "once" will give a high confidence level that all combinations will meet specifications, unless:

1. the trigger self-test (performed at power-up) fails, or

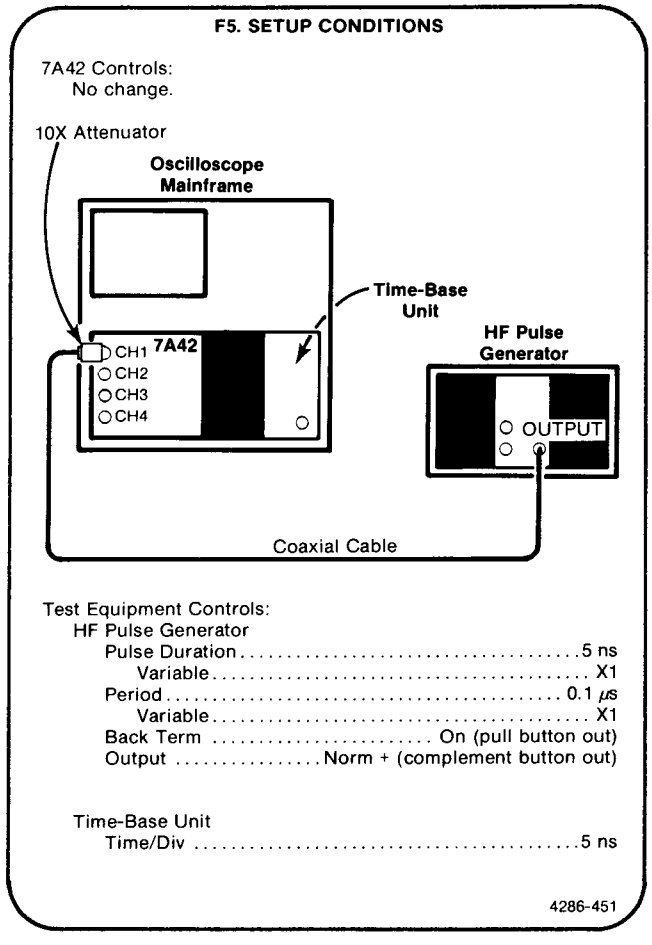
2. any ICs on the Trigger Board have been replaced. (Refer to the Maintenance section for a list of checks to perform when specific ICs have been replaced.)

tt. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

F5. CHECK EDGE HOLD TIME (EDGE-SENS CHAN)

NOTE

If the preceding step was not performed, first perform step F1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the CH2 button (button light on).

e. Press the TTL/ECL button (CH2 ECL TTL light off).

f. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

g. Press the CH1 button (button light on).

h. Press the GND button (CH1 GND light on).

i. Set the CH1 trace 1 division above the center horizontal graticule line.

j. Press the GND button (CH1 GND light off).

k. Set the HF pulse generator High Level Output control to position the top of the pulse 0.8 division below the GND Reference level.

l. Set the HF pulse generator Low Level Output control to position the bottom of the pulse 1.7 divisions below the GND Reference level.

m. Set the time-base unit Triggering Level control as necessary for a stable display.

n. Set the HF pulse generator Variable Pulse Duration control for a displayed pulse width of 1 division (5 ns) measured at the 50% amplitude levels.

o. Press the PROG TRIG button (button light on).

p. Press the CLEAR button.

q. Press the TRIG VIEW button (button light on).

r. Press the EDGE button, and the CH1 button.

s. **CHECK**—that the pulse display remains triggered (rising edge of pulse aligned with the leading edge of the trigger view pulse).

t. Press the CLEAR button.

u. Press the NOT button, the CH2 button, the OR button, the EDGE button, and the CH1 button, respectively.

v. **CHECK**—that the pulse display remains triggered (rising edge of pulse aligned with the leading edge of the trigger view pulse).

w. Press the CLEAR button.

x. Press the B button (button light on).

y. Press the EDGE button, and the CH1 button.

z. **CHECK**—that the pulse display remains triggered (rising edge of pulse aligned with the leading edge of the trigger view pulse).

aa. Press the CLEAR button.

bb. Press the NOT button, the CH2 button, the OR button, the EDGE button, and the CH1 button, respectively.

cc. **CHECK**—that the pulse display remains triggered (rising edge of pulse aligned with the leading edge of the trigger view pulse).

dd. Press the CLEAR button.

ee. Press the HF pulse generator Complement (-) button in.

ff. Press the NOT button, the EDGE button, and the CH1 button, respectively.

gg. **CHECK**—that the inverted pulse remains triggered (falling edge of pulse aligned with the leading edge of the trigger view pulse).

hh. Press the CLEAR button.

ii. Press the NOT button, the CH2 button, the OR button, the NOT button, the EDGE button, and the CH1 button, respectively.

jj. **CHECK**—that the inverted pulse remains triggered (falling edge of pulse aligned with the leading edge of the trigger view pulse).

kk. Press the CLEAR button.

ll. Press the A button (button light on).

mm. Press the NOT button, the EDGE button, and the CH1 button, respectively.

nn. **CHECK**—that the inverted pulse remains triggered (falling edge of pulse aligned with the leading edge of the trigger view pulse).

oo. Press the CLEAR button.

pp. Press the NOT button, the CH2 button, the OR button, the NOT button, the EDGE button, and the CH1 button, respectively.

qq. **CHECK**—that the inverted pulse remains triggered (falling edge of pulse aligned with the leading edge of the trigger view pulse).

NOTE

The "Edge-Sensitive Channel Edge Hold Time" performance requirement applies for all combinations of channels in A and B trigger functions. To completely verify this specification would require performing the preceding checks 4 times. This specification was completely checked at the factory. Because of this, if you make performance checks on a routine basis we feel that completing the preceding checks "once" will give a high confidence level that all combinations will meet specifications, unless:

1. the trigger self-test (performed at power-up) fails, or

2. any ICs on the Trigger Board have been replaced. (Refer to the Maintenance section for a list of checks to perform when specific ICs have been replaced.)

rr. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

G. TRIGGER-A THEN B

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
2. Time-Base Unit
3. Calibration Generator
5. HF Pulse Generator
13. Dual-Input Cable
14. Coaxial Cable (Two Required)
16. Precision Cable
20. Adapter, Female-To-Female
22. 10X Attenuator

G1. PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modification which may affect this procedure.

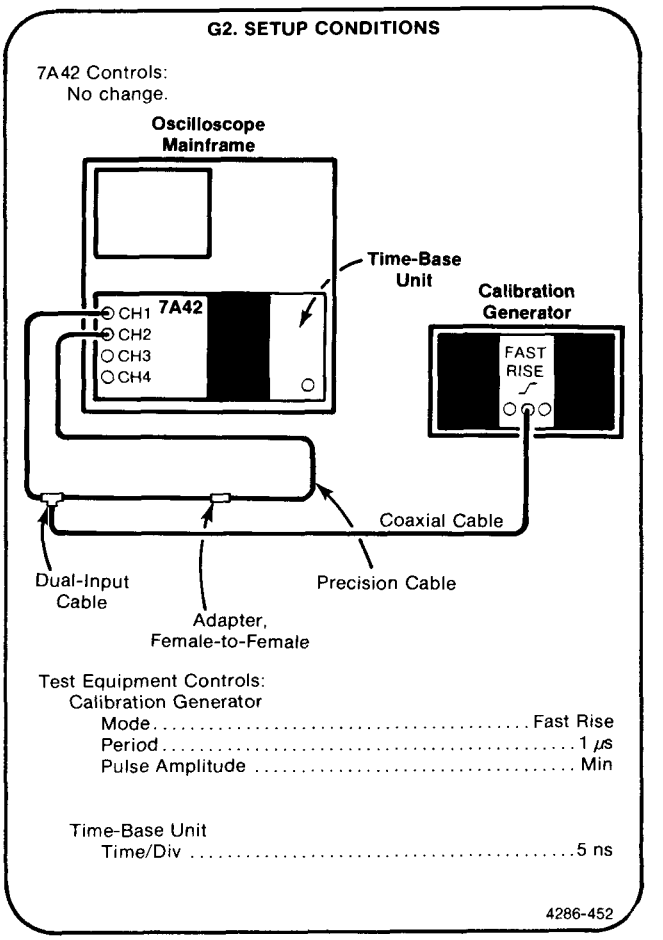
c. Set the time-base unit controls:

Triggering
Mode ..... Auto
Coupling ..... Dc
Source ..... Int
Mag ..... In (X1)

G2. CHECK TIME BETWEEN EVENT A AND EVENT B

NOTE

First perform step G1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the CH2 button (button light on).

e. Press the TTL/ECL button (CH2 ECL TTL light off).

f. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

g. Press the DISPLAY button (CH2 DISPLAY light on).

h. Set the calibration generator Pulse Amplitude control to display a signal amplitude of 2 divisions on the CH1 and CH2 traces. The two signal displays should be triggered on the screen, with the CH2 transition delayed about 5 ns behind the CH1 transition.

i. Press the PROG TRIG button (button light on).

j. Press the CLEAR button.

k. Press the CH1 button, and the EDGE button.

l. Press the B button.

m. Press the CH2 button, and the EDGE button.

n. Press the A THEN B button (button light on).

o. Press the TRIG VIEW button (button light on).

p. **CHECK**—that the waveform display is triggered on the screen, and that the rising edge of the CH2 transition is aligned with the leading edge of the trigger view pulse.

q. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

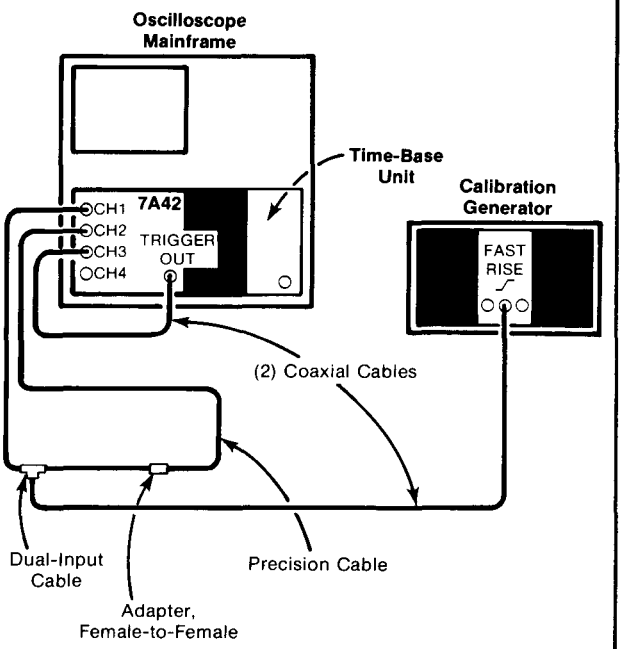
G3. CHECK TIME FROM EVENT B TO EVENT A

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G3. SETUP CONDITIONS

7A42 Controls:
First, remove the 7A42 from the oscilloscope mainframe. Then move the J701 (link-plug) jumper to the "A Then B Gate To Front Panel" position, as shown in Figure 4-14 and replace the 7A42 in the oscilloscope mainframe.



Test Equipment Controls:
Calibration Generator
Mode ..... Fast Rise
Period ..... 1 μs
Pulse Amplitude ..... Min

Time-Base Unit
Time/Div ..... 10 ns

4286-453

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the CH2 button (button light on).

e. Press the DISPLAY button (CH2 DISPLAY light on).

f. Press the TTL/ECL button (CH2 ECL TTL light off).

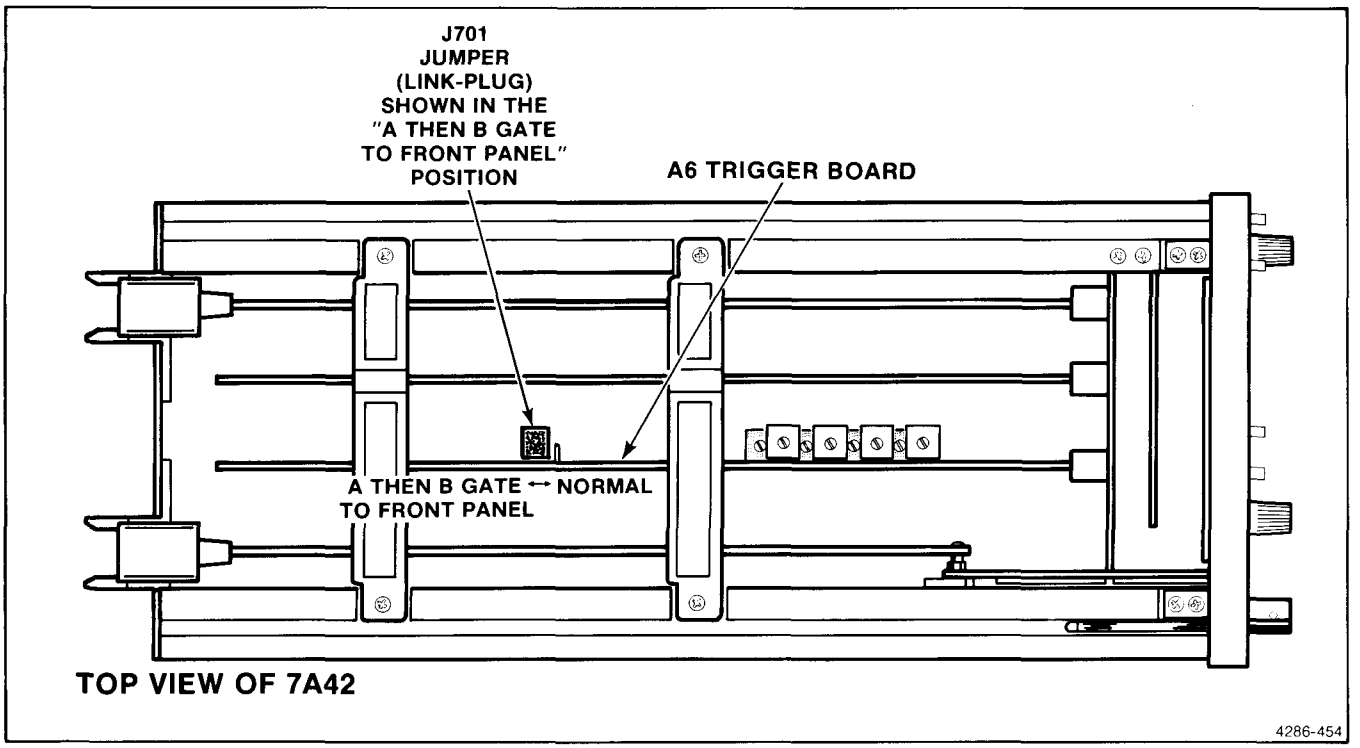


Figure 4-14. Location of J701 (Link-Plug) on the A6 Trigger Board.

g. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

h. Press the CH3 button (button light on).

i. Press the DISPLAY button (CH3 DISPLAY light on).

j. Press the 1MΩ/50Ω button (CH3 50Ω 1MΩ 15pf light off).

k. Set the calibration generator Pulse Amplitude control to display a signal amplitude of 2 divisions on the CH1 and CH2 traces. The two signal displays should be triggered on the screen, with the CH2 transition delayed about 5 ns behind the CH1 transition. The CH3 trace should display the trigger output signal, about 2 divisions in amplitude and somewhat delayed behind the other two signals.

l. Press the PROG TRIG button (button light on).

m. Press the CLEAR button.

n. Press the CH2 button, and the EDGE button.

o. Press the B button (button light on).

p. Press the NOT button, and the CH1 button.

q. Press the A THEN B button (button light on).

r. Set the time-base unit Time/Div to 10 ns.

s. **CHECK**—that the waveforms are triggered on the screen, and that the falling edge of the CH1 transition is followed by both the falling edge of the CH2 transition and the falling edge of the CH3 trigger output transition. (The ring at the falling CH3 transition is normal.)

t. Set the oscilloscope mainframe B Trigger Source to Right Vert.

u. Note the relative timing between the CH3 transition and either the CH1 or CH2 transition.

v. Repeatedly press the EDGE button.

w. **CHECK**—that the relative timing between the CH3 transition and either the CH1 or CH2 transition does not change more than 0.2 division.

x. **CHECK**—for little or no change in the general shape of the CH3 transition.

y. Set the oscilloscope mainframe B Trigger Source to Vert Mode.

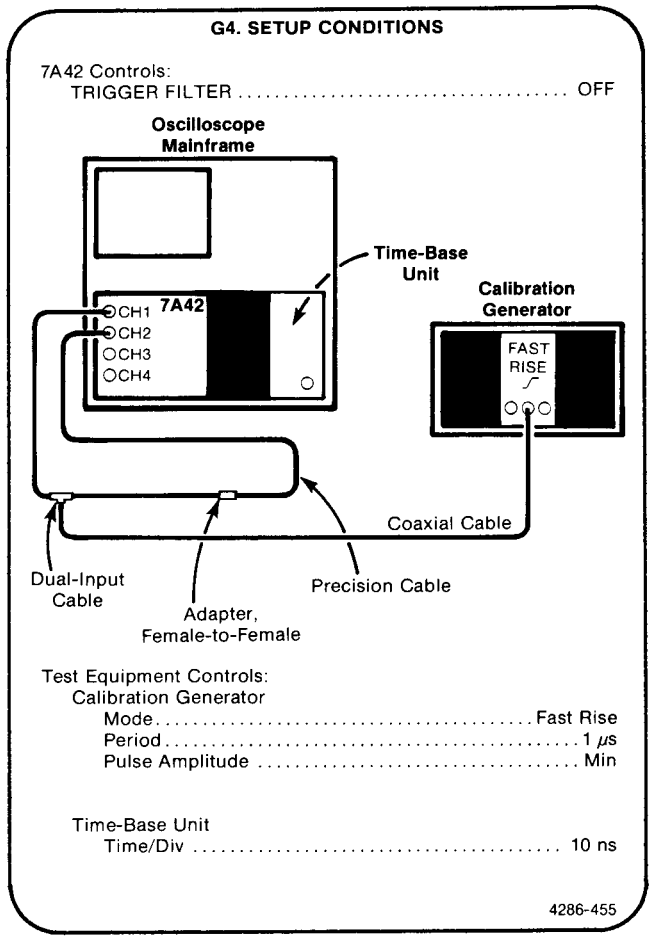
z. Move the J701 link-plug back to the Normal position (refer to Fig. 4-14).

aa. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

G4. CHECK MINIMUM EVENT DURATION

NOTE

If the preceding step was not performed, first perform step G1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the CH2 button (button light on).

e. Press the DISPLAY button (CH2 DISPLAY light on).

f. Press the TTL/ECL button (CH2 ECL TTL light off).

g. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

h. Set the calibration generator Pulse Amplitude control to display a signal amplitude of 2 divisions on the CH1 and CH2 traces.

i. Press the PROG TRIG button (button light on).

j. Press the CLEAR button.

k. Press the CH1 button, the AND button, the NOT button, and the CH2 button, respectively.

l. Press the B button.

m. Press the NOT button, and the CH1 button.

n. Press the A THEN B button (button light on).

o. Press the TRIG VIEW button (button light on).

p. **CHECK**—that the waveform display is triggered on the screen.

q. Press the A button (button light on).

r. Press the A THEN B button (button light off).

s. Press the CLEAR button.

t. Press the NOT button, and the CH1 button.

u. Press the B button (button light on).

v. Press the CLEAR button.

w. Press the CH1 button, the AND button, the NOT button, and the CH2 button, respectively.

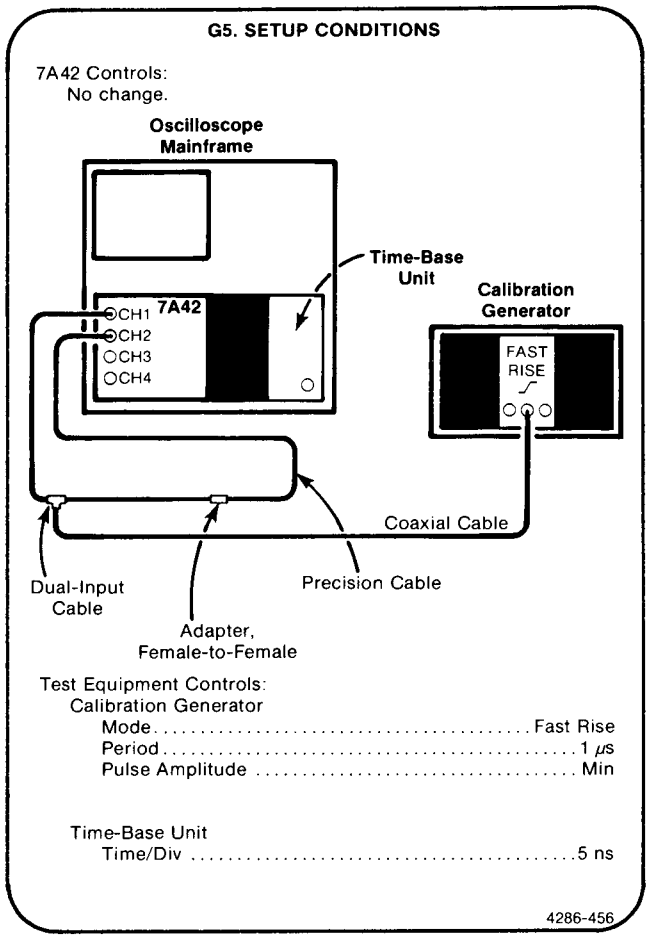
x. **CHECK**—that the waveform display is triggered on the screen.

y. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

G5. CHECK A THEN B GATE OUTPUT WIDTH

NOTE

If the preceding step was not performed, first perform step G1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the CH2 button (button light on).

e. Press the TTL/ECL button (CH2 ECL TTL light off).

f. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

g. Press the DISPLAY button (CH2 DISPLAY light on).

h. Set the calibration generator Pulse Amplitude control to display a signal amplitude of 2 divisions on the CH1 and CH2 traces. The two signal displays should be triggered on the screen, with the CH2 transition delayed about 5 ns behind the CH1 transition.

i. Press the PROG TRIG button (button light on).

j. Press the B button (button light on).

k. Press the CH2 button (red CH2 TRIGGER FUNCTION light on).

l. Press the A THEN B button (button light on).

m. Connect a coaxial cable from the oscilloscope mainframe Sig Out connector to the CH4 input connector.

n. Press the PROG CHAN button.

o. Press the CH4 button.

p. Press the DISPLAY button.

q. Press the 1MΩ/50Ω button.

r. Press the TTL/ECL button.

s. Set the oscilloscope mainframe B Trigger Source to Right Vert.

t. **CHECK**—that the width of the A THEN B gate pulse, displayed in CH4, is 1 division, within 0.2 division, measured at the 50% amplitude levels.

u. Set the oscilloscope mainframe B Trigger Source back to Vert Mode.

v. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

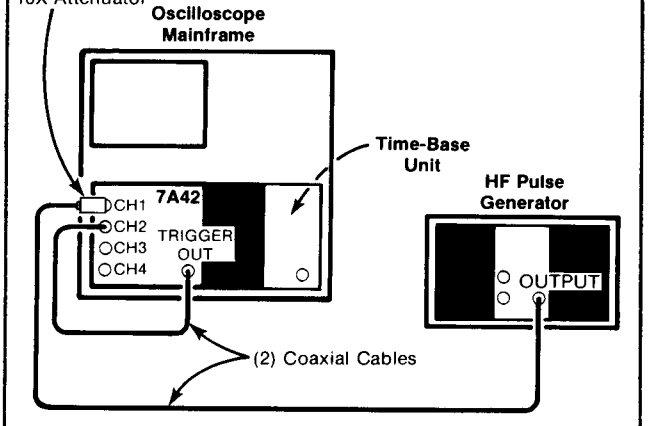
G6. CHECK GATE OUTPUT TIMING

NOTE

If the preceding step was not performed, first perform step G1, then proceed.

G6. SETUP CONDITIONS

7A42 Controls:
First, remove the 7A42 from the oscilloscope mainframe. Then move the J701 (link-plug) jumper to the "A Then B Gate To Front Panel" position, as shown in Figure 4-14 and replace the 7A42 in the oscilloscope mainframe.



Test Equipment Controls:

HF Pulse Generator
- Pulse Duration ..... Sq Wave (Int Period)
- Variable X1
- Period ..... 0.1 μs
- Variable X1
- Back Term ..... On (pull button out)
- Output ..... Norm + (complement button out)

Time-Base Unit
- Time/Div ..... 10 ns

4286-457

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the GND button (CH1 GND light on).

e. Set the CH1 trace 1 division above the center horizontal graticule line.

f. Press the GND button (CH1 GND light off).

g. Set the HF pulse generator High Level Output control to position the top of the square wave 0.8 divisions below the GND Reference level.

h. Set the HF pulse generator Low Level Output control to position the bottom of the square wave 1.7 divisions below the GND reference level.

i. Press the upper VOLTS/DIV button to display 20 mV in the crt readout display.

j. Press the CH2 button (button light on).

k. Press the DISPLAY button (CH2 DISPLAY light on).

l. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

m. Press the PROG TRIG button (button light on).

n. Press the B button.

o. Press the NOT button, and the CH1 button.

p. Press the A THEN B button (button light on).

q. Set the CH1 and CH2 POSITION controls to vertically center the two waveforms on the graticule.

r. **CHECK**—for less than 3 divisions between the rising edge of the CH1 signal and the rising edge of the CH2 signal.

s. Move the J701 link-plug back to the Normal position (refer to Fig. 4-14).

t. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

H. TRIGGER-RESET

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment).

1. Oscilloscope Mainframe
2. Time-Base Unit
5. HF Pulse Generator
6. Function Generator
9. LF Pulse Generator
11. Dual-Input Cable
14. Coaxial Cable (Three Required)
15. Adapter Cable
19. Adapter, BNC-T
20. Adapter, Female-To-Female (Two Required)
22. 10X Attenuator (Two Required)
23. 50Ω Feedthrough Terminator

H1. PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modification which may affect this procedure.

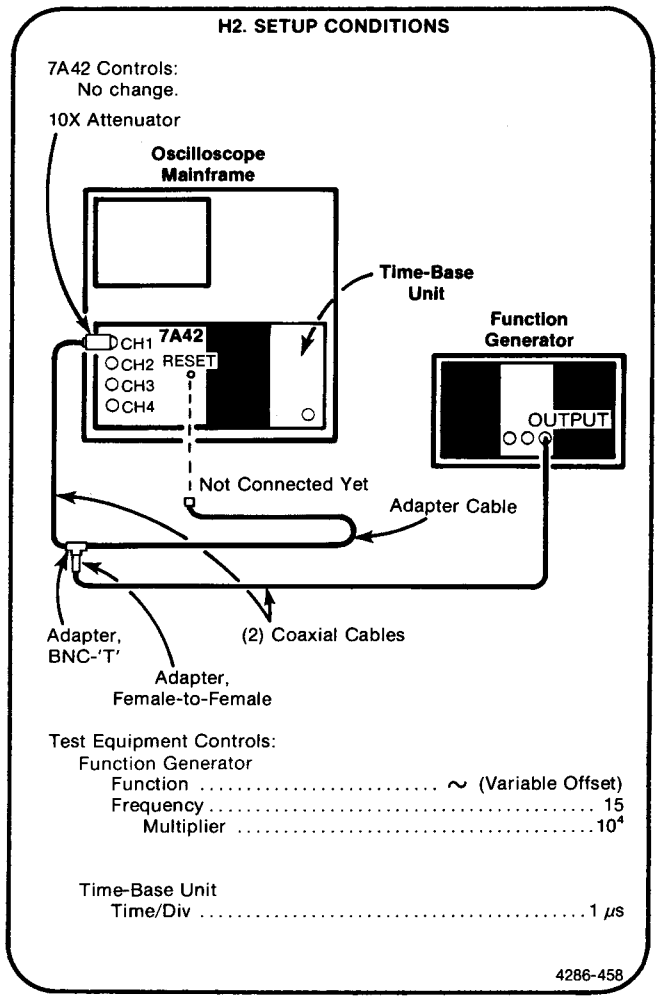
c. Set the time-base unit controls:

Triggering
Mode ..... Auto
Coupling ..... Dc
Source ..... Int
Mag ..... In (X1)

H2. CHECK RESET INPUT THRESHOLDS

NOTE

First perform step H1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

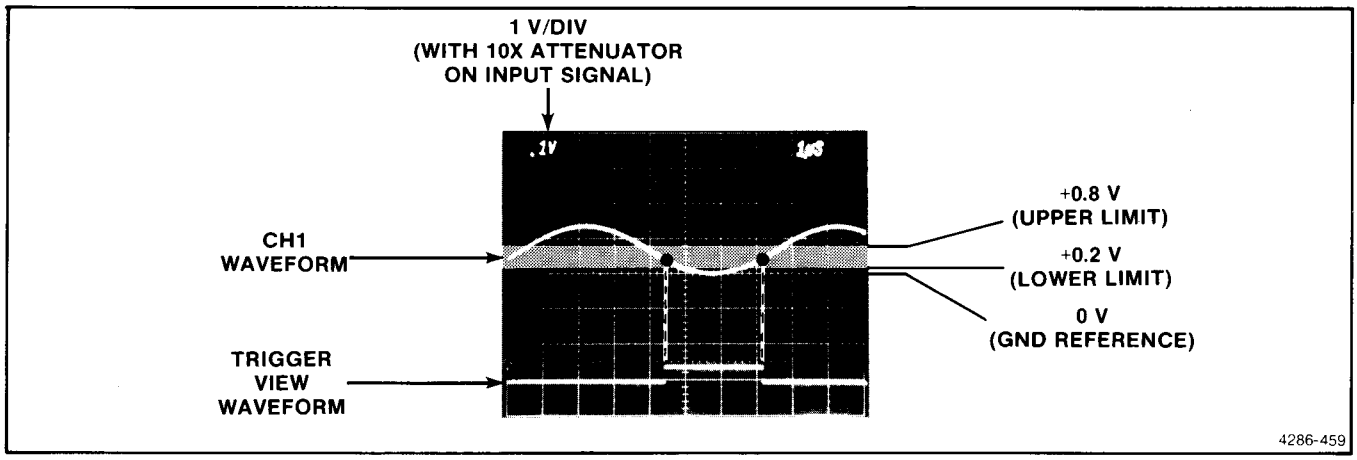


Figure 4-15. Trigger view transitions referenced to the CH1 waveform voltage levels.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the upper VOLTS/DIV button for a crt readout display of 0.1 V.

d. Press the GND button (CH1 GND light on).

e. Position the CH1 trace to the center horizontal graticule line.

f. Press the GND button (CH1 GND light off).

g. Set the function generator Amplitude and Offset controls to position the bottom of the sine wave to center horizontal graticule line (GND reference) and the top of the sine wave 2 divisions above the horizontal graticule line.

h. Press the PROG TRIG button (button light on).

i. Press the B button (button light on).

j. Press the CH2 button, the OR button, the NOT button, and the CH2 button, respectively.

k. Press the TRIG VIEW button (button light on).

l. Connect the open end of the Adapter Cable to the RESET connector.

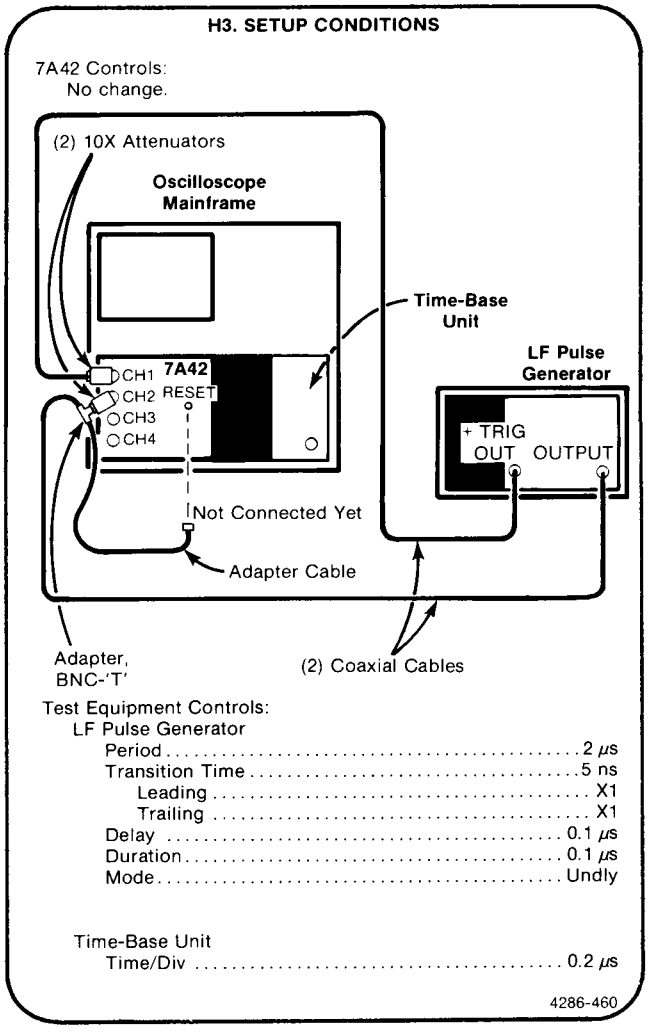
m. **CHECK**—that the rising and falling transitions of the trigger view waveform occur when the CH1 waveform amplitude level is within the limits of the +0.2 V to +0.8 V window. Refer to Figure 4-15.

n. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

H3. CHECK RESET INPUT PULSE WIDTH

NOTE

If the preceding step was not performed, first perform step H1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

c. Press the TTL/ECL button (CH1 ECL TTL light off).

d. Press the CH2 button (button light on).

e. Press the 1MΩ/50Ω button (CH2 50Ω 1MΩ 15pf light off).

f. Press the TTL/ECL button (CH2 ECL TTL light off).

g. Press the DISPLAY button (button light on)

h. Press the GND button (CH2 GND light on).

i. Position the CH2 trace 2 divisions below the center horizontal graticule line.

j. Press the GND button (CH2 GND light off).

k. Set the LF pulse generator Low Level Output control to position the baseline of the CH2 pulse 2 divisions below the center horizontal graticule line (GND reference).

l. Set the LF pulse generator High Level Output control to position the top of the pulse 0.5 division below the center horizontal graticule line (1.5 V pulse).

m. Press the TRIG VIEW button (button light on).

n. Press the CH1 button (button light on).

o. Press the THRESH button (button light on).

p. Press the LEVEL button to display +.050 on the SWITCHING THRESHOLD readout.

q. Press the oscilloscope mainframe B Trigger Source Left Vert button.

r. Connect the adapter cable to the RESET connector.

s. Set the time-base Hold Off control as necessary for a stable display.

t. **CHECK**—that the display is triggered, and appears the same as illustrated in Figure 4-16.

u. Press the PROG TRIG button (button light on).

v. Press the CLEAR button.

w. Press the CH1 button, and the EDGE button.

x. Press the B button (button light on).

y. Press the NOT button, and the CH4 button.

z. Press the PROG CHAN button (button light off).

aa. Press the CH3 button (button light on).

bb. Press the DISPLAY button.

cc. Press the TTL/ECL button (CH3 ECL TTL light off).

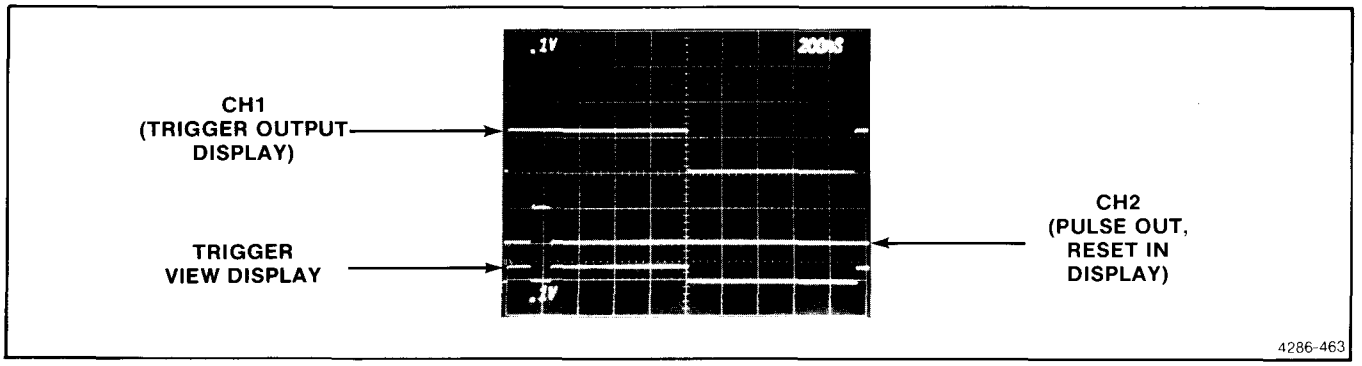


Figure 4-16. Relationship between the CH1, CH2, and Trigger View waveforms when checking the reset input pulse width.

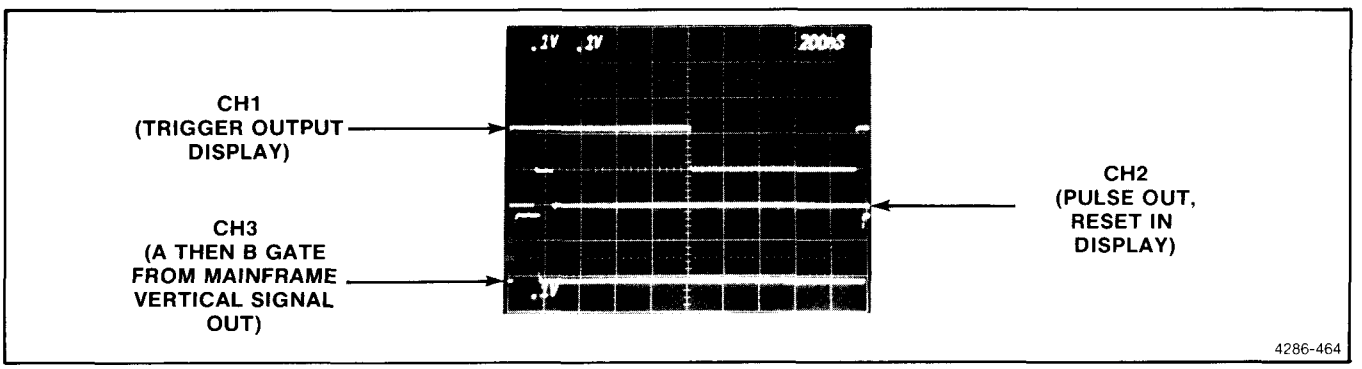


Figure 4-17. Relationship between the CH1, CH2, and CH3 waveforms when checking the Reset Input Pulse Width.

dd. Press the 1MΩ/50Ω button (CH3 50Ω 1MΩ 15pf light off).

ee. Press the CH4 button (button light on).

ff. Press the TTL/ECL button (CH4 ECL TTL light off).

gg. Press the LEVEL buttons for a readout of -.130 volt on the SWITCHING THRESHOLD readout display.

hh. Press the TRIG VIEW button (button light off).

ii. Press the A THEN B button (button light on).

jj. Press the oscilloscope mainframe B Triggering Source Right Vert button.

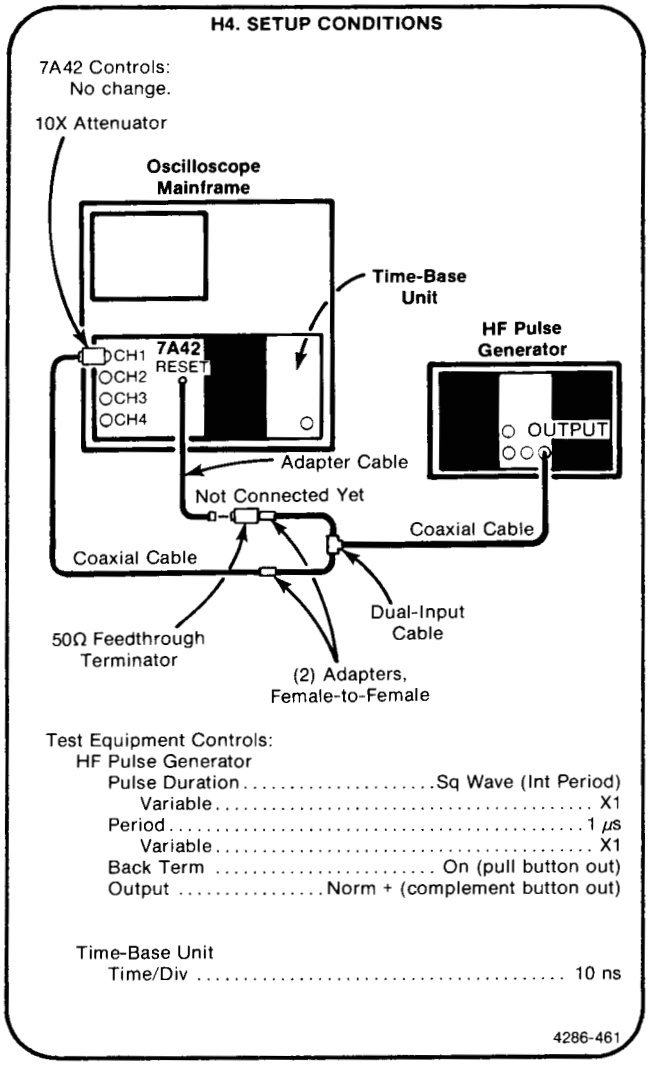
kk. **CHECK**—that the display is triggered, and appears the same as illustrated in Figure 4-17.

ll. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

H4. CHECK POST-RESET INHIBIT TIME

NOTE

If the preceding step was not performed, first perform step H1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the GND button (CH1 GND light on).

e. Set the CH1 trace to the center horizontal graticule line.

f. Press the GND button (CH1 GND light off).

g. Set the HF pulse generator High Level Output control to position the top of the square wave 1.5 divisions above the center horizontal graticule line.

h. Set the HF pulse generator Low Level Output control to position the bottom of the square wave to the center horizontal graticule line.

i. Press the PROG TRIG button (button light on).

j. Press the CLEAR button.

k. Press the NOT button, and the CH1 button.

l. Press the B button (button light on).

m. Press the CH2 button, the OR button, the NOT button, and the CH2 button, respectively.

n. Press the A button (button light on).

o. Press the PROG CHAN button (button light off).

p. Press the THRESH button (button light on).

q. Press the LEVEL buttons for a readout of +.050 volts on the SWITCHING THRESHOLD readout display.

r. Set the time-base Position control to align the falling edge of the square wave with a vertical graticule line, and note its position.

s. Remove the 50Ω feedthrough termination and connect the adapter cable (from the RESET connector) in its place.

t. Press the B button (button light on).

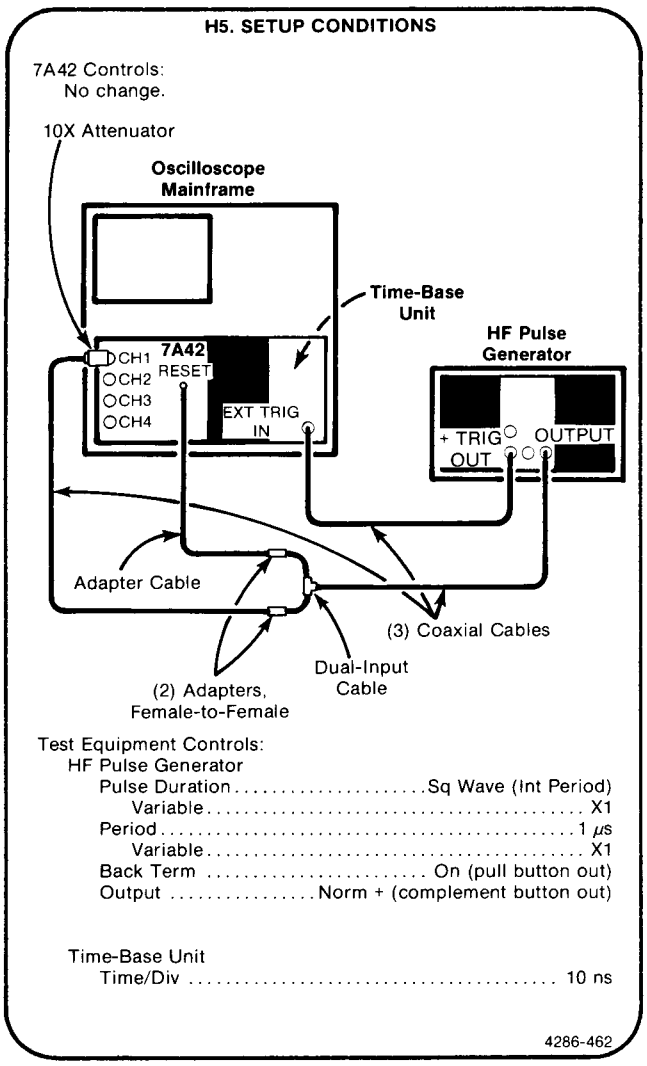
u. **CHECK**—that the falling edge of the square wave has shifted to the left not more than 1 division (10 ns), from the point noted in part r.

v. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

H5. CHECK RESET ACTIVATION WINDOW

NOTE

If the preceding step was not performed, first perform step H1, then proceed.



a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe Power off, then back on again.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the 1MΩ/50Ω button (CH1 50Ω 1MΩ 15pf light off).

d. Press the GND button (CH1 GND light on).

e. Set the CH1 trace to the center horizontal graticule line.

f. Press the GND button (CH1 GND light off).

g. Set the HF pulse generator High Level Output control to position the top of the square wave 1.5 divisions above the center horizontal graticule line.

h. Set the HF pulse generator Low Level Output control to position the bottom of the square wave to the center horizontal graticule line.

i. Press the THRESH button (button light on).

j. Press the LEVEL buttons for a readout of +.050 volts on the SWITCHING THRESHOLD readout display.

k. Press the TRIG VIEW button (button light on).

l. **CHECK**—that the square-wave signal is not triggered on the screen.

m. Press the time-base unit Ext Triggering Source button. Note that the rising edge of the square wave signal is triggered on the screen, but there is no signal on the trigger view trace.

n. Press the time-base unit Int Triggering Source button.

o. Remove the coaxial cable and female-to-female adapter that connects the CH1 10X attenuator to the dual-input cable. Connect that leg of the dual-input cable directly to the CH1 10X attenuator.

p. Connect the coaxial cable and female-to-female adapter just removed, between the other leg of the dual-input connector and the adapter cable going to the RESET connector.

q. **CHECK**—that the CH1 square wave rising edge and the trigger view pulse rising edge are both triggered on the screen, and that both occur at approximately the same time.

r. Replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

This completes the Part II—Performance Check Procedure.

PART III—ADJUSTMENT PROCEDURE

The Part III—Adjustment Procedure contains the information necessary to perform all internal adjustments. This procedure provides a logical sequence of adjustment steps, and is intended to return the instrument to specified operation following repair, or as a part of a routine maintenance program.

Most adjustment steps can be performed independently, except when it is specifically noted that the adjustment sequence is important, or interaction is involved. In all cases, perform the appropriate steps in the Performance Check Procedure or Functional Check Procedure following any repair or adjustment activity.

NOTE

Limits, tolerances, and waveform information in this section are not guaranteed specifications except when they agree with the Performance Requirements in the Specification tables.

INDEX TO PART III—ADJUSTMENT PROCEDURE

ADJUSTMENT INITIAL SETUP PROCEDURE

NOTE

The following Adjustment procedure must be performed within the ambient temperature range of +20° and +30° C, to assure proper instrument adjustment.

CAUTION

To avoid instrument damage, we recommend that the oscilloscope mainframe Power switch be turned off before removing or replacing the 7A42.

1. Remove the 7A42 side covers.
2. Remove the oscilloscope mainframe left side cover.
3. Connect the 7A42 to the appropriate oscilloscope mainframe Left and Right Vertical compartments using the two flexible plug-in extenders.
4. Install the time-base unit in the B Horizontal compartment of the oscilloscope mainframe.
5. Remove the internal J747 BE (Battery Enable) link-plug to disable the battery backup feature. Refer to Figure 4-18. The removal of J747 permits the front-panel settings to be initialized to a known condition each time the oscilloscope mainframe power is turned off, then on. For this reason the "power off, then on" routine is used frequently throughout the following procedures.
6. Connect the oscilloscope mainframe to a suitable power source, and turn power on. Allow at least 20 minutes warmup before beginning the procedure.

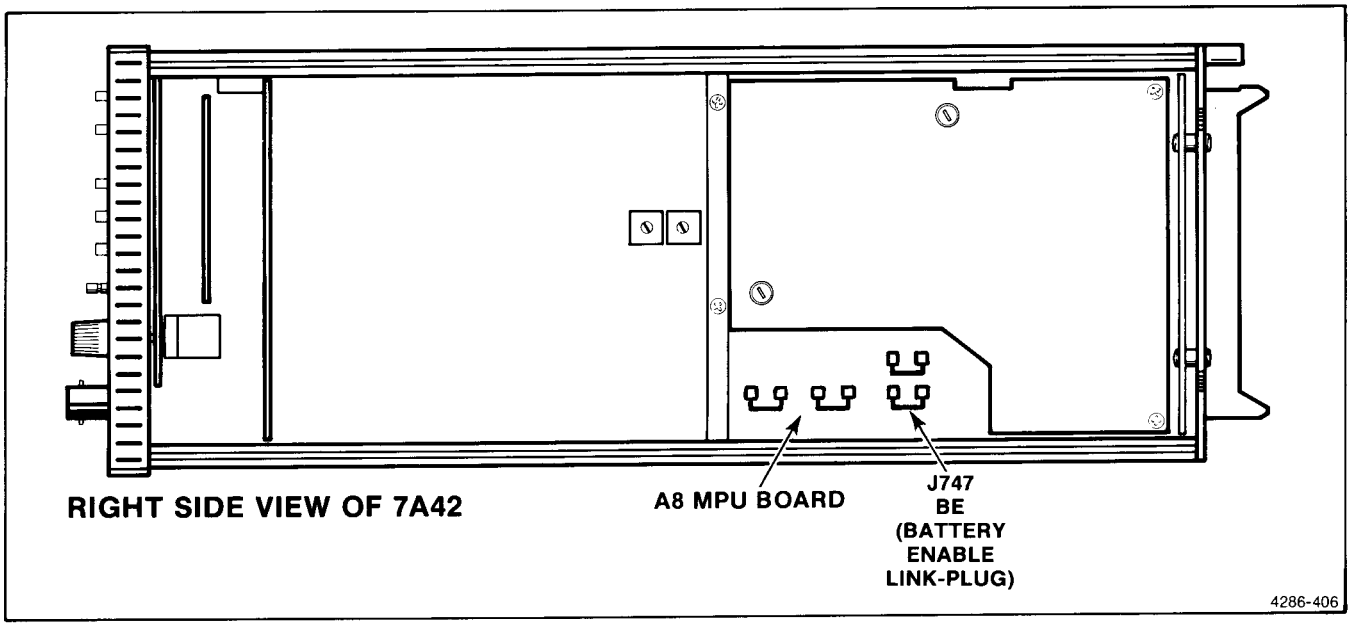


Figure 4-18. Location of the J747 BE (Battery Enable) link plug.

A. POWER SUPPLY

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment):

1. Oscilloscope Mainframe
4. Digital Multimeter
11. Flexible Plug-In Extender (Two required)
18. Meter Leads
24. Alignment Tool

A1. PRELIMINARY SETUP

a. Perform the Adjustment Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

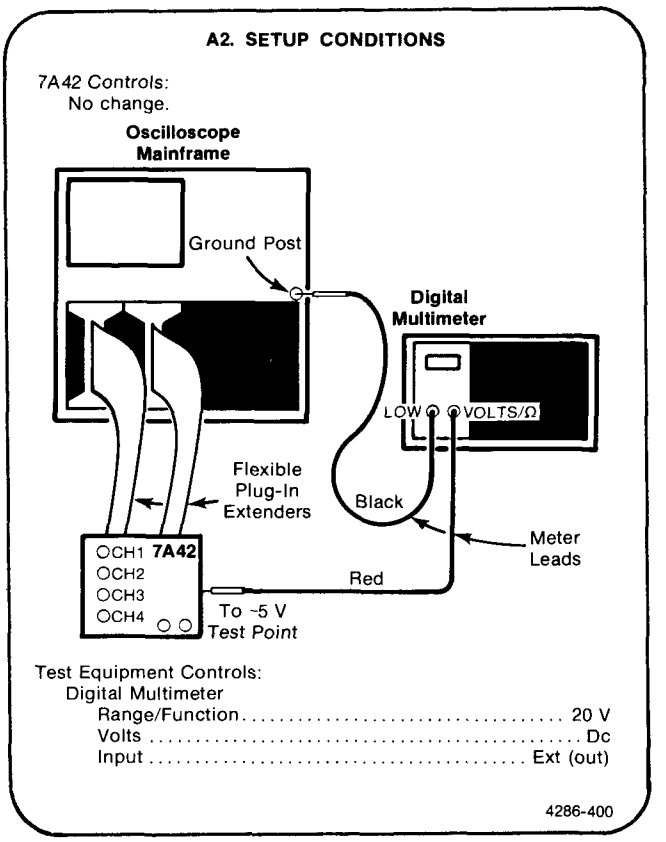
c. Set the oscilloscope mainframe controls:

Power ..... On
Intensity ..... Fully counterclockwise

A2. ADJUST POWER SUPPLY (R228)

NOTE

First perform step A1, then proceed.



a. **EXAMINE**—the digital multimeter readout for a reading of -5.10 V, within the limits of -5.05 to -5.15 V.

b. **ADJUST**—the -5 V Adj, R228, for a reading of -5.10 V.

c. Remove the meter leads.

d. Rotate the R400 I Limit adjustment fully counterclockwise.

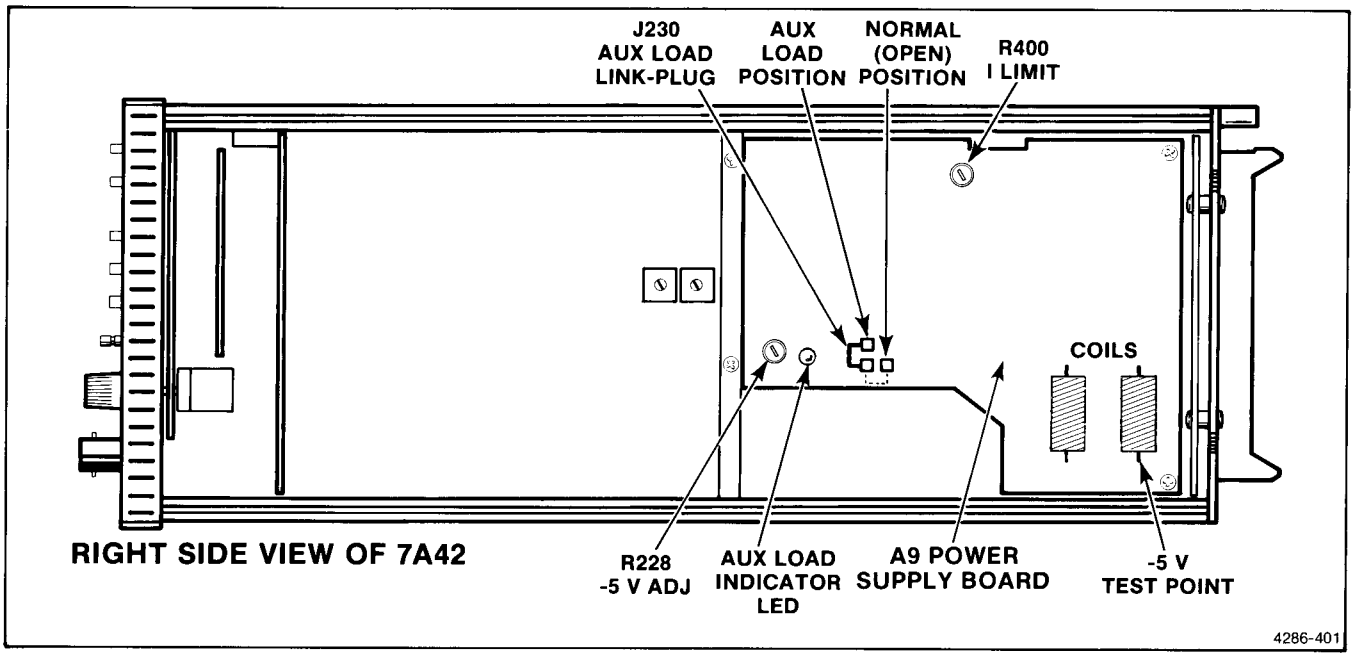
e. Move the J230 Aux Load link-plug from the Normal (Open) position to the Aux Load position. Note the Aux Load Indicator LED turns on.

f. **ADJUST**—the I Limit adjustment, R400, clockwise until the red LED flashes. Rotate the control counterclockwise just until the LED stops flashing, and remains on.

g. Move the J230 Aux Load link-plug back to the Normal (open) position. Note the Aux Load Indicator turns off.

h. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

A2. TEST POINT & ADJUSTMENT LOCATIONS



B. ATTENUATOR OFFSET

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment):

1. Oscilloscope Mainframe
2. Time-Base Unit
11. Flexible Plug-In Extender (Two required)
24. Alignment Tool

B1. PRELIMINARY SETUP

a. Perform the Adjustment Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

c. Set the oscilloscope mainframe and time base controls:

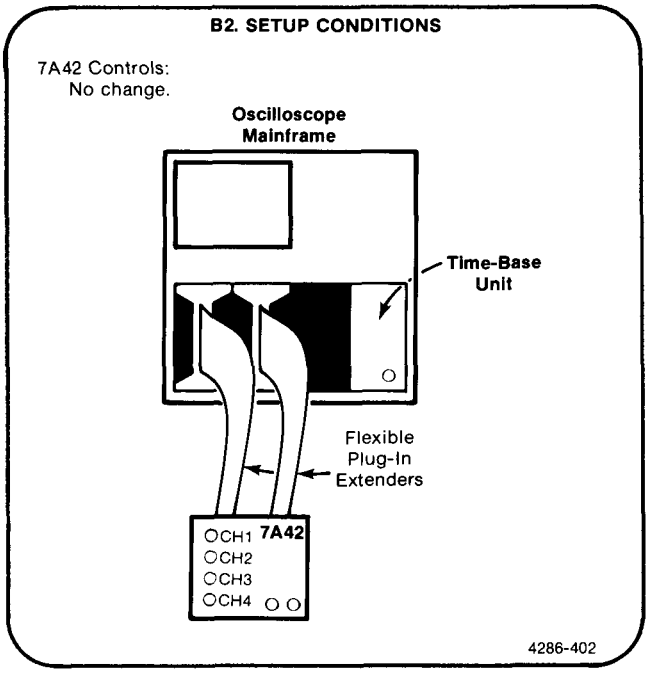
MAINFRAME
- Power ..... On
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Source ..... Left Vert
- B Intensity ..... Visible display
- Focus ..... Well defined display

TIME BASE
- Triggering
  - Mode ..... Auto
  - Coupling ..... Dc
  - Source ..... Int

B2. ADJUST ATTENUATOR OFFSET (R320, R321, R322, R323)

NOTE

First perform step B1, then proceed.



a. Turn oscilloscope mainframe power off.

b. Remove the link-plug from J410.

c. Turn the power on.

d. Press B (relays will continuously cycle).

e. **ADJUST**—Atten Offset, R320, R321, R322, and R323, for no vertical shift of the CH1, CH2, CH3 and CH4 traces, respectively.

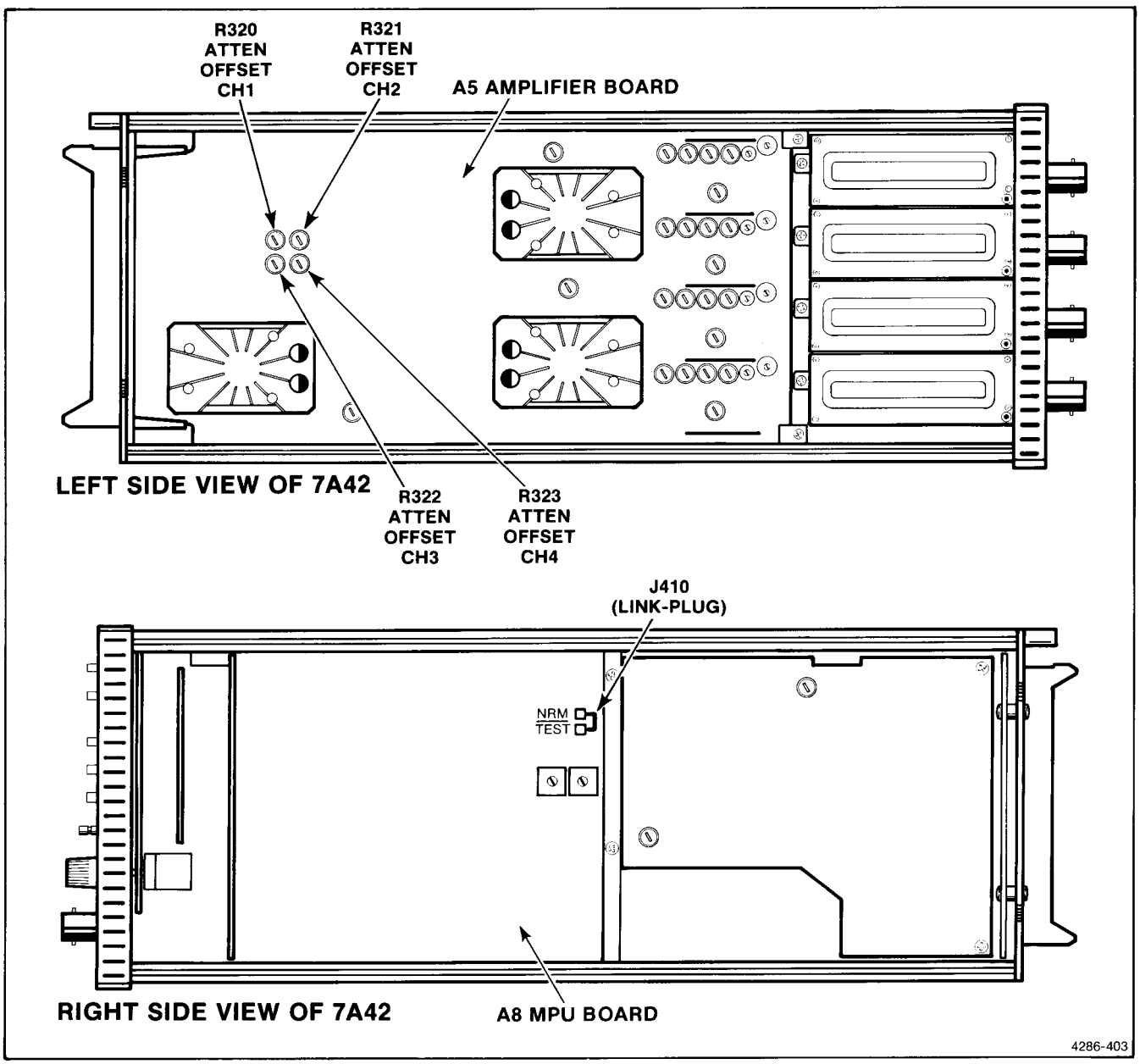
f. Press A to stop cycle.

g. Turn power off.

h. Replace the link-plug on J410.

i. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

B2. ADJUSTMENT LOCATIONS



C. AMPLIFIER

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment):

1. Oscilloscope Mainframe
2. Time-Base Unit
3. Calibration Generator
11. Flexible Plug-In Extender (Two required)
14. Coaxial Cable (Two required)
22. 10X Attenuator
24. Alignment Tool

C1. PRELIMINARY SETUP

a. Perform the Adjustment Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

c. Set the oscilloscope mainframe and time-base unit controls:

MAINFRAME
- Power ..... On
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Source ..... Left Vert
- B Intensity ..... Visible display
- Readout ..... Visible display
- Focus ..... Well defined display

TIME BASE
- Triggering
  - Mode ..... Auto
  - Coupling ..... Dc
  - Source ..... Ext
  - Time/Div ..... 1 μs
  - Mag ..... X1 (In)

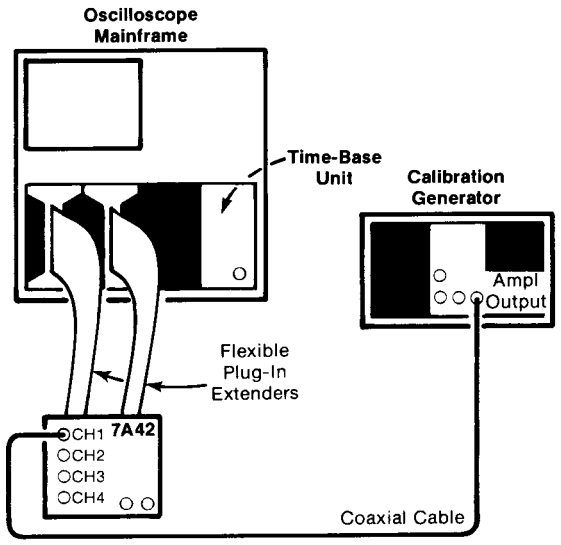
C2. ADJUST AMPLIFIER GAIN (R1010, R1030, R1040, R1060)

NOTE

First perform step C1, then proceed.

C2. SETUP CONDITIONS

7A42 Controls:
- CH1 POSITION ..... Midrange
- CH2 POSITION ..... Midrange
- CH3 POSIITON ..... Midrange
- CH4 POSITION ..... Midrange



Test Equipment Controls:
Calibration Generator
- Mode ..... Std. Ampl.
- Amplitude ..... 0.1 V

4286-404

a. Initialize the 7A42 front-panel settings by turning the oscilloscope mainframe power off, then back on.

b. Press the TTL/ECL button (CH1 ECL TTL light off).

c. Press the upper VOLTS/DIV button until a crt readout of 20 mV is displayed.

d. Set the front-panel GAIN adjustment to the center of its range. Position the bottom of the waveform 2 divisions below the center horizontal graticule line, using the CH1 POSITION control.

e. **EXAMINE**—the display for a signal amplitude of 5 divisions, within 0.1 division.

f. **ADJUST**—CH1 Gain, R1010, for exactly 5 divisions of signal amplitude.

g. Press the DISPLAY button (CH1 DISPLAY light out).

h. Move the coaxial cable from the CH1 input to the CH2 input connector.

i. Press the CH2 button (CH2 button light on).

j. Press the DISPLAY button (CH2 DISPLAY light on).

k. Press the TRIG VIEW button (button light off).

l. Press the TTL/ECL button (CH2 ECL TTL light off).

m. Press the upper VOLTS/DIV button until a crt readout of 20 mV is displayed.

n. Position the bottom of the waveform 2 divisions below the center horizontal graticule line, using the CH2 POSITION control.

o. **EXAMINE**—the display for a signal amplitude of 5 divisions, within 0.1 division.

p. **ADJUST**—CH2 Gain, R1030, for exactly 5 divisions of signal amplitude.

q. Press the DISPLAY button (CH2 DISPLAY light out).

r. Move the coaxial cable from the CH2 input to the CH3 input connector.

s. Press the CH3 button (CH3 button light on).

t. Press the DISPLAY button (CH3 DISPLAY light on).

u. Press the TRIG VIEW button (button light off).

v. Press the TTL/ECL button (CH2 ECL TTL light off).

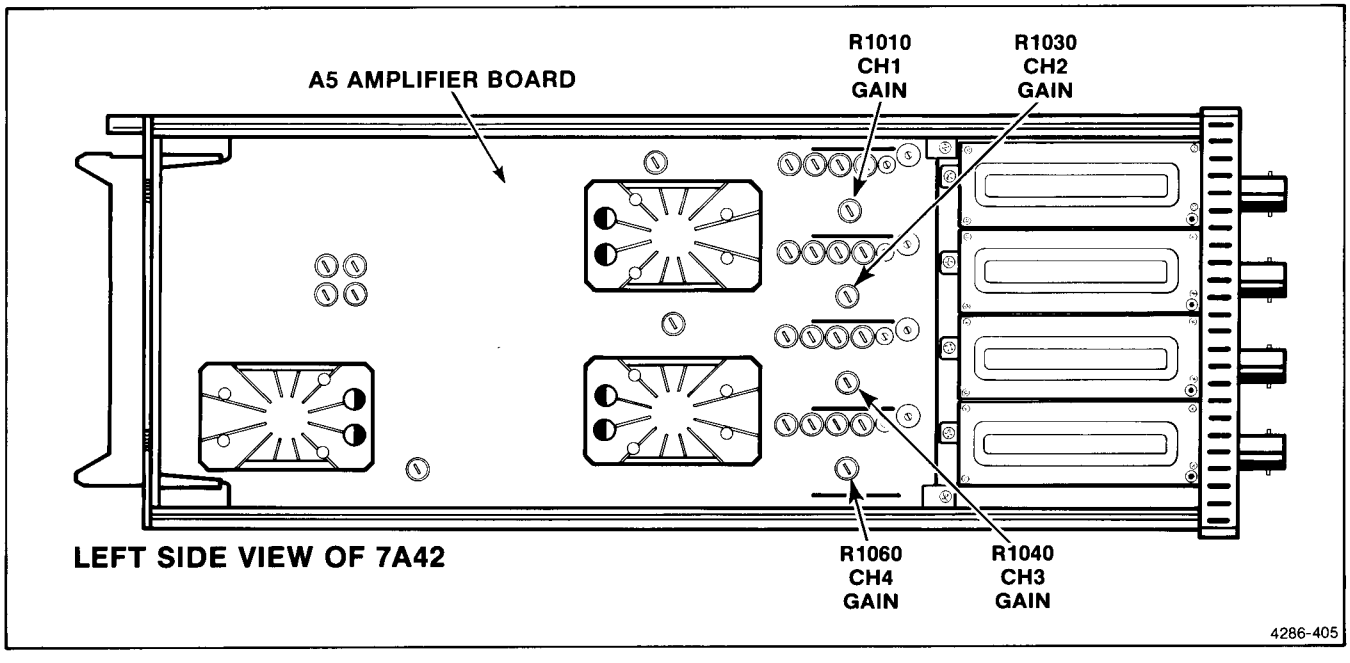
w. Press the upper VOLTS/DIV button until a crt readout of 20 mV is displayed.

x. Position the bottom of the waveform 2 divisions below the center horizontal graticule line, using the CH3 POSITION control.

y. **EXAMINE**—the display for a signal amplitude of 5 divisions, within 0.1 division.

z. **ADJUST**—CH3 Gain, R1040, for exactly 5 divisions of signal amplitude.

C2. ADJUSTMENT LOCATIONS



aa. Press the DISPLAY button (CH3 DISPLAY light out).

bb. Move the coaxial cable from the CH3 input to the CH4 input connector.

cc. Press the CH4 button (CH4 button light on).

dd. Press the DISPLAY button (CH4 DISPLAY light on).

ee. Press the TRIG VIEW button (button light off).

ff. Press the TTL/ECL button (CH4 ECL TTL light off).

gg. Press the upper VOLTS/DIV button until a crt readout of 20 mV is displayed.

hh. Position the bottom of the waveform 2 divisions below the center horizontal graticule line, using the CH4 POSITION control.

ii. **EXAMINE**—the display for a signal amplitude of 5 divisions, within 0.1 divisions.

jj. **ADJUST**—CH4 Gain, R1060, for exactly 5 divisions of signal amplitude.

kk. Disconnect the coaxial cable from the CH4 input connector.

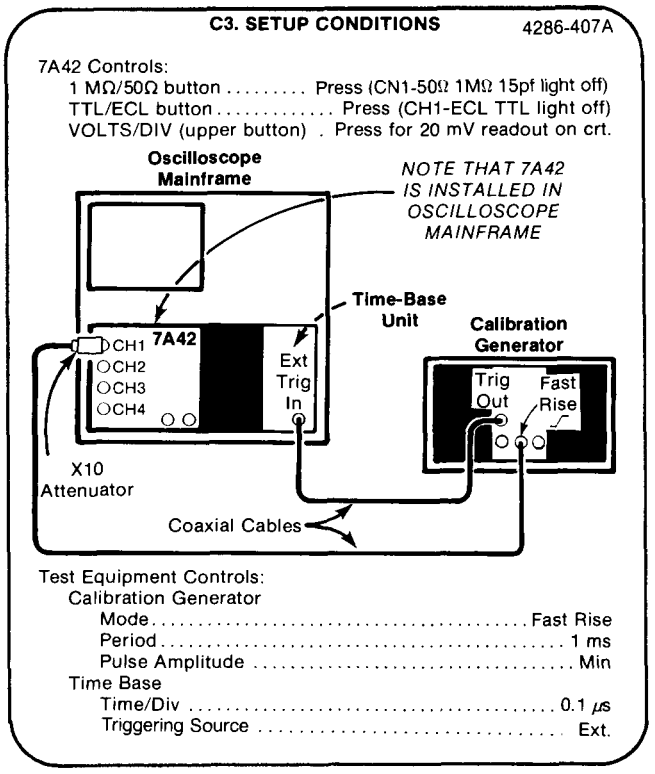
ll. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

C3. ADJUST AMPLIFIER COMPENSATION (R903, R902, R700, R901, R1000, C1100, C1000, R922, R921, R920, R1020, C1120, C1020, R935, R934, R730, R933, R1031, C1130, C1031, R953, R952, R951, R1050, C1150, C1050)

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

a. Turn the oscilloscope mainframe Power off, then back on again to initialize the front-panel control settings.



b. Set the calibration generator Pulse Amplitude control to display 5 divisions of signal amplitude on the crt. Adjust the Triggering Level control as necessary for a stable display.

c. Center the rising edge of the pulse both vertically and horizontally on the graticule.

d. Perform the Step 1 setup shown in Table 4-5 and adjust the CH1 adjustment.

e. Perform the Step 2 setup, and adjust the CH1 adjustment. Adjust the time-base unit Triggering as necessary.

f. Perform the Step 3 adjustment for CH1.

g. Perform the Step 4 setup, and adjust the CH1 adjustment. (Adjust the oscilloscope B Intensity for desired display.)

h. Perform the setup for steps 5, 6, and 7, and adjust the appropriate adjustments for CH1.

i. Move the X10 attenuator and signal to the next channel input connector (i.e., CH2).

j. Press the DISPLAY button (channel DISPLAY light out).

k. Press the next channel button (i.e., CH2).

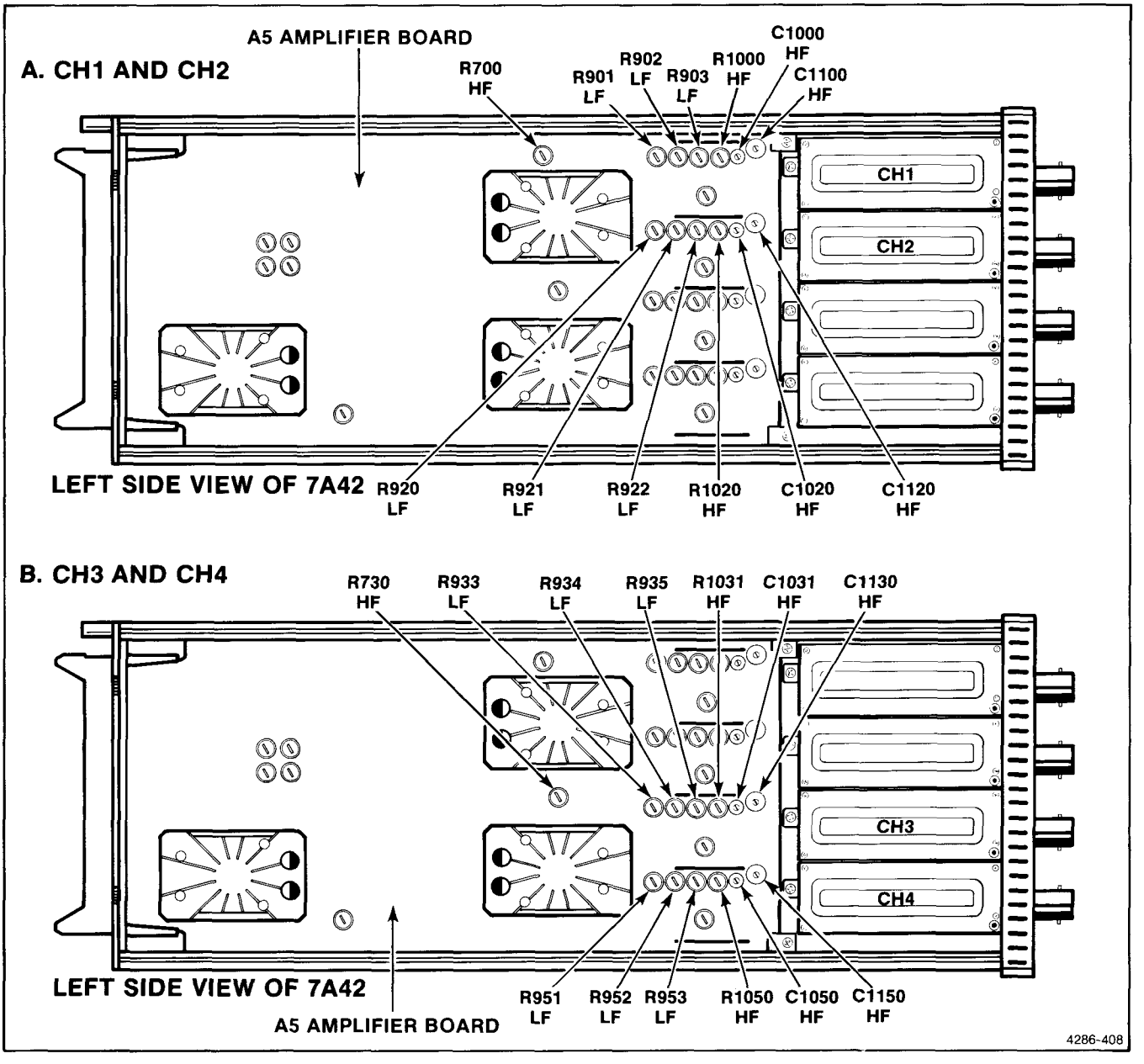
l. Press the DISPLAY button again.

m. Press the TRIG VIEW button to remove the unwanted trace.

n. Press the 1 MΩ/50 Ω button (50 Ω/MΩ 15 pF light out).

o. Press the TTL/ECL button (ECL TTL light out).

C3. ADJUSTMENT LOCATIONS



p. Press the upper VOLTS/DIV button until a 20 mV readout is displayed on the crt.

q. Repeat parts b through p for each of the remaining three channels.

r. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

TABLE 4-5
High- and Low-Frequency Compensation Adjustments

SETUP			ADJUSTMENT				ADJUST FOR
Step	Time/Div	Function Generator	CH1	CH2	CH3	CH4	
1	0.1 ms	1 ms	R901 LF	R920 LF	R933 LF	R951 LF	Optimum pulse flat top.
2	1 μs	10 μs	R902 LF	R921 LF	R934 LF	R952 LF	Optimum pulse flat top.
3	20 ns	1 μs	R700 HF	—	R730 HF	—	Maximum overshoot.[2]
4	20 ns	1 μs	R903 LF	R922 LF	R935 LF	R953 LF	Optimum pulse flat top.
5	20 ns	1 μs	R1000 HF	R1020 HF	R1031 HF	R1150 HF	Optimum square corner.[1]
6	20 ns	1 μs	C1100 HF	C1120 HF	C1130 HF	C1150 HF	Optimum square corner.[1]
7	20 ns	1 μs	C1000 HF	C1020 HF	C1031 HF	C1050 HF	Minimum spike amplitude.[1]

[1]This adjustment may have to be compromised in order to meet the minimum bandwidth specifications. To verify proper adjustment of each channel, perform the "A4. CHECK BANDWIDTH" procedure located in Part II—Performance Check Procedure in this section. If the bandwidth specifications are not met, the adjustments should be compromised until the required bandwidth is obtained.

[2]Further optimization can be obtained by setting these two adjustments for maximum gain (displayed amplitude) using a 300 MHz sine-wave input signal.

D. TRIGGER THRESHOLD AND PROBE OFFSET

Equipment Required (Numbers correspond to those listed in Table 4-2, Test Equipment):

1. Oscilloscope Mainframe
2. Time-Base Unit
3. Calibration Generator
4. Digital Multimeter
10. Power Supply
11. Flexible Plug-In Extender (Two required)
14. Coaxial Cable
17. Patch Cords (two required)
18. Meter Leads
23. 50Ω Feedthrough Terminator
24. Alignment Tool

D1. PRELIMINARY SETUP

a. Perform the Adjustment Initial Setup Procedure.

b. Refer to Section 5, Instrument Options, and to the change information at the rear of the manual for any modifications which may affect this procedure.

c. Set the oscilloscope mainframe and time-base unit controls:

MAINFRAME
- Power ..... On
- Vertical Mode ..... Left
- Horizontal Mode ..... B
- B Trigger Source ..... Left Vert
- B Intensity ..... Visible display
- Readout ..... Visible display
- Focus ..... Well defined display

TIME BASE
- Triggering
  - Mode ..... Auto
  - Coupling ..... Dc
  - Source ..... Int
- Time/Div ..... 1 μs
- Mag ..... X1 (In)

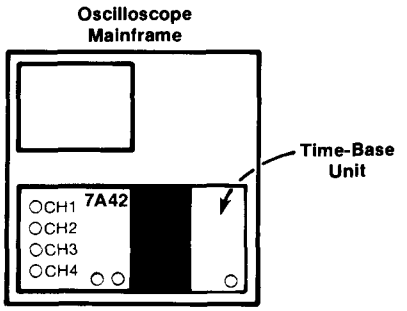
D2. ADJUST TRIGGER VIEW POSITION (R460)

NOTE

First perform step D1, then proceed.

D2. SETUP CONDITIONS

7A42 Controls:
DISPLAY button ..... Press (CH1 DISPLAY light out)

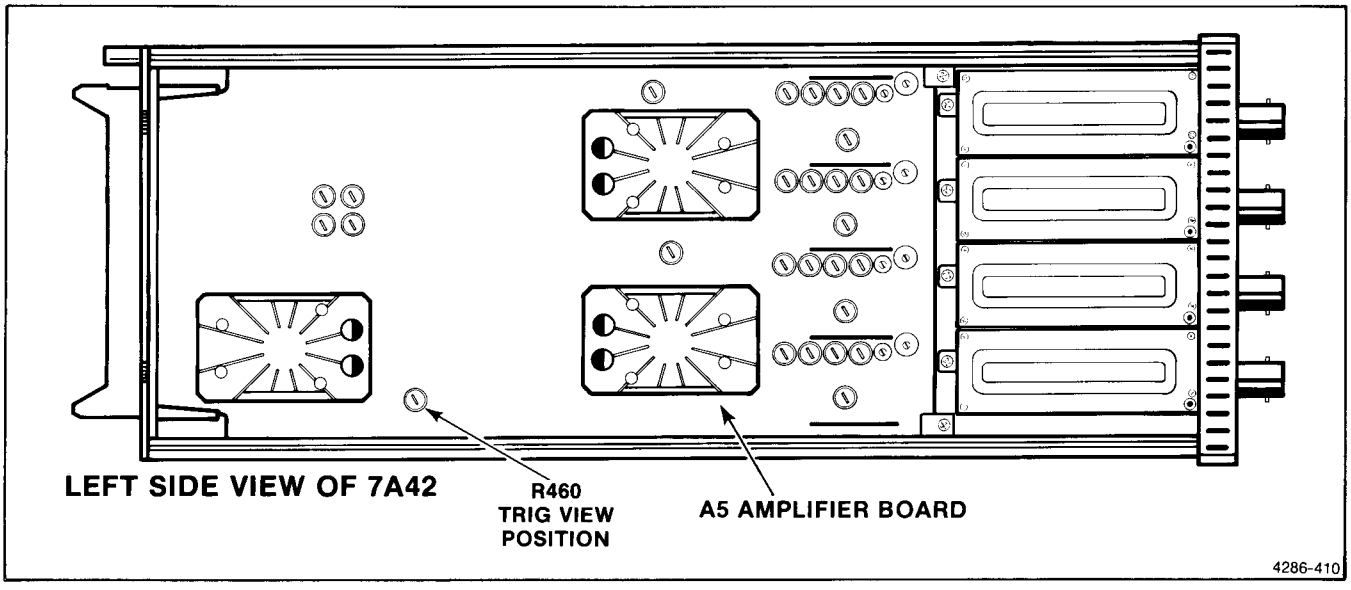


a. Press the TRIG VIEW button (button light on).

b. **ADJUST**—Trig View Position, R460, to position the trace exactly 3 divisions below the center horizontal graticule line.

c. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

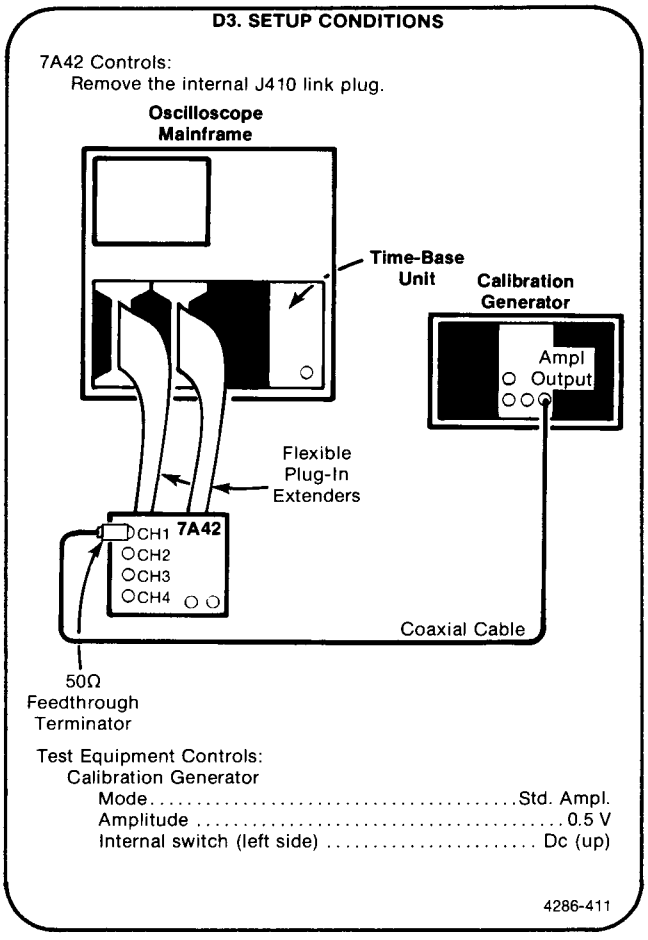
D2. ADJUSTMENT LOCATION



D3. ADJUST TRIGGER THRESHOLDS (R300, R302, R301, R303, R400, R402, R401, R403)

NOTE

If the preceding step was not performed, first perform step D1, then proceed.



a. Turn the oscilloscope mainframe Power off. Remove the link-plug from J410. Turn the oscilloscope mainframe Power on.

b. Press the NOT button.

c. **ADJUST**—Offset CH1, R302 by rotating the adjustment throughout its range and observing that the trigger view trace jumps both up and down. Observe the adjustment setting when the trigger view trace jumps up, and when the trigger view trace jumps down. Center the adjustment between these observed transition points.

d. Press the NOT button.

e. **ADJUST**—Offset CH2, R303 by rotating the adjustment throughout its range and observing that the trigger view trace jumps both up and down. Observe the adjustment setting when the trigger view trace jumps up, and when the trigger view trace jumps down. Center the adjustment between these observed transition points.

f. Press the NOT button.

g. **ADJUST**—Offset CH3, R402 by rotating the adjustment throughout its range and observing that the trigger view trace jumps both up and down. Observe the adjustment setting when the trigger view trace jumps up, and when the trigger view trace jumps down. Center the adjustment between these observed transition points.

h. Press the NOT button.

i **ADJUST**—Offset CH4, R403 by rotating the adjustment throughout its range and observing that the trigger view trace jumps both up and down. Observe the adjustment setting when the trigger view trace jumps up, and when the trigger view trace jumps down. Center the adjustment between these observed transition points.

j. Press the NOT button.

k. **ADJUST**—Gain CH1, R300 by rotating the adjustment throughout its range and observing that the trigger view trace jumps both up and down. Observe the adjustment setting when the trigger view trace jumps up, and when the trigger view trace jumps down. Center the adjustment between these observed transition points.

l. Press the NOT button.

m. Move the coaxial cable from the CH1 input connector to the CH2 input connector.

n. **ADJUST**—Gain CH2, R301 by rotating the adjustment throughout its range and observing that the trigger view trace jumps both up and down. Observe the adjustment setting when the trigger view trace jumps up, and when the trigger view trace jumps down. Center the adjustment between these observed transition points.

o. Press the NOT button.

p. Move the coaxial cable from the CH2 input connector to the CH3 input connector.

q. **ADJUST**—Gain CH3, R400 by rotating the adjustment throughout its range and observing that the trigger view trace jumps both up and down. Observe the adjustment setting when the trigger view trace jumps up, and when the trigger view trace jumps down. Center the adjustment between these observed transition points.

r. Press the NOT button.

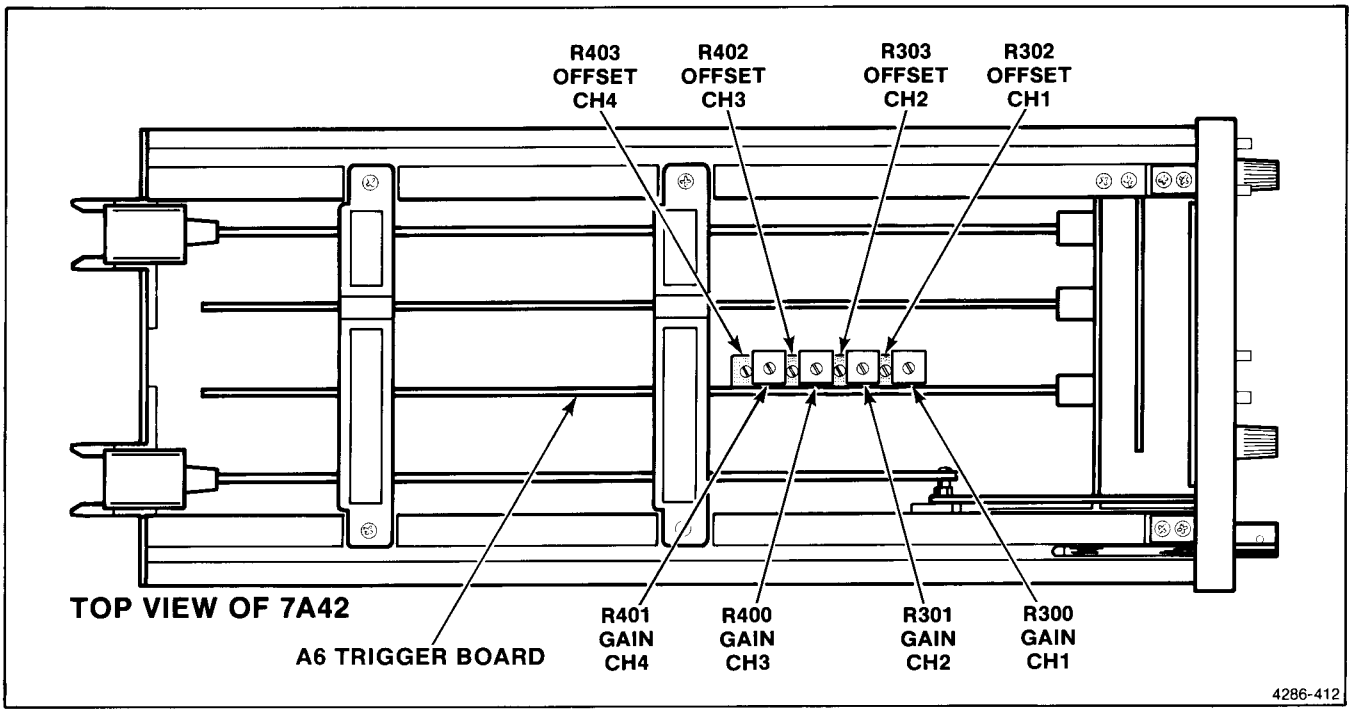
s. Move the coaxial cable from the CH3 input connector to the CH4 input connector.

t. **ADJUST**—Gain CH4, R401 by rotating the adjustment throughout its range and observing that the trigger view trace jumps both up and down. Observe the adjustment setting when the trigger view trace jumps up, and when the trigger view trace jumps down. Center the adjustment between these observed transition points.

u. Turn the oscilloscope mainframe Power off and replace the internal J410 link plug you removed in the D3. Setup Conditions.

v. If you do not intend to perform the following step, replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

D3. ADJUSTMENT LOCATIONS



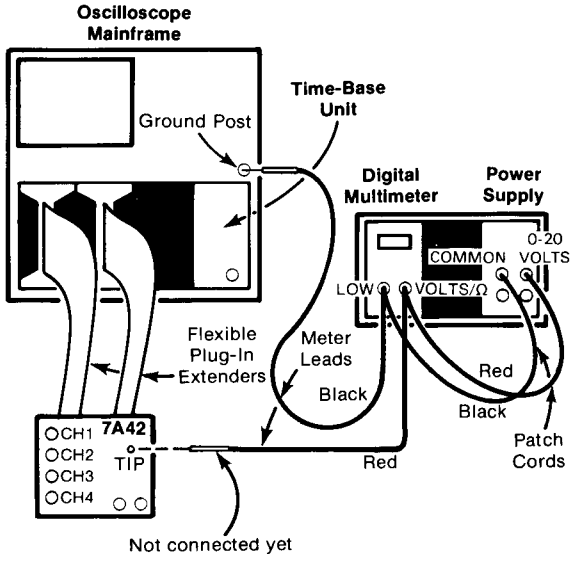
D4. ADJUST PROBE OFFSET (R425, R525)

NOTE

If the preceeding step was not performed, first perform step D1, then proceed.

D4. SETUP CONDITIONS

7A42 Controls:
No change.



Test Equipment Controls:
Digital Multimeter
Range/Function ..... 20 V
Volts ..... Dc
Input ..... Ext (out)
Power Supply
Output button ..... On (pressed in)

4286-413

a. Turn the oscilloscope mainframe Power off, then back on again to initialize the front-panel control settings.

b. Press the THRESH button (button light on).

c. Press the PROBE OFFSET button (button red light on).

d. **EXAMINE**—the SWITCHING THRESHOLD readout should read 0.00 volts.

e. **ADJUST**—DVM Offset, R425, for a reading of 0.00 volts on the SWITCHING THRESHOLD readout display. Observe the adjustment position at +0.04 volts, then observe the adjustment position at -0.04 volts. Center the adjustment between the two positions where the readout display reads +0.04 and -0.04 volts.

f. Set the power-supply output voltage for a reading of 5.00 volts on the digital multimeter.

g. Connect the red meter lead to the TIP connector on the 7A42 front panel.

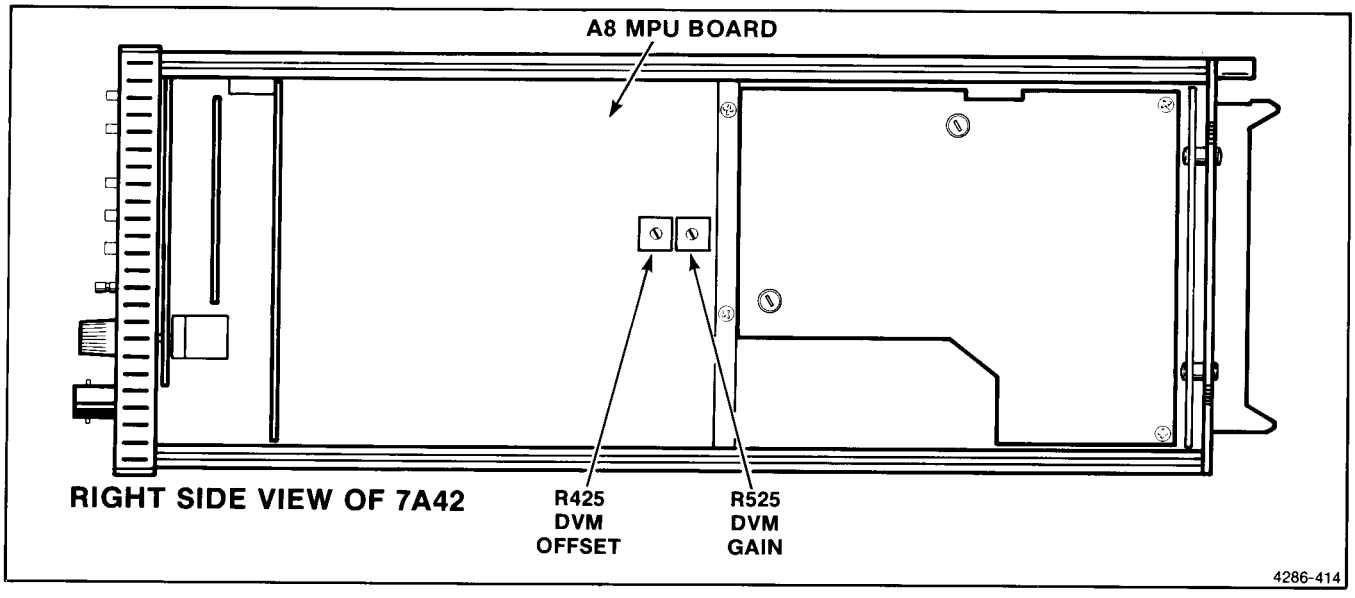
h. **EXAMINE**—the SWITCHING THRESHOLD readout display for a reading of 5.00 volts, within 0.10 volts.

i. **ADJUST**—DVM Gain, R525, for a SWITCHING THRESHOLD readout display of exactly 5.00 volts.

j. Turn the oscilloscope mainframe Power off. Replace the J747 BE (Battery Enable) link plug that you removed in the Initial Setup Procedure.

This completes the Part III—Adjustment Procedure.

D4. ADJUSTMENT LOCATIONS



INSTRUMENT OPTIONS

No options existed for the 7A42 at the time of this printing. Information about any subsequent options will be included in the CHANGE INFORMATION section at the back of this manual.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

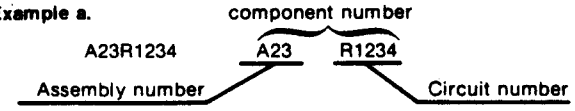
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

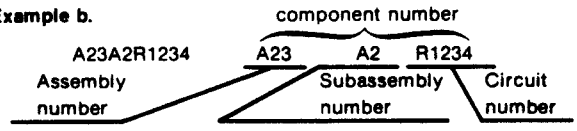
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00213	NYTRONICS COMPONENTS GROUP INC SUBSIDIARY OF NYTRONICS INC	ORANGE ST	DARLINGTON SC 29532
00853	SANGAMO WESTON INC COMPONENTS DIV	SANGAMO RD PO BOX 128	PICKENS SC 29671-9716
01121	ALLEN-BRADLEY CO	1201 SOUTH 2ND ST	MILWAUKEE WI 53204-2410
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXP PO BOX 655012	DALLAS TX 75265
02735	RCA CORP SOLID STATE DIVISION	ROUTE 202	SOMERVILLE NJ 08876
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	W GENESEE ST	AUBURN NY 13021
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS SECTOR	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
07263	FAIRCHILD SEMICONDUCTOR CORP NORTH AMERICAN SALES SUB OF SCHLUMBERGER LTD MS 118	10400 RIDGEVIEW CT	CUPERTINO CA 95014
07716	TRW INC TRW IRC FIXED RESISTORS/BURLINGTON	2850 MT PLEASANT AVE	BURLINGTON IA 52601
09052	SAFT AMERICA INC POWER SOURCES DIV	711 INDUSTRIAL BLVD PO BOX 1886	VALDOSTA GA 31603
11236	CTS CORP BERNE DIV THICK FILM PRODUCTS GROUP	406 PARR ROAD	BERNE IN 46711-9506
12697	CLAROSTAT MFG CO INC	LOWER WASHINGTON ST	DOVER NH 03820
14552	MICROSEMI CROP	2830 S FAIRVIEW ST	SANTA ANA CA 92704-5948
15513	DATA DISPLAY PRODUCTS	301 CORAL CIR	EL SEGUNDO CA 90245-4620
18324	SIGNETICS CORP MILITARY PRODUCTS DIV	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
19701	MEPCO/CENTRALAB A NORTH AMERICAN PHILIPS CO	P O BOX 760	MINERAL WELLS TX 76067-0760
20932	KYOCERA INTERNATIONAL INC	11620 SORRENTO VALLEY RD PO BOX 81543 PLANT NO 1	SAN DIEGO CA 92121
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS DIV MILITARY PRODUCTS GROUP	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
24355	ANALOG DEVICES INC	RT 1 INDUSTRIAL PK PO BOX 9106	NORWOOD MA 02062
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701-3737
24931	SPECIALTY CONNECTOR CO INC	2100 EARLYWOOD DR PO BOX 547	FRANKLIN IN 46131
24972	AEG-TELEFUNKEN CORP	RT 22 ORR DR P O BOX 3800	SUMMERVILLE NJ 08876-3333
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051-0606
32293	INTERSIL INC SUB OF GENERAL ELECTRIC CO	10600 RIDGEVIEW COURT	CUPERTINO CA 95014-0704
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507-2114
34333	SILICON GENERAL INC	11651 MONARCH ST	GARDEN GROVE CA 92641-1816
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL	SUNNYVALE CA 94086-4518
34371	HARRIS CORP HARRIS SEMICONDUCTOR PRODUCTS GROUP	200 PALM BAY BLVD PO BOX 883	MELBOURNE FL 32919
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
51642	CENTRE ENGINEERING INC	2820 E COLLEGE AVE	STATE COLLEGE PA 16801-7515
54473	MATSUSHITA ELECTRIC CORP OF AMERICA	ONE PANASONIC WAY PO BOX 1501	SECAUCUS NJ 07094-2917
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195-4526
56289	SPRAGUE ELECTRIC CO WORLD HEADQUARTERS	92 HAYDEN AVE	LEXINGTON MA 02173-7929
57668	ROHM CORP	16931 MILLIKEN AVE	IRVINE CA 92713
58361	GENERAL INSTRUMENT CORP OPTOELECTRONICS DIV	3400 HILLVIEW AVE	PALO ALTO CA 94304-1319

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
59660	TUSONIX INC	7741 N BUSINESS PARK DR PO BOX 37144	TUCSON AZ 85740-7144
71279	MIDLAND-ROSS CORP CAMBION DIV	ONE ALEWIFE PLACE	CAMBRIDGE MA 02138-2310
72982	ERIE SPECIALTY PRODUCTS INC	645 W 11TH ST	ERIE PA 16512
73138	BECKMAN INDUSTRIAL CORP BECKMAN ELECTRONIC TECHNOLOGIES SUB OF EMERSON ELECTRIC	4141 PALM ST	FULLERTON CA 92635
75042	IRC ELECTRONIC COMPONENTS PHILADELPHIA DIV TRW FIXED RESISTORS	401 N BROAD ST	PHILADELPHIA PA 19108-1001
76493	BELL INDUSTRIES INC JW MILLER DIV	19070 REYES AVE PO BOX 5825	COMPTON CA 90224-5825
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500 MS 53-111	BEAVERTON OR 97707-0001
91637	DALE ELECTRONICS INC	2064 12TH AVE PO BOX 609	COLUMBUS NE 68601-3632
95238	CONTINENTAL CONNECTOR CORP	34-63 56TH ST	WOODSIDE NY 11377-2121
S4431	MURATA MFG CO LTD	16 KAIDEN NISHIJM CHO NAGAOKAKY-CITY	KYOTO JAPAN
TK0271	COMPONENT CONCEPTS INC	3229 PINE ST	EVERETT WA 98201-4536
TK0510	PANASONIC COMPANY DIV OF MATSUSHITA ELECTRIC CORP	ONE PANASONIC WAY	SECAUCUS NJ 07094
TK1345	ZMAN AND ASSOCIATES	7633 S 180TH	KENT WA 98032
TK2042	ZMAN & ASSOCIATES	7633 S 180TH	KENT WA 98032

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
AT10	119-1517-00			ATTENUATOR,VAR: (LIMITED ATTENUATOR SUBPARTS AVAILABLE)	80009	119-1517-00
AT20	119-1517-00			ATTENUATOR,VAR: (LIMITED ATTENUATOR SUBPARTS AVAILABLE)	80009	119-1517-00
AT30	119-1517-00			ATTENUATOR,VAR: (LIMITED ATTENUATOR SUBPARTS AVAILABLE)	80009	119-1517-00
AT40	119-1517-00			ATTENUATOR,VAR: (LIMITED ATTENUATOR SUBPARTS AVAILABLE)	80009	119-1517-00
A1	670-7435-00			CIRCUIT BD ASSY:FRONT PANEL,SWITCH	80009	670-7435-00
A2	670-7436-00			CIRCUIT BD ASSY:FRONT PANEL,LED	80009	670-7436-00
A3	670-7438-00			CIRCUIT BD ASSY:INTCON	80009	670-7438-00
A4	670-7439-00			CIRCUIT BD ASSY:ATTENUATOR CONTROL	80009	670-7439-00
A5	670-7440-00	B010100	B010199	CIRCUIT BD ASSY:AMPL	80009	670-7440-00
A5	670-7440-01	B010200	B010624	CIRCUIT BD ASSY:AMPLIFIER	80009	670-7440-01
A5	670-7440-02	B010625	B010853	CIRCUIT BD ASSY:AMPLIFIER	80009	670-7440-02
A5	670-7440-03	B010854		CIRCUIT BD ASSY:AMPLIFIER	80009	670-7440-03
A6	672-1100-00			CIRCUIT BD ASSY:TRIGGER (NO LONGER AVAILABLE)	80009	672-1100-00
A6A1	670-7441-00	B010100	B010624	CIRCUIT BD ASSY:TRIGGER	80009	670-7441-00
A6A1	670-7441-01	B010625		CIRCUIT BD ASSY:TRIGGER	80009	670-7441-01
A6A2	670-7940-00			CIRCUIT BD ASSY:TRIGGER SHIELD 388-8268-XX (NO ELECTRICAL PARTS)	80009	670-7940-00
A6A3	670-7941-00			CIRCUIT BD ASSY:TRIGGER SHIELD (NO ELECTRICAL PARTS)	80009	670-7941-00
A7	670-7442-00			CIRCUIT BD ASSY:DIGITAL	80009	670-7442-00
A8	670-7443-00	B010100	B010825	CIRCUIT BD ASSY:MPU	80009	670-7443-00
A8	670-7443-01	B010826		CIRCUIT BD ASSY:MPU	80009	670-7443-01
A9	670-7513-00			CIRCUIT BD ASSY:PWR SPLY	80009	670-7513-00
A10	670-7514-00			CIRCUIT BD ASSY:DVM	80009	670-7514-00
AT10	119-1517-00			ATTENUATOR,VAR: (LIMITED ATTENUATOR SUBPARTS AVAILABLE)	80009	119-1517-00
AT10K11	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT10K12	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT10K13	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT10K14	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT10K15	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT20	119-1517-00			ATTENUATOR,VAR: (LIMITED ATTENUATOR SUBPARTS AVAILABLE)	80009	119-1517-00
AT20K11	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT20K12	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT20K13	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
AT20K14	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT20K15	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT30	119-1517-00			ATTENUATOR,VAR: (LIMITED ATTENUATOR SUBPARTS AVAILABLE)	80009	119-1517-00
AT30K11	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT30K12	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT30K13	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT30K14	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT30K15	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT40	119-1517-00			ATTENUATOR,VAR: (LIMITED ATTENUATOR SUBPARTS AVAILABLE)	80009	119-1517-00
AT40K11	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT40K12	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT40K13	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT40K14	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
AT40K15	148-0145-00			RELAY,ARMATURE:LATCHING	80009	148-0145-00
A1	670-7435-00			CIRCUIT BD ASSY:FRONT PANEL,SWITCH	80009	670-7435-00
A1DS170	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1DS171	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS270	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS271	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS272	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1DS370	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS371	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS372	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS470	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1DS471	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS472	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS570	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS571	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1DS572	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS670	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1DS671	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A1J140	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 26)	22526	48283-036
A1S100	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S110	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S140	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S150	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S200	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S201	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S240	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S241	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S250	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S251	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S300	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S340	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S350	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S351	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S400	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S440	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S441	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S450	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1S451	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S520	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S530	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S540	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S541	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S550	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S551	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S640	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A1S650	263-0020-00			SWITCH PB ASSY:MOMENTARY	80009	263-0020-00
A2	670-7436-00			CIRCUIT BD ASSY:FRONT PANEL,LED	80009	670-7436-00
A2C210	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2DS150	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A2DS160	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A2DS200	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS300	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A2DS310	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS320	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS350	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A2DS400	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A2DS410	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS420	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS450	150-1078-00			LT EMITTING DIO:GREEN,565NM,20MA	50434	HLMP 1503
A2DS500	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A2DS510	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS520	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS610	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS620	150-0755-00			LT EMITTING DIO:ORN/GRN,630NM/560NM,30MA	24972	CQX 95
A2DS760	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A2DS820	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A2DS840	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
A2DS860	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A2DS960	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A2DS1060	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A2J110	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 1)	22526	48283-029
A2J260	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 26)	22526	48283-036
A2J340	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 34)	22526	48283-036
A2J710	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 3)	22526	48283-029
A2R210	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A3	670-7438-00			CIRCUIT BD ASSY:INTCON	80009	670-7438-00
A3J100	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 26)	22526	48283-036
A3J120	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 26)	22526	48283-036
A3J200	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 34)	22526	48283-036
A3J300	131-2843-00			CONN,RCPT,ELEC:EDGECARD,2 X 36,0.1 SPACING	95238	K600-121-72 DD16
A3J400	131-2843-00			CONN,RCPT,ELEC:EDGECARD,2 X 36,0.1 SPACING	95238	K600-121-72 DD16
A3J500	131-2843-00			CONN,RCPT,ELEC:EDGECARD,2 X 36,0.1 SPACING	95238	K600-121-72 DD16
A3J600	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 26)	22526	48283-036
A3J700	131-2724-00			CONN,RCPT,ELEC:CKT BD,RTANG,2 X 5,0.1 CTR (QUANTITY OF 4)	22526	67117-005

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A4	670-7439-00			CIRCUIT BD ASSY:ATTENUATOR CONTROL	80009	670-7439-00
A4C101	290-0943-00			CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A4C102	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A4C104	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C106	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A4C110	290-0943-00			CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A4C115	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C118	281-0826-00			CAP,FXD,CER DI:2200PF,10%,100V	20932	401EM100AD222K
A4C201	290-0943-00			CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A4C202	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A4C204	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C206	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A4C215	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C301	290-0943-00			CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A4C302	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A4C306	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A4C311	290-0943-00			CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A4C315	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C317	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C401	290-0943-00			CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A4C402	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A4C406	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A4C414	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C415	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C416	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4CR101	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR102	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR103	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR104	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR105	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR106	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR110	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR111	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR112	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR113	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR201	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR202	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR203	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR204	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR205	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR206	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR210	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR211	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR212	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR213	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR301	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR302	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR303	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR304	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR305	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR306	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR310	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR311	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR312	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR313	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR401	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A4CR402	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR403	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR404	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR405	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR406	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR411	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR412	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR413	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR414	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4J700	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 40)	22526	48283-029
A4J1100	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A4J1110	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A4J1120	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A4J1121	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A4J1140	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A4J1141	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A4J1150	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A4J1160	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A4P112	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A4P211	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A4P311	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A4P411	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A4R101	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R102	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R110	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R111	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R112	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A4R210	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R211	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A4R301	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R310	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R311	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A4R401	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R410	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R411	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A5	670-7440-00	B010100	B010199	CIRCUIT BD ASSY:AMPL	80009	670-7440-00
A5	670-7440-01	B010200	B010624	CIRCUIT BD ASSY:AMPLIFIER	80009	670-7440-01
A5	670-7440-02	B010625	B010853	CIRCUIT BD ASSY:AMPLIFIER	80009	670-7440-02
A5	670-7440-03	B010854		CIRCUIT BD ASSY:AMPLIFIER	80009	670-7440-03
A5C120	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C121	290-0745-00			CAP,FXD,ELCTLT:22UF,+50-20%,25WVDC	54473	ECE-A25V22L
A5C135	281-0758-00			CAP,FXD,CER DI:15PF,20%,100V	04222	MA101A150MAA
A5C203	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C212	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C220	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C300	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C310	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C360	290-0847-00			CAP,FXD,ELCTLT:47UF,+50-20%,10WVDC	55680	TLB1A470MAA2
A5C400	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	SA106E222MAA
A5C403	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	SA106E222MAA
A5C410	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	SA106E222MAA
A5C411	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	SA106E222MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5C412	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C430	290-0745-00			CAP,FXD,ELCTLT:22UF,+50-20%,25WVDC	54473	ECE-A25V22L
A5C530	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C610	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C620	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-20 %,10V	55680	ULA1A220TAA
A5C700	283-0397-00	B010100	B010199	CAP,FXD,CER DI:1160PF,2%,100V	04222	SR301AVG6GAA
A5C700	283-0195-00	B010200	B010853	CAP,FXD,CER DI:680PF,5%,50V (TEST SELECTABLE)	04222	SR205A681JAA
A5C700	283-0397-00	B010854		CAP,FXD,CER DI:1160PF,2%,100V	04222	SR301AVG6GAA
A5C760	283-0397-00	B010100	B010199	CAP,FXD,CER DI:1160PF,2%,100V	04222	SR301AVG6GAA
A5C760	283-0195-00	B010200	B010853	CAP,FXD,CER DI:680PF,5%,50V (TEST SELECTABLE)	04222	SR205A681JAA
A5C760	283-0397-00	B010854		CAP,FXD,CER DI:1160PF,2%,100V	04222	SR301AVG6GAA
A5C833	283-0397-00	B010100	B010199	CAP,FXD,CER DI:1160PF,2%,100V	04222	SR301AVG6GAA
A5C833	283-0195-00	B010200	B010853	CAP,FXD,CER DI:680PF,5%,50V (TEST SELECTABLE)	04222	SR205A681JAA
A5C833	283-0397-00	B010854		CAP,FXD,CER DI:1160PF,2%,100V	04222	SR301AVG6GAA
A5C834	283-0397-00	B010100	B010199	CAP,FXD,CER DI:1160PF,2%,100V	04222	SR301AVG6GAA
A5C834	283-0195-00	B010200	B010853	CAP,FXD,CER DI:680PF,5%,50V (TEST SELECTABLE)	04222	SR205A681JAA
A5C834	283-0397-00	B010854		CAP,FXD,CER DI:1160PF,2%,100V	04222	SR301AVG6GAA
A5C912	283-0339-00			CAP,FXD,CER DI:0.22UF,10%,50V	05397	C330C224K5R5CA
A5C913	283-0398-00			CAP,FXD,CER DI:680PF,2%,100V	04222	3429100A681G
A5C914	283-0398-00			CAP,FXD,CER DI:680PF,2%,100V	04222	3429100A681G
A5C915	283-0144-00			CAP,FXD,CER DI:33PF,2%,500V	59660	801-547P2G330G
A5C932	283-0339-00			CAP,FXD,CER DI:0.22UF,10%,50V	05397	C330C224K5R5CA
A5C933	283-0398-00			CAP,FXD,CER DI:680PF,2%,100V	04222	3429100A681G
A5C934	283-0398-00			CAP,FXD,CER DI:680PF,2%,100V	04222	3429100A681G
A5C935	283-0144-00			CAP,FXD,CER DI:33PF,2%,500V	59660	801-547P2G330G
A5C936	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C942	283-0339-00			CAP,FXD,CER DI:0.22UF,10%,50V	05397	C330C224K5R5CA
A5C943	283-0398-00			CAP,FXD,CER DI:680PF,2%,100V	04222	3429100A681G
A5C944	283-0398-00			CAP,FXD,CER DI:680PF,2%,100V	04222	3429100A681G
A5C945	283-0144-00			CAP,FXD,CER DI:33PF,2%,500V	59660	801-547P2G330G
A5C946	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C963	283-0339-00			CAP,FXD,CER DI:0.22UF,10%,50V	05397	C330C224K5R5CA
A5C964	283-0398-00			CAP,FXD,CER DI:680PF,2%,100V	04222	3429100A681G
A5C965	283-0398-00			CAP,FXD,CER DI:680PF,2%,100V	04222	3429100A681G
A5C966	283-0144-00			CAP,FXD,CER DI:33PF,2%,500V	59660	801-547P2G330G
A5C967	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C1000	281-0221-00			CAP,VAR,CER DI:2-10PF,100V	72982	0513013A 2 0-10
A5C1001	283-0260-00			CAP,FXD,CER DI:5.6PF,+/-0.25PF,200V	51642	150 200NP0569C
A5C1002	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A5C1015	283-0260-00			CAP,FXD,CER DI:5.6PF,+/-0.25PF,200V	51642	150 200NP0569C
A5C1016	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A5C1020	281-0221-00			CAP,VAR,CER DI:2-10PF,100V	72982	0513013A 2 0-10
A5C1021	281-0158-00			CAP,VAR,CER DI:7-45PF,100WVDC SUBMIN	59660	518-006 G 7-45
A5C1031	281-0221-00			CAP,VAR,CER DI:2-10PF,100V	72982	0513013A 2 0-10
A5C1050	281-0221-00			CAP,VAR,CER DI:2-10PF,100V	72982	0513013A 2 0-10
A5C1100	281-0158-00			CAP,VAR,CER DI:7-45PF,100WVDC SUBMIN	59660	518-006 G 7-45
A5C1110	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C1111	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C1120	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C1121	283-0260-00			CAP,FXD,CER DI:5.6PF,+/-0.25PF,200V	51642	150 200NP0569C
A5C1122	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A5C1130	281-0158-00			CAP,VAR,CER DI:7-45PF,100WVDC SUBMIN	59660	518-006 G 7-45
A5C1140	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C1141	283-0260-00			CAP,FXD,CER DI:5.6PF,+/-0.25PF,200V	51642	150 200NP0569C
A5C1142	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5C1150	281-0158-00			CAP,VAR,CER DI:7-45PF,100WVDC SUBMIN	59660	518-006 G 7-45
A5C1160	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5CR100	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR101	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR102	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR103	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR104	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR110	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR111	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR112	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR113	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR114	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR900	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR910	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR920	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR930	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR940	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR941	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR950	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR961	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5DL600	119-1531-00			DELAY LINE,ELEC:17.5MS,150 OHM	80009	119-1531-00
A5DL640	119-1531-00			DELAY LINE,ELEC:17.5MS,150 OHM	80009	119-1531-00
A5J1100	136-0263-07			SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
A5J1110	136-0263-07			SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
A5J1120	136-0263-07			SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
A5J1121	136-0263-07			SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
A5J1140	136-0263-07			SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
A5J1141	136-0263-07			SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
A5J1150	136-0263-07			SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
A5J1160	136-0263-07			SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
A5L120	108-0245-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A5L121	108-0549-00			COIL,RF:FIXED,4.45UF	TK1345	108-0549-00
A5L220	108-0245-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A5L260	108-0422-00			COIL,RF:FIXED,80UH	80009	108-0422-00
A5L420	108-0422-00			COIL,RF:FIXED,80UH	80009	108-0422-00
A5P230	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 3)	22526	48283-029
A5P320	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 20)	22526	48283-036
A5P420	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 6)	22526	48283-036
A5P500	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 26)	22526	48283-036
A5P560	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 3)	22526	48283-036
A5Q100	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A5Q130	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A5Q131	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A5Q210	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A5Q600	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q660	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q700	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q730	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q731	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q732	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q733	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q760	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5R110	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A5R111	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5R112	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A5R120	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A5R121	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A5R130	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A5R131	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A5R132	321-0132-00			RES,FXD,FILM:232 OHM,1%,0.125W,TC=T0	19701	5043ED232R0F
A5R133	321-0225-00			RES,FXD,FILM:2.15K OHM,1%,0.125W,TC=T0	19701	5033ED2K15F
A5R134	321-0225-00			RES,FXD,FILM:2.15K OHM,1%,0.125W,TC=T0	19701	5033ED2K15F
A5R135	315-0680-00			RES,FXD,FILM:68 OHM,5%,0.25W	57668	NTR25J-E68E0
A5R141	317-0221-00			RES,FXD,CMPSN:220 OHM,5%,0.125W	01121	BB2215
A5R142	311-1832-00			RES,VAR,NONWW:PNL,5K OHM,10%,0.375W	01121	73M4G040L502A
A5R150	321-0132-00			RES,FXD,FILM:232 OHM,1%,0.125W,TC=T0	19701	5043ED232R0F
A5R151	317-0221-00			RES,FXD,CMPSN:220 OHM,5%,0.125W	01121	BB2215
A5R200	321-0287-00			RES,FXD,FILM:9.53K OHM,1%,0.125W,TC=T0	19701	5033ED9K530F
A5R201	321-0287-00			RES,FXD,FILM:9.53K OHM,1%,0.125W,TC=T0	19701	5033ED9K530F
A5R202	321-0297-00			RES,FXD,FILM:12.1K OHM,1%,0.125W,TC=T0	07716	CEAD12101F
A5R203	321-0297-00			RES,FXD,FILM:12.1K OHM,1%,0.125W,TC=T0	07716	CEAD12101F
A5R204	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A5R205	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A5R210	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A5R211	321-0297-00			RES,FXD,FILM:12.1K OHM,1%,0.125W,TC=T0	07716	CEAD12101F
A5R212	321-0297-00			RES,FXD,FILM:12.1K OHM,1%,0.125W,TC=T0	07716	CEAD12101F
A5R213	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A5R220	321-0287-00			RES,FXD,FILM:9.53K OHM,1%,0.125W,TC=T0	19701	5033ED9K530F
A5R221	321-0287-00			RES,FXD,FILM:9.53K OHM,1%,0.125W,TC=T0	19701	5033ED9K530F
A5R230	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A5R231	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A5R232	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A5R233	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A5R300	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A5R301	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A5R310	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A5R320	311-1757-00			RES,VAR,NONWW:2.5K OHM 10%,.5W LIN,CERMET	73138	82PR2.5K-124C
A5R321	311-1757-00			RES,VAR,NONWW:2.5K OHM 10%,.5W LIN,CERMET	73138	82PR2.5K-124C
A5R322	311-1757-00			RES,VAR,NONWW:2.5K OHM 10%,.5W LIN,CERMET	73138	82PR2.5K-124C
A5R323	311-1757-00			RES,VAR,NONWW:2.5K OHM 10%,.5W LIN,CERMET	73138	82PR2.5K-124C
A5R400	321-0614-00			RES,FXD,FILM:10.1K OHM,1%,0.125W,TC=T0	19701	5043ED10K10F
A5R401	321-0297-00			RES,FXD,FILM:12.1K OHM,1%,0.125W,TC=T0	07716	CEAD12101F
A5R402	321-0614-00			RES,FXD,FILM:10.1K OHM,1%,0.125W,TC=T0	19701	5043ED10K10F
A5R403	321-0297-00			RES,FXD,FILM:12.1K OHM,1%,0.125W,TC=T0	07716	CEAD12101F
A5R410	321-0297-00			RES,FXD,FILM:12.1K OHM,1%,0.125W,TC=T0	07716	CEAD12101F
A5R411	321-0297-00			RES,FXD,FILM:12.1K OHM,1%,0.125W,TC=T0	07716	CEAD12101F
A5R420	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A5R421	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A5R422	321-0614-00			RES,FXD,FILM:10.1K OHM,1%,0.125W,TC=T0	19701	5043ED10K10F
A5R423	321-0614-00			RES,FXD,FILM:10.1K OHM,1%,0.125W,TC=T0	19701	5043ED10K10F
A5R450	321-0202-00			RES,FXD,FILM:1.24K OHM,1%,0.125W,TC=T0	24546	NA55D1241F
A5R451	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A5R452	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A5R453	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A5R460	311-0634-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329H-L58-501
A5R461	315-0751-00			RES,FXD,FILM:750 OHM,5%,0.25W	57668	NTR25J-E750E
A5R462	315-0751-00			RES,FXD,FILM:750 OHM,5%,0.25W	57668	NTR25J-E750E
A5R463	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A5R500	321-0614-00			RES,FXD,FILM:10.1K OHM,1%,0.125W,TC=T0	19701	5043ED10K10F
A5R501	321-0614-00			RES,FXD,FILM:10.1K OHM,1%,0.125W,TC=T0	19701	5043ED10K10F
A5R502	321-0300-00			RES,FXD,FILM:13.0K OHM,1%,0.125W,TC=T0	07716	CEAD13001F
A5R503	321-0266-00			RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5R504	321-0266-00			RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F
A5R510	321-0614-00			RES,FXD,FILM:10.1K OHM,1%,0.125W,TC=T0	19701	5043ED10K10F
A5R511	321-0614-00			RES,FXD,FILM:10.1K OHM,1%,0.125W,TC=T0	19701	5043ED10K10F
A5R530	321-0300-00			RES,FXD,FILM:13.0K OHM,1%,0.125W,TC=T0	07716	CEAD13001F
A5R531	321-0300-00			RES,FXD,FILM:13.0K OHM,1%,0.125W,TC=T0	07716	CEAD13001F
A5R532	321-0300-00			RES,FXD,FILM:13.0K OHM,1%,0.125W,TC=T0	07716	CEAD13001F
A5R533	321-0266-00			RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F
A5R534	321-0266-00			RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F
A5R535	321-0266-00			RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F
A5R540	321-0187-00			RES,FXD,FILM:866 OHM,1%,0.125W,TC=T0	07716	CEAD866R0F
A5R541	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A5R542	321-0187-00			RES,FXD,FILM:866 OHM,1%,0.125W,TC=T0	07716	CEAD866R0F
A5R555	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R556	321-0187-00			RES,FXD,FILM:866 OHM,1%,0.125W,TC=T0	07716	CEAD866R0F
A5R560	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A5R561	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A5R562	315-0620-00	B010100	B010624	RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A5R562	315-0270-00	B010625		RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A5R562	315-0300-00	B010625		RES,FXD,FILM:30 OHM,5%,0.25W	19701	5043CX30R00J
A5R562	315-0360-00	B010625		RES,FXD,FILM:36 OHM,5%,0.25W	19701	5043CX36R00J
A5R562	315-0430-00	B010625		RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A5R562	315-0470-00	B010625		RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A5R562	315-0560-00	B010625		RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A5R562	315-0620-00	B010625		RES,FXD,FILM:62 OHM,5%,0.25W (A5R562 IS TEST SELECTED)	19701	5043CX63R00J
A5R564	315-0620-00	B010100	B010624	RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A5R564	315-0270-00	B010625		RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A5R564	315-0300-00	B010625		RES,FXD,FILM:30 OHM,5%,0.25W	19701	5043CX30R00J
A5R564	315-0360-00	B010625		RES,FXD,FILM:36 OHM,5%,0.25W	19701	5043CX36R00J
A5R564	315-0430-00	B010625		RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A5R564	315-0470-00	B010625		RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A5R564	315-0560-00	B010625		RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A5R564	315-0620-00	B010625		RES,FXD,FILM:62 OHM,5%,0.25W (A5R564 IS TEST SELECTED)	19701	5043CX63R00J
A5R600	321-0187-00			RES,FXD,FILM:866 OHM,1%,0.125W,TC=T0	07716	CEAD866R0F
A5R601	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A5R602	321-0187-00			RES,FXD,FILM:866 OHM,1%,0.125W,TC=T0	07716	CEAD866R0F
A5R603	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R604	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R620	321-0202-00			RES,FXD,FILM:1.24K OHM,1%,0.125W,TC=T0	24546	NA55D1241F
A5R630	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R631	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R632	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R633	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R634	321-0266-00			RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F
A5R635	321-0266-00			RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F
A5R636	321-0266-00			RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F
A5R640	321-0187-00			RES,FXD,FILM:866 OHM,1%,0.125W,TC=T0	07716	CEAD866R0F
A5R641	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A5R642	321-0187-00			RES,FXD,FILM:866 OHM,1%,0.125W,TC=T0	07716	CEAD866R0F
A5R650	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A5R651	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R652	321-0187-00			RES,FXD,FILM:866 OHM,1%,0.125W,TC=T0	07716	CEAD866R0F
A5R660	321-0202-00			RES,FXD,FILM:1.24K OHM,1%,0.125W,TC=T0	24546	NA55D1241F
A5R700	311-0607-00			RES,VAR,NONWW:TRMR,10K OHM,0.5W	73138	82-25-2
A5R701	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A5R730	311-0607-00			RES,VAR,NONWW:TRMR,10K OHM,0.5W	73138	82-25-2
A5R760	315-0272-00	B010100	B010199	RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A5R760	315-0512-00	B010200	B010853	RES,FXD,FILM:5.1K OHM,5%,0.25W (TEST SELECTABLE)	57668	NTR25J-E05K1

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5R760	315-0272-00	B010854		RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A5R761	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A5R762	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A5R800	315-0272-00	B010100	B010199	RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A5R800	315-0512-00	B010200	B010853	RES,FXD,FILM:5.1K OHM,5%,0.25W (TEST SELECTABLE)	57668	NTR25J-E05K1
A5R800	315-0272-00	B010854		RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A5R830	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A5R831	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A5R832	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A5R833	315-0272-00	B010100	B010199	RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A5R833	315-0512-00	B010200	B010853	RES,FXD,FILM:5.1K OHM,5%,0.25W (TEST SELECTABLE)	57668	NTR25J-E05K1
A5R833	315-0272-00	B010854		RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A5R834	315-0272-00	B010100	B010199	RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A5R834	315-0512-00	B010200	B010853	RES,FXD,FILM:5.1K OHM,5%,0.25W (TEST SELECTABLE)	57668	NTR25J-E05K1
A5R834	315-0272-00	B010854		RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A5R900	307-0831-00			RES NTWK,FXD,FI:H1122	80009	307-0831-00
A5R901	311-0607-00			RES,VAR,NONWW:TRMR,10K OHM,0.5W	73138	82-25-2
A5R902	311-0609-00			RES,VAR,NONWW:TRMR,2K OHM,0.5W	32997	3329H-L58-202
A5R903	311-0635-00			RES,VAR,NONWW:TRMR,1K OHM,0.5W	32997	3329H-G48-102
A5R910	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R911	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R912	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A5R913	307-0831-00			RES NTWK,FXD,FI:H1122	80009	307-0831-00
A5R916	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A5R920	311-0607-00			RES,VAR,NONWW:TRMR,10K OHM,0.5W	73138	82-25-2
A5R921	311-0609-00			RES,VAR,NONWW:TRMR,2K OHM,0.5W	32997	3329H-L58-202
A5R922	311-0635-00			RES,VAR,NONWW:TRMR,1K OHM,0.5W	32997	3329H-G48-102
A5R923	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R930	307-0831-00			RES NTWK,FXD,FI:H1122	80009	307-0831-00
A5R931	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R932	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A5R933	311-0607-00			RES,VAR,NONWW:TRMR,10K OHM,0.5W	73138	82-25-2
A5R934	311-0609-00			RES,VAR,NONWW:TRMR,2K OHM,0.5W	32997	3329H-L58-202
A5R935	311-0635-00			RES,VAR,NONWW:TRMR,1K OHM,0.5W	32997	3329H-G48-102
A5R940	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R941	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R942	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A5R950	307-0831-00			RES NTWK,FXD,FI:H1122	80009	307-0831-00
A5R951	311-0607-00			RES,VAR,NONWW:TRMR,10K OHM,0.5W	73138	82-25-2
A5R952	311-0609-00			RES,VAR,NONWW:TRMR,2K OHM,0.5W	32997	3329H-L58-202
A5R953	311-0635-00			RES,VAR,NONWW:TRMR,1K OHM,0.5W	32997	3329H-G48-102
A5R960	307-0831-00			RES NTWK,FXD,FI:H1122	80009	307-0831-00
A5R961	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R962	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R963	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A5R1000	311-0634-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329H-L58-501
A5R1001	317-0510-00			RES,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A5R1002	317-0102-00			RES,FXD,CMPSN:1K OHM,5%,0125W	01121	BB1025
A5R1010	311-0633-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3329H-G48-502
A5R1011	325-0044-00	B010100	B010159	RES,FXD,FILM:100 OHM,0.5%,0.05W,TC=150PPM	91637	CMF50G100R0D
A5R1011	321-0097-03	B010160		RES,FXD,FILM:100 OHM,0.25%,0.125W,TC=T0	91637	CMF55116D100R0C
A5R1015	317-0510-00			RES,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A5R1016	317-0102-00			RES,FXD,CMPSN:1K OHM,5%,0125W	01121	BB1025
A5R1020	311-0634-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329H-L58-501

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5R1021	325-0044-00	B010100	B010159	RES,FXD,FILM:100 OHM,0.5%,0.05W,TC=150PPM	91637	CMF50G100R0D
A5R1021	321-0097-03	B010160		RES,FXD,FILM:100 OHM,0.25%,0.125W,TC=T0	91637	CMF55116D100R0C
A5R1030	311-0633-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3329H-G48-502
A5R1031	311-0634-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329H-L58-501
A5R1040	311-0633-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3329H-G48-502
A5R1041	325-0044-00	B010100	B010159	RES,FXD,FILM:100 OHM,0.5%,0.05W,TC=150PPM	91637	CMF50G100R0D
A5R1041	321-0097-03	B010160		RES,FXD,FILM:100 OHM,0.25%,0.125W,TC=T0	91637	CMF55116D100R0C
A5R1050	311-0634-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329H-L58-501
A5R1060	311-0633-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3329H-G48-502
A5R1061	325-0044-00	B010100	B010159	RES,FXD,FILM:100 OHM,0.5%,0.05W,TC=150PPM	91637	CMF50G100R0D
A5R1061	321-0097-03	B010160		RES,FXD,FILM:100 OHM,0.25%,0.125W,TC=T0	91637	CMF55116D100R0C
A5R1110	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25W	19701	5043CX200K0J
A5R1120	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25W	19701	5043CX200K0J
A5R1121	317-0510-00			RES,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A5R1122	317-0102-00			RES,FXD,CMPSN:1K OHM,5%,0125W	01121	BB1025
A5R1140	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25W	19701	5043CX200K0J
A5R1141	317-0510-00			RES,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A5R1142	317-0102-00			RES,FXD,CMPSN:1K OHM,5%,0125W	01121	BB1025
A5R1160	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25W	19701	5043CX200K0J
A5T800	120-0444-00			XFMR,TOROID:	80009	120-0444-00
A5T833	120-0444-00			XFMR,TOROID:	80009	120-0444-00
A5T860	120-0444-00			XFMR,TOROID:	80009	120-0444-00
A5T930	120-0444-00			XFMR,TOROID:	80009	120-0444-00
A5T1110	120-0286-00			XFMR,TOROID:	80009	120-0286-00
A5T1120	120-0286-00			XFMR,TOROID:	80009	120-0286-00
A5T1140	120-0286-00			XFMR,TOROID:	80009	120-0286-00
A5T1160	120-0286-00			XFMR,TOROID:	80009	120-0286-00
A5TP200	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (A5TP200-1 THRU A5TP200-5)	22526	48283-029
A5TP400	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (A5TP400-1 THRU A5TP400-5)	22526	48283-029
A5U240	155-0236-00			MICROCKT,LINEAR:VERTICAL CHANNEL SWITCH	80009	155-0236-00
A5U300	156-0495-02			MICROCKT,LINEAR:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A5U310	156-0495-02			MICROCKT,LINEAR:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A5U600	155-0236-00			MICROCKT,LINEAR:VERTICAL CHANNEL SWITCH	80009	155-0236-00
A5U640	155-0236-00			MICROCKT,LINEAR:VERTICAL CHANNEL SWITCH	80009	155-0236-00
A5U1010	155-0078-10			MICROCKT,LINEAR:VERTICAL AMPLIFIER ML	80009	155-0078-10
A5U1020	155-0078-10			MICROCKT,LINEAR:VERTICAL AMPLIFIER ML	80009	155-0078-10
A5U1040	155-0078-10			MICROCKT,LINEAR:VERTICAL AMPLIFIER ML	80009	155-0078-10
A5U1060	155-0078-10			MICROCKT,LINEAR:VERTICAL AMPLIFIER ML	80009	155-0078-10
A6	672-1100-00			CIRCUIT BD ASSY:TRIGGER (NO LONGER AVAILABLE)	80009	672-1100-00
A6A1	670-7441-00	B010100	B010624	CIRCUIT BD ASSY:TRIGGER	80009	670-7441-00
A6A1	670-7441-01	B010625		CIRCUIT BD ASSY:TRIGGER	80009	670-7441-01
A6A1C103	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C110	290-0755-00			CAP,FXD,ELCTLT:100UF,+50%-20%,10WVDC	54473	ECE-A10V100L
A6A1C111	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C120	290-0755-00			CAP,FXD,ELCTLT:100UF,+50%-20%,10WVDC	54473	ECE-A10V100L
A6A1C121	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C130	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C200	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C202	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C210	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C212	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C213	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C220	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A6A1C222	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C223	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C230	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C232	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C233	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C234	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C300	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C301	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C330	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C331	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C400	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C411	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C430	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C500	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C501	281-0788-00			CAP,FXD,CER DI:470PF,10%,100V	04222	SA101C471KAA
A6A1C521	281-0788-00			CAP,FXD,CER DI:470PF,10%,100V	04222	SA101C471KAA
A6A1C530	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C600	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C602	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C630	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C631	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	MA101A100KAA
A6A1C632	283-0330-00			CAP,FXD,CER DI:100PF,5%,50V (SELECTED. MAY NOT BE REQUIRED)	05397	C320C101J5R5CA
A6A1C700	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C701	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C710	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C711	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C712	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A6A1C720	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	MA101A100KAA
A6A1C721	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C722	290-0755-00			CAP,FXD,ELCTLT:100UF,+50%-20%,10WVDC	54473	ECE-A10V100L
A6A1C726	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A6A1C800	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C830	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C900	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6A1C901	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C910	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C1020	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1C1021	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6A1CR520	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR521	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR620	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR622	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR720	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR721	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR722	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR723	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR730	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1CR731	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A6A1J602	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A6A1J634	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 3)	22526	48283-036
A6A1J700	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A6A1J701	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 3)	22526	48283-036
A6A1P200	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 3)	22526	48283-029
A6A1P210	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 3)	22526	48283-029

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A6A1P220	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 3)	22526	48283-029
A6A1P230	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 3)	22526	48283-029
A6A1P600	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 3)	22526	48283-036
A6A1P610	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 3)	22526	48283-036
A6A1P630	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 3)	22526	48283-029
A6A1P632	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A6A1Q532	156-0197-00			MICROCKT,LINEAR:5-TRANSISTOR ARRAY	02735	CA3086
A6A1Q600	151-0221-05			TRANSISTOR:SCREENED	TK0271	151-0221-05
A6A1Q610	151-0221-05			TRANSISTOR:SCREENED	TK0271	151-0221-05
A6A1Q620	151-0220-03			TRANSISTOR:PNP,SI,TO-92	04713	SPS6915
A6A1Q622	151-0220-03			TRANSISTOR:PNP,SI,TO-92	04713	SPS6915
A6A1Q720	151-0220-03			TRANSISTOR:PNP,SI,TO-92	04713	SPS6915
A6A1Q722	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A6A1Q724	151-0220-03			TRANSISTOR:PNP,SI,TO-92	04713	SPS6915
A6A1Q726	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A6A1Q1000	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A6A1Q1002	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A6A1Q1004	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A6A1Q1010	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A6A1Q1012	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A6A1Q1014	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A6A1R100	321-0185-00			RES,FXD,FILM:825 OHM,1%,0.125W,TC=T0	07716	CEAD825R0F
A6A1R101	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6A1R102	321-0295-00			RES,FXD,FILM:11.5K OHM,1%,0.125W,TC=T0	07716	CEAD11501F
A6A1R103	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A6A1R111	321-0185-00			RES,FXD,FILM:825 OHM,1%,0.125W,TC=T0	07716	CEAD825R0F
A6A1R112	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6A1R113	321-0295-00			RES,FXD,FILM:11.5K OHM,1%,0.125W,TC=T0	07716	CEAD11501F
A6A1R114	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A6A1R120	321-0185-00			RES,FXD,FILM:825 OHM,1%,0.125W,TC=T0	07716	CEAD825R0F
A6A1R121	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6A1R122	321-0295-00			RES,FXD,FILM:11.5K OHM,1%,0.125W,TC=T0	07716	CEAD11501F
A6A1R123	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A6A1R130	321-0185-00			RES,FXD,FILM:825 OHM,1%,0.125W,TC=T0	07716	CEAD825R0F
A6A1R131	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6A1R132	321-0295-00			RES,FXD,FILM:11.5K OHM,1%,0.125W,TC=T0	07716	CEAD11501F
A6A1R133	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A6A1R200	307-0707-00			RES NTWK,FXD,FI:4,4.7K OHM,2%,0.2W EA	01121	108B472
A6A1R201	307-0707-00			RES NTWK,FXD,FI:4,4.7K OHM,2%,0.2W EA	01121	108B472
A6A1R202	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A6A1R203	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R204	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R210	321-0327-00			RES,FXD,FILM:24.9K OHM,1%,0.125W,TC=T0	07716	CEAD24901F
A6A1R211	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R212	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R220	321-0327-00			RES,FXD,FILM:24.9K OHM,1%,0.125W,TC=T0	07716	CEAD24901F
A6A1R221	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R222	321-0327-00			RES,FXD,FILM:24.9K OHM,1%,0.125W,TC=T0	07716	CEAD24901F
A6A1R224	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R230	321-0327-00			RES,FXD,FILM:24.9K OHM,1%,0.125W,TC=T0	07716	CEAD24901F
A6A1R231	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R232	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R233	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A6A1R234	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A6A1R300	311-1917-00			RES,VAR,NONWW:TRMR,5K OHM,10%,0.5 W	32997	3386C-T07-502
A6A1R301	311-1917-00			RES,VAR,NONWW:TRMR,5K OHM,10%,0.5 W	32997	3386C-T07-502
A6A1R302	311-1138-00			RES,VAR,NONWW:TRMR,1K OHM,0.5W	32997	3386J-T07-102
A6A1R303	311-1138-00			RES,VAR,NONWW:TRMR,1K OHM,0.5W	32997	3386J-T07-102
A6A1R400	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A6A1R401	311-1917-00			RES,VAR,NONWW:TRMR,5K OHM,10%,0.5 W	32997	3386C-T07-502
A6A1R402	311-1138-00			RES,VAR,NONWW:TRMR,1K OHM,0.5W	32997	3386J-T07-102
A6A1R403	311-1138-00			RES,VAR,NONWW:TRMR,1K OHM,0.5W	32997	3386J-T07-102
A6A1R404	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A6A1R405	311-1917-00			RES,VAR,NONWW:TRMR,5K OHM,10%,0.5 W	32997	3386C-T07-502
A6A1R406	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A6A1R410	307-0486-00			RES NTWK,FXD,FI:100 OHM,20%,1.125W	11236	750-101-R100 OHM
A6A1R411	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A6A1R420	307-0486-00			RES NTWK,FXD,FI:100 OHM,20%,1.125W	11236	750-101-R100 OHM
A6A1R421	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A6A1R430	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A6A1R431	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A6A1R432	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A6A1R500	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A6A1R501	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A6A1R502	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A6A1R505	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A6A1R510	307-0486-00			RES NTWK,FXD,FI:100 OHM,20%,1.125W	11236	750-101-R100 OHM
A6A1R511	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R512	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6A1R513	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A6A1R514	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A6A1R515	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A6A1R516	307-0108-00			RES,FXD,CMPSN:6.8 OHM,5%,0.25W	01121	CB68G5
A6A1R517	307-0108-00			RES,FXD,CMPSN:6.8 OHM,5%,0.25W	01121	CB68G5
A6A1R520	307-0486-00			RES NTWK,FXD,FI:100 OHM,20%,1.125W	11236	750-101-R100 OHM
A6A1R521	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A6A1R522	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A6A1R525	317-0101-00			RES,FXD,CMPSN:100 OHM,5%,0.125W	01121	BB1015
A6A1R530	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A6A1R600	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A6A1R601	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A6A1R610	307-0486-00			RES NTWK,FXD,FI:100 OHM,20%,1.125W	11236	750-101-R100 OHM
A6A1R611	315-0220-00			RES,FXD,FILM:22 OHM,5%,0.25W	19701	5043CX22R00J
A6A1R620	307-0486-00			RES NTWK,FXD,FI:100 OHM,20%,1.125W	11236	750-101-R100 OHM
A6A1R621	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A6A1R622	315-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A6A1R623	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A6A1R630	315-0822-00	B010100	B010624	RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A6A1R630	315-0822-03	B010625		RES,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A6A1R631	315-0822-00	B010100	B010624	RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A6A1R631	315-0822-03	B010625		RES,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A6A1R632	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A6A1R633	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A6A1R700	307-0486-00			RES NTWK,FXD,FI:100 OHM,20%,1.125W	11236	750-101-R100 OHM
A6A1R702	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A6A1R705	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A6A1R706	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A6A1R707	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A6A1R708	315-0271-00			RES,FXD,FILM:270 OHM,5%,0.25W	57668	NTR25J-E270E
A6A1R709	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A6A1R710	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A6A1R711	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A6A1R712	315-0271-00			RES,FXD,FILM:270 OHM,5%,0.25W	57668	NTR25J-E270E
A6A1R713	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A6A1R714	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A6A1R715	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A6A1R716	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A6A1R720	315-0243-00			RES,FXD,FILM:24K OHM,5%,0.25W	57668	NTR25J-E24K0
A6A1R721	315-0430-00			RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A6A1R722	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A6A1R723	315-0271-00			RES,FXD,FILM:270 OHM,5%,0.25W	57668	NTR25J-E270E
A6A1R724	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A6A1R725	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A6A1R726	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A6A1R727	321-0238-00			RES,FXD,FILM:2.94K OHM,1%,0.125W,TC=T0	07716	CEAD29400F
A6A1R728	321-0229-00			RES,FXD,FILM:2.37K OHM,1%,0.125W,TC=T0	19701	5043ED2K37F
A6A1R729	321-0248-00			RES,FXD,FILM:3.74K OHM,1%,0.125W,TC=T0	19701	5043ED3K740F
A6A1R730	307-1096-00			RES NTWK,FXD,FI:7,2K OHM,2 %,1 W,TC-2	11236	750-81-R2K
A6A1R731	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A6A1R732	307-0856-00			RES NTWK,FXD,FI:(8) 2.7K OHM,2%,0.125W EA	01121	316B272
A6A1R733	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A6A1R734	321-0114-00			RES,FXD,FILM:150 OHM,1%,0.125 W,TC=T0	19701	5033ED150R0F
A6A1R735	321-0114-00			RES,FXD,FILM:150 OHM,1%,0.125 W,TC=T0	19701	5033ED150R0F
A6A1R736	315-0120-00			RES,FXD,FILM:12 OHM,5%,0.25W	57668	NTR25J-R12
A6A1R806	307-0675-00			RES NTWK,FXD,FI:9,1K OHM,2%1.25W	11236	750-101-R1K OHM
A6A1R808	307-0856-00			RES NTWK,FXD,FI:(8) 2.7K OHM,2%,0.125W EA	01121	316B272
A6A1R810	307-1096-00			RES NTWK,FXD,FI:7,2K OHM,2 %,1 W,TC-2	11236	750-81-R2K
A6A1R812	307-1096-00			RES NTWK,FXD,FI:7,2K OHM,2 %,1 W,TC-2	11236	750-81-R2K
A6A1R814	307-0856-00			RES NTWK,FXD,FI:(8) 2.7K OHM,2%,0.125W EA	01121	316B272
A6A1R816	307-0675-00			RES NTWK,FXD,FI:9,1K OHM,2%1.25W	11236	750-101-R1K OHM
A6A1R820	307-1096-00			RES NTWK,FXD,FI:7,2K OHM,2 %,1 W,TC-2	11236	750-81-R2K
A6A1R822	307-1096-00			RES NTWK,FXD,FI:7,2K OHM,2 %,1 W,TC-2	11236	750-81-R2K
A6A1R824	307-0856-00			RES NTWK,FXD,FI:(8) 2.7K OHM,2%,0.125W EA	01121	316B272
A6A1R826	307-0675-00			RES NTWK,FXD,FI:9,1K OHM,2%1.25W	11236	750-101-R1K OHM
A6A1R834	307-0856-00			RES NTWK,FXD,FI:(8) 2.7K OHM,2%,0.125W EA	01121	316B272
A6A1R900	307-1096-00			RES NTWK,FXD,FI:7,2K OHM,2 %,1 W,TC-2	11236	750-81-R2K
A6A1R901	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A6A1R902	307-0856-00			RES NTWK,FXD,FI:(8) 2.7K OHM,2%,0.125W EA	01121	316B272
A6A1R903	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A6A1R904	307-1096-00			RES NTWK,FXD,FI:7,2K OHM,2 %,1 W,TC-2	11236	750-81-R2K
A6A1R910	307-0675-00			RES NTWK,FXD,FI:9,1K OHM,2%1.25W	11236	750-101-R1K OHM
A6A1R914	307-0675-00			RES NTWK,FXD,FI:9,1K OHM,2%1.25W	11236	750-101-R1K OHM
A6A1R930	307-0675-00			RES NTWK,FXD,FI:9,1K OHM,2%1.25W	11236	750-101-R1K OHM
A6A1R932	321-0114-00			RES,FXD,FILM:150 OHM,1%,0.125 W,TC=T0	19701	5033ED150R0F
A6A1R1000	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W	19701	5043CX1K100J
A6A1R1001	315-0361-00			RES,FXD,FILM:360 OHM,5%,0.25W	19701	5043CX360R0J
A6A1R1002	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6A1R1003	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W	19701	5043CX1K100J
A6A1R1004	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A6A1R1005	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A6A1R1010	315-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.25W	19701	5043CX1K600J
A6A1R1011	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A6A1R1012	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A6A1R1013	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A6A1R1014	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A6A1R1030	321-0114-00			RES,FXD,FILM:150 OHM,1%,0.125 W,TC=T0	19701	5033ED150R0F
A6A1TP800	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP801	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP802	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A6A1TP803	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP804	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP900	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP1000	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP1001	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP1002	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP1003	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1TP1004	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A6A1U200	156-1344-00			MICROCKT,LINEAR:ECL,COMPARATOR	24355	AD9685BH
A6A1U210	156-1344-00			MICROCKT,LINEAR:ECL,COMPARATOR	24355	AD9685BH
A6A1U220	156-1344-00			MICROCKT,LINEAR:ECL,COMPARATOR	24355	AD9685BH
A6A1U230	156-1344-00			MICROCKT,LINEAR:ECL,COMPARATOR	24355	AD9685BH
A6A1U300	156-1674-00			MICROCKT,DGTL:SCREENED	04713	MC10H104LD
A6A1U302	156-1674-00			MICROCKT,DGTL:SCREENED	04713	MC10H104LD
A6A1U310	156-1667-00			MICROCKT,DGTL:SCREENED	04713	MC10H164LD
A6A1U312	156-1667-00			MICROCKT,DGTL:SCREENED	04713	MC10H164LD
A6A1U320	156-1667-00			MICROCKT,DGTL:SCREENED	04713	MC10H164LD
A6A1U322	156-1667-00			MICROCKT,DGTL:SCREENED	04713	MC10H164LD
A6A1U330	156-1674-00			MICROCKT,DGTL:SCREENED	04713	MC10H104LD
A6A1U332	156-1674-00			MICROCKT,DGTL:SCREENED	04713	MC10H104LD
A6A1U400	156-0687-01			MICROCKT,DGTL:QUAD EXCL OR CMPTR	04713	MC10113PD/LD
A6A1U402	156-1641-01			MICROCKT,DGTL:SCREENED	04713	MC10H102(LDORPD)
A6A1U410	156-0687-01			MICROCKT,DGTL:QUAD EXCL OR CMPTR	04713	MC10113PD/LD
A6A1U412	156-1641-01			MICROCKT,DGTL:SCREENED	04713	MC10H102(LDORPD)
A6A1U420	156-0687-01			MICROCKT,DGTL:QUAD EXCL OR CMPTR	04713	MC10113PD/LD
A6A1U422	156-1641-01			MICROCKT,DGTL:SCREENED	04713	MC10H102(LDORPD)
A6A1U430	156-0687-01			MICROCKT,DGTL:QUAD EXCL OR CMPTR	04713	MC10113PD/LD
A6A1U432	156-1641-01			MICROCKT,DGTL:SCREENED	04713	MC10H102(LDORPD)
A6A1U500	156-1674-00			MICROCKT,DGTL:SCREENED	04713	MC10H104LD
A6A1U510	156-1641-01			MICROCKT,DGTL:SCREENED	04713	MC10H102(LDORPD)
A6A1U520	156-1641-01			MICROCKT,DGTL:SCREENED	04713	MC10H102(LDORPD)
A6A1U530	156-1674-00			MICROCKT,DGTL:SCREENED	04713	MC10H104LD
A6A1U600	156-1674-00			MICROCKT,DGTL:SCREENED	04713	MC10H104LD
A6A1U610	156-1674-00			MICROCKT,DGTL:SCREENED	04713	MC10H104LD
A6A1U620	156-1676-00			MICROCKT,DGTL:SCREENED	04713	MC10H107LD
A6A1U630	156-0632-02			MICROCKT,DGTL:QUAD 2 INPUT MUX/LATCH,SCRN	80009	156-0632-02
A6A1U700	156-0458-01			MICROCKT,DGTL:QUAD AND GATE 2 INP	04713	MC10104PD/LD
A6A1U800	156-0458-01			MICROCKT,DGTL:QUAD AND GATE 2 INP	04713	MC10104PD/LD
A6A1U818	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A6A1U828	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A6A1U838	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A6A1U912	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A6A1U922	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A6A1U932	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A6A1U1010	156-1327-00			MICROCKT,DGTL:CMOS,3 STATE OCTAL D FF,SCRN	27014	MM74C374NA+
A6A1U1020	156-1623-00			MICROCKT,LINEAR:D/A CONVERTER,8 BIT,VOLTAGE OUTPUT	24355	AD41201
A6A1U1022	156-1623-00			MICROCKT,LINEAR:D/A CONVERTER,8 BIT,VOLTAGE OUTPUT	24355	AD41201
A6A1U1030	156-1623-00			MICROCKT,LINEAR:D/A CONVERTER,8 BIT,VOLTAGE OUTPUT	24355	AD41201
A6A1U1032	156-1623-00			MICROCKT,LINEAR:D/A CONVERTER,8 BIT,VOLTAGE OUTPUT	24355	AD41201
A6A1VR700	152-0279-00	B010100	B010199	SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	14552	TD3810989
A6A1VR700	152-0195-00	B010200		SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A6A1VR710	152-0279-00	B010100	B010199	SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	14552	TD3810989
A6A1VR710	152-0195-00	B010200		SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A6A1W612	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A6A1W620	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A6A1W700	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A6A1W701	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A6A2	670-7940-00			CIRCUIT BD ASSY:TRIGGER SHIELD 388-8268-XX (NO ELECTRICAL PARTS)	80009	670-7940-00
A6A3	670-7941-00			CIRCUIT BD ASSY:TRIGGER SHIELD (NO ELECTRICAL PARTS)	80009	670-7941-00
A7	670-7442-00			CIRCUIT BD ASSY:DIGITAL	80009	670-7442-00
A7C120	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-20 %,10V	55680	ULA1A220TAA
A7C200	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A7C230	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7C231	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7C310	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C325	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C330	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7C331	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7C410	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C411	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C420	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C421	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C520	290-0846-00			CAP,FXD,ELCTLT:47UF,+75-20%,35V	54473	ECE-A35V47LU
A7C521	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C525	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A7C526	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A7C610	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C611	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A7C710	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C730	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A7C731	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A7C800	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C802	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V TUBULAR,MI	04222	MA101A100MAA
A7C810	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C825	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A7C829	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	SA106E222MAA
A7C830	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C910	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7C912	281-0816-00			CAP,FXD,CER DI:82 PF,5%,100V	04222	MA106A820JAA
A7C925	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-20%,10V	55680	ULB1A221TPAANA
A7C926	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7C1030	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A7CR230	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7CR231	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7CR520	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7CR521	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7CR530	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7CR630	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7CR810	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7CR811	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7J401	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A7J730	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A7P1010	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 20)	22526	48283-036

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A7Q625	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A7Q626	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A7Q720	156-0048-02			MICROCKT,LINEAR:5 XSTR ARRAY,CHECKED	80009	156-0048-02
A7Q810	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A7Q811	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A7R200	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R201	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R202	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R203	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R204	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R205	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R206	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R230	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A7R231	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A7R232	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A7R233	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A7R234	321-0291-00	B010100	B010159	RES,FXD,FILM:10.5K OHM,1%,0.125W,TC=T0	19701	5033ED10K50F
A7R234	321-0296-00	B010160		RES,FXD,FILM:11.8K OHM,1%,0.125W,TC=T0	07716	CEAD11801F
A7R235	321-0777-00			RES,FXD,FILM:5.14K OHM,1%,0.125W,TC=T0	24546	NA55D5141F
A7R236	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A7R238	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R239	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R300	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R330	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R331	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7R332	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A7R333	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A7R430	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A7R431	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A7R520	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A7R521	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A7R530	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A7R600	315-0431-00	B010100	B010159	RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A7R600	315-0221-00	B010160		RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A7R620	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A7R622	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A7R623	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A7R624	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A7R625	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25W	19701	5043CX6K200J
A7R626	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25W	19701	5043CX6K200J
A7R627	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A7R628	307-0104-00			RES,FXD,CMPSN:3.3 OHM,5%,0.25W	01121	CB33G5
A7R629	307-0104-00			RES,FXD,CMPSN:3.3 OHM,5%,0.25W	01121	CB33G5
A7R720	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A7R721	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A7R722	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A7R725	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A7R726	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A7R728	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A7R729	315-0183-00			RES,FXD,FILM:18K OHM,5%,0.25W	19701	5043CX18K00J
A7R730	315-0183-00			RES,FXD,FILM:18K OHM,5%,0.25W	19701	5043CX18K00J
A7R800	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A7R801	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A7R802	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A7R805	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A7R806	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A7R807	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A7R811	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A7R820	321-0394-00			RES,FXD,FILM:124K OHM,1%,0.125W,TC=T0	07716	CEAD12402F
A7R821	321-0367-00			RES,FXD,FILM:64.9K OHM,1%,0.125W,TC=T0	07716	CEAD64901F
A7R822	321-0338-00			RES,FXD,FILM:32.4K OHM,1%,0.125W,TC=T0	19701	5033ED32K40F
A7R823	321-0309-00			RES,FXD,FILM:16.2K OHM,1%,0.125W,TC=T0	19701	5033ED16K20F
A7R824	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A7R825	315-0912-00			RES,FXD,FILM:9.1K OHM,5%,0.25W	57668	NTR25J-E09K1
A7R826	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25W	19701	5043CX6K200J
A7R827	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A7R828	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A7R829	315-0563-00			RES,FXD,FILM:56K OHM,5%,0.25W	19701	5043CX56K00J
A7R831	321-0394-00			RES,FXD,FILM:124K OHM,1%,0.125W,TC=T0	07716	CEAD12402F
A7R832	321-0367-00			RES,FXD,FILM:64.9K OHM,1%,0.125W,TC=T0	07716	CEAD64901F
A7R833	321-0338-00			RES,FXD,FILM:32.4K OHM,1%,0.125W,TC=T0	19701	5033ED32K40F
A7R834	321-0309-00			RES,FXD,FILM:16.2K OHM,1%,0.125W,TC=T0	19701	5033ED16K20F
A7R835	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A7R910	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A7R911	315-0113-00			RES,FXD,FILM:11K OHM,5%,0.25W	19701	5043CX11K00J
A7R912	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A7R920	321-0394-00			RES,FXD,FILM:124K OHM,1%,0.125W,TC=T0	07716	CEAD12402F
A7R921	321-0367-00			RES,FXD,FILM:64.9K OHM,1%,0.125W,TC=T0	07716	CEAD64901F
A7R922	321-0338-00			RES,FXD,FILM:32.4K OHM,1%,0.125W,TC=T0	19701	5033ED32K40F
A7R923	321-0309-00			RES,FXD,FILM:16.2K OHM,1%,0.125W,TC=T0	19701	5033ED16K20F
A7R930	321-0394-00			RES,FXD,FILM:124K OHM,1%,0.125W,TC=T0	07716	CEAD12402F
A7R931	321-0367-00			RES,FXD,FILM:64.9K OHM,1%,0.125W,TC=T0	07716	CEAD64901F
A7R932	321-0338-00			RES,FXD,FILM:32.4K OHM,1%,0.125W,TC=T0	19701	5033ED32K40F
A7R933	321-0309-00			RES,FXD,FILM:16.2K OHM,1%,0.125W,TC=T0	19701	5033ED16K20F
A7R934	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A7R1020	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A7TP100	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 9)	22526	48283-029
A7TP200	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 4)	22526	48283-029
A7TP300	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 9)	22526	48283-029
A7TP400	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY 5)	22526	48283-029
A7TP420	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 5)	22526	48283-036
A7TP520	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 4)	22526	48283-036
A7TP521	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 4)	22526	48283-036
A7TP620	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 5)	22526	48283-036
A7U110	156-1622-00			MICROCKT,DGTL:CMOS,8 DIGIT LED DRIVER SYS COMMON CATHODE	32293	ICM7218BIJI
A7U130	156-0411-02			MICROCKT,LINEAR:QUAD COMPARATOR,SCREENED	04713	LM339JDS
A7U300	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A7U320	156-1621-00			MICROCKT,DGTL:CMOS,8 DIGIT LED DRIVER	32293	ICM7218AIJI
A7U330	156-0206-02			MICROCKT,DGTL:CORE DRIVER,SCREENED	01295	SN75325(N OR J)
A7U400	156-0989-02			MICROCKT,DGTL:4 X 4 RGTR FILE W/3 STATE OUT	01295	SN74LS670NP3
A7U401	156-0989-02			MICROCKT,DGTL:4 X 4 RGTR FILE W/3 STATE OUT	01295	SN74LS670NP3
A7U420	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A7U421	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A7U430	156-0206-02			MICROCKT,DGTL:CORE DRIVER,SCREENED	01295	SN75325(N OR J)
A7U431	156-0206-02			MICROCKT,DGTL:CORE DRIVER,SCREENED	01295	SN75325(N OR J)
A7U500	156-1327-00			MICROCKT,DGTL:CMOS,3 STATE OCTAL D FF,SCRN	27014	MM74C374NA+
A7U520	156-0206-02			MICROCKT,DGTL:CORE DRIVER,SCREENED	01295	SN75325(N OR J)
A7U530	156-0058-02			MICROCKT,DGTL:HEX INV,SCRN	18324	N7404(NB OR FB)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A7U531	156-0206-02			MICROCKT,DGTL:CORE DRIVER,SCREENED	01295	SN75325(N OR J)
A7U600	156-0989-02			MICROCKT,DGTL:4 X 4 RGTR FILE W/3 STATE OUT	01295	SN74LS670NP3
A7U601	156-0989-02			MICROCKT,DGTL:4 X 4 RGTR FILE W/3 STATE OUT	01295	SN74LS670NP3
A7U630	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A7U700	156-1327-00			MICROCKT,DGTL:CMOS,3 STATE OCTAL D FF,SCRN	27014	MM74C374NA+
A7U730	156-0402-03			MICROCKT,LINEAR:TIMER,TESTED	27014	LM555CJ
A7U800	160-1714-00			MICROCKT,DGTL:HEX 16-INPUT REGISTERED &	80009	160-1714-00
A7U820	156-0644-02			MICROCKT,DGTL:CMOS,QUAD BILATERAL SWITCH	02735	CD4066BF
A7U830	156-0721-02			MICROCKT,DGTL:QUAD ST 2-INP NAND GATES	18324	N74LS132(NBORFB)
A7U900	156-0480-02			MICROCKT,DGTL:QUAD 2-INP & GATE,SCRN,	01295	SN74LS08NP3
A7U920	155-0038-01			MICROCKT,DGTL:D-A CONVERTER	80009	155-0038-01
A7U930	155-0038-01			MICROCKT,DGTL:D-A CONVERTER	80009	155-0038-01
A7U1020	155-0038-01			MICROCKT,DGTL:D-A CONVERTER	80009	155-0038-01
A7U1030	155-0038-01			MICROCKT,DGTL:D-A CONVERTER	80009	155-0038-01
A7Y630	119-1539-00			TRANSDUCER,AUD:4KHZ PIEZOELECTRIC	S4431	PKM24-4A0
A8	670-7443-00	B010100	B010825	CIRCUIT BD ASSY:MPU	80009	670-7443-00
A8	670-7443-01	B010826		CIRCUIT BD ASSY:MPU	80009	670-7443-01
A8BT650	146-0035-00			BATTERY,STORAGE:3.75V,0.1AH @ 20MA,(3)1/3 A CELLS,NICAD	09052	406349
A8C100	290-0845-00			CAP,FXD,ELCTLT:330UF,+50-10%,25V	54473	ECE-A25V330L
A8C115	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C145	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C230	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C245	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C305	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C320	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C335	281-0798-00			CAP,FXD,CER DI:51PF,1%,100V	04222	MA101A510GAA
A8C336	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A8C337	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-20 %,10V	55680	ULA1A220TAA
A8C340	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C405	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-10%,35VDC	55680	ULB1V4R7TAAANA
A8C500	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C505	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C513	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C535	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C600	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C615	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C635	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C700	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C710	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C735	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C755	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-10%,35VDC	55680	ULB1V4R7TAAANA
A8C810	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A8C815	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C840	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C900	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A8C912	283-0339-00			CAP,FXD,CER DI:0.22UF,10%,50V	05397	C330C224K5R5CA
A8C930	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAATR
A8C940	290-0107-00			CAP,FXD,ELCTLT:25UF,+75-10%,25V	00853	556DB250U025B
A8C945	290-0107-00			CAP,FXD,ELCTLT:25UF,+75-10%,25V	00853	556DB250U025B
A8C950	290-0107-00			CAP,FXD,ELCTLT:25UF,+75-10%,25V	00853	556DB250U025B
A8C1000	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-20 %,10V	55680	ULA1A220TAA
A8C1005	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-20 %,10V	55680	ULA1A220TAA
A8C1016	281-0758-00			CAP,FXD,CER DI:15PF,20%,100V	04222	MA101A150MAA
A8C1030	281-0765-00			CAP,FXD,CER DI:100PF,5%,100V	04222	MA101A101JAA
A8CR50	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8CR400	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR505	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR508	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR530	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR852	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR853	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR923	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR927	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR1001	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR1002	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8CR1010	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A8DS750	150-1031-00			LT EMITTING DIO:RED,650NM,40MA MAX	50434	HLMP-1002
A8J335	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8J405	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8J410	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8J420	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 16)	22526	48283-036
A8J540	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 10)	22526	48283-036
A8J645	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 3)	22526	48283-036
A8J742	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8J747	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8J900	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8J930	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8J940	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8L335	108-0443-00			COIL,RF:FIXED,23.5UH	80009	108-0443-00
A8L1040	108-0020-00			COIL,RF:FIXED,7.1UH	TK1345	108-0020-00
A8L1045	108-0020-00			COIL,RF:FIXED,7.1UH	TK1345	108-0020-00
A8L1050	108-0020-00			COIL,RF:FIXED,7.1UH	TK1345	108-0020-00
A8P440	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 7)	22526	48283-036
A8P445	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 6)	22526	48283-036
A8P740	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 1)	22526	48283-036
A8P745	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 1)	22526	48283-036
A8P755	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 2)	22526	48283-036
A8P910	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A8P945	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 9)	22526	48283-036
A8Q830	156-0048-02			MICROCKT,LINEAR:5 XSTR ARRAY,CHECKED	80009	156-0048-02
A8Q1010	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A8Q1015	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A8R100	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A8R101	307-0104-00			RES,FXD,CMPSN:3.3 OHM,5%,0.25W	01121	CB33G5
A8R300	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A8R337	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R400	315-0134-00			RES,FXD,FILM:130K OHM,5%,0.25W	57668	NTR25J-E130K
A8R401	315-0913-00			RES,FXD,FILM:91K OHM,5%,0.25W	19701	5043CX91K00J

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8R425	311-1228-00			RES,VAR,NONWW:TRMR,10K OHM,0.5W	32997	3386F-T04-103
A8R426	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R511	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A8R513	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25W	19701	5043CX6K200J
A8R515	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8R517	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8R518	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8R519	315-0753-00			RES,FXD,FILM:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A8R520	315-0623-00			RES,FXD,FILM:62K OHM,5%,0.25W	19701	5043CX62K00J
A8R521	315-0132-00			RES,FXD,FILM:1.3K OHM,5%,0.25W	57668	NTR25J-E01K3
A8R525	311-1232-00			RES,VAR,NONWW:TRMR,50K OHM,0.5W	32997	3386F-T04-503
A8R530	315-0303-00			RES,FXD,FILM:30K OHM,5%,0.25W	19701	5043CX30K00J
A8R531	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A8R600	315-0273-00			RES,FXD,FILM:27K OHM,5%,0.25W	57668	NTR25J-E27K0
A8R700	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8R701	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R702	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R703	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R704	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R706	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8R708	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8R709	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8R745	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R747	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R813	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R815	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R818	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R820	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A8R821	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R823	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A8R825	315-0362-00			RES,FXD,FILM:3.6K OHM,5%,0.25W	19701	5043CX3K600J
A8R827	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A8R829	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A8R841	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R842	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A8R844	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A8R850	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A8R852	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A8R921	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A8R922	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R923	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8R924	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A8R925	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A8R926	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A8R927	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A8R928	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A8R929	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A8R1000	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A8R1001	315-0912-00			RES,FXD,FILM:9.1K OHM,5%,0.25W	57668	NTR25J-E09K1
A8R1002	315-0363-00			RES,FXD,FILM:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A8R1003	315-0154-00			RES,FXD,FILM:150K OHM,5%,0.25W	57668	NTR25J-E150K
A8R1004	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W	57668	NTR25J-E04K3
A8R1005	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W	57668	NTR25J-E04K3
A8R1010	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A8R1011	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A8R1013	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A8R1014	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A8R1015	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8R1016	321-0225-00			RES,FXD,FILM:2.15K OHM,1%,0.125W,TC=T0	19701	5033ED2K15F
A8R1018	315-0680-00			RES,FXD,FILM:68 OHM,5%,0.25W	57668	NTR25J-E68E0
A8R1019	321-0225-00			RES,FXD,FILM:2.15K OHM,1%,0.125W,TC=T0	19701	5033ED2K15F
A8R1020	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A8R1021	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A8R1023	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A8R1025	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A8R1027	321-0411-00			RES,FXD,FILM:187K OHM,1%,0.125W,TC=T0	91637	MFF1816G18702F
A8R1029	321-0414-00			RES,FXD,FILM:200K OHM,1%,0.125W,TC=T0	07716	CEAD20002F
A8R1030	321-0414-00			RES,FXD,FILM:200K OHM,1%,0.125W,TC=T0	07716	CEAD20002F
A8R1033	321-0414-00			RES,FXD,FILM:200K OHM,1%,0.125W,TC=T0	07716	CEAD20002F
A8TP100	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP100-1 THRU A8TP100-10)	22526	48283-036
A8TP120	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP120-1 THRU A8TP120-9)	22526	48283-036
A8TP130	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP130-1 THRU A8TP130-4)	22526	48283-036
A8TP135	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP135-1 AND A8TP135-2)	22526	48283-036
A8TP140	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP140-1 THRU A8TP140-9)	22526	48283-036
A8TP145	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP145-1 THRU A8TP145-4)	22526	48283-036
A8TP430	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP430-1 THRU A8TP430-10)	22526	48283-036
A8TP435	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP435-1 THRU A8TP435-9)	22526	48283-036
A8TP640	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP640-1, A8TP640-2 AND A8TP640-3)	22526	48283-036
A8TP840	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (A8TP840-1 THRU A8TP840-9)	22526	48283-036
A8U105	156-1622-00			MICROCKT,DGTL:CMOS,8 DIGIT LED DRIVER SYS COMMON CATHODE	32293	ICM7218BIJI
A8U145	160-1959-00			MICROCKT,DGTL:8192 X 8 EPROM,PRGM	80009	160-1959-00
A8U205	156-1535-00			MICROCKT,DGTL:NMOS,PROGRAMMABLE KYBD/DLY INTERFACE,	34335	AM8279-5(N OR J)
A8U245	160-1960-00			MICROCKT,DGTL:8192 X 8 EPROM,PRGM	80009	160-1960-00
A8U300	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A8U305	156-1088-01			MICROCKT,DGTL:8 BIT MICRORROCESSOR,SCRN	34335	P OR D 8085A
A8U320	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A8U340	160-1961-00			MICROCKT,DGTL:8192 X 8 EPROM,PRGM	80009	160-1961-00
A8U505	156-1225-01			MICROCKT,LINEAR:DUAL COMPARATOR,SCREENED	01295	LM393P3
A8U515	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A8U535	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A8U600	156-1623-00			MICROCKT,LINEAR:D/A CONVERTER,8 BIT,VOLTAGE OUTPUT	24355	AD41201
A8U605	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A8U610	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A8U615	156-1429-01	B010100	B010825	MICROCKT,DGTL:1024 X 4 STATIC RAM W/3 STATE OUT,SCREENED	80009	156-1429-01
A8U615	156-2104-00	B010826		MICROCKT,DGTL:CMOS,1024 X 4 STATIC RAM	34371	HM6514-9
A8U630	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A8U635	156-0383-02			MICROCKT,DGTL:QUAD 2-INP NOR GATE,SCRN,	18324	N74LS02NB
A8U700	156-0869-01			MICROCKT,DGTL:8 CHANNEL DGTL MUXER,SCRN	27014	MM74C151JA+
A8U710	156-1429-01	B010100	B010825	MICROCKT,DGTL:1024 X 4 STATIC RAM W/3 STATE OUT,SCREENED	80009	156-1429-01
A8U710	156-2104-00	B010826		MICROCKT,DGTL:CMOS,1024 X 4 STATIC RAM	34371	HM6514-9
A8U715	156-1327-00			MICROCKT,DGTL:CMOS,3 STATE OCTAL D FF,SCRN	27014	MM74C374NA+
A8U730	156-0385-02			MICROCKT,DGTL:HEX INVERTER,SCRN	07263	74LS04PCQR

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8U735	156-0390-02			MICROCKT,DGTL:DUAL 4/2 LINE DCDR/DEMUX,SCRN	01295	SN74LS155NP3
A8U800	156-0411-02			MICROCKT,LINEAR:QUAD COMPARATOR,SCREENED	04713	LM339JDS
A8U805	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A8U815	156-0402-03			MICROCKT,LINEAR:TIMER,TESTED	27014	LM555CJ
A8U825	156-1225-01			MICROCKT,LINEAR:DUAL COMPARATOR,SCREENED	01295	LM393P3
A8U835	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A8U900	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A8U927	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A8U935	156-0385-02			MICROCKT,DGTL:HEX INVERTER,SCRN	07263	74LS04PCQR
A8VR510	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A9	670-7513-00			CIRCUIT BD ASSY:PWR SPLY	80009	670-7513-00
A9C105	283-0051-00			CAP,FXD,CER DI:0.0033UF,5%,100V	04222	SR301A332JAA
A9C108	283-0179-00			CAP,FXD,CER DI:0.68UF,10%,100V	04222	SR501C684KAA
A9C111	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C115	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-10%,35VDC	55680	ULB1V4R7TAAANA
A9C116	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-10%,35VDC	55680	ULB1V4R7TAAANA
A9C117	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C118	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C119	281-0765-00			CAP,FXD,CER DI:100PF,5%,100V	04222	MA101A101JAA
A9C122	283-0249-00			CAP,FXD,CER DI:0.068PF,10%,50V	04222	SR305C683KAA
A9C205	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-20 %,10V	55680	ULA1A220TAA
A9C207	283-0164-00			CAP,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A9C220	290-0683-00			CAP,FXD,ELCTLT:100UF,+20%,200V	TK0510	ECE-A2ES101
A9C301	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A9C302	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A9C325	290-0768-00			CAP,FXD,ELCTLT:10UF,+50-20%,100WVDC	54473	ECE-A100V10L
A9C330	290-0768-00			CAP,FXD,ELCTLT:10UF,+50-20%,100WVDC	54473	ECE-A100V10L
A9C405	283-0693-00			CAP,FXD,MICA DI:1730PF,1%,500V	00853	D195F1731F0
A9C410	290-0818-00	B010100	B010199	CAP,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A9C410	290-0818-02	B010200		CAP,FXD,ELCTLT:390UF,+100-10%,40V	00853	301AER391U040B3
A9C425	290-0771-00			CAP,FXD,ELCTLT:220UF,+50-10%,10VDC	55680	ULA1A221TPA2
A9C530	290-0932-00			CAP,FXD,ELCTLT:390UF,+100-10%,15VDC	56289	672D676
A9C540	290-0771-00			CAP,FXD,ELCTLT:220UF,+50-10%,10VDC	55680	ULA1A221TPA2
A9C630	290-0818-00	B010100	B010199	CAP,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A9C630	290-0818-02	B010200		CAP,FXD,ELCTLT:390UF,+100-10%,40V	00853	301AER391U040B3
A9C640	290-0771-00			CAP,FXD,ELCTLT:220UF,+50-10%,10VDC	55680	ULA1A221TPA2
A9CR100	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A9CR110	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A9CR111	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A9CR121	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A9CR230	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A9CR400	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A9CR402	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A9CR406	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A9CR407	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A9CR410	152-0582-00			SEMICOND DVC,DI:RECT,SI,20V,3A	80009	152-0582-00
A9CR503	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A9CR520	152-0581-00			SEMICOND DVC,DI:RECT,SI,20V,1A,A59	04713	1N5817
A9CR620	152-0582-00			SEMICOND DVC,DI:RECT,SI,20V,3A	80009	152-0582-00
A9DS125	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A9J230	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 3)	22526	48283-036
A9J440	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 6)	22526	48283-036
A9J450	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY 7)	22526	48283-036
A9L220	108-0473-00			COIL,RF:FIXED,174UH	TK2042	ORDER BY DESCR

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A9L310	108-0473-00			COIL,RF:FIXED,174UH	TK2042	ORDER BY DESCR
A9L420	108-0336-00			COIL,RF:FIXED,100UH	80009	108-0336-00
A9L530	108-0336-00			COIL,RF:FIXED,100UH	80009	108-0336-00
A9L630	108-0336-00			COIL,RF:FIXED,100UH	80009	108-0336-00
A9Q100	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A9Q200	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A9Q300	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A9Q305	151-0350-02			TRANSISTOR:SELECTED	80009	151-0350-02
A9Q312	151-0207-00			TRANSISTOR:NPN,SI,X-55,SEL	57668	XD11BCP0207
A9Q313	151-0347-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7951
A9Q315	151-0350-02			TRANSISTOR:SELECTED	80009	151-0350-02
A9Q317	151-0347-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7951
A9Q402	151-0444-03			TRANSISTOR:NPN,SI,TO-92,SCREENED	TK0271	151-0444-00
A9Q500	151-0678-00			TRANSISTOR:NPN,SI,TO-220	04713	MJE13005
A9R100	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A9R102	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A9R105	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A9R109	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W	57668	NTR25J-E04K3
A9R113	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A9R119	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A9R120	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A9R121	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A9R122	321-0305-00			RES,FXD,FILM:14.7K OHM,1%,0.125W,TC=T0	19701	5033ED14K70F
A9R125	311-0609-00			RES,VAR,NONWW:TRMR,2K OHM,0.5W	32997	3329H-L58-202
A9R128	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A9R130	308-0290-00			RES,FXD,WW:8 OHM,5%,5W	00213	1250SB-8-5
A9R208	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W	19701	5043CX1K100J
A9R215	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A9R216	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A9R218	321-0282-00			RES,FXD,FILM:8.45K OHM,1%,0.125W,TC=T0	07716	CFAD84500F
A9R220	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A9R222	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A9R225	315-0132-00			RES,FXD,FILM:1.3K OHM,5%,0.25W	57668	NTR25J-E01K3
A9R226	301-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.5W	19701	5053CX6K800J
A9R300	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A9R301	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A9R302	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A9R303	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A9R305	307-0106-00			RES,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB 47G5
A9R308	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A9R309	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A9R310	315-0361-00			RES,FXD,FILM:360 OHM,5%,0.25W	19701	5043CX360R0J
A9R400	311-1007-00			RES,VAR,NONWW:TRMR,20 OHM,20%,0.5W	32997	3329H-G48-200
A9R401	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A9R405	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A9R410	308-0710-00			RES,FXD,WW:0.27 OHM,5%,1W	75042	BW-20-R2700J
A9R420	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A9R500	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A9T510	120-1462-00			TRANSFORMER,RF:HF FLYBACK	80009	120-1462-00
A9U210	156-0933-01			MICROCKT,LINEAR:RGLTR,PULSE WIDTH MOD,SCRN	34333	SG9976
A9W310	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10	670-7514-00			CIRCUIT BD ASSY:DVM	80009	670-7514-00
A10U120	150-1012-07			LAMP,LED RDOUT:RED,7 SEG,4.0 DIGIT W/FR & FILTER	80009	150-1012-07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
J19	136-0387-01			JACK,TIP:U/W 0.04 DIA PIN,BLACK	71279	4504252010310
J39	131-0372-00			CONN,RCPT,ELEC:CON-HEX,MALE	24931	32JR104-1
J47	131-1315-01			CONN,RCPT,ELEC:BNC,FEMALE	80009	131-1315-01
J49	131-1315-01			CONN,RCPT,ELEC:BNC,FEMALE	80009	131-1315-01
R39	311-2187-00			RES,VAR,NONWW:PNL,10K OHM,10%,0.5W	12697	CM43520
R170	311-2186-00			RES,VAR,NONWW:PNL,5K OHM,10%,0.5W	12697	CM43519
R370	311-2186-00			RES,VAR,NONWW:PNL,5K OHM,10%,0.5W	12697	CM43519
R670	311-2186-00			RES,VAR,NONWW:PNL,5K OHM,10%,0.5W	12697	CM43519
R870	311-2186-00			RES,VAR,NONWW:PNL,5K OHM,10%,0.5W	12697	CM43519
S39	----- -----			(FURNISHED AS A SET WITH R39)		

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

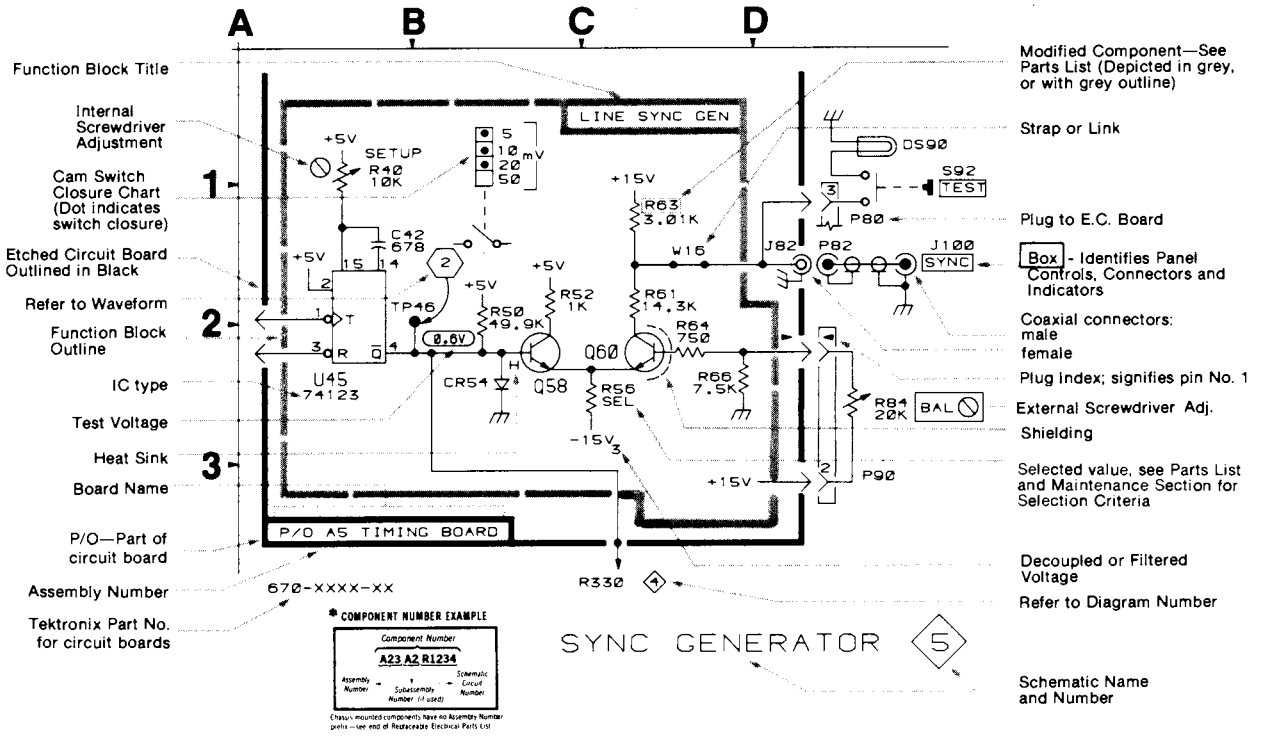
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

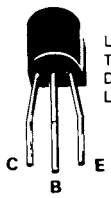
Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.

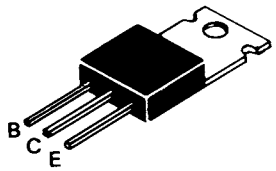


NOTE
LEAD CONFIGURATIONS AND CASE STYLES ARE TYPICAL, BUT MAY VARY DUE TO VENDOR CHANGES OR INSTRUMENT MODIFICATIONS.

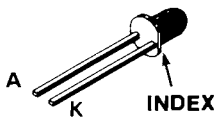


LEAD CONFIGURATION IS MARKED ON TRANSISTOR CASE - SEE SCHEMATIC DIAGRAMS FOR CIRCUIT NUMBER LISTINGS.

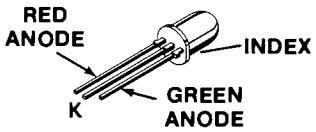
PLASTIC-CASED TRANSISTOR



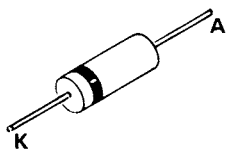
PLASTIC-CASED POWER TRANSISTOR



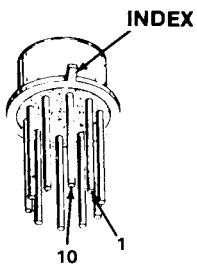
LIGHT EMITTING DIODE (LED)



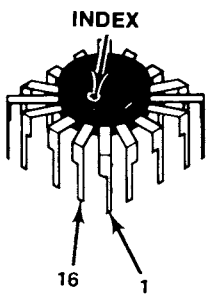
TWO-COLOR LED

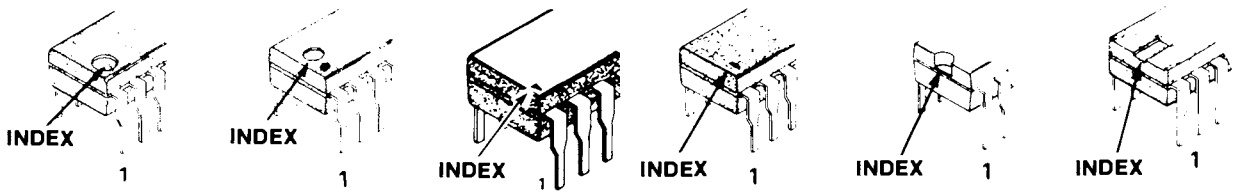


SIGNAL DIODE

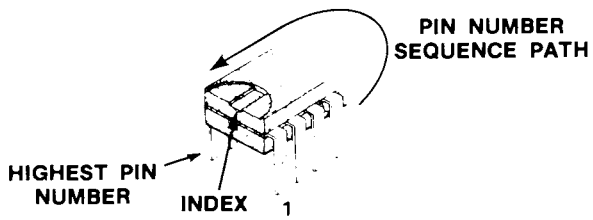


10-PIN





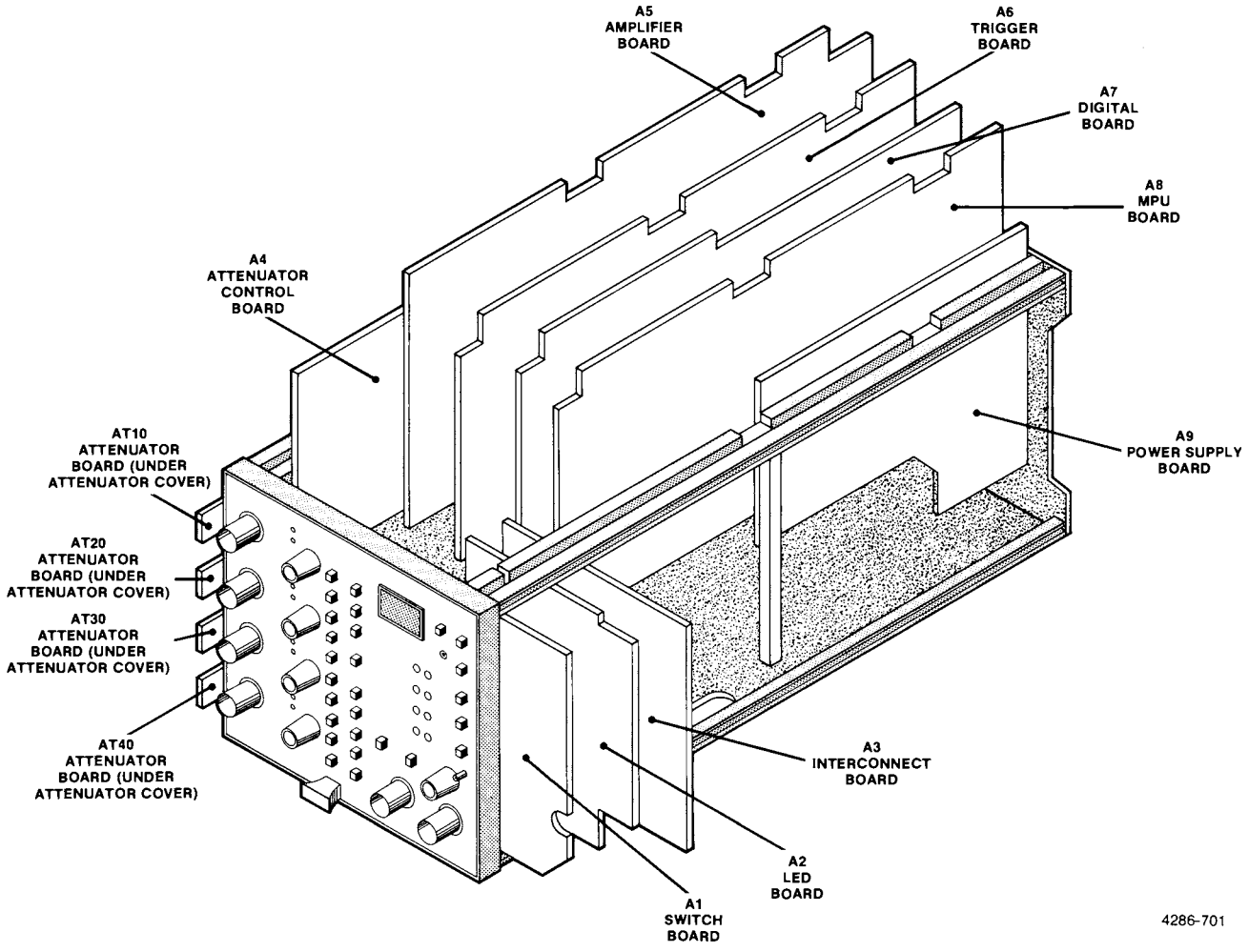
IC PINS ARE NUMBERED COUNTERCLOCKWISE FROM THE INDEX (VIEWED FROM THE TOP)



INTEGRATED CIRCUITS

4286-711

Figure 7-1. Semiconductor lead configuration.



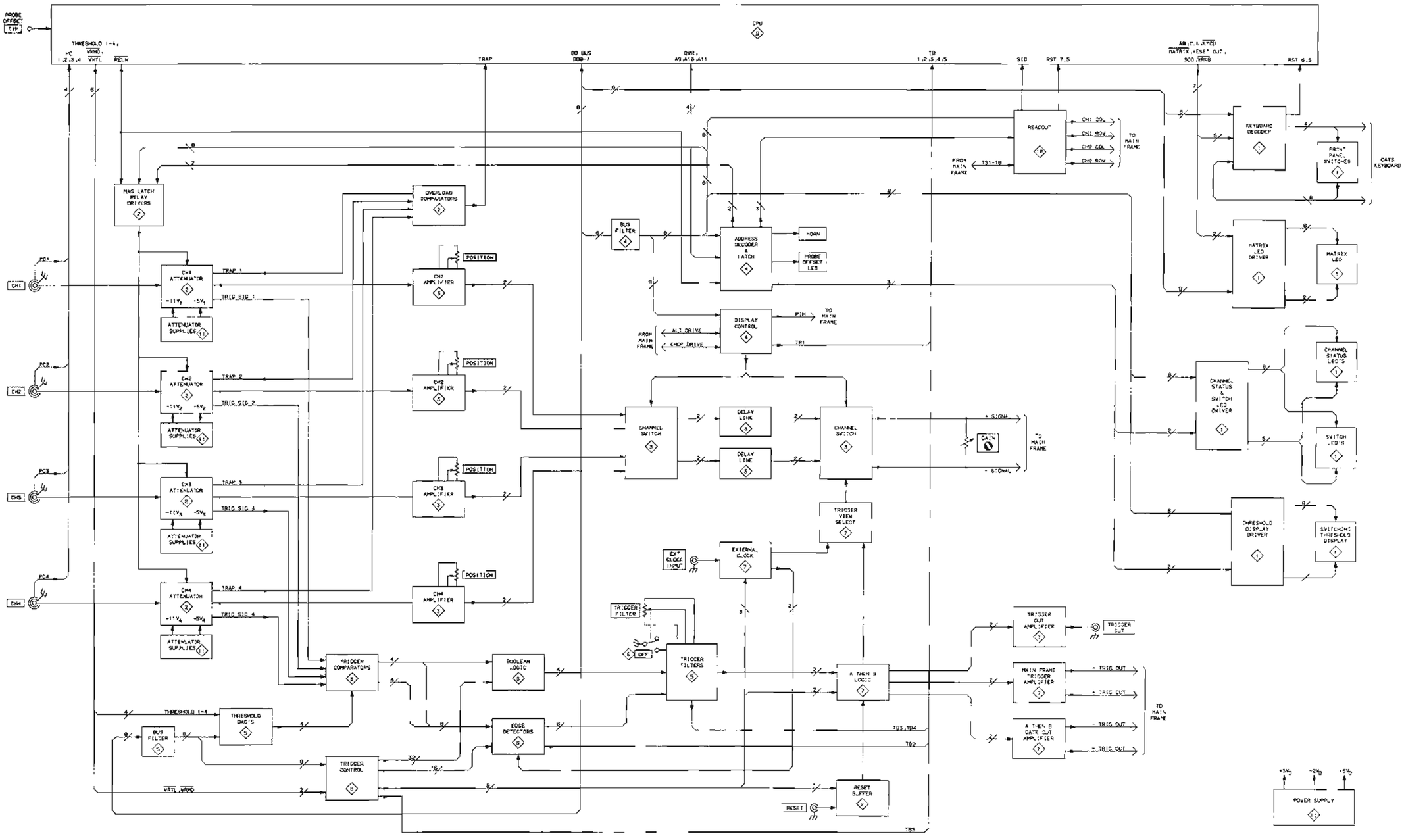
BOARD LOCATOR BY ASSEMBLY NUMBER

Assembly Number	Board Name	Diagram Number
A1	Switch	1,14
A2	LED	1,4,5,6,7,9,14
A3	Interconnect	4,5,6,8,9,10,11,12,14
A4	Attenuator Control	2,3,11,14
A5	Amplifier	3,4,7,10,11,13,14
A6	Trigger	5,6,7,8,11,14
A7	Digital	1,2,4,10,11,14
A8	MPU	1,7,9,11,13,14
A9	Power Supply	11,14
AT10	Attenuator	2
AT20	Attenuator	2
AT30	Attenuator	2
AT40	Attenuator	2

BOARD LOCATOR BY BOARD NAME

Board Name	Assembly Number	Diagram Number
Attenuator	AT10	2
Attenuator	AT20	2
Attenuator	AT30	2
Attenuator	AT40	2
Amplifier	A5	3,4,7,10,11,13,14
Attenuator Control	A4	2,3,11,14
Digital	A7	1,2,4,10,11,14
Interconnect	A3	4,5,6,8,9,10,11,12,14
LED	A2	1,4,5,6,7,9,14
MPU	A8	1,7,9,11,13,14
Power Supply	A9	11,14
Switch	A1	1,14
Trigger	A6	5,6,7,8,11,14

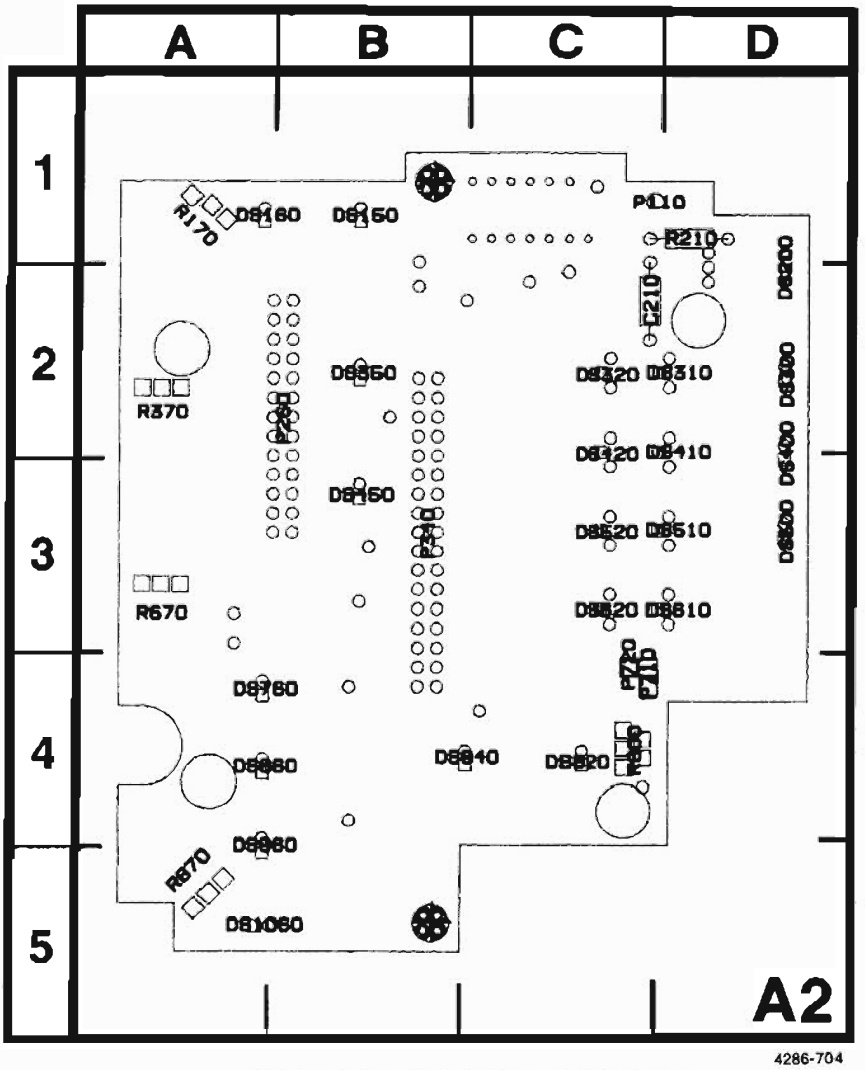
Figure 7-2. 7A42 board locator illustration.



7A42

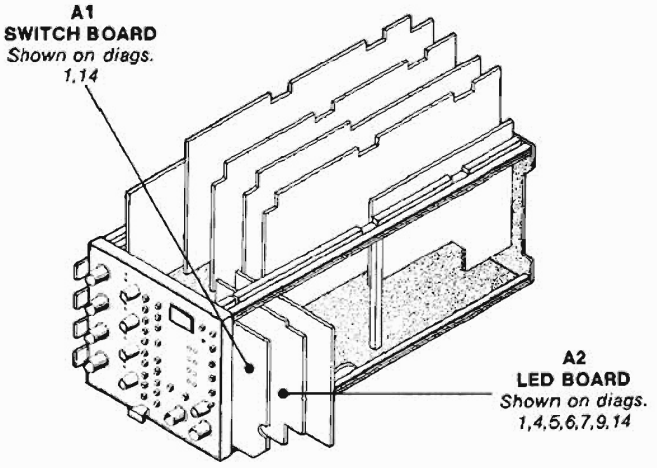
420X-700

BLOCK DIAGRAM



4286-704

Figure 7-4. A2—LED circuit board assembly.



FRONT PANEL DISPLAY & CONTROL DIAGRAM ①

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS170	D2	1A	P140	C1	1B	S400	F2	3E
DS171	D2	1A				S440	E1	3C
DS270	D3	2A	S100	D2	1E	S441	F1	4C
DS271	D3	2A	S110	D2	1D	S450	F1	3B
DS272	E2	2A	S140	D1	1C	S451	F1	4B
DS370	E2	2A	S150	D1	1B	S520	E1	4D
DS371	E3	3A	S200	E2	2E	S530	E1	4C
DS372	E3	3A	S201	E2	2E	S540	F1	4C
DS470	E2	3A	S240	D1	2C	S541	F1	4C
DS471	E2	3A	S241	E1	2C	S550	F1	4B
DS472	E3	4A	S250	D1	2B	S551	F1	4B
DS570	E3	4A	S251	E1	2B	S640	F1	5C
DS571	F2	4A	S300	E2	3E	S650	F1	5B
DS572	F2	4A	S340	E1	3C			
DS670	F3	5A	S350	E1	2B			
DS671	F3	5A	S351	E1	3B			

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS150	D3	1B	DS450	F4	3B	DS860	F3	4A
DS160	E3	1B	DS500	E4	3D	DS960	F3	5A
DS300	F4	2D	DS510	E5	3D	DS1060	E3	5A
DS310	E5	2D	DS520	E5	3C			
DS320	E5	2C	DS610	E6	3D	P260	C3	2B
DS350	D3	2B	DS620	E6	3C	P340	C4	3B
DS400	E4	2D	DS760	F3	4A			
DS410	E5	2D	DS820	F4	4C			
DS420	E5	2C	DS840	F4	4B			

Partial A2 also shown on diagrams 3, 4, 5, 6, 7 and 9.

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J100	C3	3A	J200	C4	4B	J300	C5	5B
J120	C1	5A	J300	C1	5B	J400	C2	5C

Partial A3 also shown on diagrams 3, 4, 5, 6, 8, 9, 11 and 12.

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C310	A2	2C	R628	B2	4G	TP400	B4	1D
C325	A4	4B	R629	B4	4G			
C525	B2	4F				U110	B4	3B
C526	B2	4G	TP100	B4	1B	U320	B3	3C
C825	B4	4J	TP200	B5	1C			
C925	B4	4K	TP300	B2	1C			

Partial A7 also shown on diagrams 2, 4, 10 and 11.

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	B5	2B	TP120	B5	3B	U105	B5	2B
C115	B5	2B	TP130	B1	3B	U205	B1	2C
			TP135	B6	3B			
R101	B5	2B	TP140	B2	4B			

Partial A8 also shown on diagrams 7, 9 and 11.

FRONT PANEL DISPLAY & CONTROL ⟨1⟩

ATTENUATORS & CONTROL DIAGRAM ②

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
AT00010	F6	**	CR203	F2	2C	Q3	G5	**
AT20	F3	**	CR204	F2	2C	Q4	G5	**
AT30	F2	**	CR205	F2	3C			
AT40	F1	**	CR206	F2	3C	R1	E5	**
			CR210	H2	2B	R2	E5	**
C1	E5	**	CR211	G2	2B	R4	E5	**
C2	F5	**	CR212	G2	3B	R5	F5	**
C3	F5	**	CR213	G2	3B	R6	F6	**
C4	F5	**	CR301	G3	3C	R8	F5	**
C5	F5	**	CR302	G3	3C	R9	F5	**
C6	F5	**	CR303	F3	3C	R10	F5	**
C7	G5	**	CR304	F3	4C	R11	F5	**
C8	G6	**	CR305	F3	4C	R12	F5	**
C9	H6	**	CR306	F3	4C	R13	F5	**
C10	G6	**	CR310	H3	3B	R14	F5	**
C11	H6	**	CR311	G3	3B	R15	F5	**
C12	G5	**	CR312	G3	4B	R16	G5	**
C13	G5	**	CR313	G3	4B	R17	G5	**
C14	H6	**	CR401	F4	4C	R18	F5	**
C101	D6	1C	CR402	F4	4C	R19	G6	**
C102	D2	2C	CR403	E4	4C	R20	G5	**
C104	D1	1C	CR404	F4	5C	R21	G5	**
C106	E1	2D	CR405	E4	5C	R22	G4	**
C110	D1	2B	CR406	E4	5C	R23	G4	**
C115	C2	1B	CR411	H4	4B	R24	G5	**
C118	H2	1A	CR412	G4	5B	R25	G5	**
C201	D6	2C	CR413	G4	5B	R26	G5	**
C202	D2	3C	CR414	G4	4B	R27	G5	**
C204	D1	2B				R28	G5	**
C206	E2	3D	K11	E4	**	R29	G5	**
C215	C2	3B	K12	F4	**	R30	G5	**
C301	D6	3C	K13	F4	**	R31	G5	**
C302	D2	4C	K14	G4	**	R32	G5	**
C306	E3	4D	K15	H4	**	R33	G5	**
C311	D1	4B	K21	F3	**	R34	G5	**
C315	C2	4B	K22	F3	**	R101	E1	1C
C317	D1	3B	K23	G3	**	R102	D2	2C
C401	D6	4C	K24	G3	**	R110	D2	2B
C402	D3	5C	K25	G3	**	R111	D2	1B
C406	E5	5D	K31	F2	**	R112	H1	1B
C414	D1	5B	K32	F2	**	R210	E2	2B
C415	C3	4B	K33	G2	**	R211	H2	2B
C416	D1	5B	K34	G2	**	R301	D3	3C
			K35	G2	**	R310	E3	3B
CR101	G1	1C	K41	F1	**	R311	H3	3B
CR102	G1	1C	K42	F1	**	R401	D3	4C
CR103	F1	1C	K43	G1	**	R410	E5	4B
CR104	F1	1C	K44	G1	**	R411	H5	4B
CR105	F1	2C	K45	G1	**			
CR106	F1	2C				RT3	E5	**
CR110	G1	1B	L1	F6	**	RT7	E6	**
CR111	H1	1B	L2	G5	**			
CR112	G1	2B	L3	G5	**	U1	G5	**
CR113	G1	2B				U1	G6	**
CR201	G2	2C	Q1	G5	**			
CR202	G2	2C	Q2	G5	**			

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C120	A5	4B	R236	A5	5C	U130A	B6	4B
C230	B6	5C	R236	B5	5C	U130B	B5	4B
C231	B6	5C	R238	B6	4C	U130C	B5	4B
C330	B5	5C	R239	B6	4C	U130D	B5	4B
C331	B5	5C	R330	B5	4C	U330	B1	4D
			R331	B5	4C	U420	A1	3D
CR230	A5	4C	R333	B1	5D	U421	A3	3E
CR231	A5	5C	R430	B2	5D	U430	B2	4D
CR520	B3	4F	R431	B3	5E	U431	B2	4E
CR521	B3	4F	R520A	A3	3E	U520	B3	3F
CR530	B4	5E	R520B	B4	3E	U530A	B1	4E
CR630	B4	5F	R520C	A4	3E	U530B	B3	4E
			R520D	A5	3E	U530C	B2	4E
J401	A5	1E	R520E	A3	3E	U530D	B2	4E
			R520F	A4	3E	U530E	B2	4E
R230	B6	4C	R520G	B4	3E	U530F	B3	4E
R231	B6	4C	R520H	B4	3E	U531	B4	4F
R232	B5	4C	R520J	A4	3E	U830C	C5	4H
R233	B5	4C	R521	B3	3F			
R234	A5	5C	R530	B4	5F			

Partial A7 also shown on diagrams 1, 4, 10 and 11.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C10	E5	CHASSIS	C40	E1	CHASSIS	J20	E3	CHASSIS
C20	E3	CHASSIS				J30	E2	CHASSIS
C30	E2	CHASSIS	J10	E5	CHASSIS	J40	E1	CHASSIS

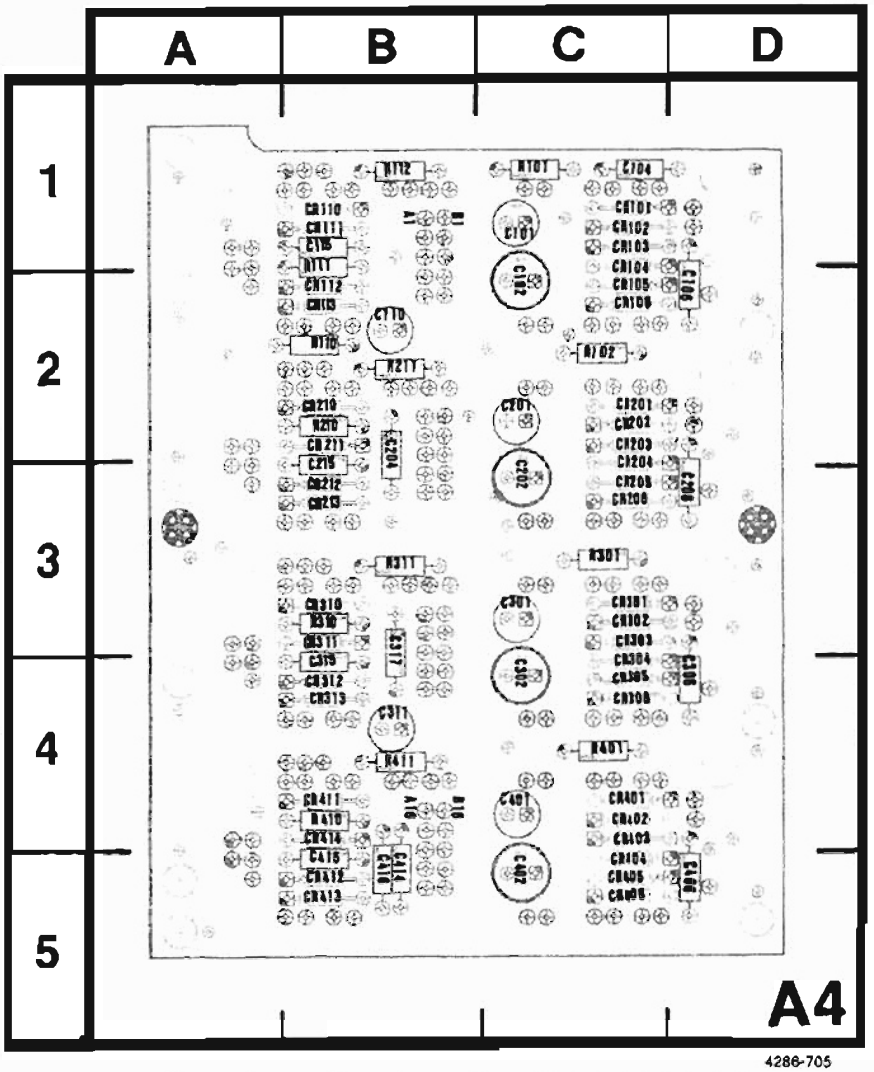


Figure 7-5. A4—Attenuator Control circuit board assembly.

Illustration and locator

COMPONENT NUMBER EXAMPLE

Component Number

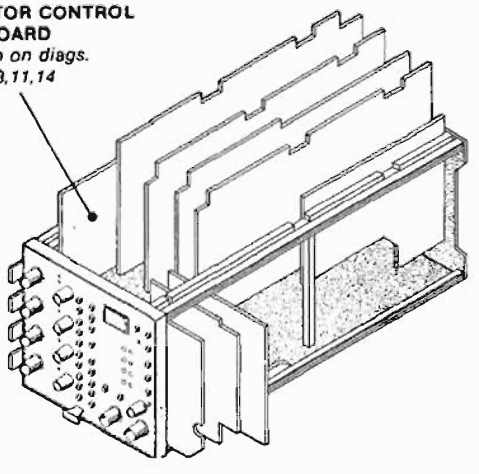
A23 A2 R1234

Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

A4
ATTENUATOR CONTROL
BOARD
Shown on diags.
2,3,11,14

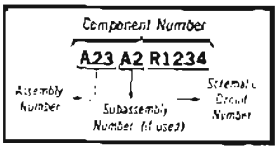


VOLTAGE CONDITIONS ◇2

Do not press front-panel keys.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Cross-mounted components have no Assembly Number (refer to end of Replaceable Electrical Parts List)

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

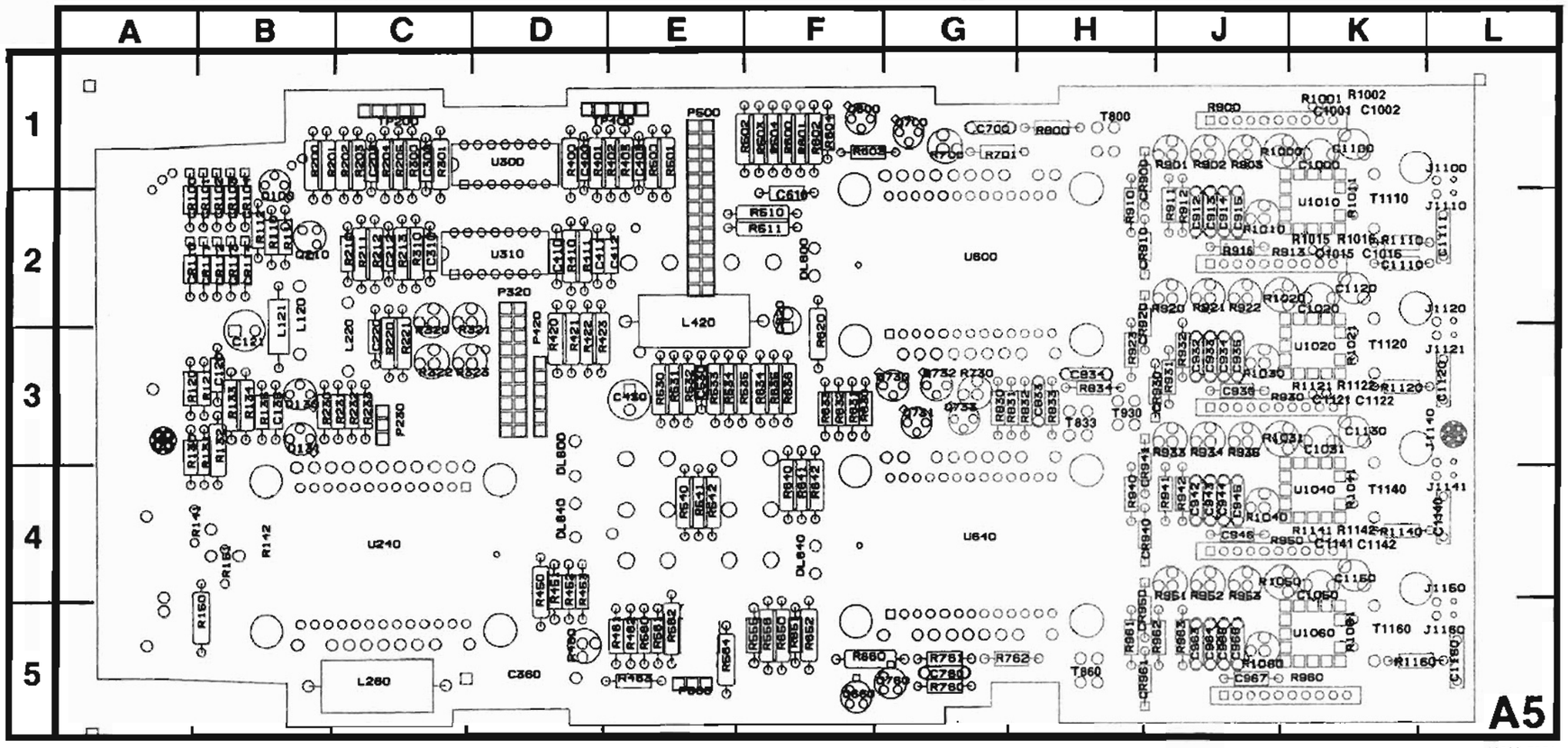
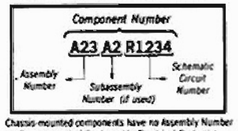


Figure 7-6. A5—Amplifier circuit board assembly.

A5-Amplifier circuit bd
Illustration and locator

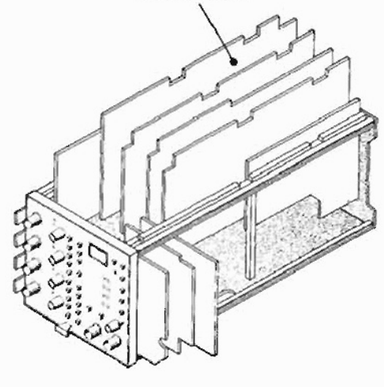
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

A5
AMPLIFIER BOARD
Shown on diags.
3,4,7,10,11,13,14



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CHANNEL SWITCHING & AMPLIFIERS DIAGRAM ③

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C700	C1	1G
C760	C5	5G
C833	C4	3H
C834	C3	3H
C912	B1	2J
C913	B1	2J
C914	B1	2J
C915	A1	2J
C932	B3	3J
C933	B3	3J
C934	B3	3J
C935	A3	3J
C936	C3	3J
C942	B4	4J
C943	B4	4J
C944	B4	4J
C945	A4	4J
C946	C4	4J
C963	B5	5J
C964	B5	5J
C965	B5	5J
C966	A5	5J
C967	C6	5J
C1000	B1	1K
C1001	B1	1K
C1002	B1	1K
C1015	B3	2K
C1016	B3	2K
C1020	B3	2K
C1031	B4	3K
C1050	B5	4K
C1100	B1	1K
C1110	C2	2K
C1111	A1	2L
C1120	A3	3L
C1121	B4	3K
C1122	B4	3K
C1130	B4	3K
C1140	A4	4L
C1141	B5	4L
C1142	B5	4K
C1150	B5	4K
C1160	A5	5L
CR900	C2	1H
CR910	C1	2H
CR920	C3	3H
CR930	C2	3J
CR940	C3	4H
CR941	C4	4H
CR950	C6	5H
CR961	C5	5H
DL600	F2	2F
DL640	F5	4D
J1100	A1	1L
J1110	A1	2L
J1120	A2	2L
J1121	A3	3L
J1140	A4	3L
J1141	A4	4L
J1150	A5	4L
J1160	A5	5L
P320	E1	2D
P320	G1	2D
P500	D1	1E
P500	D2	1E
P500	D3	1E
P500	D5	1E
P560	F6	5E
Q600	C1	1F
Q660	C5	5F
Q700	C1	1G
Q730	C3	3G
Q731	C4	3G
Q732	C2	3G
Q733	C4	3G
Q760	C5	5G
R132	H3	3B
R141	H3	4B
R142	H4	4B
R150	H4	5B
R151	H4	4B
R450	G4	4D
R451	G3	4D
R452	G3	4D
R453	H3	4D
R460	G5	5D
R461	G4	5E
R462	G4	5E
R463	G6	5E
R500	D3	1E
R501	D5	1E
R502	D4	1F
R503	D1	1F
R504	D1	1F
R510	D4	2F
R511	D1	2F
R530	D3	3E
R531	D5	3E
R532	D1	3E
R533	D5	3E
R534	D5	3E
R535	D3	3F
R540	C3	4E
R541	C2	4E
R542	C2	4E
R555	C5	5F
R556	C5	5F
R560	G5	5E
R561	G4	5E
R562	F5	5E
R564	G6	5E
R600	C1	1F
R601	C1	1F
R602	C1	1F
R603	C1	1F
R604	C1	1F
R620	E2	3F
R630	C3	3F
R631	C4	3F
R632	C2	3F
R633	C3	3F
R634	D4	3F
R635	D2	3F
R636	D3	3F
R640	C4	4F
R641	C4	4F
R642	C4	4F
R650	C5	5F
R651	C5	5F
R652	C5	5F
R660	E5	5F
R700	F2	1G
R701	F2	1G
R730	F4	3G
R760	C5	5G
R761	E6	5G
R762	E6	5H
R800	C1	1H
R830	E3	3G
R831	E3	3G
R832	F4	3H
R833	C4	3H
R834	C2	3H
R900	A1	1J
R900	A1	1J
R900	B1	1J
R900	B1	1J
R901	B1	1J
R902	B1	1J
R903	A1	1J
R910	C1	2H
R911	C1	2J
R912	B1	2J
R913	A2	2J
R913	A3	2J
R913	B2	2J
R913	B2	2J
R913	B2	2J
R913	B2	2J
R913	B3	2J
R916	C2	2J
R920	B2	2J
R921	B3	2J
R922	A2	2J
R923	C2	3H
R930	A4	3K
R930	A4	3K
R930	B3	3K
R930	B3	3K
R930	B3	3K
R930	B4	3K
R930	B4	3K
R931	C3	3J
R932	B2	3J
R933	B4	3J
R934	B4	3J
R935	A4	3J
R940	C4	4H
R941	C4	4J
R942	B4	4J
R950	A5	4J
R950	A5	4J
R950	B4	4J
R950	B5	4J
R950	B5	4J
R950	B5	4J
R951	B5	4J
R952	B5	4J
R953	A5	4J
R960	B6	5K
R960	B6	5K
R960	B6	5K
R961	C5	5H
R962	C5	5J
R963	B5	5J
R1000	B1	1J
R1001	B1	1K
R1002	B1	1K
R1010	C1	2J
R1011	B1	2K
R1015	B2	2K
R1016	B2	2K
R1020	B3	2J
R1021	B3	3K
R1030	C3	3J
R1031	B4	3K
R1040	C4	4J
R1041	B4	4K
R1050	B5	4J
R1060	C5	5J
R1061	B5	5K
R1110	A1	2K
R1120	A2	3K
R1121	B4	3K
R1122	B4	3K
R1140	A3	4K
R1141	B5	4K
R1142	B5	4K
R1160	A5	5K
T800	C1	1H
T833	C4	3H
T860	C5	5H
T930	C2	3H
T1110	A1	2K
T1120	A3	3K
T1140	A4	4K
T1160	A5	5K
U240	G2	4C
U600	E1	2G
U640	E4	4G
U1010	B1	2K
U1020	B2	3K
U1040	B3	4K
U1060	B5	5K

Partial A5 also shown on diagrams 4, 7, 10 and 11.

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P260	D1	2B
P260	D2	2B
P260	D3	2B
P260	D5	2B
R170	E1	1A
R370	E2	2A
R670	E4	3A
R870	E5	5A

Partial A2 also shown on diagrams 1, 4, 5, 6, 7 and 9.

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J100	D1	3A
J100	D2	3A
J100	D4	3A
J100	D5	3A
J600	D1	2D
J600	D2	2D
J600	D4	2D
J600	D5	2D

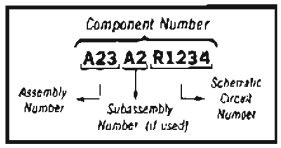
Partial A3 also shown on diagrams 1, 4, 5, 6, 8, 9, 11 and 12.

VOLTAGE CONDITIONS

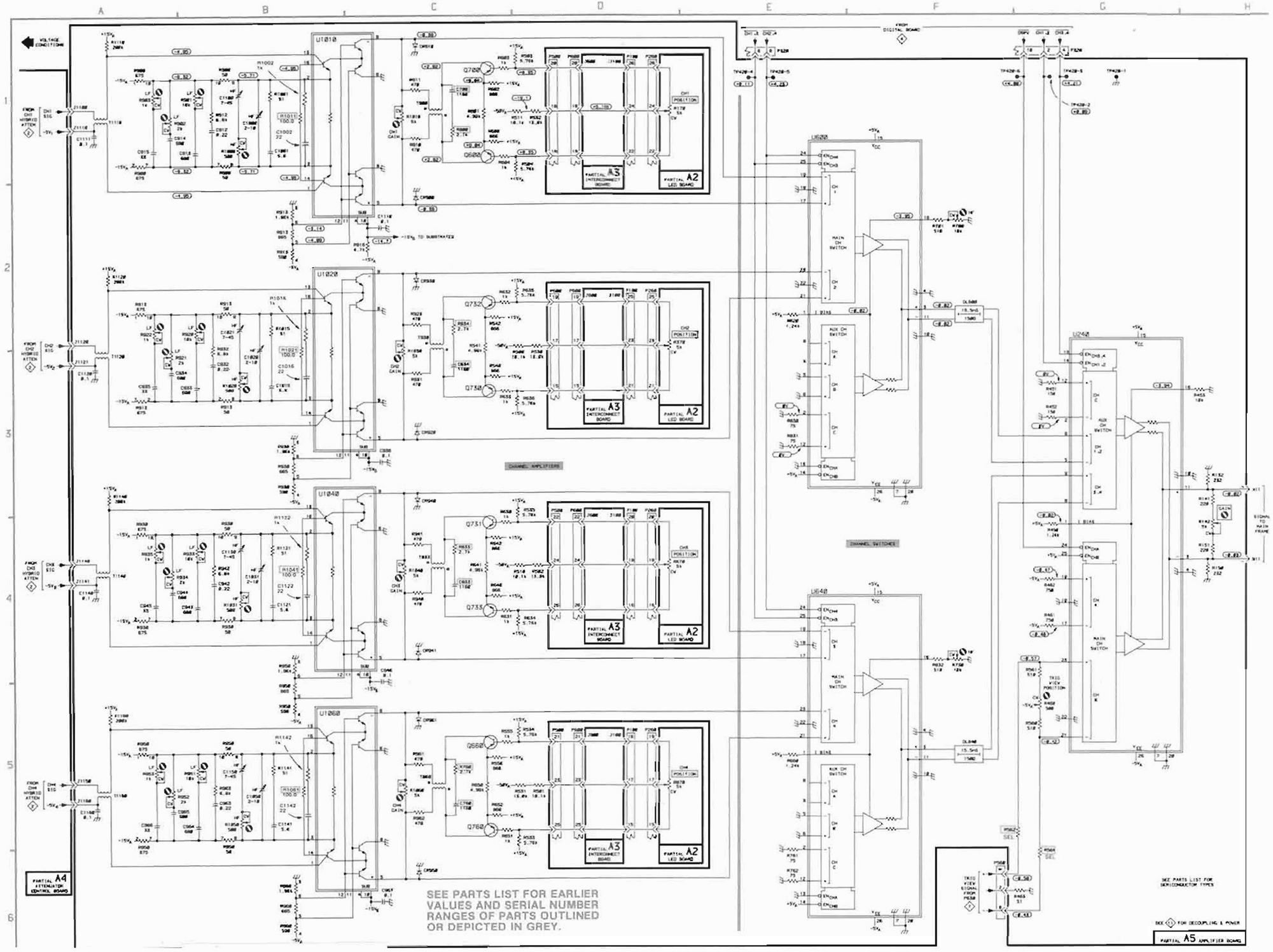
POSITION controls—centered.
CH1-CH4 inputs—Gnd.

Static Sensitive Devices
See Maintenance Section

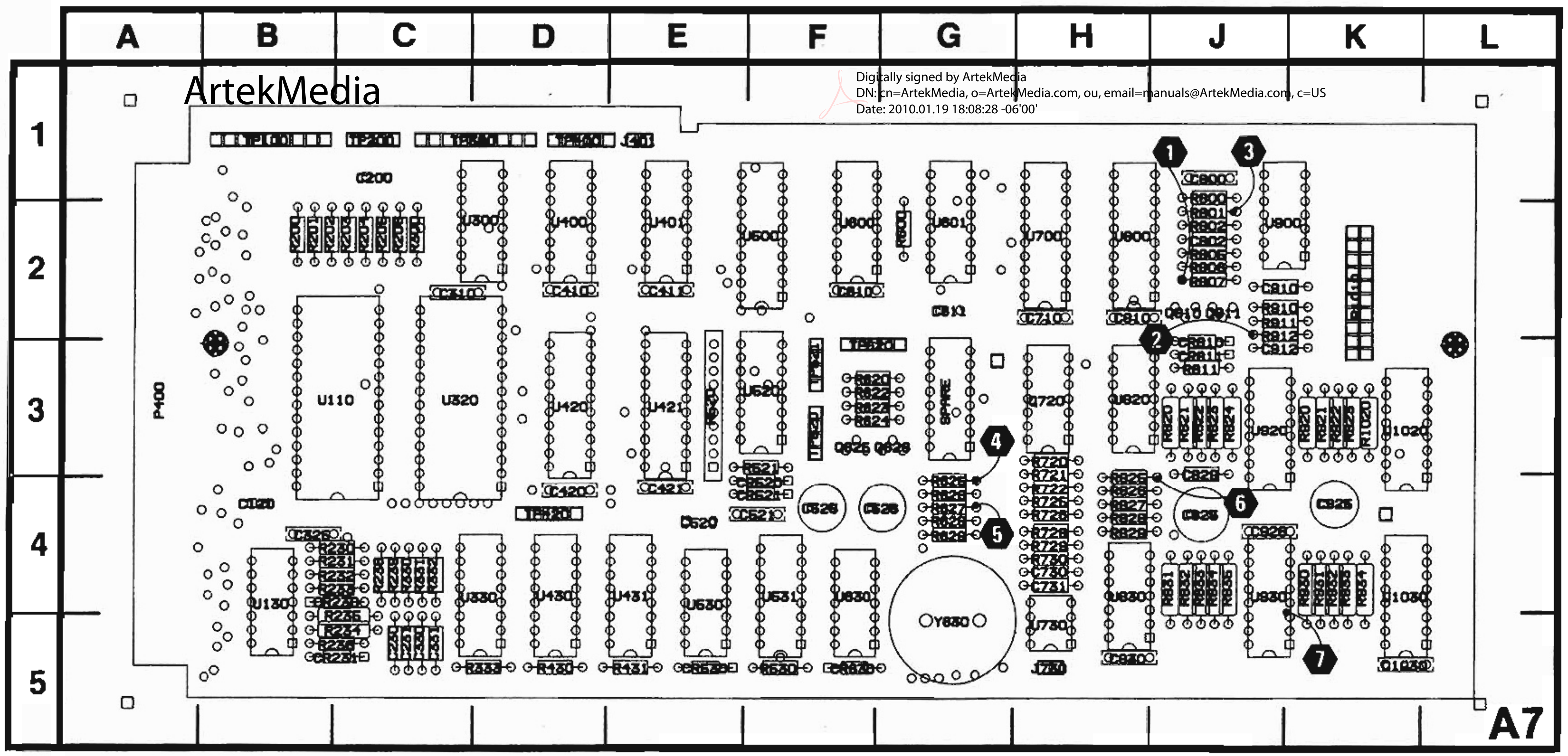
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

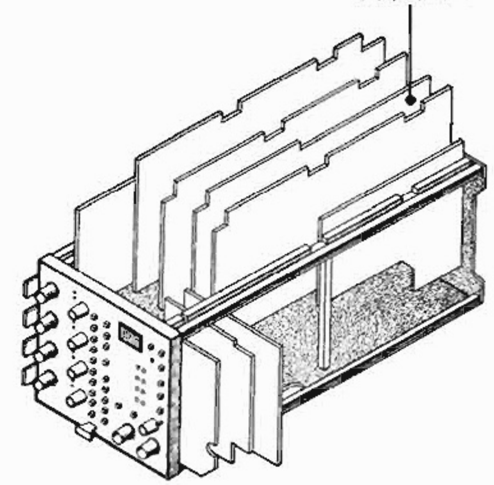


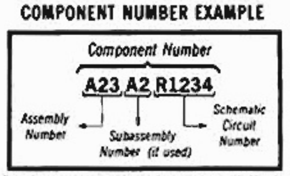
A7-Digital circuit bd
illustration and locator



4286-707

Figure 7-7. A7—Digital circuit board assembly.





Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

DISPLAY CONTROL DIAGRAM 4

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS200	G2	2D	P340	G2	3B

Partial A2 also shown on diagrams 1, 3, 5, 6, 7 and 9.

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J200	F2	4B	J400	F2	5C
J400	A1	5C			

Partial A3 also shown on diagrams 1, 3, 5, 6, 8, 9, 11 and 12.

ASSEMBLY A5

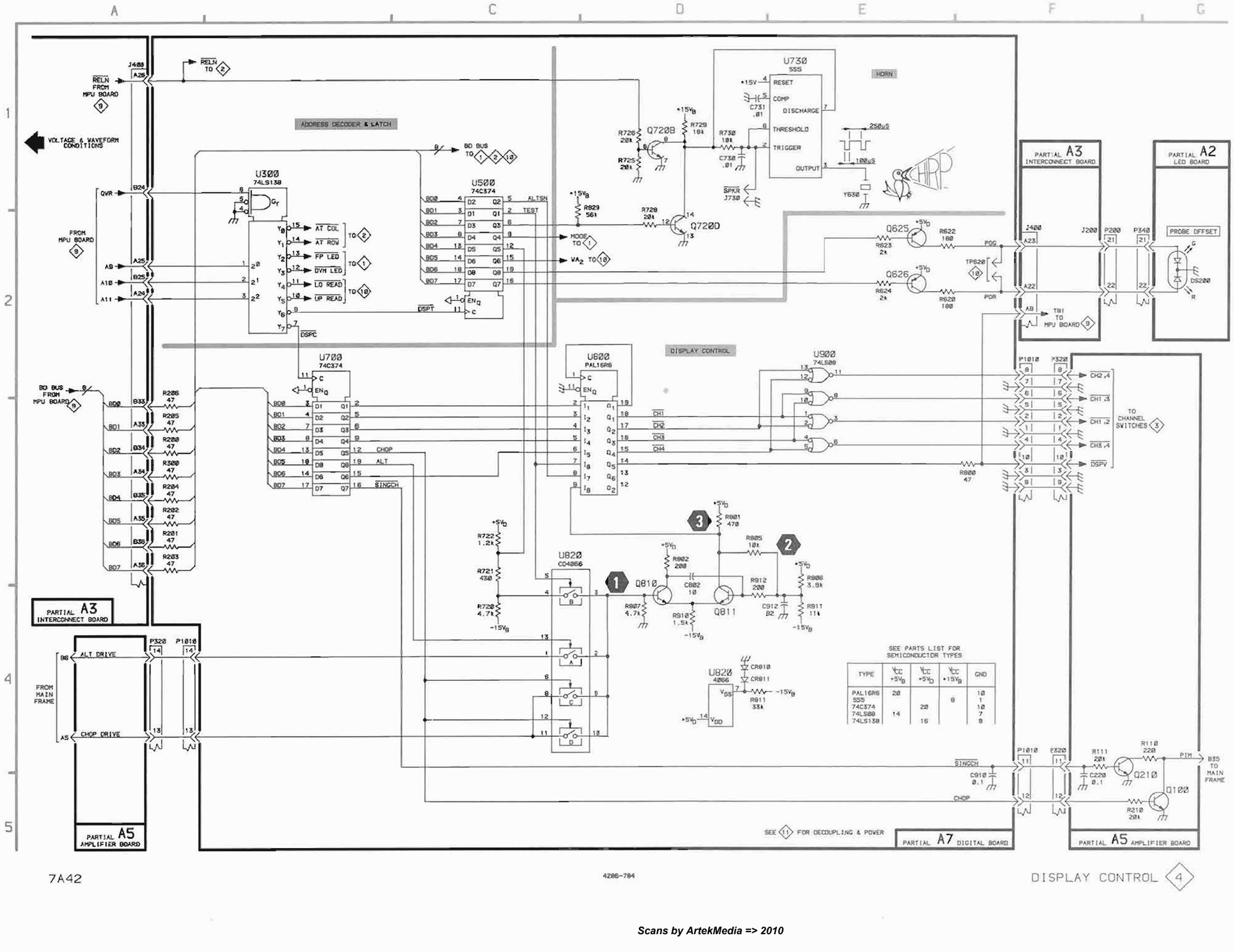
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C220	F5	3C	Q100	G5	2B
			Q210	G5	2B
P320	A4	2D			
P320	F2	2D	R110	G4	2B
P320	F4	2D	R111	F4	2B
			R210	F5	2C

Partial A5 also shown on diagrams 3, 7, 10 and 11.

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C730	D1	4H	R624	E2	3F
C731	D1	4H	R720	C4	3H
CB02	D4	2J	R721	C3	4H
C910	F5	2J	R722	C3	4H
C912	E4	3J	R725	D1	4H
			R726	D1	4H
CR810	D4	3J	R728	D2	4H
CR811	D4	3J	R729	D1	4H
			R730	D1	4H
J730	D1	5H	R800	F3	1J
			R801	D3	2J
P1010	A4	2K	R802	D3	2J
P1010	F2	2K	R805	D3	2J
P1010	F4	2K	R806	E3	2J
			R807	D4	2J
Q625	E2	3F	R811	D4	3J
Q626	E2	3G	R829	D1	4H
Q720B	D1	3H	R910	D4	2J
Q720D	D2	3H	R911	E4	2J
Q810	D3	2J	R912	D3	2J
Q811	D4	2J			
			TP620	F2	3F
R200	A3	2B			
R201	A3	2B	U300	B1	2D
R202	A3	2B	U500	C1	2F
R203	A3	2C	U700	B2	2H
R204	A3	2C	U730	E1	5H
R205	A3	2C	U800	D2	2H
R206	A2	2C	U820	C3	3H
R300	A3	2C	U820	D4	3H
R620	E2	3F	U900	E2	2J
R622	E2	3F			
R623	E2	3F	Y630	E1	5G

Partial A7 also shown on diagrams 1, 2, 10 and 11.

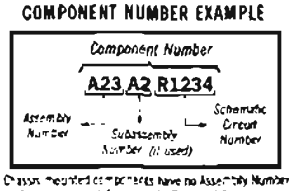


VOLTAGE CONDITIONS ⑤

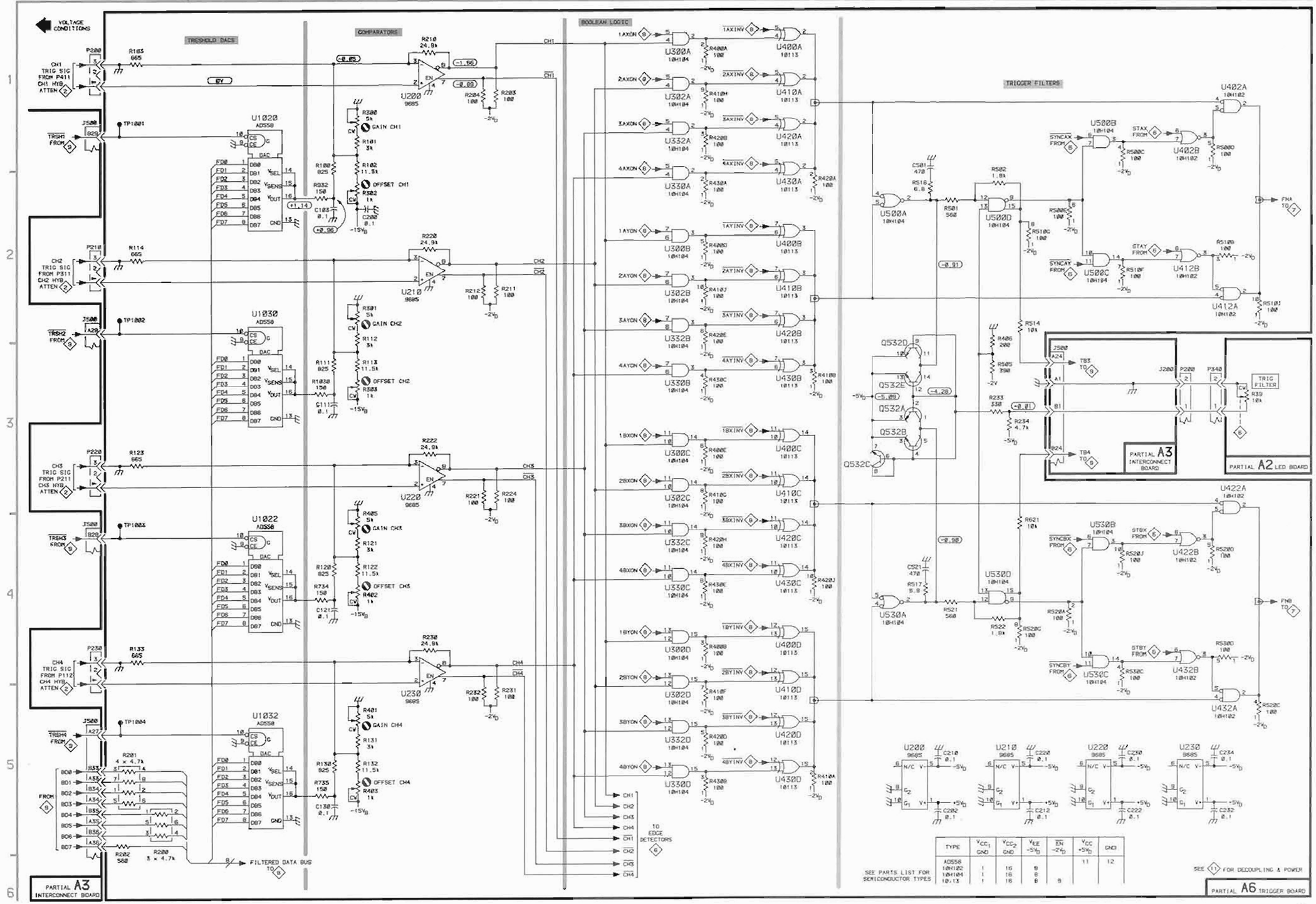
Power-up default with no inputs connected.
TRIGGER FILTER—off (in detent).

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List



Scans by ArtekMedia => 2010

EDGE DETECTORS DIAGRAM 6

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P340	E1	3B	S39	F1	4C

Partial A2 also shown on diagrams 1, 3, 4, 5, 7 and 9.

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J200	E1	4B	J500	F4	6D
J500	E1	5D			

Partial A3 also shown on diagrams 1, 3, 4, 5, 8, 9, 11 and 12

ASSEMBLY A6

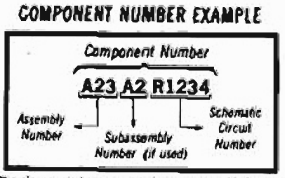
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C900	E1	1K	R700F	D3	2H
			R700G	C5	2H
Q1000	D1	1K	R700H	D4	2H
			R700J	D2	2H
R400C	B4	2D	R903	E1	1K
R404	E2	2D	R1000	D1	2K
R410C	B4	2D	R1001	D1	2K
R410D	A4	2D			
R410E	B4	2D	U310	C1	3C
R411	E3	3D	U312	C2	3D
R420C	B4	3D	U320	C3	4C
R420F	A4	3D	U322	C4	4D
R420G	A4	3D	U402C	E2	2E
R421	E3	4D	U402D	F1	2E
R430D	B4	4D	U412C	E3	3E
R431	E4	4D	U412D	F2	3E
R432	F4	5D	U422C	E3	4E
R500A	F2	2E	U422D	F3	4E
R500B	E2	2E	U432C	E4	5E
R500E	F2	2E	U432D	F4	5E
R510A	E4	3E	U510A	E2	3E
R510C	E3	3E	U510B	E2	3E
R510D	E4	3E	U510C	E3	3E
R520E	F4	3E	U510D	E4	3E
R520H	F3	3E	U700A	D3	2H
R530A	F4	4E	U700B	D2	2H
R530B	F4	4E	U700C	D4	2H
R530E	E4	4E	U700D	D5	2H
R700A	D5	2H	U800A	D3	2H
R700B	D3	2H	U800B	D2	2H
R700C	D2	2H	U800C	D5	2H
R700D	D4	2H	U800D	D4	2H
R700E	D5	2H			

Partial A6 also shown on diagrams 5, 7, 8 and 11

Edge Detectors component locator

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



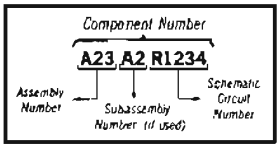
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

VOLTAGE CONDITIONS

TRIGGER FILTER—off (in detent).

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

TYPE	V_{CC_1} GND	V_{CC_2} GND	V_{EE} $-5V_D$
10H102	1	16	8
10104	1	16	8
10H164	1	16	8

VOLTAGE CONDITIONS

PARTIAL A3 INTERCONNECT BOARD

PARTIAL A2 LED BOARD

(TRIG FILTER)

CCW OFF S39

CLOSED IN CCW POSITION

Q1000 FILTER OFF

U310 10H164 U312 10H164 U320 10H164 U322 10H164

CH1 CH2 CH3 CH4 CH1 CH2 CH3 CH4

MS0AX MS1AX MS2AX MENAX

MS0AY MS1AY MS2AY MENAY

MS0BX MS1BX MS2BX MENBX

MS0BY MS1BY MS2BY MENBY

MUX SEL EN

U800B 10104 U800A 10104 U800D 10104 U800C 10104

EXEDGEN FROM 7

SYNCAX TO 5 SYNCAY TO 5 SYNCBX TO 5 SYNCBY TO 5

U700B 10104 U700A 10104 U700C 10104 U700D 10104

BEXTCLK FROM 7

U510A 10H102 U510B 10H102 U510C 10H102 U510D 10H102

RSAX FROM 7 RSAY FROM 7

U402C 10H102 U412C 10H102 U422C 10H102 U432C 10H102

U402D 10H102 U412D 10H102 U422D 10H102 U432D 10H102

STAX TO 5 STAY TO 5 STBX TO 5 STBY TO 5

TB2 TO 8 MPU BD

PARTIAL A3 INTERCONNECT BOARD

PARTIAL A6 TRIGGER BOARD

* CAPACITOR IS INTEGRAL PART OF ECB

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

SEE 11 FOR DECOUPLING & POWER

EDGE DETECTORS 6

6 Edge Detectors

Reverse Side Locator

7A42

4266-786

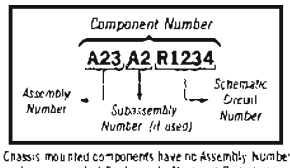
REV DEC 1983

VOLTAGE CONDITIONS ⑦

Power-up default with no inputs connected.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts list

A THEN B LOGIC & TRIGGER I/O DIAGRAM 7

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P710	A1	4C	P720	A1	4C

Partial A2 also shown on diagrams 1, 3, 4, 5, 6 and 9.

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C135	F2	3B	R121	F3	3B	R230	F2	3C
			R130	G2	3A	R231	F3	3C
Q130	F2	3B	R131	G3	3B	R232	F2	3C
Q131	F3	3B	R133	F3	3B	R233	F2	3C
			R134	F2	3B			
R120	F2	3A	R135	F2	3B			

Partial A5 also shown on diagrams 3, 4, 10 and 11.

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C602	E1	2G	R513	E3	3F	R721	B1	4G
C631	B5	5G	R515	E2	3F	R722	B1	4G
C632	F5	5F	R520B	E2	3E	R723	C5	4G
C700	F1	2G	R520F	C2	3E	R724	B1	4G
C701	F1	2G	R525	C3	4F	R725	C6	4H
C710	F1	3G	R600	E4	2F	R726	C5	4G
C712	B1	3H	R601	E3	2F	R727	C5	4G
C720	B1	4G	R610A	D5	3G	R728	D5	4G
C726	C5	4G	R610B	E1	3G	R729	D5	4G
CR520	B2	3F	R610D	C2	3G	R731	C5	5G
CR521	B2	3F	R610E	C3	3G	R733	C5	5G
CR620	B5	4G	R610F	E3	3G	R901	B3	2J
CR622	B2	3F	R610G	E3	3G	R1002	B2	2K
CR720	B1	4G	R610H	E4	3G	R1003	B2	2K
CR721	B1	4H	R610J	D2	3G	R1004	C4	2K
CR722	B5	4G	R611	F1	2G	R1005	C4	2K
CR730	C5	5G	R620A	E5	4G	R1010	D5	2K
CR731	C5	5G	R620B	E5	4G	R1014	D4	3K
			R620C	F5	4G			
J602	F1	2G	R620D	F4	4G	U520A	C2	4E
J634	B5	5G	R620E	F4	4G	U520B	C2	4E
J700	A1	2G	R620F	F5	4G	U520C	C4	4E
J701	D1	1G	R620G	E4	4G	U520D	C3	4E
			R620H	E1	4G	U600A	D2	2F
P600	F3	2F	R620J	E2	4G	U600B	E2	2F
P610	F2	2F	R622	C1	4G	U600C	D2	2F
P630	G4	5F	R623	C1	4G	U600D	D3	2F
P632	A5	5G	R630	G5	5G	U610A	E1	3F
			R631	G4	5G	U610B	C2	3F
Q600	F1	2G	R632	B5	5G	U610C	C4	3F
Q610	F1	3G	R633	B5	5G	U610D	E2	3F
Q620	B1	3G	R702	F2	2G	U620A	D5	4F
Q622	C5	4G	R705	F1	2G	U620B	E1	4F
Q720	B1	3G	R706	E1	2G	U620C	F4	4F
Q722	B1	3G	R707	F1	2G	U630	E4	5F
Q724	D5	4G	R708	F1	2G			
Q726	C5	4G	R709	B3	2G	VR700	E1	2G
Q1002	C4	1K	R710	F1	3G	VR710	F1	3G
Q1004	B3	2L	R711	F1	3G			
Q1010	B2	2K	R712	F1	3G	W612	F1	3G
Q1012	D4	2K	R713	B1	3G	W620	B5	4G
			R714	B1	3H	W700	D1	1G
R510H	D2	3E	R715	D1	3H	W701	F1	2G
R511	C2	3F	R716	E1	3H			
R512	C2	3F	R720	C1	4G			

Partial A6 also shown on diagrams 5, 6, 8 and 11.

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1016	F4	2L	R1004	G4	2K	R1018	F4	2L
			R1005	G3	2K	R1019	F4	2L
P910	F3	2L	R1011	F4	1L	R1020	F3	2L
			R1013	F4	2L	R1021	G3	3L
Q1010	F3	2L	R1014	F3	2L	R1023	G4	3L
Q1015	F4	2L	R1015	F4	2L	R1025	F4	3L
			R1016	F3	2L			

Partial A8 also shown on diagrams 1, 9 and 11.

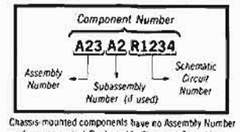
CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J39	A1	CHASSIS	J47	A5	CHASSIS	J49	G1	CHASSIS

A then B Logic & Trigger I/O component locator

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A B C D E F G

1 2 3 4 5 6

VOLTAGE CONDITIONS

PARTIAL A2 LED BOARD

RESET

TRIGEN FROM 8

RESET BUFFER

TRIGGER OUT AMPLIFIER

FD GATE OUT

TRIGGER OUT

A THEN B LOGIC

A THEN B FROM 8

A MODE FROM 8

FNA FROM 8

FNB FROM 8

RSAX TO 6

RSAY TO 6

TRIGGER CONTROL

EXT CLK SYNC FROM 8

EXEDGEN TO 6

EXT CLOCK

EXTERNAL CLOCK JUMPER

ECL

TTL

EXT CLK SLOPE FROM 8

BEXTCLK TO 6

EXT CLOCK INPUT

EXT CLK EXER FROM 8

C632 SEL

TRIGGER VIEW SELECT

TRIG VIEW OUT TO AMP BOARD 4

TO MAIN FRAME

PARTIAL A5 AMPLIFIER BOARD

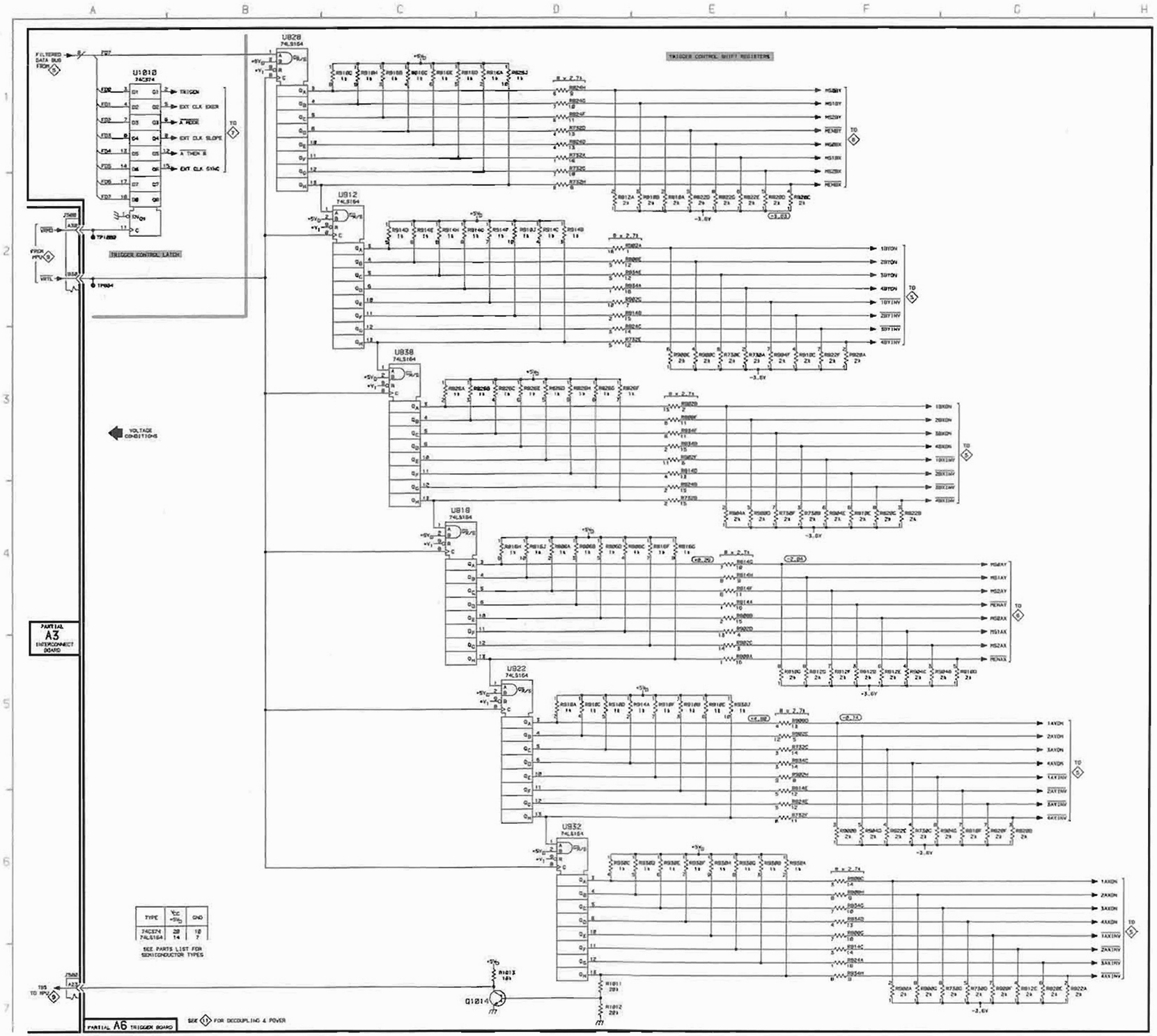
PARTIAL A8 MPU BOARD

PARTIAL A6 TRIGGER BOARD

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

SEE 7 FOR DECOUPLING & POWER

TYPE	V_{CC_1} GND	V_{CC_2} GND	V_{EE} $-5V_D$
10H102	1	16	8
10H104	1	16	8
10H107	1	16	8
10H173	16		8



8 Trigger Control

Reverse Side A8

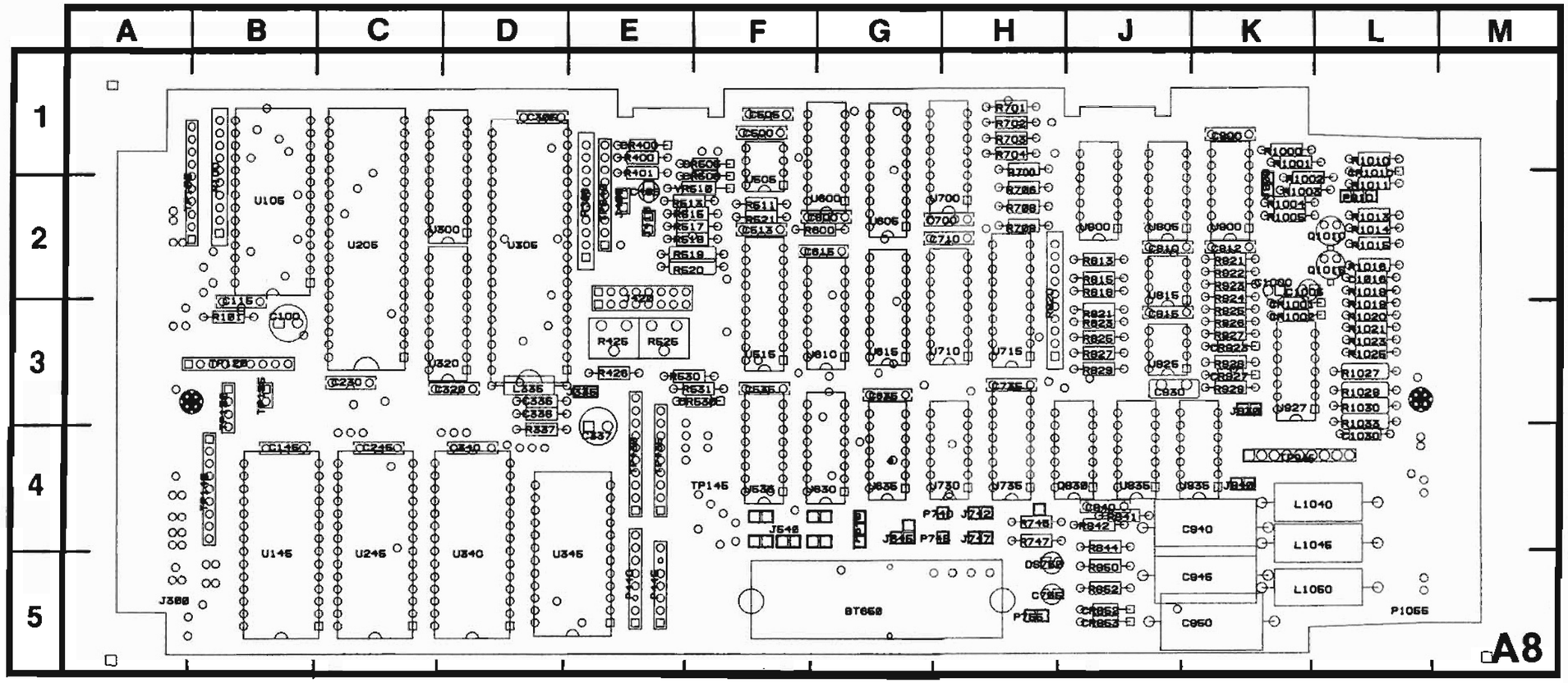
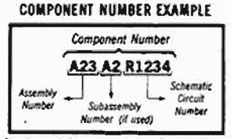


Figure 7-9. A8—MPU circuit board assembly.

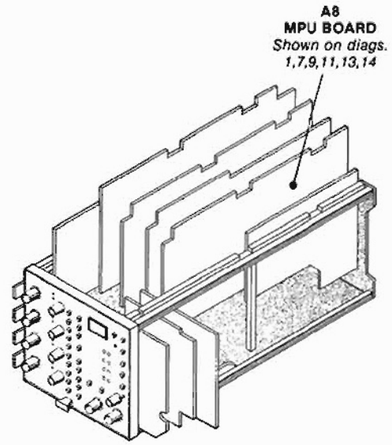
4286-702

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



CPU DIAGRAM 9

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C210	A5	2C	P110	A5	1D	R210	A5	1D
			P260	A5	2B			

Partial A2 also shown on diagrams 1, 3, 4, 5, 6 and 7.

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J100	A5	3A	J300	A5	5B	J300	I5	5B
J300	A2	5B	J300	I1	5B			

Partial A3 also shown on diagrams 1, 3, 4, 5, 6, 8, 11 and 12.

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
BT650	E4	5G	R426	G3	3E	TP640	D4	4G
			R511	H3	2E	TP840	A1	2E
C335	B4	3D	R513	E5	2E	TP840	G2	2E
C336	B4	3D	R515	F5	2E			
C337	B3	3E	R517	F5	2E	U145	D2	4B
C405	H3	1E	R518	B3	2E	U245	D2	4C
C500	E5	1F	R519	E5	2E	U300	D4	2D
C755	F3	5H	R520	E5	2E	U305	B2	2D
C810	G5	2J	R521	H3	2E	U320	E4	3D
C840	E3	4J	R525	E5	3E	U340	D2	4D
C912	G5	2K	R530	E3	3F	U505A	E5	1F
C930	F2	3J	R531	B3	3F	U505B	H4	1F
C1000	H4	2K	R600	E5	2G	U515	B1	3F
C1005	H4	2K	R700	B5	1H	U535	C1	4F
C1030	F3	3L	R701	C5	1H	U600	E5	2G
			R702	C5	1H	U605	F5	2G
CR400	H3	1E	R703	C5	1H	U610	H1	3G
CR505	E5	1F	R704	C5	1H	U615	E2	3G
CR508	E5	1F	R706	B5	1H	U615	E3	3G
CR530	B3	3F	R708	B5	2H	U630	F1	4G
CR852	E3	5J	R709	B5	2H	U635A	A2	4G
CR853	F3	5J	R745	A2	4H	U635B	D4	4G
CR923	F3	3K	R747	A2	4H	U635C	H1	4G
CR927	F3	3K	R813	C5	2J	U635D	D4	4G
CR1001	H4	2K	R815	C5	2J	U700	D5	2H
CR1002	H4	2K	R818	C5	2J	U710	E2	3H
CR1010	B6	1L	R820	E1	2H	U710	E4	3H
			R821	B5	2J	U715	G2	3H
DS750	H2	4H	R823	F3	3J	U730A	C3	4H
			R825	F3	3J	U730B	F4	4H
J335	B4	3E	R827	G2	3J	U730C	F4	4H
J405	H3	2E	R829	G2	3J	U730D	B3	4H
J410	F5	2E	R842	E3	4J	U730F	B3	4H
J420	E1	2E	R844	H2	4J	U735	G1	4H
J540	A2	4F	R850	E3	4J	U800	B5	2J
J645	C3	4G	R852	F3	5J	U805A	F3	2J
J742	E3	4H	R921	H5	2K	U805C	D5	2J
J747	E3	4H	R922	H5	2K	U805D	C3	2J
J900	D5	1K	R923	H4	2K	U815	G6	2J
J930	H4	3K	R924	H4	2K	U825A	F3	3J
J940	G4	4K	R925	H4	2K	U825B	F3	3J
			R926	H4	3K	U825	F3	3J
L335	B4	3D	R927	H4	3K	U835A	G4	4J
			R928	E3	3K	U835B	G4	4J
P740	G3	4H	R929	G4	3K	U900A	H2	2K
P745	G2	4H	R1000	D5	1K	U900B	H4	2K
			R1001	G3	1K	U927A	G4	3K
Q830A	B2	4J	R1002	H3	1K	U927B	G4	3K
Q830B	G2	4J	R1003	H4	1K	U927C	D5	3K
Q830C	E3	4J	R1010	B5	1L	U927D	G4	3K
Q830D	E3	4J	R1027	F3	3L	U935D	C4	4K
			R1029	F3	3L	U935E	F3	4K
R100	G5	1B	R1030	F2	3L	U935F	D5	4K
R300	B1	2E	R1033	F2	3L			
R337	A3	3D				VR510	E5	1F
R400	H3	1E	TP100	F4	1B			
R401	H3	1E	TP430	C2	4E			
R425	E5	3E	TP435	C2	4E			

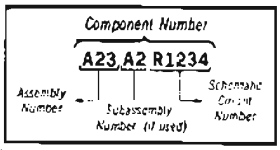
Partial A8 also shown on diagrams 1, 7 and 11.

VOLTAGE CONDITIONS

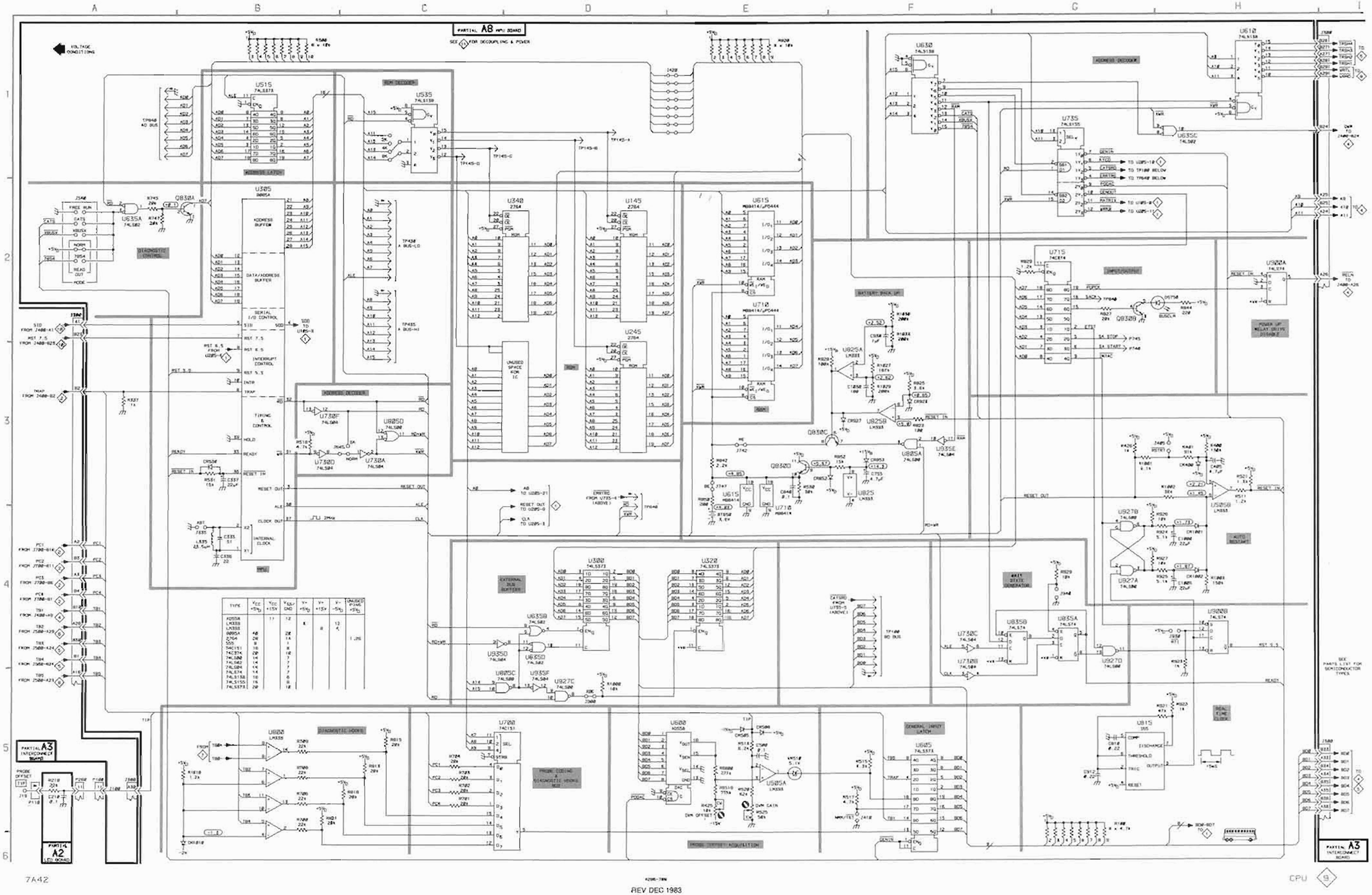
$\overline{\text{ARST}}$ jumper (J405) removed, normal operating mode (see Table 3-7).

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



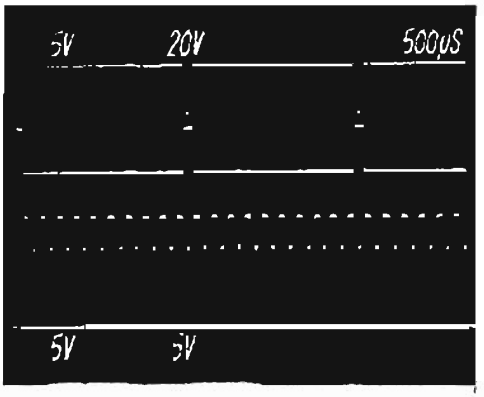
Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List



WAVEFORM CONDITIONS (10)

Use a TEKTRONIX 7704A Oscilloscope with a 7A26 Dual Trace Amplifier and a 7B80 Time Base, or equivalent.

Connect the 7A42 to the host oscilloscope with a flexible extender (Tektronix Part 067-0616-00), then turn on the host oscilloscope and set its Readout control to Off.

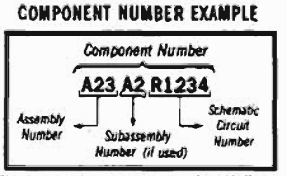


VOLTAGE CONDITIONS (10)

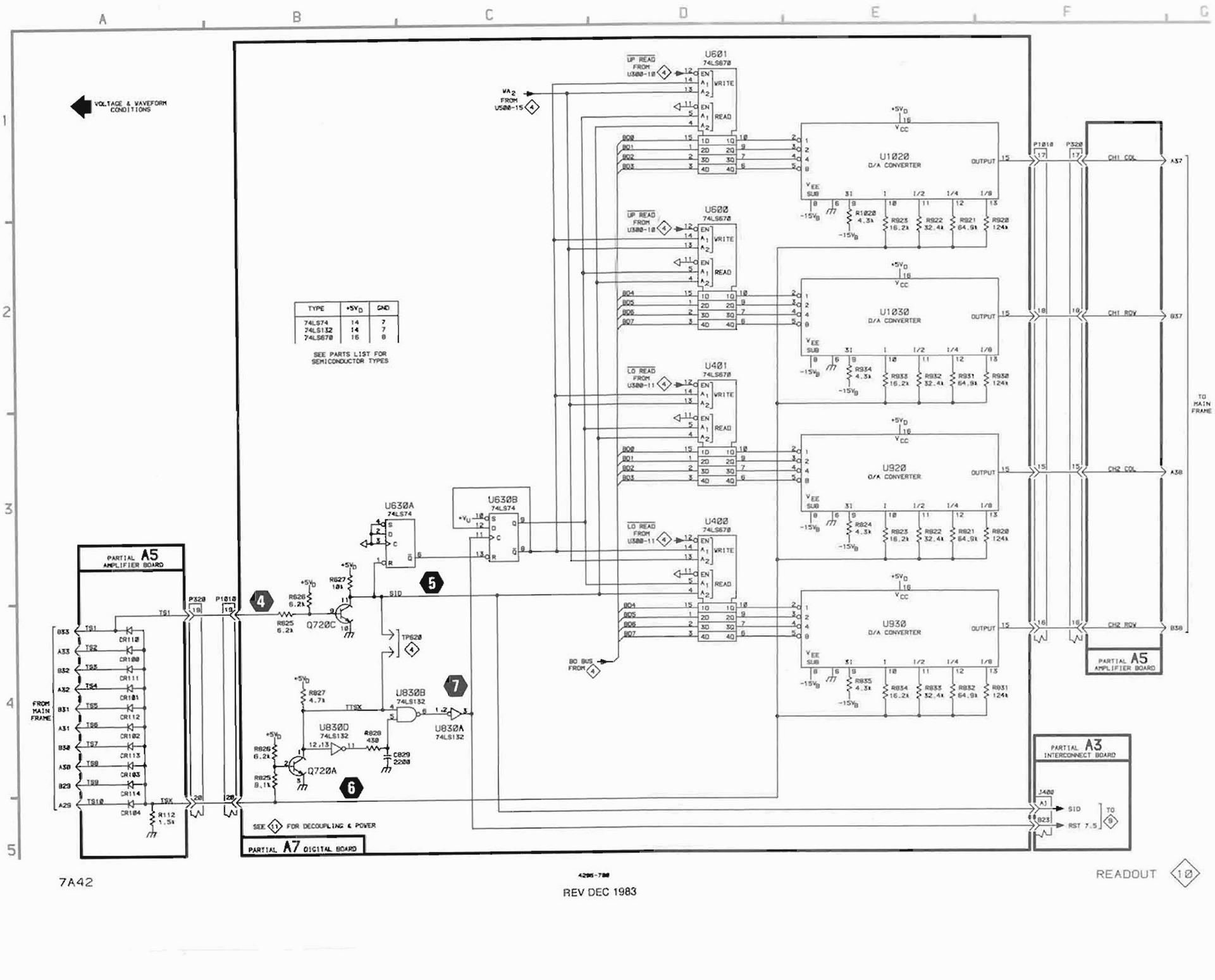
Normal operating mode.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



7A42

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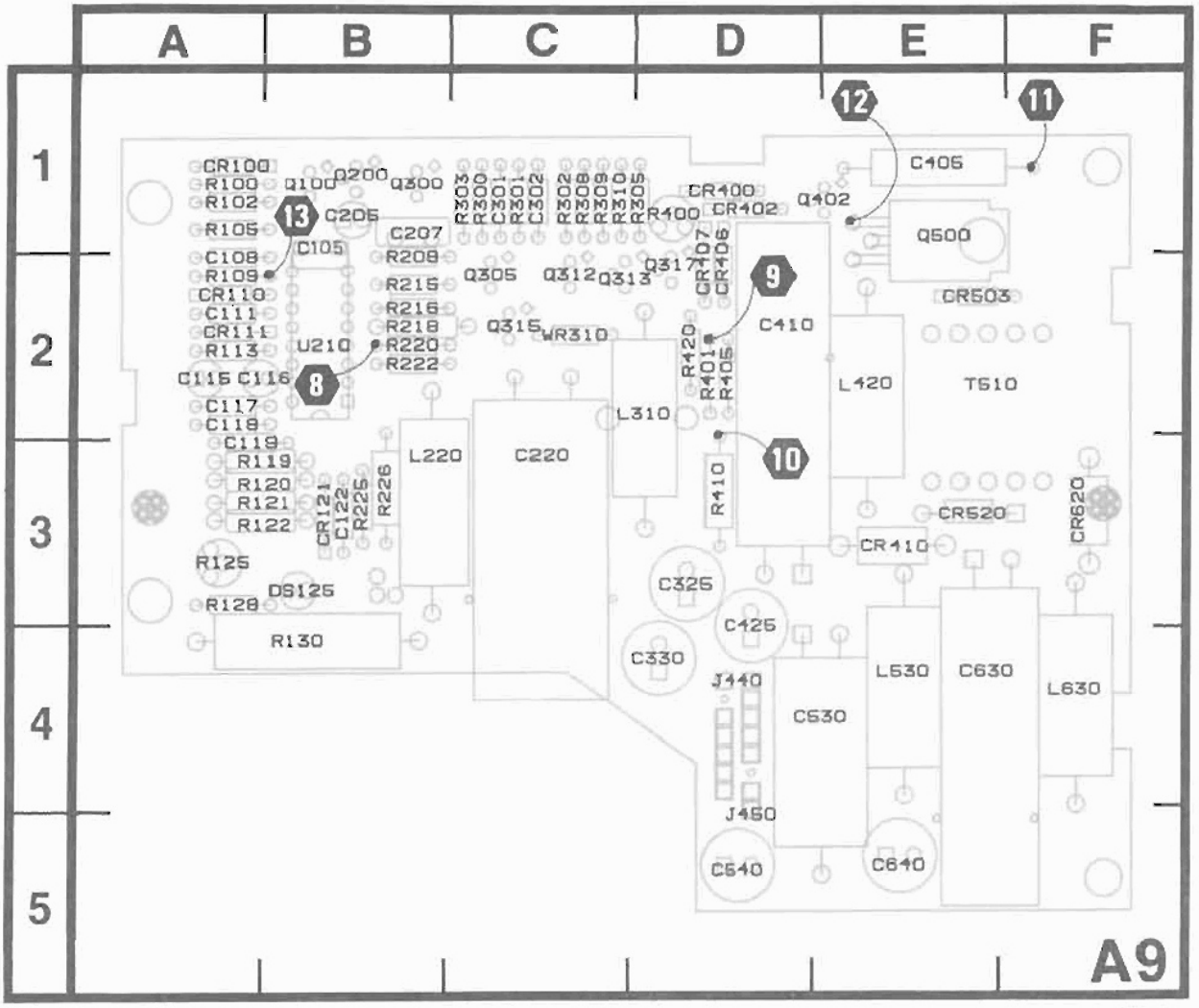
REV DEC 1983

10 Readout
Reverse Side A9



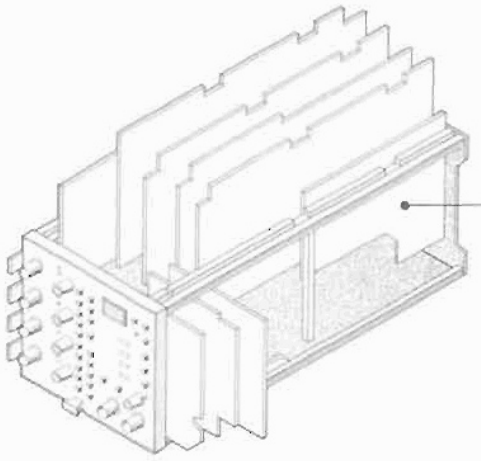
4286-709

Figure 7-10. A9—Power Supply circuit board assembly.

COMPONENT NUMBER EXAMPLE

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



A9
POWER SUPPLY
BOARD
Shown on diags. 11,14

A9-Power Supply circuit bd illustration and locator

POWER SUPPLIES & DISTRIBUTION DIAGRAM 11

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J300	E1	5B	J400	F3	5C	J500	F1	5D	J600	E3	2D	J700	F5	5E

Partial A3 also shown on diagrams 1, 3, 4, 5, 6, 8, 9 and 12.

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C120	C4	3B	C412	C3	2E	P500	E3	1E	R220	D5	3C	R402	E3	1E	U300A	D4	1D
C121	C5	3B	C430	C5	3E				R221	D5	3C	R403	E3	1E	U300B	D3	1D
C203	D4	1C	C530	C5	3E	R200	D4	1B	R300	D3	1C	R410	D4	2D	U300C	E3	1D
C212	D4	2C	C610	E3	2F	R201	E3	1B	R301	D3	1C	R411	D5	2D	U300D	E4	1D
C300	D3	1C	C620	E5	2F	R202	E3	1C	R310	D5	2C	R420	D5	3D	U310A	D5	2D
C310	D5	2C				R203	D4	1C	R320	E3	3C	R421	D4	3D	U310B	D5	2D
C360	C4	5D	L120	C5	2B	R204	D3	1C	R321	D4	3D	R422	D4	3D	U310C	D5	2D
C400	E4	1D	L121	C5	2B	R205	D3	1C	R322	D5	3C	R423	D5	3D	U310D	D4	2D
C403	E3	1E	L220	C5	3C	R211	D5	2C	R323	D5	3D						
C410	D5	2D	L260	C4	5C	R212	D5	2C	R400	D4	1D	TP200	E4	1C			
C411	D5	2D	L420	E6	2E	R213	D4	2C	R401	E4	1D	TP400	E3	1E			

Partial A5 also shown on diagrams 3, 4, 7 and 10.

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	F2	2B	C301	G3	1D	C500	G3	1E	C722	F1	4G	C1021	G1	3L	R806F	F1	2J
C120	F3	3B	C330	G2	5C	C530	G3	4F	C800	G3	2H						
C213	G2	2C	C331	G3	5D	C600	G2	1F	C830	G1	4J	CR723	F3	4G	TP800	F2	1H
C223	G2	3C	C400	G2	1E	C630	G2	5F	C901	F3	1J				TP801	G3	1H
C233	G2	4C	C411	G2	3D	C711	G1	3G	C910	G1	2K	R736	F3	5H	TP802	G2	1H
C300	G2	1C	C430	G2	5D	C721	F3	4H	C1020	G1	3K	R806E	F1	2J	TP803	G1	1H

Partial A6 also shown on diagrams 5, 6, 7 and 8.

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C200	F4	1C	C420	F5	4D	C521	G4	4F	C710	G4	2H	C830	G4	5H	R332	F4	4C
C410	G4	2D	C421	F5	4E	C610	G4	2F	C800	G4	1J	C926	G4	4J	R600	F4	2G
C411	G4	2E	C520	F4	4E	C611	F5	2G	C810	F5	2H	C1030	G4	5K			

Partial A7 also shown on diagrams 1, 2, 4 and 10.

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C145	E1	3B	C513	E1	2E	C735	E1	3H	L1040	A5	4L	R841	E1	4J	TP945	A5	4K
C230	E1	3C	C535	E1	3F	C815	E1	2J	L1045	A4	4L				TP945	E1	4K
C245	E1	3C	C600	E1	2G	C900	E1	1K	L1050	A4	5L	TP945	A4	4K	TP945	E1	4K
C305	E1	1D	C615	E1	2G	C940	A4	4K				TP945	A4	4K	TP945	E1	4K
C320	E1	3D	C635	E1	3G	C945	A5	5K	P440	D1	5E	TP945	A4	4K			
C340	E1	3D	C700	E1	2H	C950	A4	5K	P445	B3	5E	TP945	A4	4K			
C505	A4	1F	C710	E1	2H							TP945	A5	4K			

Partial A8 also shown on diagrams 1, 7 and 9.

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C105	A1	1B	C405	C1	1E	CR503	D1	2E	Q313	C2	2C	R128	D2	3A	R309	C2	1C
C108	A2	2A	C410	D1	2D	CR520	D1	3E	Q315	C1	2C	R130	D2	4B	R310	C2	1C
C111	B3	2A	C425	D1	4D	CR620	D1	3F	Q317	C2	2D	R208	B2	1B	R400	C2	1D
C115	B2	2A	C530	D1	4D				Q402	C1	1D	R215	C1	2B	R401	C2	2D
C116	B3	2A	C540	D1	5D	DS125	D2	3B	Q500	D1	1E	R216	C1	2B	R405	C2	2D
C117	B3	2A	C630	D1	4E							R218	A1	2B	R410	D2	3D
C118	B1	2A	C640	D1	5E	L310	C1	2D	R100	C2	1A	R220	B1	2B	R420	C1	2D
C119	A1	3A				L420	D1	2E	R102	B2	1A	R222	B1	2B	R500	B4	1E
C122	C2	3B	CR100	C2	1A	L530	D1	4E	R105	B2	1A	R225	C2	3B			
C205	B3	1B	CR111	B2	2A	L630	D1	4F	R109	A2	1A	R226	C2	3B	T510	D1	2E
C207	C2	1B	CR121	C1	3A				R113	B2	2A	R300	B2	1C			
C220	B3	3C	CR400	C1	1D	Q100	B2	1B	R119	A1	3A	R301	C1	1C	U210	A1	2B
C301	C1	1C	CR402	C1	1D	Q200	B2	1B	R120	A1	3A	R302	C2	1C			
C302	C2	1C	CR406	C2	2D	Q300	B2	1B	R121	A1	3A	R303	B2	1C	W310	C1	2C
C325	B3	4D	CR407	C2	2D	Q305	C1	2C	R122	A2	3A	R305	C2	1D			
C330	B4	4D	CR410	D1	3E	Q312	C2	2C	R125	A2	3A	R308	C2	1C			

VOLTAGE CONDITIONS (11)

Use a digital voltmeter with a 10 MΩ input impedance, such as the TEKTRONIX DM 501A Digital Multimeter installed in a TM 500 or TM 5000-series power module, or a TEKTRONIX 7D13A Digital Multimeter installed in a readout-equipped Tektronix 7000-series oscilloscope.

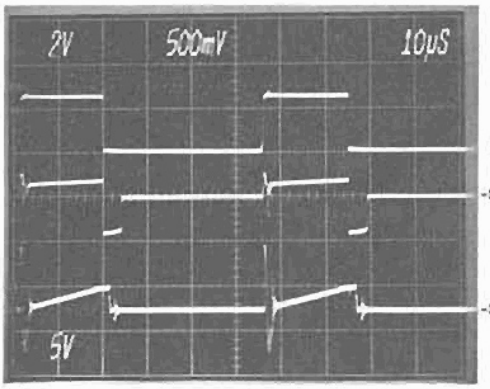
Connect the 7A42 to the host oscilloscope with a flexible extender (Tektronix Part 067-0616-00), then set the 7A42 to power-up default by removing and replacing A8P747. (Link-plug A8P747 is located on the A8 MPU Board.) Then turn on the host oscilloscope.

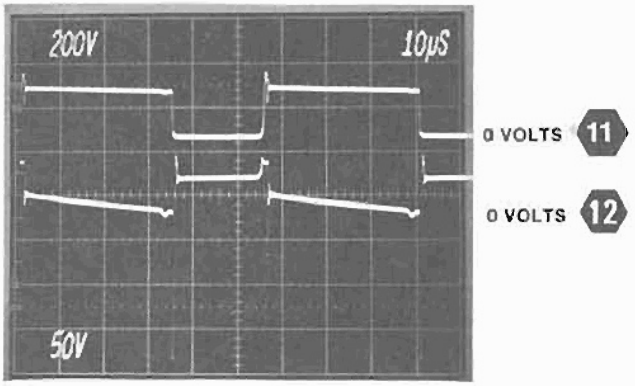
WAVEFORM CONDITIONS

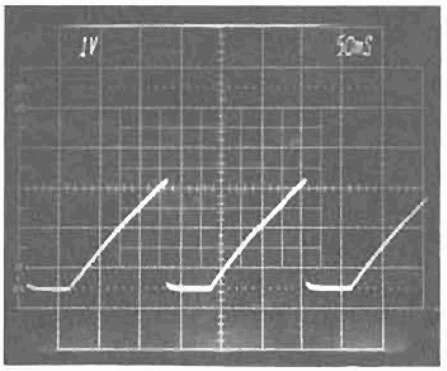
Use a TEKTRONIX 7704A Oscilloscope with a 7A26 Dual Trace Amplifier and a 7B80 Time Base, or equivalent.

For waveforms 1 through 5, connect the 7A42 to the host oscilloscope with a flexible extender (Tektronix Part 067-0616-00), then set the 7A42 to power-up default by removing and replacing A8P747. (Link-plug A8P747 is located on the A8 MPU Board.) Then turn on the host oscilloscope.

For waveform 6, set A9P230 to Aux Load position, oriented vertically. (The A9P230 link-plug is located on the A9 Power Supply Board.)

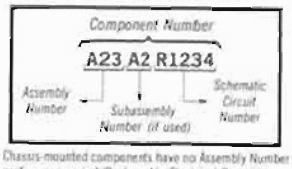






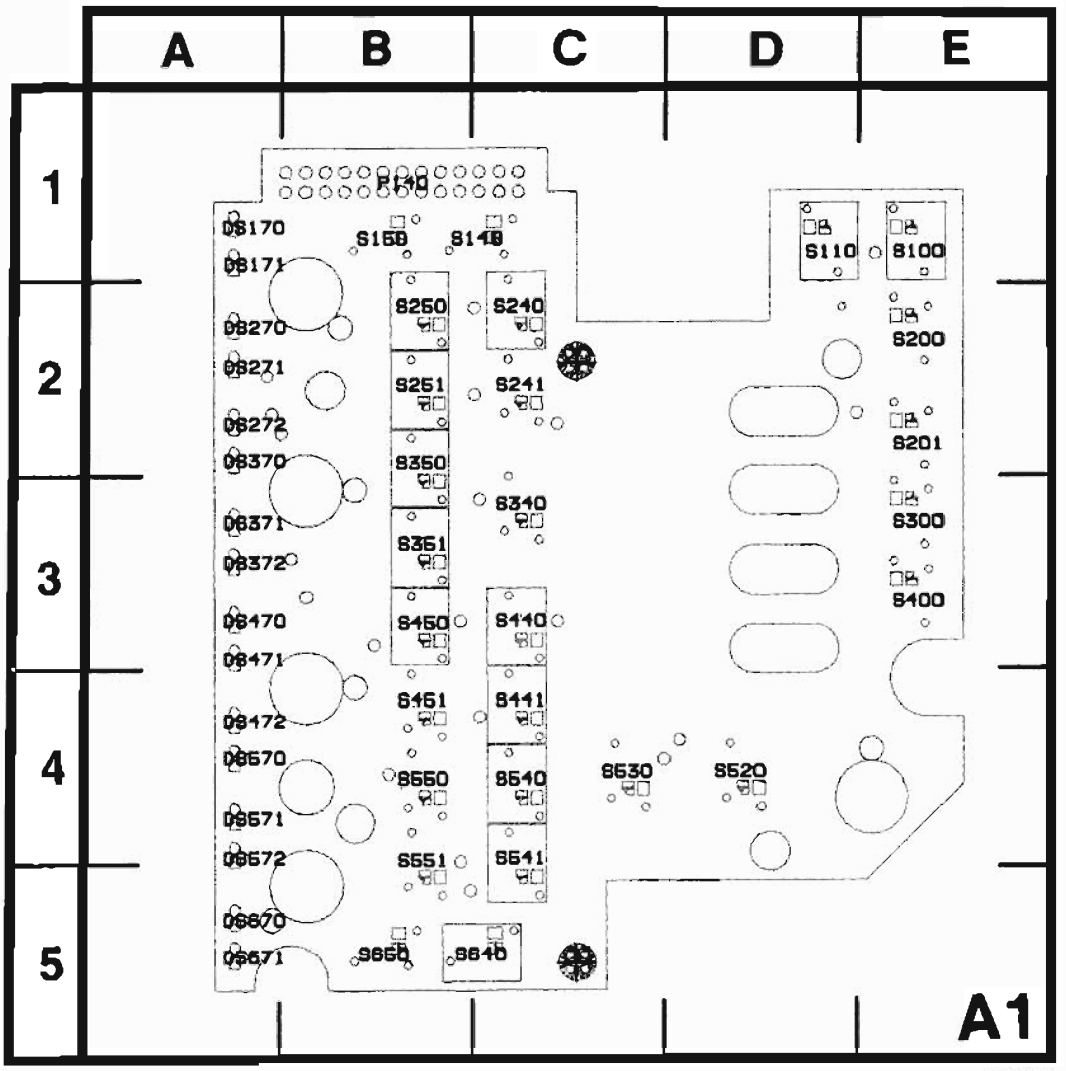
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

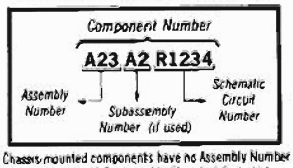
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.



4286-703

Figure 7-3. A1—Switch circuit board assembly.

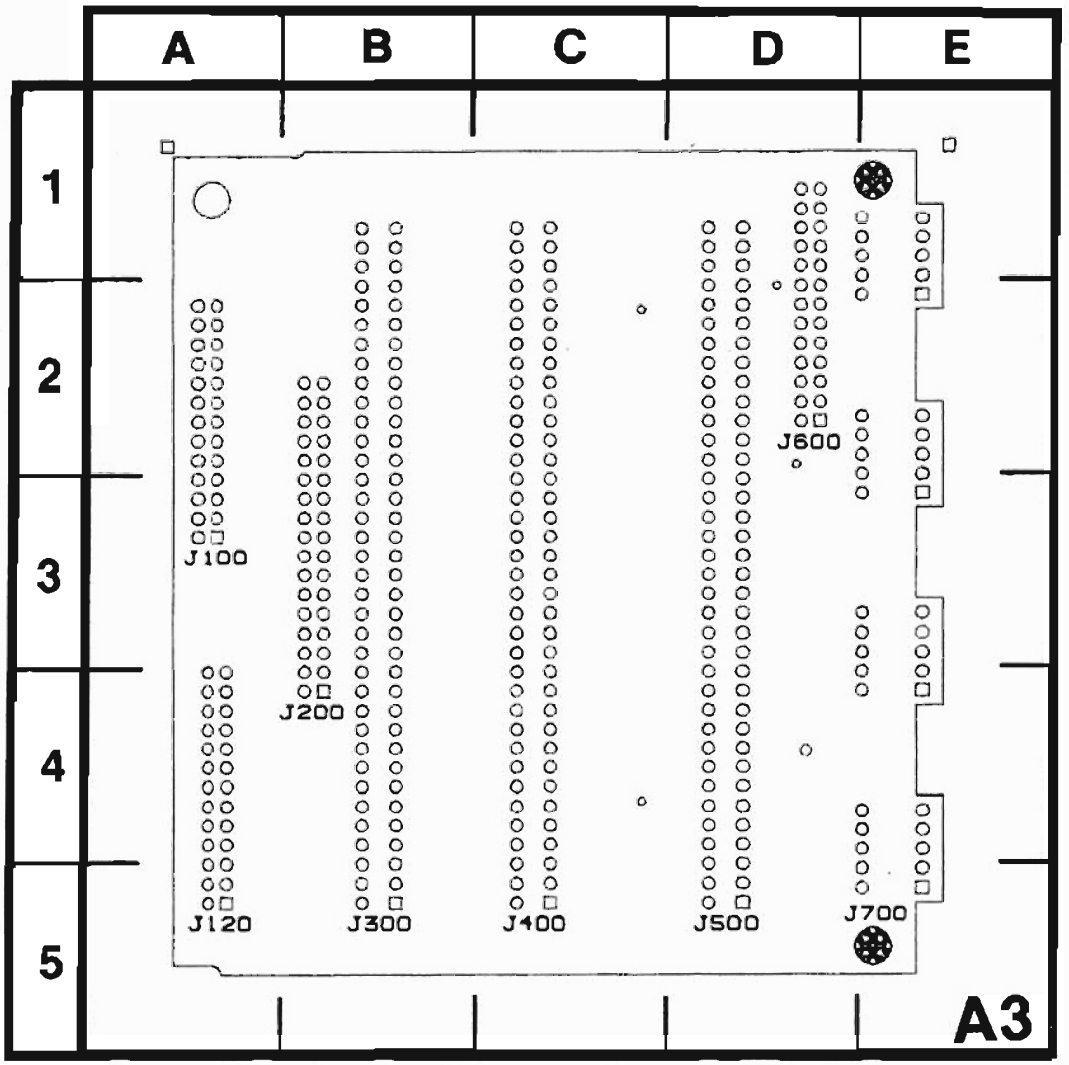
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

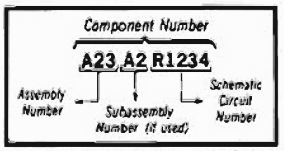
A3-Interconnect circuit bd illustration and locator



4286-710

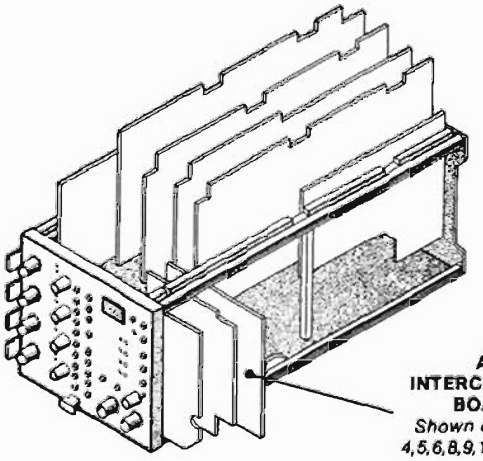
Figure 7-11. A3—Interconnect circuit board assembly.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



A3 INTERCONNECT BOARD
Shown on diags. 4,5,6,8,9,10,11,12,14

INTERCONNECT DIAGRAM 12

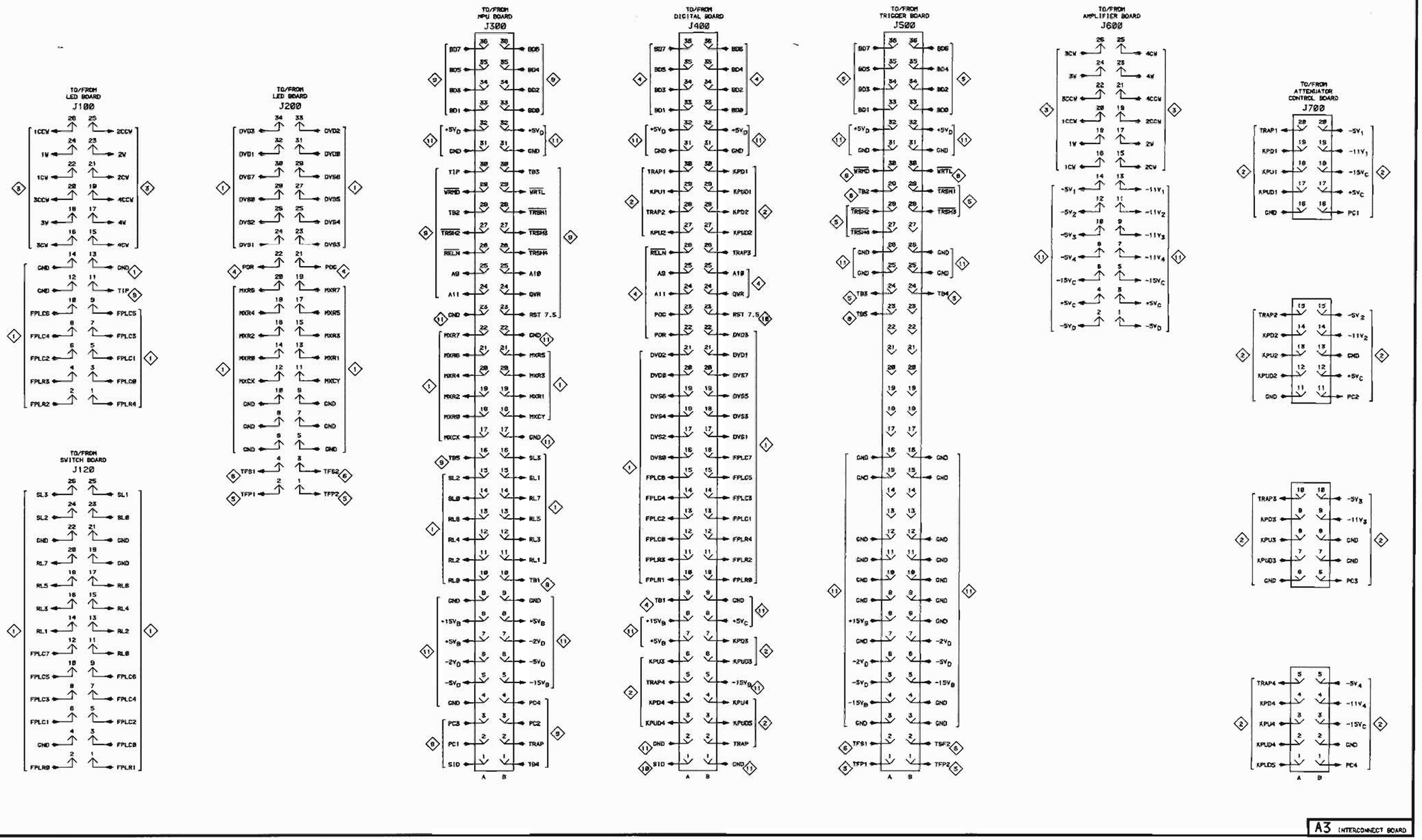
ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	
J100	A1	3A	
J120	A3	5A	
J200	B1	4B	
J300	C1	5B	
J400	D1	5C	
J500	E1	5D	
J600	F1	2D	
J700	F1	5E	

Partial A3 also shown on diagrams 1, 3, 4, 5, 6, 8, 9 and 11.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION
C10	2	E5
C20	2	E3
C30	2	E2
C40	2	E1
J10	2	E5
J19	9	A5
J20	2	E3
J30	2	E2
J39	7	A1
J40	2	E1
J47	7	A5

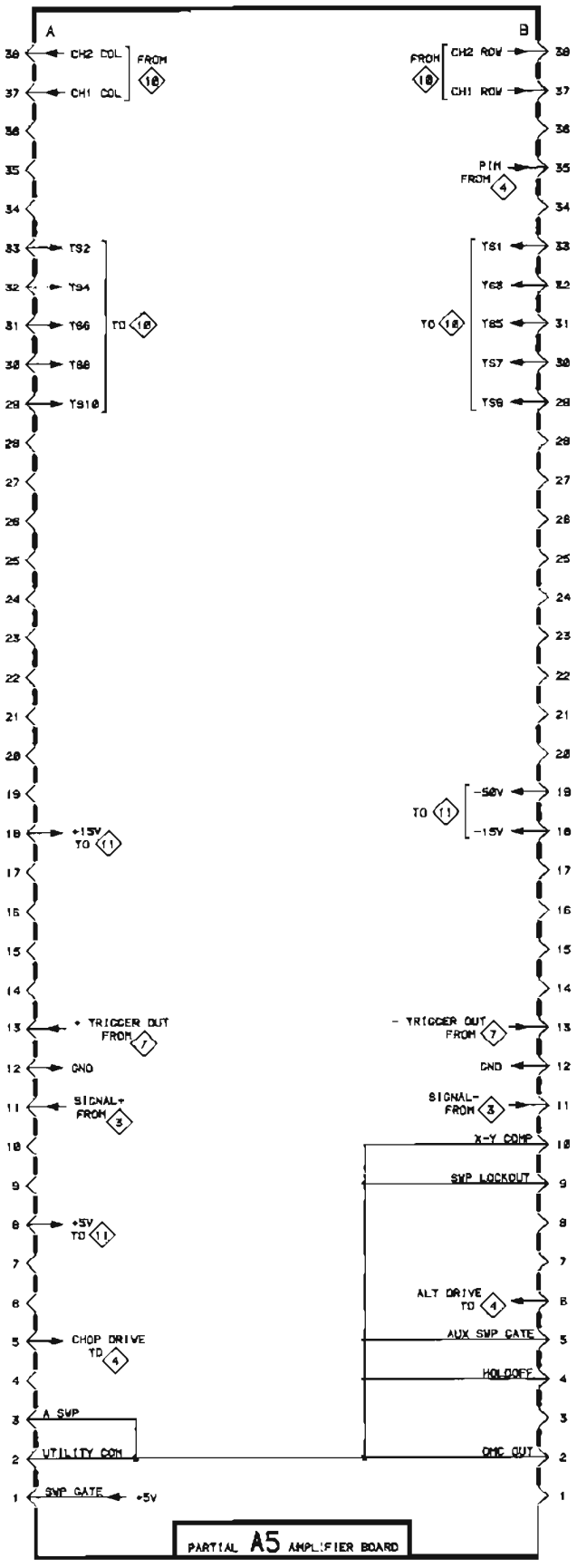


12 Interconnect

Reverse Side Locator 13

A3 INTERCONNECT BOARD

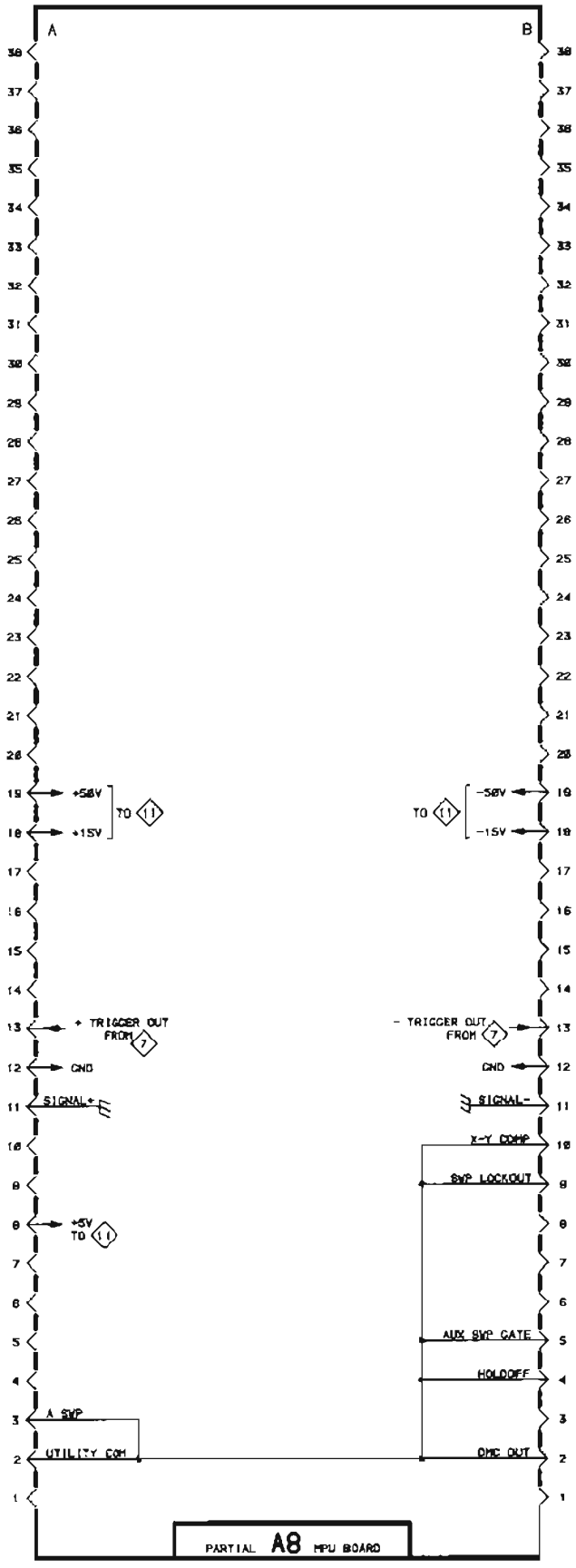
VIEWED FROM INSTRUMENT FRONT



7A42

4286-783

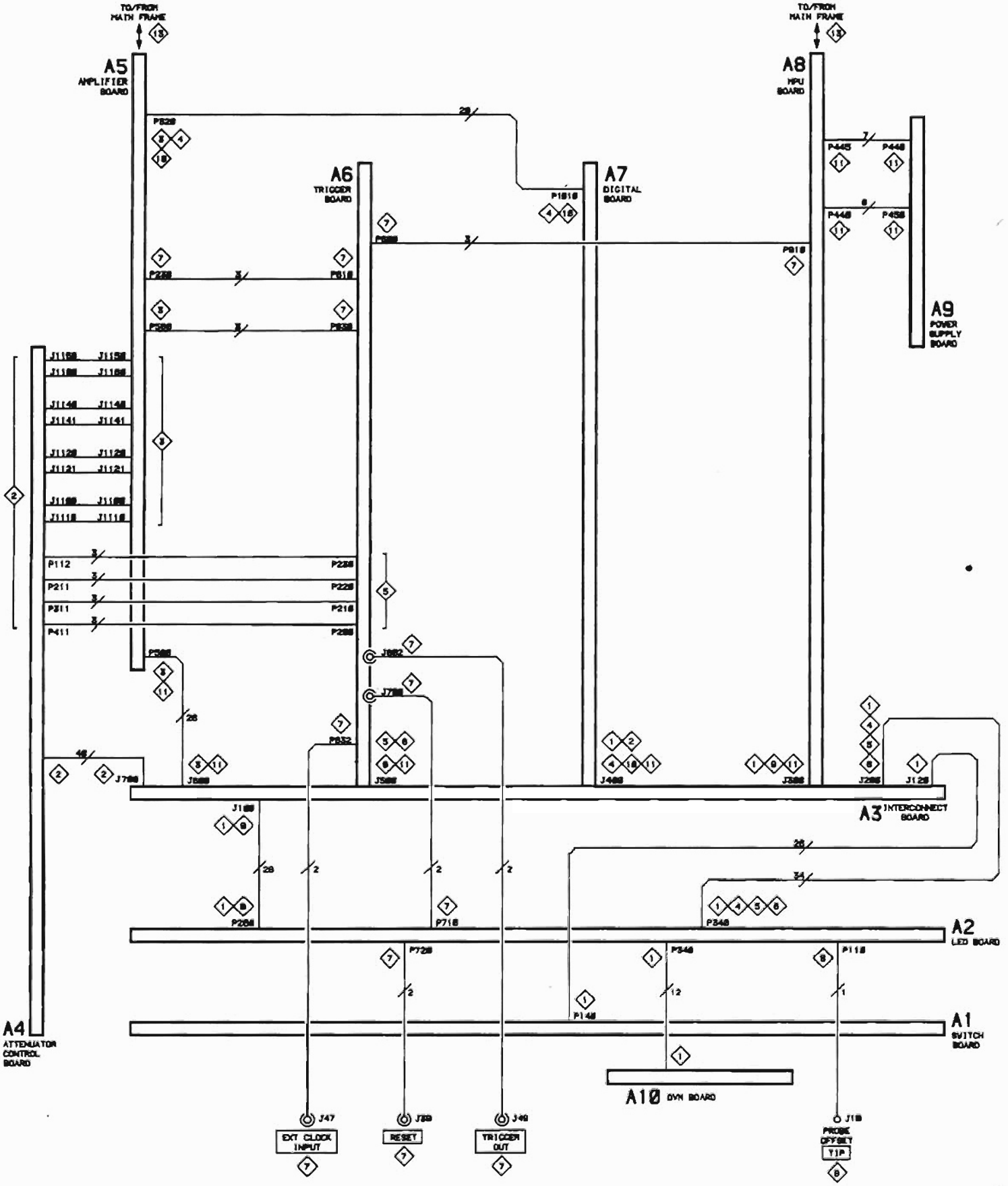
EWED FROM INSTRUMENT FRONT



CONNECTORS TO MAINFRAME 13

13 Connectors to Mainframe

86-703



REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
06383	PANDUIT CORP	17301 RIDGELAND	TINLEY PARK IL 07094-2917
09772	WEST COAST LOCKWASHER CO INC	16730 E JOHNSON DRIVE P O BOX 3588	CITY OF INDUSTRY CA 91744
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
12327	FREEWAY CORP	9301 ALLEN DR	CLEVELAND OH 44125-4632
13103	THERMALLOY CO INC	2021 W VALLEY VIEW LN PO BOX 810839	DALLAS TX 75381
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS DIV MILITARY PRODUCTS GROUP	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
73743	FISCHER SPECIAL MFG CO	111 INDUSTRIAL RD	COLD SPRING KY 41076-9749
74445	HOLO-KROME CO	31 BROOK ST	ELMWOOD CT 06110-2350
75915	LITTELFUSE TRACTOR INC SUB TRACTOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016-3049
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIV	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500 MS 53-111	BEAVERTON OR 97707-0001
83385	MICRODOT MFG INC GREER-CENTRAL DIV	3221 W BIG BEAVER RD	TROY MI 48098
83486	ELCO INDUSTRIES INC	1101 SAMUELSON RD	ROCKFORD IL 61101
85471	BOYD CORP	13885 RAMONA AVE	CHINO CA 91710
86928	SEASTROM MFG CO INC	701 SONORA AVE	GLENDALE CA 91201-2431
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61108-5181
98159	RUBBER TECK INC	19115 HAMILTON AVE PO BOX 389	GARDENA CA 90247
TK0171	ZEPHER ELECTRONICS	647 INDUSTRY DRIVE	SEATTLE WA 98188
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609-3320
TK0456	ARROW FASTERNERS INC	2112 AMERICAN AVE	HAYWARD CA 94545
TK1326	NORTHWEST FOURSLIDE INC	18224 SW 100TH CT	TUALATIN OR 97062
TK1465	BEAVERTON PARTS MFG CO	1800 NW 216TH AVE	HILLSBORO OR 97124-6629

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	337-1064-12			2	SHIELD,ELEC:SIDE FOR PLUG-IN UNIT	80009	337-1064-12
-2	366-1833-01			4	KNOB:DOVE GRAY,0.25 ID X 0.392 OD X 0.466 H	80009	366-1833-01
-3	366-2041-01			1	KNOB:GY,BAR,0.172 ID X 0.41 OD X0.496 H	80009	366-2041-01
-4	358-0378-00			1	BUSHING,SLEEVE:0.131 ID X 0.18 OD X 0.125 L	80009	358-0378-00
-5	333-2903-00			1	PANEL,FRONT:	80009	333-2903-00
					(ATTACHING PARTS)		
-6	210-0406-00			2	NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
					(END ATTACHING PARTS)		
-7	348-0235-00			2	SHLD GSKT,ELEK:FINGER TYPE,4.734 L	80009	348-0235-00
-8	386-4820-00			1	SUBPANEL,FRONT:	80009	386-4820-00
					(ATTACHING PARTS)		
-9	211-0541-00			8	SCREW,MACHINE:6-32 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-10	377-0512-00			5	INSERT,KNOB:0.125 ID X 0.247 OD X 0.663,AL	80009	377-0512-00
-11	----- -----			1	JACK TIP:(SEE J19 REPL)		
-12	195-1332-00			2	LEAD,ELECTRICAL:26 AWG,1.5 L,9-1	80009	195-1332-00
					(J39 TO A2P720;J19 TO A2P118)		
-13	131-0707-00			2	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-14	352-0171-00			2	.HLDR,TERM CONN:1 WIRE,BLACK	80009	352-0171-00
-15	----- -----			1	CONN:(SEE J39 REPL)		
-16	----- -----			2	CONN,BNC:(SEE J47,J49 REPL)		
					(ATTACHING PARTS)		
-17	220-0495-00			2	NUT,PLAIN,HEX:0.375-32 X 0.438 HEX,BRS	73743	ORDER BY DESCR
-18	210-0012-00			2	WASHER,LOCK:0.384 ID,INTL,0.022 THK,STL	09772	ORDER BY DESCR
					(END ATTACHING PARTS)		
-19	426-1899-00			1	FR SECT,PLUG-IN:LOWER LEFT	80009	426-1899-00
					(ATTACHING PARTS)		
-20	213-0793-00			2	SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FILH	83486	239-006-406043
					(END ATTACHING PARTS)		
-21	----- -----			1	CKT BOARD ASSY:SWITCH(SEE A1 REPL)		
-22	----- -----			1	CKT BOARD ASSY:DVM(SEE A10 REPL)		
-23	----- -----			1	CKT BOARD ASSY:LED(SEE A2 REPL)		
					(ATTACHING PARTS)		
-24	210-0940-00			5	WASHER,FLAT:0.25 ID X 0.375 OD X 0.02,STL	12327	ORDER BY DESCR
-25	210-0583-00			5	NUT,PLAIN,HEX:0.25-32 X 0.312,BRS CD PL	73743	2X-20319-402
-26	211-0018-00			4	SCREW,MACHINE:4-40 X 0.875,PNH,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
					LED BOARD INCLUDES:		
-27	136-0263-07	B010100	B010624	13	.SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
	136-0263-04	B010625		13	.SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	75377-001
-28	361-0976-00			4	.SPACER,STEPPED:0.56 L X 0.14-0.125 ID BRS	80009	361-0976-00
-29	220-0932-00			1	NUT BLOCK:4-40,0.625 X 0.5 X 0.25,AL	80009	220-0932-00
					(ATTACHING PARTS)		
-30	211-0038-00			2	SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-31	----- -----			1	CKT BOARD ASSY:INTERCONNECT(SEE A3 REPL)		
					(ATTACHING PARTS)		
-32	211-0008-00			1	SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-33	214-1061-00			1	CONTACT,ELEC:GROUNDING,CU BE	80009	214-1061-00
-34	426-1896-00			1	FR SECT,PLUG-IN:UPPER LEFT	80009	426-1896-00
					(ATTACHING PARTS)		
-35	213-0793-00			2	SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FILH	83486	239-006-406043
					(END ATTACHING PARTS)		
-36	210-0288-00			3	TERM,LUG:0.125 ID,PLAIN,CU BE,CU-SN-ZN PL	80009	210-0288-00
					(ATTACHING PARTS)		
-37	211-0025-00			3	SCREW,MACHINE:4-40 X 0.375,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
-38	210-0406-00			3	NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
-39	210-0994-00			3	WASHER,FLAT:0.125 ID X 0.25 OD X 0.022,STL	86928	A371-283-20
					(END ATTACHING PARTS)		
-40	220-0923-00			2	NUT BLOCK:4-40 X 0.4 L X 0.375 SQ,	80009	220-0923-00
					(ATTACHING PARTS)		
-41	211-0016-00			2	SCREW,MACHINE:4-40 X 0.625,PNH,STL	TK0435	ORDER BY DESCR
-42	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					(END ATTACHING PARTS)		
-43	200-0929-00			1	COV,TEST ADPTR:TO-66 XSTR,PLASTIC	80009	200-0929-00
					(ATTACHING PARTS)		
-44	211-0101-00			4	SCREW,MACHINE:4-40 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-					(END ATTACHING PARTS)		
-45	----- -----			4	ATTENUATOR:(SEE AT10,AT20,AT30,AT40 REPL)		
					(ATTACHING PARTS)		
-46	211-0335-00			4	SCREW,CAP:4-40 X 1.06,HEX SCH,STL CD PL	TK0456	ORDER BY DESCR
-47	211-0198-00			4	SCREW,MACHINE:4-40 X 0.438,PNH,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
					ATTENUATOR ASSY INCLUDES:		
-48	200-2777-00			4	.COVER,ATTEN:ALUMINUM	TK1465	
					.(ATTACHING PARTS)		
-49	211-0022-00			16	.SCREW,MACHINE:2-56 X 0.188,PNH,STL	TK0435	ORDER BY DESCR
					.(END ATTACHING PARTS)		
-50	348-0759-00			4	.PAD,PRESSURE:2.15 L X 0.3 W X 0.188 THK	85471	R10470 FIRM
-51	----- -----			1	CKT BOARD ASSY:ATTEN CONTROL(SEE A4 REPL)		
-52	136-0252-07			80	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-53	----- -----			1	CKT BOARD ASSY:AMPLIFIER(SEE A5 REPL)		
-54	136-0252-07			60	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-55	136-0263-07			8	.SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
-56	344-0286-00			8	.CLIP,ELECTRICAL:FUSE,SPR BRS	75915	102074
-57	136-0763-00			3	.SKT,PL-IN ELEK:26 LINE CONT IMPD HYBRID	00779	ORDER BY DESCR
	129-0656-00			4	.SPCR,POST:0.288 L,4-40 ONE END,BRS,0.25 OD	80009	129-0656-00
-58	----- -----			3	.MICROCIRUIT:(SEE U240,U600,U640 REPL)		
					.(ATTACHING PARTS)		
-59	210-0406-00			9	.NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
					.(CAREFULLY TORQUE TO 3 1/2-4 IN/LBS)		
-60	129-0553-00			3	.SPACER,POST:0.41 L,4-40,BRS,0.188 HEX	80009	129-0553-00
					.(END ATTACHING PARTS)		
-61	346-0121-00			3	STRAP,TIEDOWN,E:6.125 L,NYLON	06383	PLC1.5I-S8
					(TIE WRAP IS PART OF DELAY LINE)		
					(ATTACHING PARTS)		
-62	211-0097-00			3	SCREW,MACHINE:4-40 X 0.312,PNH,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-63	384-1112-08			1	EXTENSION SHAFT:10.975 L X 0.188 OD,PLASTIC	80009	384-1112-08
-64	376-0029-00			1	CPLG,SHAFT,RGD:0.128 ID X 0.312 OD,AL	80009	376-0029-00
-65	213-0075-00			2	.SETSCREW:4-40 X 0.094,STL	74445	ORDER BY DESCR
-66	----- -----			1	CKT BOARD ASSY:TRIG SHIELD,BACK		
					(SEE A6A2 REPL)		
					(ATTACHING PARTS)		
-67	211-0008-00			2	SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-68	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					(END ATTACHING PARTS)		
					TRIG SHIELD BOARD INCLUDES:		
-69	136-0263-07			23	.SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
-70	386-1635-00			7	.SUPPORT,CKT BD:CHASSIS MT,ACETAL	80009	386-1635-00
-71	195-0714-00			2	.LEAD,ELECTRICAL:18 AWG,2.0 L,5-4	80009	195-0714-00
-72	210-0201-00			2	.TERMINAL,LUG:0.12 ID,LOCKING,BRZ TIN PL	86928	A373-157-2
-73	----- -----			1	CKT BOARD ASSY:TRIGGER(SEE A6A1 REPL)		
-74	131-0993-00			2	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-75	136-0252-07			2	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-76	131-2441-00			23	.TERMINAL,PIN:1.0 L X 0.025 SQ,BRASS	22526	47799
-77	----- -----			1	CKT BOARD ASSY:TRIG SHLD,FR(SEE A6A3 REPL)		
-78	386-1559-00			7	.SPACER,CKT BD:0.47 H,ACETAL	80009	386-1559-00
-79	136-0263-07			23	.SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORDER BY DESCR
-80	----- -----			1	CKT BOARD ASSY:DIGITAL(SEE A7 REPL)		
-81	131-0993-00			1	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-82	136-0752-00			1	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-83	----- -----			1	CKT BOARD ASSY:MPU(SEE A8 REPL)		
-84	131-0993-00			15	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-85	136-0755-00			3	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-86	----- -----			1	.BATTERY:(SEE BT650 REPL)		
					.(ATTACHING PARTS)		
-87	346-0032-00			1	.STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2829-75-4
					.(END ATTACHING PARTS)		
-88	407-2889-00			1	BRACKET,ANGLE:POWER SUPPLY,AL	80009	407-2889-00
					(ATTACHING PARTS)		
-89	211-0198-00			2	SCREW,MACHINE:4-40 X 0.438,PNH,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-90	361-0340-00			2	SPACER,SLEEVE:0.22 L X 0.12 ID,BRS	80009	361-0340-00
-91	----- -----			1	CKT BOARD ASSY:POWER SUPPLY(SEE A9 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-					(ATTACHING PARTS)		
-92	211-0008-00			2	SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
					POWER SUPPLY BOARD INCLUDES:		
-93	----- -----			1	.TRANSISTOR:(SEE Q500 REPL)		
					.(ATTACHING PARTS)		
-94	211-0008-00			1	.SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-95	210-1178-00			1	.WASHER,SHLDR:	13103	7721-7PPS
-96	210-0586-00			1	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					.(END ATTACHING PARTS)		
-97	----- -----			3	.CAPACITOR:(SEE C220,C410,C630 REPL)		
					.(ATTACHING PARTS)		
-98	346-0032-00			3	.STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2829-75-4
					.(END ATTACHING PARTS)		
-99	131-0993-00			1	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-100	129-0966-00			1	SPCR,POST:4.496 4-40 INT ENDS,AL,0.25HEX	80009	129-0966-00
					(ATTACHING PARTS)		
-101	211-0198-00			2	SCREW,MACHINE:4-40 X 0.438,PNH,STL	TK0435	ORDER BY DESCR
-102	211-0101-00			1	SCREW,MACHINE:4-40 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
-103	211-0025-00			1	SCREW,MACHINE:4-40 X 0.375,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-104	426-1895-00			1	RF SECT,PLUG-IN:LOWER RIGHT	80009	426-1895-00
					(ATTACHING PARTS)		
-105	213-0793-00			2	SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FILH	83486	239-006-406043
					(END ATTACHING PARTS)		
-106	214-1054-00			2	SPRING,FLAT:0.825 X 0.322,SST	TK1326	ORDER BY DESCR
-107	214-3386-00			1	SPRING,HLEXT:0.156 OD X 2.5 L,XLOOP,MUW	80009	214-3386-00
-108	214-3286-01			1	CATCH,LEVER:LATCH,PLASTIC	80009	214-3286-01
-109	105-0922-00			1	RELEASE,LATCH:PLUG-IN UNIT	80009	105-0922-00
-110	366-2023-00			1	KNOB:GRAY,0.62 X 0.255 X 0.35 H	80009	366-2023-00
-111	386-4848-00			3	SUPPORT,CKT BD:LOWER	80009	386-4848-00
					(ATTACHING PARTS)		
-112	211-0101-00			3	SCREW,MACHINE:4-40 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
-113	211-0038-00			3	SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-114	426-1897-00			1	FR SECT,PLUG-IN:UPPER RIGHT	80009	426-1897-00
					(ATTACHING PARTS)		
-115	213-0793-00			2	SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FILH	83486	239-006-406043
-116	361-0326-00			1	SPACER,SLEEVE:0.1 L X 0.18 ID,AL	80009	361-0326-00
					(END ATTACHING PARTS)		
-117	386-4818-00			2	SUPPORT,CKT BD:UPPER,NYLON 6/6	80009	386-4818-00
					(ATTACHING PARTS)		
-118	211-0038-00			2	SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
-119	210-0586-00			4	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-120	211-0101-00			2	SCREW,MACHINE:4-40 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-121	351-0217-00	B010100	B011034	2	GUIDE,CKT BOARD:SIL GRAY DELRIN,4.7 L	80009	351-0217-00
	386-5467-00	B011035		2	GUIDE,CKT BD:4.7 L,MULTIPLE WIDTH PLUG-IN	80009	386-5467-00
					(ATTACHING PARTS)		
-122	211-0507-00			8	SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-123	220-0557-00			8	NUT,SLEEVE:6-32 X 0.204 OD BRS CD PL	80009	220-0557-00
					(END ATTACHING PARTS)		
-124	426-1898-00			1	FR SECT,PLUG-IN:REAR	80009	426-1898-00
					WIRE ASSEMBLIES:		
-125	175-6895-00			1	CA ASSY,SP,ELEC:26,28 AWG,7.5 L,RIBBON	80009	175-6895-00
					(A1P140 TO A3J120)		
-126	175-6899-00			1	CA ASSY,SP,ELEC:34,28 AWG,3.75 L,RIBBON	80009	175-6899-00
					(A2P340 TO A3J200)		
-127	175-6898-00			1	CA ASSY,SP,ELEC:26,28 AWG,3.75 L,RIBBON	TK0171	ORDER BY DESCR
					(A2P260 TO A3J700)		
-128	175-6897-00			1	CA ASSY,SP,ELEC:26,28 AWG,6.87 L,RIBBON	80009	175-6897-00
					(A3J600 TO A5P500)		
-129	175-6896-00			1	CA ASSY,SP,ELEC:20,28 AWG,5.85 L,RIBBON	80009	175-6896-00
					(A7P1010 TO A5P320)		
-130	175-8026-00			1	CA ASSY,SP,ELEC:7,22 AWG,5.0 L,RIBBON	80009	175-8026-00
					(A8P440 TO A9P450)		

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-131	131-0707-00			14	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
	214-2629-00			2	.PIN,ACTUATOR:	80009	214-2629-00
-132	352-0166-00			2	.HLDR,TERM CONN:8 WIRE,BLACK	80009	352-0166-00
-133	175-0858-00			AR	.CABLE,SP,ELEC:7,22 AWG,STRD,PVC INSUL,RBN	TK0846	07CF22M7-BBT
-134	175-8027-00			1	CA ASSY,SP,ELEC:6,22 AWG,4.5 L,RIBBON (A8P445 TO A9P440)	80009	175-8027-00
-135	131-0707-00			12	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
	214-2629-00			2	.PIN,ACTUATOR:	80009	214-2629-00
-136	352-0165-00			2	.HLDR,TERM CONN:7 WIRE,BLACK	80009	352-0165-00
-137	175-0859-00			AR	.CABLE,SP,ELEC:6,22 AWG,STRD,PVC JKT,RBN	TK0846	06CF22M7-BBT
-138	175-8032-00			1	CA ASSY,SP,ELEC:3,26 AWG,8.0 L,RIBBON (A8P910 TO A6P600)	80009	175-8032-00
-139	131-0707-00			6	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-140	352-0161-00			2	.HLDR,TERM CONN:3 WIRE,BLACK	80009	352-0161-00
-141	175-0826-00			AR	.CABLE,SP,ELEC:3,26 AWG,STRD,PVC JKT,RBN	80009	175-0826-00
-142	175-8031-00			1	CA ASSY,SP,ELEC:3,26 AWG,5.0 L,RIBBON (A5P230 TO A6P610)	80009	175-8031-00
-143	131-0707-00			6	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-144	352-0161-00			2	.HLDR,TERM CONN:3 WIRE,BLACK	80009	352-0161-00
-145	175-0826-00			AR	.CABLE,SP,ELEC:3,26 AWG,STRD,PVC JKT,RBN	80009	175-0826-00
-146	175-4150-00			5	CA ASSY,SP,ELEC:3,26 AWG,3.0 L,RIBBON (A5P560 TO A6J630;A4P112 TO A6P230; .A4P211 TO A6P220;A4P311 TO A6P210; .A4P411 TO A6P200)	80009	175-4150-00
-147	131-0707-00			30	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-148	352-0161-00			10	.HLDR,TERM CONN:3 WIRE,BLACK	80009	352-0161-00
-149	175-0826-00			AR	.CABLE,SP,ELEC:3,26 AWG,STRD,PVC JKT,RBN	80009	175-0826-00
-150	175-8028-00			1	CABLE ASSY,RF:50 OHM COAX,11.0 L,9-6 (J47 TO A6P632)	80009	175-8028-00
-151	131-0707-00			1	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
	131-2428-00			1	.CONTACT,ELEC:18-20 AWG,BRS,CU BE,GLD PL	22526	47441-000
-152	352-0169-00			1	.HLDR,TERM CONN:2 WIRE,BLACK	80009	352-0169-00
-153	177-1069-00			AR	.CABLE,RF:50 OHM COAX,9-6	80009	177-1069-00
-154	210-0775-00			1	.EYELET,METALLIC:0.126 OD X 0.205 L,BRS	80009	210-0775-00
-155	210-0774-00			1	.EYELET,METALLIC:0.152 OD X 0.218 L,BRS	80009	210-0774-00
-156	175-8029-00			1	CABLE ASSY,RF:50 OHM COAX,12.0 L,9-2 (J49 TO A6J602)	80009	175-8029-00
-157	177-1065-00			AR	.CABLE,RF:50 OHM COAX,9-2	80009	177-1065-00
-158	210-0775-00			2	.EYELET,METALLIC:0.126 OD X 0.205 L,BRS	80009	210-0775-00
-159	210-0774-00			2	.EYELET,METALLIC:0.152 OD X 0.218 L,BRS	80009	210-0774-00
-160	175-8030-00			1	CABLE ASSY,RF:50 OHM COAX,14.0 L,9-5 (A2J710 TO A6J700)	80009	175-8030-00
-161	131-0707-00			1	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
	131-2428-00			1	.CONTACT,ELEC:18-20 AWG,BRS,CU BE,GLD PL	22526	47441-000
-162	352-0169-00			1	.HLDR,TERM CONN:2 WIRE,BLACK	80009	352-0169-00
-163	177-1068-00			AR	.CABLE,RF:50 OHM COAX,9-5	80009	177-1068-00
-164	210-0775-00			1	.EYELET,METALLIC:0.126 OD X 0.205 L,BRS	80009	210-0775-00
-165	210-0774-00			1	.EYELET,METALLIC:0.152 OD X 0.218 L,BRS	80009	210-0774-00

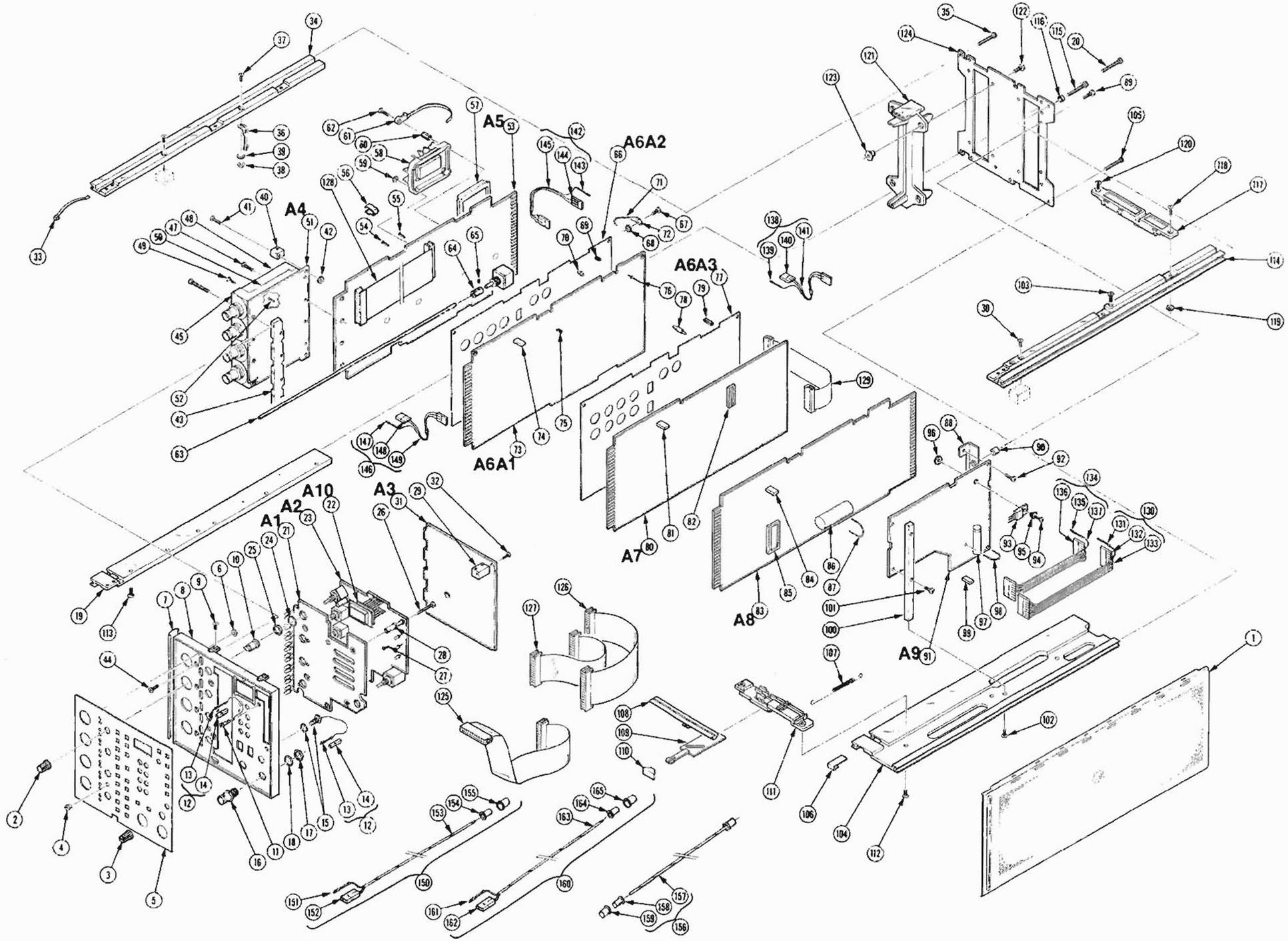


FIG. 1 EXPLODED VIEW

7A42 LOGIC TRIGGERED VERTICAL AMPLIFIER

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-							
					STANDARD ACCESSORIES		
-1	012-0403-00			1	CABLE ASSY,RF:50 OHM COAX,44.0 L	80009	012-0403-00
	070-4285-00			1	MANUAL,TECH:OPERATOR,7A42	80009	070-4285-00
	070-4286-00			1	MANUAL,TECH:SERVICE,7A42	80009	070-4286-00
					OPTIONAL ACCESSORIES		
	067-1112-00			1	FIXTURE,CAL:EXTENDER CABLE	80009	067-1112-00
	067-0616-00			1	FIXTURE,CAL:PLUG-IN EXTENDER	80009	067-0616-00

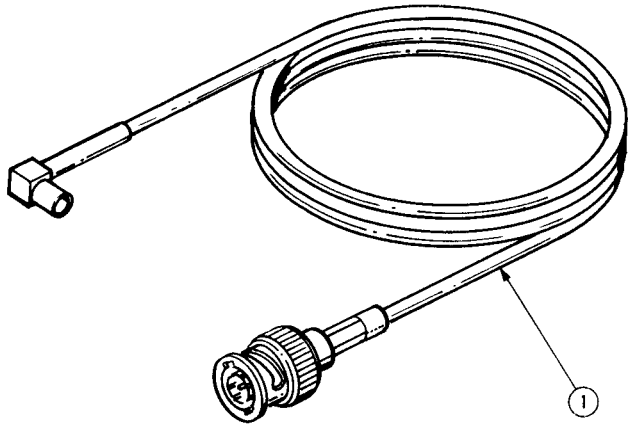


FIG. 2 ACCESSORIES

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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MANUAL CHANGE INFORMATION

Date: 9/23/86 Change Reference: C7/986

Product: 7A42 Manual Part No.: 070-4286-00

DESCRIPTION PG 42

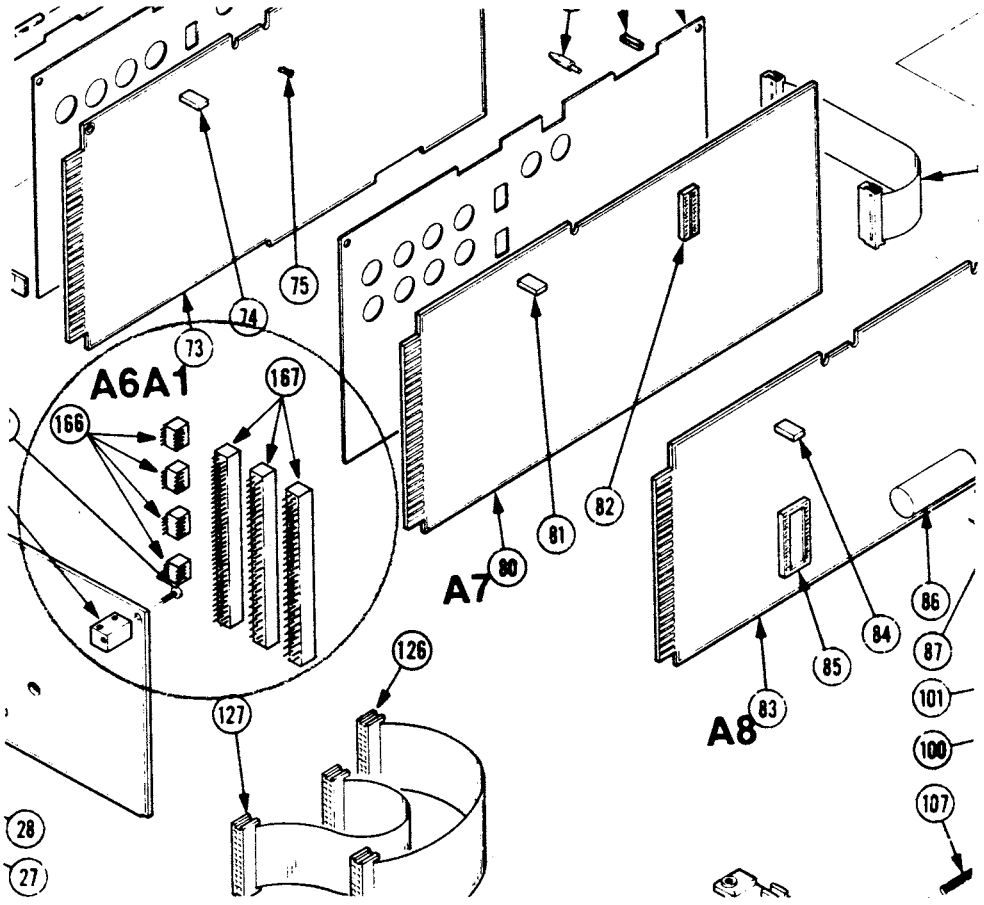
THESE CHANGES ARE EFFECTIVE FOR ALL SERIAL NUMBERS.

MECHANICAL PARTS LIST CHANGES

ADD:

1-166	131-2724-00	4	CONN,RCPT,ELEC,CK BD,RTANG,2 x 5, 0.1 CTR HORIZ
1-167	131-2843-00	3	CONN,RCPT,ELEC,EDGECARD,2 x 36, 0.1 SPACING

ADD THESE 2 PART NUMBERS TO THE FIG. 1 EXPLODED VIEW
7A42 LOGIC TRIGGERED VERTICAL AMPLIFIER



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MANUAL CHANGE INFORMATION

Date: 12/15/87 Change Reference: M60204

Product: 7A42 Logic Triggered Vertical Amplifier

Manual Part No.: 070-4286-00

PRODUCT GROUP CODE: 42

DESCRIPTION

These changes are effective at serial number B011035.

MECHANICAL PARTS LIST CHANGE

CHANGE TO:

FIG. & INDEX NO.		
1-121	386-5467-00	GUIDE, CKT BD:4.7 L, MULTIPLE WIDTH PLUG-IN

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MANUAL CHANGE INFORMATION

Date: 5/6/88 Change Reference: C110/0588

Product: All 7000 Service manuals

Manual Part No.: see product

Product Group: 42

DESCRIPTION

Effective for all serial numbers.

REPLACEABLE ELECTRICAL PARTS LIST CHANGE

The part number has changed for a transistor which may be used in your 7000-Series product. Part number 151-0220-00 has changed to 151-0220-07. Use the new 151-0220-07 part number when ordering a replacement for transistors listed as151-0220-00 in your Replaceable Electrical Parts List.

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 6/6/88 Change Reference: C120/0688

Product: All 7000 Service manuals

Manual Part No.: 7000 Service

Product Group: 42

DESCRIPTION

This change is effective for all serial numbers.

REPLACEABLE PARTS LIST CHANGE

Most berg sockets, part number 136-0252-07, have been removed from this 7000 series instrument to facilitate assembly and improve reliability.