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7S14

DUAL TRACE DELAYED SWEEP SAMPLER

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-1410-00
Product Group 42

Serial Number _____

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
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TABLE OF CONTENTS

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

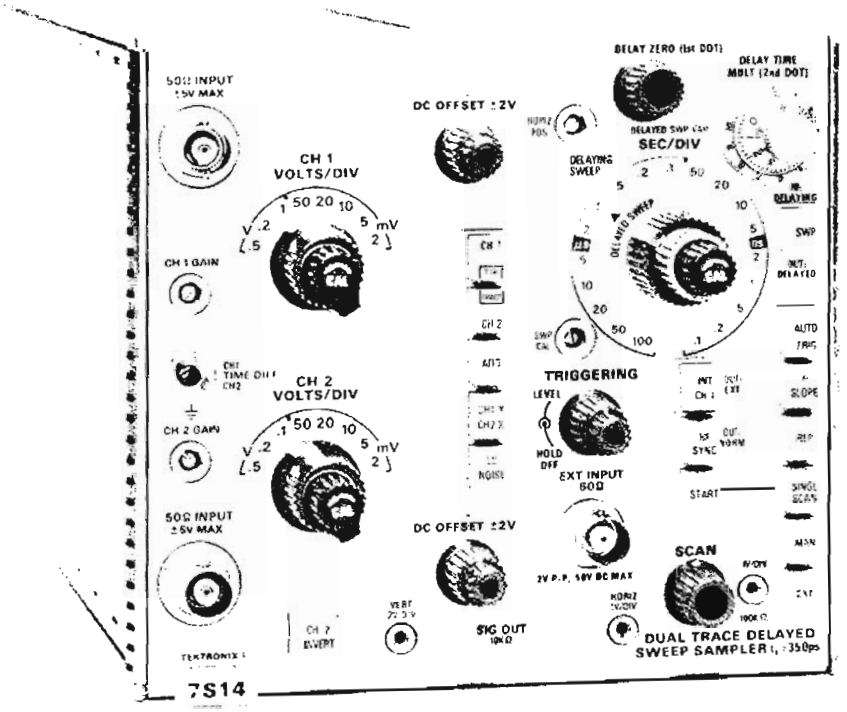

Fig. 1-1. 7S14 Dual Trace Delayed Sweep Sampler.

CHARACTERISTICS

General Information

The Tektronix 7S14 Dual Trace Delayed Sweep Sampler is a general purpose sampling unit with a DC-to-1000 MHz bandwidth. It will operate in any Tektronix 7000 Series mainframe. The front panel terminology is similar to that of conventional oscilloscopes.

The 7S14 has two time bases to provide "delaying" and "delayed sweep" operation. The delayed sweep starts after the selected delay interval, giving the effect of a wide-range sweep operation. The delayed sweep starts after the selected delay interval, giving the effect of a wide-range sweep magnifier. The calibrated delay replaces the "time position" control found on most sampling time-base units.

The 7S14 has a two dot time-interval measurement method that provides a means of measuring the time between two points on the "normal" (delaying) display. A brightened dot on the trace can be positioned to the start of the event to be measured. A second brightened dot can be positioned to the end of the event by using the Delay Time Mult control. The time interval between the two points is the product of the reading on the Delay Time Mult dial times the Delaying Sweep Sec/Div setting.

Delay lines in the input signal channels permit display of the leading edge of the triggering waveform. The Auto Level mode provides a bright baseline in the absence of a triggering signal. Other features include 2 mV/div sensitivity, low tangential noise, versatile triggering capabilities, a broad range of sweep rates, and crt readout of both the attenuation and timing values.

The characteristics given in the following Table apply over an ambient temperature range from 0°C to +50°C after the instrument has been calibrated at +25°C ±5°C. Under these conditions, the 7S14 will perform to the requirements given in the Performance Check section of this manual.

The Supplemental Information column of the Table provides additional information about the operation of the 7S14. Characteristics given in the Supplemental Information column are not requirements in themselves and are not necessarily checked in the Performance Check procedure.

ELECTRICAL CHARACTERISTICS

	VERTICAL SYSTEM	
Characteristics	**Performance Requirements**	**Supplemental Information**
Risetime	350 ps or less, 10% to 90% of step pulse signal.	
Step Aberrations	+2%, −3%, total of 5% or less P-P within first 5 ns after step transition; +1%, −1%, total of 2% or less P-P thereafter.	Check made with Tektronix 284 Pulse Generator; includes aberrations from the 284.
Bandwidth (−3 dB)	DC to 1 GHz or more.	Calculated from risetime.
Input Resistance	50 Ω within 2%.	
Deflection Factor	2 mV/Div to 0.5 V/Div.	8 steps, 1-2-5 sequence.
Accuracy	Within ±3% (with VARIABLE at CAL).	
Variable	At least 2.5:1.	Extends uncalibrated deflection factor to approximately 800 μV/Div.
Input Signal Range		
Maximum Operation	2 V P-P (DC + Peak AC) within a +2 V to −2 V window at any sensitivity.	
Maximum Overload	±5 V.	

ELECTRICAL CHARACTERISTICS (cont)

VERTICAL SYSTEM (cont)

Characteristics	Performance Requirements	Supplemental Information
DC Offset Range	+2 V or more to −2 V or more.	
Displayed Noise (tangential)	2 mV or less, LOW NOISE switch "out".	
Low Noise Operation	Displayed noise reduced by at least five times.	
Vertical Signal Out	0.2 V/Div of deflection ±3%.	Source resistance is 10 kΩ ±0.5%.
Dot Slash	Less than 0.1 Div at 10 Hz and above.	
Interchannel Crosstalk	−60 dB or less.	When input signal is 0.5 GHz sine wave.
ΔT Range	Shifts Channel 2 at least +1 ns to −1 ns with respect to Channel 1.	Range may be centered with internal adjustment.

HORIZONTAL SYSTEM

Delaying Time Base

Time Base Range	100 μs/Div to 10 ns/Div.	13 steps, 1-2-5 sequence.
Time Base Accuracy	Within ±2%, excluding first ½ division of displayed sweep.	No time mark between 1st and 9th divisions can be more than 0.2 divisions from the major division line when the 1st mark is set on the 1st division line.
Delay Zero Range	0-9 divisions or more.	When Delay Time Multiplier is set to 0.00, the 1st dot can be moved past the 9th graticule line.
Delay Time Multiplier	Each turn equal to 1 crt division.	Delaying Time/Div X Delay Time Mult = Time between dots.
Delay Accuracy	Within 1% of full screen (10 crt divisions) when measurement is made between 1st and 9th crt divisions.	

Delayed Time Base

Time Base Range	100 μs/Div to 100 ps/Div.	19 steps, 1-2-5 sequence.
Accuracy	Within ±3%, excluding first ½ division of displayed sweep.	No time mark between 1st and 9th divisions can be more than 0.3 divisions from the major divison line when the 1st mark is set on the 1st division line.
Variable	At least 2.5:1.	Extends uncalibrated Time/Div to approximately 40 ps/Div.

ELECTRICAL CHARACTERISTICS (cont)

HORIZONTAL SYSTEM (cont)

Characteristics	Performance Requirements	Supplemental Information
Time Base Display Modes		
Delaying Time Base		Conventional display, maximum lead time. Left intensified dot indicates Time Zero (Multiplier Zero). Right intensified dot indicates point at which Delayed Sweep starts. Time between dots is read from the crt or the Delay Time Multiplier dial.
Delayed Time Base		Delayed sweep display starts immediately at end of delay time. Set by Delay Zero plus Delay Time Multiplier. Operates in same manner as "run after delay" mode in conventional oscilloscopes except Time Zero is adjustable and identified.
Triggering		
Amplitude Range		
External	10 mV to 2 V, P-P.	Rate of rise, 10 mV/μs or faster.
Internal	50 mV to 2 V, P-P.	At Sampler Input (vertical input signal). Rate of rise, 50 mV/μs or faster.
Input Resistance	51 Ω within ±10%, AC coupled.	
Jitter	Less than 40 ps with 50 mV, 5 ns width trigger at external input. Less than 30 ps when internally triggered from 284 pulse.	
NORMAL Triggered Mode		
Sine waves	150 kHz to 100 MHz.	
Pulse	10 Hz to 100 MHz.	
Minimum Rise Rate	10 mV/μs.	
AUTO TRIG Mode (Auto baseline when not triggered)		
Sine waves	150 kHz to 100 MHz.	
Minimum Amplitude	10 mV P-P at 100 MHz (Ext).	
Pulse	1 kHz to 100 MHz.	Auto baseline below 800 Hz.
Minimum Pulse Width	10 ns at 1 kHz.	
Minimum Rise Rate	10 mV/μs.	

ELECTRICAL CHARACTERISTICS (cont)

HORIZONTAL SYSTEM (cont)

Characteristics	Performance Requirements	Supplemental Information
HF SYNC Mode		
Sine waves	100 MHz to 1 GHz.	Free-Running Sync.
Scan Controls		
Repetitive	25-40 Hz Repetition Rate.	Repetition rate barely into flicker rate. Controls must be set as follows: Low Noise Control, out; HF SYNC Control, in; Scan Control, fully CW; Holdoff control, fully CCW; Delaying sweep, 1 μs/Div or faster; Approximately 20 samples per div at low trigger or sweep rates.
Single Sweep	One sweep per Single Sweep Start button depression.	Scan Rate is the same as set in Repetitive mode.
Manual	Scan control moves the spot over a slightly greater range than 10 divisions.	
Ext Scan		
Maximum Sensitivity	1 V/Div within ±5%.	Scan control serves as an attenuator. Full scale scan signal must run from 0 V to +10 V or more.
Maximum Input Voltage	150 V.	
Horizontal Output Signal Amplitude	1 V/Div ±5%.	Source resistance is 10 kΩ within ±0.5%.

ENVIRONMENTAL CHARACTERISTICS

Characteristics	Description
Temperature	
Operating Range	0°C to +50°C.
Non-operating Range	−40°C to +70°C.
Altitude	
Operating Range	To 15,000 feet.
Non-operating Range	To 50,000 feet.
Vibration Range	To 0.025 inch peak-to-peak displacement at 55 cycles per second.
Shock Range	To 30 g, ½ sine, 11 milliseconds duration.
Transportation (Non-operating)	Meets National Safe Transit Test Requirements.

BASIC SEQUENTIAL SAMPLING PRINCIPLES

Introduction

Sampling provides the means to display fast-changing signals of low amplitude that cannot be displayed in any other way. Sampling overcomes the gain-bandpass limitation inherent with conventional amplifiers and oscilloscopes. It does so by displaying a real-time signal in "equivalent" time. Only the input stage of a sampler is subjected to the input signal; all subsequent signal amplification takes place through relatively low bandwidth amplifiers.

Sampling, however, does require repetitive input signals. Fortunately, most fractional-nanosecond risetime signals exist in low impedance environments; thus they may be delivered directly through 50 ohm cables to a 50 ohm load. They are generally low amplitude signals, so 50 ohm attenuators are used when the signal is more than one or two volts.

There are three types of sampling: sequential, random, and real-time. The 7S14 uses the sequential sampling method; this technique will be discussed in this section of the manual.

Equivalent-time Sequential Sampling

The sampling system looks at the instantaneous amplitude of a signal during a specific small time period, remembers the amplitude, and displays a single dot on the crt that corresponds to the amplitude. The horizontal position of the dot represents the equivalent time when the sample was taken. After a dot is displayed for a fixed amount of time, the system again looks at the instantaneous amplitude of a different cycle of the input signal. Each successive look, or sample, is at a slightly later time in relation to a fixed point of each sampled signal cycle. After many cycles of the input signal, the sampling system has reconstructed and displayed a single facsimile made up of many samples, each sample taken in sequence from a different cycle of the input signal; thus, the term "sequential sampling".

Because the reconstructed signal is not completed until long after the first signal cycle has occurred, it is not displayed in "real" time. The time displayed on the crt is termed "equivalent-time". Such a display is shown in Fig. 2-1. The equivalent time between dots is determined by the time delay between the fixed point on the signal at which sweep triggering occurs and the point at which the sample is taken. The real-time and equivalent-time relationship is depicted in Fig. 2-2. Since both time references (triggering and sampling) are taken from the same cycle of the signal, the signal repetitions do not have to be identical in amplitude, time duration, and shape. Periodic differences in individual cycles, however, will show as noise or jitter in the reconstructed display if the shape or amplitude changes from cycle to cycle.

The number of dots per horizontal division in one sweep is called dot density. Since only one sample is taken from any particular input cycle, the time needed to reconstruct a display depends on the dot density and the repetition rate of the signal. The greater the dot density and the slower the repetition rate, the longer the time to construct the equivalent-time display.

Sampling systems have maximum signal repetition rates at which samples can be taken and accurately displayed.

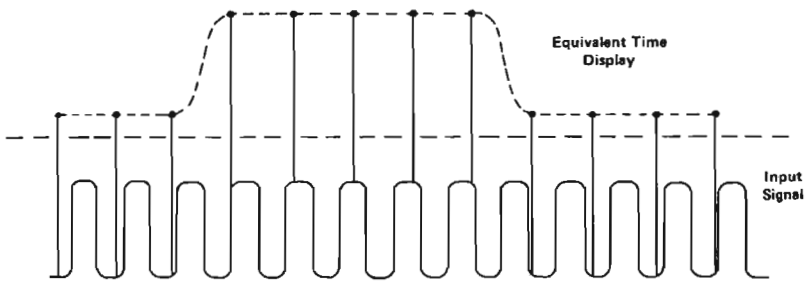

Fig. 2-1. Input pulse of a repetitive real-time signal is reconstructed in an equivalent-time display via sequencial sampling.

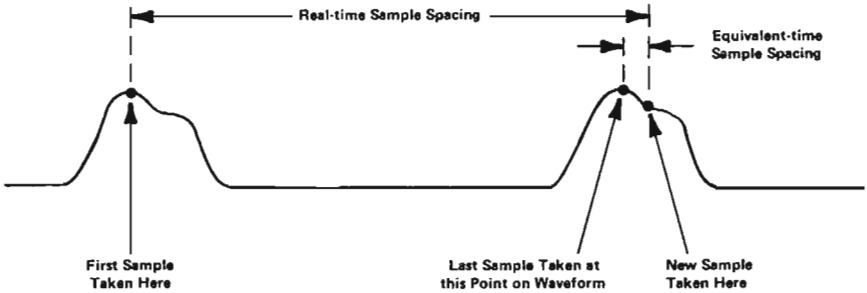

Fig. 2-2. Real-time and equivalent-time relationship.

The primary limit is the time needed for the vertical amplifiers to stabilize after a sample has been taken. For signals with a repetition rate higher than 30 kHz, the timing unit holds off retriggering for a maximum of approximately 35 μs. This means that a sample will not be taken from every cycle of a high repetition rate signal; only those cycles are sampled that occur after the end of the trigger holdoff. If the signal is truly repetitive and each cycle is identical, these "missed" cycles are of little significance.

Signals below 30 kHz may have considerable repetitive rate jitter, but the sampling oscilloscope can still give a sample of each cycle without display jitter because triggering and sampling both occur on the same cycle.

Vertical Functions

The sampling oscilloscope's vertical stages perform the same basic functions as those in a nonsampling oscilloscope: i.e., signal amplification and attenuation. Vertical signal delay is also used to permit viewing a signal's leading edge.

All the amplification and signal processing in the sampling oscilloscope (except for the passive 50 ohm input) is done at relatively low frequencies. It is this feature that makes the sampling oscilloscope unique in performance and design.

Sampling begins with the input signal being changed to stored, long duration, low frequency voltages consisting of brief portions (samples) of the input. This change is not a frequency conversion; rather, it is a different way to represent the input signal.

The sampled energy is stored in a memory circuit so that it stays constant between samples. Each time a new sample is taken, the memory is refreshed. The amount of sampled and stored energy represents the amplitude of the input signal when that sample is displayed on the crt.

Vertical stages in a sampling oscilloscope include some not found in a nonsampling oscilloscope, such as a Sampling Gate, Blow-by Compensation, Preamplifier, Memory Gate, Memory Amplifier and Feedback, and Memory Gating Generator. Circuit descriptions for these stages appear in Section 5. In summary, stage purposes are: Sampling Gate samples brief portions of the input signal; Blow-by Compensation nullifies unwanted signal coupling; Preamplifier and Memory Amplifier and Feedback keep the Sampling Gate output and Memory constant between samples, making the Sampling Gate output proportional to its input; the Memory Gate passes the sampled signal to the Memory; and the Memory Gating Generator turns on the two gates.

An important part of the sampling process is a sampling loop. This loop provides in-phase feedback of the sampled and memory energy to the Sampling Gate output. The feedback forms a null-seeking servo loop that attempts to make a zero difference between the Sampling Gate input and output.

When the gain of the feedback loop is unity, it compensates for the attenuation across the Sampling Gate. In this case, the feedback voltage equals the value of the sampled input signal voltage. When the loop gain is less than unity, the feedback voltage is less than necessary to equalize the voltage across the gate. The Memory output and feedback will then approach the signal asymptotically after several samples have been taken. The Memory output

is effectively a moving average of several preceding samples. When the loop gain is greater than unity, the feedback voltage is greater than the Sampling Gate input signal. The resulting crt display of a step signal input will alternately overshoot and undershoot for a few samples. For the least display distortion, the loop gain must be unity, allowing the system to track the input signal as closely as possible.

A loop gain of less than unity can be useful, if the resulting condition is understood and the system is operated properly. Random noise in the display is reduced when loop gain is less than unity, since several consecutive samples are averaged. The averaging, however, will slow the risetime of an abrupt step signal depending on the number of dots in the step transition and how much less than unity the loop gain may be. Averaging will also reduce the amplitude of a sine wave if there are not enough dots per cycle.

When the memory gate is open, it passes the sampled signal and charges a capacitor in the memory gate output. This stored charge remains essentially constant until another sample is taken. The memory output is not reset to zero after a given sample, but is held at the level of the previous sample by the feedback signal.

In the memory gate output there is a LO NOISE control that reduces the random noise seen at high sensitivities. The function of this control is known as "smoothing," in that it smoothes or averages several consecutive samples. A check for whether smoothing is producing any distortion is accomplished by increasing the number of dots in the display with the SCAN control and observing whether there is any significant change in the waveform.

Fig. 2-3 shows the usual effects of smoothing for two different sampling densities (sampling density or dot density is the number of samples or dots per horizontal division).

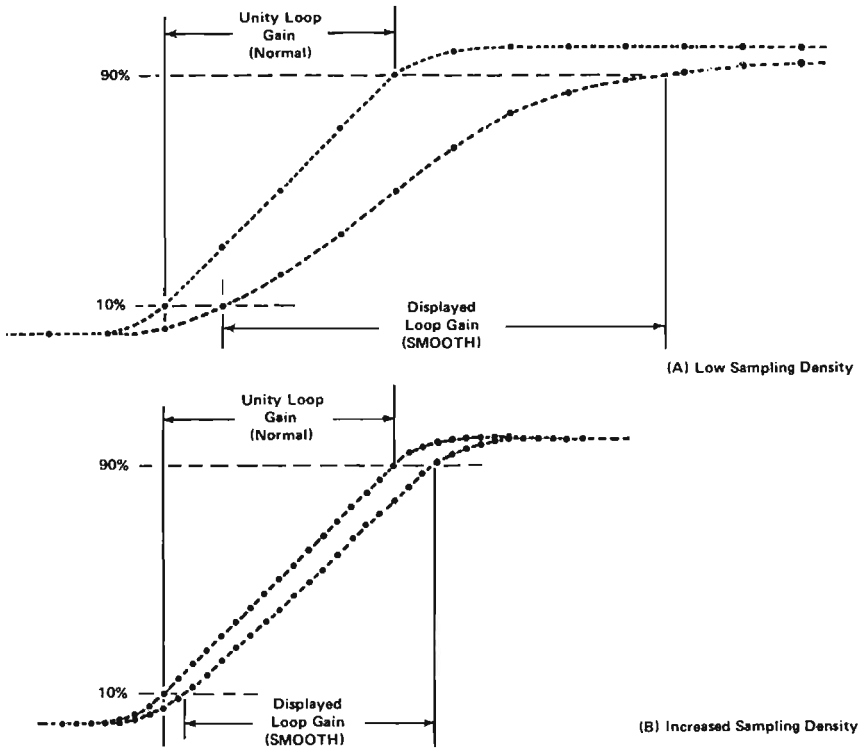

Fig. 2-3. Equivalent-time display with and without smoothing for two different sampling densities.

The signal out of the memory gate gets amplified by the memory circuit. Each change in voltage at the memory output is a step change proportional in amplitude to a step at the input to the preamplifier.

On sampling systems having two input channels, such as the 7S14, there are two sets of sampling-loop circuits. The output from each of the memories is fed to a channel switching multivibrator that selects which output each dot represents, so that either channel can be displayed, or so that both channels can be displayed, as two traces, by alternating outputs with each successive dot.

Horizontal Functions

The Horizontal system provides deflection voltage for the crt display and simultaneously controls the time at which the vertical system samples the input signal. The system uses (1) a 1 GHz trigger circuit, (2) two fast ramps for either Delaying sweep or Delayed sweep operation, (3) a combination scan ramp and staircase generator to provide horizontal deflection and a comparison level for the fast ramps, (4) two intensified positionable dots to provide an accurate dial read-out for time measurements and (5) a delay generator to provide strobe drive to the two vertical channels so that the signal at one input channel may be sampled consistently earlier than, later than, or coincident with the signal at the other input.

The sampling oscilloscopes's horizontal sweep is produced by a staircase voltage that advances one step each time a sample is taken. One cycle of the input signal causes the trigger circuit to initiate one cycle of the sampling process and produce one dot for the display.

The sampling cycle starts when the trigger circuit recognizes a point in a cycle of the triggering signal and unclamps the fast ramp generator. The fast ramp generator produces a linear rundown voltage that is compared to the slowly changing staircase voltage. The resulting pulse that occurs the instant the fast ramp voltage level equals the staircase voltage level is sent to the vertical circuit via the Delta Delay Generator as a strobe drive pulse. From there the strobe also goes to the Scan Ramp and Staircase Generator as a staircase-advance pulse.

The staircase generator advances one step just after the sampling circuit takes a sample of the input signal. The sampling memory output is applied to the vertical amplifier and the staircase output level is applied to the horizontal deflection system of the oscilloscope. As soon as the sample has been taken, a dot is displayed on the crt screen at a vertical position proportional to the input signal voltage level at the instant it was sampled. The dot then remains stationary on the screen until another sample is taken.

Each subsequent recognized triggering signal cycle initiates the same sequence of events. But since the staircase voltage moves down one step each time, the fast ramp has to run slightly farther each time before a comparison pulse is produced. In this way the sampling event is delayed by successively longer intervals and the samples are taken successively later along the waveform with respect to the triggering point. Each time a sample is taken, the crt is blanked momentarily while the dot on the crt moves horizontally by one increment.

The 7S14 contains a "two-dot circuit" that provides two bright dots for each trace. With the two dot circuit it is possible to position the dots to two specific points in the waveform and measure the time interval between the points directly from the 2nd dot positioning control.

Glossary of Sampling Terms

There are many terms used in the discussion of sampling systems whose definitions may not be universal. The following terms, used in this manual, have been compiled to help avoid confusion.

Blow-by—A display aberration resulting from signal-induced displacement current through all capacitance shunting the Sampling Gate.

Display Window—The particular time interval represented within the horizontal limits of the graticule.

Dot—A displayed spot indicating the horizontal and vertical coordinates of a particular sample.

Dot Density—The number of dots per horizontal division in any one scan.

Equivalent Time—The time scale represented in the display of a sampling oscilloscope operating in the equivalent-time sampling mode.

Equivalent-time Sampling—A sampling process in which a least one repetitive signal event is required for each sample taken. The time required for display construction is thus greater than the time represented in the display.

Fast Ramp or Slewing Ramp—A linear ramp which acts with a slower staircase, ramp, or other changing voltage to cause slewing.

Feedback—The effective intersample attenuation in the signal path between Memory output and Sampling Gate output in a sampling loop.

Forward Gain—The effective gain between the Sampling Gate output and Memory output in a sampling loop.

Loop Gain—The product of sampling efficiency, forward gain and feedback attenuation in a sampling loop. Loop gain is normally unity except in a smoothed display where it may be less than unity.

Memory—A circuit which stores the vertical (or horizontal) coordinate value of a sample.

Memory Gate—An electronic switch between a Memory and its driving amplifier.

Pretrigger—A trigger signal which occurs before a related signal event.

Real Time—The time scale associated with signal events.

Sampling—A process of sensing and storing one or more instantaneous values of a signal for further processing or display.

Sampling Efficiency—The ratio of the voltage change between the instant before sampling, t^-, and the instant after sampling, t^+, at the output of a Sampling Gate to the difference between gate input voltage, E_i, and gate output voltage, E_o, at the instant before sampling.

$$E = \frac{E_o(t^+) - E_o(t^-)}{E_i(t^-) - E_o(t^-)}$$

Sampling Gate—An electronic switch which conducts briefly upon command for the purpose of collecting and storing the instantaneous value of a signal.

Sampling Loop—Those circuits providing the main signal path through the Sampling Gate, Preamplifier, Loop Gain attenuator, DC Balance Amplifier, Memory Gate, Memory, and the Feedback attenuator.

Scanning—The process by which slewing is controlled.

Sequential Sampling—A sampling process in which samples are taken at successively later times relative to a fixed point of each sampled signal cycle.

Slewing—The process of causing successive samples to be taken at different instants relative to a fixed point of each sampled signal cycle.

Smoothing—A process that reduces the effect of random noise or jitter in the display by averaging several consecutive samples.

Strobe—A pulse of short duration which operates the Sampling Gate.

OPERATING INSTRUCTIONS

General Information

The 7S14 is a double-width plug-in unit containing both vertical and horizontal deflection circuits. The 7S14 operates in any Tektronix 7000 Series mainframe when the unit is completely inserted into the proper two slots of the mainframe plug-in compartment. When inserted into mainframes that accommodate three single-width plug-ins, the two slots toward the operators right should be used. The middle two slots should be used in four-hole mainframes.

NOTE

When the 7S14 is used in the R7603, R7613, R7623, or R7903 rackmount instruments, the support posts between the rackmount plug-in compartments must be removed so that the dual width 7S14 can be inserted into the mainframe.

A blank plug-in panel may be used to cover the opening of any slot not occupied by a plug-in unit. Use panel 016-0155-00 for 7000 Series mainframes.

Assuming it is clean and dry, the plug-in unit is ready to operate as soon as it has been correctly installed in the mainframe. However, the mainframe power cord must first be plugged into a power outlet that supplies AC voltage of the correct frequency and amplitude and the mainframes power switch must be turned on. It should not be necessary to turn the power off before removing or inserting the plug-in unit.

Mainframe Controls

Besides the power switch, there are other switches and controls on the mainframe that must be set for the 7S14 to operate correctly. If you are not already familiar with the functions of the mainframe controls you may need to refer to the instruction manual for that mainframe.

Getting A Trace On Screen

With power applied and the plug-in properly inserted, the next step is to get a trace on screen. The recommended procedure is to (1) temporarily disconnect any vertical input or trigger input signals, (2) select the repetitive scan mode by pushing the REP button, (3) select 1 μs per division or faster for the DELAYING SWEEP (dark gray) control, (4) free-run the time base and sampling circuits by pushing the AUTO TRIG and HF SYNC buttons, (5) select Channel 1 Vertical input by pushing the CH 1 button, (6) set the Channel 1 VOLTS/DIV control to the least sensitive position, counterclockwise to .5 V, (7) center the Channel 1 DC OFFSET controls, and (8) adjust the mainframe crt intensity control for a medium bright trace. If a trace does not appear under these conditions, it is likely that either some mainframe control was incorrectly set, or that the mainframe or plug-in unit is not functioning properly.

Front Panel Controls

A brief description of the purpose and use of each front panel connector, pushbutton, control, and screwdriver-adjustment on the 7S14 follows. If you have never operated a sampling oscilloscope, you should read the entire section before proceeding to display a signal waveform. You should refer to Fig. 3-1 as a guide to specific operating instructions relating to each front panel control or connector.

1. 50 Ω INPUT ±5 V MAX

These are input connectors to both Channel 1 and Channel 2 sampling gate circuits and vertical deflection amplifiers. Signals as large as 2 V P-P in amplitude may be handled, as long as no swing exceeds +4 volts or −4 volts. However, peak signal excursions that exceed +2 volts or −2 volts cannot be displayed at the more sensitive setting, even when using maximum DC OFFSET. Voltage greater than ±5 volts may alter the accuracy of precision delay line compensation resistors or cause input circuit components to fail. External probes or 50 ohm attenuators should be used to display signal voltages greater than 4 volts. The following probes are recommeded: P6056, 10X probe; P6057, 100X probe; P6201, 1X, 10X and 100X FET probe. You will need a 1101 Power Supply for the P6201 probe if the mainframe does not have a probe power output jack. The BNC 50 ohm attenuators recommended are: 011-0059-02 (10X), 011-0060-02 (5X), and 011-0069-02 (2X). Signals as great as ±20 volts peak or 14 volts RMS may be applied to these attenuators before exceeding the wattage rating. 50 ohm attenuators having connectors other than the BNC type may be used if adapters to BNC connectors are available.

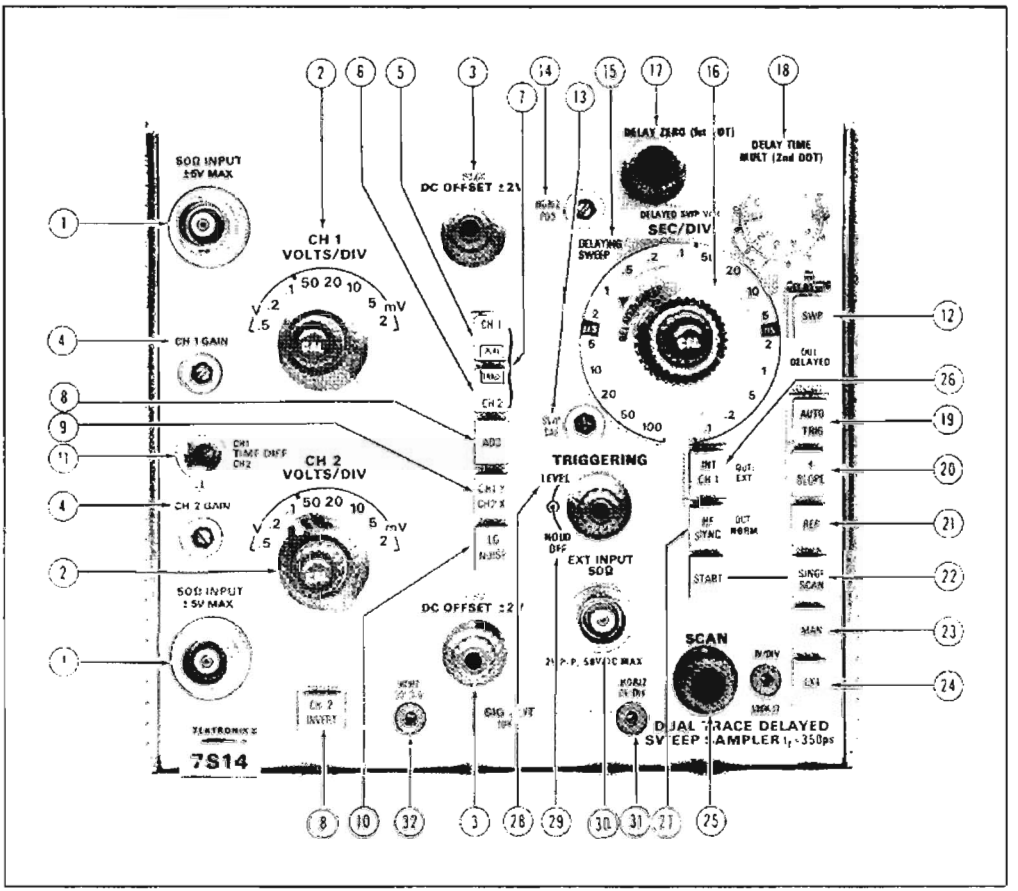

Fig. 3-1. Key to Operating Instructions.

2. CH 1 VOLTS/DIV and CH 2 VOLTS/DIV

The outer control selects the vertical deflection factor from .5 V/Div to 2 mV/Div. The red variable control (CAL) adjusts sensitivity over a range of at least 2.5 to 1. The two controls provide any sensitivity between .5 V per division and .8 mV per division. The CAL control must be set in the fully counterclockwise (detented) position before the indicated deflection factor can be expected to be accurate.

3. DC OFFSET ±2 V

These two controls position the display up or down or position a signal on screen that otherwise may be off screen. A signal riding on a DC level as great as +2 volts or −2 volts may be positioned to center screen. The FINE control makes it easier to precisely position the display at high sensitivities.

4. CH 1 GAIN and CH 2 GAIN

These screwdriver adjustments set the gain of the corresponding channels so that the chosen deflection factor corresponds to the deflection displayed on the crt by a signal voltage of known amplitude. For example, a signal of precisely 1 volt P-P amplitude should produce five divisions of deflection when the VOLTS/DIV is .2 V. Each adjustment should normally be checked each time a plug-in is placed in a different mainframe.

CAUTION

The applied signal voltage should be from a 50 ohm source so that the voltage arriving at the input may be precisely one half of the open circuit, unloaded voltage value.

5. CH 1

Push this button to display a signal at Channel 1 input.

6. CH 2

Push this button to display a signal at Channel 2 input. There is no internal signal pickoff from Channel 2 input; internal triggering is from the signal picked off from Channel 1. Therefore, if you have only one input signal it should be connected to CH 1 input unless you use an external trigger input signal or using a power divider, first divide the signal so part may be applied to the external trigger input jack.

7. DUAL TRACE

Dual trace operation is achieved by pushing both CH 1 and CH 2 buttons at the same time.

8. ADD and CH 2 INVERT

Pushing the ADD button allows the signals at CH 1 INPUT and CH 2 INPUT to be, in effect, summed. Actually, the summing operation is performed on the sampled replicas of the two input signals following the vertical channel memories. This button should normally be pushed when two balanced, push-pull signals are applied to the CH 1 and CH 2 INPUTS. You may then also push the CH 2 INVERT button to achieve, in effect, differential input operation. Or, if you wish to see how similar the two halves of the push-pull signal may be, any difference between them can be displayed by leaving the CH 2 INVERT button out.

To display the difference between two similar signals that have nearly the same polarity or phase and the same amplitude, the CH 2 INVERT button should be pushed.

NOTE

A front panel screwdriver adjustment (CH 1-TIME DIFF-CH 2) can be set for very precise phase or time comparisons. Refer to a later discussion of the purpose of that control.

9. CH 1 Y CH 2 X

This button should be pushed for X-Y displays, such as Lissajous patterns. The signal applied to the Channel 1 input produces vertical deflection (Y) in the normal way and the signal applied to the Channel 2 input produces horizontal deflection (X). When using this mode, neither the DELAYING SWEEP nor DELAYED SWEEP controls affect the display in any way, except to change the maximum possible number of samples per second. Set the DELAYING SWEEP time per division to 10 ns and the triggering HOLDOFF control fully counterclockwise to ensure the greatest possible number of samples per second. The cleanest X-Y displays are achieved by triggering or synchronizing in the usual way before pushing the CH 1 Y-CH 2 X pushbutton.

10. LO NOISE

Push this button to reduce the amplitude of random noise in the display or, in some cases, to reduce horizontal time-jitter. It is normal for the horizontal scan rate to reduce greatly when this button is pushed.

11. CH 1 TIME DIFF CH 2

This screwdriver control should normally be set (and is set at the factory) so that identical signals applied to the two inputs will be displayed in precisely the same horizontal positions. For example,

if a single signal is applied to the middle port of a coaxial tee and the output from each of the other two ports is applied through similar cables of precisely equal length to the two input channels, a dual trace display should show two nearly identical waveforms that can be made to coincide with the DC OFFSET controls. If a very fast step-signal is applied in this manner and displayed at 100 ps per division, the fast edge of either signal may be seen to be positionable horizontally with the CH 1-TIME DIFF-CH 2 control so as to occur before, after, or coincident with the fast edge of the other input signal.

Although this control should normally be left set so two such signals can be made to coincide, the control may also be deliberately set to other positions to (1) compensate for the delay difference in two input cables or (2) critically compare two similar repetitive signals that do not occur simultaneously. If you wish to use this control to critically compare two such signals that occur at widely separated instances, two similar cables of unequal length may be used at the proper inputs if the difference in length is chosen to introduce a propagation delay difference nearly equal to the time between the events. Most coaxial cables, i.e., those made with a dielectric of solid polyethylene, cause a signal delay of approximately 1.5 ns per foot (50 ps per cm). The delay through most other cables will be less; some nearly as little as 1 ns per foot.

12. SWP (MODE)

Push this button to display a signal when sweep delay is not needed, unless the time per division must be less than 10 ns. Pushing this button allows the Delaying Sweep to determine the crt time per division. Releasing the button allows the Delayed Sweep to determine the crt time per division.

When the Delayed Sweep is selected to determine the crt time per division, the delaying sweep ramps are used in conjunction with the DELAY ZERO and DELAY TIME MULT controls to select the delay needed to display the signal of interest.

13. SWP CAL

This screwdriver adjustment sets the amplitude of the horizontal output signal (to the mainframe) to produce the correct deflection on the crt to correspond with any time per division selected. Ideally, the adjustment should be checked using a time mark generator each time the 7S14 is placed in a different mainframe. However, if internal adjustments in the plug-in are set correctly, the SWP CAL adjustment may be set using the two intensified dots displayed in each trace when using the Delaying Sweep mode. There should be precisely 8 divisions of separation between corresponding parts of the two dots when (1) the Delaying Sweep is set to 1 μs per division, (2) the DELAY TIME MULT dial is set to 8.00, and (3) the DELAY ZERO control is set to position the first dot one horizontal division from the left edge of the crt graticule.

14. HORIZ POS

This screwdriver adjustment should be used to set the left edge of a trace even with the left edge of the crt graticule after the SWP CAL adjustment has been made.

15. DELAYING SWEEP

The time indicated between the orange lines on the clear plastic skirt of the DELAYING SWEEP (dark gray) control is the crt time per division when the Delaying Sweep has been selected (SWP mode button pushed in).

16. DELAYED SWEEP

The time indicated at the point of the arrow on the clear plastic skirt of the DELAYED SWEEP (light gray) control is the crt time per division when the Delayed Sweep has been selected (SWP mode button released). Be sure that the concentric, red CAL control is counterclockwise in the detented position; otherwise, the indicated time per division will not be correct. The CAL control varies the time per division over a range of at least 2.5 to 1.

To reduce delay time-jitter and to increase scan rate, the time per division of the Delaying Sweep should be as close as possible to the time per division of the Delayed Sweep. Ten divisions of delay is available when both sweep rates are the same. When more than ten divisions of delay is needed, the Delaying Sweep time per division must be set to be greater. If set to be 1,000 times longer, 10,000 divisions of delay is available, but delay time-jitter may be as much as ½ division.

17. DELAY ZERO (1st DOT) — When using the Delaying Sweep mode, this control is used to set the position of the first intensified dot in the trace to a point in the displayed waveform suitable to be called time-zero, a beginning reference point for a time interval measurement. You will notice that this control usually moves the second dot as well. If, in some cases, it appears that you cannot position the first dot as far to the right as you may wish, it is probably because the second dot is at the right end of the trace. You may avoid this condition by running the DELAY TIME MULT dial completely counterclockwise first.

18. DELAY TIME MULT (2nd DOT) — This dial controls the separation between the first and second bright dots in a trace when the Delaying Sweep mode is selected. It controls the position of only the second dot until the second dot is positioned to the right end of the trace, at which time it continues to control the separation between dots by moving the first dot to the left. The point in a waveform identified by the second dot is the point corresponding to the left edge of the trace that you display when you switch from the Delaying Sweep mode to the Delayed Sweep mode (SWP mode button released).

The number indicated on the dial is proportional to the separation between dots; one turn equals one division. The time between dots is equal to the time indicated between the orange colored lines on the skirt of the clear plastic DELAYING SWEEP control multiplied by the number indicated by the dial. Precise time interval tests of whether the time between two particular points in a waveform is greater than or less than a given amount may be quickly made by first separating the dots by the right amount, then positioning them with the DELAY ZERO control to see whether the distance between dots is more than or less than the distance between the two particular points in the waveform.

19. AUTO TRIG — Push this button for nearly every triggering signal or condition you may encounter, except when the triggering signal has a frequency or repetition rate less than about 800 hertz. When this button is pushed, strobe pulses are automatically generated (at about 800 hertz) when no triggering signal is being delivered or recognized. This keeps the sampling memories refreshed, produces a slow moving scan and keeps the crt beam positionable on screen even in the absence of a triggering signal.

20. + SLOPE — Push this button when you wish to trigger on the positive-going portion of a signal. Release the button when you wish to trigger on a negative-going portion. The position of the button is immaterial when the HF SYNC button is pushed.

21. REP — The REP button should be pushed whenever repetitive scans (sweeps) are desired, which is the condition for most normal uses.

22. SINGL SCAN and START — Push the SINGL SCAN button when you wish to produce only one scan at a time; this scan is displayed on command by the START button. This mode is useful when photographing waveforms where the scan repetition rate is low, or for stored displays when using an oscilloscope mainframe having a storage crt. It is also recommended when making chart recordings using the VERT and HORIZ output signals. Note that each scan starts when the spring loaded START button is released, not when it is

pushed. The HORIZ output voltage returns to −5 volts when the START button is pressed and remains at about +5 volts at the completion of each scan. When driving a chart recorder, the START button should be held in while the recording apparatus is being set. The scan rate should be very slow when making chart recordings. Refer to the discussion about the SCAN control knob and the LO NOISE pushbutton, to set the scan rate as low as desired.

23. MAN — Push this button when you wish to scan the crt manually, instead of with the internally generated scanning ramp signal or with an externally supplied scanning signal. The scan control determines the point being sampled. This mode is particularly useful when you wish to repeatedly sample the same point in a signal for a period of time. High random noise may be separated from the signal this way by averaging the voltage at the VERT output jack.

24. EXT[1] — Push this button when you wish to control the horizontal position of the crt beam with an externally supplied scanning signal. The input jack adjacent to the EXT pushbutton is for introducing such a signal. A zero to +10 volt (or higher) signal is needed to produce a full scale horizontal scan. A signal that goes from zero to more than +10 volts may be attenuated with the SCAN control to produce ten divisions of scan. This mode is useful when you wish to slave the scan operation to an external instrument such as a chart recorder.

25. SCAN — This control determines the horizontal velocity of the crt beam (scan rate) whenever the REP button or the SINGL SCAN button is pushed. (This rate is partly determined by some other factors also, like trigger repetition rate, holdoff, time per division, and whether the LO NOISE button is pushed or released.)

[1]Pin tip plugs of 0.08 inch diameter should be used with the pin jacks.

26. INT CH 1 — Push this button to trigger on the internal signal introduced at the Channel 1, 50 Ω INPUT connector. Release this pushbutton to trigger on the external triggering signal introduced at the EXT INPUT connector.

27. HF SYNC — Push this button to synchronize on signals above 100 MHz. Be sure to release the pushbutton when triggering on any signal below 100 MHz.

28. LEVEL — The LEVEL control is used to "lock" on to the triggering or synchronizing signal to reproduce a steady, coherent waveform on the crt. The triggering signal must have a steady, synchronous time relationship with the vertical signal for the display to be steady.

29. HOLDOFF — The HOLDOFF control is normally left fully counterclockwise to allow a maximum scan rate. The HOLDOFF control is used to help display complex waveforms and pulse trains, such as digital words, by varying the period of trigger holdoff. That inhibits recognition of early, unwanted triggering signal edges.

30. EXT INPUT 50 Ω — This input connector is AC coupled into a nominal 50 ohm load. The blocking capacitor has a DC voltage rating of 50 volts and more than 1 megohm resistance. External triggering signals may be delivered to this input via a 50 ohm coaxial cable, unattenuated. For large signals the P6056 10X probe or P6057, 100X probe is recommended. When AC coupled, the DC load resistance imposed by these probes is essentially the same as that of the blocking capacitor, i.e., more than 1 megohm.

31. HORIZ 1 V/DIV[1] — The signal voltage available at this output pin jack is proportional to the horizontal position of the beam at any instant; zero volts corresponds to approximately center screen. The output waveform resembles that of a sawtooth or staircase when produced internally, using the REP or SINGL SCAN modes. The output voltage starts at

–5 volts and goes positive to +5 volts as the beam scans the ten crt divisions. The output waveform is most often used to drive chart recorders. Also refer to the discussion of the SINGL SCAN control.

32. VERT .2 V/DIV[1] — The signal available at this output pin jack is a replica of the signal that produces vertical deflection. This waveform is most often used to drive chart recorders.

Other Plug-Ins

Most any vertical plug-in may be used in a limited way with the 7S14. However, you should remember that the horizontal scan rate of the beam is not calibrated in the 7S14, and the time per division selected by the SEC/DIV switch does not set the horizontal velocity of the beam as with conventional oscilloscope time base plug-ins. The 7A13 Differential Comparator is a particular useful example, because it is often used to measure DC levels or peak signal levels when the signal waveform is of no importance. It may be placed alongside the 7S14 to produce a time-shared three-trace display when the 7S14 is used in the DUAL TRACE mode. The DISPLAY pushbutton on the other plug-in must be pushed to display a signal with that plug-in.

With the four-hole mainframe series, it is possible to use a horizontal plug-in and a vertical plug-in in conjunction with the 7S14. This is particularly useful in that the same mainframe can be used to troubleshoot the 7S14.

For a complete explanation of uses of the mainframe, refer to the operating manual for the particular mainframe.

APPLICATIONS

Introduction

The display waveform on the crt screen propagated by a 7S14 is a plot of voltage per unit equivalent time. Since the 7S14 has calibrated deflection factors both vertically and horizontally, the sampling system can be used for making accurate voltage and time measurements of an input signal.

The 7S14 offers dual-trace capabilities that allow the user to simultaneously view two signals and determine the time and amplitude relationship between the two signals. In addition, dual trace operation allows interactive displays of the two signals; e.g., X-Y and added algebraically.

The 7S14 also provides a two-dot time-interval measurement that provides a means of measuring the time between two points of a display. The two dots represent two points in time on the delaying sweep of the 7S14.

The dual trace capabilities and the two-dot system provide a great versatility for measurements. Some of the applications will be discussed in the following paragraphs.

PHASE DIFFERENCE MEASUREMENTS

The time difference between two sine-wave signals of the same frequency may be measured by using one of the signals as the reference and observing the phase difference between the reference and the second signal. There are two convenient methods of measuring the phase difference using the 7S14. The main differences in the two methods are in terms of accuracy and convenience.

Signals other than sinusoidal can be measured using these techniques, but the discussion here will be confined to sine-wave applications. With signals other than sine waves, the resultant display will depend on the waveshape of the applied signal. The calculation methods given in this discussion apply only to sine-wave signals.

X-Y Phase Measurements

When displaying sinusoidal signals, the X-Y phase measurement method provides a Lissajous display. This method can be used to measure the phase relationship of two identical frequencies, or to display the frequency relationship between two signals that are harmonically related. Other uses for the Lissajous display are to check distortion of a signal or as a "null detector" for accurately matching phase. X-Y phase measurements can be made up to the bandwidth limit of the sampler. This is possible because sampling requires high-frequency circuitry only at the input to the system; low frequency measurement techniques are used through the amplifiers and to produce the display.

To set up the 7S14 for a correct X-Y display, push the following buttons: CH 1 Y CH 2 X, INT CH 1, AUTO TRIG, +SLOPE, and REP. Set the DELAYING SWEEP and DELAYED SWEEP controls to .1 μs. Connect one of the signals to both inputs through a power divider and identical cables. Adjust the DC OFFSET and TIME DIFF controls for a straight-line display, slanted from the upper right toward the lower left corner of the crt. Adjust the deflection factors of both channels, using the variable controls as necessary, to obtain a display that is exactly six divisions both vertically and horizontally. The display should appear similar to Fig. 4-1, indicating that the cables and two channels have been matched for minimum difference.

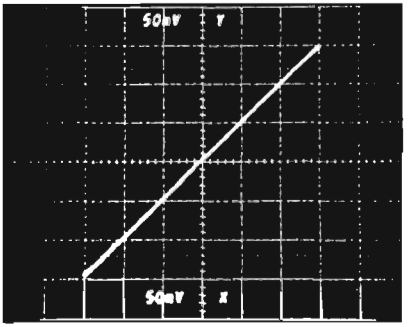

Fig. 4-1. An X-Y display of two in-phase sine wave signals.

Disconnect the power divider and connect the signals to be measured to the two inputs using the same cables used in the set-up. Check that the display is still six divisions both vertically and horizontally; adjust the deflection factor as necessary for the correct display. A difference in phase between the two signals is shown by the amount of opening in the loop. A circle display shows 90° phase difference and a straight line from the upper left to lower right shows 180° phase shift. The phase difference between two signals can be accurately measured by reading the lengths A and B, as shown in Fig. 4-2, and applying the formula:

$$\sin \theta \approx A/B.$$

The Lissajous figure can be used as a null indicator, to adjust the phase shift through a device, or between devices. To do this, the 7S14 must be set up for an X-Y display and

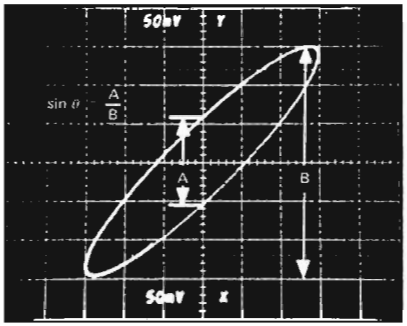

Fig. 4-2. Phase difference between two signals.

the delay compensation adjusted as described before. After the delay compensation has been adjusted, apply the signals to the inputs through the cables used for the set-up. Then, calibrate the unit under test for a "null" (zero delay) indication, as shown by a straight line display from the upper right to lower left of the graticule. Other reference points can be chosen such as a full circle to indicate 90° delay, straight line from upper left to lower right for 180° delay, or any other display which indicates the desired amount of delay.

The "null" display can also be used to make accurate frequency adjustment. After setting up the system with the reference signal, connect the signal to be adjusted to the other input. As the frequency of this signal is adjusted, a stable Lissajous display will be obtained only when the frequencies of the two signals are matched. At other frequencies, the display will appear to rotate on screen.

Dual-Trace Phase Measurement

This phase measurement methode provides a very accurate means of determining phase difference, where very small differences exist between the two signals. For this measurement, the signals must be the same frequency.

To set-up the 7S14 for correct display, push the following buttons: CH 1, INT CH 1, AUTO TRIG, + SLOPE, and REP. Connect the primary or reference signal to both inputs through a power divider and identical cables (the same cables which will be used for the measurement). Adjust the DELAYED SWEEP (light gray) control and the SWP VAR (CAL) control so that one complete cycle of the signal spans exactly eight horizontal divisions. This calibrates the system in terms of degrees/division such that there is 45°/division (i.e., 360° is equal to 8 divisions).

Now push both CH 1 and CH 2 buttons simultaneously for dual-trace operation. With the same vertical deflection on both channels, adjust the CH 1 and CH 2 DC OFFSET and TIME DIFF controls so that the two traces coincide. Disconnect the power divider and reconnect the reference signal to the Channel 1 Input. Connect the other signal to the Channel 2 Input. If necessary, adjust the vertical deflection factors so that the waveforms are the same height vertically. Now measure the distance between the corresponding points on the waveform and multiply by 45°/division to determine the exact phase difference. For small phase differences, a more precise measurement can be made by using the delayed sweep for magnification (do not change the variable control setting). The magnified horizontal rate can be determined by dividing the previous rate (45°/division) by the amount of magnification. Fig. 4-3 shows a typical magnified display.

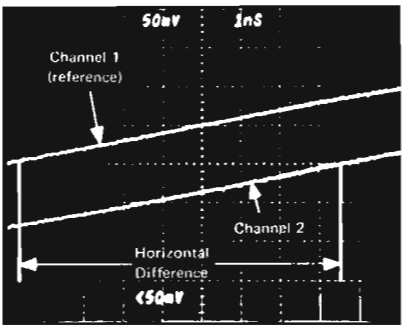

Fig. 4-3. Magnified display of signal with a small phase difference.

TIME DIFFERENCE MEASUREMENTS

The basic techiques of time-difference measurements are the same as for phase measurements. This measurement method is normally used when viewing two signals that are not time related. After setting the instrument up in the same manner as described for Phase Difference Measurements and connecting the two signals to the Channel 1 and Channel 2 Inputs, adjust the vertical deflection factors, if necessary, so that the waveforms are the same height vertically. Adjust the time per division so that the points on the two waveforms between which the time-difference measurement is to be made, are displayed within the graticule area. Now measure the distance between the desired points on the two waveforms and multiply it by the time per division. This will provide accurate time difference if the DELAYED SWP VAR control is in the calibrated position when the measurement is in the Delayed (SWP button out) Mode. When in the Delaying Mode the variable control has no effect.

TWO-DOT MEASUREMENTS

The two-dot measurement method permits more accurate time-measurement of signals. The following are examples where the two-dot system is useful.

Phase Measurements Using the Two-Dot System

For signals where the time/division is set at 10 ns/division or greater, a faster, more accurate phase measurement can be made using the two-dot system. The two-dot system is more accurate because the time base accuracy can be ignored. The two-dot phase measurement is made in the following manner.

Set up the 7S14 by pushing the following buttons: CH 1 and CH 2, INT CH 1, SWP, AUTO TRIG, and REP. Connect the primary or reference signal to both inputs through a power divider and identical cables. Adjust the DELAYING SWEEP (dark gray) control for maximum horizontal display for one complete sine wave. With the same vertical deflection on both channels, adjust the CH 1 and CH 2 DC OFFSET and TIME DIFF controls so that the two traces coincide exactly. Disconnect the power divider and reconnect the reference signal to the Channel 1 Input. Connect the other signal to the Channel 2 Input. If necessary, adjust the vertical deflection factors so that the waveforms are the same height vertically. This should create a display similar to that shown in Fig. 4-4.

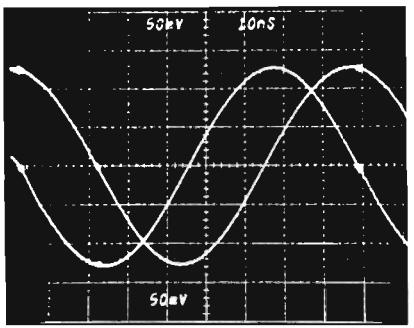

Fig. 4-4. Display of phase difference with two-dot system.

Once you have the signals displayed as in Fig. 4-4, the DELAY ZERO (1st DOT) control is used to set the first dot to the point where the reference waveform first crosses the horizontal centerline. The DELAY TIME MULT (2nd DOT) control is set to position the second dot to the point where the reference waveform crosses the horizontal centerline one complete cycle later. Note the reading on the DELAY TIME MULT dial (the number of dial divisions corresponds to 360°, or one cycle). Now change the DELAY TIME MULT control to move the second dot to where the second waveform first crosses the horizontal centerline and note the reading on the DELAY TIME MULT dial. The phase difference between the two signals is calculated using the formula:

$$\text{Phase Difference} = \frac{\text{Second DTM Reading}}{\text{First DTM Reading}} \times 360^\circ$$

Pulse Width Measurements

Pulse width measurements are often necessary, and while they are not particularly difficult, they can be time consuming. This is especially true if the 50% points do not conveniently fall on the vertical graticule lines of the crt. With the two-dot system, it is relatively simple to measure pulse width. The pulse to be measured is displayed using the Delaying Sweep (SWP button pushed in). The sweep rate and vertical deflection factor are selected to present the entire pulse on-screen, using as much of the screen as possible. Buttons that are to be pushed in are as follows: CH 1, SWP, AUTO TRIG, + SLOPE, and REP.

After the instrument has been set up, a signal has been triggered, and the deflection factors are chosen, turn the crt intensity down enough that the two bright dots can be easily seen. Then, adjust the DELAY ZERO (1st DOT) control so that the first dot is located at the 50% point on the leading edge of the waveform. Adjust the DELAY TIME MULT (2nd DOT) control so the second dot is located at the 50% point of the trailing edge of the waveform. See Fig. 4-5 for a typical display. The pulse width is the product of the DELAY TIME MULT dial setting and the SEC/DIV (DELAYING SWEEP) control setting.

If the rise and fall times are fast, you may notice more than one bright sampling dot on the rise and fall. This is because the bright dot occupies about one-tenth of a division on a horizontal trace. The beam is sometimes deflected vertically more rapidly than it is horizontally, so the brightened portion appears longer vertically than

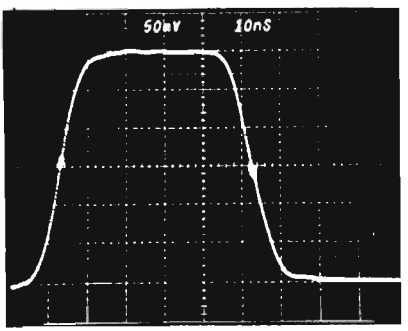

Fig. 4-5. Display of pulse width with two-dot system.

horizontally. To avoid making an error in the time measurement, make sure you set the beginning of both the "start" and "stop" dots at the 50% points. Remember that the sweep is moving left to right, so the beginning of the bright dot is at the left.

Time Between Pulses Using Dual Trace

The two-dot system is very useful for measuring the time between two independent pulses. To set up the 7S14 for a correct display, push the following buttons: CH 1 and CH 2, INT CH 1, SWP, AUTO TRIG, + SLOPE, and REP. Connect the primary or reference signal to both inputs through a power divider and identical cables (the same cables to be used for the measurement). Adjust the DELAYING SWEEP (dark gray) control for a maximum horizontal display for one complete waveform. With the same vertical deflection on both channels, adjust the CH 1 and CH 2 DC OFFSET and TIME DIFF controls to make the two traces coincide. Disconnect the power divider and reconnect the reference signal to Channel 1 Input. Connect the other signal to the Channel 2 Input.

Once the two pulses have been properly displayed, adjust the DELAY ZERO (1st DOT) control until the first dot is set to the 10% point of the rising edge of the reference pulse. Then adjust the DELAY TIME MULT (2nd DOT) control until the second dot is set to the 10% point of the rising edge of the second pulse. (The 10% points are used to provide more accurate measurements between pulses with different risetimes.) The delay between the two pulses is now determined by multiplying the DELAY TIME MULT setting by the DELAYING SWEEP SEC/DIV setting.

You will notice that there are four bright dots on-screen. The first dot on each trace indicates the delay selected by the DELAY TIME MULT control. The two dots that are not indicating a measurement point can be ignored.

There are many measurements that can be made with the 7S14. Only a few basic techniques have been presented in this section of the manual.

CIRCUIT DESCRIPTION

This section of the manual describes circuit operation of the 7S14 using a block diagram analysis. The circuit functions follow the description of each circuit. The 7S14 has triggering and time base circuits as well as vertical deflection circuits. The Vertical System is described first, followed by the description of the Horizontal System. The block and circuit diagrams at the end of the manual should be used in the analysis.

VERTICAL SYSTEM

The vertical system amplifies and attenuates the input signal. A delay line permits viewing a signal's leading edge. The two vertical channels in the dual-trace 7S14 are basically the same. The block diagram analysis discusses channel number one, with channel differences noted as they arise.

Compensation Network

The Compensation network reduces the effects of input pulse distortion in the delay line. For channel number one, the Compensation network also provides a trigger takeoff point. Input signals incur a 50% attenuation through the network, which consists of passive RC and RL components.

Delay Line

The Delay Line delays the arrival of the applied signal to the Sampling Gate long enough for the timing unit to trigger and start the ramps; this permits viewing the leading edge of signals.

Inherent with the Delay Line is some high frequency distortion (called "dribble up") of a step signal. Effects of this distortion are compensated for in the Compensation Network.

The Delay Line consists of a length of 50 ohm, low-loss transmission line with a signal propagation time of approximately 65 nanoseconds.

Sampling Gate

The Sampling Gate periodically passes a small portion of the input signal; i.e., it samples the input signal.

The gate is a bridge network consisting of a dual diode CR1 and bias cells BT1 and BT2. The diodes are held off by the cells except when strobed by Strobe Generator pulses. When the diodes are on, they pass the input signal to the Preamplifier. Only a small percent of the input signal passes through the gate because of its low transmission efficiency (sampling efficiency).

The sampled signal charges the Sampling Gate output stray capacitance, Preamplifier input stray capacitance, and Strobe Generator coupling capacitors C1 and C2. Also charging these capacitors are two positive feedback signals: one from the Preamplifier and one from the Memory. With the feedback signals, the Sampling Gate output becomes the same as the input.

Sampling Gate Blow-by Compensation

A small part of a high frequency signal couples through the capacitance of the Sampling Gate diodes when they are back biased and not conducting. This signal is called blow-by and is undesirable. A Sampling Gate Blow-by Compensation circuit inverts the input signal and applies some of it to the output of the Sampling Gate to nullify the unwanted capacitively coupled signal.

The Sampling Gate Blow-by Compensation circuit consists of: inverter Q30; an internally adjustable gain control called LF Compensation, R30; and feedback capacitor C30.

Strobe Generator

The Strobe Generator produces fast opposite polarity pulses used to turn on the Sampling Gate. It consists of avalanche transistor Q10, whose operating voltage is controlled by the voltage controller Q20 and internally adjustable Avalanche Voltage control R20.

Signals from the Delta Delay Generator drive the avalanche transistor whose breakdown characteristic gives the high speed output pulses. In the avalanche transistor output, there is a shorted transmission line that generates the pulses.

Preamplifier

The Preamplifier brings the Sampling Gate output level up to that of its input. Positive feedback via C45 from the Preamplifier output to the Sampling Gate output gives a bootstrap operation. This feedback effectively reduces the capacitance of the Sampling Gate output by charging the capacitance with the in-phase feedback signal.

Negative feedback from the voltage divider consisting of R229, R231, and R232 provides amplifier stability and

establishes loop gain. Loop Gain is internally adjustable and controlled by R232. The Preamplifier consists of a dual FET Q40 driving integrated circuit operational amplifier U10.

DC Balance and DC Balance Amplifier

In passing through the Preamplifier, the sampled signal undergoes a change in its DC level. The DC Balance and DC Balance Amplifier restores the proper DC level. It also provides a low-impedance input to the Memory capacitor C248 and the Lo Noise capacitor C247. The Balance and Balance Amplifier unit consists of internally adjustable balance control R233 and integrated circuit operational amplifier U230.

Memory Gate

Whereas the Sampling Gate has a fast risetime response, the other vertical amplifiers and circuits through which the sampled signal passes have a slower risetime response. To accommodate the slower risetimes, the Memory Gate is used.

The Memory Gate, FET Q240, acts as an on-off switch to pass the sampled signal from the DC Balance Amplifer to the Memory. Pulses that turn on the Memory Gate originate in the Strobe Logic circuits, which will be detailed later. The Strobe Logic circuits also drive the Strobe Generator and Sampling Gate; however, the Memory Gate is on longer than the Sampling Gate.

The signal passed by the Memory Gate charges one or two capacitors in its output. One capacitor, C248, is always in the circuit. The other, C247, is paralleled with C248 when the Lo Noise switch is operated. With both capacitors in the circuit the Memory Gate output cannot charge to as high a level as it could with just C248. Thus, the gate output cannot equal the input signal at the instant a sample is taken, and it will take more than one sample to display the true value of the input signal. This effect is known as "smoothing".

Memory Gating Generator

Providing turn-on pulses for the Memory Gates in both channels is a common Memory Gating Generator, Q310 and Q311. This driver amplifies and shapes strobe pulses from the Strobe Logic circuit and feeds them to the Memory Gate.

Memory Gate Blow-by Compensation

A small part of the Memory Gating Generator pulse capacitively couples through the Memory Gate via the FET gate terminal. This signal is called blow-by and is undesirable. A Memory Gate Blow-by Compensation circuit inverts the driver pulse and applies some of it to the output of the Memory Gate to nullify the unwanted capacitively coupled signal.

The Memory Gate Blow-by Compensation circuit consists of: inverter Q241, an internally adjustable gain control called Gate Balance, R242; and feedback capacitor C249.

Memory

The Memory amplifies the Memory Gate output signal and feeds back an in-phase signal to the Sampling Gate output. The amplified signal (X1 gain) drives the Post Memory Amplifier. The feedback signal combines with the positive feedback signal from the Preamplifier to keep the Sampling Gate output charge from leaking off with time. The positive feedback from the Preamplifier keeps the instantaneous charge replenished; feedback from the Memory ensures a constant charge over a long time period and for signals with a low repetition rate.

Dual FET Q140 and integrated circuit operational amplifier U140A compose the Memory. Negative feedback from the amplifier output to Q140 provides amplifier stability.

Post Memory Amplifier

The Post Memory Amplifier provides a maximum gain of 7.63, adjustable with front-panel Variable Attenuation (VOLTS/DIV CAL) control R109 and front-panel Gain screwdriver adjustment R119. DC OFFSET control R115, paralleled with FINE adjust control R114, provides a DC offset voltage to the amplifier that allows the operator to shift the vertical position of the display.

Integrated circuit operational amplifier U140B is the Variable Vertical Amplifier.

Unity Gain Inverter (Channel 2 only)

The Unity Gain Inverter inverts the Channel 2 signal to reverse its display direction; e.g., a negative-going input gives an upward display. The Channel 2 Invert switch selects the inverted mode or (in the noninvert position) bypasses the Channel 2 signal with no inversion. Channel 1 is not affected by the inverter switch.

Integrated circuit operational amplifier U350 is the Inverter Amplifier.

Output Amplifier

The Output Amplifier gives a constant output of 200 mV/Div for all operating levels of signals applied to the vertical input. The gain of this amplifier is controlled by the Volts/Div switch and is such that the overall amplification from the vertical signal input to the Output Amplifier output gives a deflection factor of 200 mV/Div at the Output Amplifier output.

Fig. 5-1 shows fixed gains of 0.5 for the Compensation Network, 7.63 for the Post Memory Amplifier (in calibrated model), and from 0.105 to 26.2 for the Output Amplifier. Other stages have unity gain. With, for example, a 2 mV signal applied to the vertical input and with the Volts/Div switch set for 2 mV/Div, the overall gain is 0.5 X 7.63 X 26.2 = 100; this gain of 100, with the 2 mV signal, gives the required 200 mV/Div deflection factor.

Integrated circuit operational amplifier U250 is the Output Amplifier.

Switching

The switching networks are common to both channels and consist of the Channel Switching Multivibrator and the Vertical Channel Switch. The Channel Switching Multivibrator is controlled by the Channel 1 - Channel 2 switches on the front panel. The multivibrator pulses the Vertical Channel Switch to select which output to display. The Vertical Channel Switch takes the pulses from the Channel Switching Multivibrator and selects the trace to be displayed by the mainframe.

The Channel Switching Multivibrator consists of transistors Q354 and Q351. The Vertical Channel Switch consists of FETs Q352 and Q353.

Vertical Power Supplies

The 7S14 vertical section contains two regulators that provide +30 V, and −30 V supplies. The remainder of the voltage supplies to the vertical section are provided by the mainframe. The Power Distribution is shown on schematics 9A and 9B at the rear of the manual.

The +30 V supply is developed by integrated circuit U1, transistor Q1 and zener diode VR610 (see Diagram 6). The −30 V supply is developed by integrated circuit U3, transistor Q3 and zener diode VR613. The above U and Q numbers are those located on the Vertical Interface board. The Vertical Interface board is shown on schematic 6 at the rear of the manual.

HORIZONTAL SYSTEM

The Horizontal System provides deflection voltage for the display oscilloscope and simultaneously controls the time at which the vertical system samples the input signal. The system uses a 150 KHz to 1 GHz trigger circuit, two fast ramps (delaying and delayed sweep) to generate the real time sweep, a slow scan ramp to generate the equivalent time sweep, an amplifier, a scan ramp inverter, a two dot position circuit for the horizontal measurement and a delay generator for the strobe drive to the vertical system.

Peak-To-Peak Signal Follower

When the Auto Trig mode is selected, the Peak-To-Peak Signal Follower provides an amplified voltage to the Triggering Level control and the Auto Baseline Trigger circuit.

The circuit has both a positive and a negative signal circuit. A positive input signal is received by transistor Q421 and passed through transistor Q430 to charge capacitor C430 to a positive peak amplitude. A negative input signal is received by transistor Q420 and passed through transistor Q520 to charge capacitor C531 to a negative peak amplitude. The +Bal and −Bal potentiometers, R524 and R521, calibrate the internal voltage level so that it is approximately ±200 mV at the outputs of operational amplifiers U430 and U530.

HF Synchronizer Oscillator

The HF Synchronizer Oscillator is used for input signals above 100 MHz and is controlled by the HF SYNC button on the front panel. The circuit is a free-running oscillator that operates from 16.5 to 25 MHz.

The circuit, consisting of tunnel diode CR221 and back diode CR220, is coupled to coil L220 and internally adjustable resistor R209, which controls the bias. When one of the diodes is in its higher voltage state, the other is in its lower voltage state, with the back diode controlling the tunnel diode to its low state. The current to the diodes is determined by the Triggering Level control, the coil determines the time each diode is turned on.

Trigger Amplifier

The Trigger Amplifier is an exclusive OR circuit, in which the first stage provides trigger polarity control. The circuit has a X25 gain. When the Triggering Level control is connected through the Trigger Level Comparator circuit, it raises or lowers the level of the trigger signal at the input to the Trigger Amplifier.

Integrated circuit U220 is the Trigger Amplifier network.

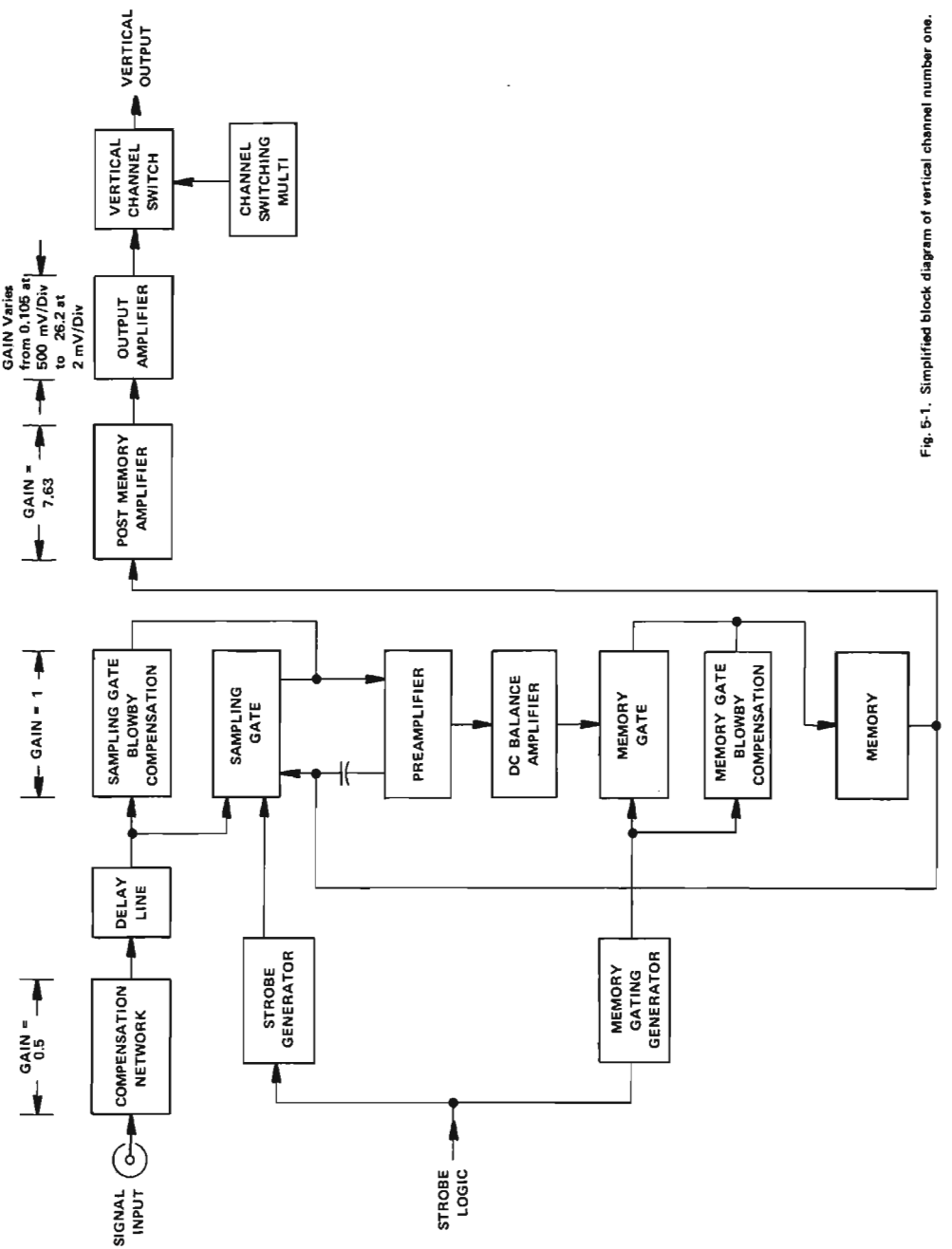

Fig. 5-1. Simplified block diagram of vertical channel number one.

Fig. 5-1. Simplified block diagram of vertical channel number one.

Holdoff Ramp Generator

The Holdoff Ramp Generator provides sweep signals to the Trigger circuit and determines the time between the sweeps.

The logic gate, consisting of diodes CR120, CR121, CR122, and CR123, senses the delaying sweep signal. When diodes CR120 and CR122 are turned on, diodes CR121 and CR123 are reverse biased, which causes transistor Q123 to be reverse biased and transistor Q124 to be turned on. In this condition, the Trigger circuit is waiting to accept a trigger signal. When a trigger signal is accepted, the delaying sweep runs down; when the delaying sweep is at its lowest level, delaying sweep transistor Q339 supplies current to the Holdoff Ramp Generator input, turning diode CR123 on and turning diode CR122 off. Diode CR120 is turned off and diode CR121 is turned on, therefore, current flowing through CR121 starts a negative-going holdoff ramp into holdoff capacitor C120. Transistor Q122 is turned on and Holdoff Schmidt U240C is returned to the holdoff condition (holdoff lockout occurs) and the Fast Ramp is returned to 0. Diode CR122 is now turned on, diodes CR121 and CR123 are turned off, and diode CR120 is turned on. The current source (Holdoff potentiometer) is passed through diode CR120, causing a positive holdoff ramp. When the holdoff turns transistor Q123 off, transistor Q124 is turned on. This puts Holdoff Schmidt U240C in the Hi state. This causes the Holdoff Lockout gates to revert; Delay gate U240A and Ramp Drive Lockout gate U260C accept a trigger signal. The time from the end of one sweep to the trigger of the next sweep is controlled by the Triggering Holdoff potentiometer R128.

Trigger Circuit

The Trigger Circuit is a logic network consisting of a Holdoff Schmidt, which is part of the Holdoff Ramp Generator circuit; the Reset and Arming Gates, which consist of the $C = \overline{A} \cdot \overline{B}$ gate and two Holdoff Lockout gates; two Delay gates; and two Ramp Drive Lockout gates. The Delay gates, $\overline{C} = A \cdot B$ gate, and the Holdoff Schmidt are contained in integrated circuit U240 and the Ramp Drive Lockout gate; the Holdoff Lockout gates are contained in integrated circuit U260. A simplified diagram is shown in Fig. 5-2 with each gate identified.

An output signal from the network occurs when the output level of the second Ramp Drive Lockout gate changes. This is caused by level changes to the inputs of the Holdoff Schmidt and the delay gate. The following is an example of how the logic of the Trigger Circuit may operate. The logic for this network is $C = \overline{A} \cdot \overline{B}$ and $\overline{C} = A + B$. Refer to Fig. 5-2 during this discussion.

Logic Example. With a negative signal to the input of the Holdoff Schmidt (U240C, pin 13), the output (pin 15) is Hi, which means the inputs of U240D (pin 10) and U260B (pin 7) are Hi. The outputs U240D (pin 14) and U260B (pin 3) are therefore Lo, which means the inputs of U260A (pins 4 and 5) are Lo. The output of U260A (pin 2) must therefore be Hi, which means the inputs of U260B (pin 6), U260C (pin 12), and U240A (pin 5) are Hi, therefore, the outputs of U260C (pin 15) and U240A (pin 2) are Lo.

If we have a negative input to U240B (pin 6) and U240D (pin 11), the output of U240B (pin 3) must be Hi, which means the input of U240A (pin 4) is Hi. The output of U240A (pin 2) and therefore, the input of U260D (pin 11) is Lo. Since the output of U260C (pin 15) is Lo, the input of U260D (pin 10) must be Lo. With both inputs of U260D Lo, the output of U260D (pin 14) must be Hi, which means the input of U260C (pin 13) is Hi.

Now, if the input U240C (pin 13) goes positive, the output (pin 15) must go Lo, which makes the inputs of U240D (pin 10) and U260B (pin 7) Lo. Since both inputs of U240D (pins 10 and 11) are now Lo, the output (pin 14) must go Hi, which means the input of U260A (pin 5) is Hi. The output of U260A (pin 2) must go Lo, which makes the inputs of U260C (pin 12) and U240A (pin 5) Lo; however, since the inputs of U260C (pin 13) and U240A (pin 4) are Hi, there is no change to the outputs of U260C (pin 15) and U240A (pin 2), so there is no change in the output signal and consequently no output signal propagation.

If the input to U240B (pin 6) now goes Hi, the output of U240B (pin 3) must go Lo, which means the input of U240A (pin 4) is Lo. Since both inputs of U240A are now Lo, the output (pin 2) must go Hi, which makes the input of U260D (pin 11) Hi. The output of U260D (pin 14) must go Lo, which makes the input of U260C (pin 13) Lo. Since both inputs of U260C are now Lo, the output (pin 15) must go Hi. This is a level change at the Trigger Circuit output, therefore, an output signal is propagated.

Fast Ramps

There are two Fast Ramp generators; the Delaying Ramp Generator and the Delayed Ramp Generator. Each Ramp has a Comparator and a Ramp Inverter. The Ramp Inverters are driven by a 1-2-5 position Timing (SEC/DIV) switch. These Ramps generate a real time sweep to provide pulses to the Delta Delay Generator and the Buffer circuit.

The trigger signals to the Delaying Ramp Generator are held off by saturation transistor Q342, which is driven by transistor Q343. Transistor Q338 is the Delaying circuit Fast Ramp current source for the timing capacitors, C239, C241, C243, C244, and C252. The timing capacitors determine the rate of the signal. The sensing transistor Q339 clamps the negative excursions of the input signal. The Comparator consists of two comparator transistors,

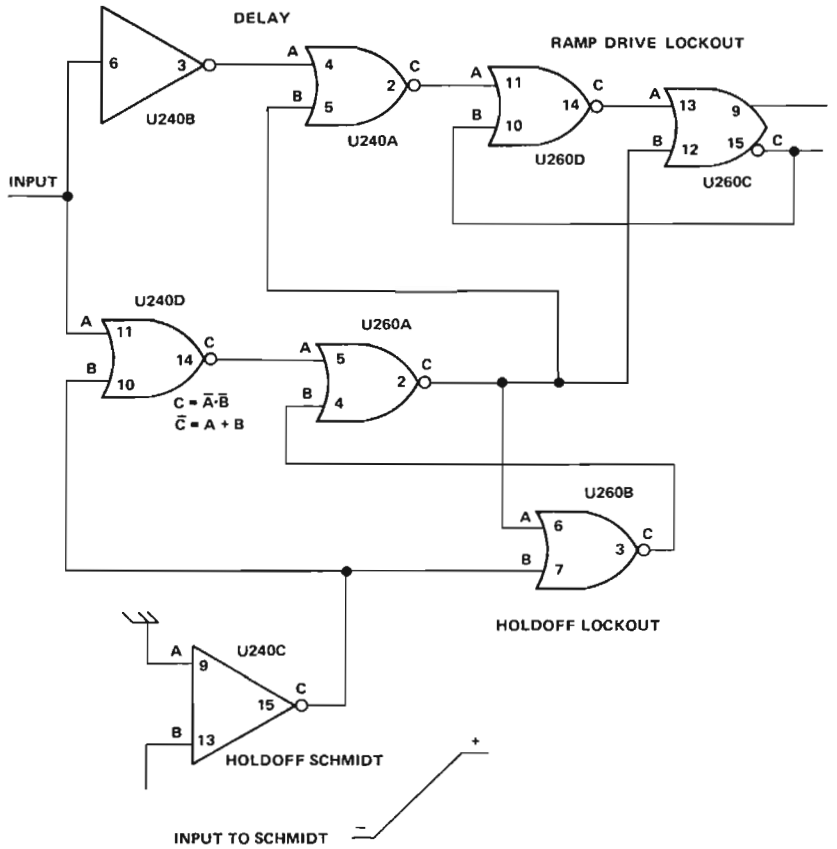

Fig. 5-2. Trigger Circuit Logic.

Q356 and Q357, with output provided by two line receivers, U455A and U455B. The level of the comparator transistors is determined by the Ramp Inverter U355, which is driven by the Timing switch. Resistor R230 is used to balance the input to the Inverter.

When Comparator transistor Q356 is on, transistor Q357 is off, therefore, the output (pin 2) of line receiver U455A is Hi and the output (pin 3) of line receiver U455B is Lo. At the comparison level, transistor Q357 is on and transistor Q356 is off. This makes the output (pin 3) of receiver U455B go positive and the output (pin 2) of receiver U455A go negative, which provides drive to the saturation transistor Q362 in the Delayed circuit.

The Delayed Fast Ramp Generator operates the same as the Delaying circuit, except that there is a tunnel diode (CR459) in the Comparator of the Delayed circuit that sharpens the delayed strobe output so that the output is independent of the ramp rate.

Delta Delay Generator

The Delta Delay Generator produces pulses that drive the Channel 1 Strobe Generator, Channel 2 Strobe Generator, and Memory Gating Generator. Two voltage comparators, contained in integrated circuit operational amplifier U470, make up the Delta Delay Generator.

One input to each of the two comparators is a reference voltage. The other input is a step from the delayed sweep circuit. When these two inputs are equal, the comparator produces an output pulse (comparator output rises). When the comparator input step ends, the comparator output falls and ends the output pulse.

Front panel CH 1 TIME DIFF CH 2 control R139 controls the comparator reference voltage. A change in this voltage changes the time when the two comparator output pulses start, relative to one another. This change, in turn, changes the time when the Channel 1 and Channel 2 Sampling Gates sample signals. A maximum of approximately 2 nanoseconds difference between the channels is possible.

Buffer

The Buffer circuit is a Schmidt with constant time feedback. It drives the Interdot Blanking Pulse Generator, Gating Generator and Scan Ramp Gating Multivibrator. In addition, it also drives the vertical Memory Gating Generator.

The Buffer consists of integrated circuit operational amplifiers U470A and U470B, and a capacitor C474 that determines the time constant for all trigger rates.

Scan Ramp Gating Multivibrator

The Scan Ramp Gating Multivibrator gates the Scan Ramp to generate equivalent time sweep. Among some of the functions performed by the Scan Ramp Ramp Gating Multivibrator are the sensing of sweep lockout, single sweep start, providing axis gating, and controlling the reset of the Scan Ramp and Staircase Generator.

The circuit consists of integrated circuit U390.

Interdot Blanking Pulse Generator

The Interdot Blanking Pulse Generator takes an output from the delayed strobe drive to create blanking and drive the alternating multivibrator signal. The circuit consists of a transistor Q590 and two capacitors C492 and C173.

Inverter, Gating Generator and Gated Current Generator

The Inverter is a multi-purpose operational amplifier, U490, which accepts an external scan ramp and provides an output either as a horizontal scan or as scan current to the Gated Current Generator. The Gating Generator takes output from the Buffer and provides drive to the Gated Current Generator by means of transistor Q480 and diode CR480. The Gated Current Generator is a current generator that is gated by an inverter Q380. It provides an output signal to the Scan Ramp and Staircase Generator.

Scan Ramp and Staircase Generator

The Scan Ramp and Staircase Generator is an integrated circuit integrater with various ramps. The circuit is controlled by the Gated Current Generator and Scan Ramp Gating Multivibrator. When the circuit is in the Single Scan mode, it saturates at approximately 12 V. By pushing the START button, diode CR280 will be returned to its Lo state and the circuit can receive the next pulse.

The Scan Ramp and Staircase Generator circuit consists of integrated circuit U280, diode CR280, and two timing capacitors C280 and C281.

Two Dot Circuit

The Two Dot Circuit provides horizontal comparison for the two dots. The circuit contains the Two Dot Pulse and Delay Generator, Delay Voltage Follower, and 1st Dot Stop circuit.

The Two Dot Circuit produces two current sources through transistors Q139 and Q141. One source is for the delay multiplier stop and the other source is for calibration of the DELAY ZERO (1st DOT) and DELAY TIME MULT (2nd DOT) controls. The current sources are calibrated by variable resistors R130 and R131. The DELAY ZERO (1st DOT) control is adjustable over nine cm of the delaying sweep display, the DELAY TIME MULT (2nd DOT) control is adjustable over ten cm of display, and the time multiplier between the dots is read directly on the Delay Time Mult dial.

Input to the Two Dot Circuit is provided by the Scan Ramp and is compared against the voltages of the 1st and 2nd Dots. The comparator offset (dot width) is determined by resistor R161. As the Scan Ramp goes from 0 to 10 volts, the 1st and 2nd dot comparator inputs are traversed so that the first crossing turns the dot on and second crossing turns the dot off.

The 1st dot stop circuit is required to stop the 2nd dot from going beyond the right hand edge of the display; thus the reading on the dial is always correct.

The Delay Voltage Follower circuit consists of integrated circuit U145B. The Delay Generator consists of the integrated circuit U145A, variable resistor (1st dot stop control) R130, diode CR150, transistors Q139, Q141, Q142, and Q143. The Two Dot Pulse circuit consists of integrated circuits U150 and U155.

Intensity Blanking Mixer

The Intensity Blanking Mixer is a circuit that intensifies each dot width received from the Two Dot circuit and provides blanking during the time the sampler is taking a new sample.

Transistor Q160 is used to intensify the dot and transistor Q161 is the blanking transistor in the Intensity Blanking Mixer circuit.

Position Voltage Follower and Horizontal Amplifier

The Position Voltage Follower is the operational amplifier U180A used as the horizontal position calibrator. Input current to the Voltage Follower is provided by variable resistor R100. The output of the Position Voltage Follower and the horizontal drive current are summed by the the Horizontal Amplifier. The selection of the Vertical Mode Switch determines the drive (sawtooth or X from Channel 2 Vertical Amplifier) to the Horizontal Amplifier. The Horizontal Amplifier is an operational amplifier U180B that provides input to the Sweep Calibrator R183.

Readout

Readout Logic is provided to the oscilloscope readout circuitry by signals from the readout board. The logic to the readout board comes from the Channel 1 and Channel 2 attenuator switches of the vertical section and from the Delaying Sweep and Delayed Sweep sections of the Timing switch of the horizontal section.

The Readout logic is shown on schematics 3 and 5C in Section 9 of the manual. For more specific information on the readout circuitry, refer to the Circuit Description section of your Tektronix 7000 Series oscilloscope manual.

Horizontal Power

The power to the Horizontal section of the 7S14 is supplied by the vertical section of the 7S14 and the mainframe of the 7000 series instrument used. The Power Distribution is shown on schematics 9A and 9B at the rear of the manual.