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7L18 SPECTRUM ANALYZER

INTERIM SERVICE

INSTRUCTION MANUAL

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INTRODUCTION

This is an interim service manual. It is our intention to provide as much and as complete information as possible to aid in servicing. We welcome all suggestions, corrections, criticizms, and contributions you care to make.

The 7L18 Spectrum Analyzer is a three-unit-wide plug-in unit for Tektronix 7000-Series oscilloscope mainframes. The analyzer covers the spectrum range from 1.5 GHz to 18 GHz in five bands with direct input, and 12.5 GHz to 60.5 GHz in six bands with external waveguide mixers. The instrument features digital storage, internal preselector, a dynamic range of 80 dB, less than 10 Hz of incidental oscillator frequency modulation, and a resolution bandwidth range of 30 Hz to 3 MHz. Further description and complete specifications appear in the Operator's Manual.

Although the 7L18 is a highly complex instrument with high component density, its modular design aids its serviceability. IC and transistor sockets are used where possible, and most circuit card interconnections are made via plugs rather than soldered connections. Adjustment and test point locations are conveniently located where possible. Modular design should reduce instrument downtime by allowing defective modules to be exchanged. Much of the troubleshooting and circuit description information will be module-oriented.

CIRCUIT DESCRIPTION

INTRODUCTION

The circuit descriptions in the following sections are intended to give an overview of the 7L18's functions. This should aid in troubleshooting the various systems in the instrument. It may also aid in understanding how to utilize the full capabilities of the 7L18 for particular applications.

A simplified block diagram of the 7L18 is located on the first tabbed pull-out sheet. The blocks on this diagram represent two types of circuits: control circuits and signal circuits. The control circuits include the sweep generator, span attenuator, oscillators and drivers, and switching circuits necessary to make the instrument function. The signal circuits include the attenuator, preselector, mixers, amplifiers, filters, and other stages that process the signals to form the crt display. Not included in this diagram are the switching functions and control logic, and front panel controls. All blocks are discussed in greater detail in the following sections. The numbers in the diamonds refer to the corresponding schematic diagrams. Note that these numbers on block diagram 1 provide an index of most of the schematics (not all schematics are referenced on the block diagram).

PRESELECTOR AND FIRST LOCAL OSCILLATOR ◇2◇

The first local oscillator of the 7L18 operates in the 2 to 4 GHz region. With the 510 MHz intermediate frequency, the input frequencies that may be tuned using a fundamental conversion are 1.5 to 3.5 GHz or 2.5 to 4.5 GHz (bands 1 and 2). With higher input frequencies, conversions are with harmonics of the local oscillator frequency (for the actual harmonics used, refer to Table 1-1 in the Operator's Manual). The oscillator's fundamental or harmonic is 510 MHz away from the displayed signal, either above or below, depending upon the band being used.

The preselector and first local oscillator utilize YIG (Yttrium-Iron-Garnet) spheres. This material resonates at a frequency which varies in proportion to the magnetic field caused by a current through an electromagnet. The preselector is a tunable bandpass filter with a bandwidth of about 50 MHz. It is tunable through the range of 1.5 to 18 GHz, and tracks the portion of the spectrum being displayed.

Since the intermediate frequency is relatively low compared to the operating frequencies and available spans, and since the mixer produces many harmonics, the instrument is potentially capable of many conversions other than the one intended. The preselector selects which conversion is allowed. This results in a spurious-free, unambiguous display.

Internally, the preselector consists of three cascaded sections. Each section contains a YIG sphere and input and output loops oriented so that their axes are perpendicular to each other and to the applied magnetic field. The resonant frequency of the filter is proportional to the applied magnetic field.

The preselector, as well as the YIG oscillator, is not repairable in the field, and should be returned to the factory in case of failure.

FIRST CONVERTER 2

In the first converter, incoming signals from the preselector are mixed with the first local oscillator signal to produce a 510 MHz intermediate frequency (*if*). The mixing action is accomplished by the inherent nonlinearity of the diode in assembly A45.

The first converter assembly also serves to route signals to the front panel EXT MIXER connector. This connector supplies the local oscillator signal and dc bias to the mixer, and also receives back the intermediate frequency from the mixer.

INTERMEDIATE FREQUENCY AMPLIFIERS 3

The heterodyne action of the mixer produces an intermediate frequency signal that contains a frequency component for every frequency component in the input, but is translated in frequency. These offset signals sweep past the 510 MHz input frequency of the first *if* amplifier; a deflection is produced on the analyzer screen each time a frequency component falls within the *if* passband. A logic signal controls whether the waveguide bands input or the coaxial bands input to the *if* amplifier is enabled.

The *if* amplifier uses three or four stages of gain with two stages of PIN diode attenuation. The attenuators change gain as necessary to accommodate changes in attenuation of the first converter with different bands.

THREE-CAVITY FILTER 3

The output of the 510 MHz *if* amplifier is applied to a three-pole bandpass filter with a bandwidth of 3 MHz. The filter network consists of three helical resonators, and is the main selective element in the analyzer when operated in the 3 MHz resolution bandwidth position.

500 MHz LOCAL OSCILLATOR, CALIBRATOR, AND SECOND CONVERTER 4

The second local oscillator uses a 125 MHz fifth overtone crystal, and has a tuned output. The oscillator signal then passes through two frequency doublers, a leveling attenuator, a power amplifier, and a band pass filter, then is coupled to the second converter and the calibrator circuit. The calibrator includes a harmonic generator which generates a series of frequency markers with 500 MHz spacing. The 1500 MHz marker is accurately adjusted to −30 dBm by a control in the leveling loop.

The second converter mixes the 510 MHz *if* output from the three-cavity filter with the 500 MHz second local oscillator to produce the 10 MHz second intermediate frequency.

VARIABLE RESOLUTION FILTERS 5 6

The variable resolution circuitry includes the six resolution bandwidth filters and their switching circuits. The switching is done with diodes which are driven from a CMOS analog switch. The six bandwidths available are from 3 MHz to 30 Hz in decade steps. A combination of L-C filters and crystal filters are used to obtain the desired bandwidths. The filtering for the four wider bandwidths are contained in the VR module, while the 30 and 300 Hz filters are placed elsewhere in the instrument with double shielded coaxial cables used for interconnection. The 30 Hz filter also includes a built-in oven to ensure stability of its high Q crystals. The operating frequency of this system is 10 MHz.

The variable resolution section also provides several gain controlling functions. The front-panel mounted AMPLITUDE CAL potentiometer is used for amplitude calibration of the instrument; the amplifier that is controlled is in the input of the variable resolution section. Similarly, the REF VAR control (which is uncalibrated) interfaces with a PIN diode in the later part of the variable resolution system. Additionally, fixed gain steps may be added in this amplifier in amounts of 10, 20, or 30 dB. These gain steps, in conjunction with others in the log amplifier (described later) allow the user to place the instrument noise floor on screen for any resolution bandwidth condition.

NOISE FILTERS 8

The noise filters reduce the bandwidth of the amplifiers feeding the log amplifier. This function is required in order to minimize the baseline noise that might result from noise generation in the latter stages of the variable resolution amplifiers.

LOG AMPLIFIER 8

The log amplifier compresses the input signal before sending it to the detector. This compression makes it possible for the input signal to vary over a 90 dB range while feeding the detector which is linear over a 35 dB range. By carefully controlling the characteristics of the compression curve, each dB change in the input results in an equal increment of output. For instance, in the 10 dB/DIV mode, each time the input varies 10 dB in amplitude, the output varies by one division.

DETECTOR 9

The detector circuit, included on the Video Amplifier diagram, changes the 10 MHz signal to a dc level that varies in accordance with the log of the signal amplitude.

VIDEO AMPLIFIER 9

This diagram shows the detector and video amplifier circuits. The detector circuit utilizes an operational amplifier to linearize the detection process. The detected video passes through a ripple filter to the first video amplifier where it is offset (this corresponds to a gain change before the log amplifier) and the gain is set for the display in use (10 dB/DIV or 2 dB/DIV). If LIN mode is selected, a four-segment shaper is used to "un-log" the video. The pulse stretcher and deflection amplifiers are also on this circuit board.

SWEEP GENERATOR 11

The sweep generator produces a sawtooth waveform that is used to sweep the crt horizontal axis, the YIG oscillator, and the YIG preselector. The sweep generator circuitry includes the triggering, selection of sweep speeds, and horizontal axis mainframe drivers. Refer to the table on Horizontal Sweep Diagram 11 for sweep speed selection logic.

The sweep generator uses two ICs. U1480 is the sweep control, and U1560 is the sweep generator. U1480 and its associated circuitry control the various events of the sweep cycle. Immediately after every sweep there is a holdoff period during which another sweep cannot occur. After this period, if the sweep is not in single sweep mode, the sweep runs after an interval determined by the bright baseline timing components (R1488 and C1489). If a trigger occurs (and the sweep is in a triggered mode) after the end of holdoff and before the end of the bright baseline interval, the sweep starts immediately. To initiate the sweep, $\overline{\text{GATE}}$ from U1480 goes low. This signal is inverted by Q1540 and applied to U1560. The high level at U1560 turns off an internal reset transistor, allowing U1560 output to ramp positive at a rate determined by a capacitor (C1555, C1557, or C1559, depending upon sweep speed) and the input current. When the ramp reaches the threshold voltage (set at 8.5 V) of a comparator in U1560, the comparator sends a signal back to U1480 to raise $\overline{\text{GATE}}$. This sets up the next holdoff period and turns on an internal reset transistor which shorts between the output and the summing node of the integrator, discharging the sweep capacitor.

If the sweep is in the single sweep mode, only one sweep will occur each time the SGL SWP button is pushed. There is no bright baseline in triggered modes in single sweep; unless FREE RUN is selected, the sweep will wait indefinitely for a trigger. This allows easy external triggering for photography. The READY indicator is on from the time the switch is pressed until the sweep ends. The holdoff time is determined by components external to U1480, and is changed with the sweep speed (not at every step, but whenever the sweep capacitor is changed, and at certain other places).

The selection of modes is done with three lines of U1480. Pin 13, when low, enables bright baselining. Pin 6, when low, selects single sweep mode. Pin 7, when taken high briefly, resets the single sweep, allowing one sweep. Pushing SGL SWP (when in single sweep mode) during a sweep will reset the sweep and start another, subject to trigger mode. The interfacing to the front panel triggering switches is done with discrete diode and transistor logic. Only one button is required for selection of single sweep mode and the initiation of each sweep. Pressing SGL SWP does not cancel the trigger source (LINE, INT/EXT, or FREE RUN), allowing either triggered or free-running single sweep operation. Pressing any other trigger control cancels SGL SWP.

The front panel switches control trigger source selection through three units of a quad comparator (U1410). The comparators—one each for INT, EXT, and LINE—have open collector outputs which are wire-OR'ed. The INT and EXT comparators are enabled together. Each comparator is disabled when the + input is taken high, and is enabled when the + input is brought to ground, allowing a signal on the − input to switch the comparator. Because of the sensitivity of the INT and EXT comparators, both inputs are referenced to the control line so that the TTL low of about 0.3 V will not falsely trigger the comparators. A clamp on the − input ensures that the + input goes higher when the comparator is disabled. The common output is sent to the trigger input of U1480.

Triggering takes place at zero volts, positive slope. Sensitivities are 0.5 division peak-to-peak for INT and 0.5 V peak-to-peak for EXT. LINE is dc-coupled, while INT and EXT are ac-coupled. An amplifier (U1390) in front of the INT comparator provides the required sensitivity.

The sweep lockout signal from the mainframe is interfaced through U1401 to pin 10 of U1480. When the sweep lockout is high, it ends any sweep in progress and prevents another sweep from occurring, irrespective of the settings of the trigger controls. The forced single sweep line places the sweep in single sweep and free run modes.

The sweep time per division code is obtained from the microcomputer through the 8 bit of port 0, and stored in an eight bit shaft register (U1530). Three bits are used to select a timing resistor, two to select a timing capacitor, one to select the voltage which drives the timing resistor, and two to change the holdoff time.

The sweep speed has an eight decade range, from 1 μs to 20 s/division. The fastest two decades—to 20 μs/div— are covered by switching resistors. The capacitor is then switched, and the resistor sequence is switched again for the next two decades. For the next decade, the voltage is lowered and the last three resistors are switched with the same capacitor. The same sequence of switched capacitor, switched resistors, then switched voltage is repeated for the last three decades. The resistors are switched by a single-channel analog multiplexer (U1540) and the capacitors by half of a dual-channel unit (U1545). The other half of U1545 switches capacitors for the holdoff timing. Other holdoff capacitors are switched by transistors to change holdoff at points where the sweep capacitor is not changed.

In the manual and single sweep modes, the sweep capacitor is replaced by a resistor, making U1560 into an operational amplifier. U1540 selects either the manual span voltage or external voltage as an input source. The external input connector is the same as that used for external trigger. Level is 0 to 10 $\pm$1 volts for a full-screen sweep. U1545 grounds the base of the transistor which inverts $\overline{\text{GATE}}$. This ensures that the gate to U1560 is always high regardless of the state of U1480, keeping the reset transistor off and the crt unblanked.

A line from the front panel OPTION connector switches input and feedback resistors onto U1560 to place the sweep voltage in the center of its range. This line also inhibits the timing current.

The voltage reference for the sweep is derived from the −50 V supply. U1610 develops a +9.0 V output.

U1595 is a selectable gain amplifier (selector switch is Q1610) which has an output of either −0.9 V or −9.0 V. R1597 is part of the timing resistance. Q1595 switches in R1594 to form a voltage divider to lower the voltage, thus slowing the sweep to generate the MAX SPAN marker.

The $\overline{\text{GATE}}$ signal from U1480 is buffered and sent to the digital storage board, where it is used to control mainframe unblanking in the non-storage mode. The $\overline{\text{GATE}}$ signal is also ANDed with the $\overline{\text{READY}}$ signal (pin 9) which is low when the sweep is ready for triggering. The ANDed signal is buffered and sent as the holdoff signal to the mainframe. The outputs of U1480 are combined with information from the SGL SWP switch to derive the drive signal for the READY indicator.

The output of U1560 goes directly to the span attenuator board for driving the oscillators. It also goes to an amplifier which drives the A and B Sweep inputs of the mainframe. After amplification on the span attenuator board, the sweep goes through the SWP CAL control to the digital storage board. Either this sweep or the digital storage readout sweep is sent back to the sweep horizontal board. The horizontal amplifier sums this signal with that from the HORIZ POSITION control, and drives the mainframe at 50 mV/division on each side.

SPAN ATTENUATOR 12

The span attenuator controls the amplitude of the sweep signal that is coupled to the first LO driver or the phase lock circuitry, thus controlling the YIG oscillator frequency deviation to set the span, or frequency/division. Refer to Figures 2-1 and 2-2 for attenuator settings for phase locked and non-phase locked operation, respectively, and to Figure 2-3 for a block diagram. When phase locked, the ramp must also be scaled as a function of the phase lock harmonic, which varies with center frequency tuning. The scaling is done automatically by programmable fixed and variable attenuators. The fixed attenuator is a simple divider which can reduce the ramp by powers of ten. The variable attenuator handles the high-resolution part of the scaling.

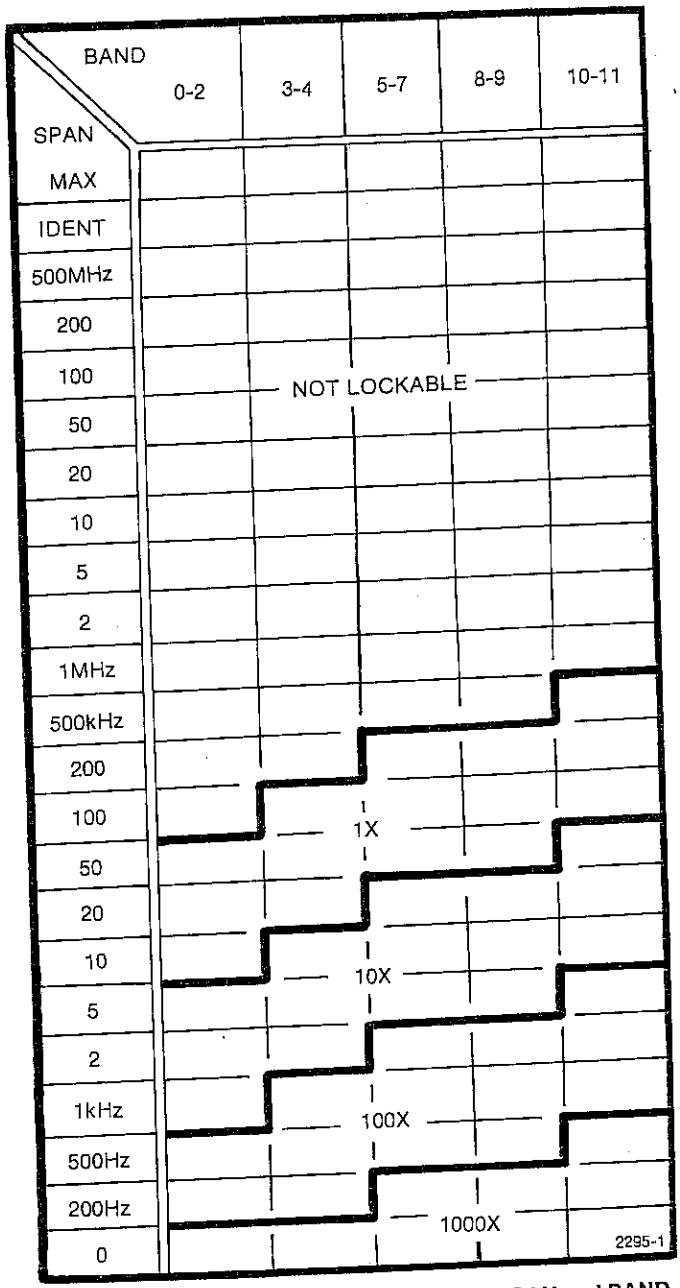

Figure 2-1. Fixed span attenuator selection vs SPAN and BAND settings for phase locked operation.

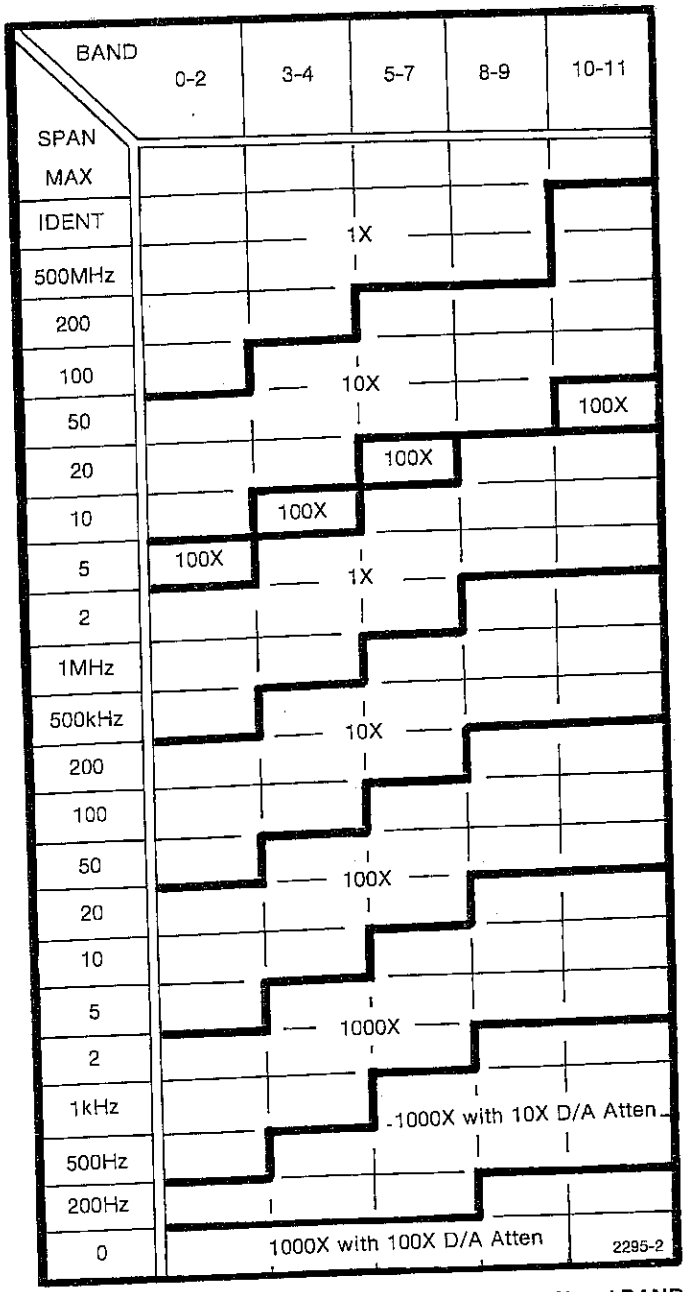

Figure 2-2. Fixed span attenuator selection vs SPAN and BAND settings for non-phase locked operation.

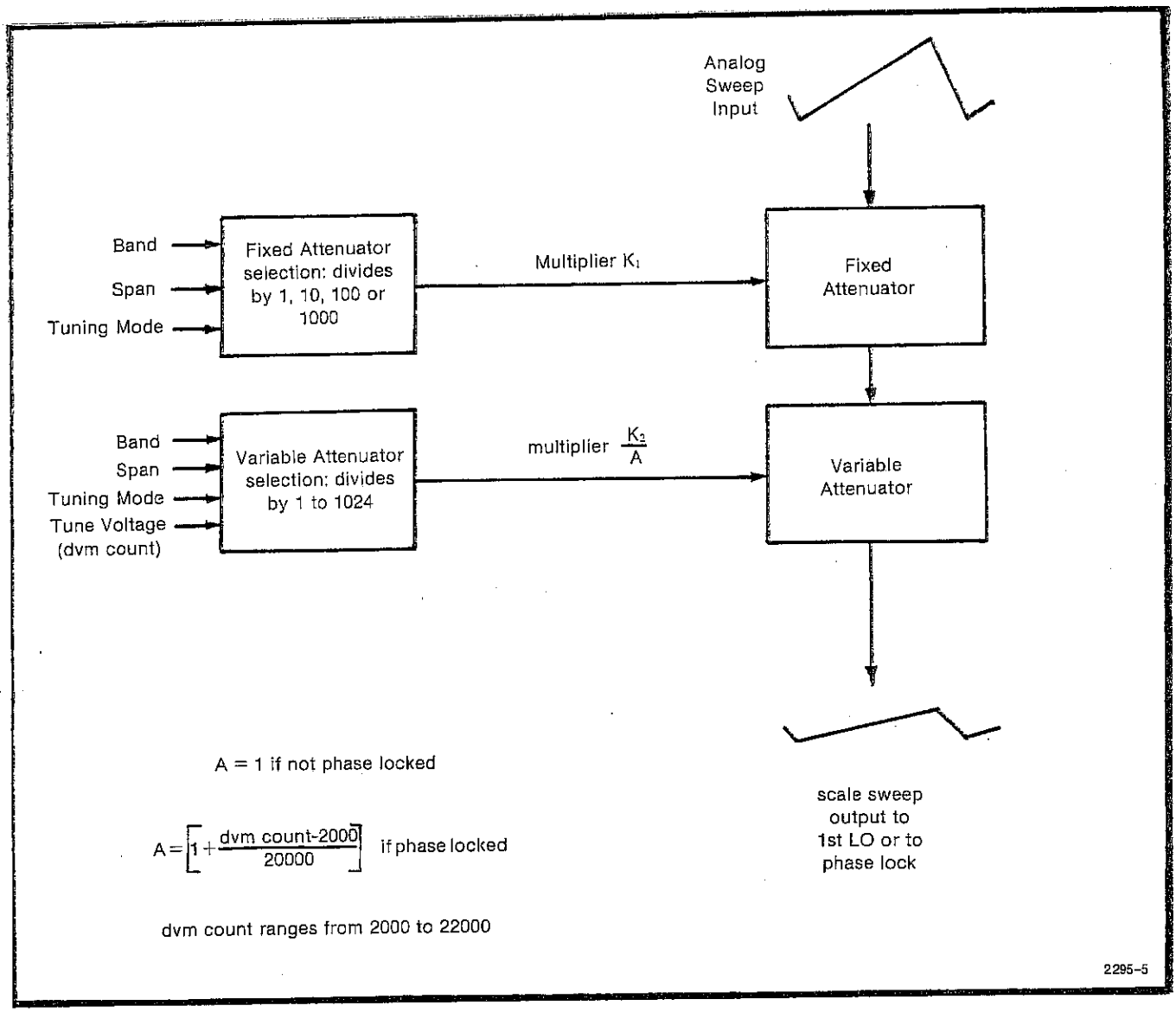

Figure 2-3. Span Attenuator block diagram.

FIRST LO AND PRESELECTOR DRIVER 13 14

The First Local Oscillator and Preselector Driver receives the attenuated sweep voltage, combines it with the TUNING voltage, and converts it to a current that drives the first local oscillator main tuning coil. The current also drives the preselector tuning coil, but is first multiplied and offset according to the band in use, in order to provide proper tracking.

On narrower spans depending on the band in use, only the TUNING voltage signal is applied to the main tuning coil, and the oscillator is swept by either applying the attenuated sweep voltage directly to the fm coil, or indirectly through the phase lock circuitry.

A different multiplier and offset is used for each band. Adjustments can be made on offset and multiplier for each band; one control moves the adjustment range up and down, while the other rotates it about the center point.

In MAX SPAN the local oscillator sweeps over its full range. A marker is generated by comparing the sweep and tune volts in the driver, and sending a signal back to the sweep to slow it down briefly, so that on fast sweeps (when the sweep is faster than the flicker rate) it appears as a bright spot, and on slow sweeps it appears as a pause.

The YIG oscillator board is soldered to the YIG oscillator terminals, interfacing the oscillator to the cables coming from the instrument. In addition, it holds the noise filter capacitors for the main oscillator coil, the relay for switching the capacitors, and a clamp diode for the oscillator collector supply.

REFERENCE VOLTAGE BOARD 14

This circuit generates the reference voltages used for the CENTER FREQUENCY TUNING controls, and for the first local oscillator driver offsets.

The voltage reference for the supply is filtered and applied to an amplifier with a variable gain that allows precise voltage settings. The output of this amplifier is the −10 V reference. The −10 V is inverted by another amplifier to produce the +10 V reference. Both amplifiers have output buffers. Resistors with extremely low temperature coefficients are used in critical places to ensure temperature stability.

PHASE LOCK SYSTEM 15 16 17 18

Because it must tune and sweep, the first local oscillator does not have the stability of a fixed oscillator. Since the drift of the oscillator is indistinguishable from drift of a signal, the 7L18 includes a system which, at narrower spans, phase locks the first local oscillator to a stable sweeping source. This gives the locked oscillator approximately the same fractional stability as a crystal oscillator. The sweep is then applied to the phase locked loop, rather than to the oscillator directly.

The phase lock circuitry is discussed in two parts. The first part, called the inner loop, covers the generation of the strobe, or reference frequency, to which the YIG oscillator is locked. The second part, called the outer loop, discusses the circuitry necessary to lock the YIG oscillator to the strobe.

Inner Loop

The inner loop includes three oscillators (refer to Figure 2-4): a crystal reference oscillator, a movable reference oscillator (referred to as the offset oscillator), and the controlled oscillator, which is phase locked to the sum of the reference and offset oscillators. Controlled oscillator frequency = Reference oscillator frequency + offset oscillator frequency/64. The controlled oscillator frequency (16 MHz) is divided by four and used as the source for the strobe driver. This strobe is the reference to which the first local oscillator is phase locked.

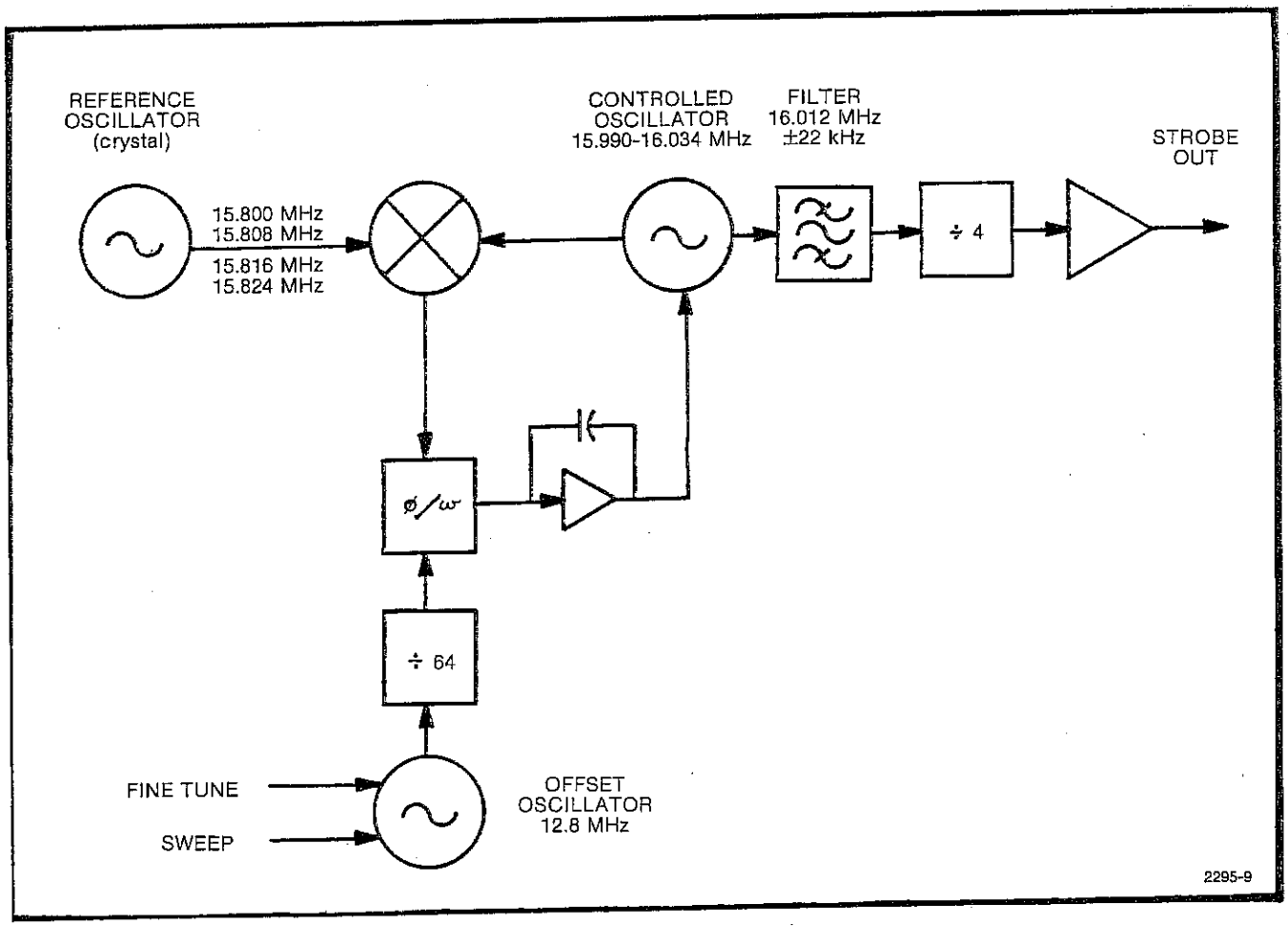

Figure 2-4. The inner loop serves as the frequency reference for the outer loop of the phase lock system.

Outer Loop

The outer loop locks the YIG oscillator to the reference (refer to Figure 2-5), and performs a host of other functions as follows:

Connects the compensation amplifier to the YIG oscillator when in phase lock positions.

Provides search when not locked.

Provides a time delay from when the strobe is turned on to when the error amplifier is connected.

Varies lock-in range as a function of tune voltage.

Commutates between crystals in the reference oscillator.

Locks the YIG oscillator to the strobes.

Senses when lock is achieved.

Moves the strobe reference to recenter the YIG oscillator.

Connects the sweep and offset oscillator filter after lock occurs.

Limits hold-in range.

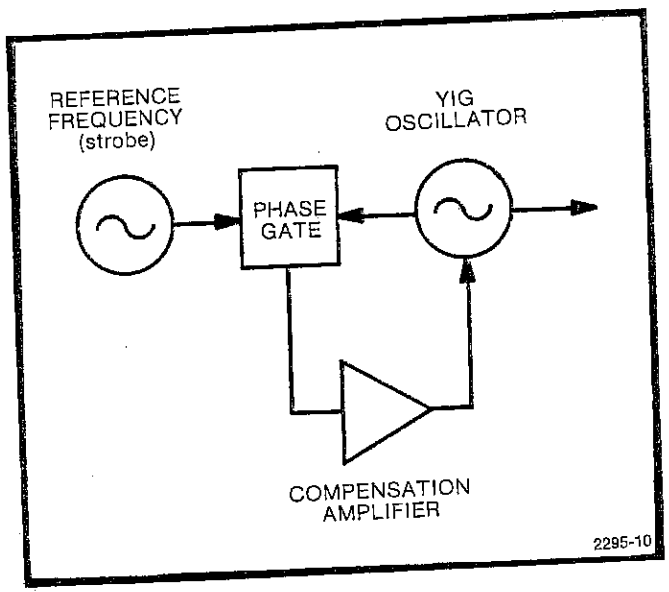

Figure 2-5. Outer loop of the phase lock system.

The **compensation amplifier** and **search oscillator** form a conditionally stable amplifier that requires the phase lock loop to have acquired, to become stable. When the loop is not locked, the compensation amplifier oscillates at about a 3 Hz rate. As the amplifier oscillates, the YIG oscillator searches an amount somewhat greater than 2.4 MHz.

The search voltage moves the oscillator more than the distance between strobe lines to ensure that neither temperature effects nor dc balance errors from the phase gate will change the lock-in range. As we discussed earlier, the lock-in range when the YIG oscillator is at 2 GHz must be greater than 1 MHz, the spacing between crystals, and less than 1.2 MHz, the maximum recenter range of the offset oscillator. At 4 GHz these numbers are 2 MHz and 2.4 MHz respectively.

The output voltage of the search oscillator is monitored, and when this voltage exceeds an absolute value determined by the tune voltage, a Lock Inhibit command is given. In this manner, the allowable lock-in range is varied a factor of two as the oscillator is moved from 2 to 4 GHz.

If the allowable lock-in range is exceeded, the oscillator was not able to acquire lock with the crystal in use, and a new crystal is selected. The inner loop has time to settle before the search oscillator comes back into lock-in range and the new crystal is tried.

Eventually the YIG oscillator locks to the strobe reference and the search oscillator stops oscillating. After a fixed period of time has elapsed to ensure that the lock is real, lock is sensed, and the crystals are no longer allowed to change.

Next, the YIG oscillator is recentered so that an on-screen signal will be in the same place it was before lock was initiated. This is done by applying a correction voltage to the offset oscillator from an 8-bit digital-to-analog converter, until the error voltage from the phase gate is zero. This converter is very stable to ensure low drift of the offset oscillator. If, for some reason, the converter doesn't have enough range to recenter the oscillator, the lock sequence is started again, with provisions to ensure that the next crystal in the sequence is tried first.

After the YIG oscillator is locked to the strobe reference and returned to the frequency it was before lock was initiated, the sweep voltage is connected to the offset oscillator to sweep the reference. The bandwidth of the outer loop must be wide enough, about 10 kHz, to ensure that the loop remains locked during sweep and retrace. The hold-in range of the loop is about 4 MHz to allow for the sweep, fine tune range, and drift of the oscillator.

DISPLAY MODE AND DEGAUSS SWITCHES 

The display mode switches (10 dB/DIV, 2 dB/DIV, LIN) control the decoding of the display mode for the crt readout, and send a display mode control signal to the log amplifier and vertical board. The 10 dB/DIV switch also indicates to the microcomputer when this mode is selected. (The microcomputer uses this information to limit the maximum *if* gain allowed in the 10 dB/DIV position.)

The DEGAUSS switch shorts the main oscillator and preselector coils when pushed. This sets the current in the coils to zero and establishes a known magnetic history in the cores.

MICROCOMPUTER 21

The microcomputer takes care of a variety of housekeeping functions within the 7L18: it reads the settings of most of the front panel controls and appropriately services the sweep generator, span attenuator, first local oscillator and preselector drivers, *if* amplifier gains and bandwidths, center frequency dvm, and crt and front panel readouts. From the user's point of view the microcomputer is most apparent in the 7L18's AUTO modes: when AUTO BANDWIDTH and AUTO TIME/DIV are selected, these functions are based upon the BAND, SPAN/DIV, and PHASE LOCK control settings (refer to Operator's Manual, Sections 3.3.2.1 and 3.5.3).

The microcomputer consists of a microprocessor plus the assembly of the I/O (Input/Output) buffers, ROM, etc. The microprocessor controls everything except the trigger and the display, which are hard-wired, and the TUNING controls; all other controls are fed to the microcomputer through the data bus. The microcomputer uses about 3000 instructions, which are contained on the ROM ICs. Each controlled condition is set up and latched at the particular interface address, so that the microcomputer does not have to continually service a port; it only does so when a condition changes (front panel setting, etc).

The First Local Oscillator and Preselector Driver Interface controls the band the filter is on, whether a marker is generated or not (markers are generated only in MAX SPAN), blanking (blanking is different on band 5 than all other bands), sweep speed, attenuation setting of the span attenuator, and readout. It also reads whether digital storage is on or not, and reads the front panel controls and dvm.

The Vertical Microcomputer Interface selects the coaxial or waveguide input to the 510 MHz *if*, controls the gain and bandwidth of the variable resolution filters, and reads the front panel controls.

In operation, the program checks the front panel; assuming nothing has changed, it reads the dvm to see if it is the same as last time. If so, it stays in this loop. When the dvm changes, it recomputes the center frequency and sends it to the readout. When a front panel control is changed, the program jumps to reload all other interfaces. A condensed block diagram of the program is shown in Figure 2-6.

CENTER FREQUENCY DIGITAL VOLTMETER 22

The center frequency dvm is a modified dual slope analog-to-digital converter which digitizes the Tune Volts from the front panel control. The digital information is sent to the microcomputer for use in computing center frequency.

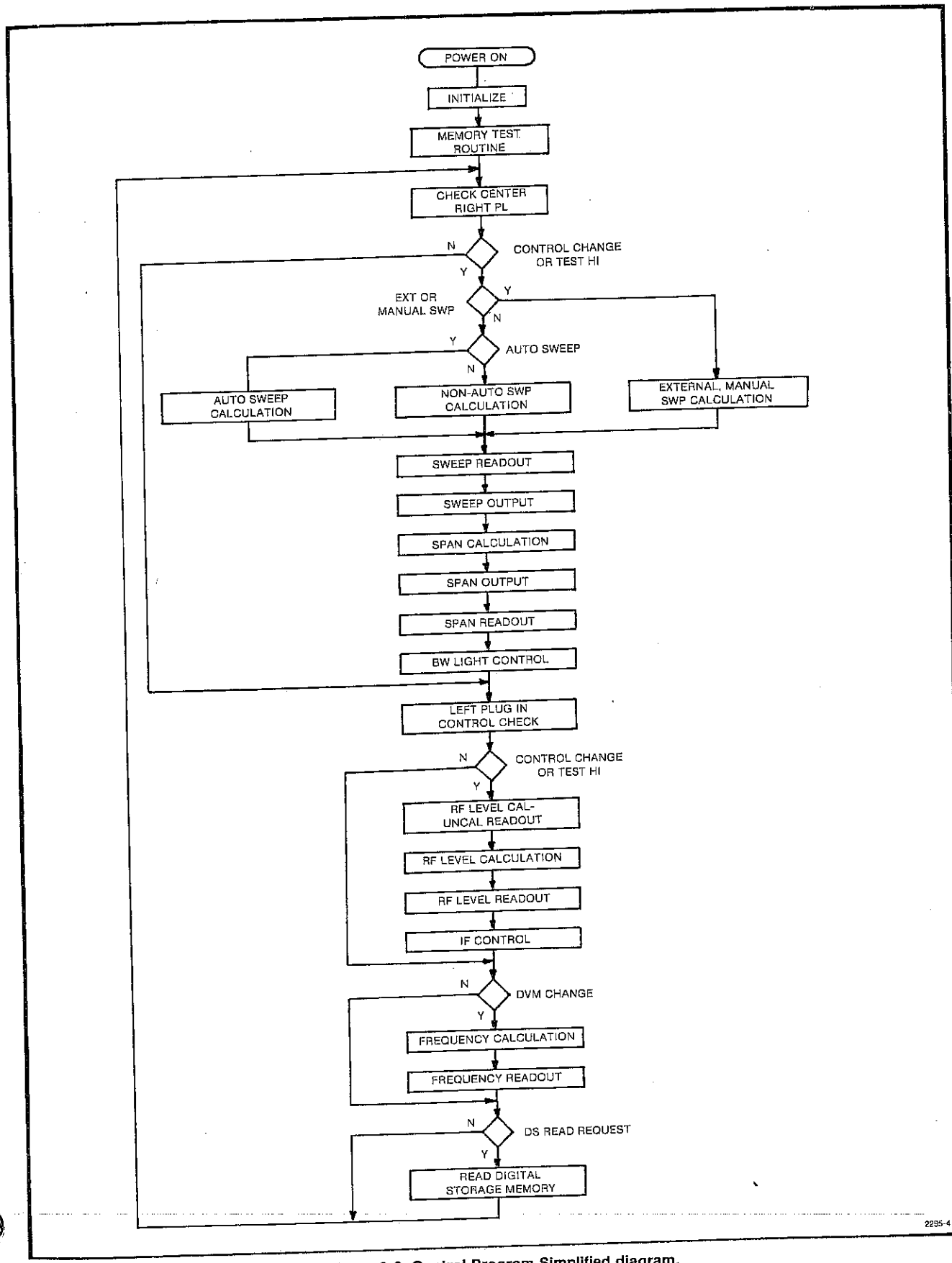

Figure 2-6. Control Program Simplified diagram.

U450 is a differential-input buffer for the Tune Volts. Adjustments R455 (Gain) and R475 (Offset) allow for calibration of the converter.

U470 is the dual-slope integrator. The slope of negative-going ramp at the output of U470 is determined by the magnitude of the current resulting from the Tune Volts input. The slope of the positive-going ramp is determined by the difference between a reference current (generated by U455 and U460) and the signal current. VR500 is the source for the reference current, as well as for an offset current which is summed with the signal current.

U490, U510D, and U480A form an 80,000 count counter which controls the operation of the converter. The clock for the counter is Q530, Q535, and associated circuitry. The counter runs cyclically. When it reaches 0, the output of U525E switches a diode switch (CR466, CR468, and CR476) to turn on the reference current, and the output of U470 ramps positive until it exceeds the threshold of U475. The output of U475 then resets the diode switch, turning off the reference current. The integrator output then ramps downward for the remainder of the cycle. When the output of U475 goes high, it also loads the count within the counters of U490 into latches in the same IC. This count is proportional to the duration of the upward ramp, and hence to the Tune Volts input. The maximum value of this count is approximately 22,000, so no information is lost by not latching the output of U480A.

The microcomputer reads the information from the latches in U490 asynchronously with the operation of the converter. It is necessary that the data in the latches not be changed during the readout; hence, the microcomputer begins reading only during the downward portion of the ramp. As the minimum duration of the upward ramp is approximately 2,000 counts, the reading operation can be completed before a new count is loaded, even if it is begun just before the ramp switches. The ramp polarity signal is coupled to the microcomputer through the 8-bit of the I/O bus when port 10 is addressed.

The data is read from the latches as five BCD digits, sequenced onto the data bus by a multiplexer internal to U490. Before starting to read data, the microcomputer must know that the scanner is on the least significant digit. This information is transferred from the Q_A output of U490 through U540A to the 1-bit of the status port. If necessary, the microcomputer steps the scanner by writing to the status port.

When the scanner is in the right position, the microcomputer switches to port 11 and reads the BCD digits, writing to port 11 to step the scanner after each read. The data appears on the bus in complemented form.

CENTER FREQUENCY AND CRT READOUT BOARDS ◇23◇ ◇24◇

The readout boards interface the microcomputer bus to the mainframe readout system, enabling the 7L18 to display its control settings on the crt. These boards also drive the front panel CENTER FREQUENCY and REFERENCE LEVEL LED displays.

Figure 2-7 shows the physical location of the different blocks of the 7L18 readout system. The shift registers and their controls are identical for the Center Frequency and Reference Level portions of the circuit. All three switch logic blocks are different internally since they must display different types of data. The specific codes required to setup the displays are shown in Table 2-1. The specific signal lines that connect to these two boards are shown in Table 2-2.

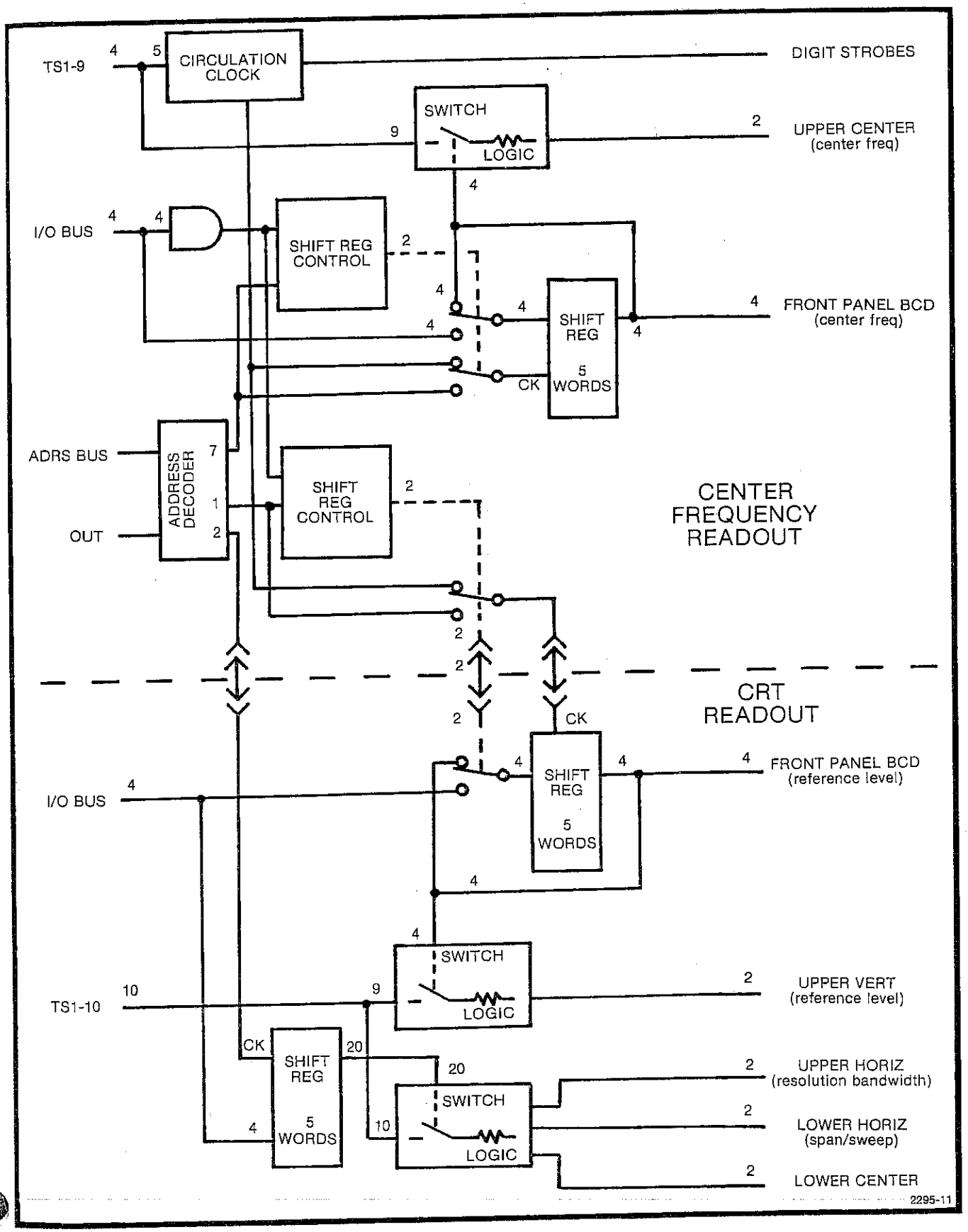

Figure 2-7. Readout block diagram.

Table 2-1

DISPLAY CODES

Port	Display	Function	Contents	Word
7	Center Frequency (loaded in MHz, decimal point to display GHz)			
		Reset to load mode	15	1
		Digits 0—9	BCD code	2-6
		Space (Blank)	12	2-6
1	Reference Level (dBm)			
		Reset to load mode	15	1
		Calibrated	4	2
		< uncalibrated	5	2
		> uncalibrated (UNCAL lit)	6	2
		Digits 0—9	BCD code	3-6
		+	10	3-6
		−	11	3-6
		Space	12	3-6
2	Resolution Bandwidth			
		3 MHz RES	8	1
		300 kHz RES	7	1
		30 kHz RES	5	1
		3 kHz RES	4	1
		300 Hz RES	3	1
		30 Hz RES	1	1
	Span/Sweep Span (Span displayed unless in 0 span, when sweep displayed)			
		0 Hz	display	sweep
		200 Hz	2,2, 8	2,3,4
		500 Hz	4,2, 8	2,3,4
		1 kHz	1,0, 9	2,3,4
		2 kHz	2,0, 9	2,3,4
		5 kHz	4,0, 9	2,3,4
		10 kHz	1,1, 9	2,3,4
		20 kHz	2,1, 9	2,3,4
		50 kHz	4,1, 9	2,3,4
		100 kHz	1,2, 9	2,3,4
		200 kHz	2,2, 9	2,3,4
		500 kHz	4,2, 9	2,3,4
		1 MHz	1,0,10	2,3,4
		2 MHz	2,0,10	2,3,4
		5 MHz	4,0,10	2,3,4
		10 MHz	1,1,10	2,3,4
		20 MHz	2,1,10	2,3,4
		50 MHz	4,1,10	2,3,4
		100 MHz	1,2,10	2,3,4
		200 MHz	2,2,10	2,3,4
		500 MHz	4,2,10	2,3,4
		IDENTIFY	0,0,12	2,3,4
		MAX	8,0, 2	2,3,4

Table 2-1 (cont)

DISPLAY CODES

Sweep External (no display)		0,0, 0	2,3,4
	Manual (no display)	0,0, 0	2,3,4
	Auto (display calculated sweep)		
	20 s	2,1, 4	2,3,4
	10 s	1,1, 4	2,3,4
	5 s	4,0, 4	2,3,4
	2 s	2,0, 4	2,3,4
	1 s	1,0, 4	2,3,4
	500 ms	4,6, 4	2,3,4
	200 ms	2,6, 4	2,3,4
	100 ms	1,6, 4	2,3,4
	50 ms	4,5, 4	2,3,4
	20 ms	2,5, 4	2,3,4
	10 ms	1,5, 4	2,3,4
	5 ms	4,4, 4	2,3,4
	2 ms	2,4, 4	2,3,4
	1 ms	1,4, 4	2,3,4
	500 μs	4,10,4	2,3,4
	200 μs	2,10,4	2,3,4
	100 μs	1,10,4	2,3,4
	50 μs	4,9, 4	2,3,4
	20 μs	2,9, 4	2,3,4
	10 μs	1,9, 4	2,3,4
	5 μs	4,8, 4	2,3,4
	2 μs	2,8, 4	2,3,4
	1 μs	1,8, 4	2,3,4

Table 2-2

INTERFACE CHART

Center Frequency Readout		CRT Readout		
Function	Level	Pin	Function	Level
I/O 8	5 V logic in	1	REF LVL C	0 to − mA out
I/O 4	5 V logic in	2	REF LVL R	0 to − mA out
I/O 2	5 V logic in	3	LWR CTR R	0 to − mA out
I/O 1	5 V logic in	4	LWR CTR C	0 to − mA out
CF BCD 4	5 V logic out	5	SPAN/SWEEP R	0 to − mA out
CF BCD 2	5 V logic out	6	SPAN/SWEEP C	0 to − mA out
CF BCD 1	5 V logic out	7	RES BW C	0 to − mA out
CF BCD 8	5 V logic out	8	RES BW R	0 to − mA out
+5 V	5 V supply	9	n.c.	
GND	common	10	REF LVL BCD 8	5 V logic out
−15 V	−15 V supply	11	REF LVL BCD 4	5 V logic out
REF LVL LOAD	5 V logic out	12	REF LVL BCD 2	5 V logic out
REF LVL RUN	5 V logic out	13	REF LVL BCD 1	5 V logic out
DIGIT 5 (MSD)	5 V logic out	18	REF LVL CLOCK	5 V logic in
DIGIT 4	5 V logic out	19	n.c.	
DIGIT 3	5 V logic out	20	"−" SIGN	5 V logic out
DIGIT 2	5 V logic out	21	REF LVL RUN	5 V logic in
DIGIT 1 (LSD)	5 V logic out	22	REF LVL LOAD	5 V logic in
OUT	5 V logic in	26	I/O 1	5 V logic in
ADR 1	5 V logic in	27	I/O 2	5 V logic in
ADR 8	5 V logic in	28	I/O 4	5 V logic in
ADR 4	5 V logic in	29	I/O 8	5 V logic in
ADR 2	5 V logic in	30	CRT LOAD	5 V logic in
CRT LOAD	5 V logic out	35	TS 1	−15 V pulse in
REF LVL CLOCK	5 V logic out	36	TS 2	−15 V pulse in
TS 5	−15 V pulse in	37	TS 3	−15 V pulse in
TS 6	−15 V pulse in	38	TS 4	−15 V pulse in
TS 4	−15 V pulse in	39	TS 5	−15 V pulse in
TS 3	−15 V pulse in	40	TS 6	−15 V pulse in
TS 2	−15 V pulse in	41	TS 7	−15 V pulse in
TS 1	−15 V pulse in	42	TS 8	−15 V pulse in
TS 7	−15 V pulse in	43	TS 9	−15 V pulse in
TS 8	−15 V pulse in	44	TS 10	−15 V pulse in
TS 9	−15 V pulse in	45	+5 V	5 V supply
CTR FREQ C	0 to −1 mA out	46	GND	common
CTR FREQ R	0 to −1 mA out	47	−15 V	−15 V supply

The circulation clock strobes the center frequency and reference level shift registers to circulate their data. This clock also produces the digit drive signals to tell the front panel displays which digit to display the current data in. These digit strobes are generated by a divide-by-five circuit that is derived from the shift register clock. To allow compatability with the mainframe readout system, the clock must circulate the registers in synchronism with the readout time slot signals. When no time slot signals are being received, an internal clock is allowed to run at about a 5 kHz rate, about the same rate as the time slot signals. When readout signals are received, this internal clock is stopped. A clock signal is derived from the time slot signals, ensuring proper synchronization with the time slot signals.

The address decoder monitors the address bus and the OUT line to determine when data is being sent to the readout system. The Center Frequency has been assigned to port 7; the Reference Level to port 1; the Resolution Bandwidth and Span/Sweep to port 2.

Since both the center Frequency and Reference Level readout circuits are identical except for the switch logic, the following description serves both. The shift register control basically controls a switch that determines whether the five-word shift register is to load new data or circulate the currently stored data. When a 15 is received on the I/O bus concurrent with an address strobe from the address decoder, the control throws the switch to the load position. After five additional words, none of which is of value 15, have been received and loaded in the shift register, the control is ready to throw the switch to the circulate position. In order for the proper data to be displayed in the proper position, the throw of the switch is delayed until the time the first character is normally displayed.

Since the Resolution Bandwidth and the Span/Sweep are displayed only on the crt, no circulation clocks are needed. When data is received from the I/O bus, the address strobe from the address decoder shifts the current data down one position and loads the new data at the top of the register. Normally five words are received during a short period of time to help prevent the display from blinking. The data is updated only when the front panel switches are changed.

The blocks labeled Switch Logic are basically switches that choose the proper currents to tell the mainframe which character to display. The currents are generated when a time slot line is pulled to −15 volts by the mainframe.

DIGITAL STORAGE 

The 7L18 has built-in digital storage, so a storage mainframe is not required. When digital storage is selected, the display is a presentation of a large number of memory locations, which stay at previously determined amplitude until updated. An intensified marker shows the point at which the memory is being updated.

Graphical presentation of mathematical functions or data is a common practice. One class of graphs are those which have a single Y value for each X coordinate. An alternate representation for a graph would be a two-column table, where the X coordinates and Y value for each X coordinate were simply listed. If the first X coordinate and the spacing between X coordinates were known, then the two-column table could be reduced to a single column and the X coordinate would be implied by the position of the Y value in the table. This is the essence of digital storage. The vertical analog voltage (Y value) is converted to a binary number and stored in a table. The location in the table is determined by the analog sweep voltage (X coordinate). Once the table is created, the function can be recreated by converting the tables values and table positions to analog voltages.

This digital storage system has two tables (memories) labeled A and B. Table B (B memory) is always updated on every sweep; Table A (A memory) is not changed if SAVE A control line is true. There are 512 A values and 512 B values. The spacing between X coordinates is the same in each table, but the origin of B is shifted such that the X coordinates of A and B are interlaced.

When the stored digital data is recreated, the user has the option of displaying either A, B, or both. If SAVE A is true, when both tables in memory are displayed, then all saved data in A is displayed and all of updated data in B is displayed alternately. When SAVE A is not selected, then sequential interlaced values of A and B are displayed as one trace with 1024 positions. A third trace option, called B—A is also available. The displayed values are the difference between the B and A values for the same X coordinate.

Since a function is continuous and a table has values for discrete X coordinates, an algorithm is used to determine the Y value to be stored for a particular X value. This system allows the user to select one of two methods for determining Y values: peak or average. The Y analog signal is continually being sampled. The number of samples depends upon the speed of the analog sweep voltage. For one X coordinate, there are always at least two samples, and there may be as many as 2^{17}. From this set of samples the user can select the largest sample value, called peak value, or the mean of all the samples, called average value. This selection is controlled by the PEAK/AVERAGE logic signal. This logic signal is created by comparing a dc level with the analog vertical signal input. The dc level is set with the front panel PEAK/AVERAGE control; when the input is below the level, average is chosen; when the input is above the level, peak is chosen. This dc level appears on the display as a positionable horizontal line. The logic line, named "cursor" is created by switching the dc level to the analog output during the marker cycle.

Superimposed on the cursor is an intensified spot or Update Marker, which shows the X-coordinate at which new Y values are being computed. Update Marker is formed by comparing the analog sweep input to the display analog X output, and forcing the sweep to pause, increasing the marker intensity.

The heart of the digital storage system is two ICs, U3526, and U3585. U3526 contains the vertical acquisition, vertical display, peak detection, signal averaging, Z axis blanking, and special Y-value processing circuits. U3585 contains the horizontal acquisition address counter, horizontal display counter, 10 bit RAM address multiplexer, and a programmable logic array system control matrix. External to the two chips are two eight-bit digital-to-analog converters, two ten-bit digital-to-analog converters, one ten-bit latch, 8k bits of random access memory, and all required analog functions. Timing is controlled by clock pulses arriving at pin D8 from the microprocessor board at about a 1 MHz rate.

Vertical Section. The vertical analog voltage is converted to a Y value binary number using an eight-bit successive approximation register U4710. Eight clock cycles are required to perform an analog-to-digital conversion. For one clock between each conversion the successive approximation register produces a low-going pulse called $\overline{\text{SYNC}}$; most functions are related to this synchronizing pulse.

The averaging circuit, contained within U3526, has three distinct parts: (1) the accumulation of all Y values for a particular X coordinate (numerator); (2) the number of samples comprising the numerator (denominator); and (3) the subtract-and-shift circuit which performs the division.

Another section of U3526 compares incoming Y values with those previously stored for each X coordinate, and retains the larger. A built-in multiplexer then selects either the average or the peak value to be routed to the memory, based on the PEAK/$\overline{\text{AVG}}$ signal.

When the MAX HOLD logic signal is high, U3526 stores in memory the larger of the current memory value or the previously-selected peak/average value, for each X coordinate.

All data enters and leaves the memory serially. Data read from the memory enters an eight-bit shift register, and, timed by $\overline{\text{SYNC}}$, is transferred to the vertical display output latch. Since this shift register is also used for other purposes, the DISPLAY ENABLE signal prevents non-display information from being transferred to the output latches. One example of other data moving through this register is during a B—A display, described below.

When B—A is selected, the actual expression implemented is B—A+K, where K is a serial input external constant specified by the user. This permits placing the B—A=0 point at any level on the display (refer to Section 3). To avoid confusion, the display is blanked when B—A+K is off screen.

U3526 contains a three-bit synchronous counter which identifies which bit of the eight-bit vertical value is to be read or written by the memory. This is the only memory addressing done by the device; all other addressing is under the control of U3585.

Horizontal Section. The analog sweep voltage is converted to an address for the current table value by the use of a ten-bit tracking analog-to-digital converter. As the sweep moves to the right, the counter increments; as the sweep retraces, the counter decrements. The increment clock is $\overline{\text{SYNC}}$; the decrement clock is the basic 1 MHz system clock. When the SAVE A line is high, the counter skips every other binary number; thus, only B coordinates appear as addresses.

The display is produced by reading from memory the Y value and converting it and its X location to analog voltages. The counter which cycles through all the X locations is located on U3585. As the counter cycles, it may be interrupted by a START DIVIDE signal; a multiplexer switches the memory address from display to acquisition.

The "intelligence" for the system is contained in a ROM, which performs several functions:

a. it controls which trace is going on screen;

b. it decides when to switch from read to write;

c. it generates the B—A coordination signals with U3526;

d. it controls the incrementing of the display counter;

e. it handles requests for the memory bus.

When an external device wishes to read or write memory contents, it must request permission by allowing BUS REQUEST to go high. U3585 will then seek an eight-cycle clock sequence which will not interfere with its functions. When that time becomes available, U3585 pulls BUS REQUEST low, signaling the start of a request cycle. For the next eight clock cycles, all address lines and the read/write line go to the high-impedance tristate mode.

When a display mode is not selected, it is skipped by U3585. The highest possible refresh rate is obtained at this time.