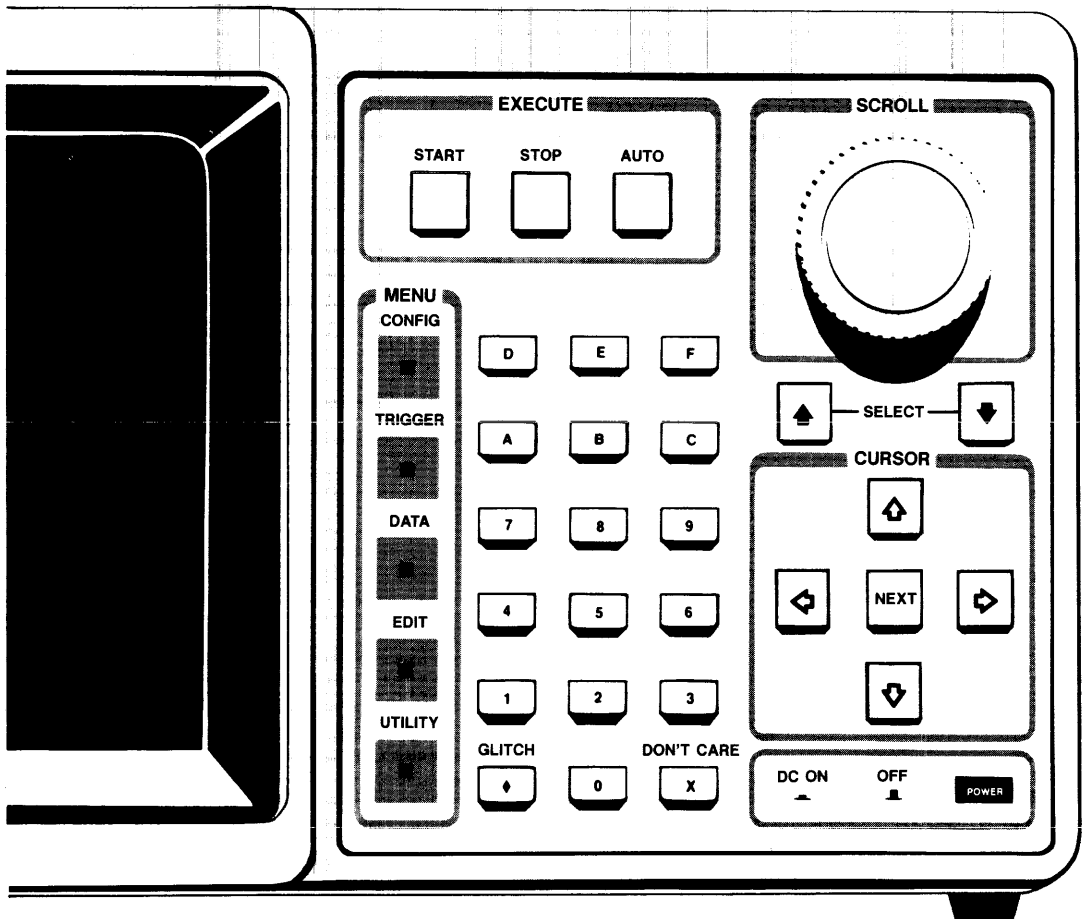


# The **1240/1241** Logic Analyzer



The  
**1240 / 1241**  
Logic Analyzer

OPERATOR'S MANUAL

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## MANUAL REVISION STATUS

**Product: 1240/1241 Logic Analyzer**

This manual supports the following versions of this product: All.

REV DATE	DESCRIPTION
MAY 1985	First Printing
NOV 1985	Revised: pages--4-17, 8-8 & 8-22.
NOV 1986	Revised: add page--Soft Key LED Cleaning Requirements to be inserted by operator before the Color Display tab.



## PREFACE

This manual is intended for use with Tektronix 1240 and 1241 Logic Analyzers. The 1240 is a configurable logic analyzer with a monochrome CRT display screen. In comparison, the 1241 Logic Analyzer offers a three-color display screen and a vertical expansion feature for timing diagram displays.

Both 1240 and 1241 Logic Analyzers use the 1240D1 (9-channel) and 1240D2 (18-channel) data acquisition cards. The sample menu displays in this manual are based on a 1240 or 1241 equipped with two 1240D1s and two 1240D2s.

Operating information for compatible COMMunication, ROM, and RAM packs is not contained in this manual. Refer to the documentation that accompanies these products for complete installation and operating instructions.

Several copies of the *1240/1241 Reference Guide* are provided with each logic analyzer. This guide provides brief descriptions of the logic analyzer menus and is a valuable quick-reference tool.

## HOW TO USE THIS MANUAL

Descriptions and procedures contained in this manual apply to both 1240 and 1241 Logic Analyzers, unless otherwise specified.

This manual is designed around the 1240/1241 menu groups represented by the MENU keys on the front panel. Each menu group has its own section in this manual. Within each section, menu descriptions follow the order of the soft key arrangement along the top of the screen, left to right. Other manual sections cover power-up and operator checkout procedures, and general reference information. Section 2 provides several setup examples for first-time users.

Each section in this manual is preceded by a tabbed page so that information can be referenced quickly. Other reference aids include:

- **Manual Table of Contents** — Refer to the Table of Contents, List of Illustrations, and List of Tables at the beginning of this manual for a complete breakdown of the manual.
- **Section Tables of Contents** — Section tables of contents are located on the back of each tab page. Refer to this information for an overview of section contents.
- **Index** — Refer to the index at the back of the manual for reference to specific subjects.

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## OPERATOR'S SAFETY SUMMARY

Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

### TERMS

**In This Manual.** CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

**As Marked on Equipment.** CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

### SYMBOLS

#### In This Manual



This symbol indicates where applicable cautionary or other information is to be found.

#### As Marked on Equipment



DANGER — High voltage.



Protective ground (earth) terminal.



ATTENTION — refer to manual.

### POWER SOURCE

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

### GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation.

### DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

### **USE THE PROPER POWER CORD**

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition.

### **USE THE PROPER FUSE**

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified in the parts list in the *1240 Service Manual*.

Refer fuse replacement to qualified service personnel.

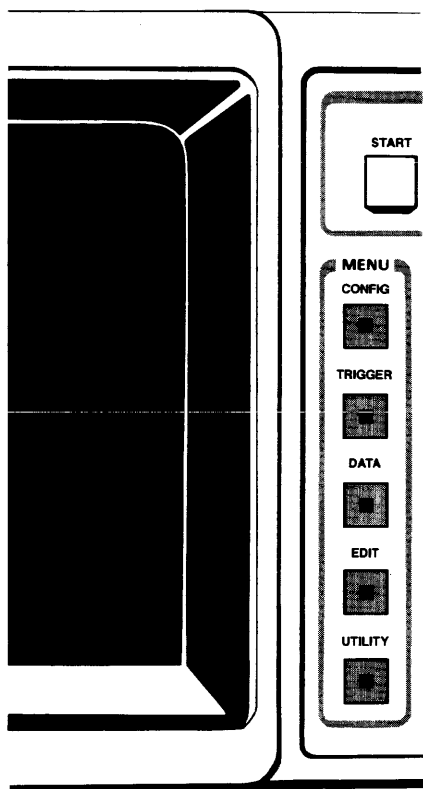
### **DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES**

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

### **DO NOT OPERATE WITHOUT COVERS**

To avoid personal injury, do not operate this product without covers or panels installed.

1



OVERVIEW  
&  
POWER-UP



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Specifications for the 1240, 1241, 1240D1, and 1240D2 are listed in Tables 8-5 through 8-9 in Section 8, *Reference Information*.

## GENERAL INFORMATION

Both the Tektronix 1240 and 1241 Logic Analyzers are portable, general-purpose, digital design and troubleshooting tools that offer similar feature sets. The 1240 displays information on a monochrome CRT display screen. The 1241 Logic Analyzer uses a Liquid Crystal Color Shutter (LCCS) to produce a three-color display screen. The 1241 also has a vertical expansion feature that doubles the height of the timing diagram traces.

Two types of data acquisition cards allow the instrument to be configured to meet your specific needs. The 1240D1 card supports high-speed hardware analysis with 9 acquisition channels at 100 MHz (10 ns) and 6 ns glitch detection. The 1240D2 has 18 acquisition channels at 50 MHz and includes a bus demultiplexing feature. Instrument configurations include any combination of 1240D1 and 1240D2 acquisition cards up to a maximum of four cards. A 1240 or 1241 configured with both card types is an effective tool for evaluating hardware-software integration. Total channel width varies from 9 channels (one 1240D1) to 72 channels (four 1240D2s).

The 1240 and 1241 Logic Analyzers provide the following features:

- Acquisition with one or two timebases. Asynchronous or synchronous selections are available.
- Powerful triggering with two event recognizers that can be used independently or together. The global event recognizer triggers on a single event in one or two timebases. In addition to the trigger action, the global event recognizer provides storage qualification, trigger reset, and detailed counter/timer functions. The sequential event recognizer consists of up to 14 separate levels. Each level specifies its own event and a trigger, wait, jump, delay, or reset action. Storage qualification is also available at each level.
- Data display in state table or timing diagram formats. The display preserves the time relationship between events, including events acquired on separate timebases.
- Simple, menu-oriented user interface featuring a front-panel keyboard (see Figure 1-1) and a display screen with touch-sensitive, on-screen soft keys. Soft keys help make the instrument easy to use because only appropriate operations are available at any given time.
- Auto-acquisition mode, for repeated acquisitions without manually restarting the instrument.
- Expandable acquisition memory depth with a memory chaining feature.
- Data search and compare functions.
- Nonvolatile memory ensures that two instrument setups (the current setup and another setup of your choice) are not lost when power is turned off.

Specifications for the 1240, 1241, 1240D1, and 1240D2 are listed in Section 8, *Reference Information*.

You control 1240/1241 operations through menus displayed on the screen. Use the MENU keys on the front panel to select general menu groups; select individual menus through on-screen soft keys. Each soft key is outlined on the screen and has a label describing its function. The keyboard layout, illustrated in Figure 1-1, is described in *Keyboard Description* later in this section. *Menu Overview*, also in this section, summarizes all menus. Figure 1-2 lists the menus accessed by each MENU key on the front panel.

Optional equipment includes nonvolatile RAM packs for storing instrument setups and memories, COMMunication packs for customizing the logic analyzer for external interfaces, and ROM packs for special added features. See *Options and Accessories* in Section 8 for a complete list.

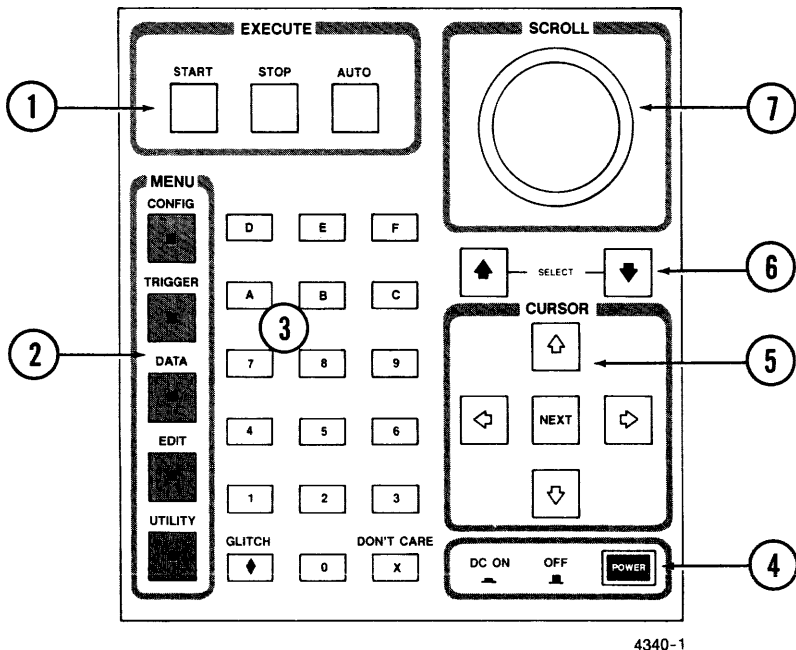


Figure 1-1. 1240 & 1241 keyboard layout.

## KEYBOARD DESCRIPTION

The keyboard is divided into seven functional areas. The following paragraphs describe these areas and their associated keys.

### 1 EXECUTE KEYS



**START** Starts data acquisition. When the trigger event specified in the Trigger Spec menu is found, the logic analyzer fills acquisition memory, then automatically stops and displays the acquired data in State Table or Timing Diagram format. While the logic analyzer is running, it displays information on the status of the trigger search.



**STOP** Stops data acquisition immediately (regardless of the status of the trigger search) and displays acquired data.



**AUTO** Starts a sequence of repeated data acquisitions based on the setups in the Trigger Spec and Auto-Run Spec menus. When the trigger event specified in the Trigger Spec menu is found, the conditions set up in Auto-Run Spec determine whether the logic analyzer stops, displays data, or continues to acquire.

2

**MENU KEYS**

These keys let you access groups of related menus. Each key has an LED in the center; the LED is lit when that menu group is in use.

For more menu information, refer to *Menu Overview* later in this section. The menus are discussed in detail in Sections 3 - 7.



Lets you access the Operation Level, Timebase, Memory Config(uration), and Channel Grouping menus. These menus work together to determine how the 1240 acquires and stores data.



Lets you access the Trigger Spec(ification) and Auto-Run Spec(ification) menus. These menus define the trigger conditions.



Lets you access the State Table and Timing Diagram data display formats.



Lets you access the Search Pattern Entry and Reference Memory Editor menus. These menus provide tools for manipulating stored data.



Lets you access the Storage Memory Manager menu. If a COMM pack is installed, a COMM Port Control menu is also available. Another menu may be available if a ROM pack is installed (not all ROM packs provide menus).

**NOTE**

*When you press a specific MENU key (e.g., CONFIG or TRIGGER), a menu within that group is displayed. A row of rectangles containing menu titles appears at the top of the screen; the label for the menu currently displayed is in reverse video (dark characters on a light background). The rectangles are menu "soft keys", and they are touch-sensitive. To change menus, touch the desired menu's soft key. Refer to Menu Soft Keys later in this section for more information.*

3

**DATA ENTRY KEYS**

Used for numeric data entry. If the field requires a specific radix, some keys may not be legal.



Used to indicate that the value of a channel or character is not considered.

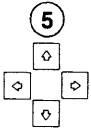


Indicates that a glitch, rather than data, is the value to be tested for.

4

**POWER SWITCH**

Controls dc power from the power supply. This switch and the MAIN POWER SWITCH on the back panel (see Figure 1-3) must both be on for the 1240 to power up.



**5 CURSOR CONTROL KEYS**

These four keys move the blinking field cursor within menu fields and from one menu field to another. The cursor must reside in a field before you can make changes to that field.



Advances the blinking field cursor to the next menu field to the right. If the cursor is positioned on the last field on a line, NEXT moves the cursor to the first field in the next line.

**6 SELECT KEYS**

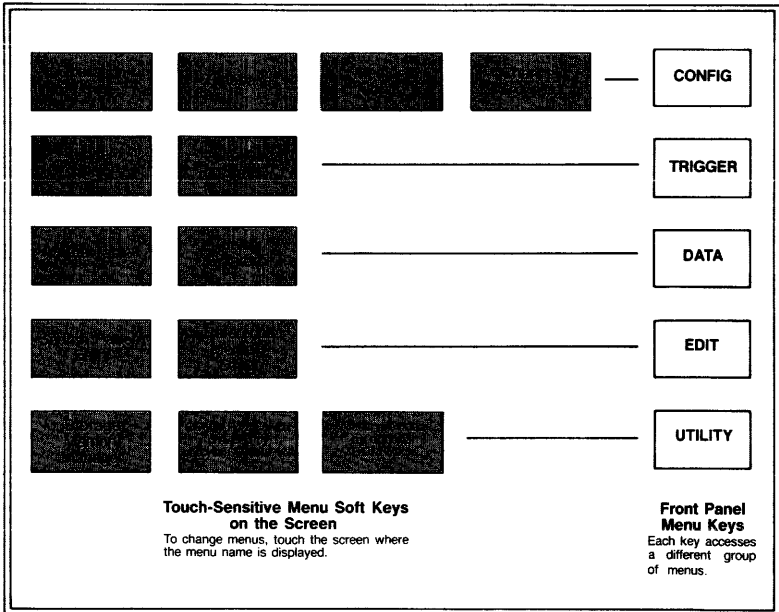


These keys are used in some menu fields to choose from predetermined field values.

**7 SCROLL KNOB**



The knob's main function is to scroll through acquired data. It also serves as an alternative to the SELECT keys to choose from predetermined values for certain menu fields. A label describing the current function of the knob is displayed in the upper-right corner of the screen. If the knob cannot be used in a particular situation, no label appears.



4340-2

Figure 1-2. Menu overview diagram, list of menus accessed by each MENU key.

## MENU OVERVIEW

You control 1240 and 1241 Logic Analyzer operations by entering selections into menus displayed on the screen. There are five groups of related menus; use the front panel MENU keys to access these menus (see previous *Keyboard Description*). Figure 1-2 shows which MENU keys access the appropriate menus. A short description of each menu follows; detailed descriptions are in Sections 3 – 7.

When you press a MENU key, the menu displayed is the last menu accessed in that group. If this is the first time the group has been accessed since power-up, the logic analyzer defaults to the menu shown at the far left of each group in Figure 1-2.

## MENU SOFT KEYS

At the top of the screen are touch-sensitive soft keys, one for each menu in the current menu group. The soft key in reverse video corresponds to the menu currently displayed. Change menus by touching the desired menu's soft key. The logic analyzer acknowledges the change with a short beep, displays the new menu, and changes the selected menu soft key to reverse video. Figure 1-2 lists the soft keys in each menu group.

### NOTE

*Fingerprints accumulate on the screen with normal use of the soft keys. While this does not affect the operation of the logic analyzer, you may want to clean the screen. For the 1240, use a soft, lint-free cloth dampened with a 5% detergent solution. For the 1241, spray glass cleaner on a lint-free cloth and wipe the color shutter. Any cleaner manufactured specifically for use on glass can be used.*

## MENU CHANGES

Many of the logic analyzer's menus are interrelated; a change in one menu may affect selections available in other menus. Tables 8-1 through 8-4 in Section 8, *Reference Information*, list the effects on other menus of changes to Operation Level, Memory Config, Timebase, and Channel Grouping.

## MENU DESCRIPTIONS

**CONFIG** Group. The menus in this group work together to determine how the 1240 and 1241 Logic Analyzers acquire and store data. Refer to Section 3 for complete details.

- Operation Level** — Displayed at power-up. Four operation levels customize the logic analyzer for different types of logic analysis tasks. The default level is Level 0 (Basic Operation), which supports most timing and state analyses. Levels 1 and 2 (Advanced Timing and State Analysis) have additional specialized features. All features are available in Level 3 (Full Operation).
- Timebase** — Specifies the number and type of timebases that can be used to control data acquisition.
- Memory Config** — Specifies the configuration of acquisition memory. Parameters involved are memory width vs. depth, acquisition card threshold, signal polarity, and pod-timebase assignments.

**Channel Grouping** — Collects channels into groups for data entry and display purposes. Specifies input and display radices for each group.

**TRIGGER** Group. These menus define the 1240 and 1241 Logic Analyzer's triggering characteristics. Refer to Section 4 for complete details.

**Trigger Spec** — Specifies the trigger event or sequence of events. Two event recognizers can be used individually or together to provide powerful, flexible triggering.

**Auto-Run Spec** — Specifies the conditions under which the logic analyzer makes repeated data acquisitions. The entries in this menu are only used if the data acquisition process is started with the AUTO key on the front panel. Auto-Run conditions do not specify trigger conditions; instead, they determine what action the logic analyzer takes when the trigger specified in the Trigger Spec menu occurs.

**DATA** Group. The first time after power-up that the 1240 and 1241 Logic Analyzers display acquired data, they use the State Table format. Subsequent acquisitions are displayed in either the State Table or the Timing Diagram format, depending on which format was used last.

The logic analyzers display data in the order it occurred at the probe tip. The display shows if event A occurred before event B, even if the events were not sampled by the same timebase. Refer to Section 5 for more information on this data correlation feature.

**State Table** — Displays acquisition memory or reference memory in a tabular format. Available operations include searching for and highlighting of data patterns. The channel arrangement, group label, and radix of displayed data are determined by the Channel Grouping menu.

**Timing Diagram** — Displays acquisition or reference memory in a logic-waveform format similar to the display of an oscilloscope. A maximum of 12 channels can be displayed at one time. The 1241's vertical expand feature doubles the trace height of displayed channels. Available operations include searching for and highlighting of data patterns.

**EDIT** Group. These menus provide tools for manipulating data in memory. See Section 6 for details.

**Search Pattern Entry** — Specifies a pattern of data to be searched for in acquisition or reference memory. The search pattern specified by this menu is used by operations in the Timing Diagram and State Table menus.

**Reference Memory Editor** — Modifies the reference memory. You can change data in existing memory locations, and you can move the trigger to a different location.

**UTILITY** Group. The Storage Memory Manager menu is always available in this menu group. If a COMM pack is installed, a COMM Port Control menu is also available. Another menu may be available if a ROM pack is installed. Refer to Section 7 for details.

- Storage Memory Manager** — Controls storage and retrieval of setups in nonvolatile memory and internal RAM; storage and retrieval of setups and memories in RAM packs; and retrieval of setups and memories from ROM packs.
- COMM Port Control** — Appears only when a COMM pack is installed. Configures the logic analyzer's external interface to the specific interface supported by the pack. The format of this menu varies among COMM packs; refer to the COMM pack's Instruction Manual for a description.
- ROM pack menu** — Appears only when certain ROM packs are installed (not all ROM packs provide menus). Menu title and function vary between packs; refer to the ROM pack manual for a description.

## TYPES OF VIDEO

The 1240 Logic Analyzer uses a monochrome (green phosphor) display screen. Most information is displayed in regular video; reverse video and highlighting are used for special cases.

- Regular video—light characters on a dark background.
- Reverse video—dark characters on a light background. The changeable portions of menu fields are displayed in reverse video. *The blinking field cursor can only be positioned on reverse video menu fields; the cursor must be positioned on a field before changes can be made to that field.* Reverse video is also used to display the currently selected soft key.
- Highlighted video—light characters on a shaded background. Highlighting emphasizes important information. For example, a label describing the current function of the SCROLL knob is displayed in highlighted video in the upper right corner of each menu. Another example: occurrences of the search pattern in a data display can be highlighted to let you quickly differentiate between data that matches the pattern and other data.

The 1241 uses three colors (red, green, and yellow) to display information. Most information is displayed in regular color video. Use of reverse color video and color highlighting are used for special cases.

- Regular color video—color characters on a dark background.
- Reverse color video—dark characters on a color-shaded background. The changeable portions of menu fields are displayed in reverse color video. *The blinking field cursor can only be positioned on reverse color video menu fields; the cursor must be positioned on a field before changes can be made to that field.* Reverse color video is also used to display the currently selected soft key.
- Highlighted color video—color characters on a color-shaded background. Highlighting emphasizes important information. For example, you can choose to highlight occurrences of the search pattern in a data display. Highlighting lets you quickly differentiate between data that matches the pattern and other data.



## POWER-UP PROCEDURE

The 1240 and 1241 Logic Analyzers are sent from the factory with all acquisition cards already installed. All you have to do is connect power and probes.

### INITIAL INSPECTION

This instrument was inspected both mechanically and electrically before shipment. It should be free of marks or scratches and should meet or exceed all electrical specifications. To confirm this, inspect the instrument for physical damage incurred in transit and test the performance by following the *Operator's Checkout Procedure* later in this section. Verify performance requirements by referring a qualified service person to the *Verification and Adjustment Procedures* section of the *1240/1241 Service Manual*. If there is damage or deficiency, contact your local Tektronix Field Office or representative.

### REPACKING FOR SHIPMENT

If the instrument is to be shipped to a Tektronix Field Service Center for repair, attach a tag to the instrument showing the owner's name and address, the instrument's serial number, and a description of the service required. Return probes with the instrument so that the entire system can be tested.

Use the original packaging. If it is unavailable or not fit for use, contact your local Tektronix Field Office to obtain new packaging.

### POWER REQUIREMENTS

**Line Voltage Selector.** Both 1240 and 1241 Logic Analyzers operate from a nominal 115 / 230 V, 48 - 63 Hz, single-phase power source. Before connecting the instrument to a power source, verify the line voltage selector on the back panel (see Figure 1-3 or 1-4) is set to the correct nominal voltage for the power source being used.



*If the line voltage selector shows the wrong voltage for the power source to be used, refer the instrument to qualified service personnel for fuse replacement.*

**Power Cords.** A three-wire power cord and three-contact plug provides connection to the power source and protective ground. The protective-ground contact connects to accessible metal parts of the instrument through the power cord protective grounding conductor. For protection against electrical shock, insert this plug into a power source socket that has a securely grounded protective-ground contact.



*Hazardous voltages may be present on the exposed metal surfaces of the instrument if the power source socket's protective-ground connection is not securely grounded.*

Both 1240 and 1241 Logic Analyzers are shipped with a 115 V power cord unless ordered otherwise. Other available power cords are listed in Section 8 under *Options and Accessories*.

**Power Switches.** There are two power switches that must both be ON for the instrument to operate. The MAIN POWER SWITCH on the back panel (see Figure 1-3 or 1-4) controls incoming ac power. The front-panel, push-button POWER switch controls dc power from the power supply. Use the front-panel switch to turn the instrument off in normal operations; it is not necessary to turn off the MAIN POWER SWITCH.

*The contents of nonvolatile memory are not affected by these switches.*

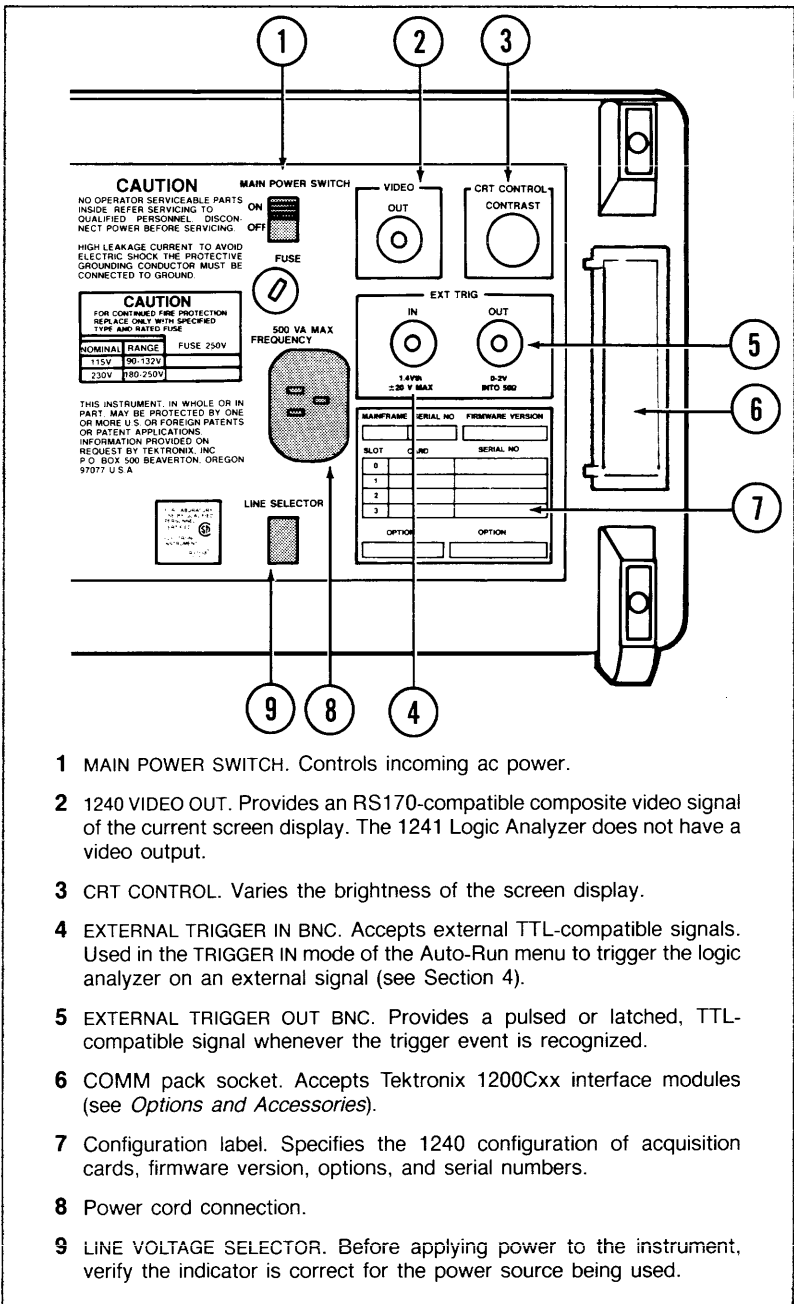


Figure 1-3. 1240 & 1241 back panel.

## POWER-UP DIAGNOSTICS

To power up the logic analyzer, set the back-panel MAIN POWER SWITCH to ON, then push the front-panel POWER button.

Both 1240 and 1241 Logic Analyzers have internal diagnostic tests that run automatically at power-up. These tests check out major mainframe components and operating firmware. When power-up diagnostics are successfully completed, most of the instrument's functions are verified.

Power-up diagnostics take six to ten seconds depending on the instrument configuration. If all tests pass, the Operation Level menu (CONFIG menu group) is displayed. This menu is shown in Figure 3-1.

If diagnostics fail, the Main Diagnostics menu is displayed. The menu lists the functional modules tested and a PASS/FAIL message for each module (FAIL message shown in highlighted video). Figure 1-5 shows an example display.

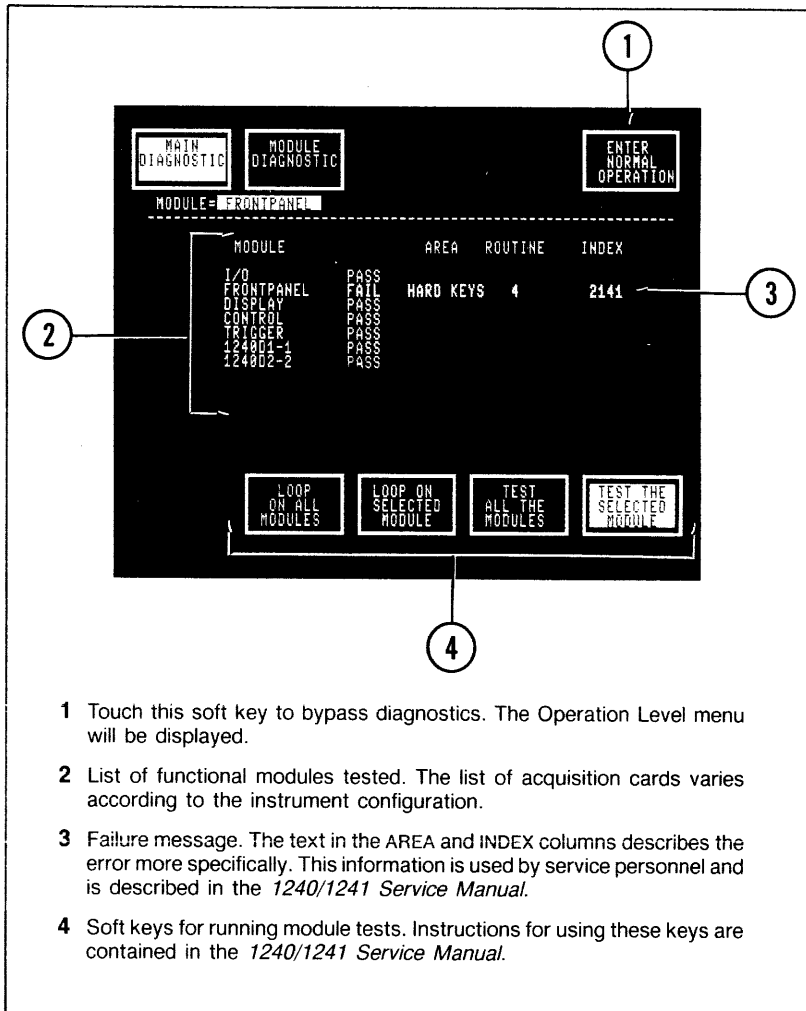
Some error conditions only inhibit a portion of the logic analyzer's functions. Table 1-1 describes the possible power-up error conditions.

**Table 1-1**  
**POWER-UP ERROR CONDITIONS**

Error Conditions	Definition
Display is blank or full raster.	A failure occurred on either the display board or the CRT driver board. No operation is possible. Refer the instrument to qualified service personnel.
Display is filled with random characters or zeros.	A failure occurred on either the I/O processor or the display board. No operation is possible. Refer the instrument to qualified service personnel.
DIAGNOSTICS FAILURE IOP RAM XXXX XXXX	One of the I/O processor RAMs failed. No operation is possible. Refer the instrument to qualified service personnel.
DIAGNOSTICS FAILURE IOP ROM n XXXX XXXX	A failure occurred in I/O processor diagnostic ROM n. Limited operation may be possible. Refer to the <i>1240/1241 Service Manual</i> for information.
IMPROPER ACQUISITION CARD SEQUENCE: RE-READ INSTALLATION INSTRUCTIONS OR CALL YOUR TEKTRONIX SERVICE REP.	Any 9-channel cards must be installed in lower-numbered slots than 18-channel cards. There can be no empty slots between acquisition cards. Refer to the <i>1240/1241 Service Manual</i> for acquisition card installation instructions.
INTER-PROCESSOR COMMUNICATION FAILURE	The control and I/O processors are unable to communicate. No operation is possible. Refer the instrument to qualified service personnel.
CONTROL PROCESSOR RAM FAILURE XXXX XX XX	A failure occurred in one of the control processor RAMs. No operation is possible. Refer the instrument to qualified service personnel.
CONTROL PROCESSOR ROM FAILURE XXXX XXXX	A failure occurred in one of the control processor ROMs. No operation is possible. Refer the instrument to qualified service personnel.

**Table 1-1 (cont.)**  
**POWER-UP ERROR CONDITIONS**

Error Conditions	Definition
I/O            FAIL	A failure occurred in the specified area of the I/O processor. Limited operation may be possible. Refer to the <i>1240/1241 Service Manual</i> for more information.
FRONTPANEL FAIL	A failure occurred in the specified area of the front panel. Limited operation may be possible unless a soft key has failed. Refer to the <i>1240/1241 Service Manual</i> for more information.
DISPLAY      FAIL	A failure occurred in the specified area of the display. Limited operation may be possible. Refer to the <i>1240/1241 Service Manual</i> for more information.
COMMPACK   FAIL	The specified area of the COMM pack failed. The pack will not operate properly, but the rest of the instrument is not affected. Power down and remove the pack.
COMMPACK ROM FAIL XXXX XXXX	The specified area of the COMM pack failed. The pack will not operate properly, but the rest of the instrument is not affected. Power down and remove the pack.
CONTROL     FAIL	A failure occurred in the specified area of the control processor. Limited operation may be possible. Refer to the <i>1240/1241 Service Manual</i> for more information.
TRIGGER     FAIL	A failure occurred in the specified area of the trigger board. Limited operation may be possible. Refer to the <i>1240/1241 Service Manual</i> for more information.
9 CH ACQn   FAIL	A failure occurred in the specified area of the 9-channel card in acquisition card position n. This card will not operate properly, and may affect other cards if it is left in the system. Refer the instrument to qualified service personnel for card removal.
18 CH ACQn  FAIL	A failure occurred in the specified area of the 18-channel card in acquisition card position n. This card will not operate properly, and may affect other cards if it is left in the system. Refer the instrument to qualified service personnel for card removal.
RAMPACK     FAIL	This message can be displayed for two reasons. 1. A failure occurred in the specified area of the pack. 2. The pack is not initialized. First, try to initialize the pack: touch the ENTER NORMAL OPERATION soft key, then press the UTILITY key on the front panel. The displayed error message indicates unknown RAM pack or bad checksum. Press X to initialize the RAM pack. Next, turn the instrument off, then on again. If the error persists, the pack has failed; it will not operate properly, but the rest of the instrument is not affected. Power down and remove the pack.
ROMPACK     FAIL	A failure occurred in the specified area of the ROM pack. The pack will not operate properly, but the rest of the instrument is not affected. Power down and remove the pack.
ROMPACK ROM FAIL XXXX XXXX	The specified area of the ROM pack failed. The pack will not operate properly, but the rest of the instrument is not affected. Power down and remove the pack.



- 1 Touch this soft key to bypass diagnostics. The Operation Level menu will be displayed.
- 2 List of functional modules tested. The list of acquisition cards varies according to the instrument configuration.
- 3 Failure message. The text in the AREA and INDEX columns describes the error more specifically. This information is used by service personnel and is described in the *1240/1241 Service Manual*.
- 4 Soft keys for running module tests. Instructions for using these keys are contained in the *1240/1241 Service Manual*.

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**Figure 1-4. Example display generated when a failure is detected by the power-up diagnostics.** Refer to Table 1-1 to see how the failure affects operation. Touch the ENTER NORMAL OPERATION soft key to bypass diagnostics. You can force this display by holding down any front-panel key during power-up.

## PROBE CONNECTIONS

The 1240 and 1241 Logic Analyzers are compatible with the P6460 Data Acquisition Probe and the P6462 Fixed Threshold TTL Acquisition Probe. Nine-channel acquisition cards use one probe; 18-channel cards use two.

Each probe has nine data lines (numbered 0-8) and one clock/qualifier (C/Q) line. Electrical, environmental, and physical specifications are listed in the instructions accompanying the probe.

Probes connect to acquisition cards through openings in the right side-panel of the instrument. Figure 1-6 shows how to connect a probe to an acquisition card. Be sure the raised tab on the probe connector is aligned with the guides in the side panel and in the edge connector.

**Pod ID.** Any time the logic analyzer refers to a probe in a menu or screen message, it uses a number called the Pod ID. ("Pod" is used throughout this manual to mean "probe"; they are equivalent terms.) A probe's Pod ID is determined by the type of acquisition card the probe is connected to and what position, or slot, the card occupies in the instrument.

The four available acquisition card slots are numbered 0-3. Pod ID numbers (two per slot, see Figure 1-6) are molded into the side panel above the slots. An 18-channel card accepts probes at both Pod ID slot locations. A 9-channel card accepts a probe only at an even-numbered Pod ID location. For example: The sample menu displays for this manual are based on a 1240 (in some cases, a 1241) equipped with two 9-channel and two 18-channel cards. Since 9-channel cards must be installed in lower-numbered slots than 18-channel cards, the 9-channel cards have probes attached at Pod IDs 0 and 2, and the 18-channel cards have probes attached at IDs 4,5 and 6,7. Pod IDs 1 and 3 are not used. Pod ID 1 is only used when no 9-channel cards are installed.

A Pod ID button is located on the back edge of the probe (see Figure 1-7). Press this button to get a screen readout of the probe's Pod ID.

**▲ Lead Sets.** A ten-inch lead set is supplied with each P6460. This lead set can be used to clock frequencies up to 25 MHz. Above 25 MHz, one of the optional five-inch lead sets may be required to meet all specifications. Refer to the documentation accompanying the P6460 for the part numbers of these lead sets.

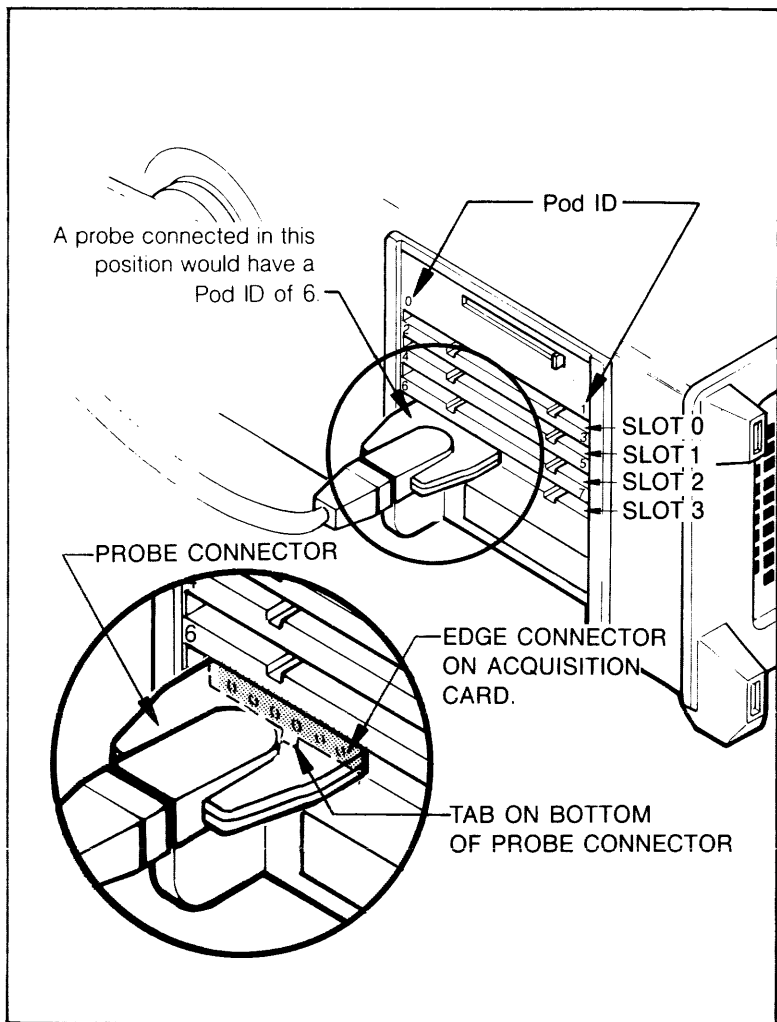
Two ground leads are also provided with each P6460. Below 25 MHz, only one ground lead is required with the ten-inch lead set. Between 25 MHz and 50 MHz, use both ground leads. For frequencies above 50 MHz or in environments with lots of electrical noise, use a five-inch lead set and both ground leads with alligator clips.

A ten-inch lead set and one ground lead are supplied with each P6462. For clock operating frequencies up to 25 MHz, use the 10-inch lead set. For clock frequencies over 25 MHz, use the optional 5-inch lead set. One ground lead is sufficient.

Figure 1-7 shows how to install lead sets and ground leads.

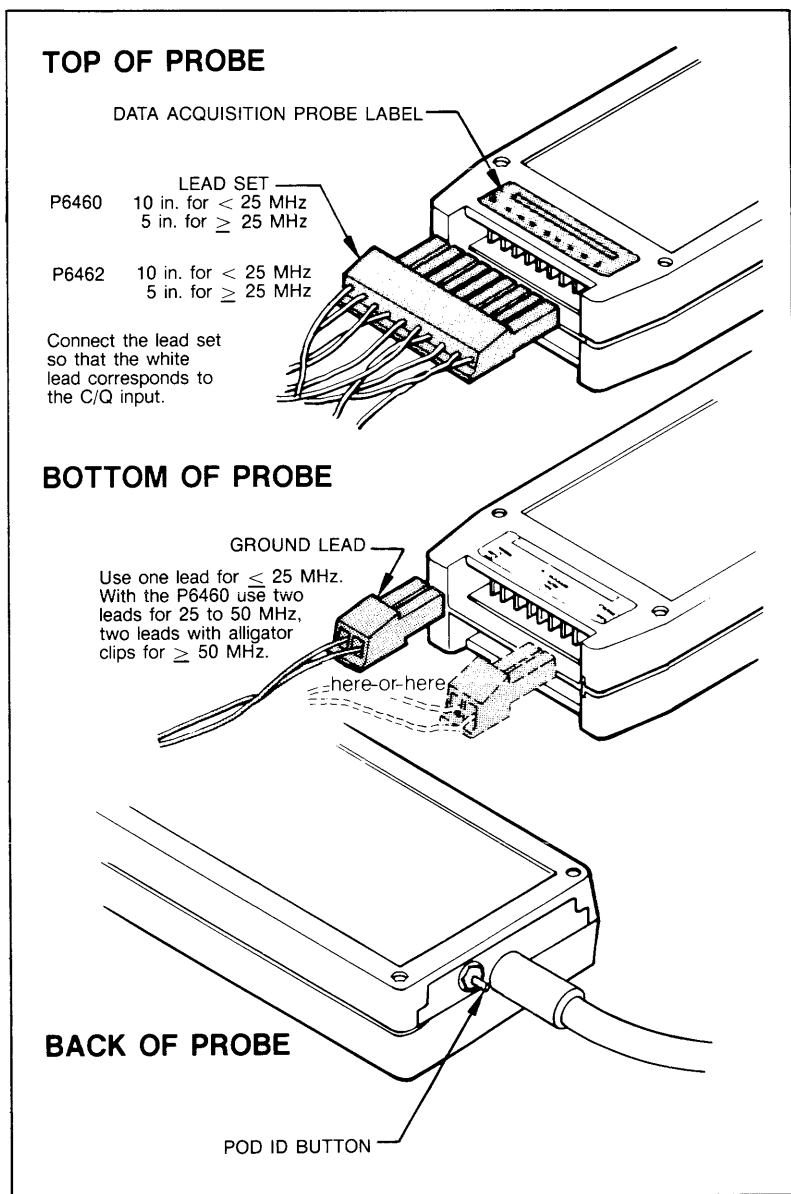


*Refer to the specifications in the probe instructions for the maximum non-destructive input voltage range. If the probe is connected to a voltage greater than this range, its circuitry may be damaged.*



4340-5

**Figure 1-5. Connecting probes to the logic analyzer.** Align the raised tab on the probe connector with the guides in the side panel and in the edge connector on the acquisition card.



4340-6

Figure 1-6. Connecting lead sets and ground leads to data acquisition probes.



## ROM/RAM AND COMM PACK CONNECTIONS

ROM and RAM packs are installed in the slot directly beneath the probe connections on the right side-panel of the instrument (see Figure 1-8). ROM and RAM packs can be installed or removed while power is on or off. If power is on, the Storage Memory Manager menu (UTILITY menu group) must be displayed on the screen, and you must press the LOAD NEW PACK soft key immediately after installing or removing the pack.

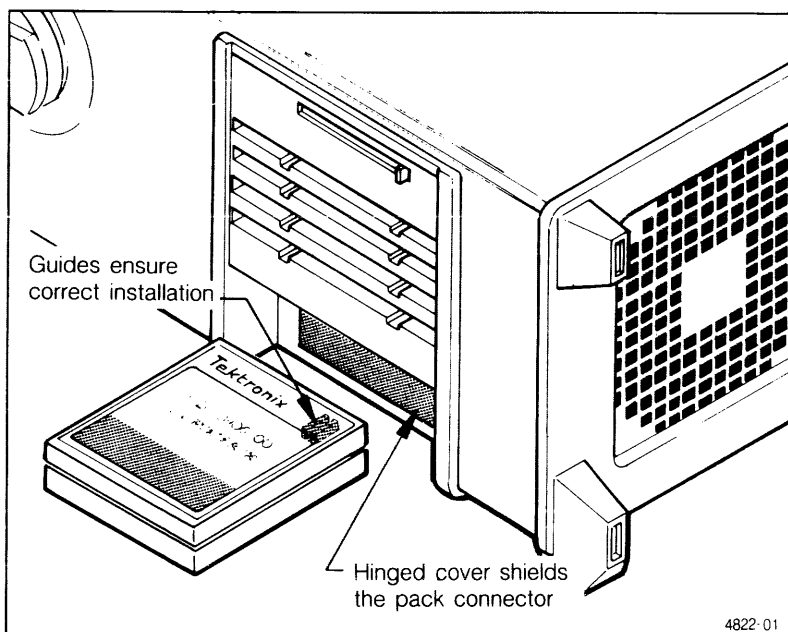


*Static discharge can damage the semiconductor devices in a ROM or RAM pack.*

*Discharge static from a pack before installing it by momentarily laying the pack (label side up) on top of the instrument.*

To install a pack, slide the pack (label side up) past the hinged slot cover and push it slowly and firmly into the connector. Two guides on the top cover of the pack ensure that the pack will be installed correctly. To remove a ROM or RAM pack, simply pull it straight out.

Refer to the description of the Storage Memory Manager menu in Section 7 for information on how to access ROM or RAM pack information.



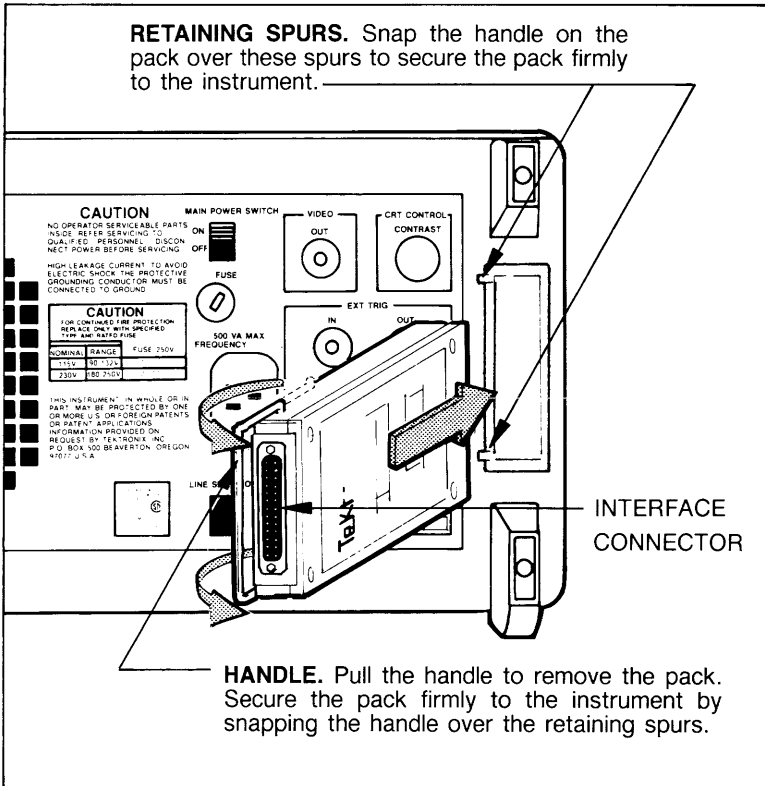
**Figure 1-7. Installing a ROM or RAM pack.** ROM or RAM packs can be installed or removed while power is on or off. If power is on, the Storage Memory Manager menu (UTILITY menu group) must be displayed on the screen, and you must press the LOAD NEW PACK soft key immediately after installing or removing the pack.

COMM packs are installed in the slot on the back panel; see Figure 1-9. With **power off**, slide the pack past the hinged cover, label to the right as you face the back panel. The pack connector is located about four inches past the hinged cover. You can anchor the pack firmly to the instrument by snapping the handle over the two small retaining spurs to the left of the slot (see Figure 1-9).

To remove a COMM pack from the instrument, first turn dc power off, then pull on the handle on the back of the pack.



*Do not install or remove a COMM pack while dc power is on; the COMM pack may be damaged.*



4340-54

**Figure 1-8. Installing a COMM pack.** Do not install or remove a COMM pack while dc power is on.

## OPERATOR'S CHECKOUT PROCEDURE

This procedure consists of diagnostic tests the operator can perform as an incoming inspection. The tests provide a basic check of the instrument's operational status. Complete operational tests are described in the *Verification and Adjustment Procedures* in the *1240/1241 Service Manual*; these procedures should be performed only by a qualified service technician.

1. With power off, plug in any COMM pack and any ROM or RAM pack you want to test.
2. Connect P6460 Data Acquisition Probes to the acquisition card you want to test. Connect one probe to a 9-channel card or two probes to an 18-channel card. Figure 1-6 shows how to connect probes to acquisition cards.
3. Connect a diagnostic lead set to each probe. Two diagnostic lead sets are standard accessories with each logic analyzer.
4. If you are testing a 9-channel card, connect the diagnostic lead set to the *left* TPG output connector.

If you are testing an 18-channel card, connect the diagnostic lead set of the left probe to the left TPG output and the other lead set to the right TPG output.

Figure 2-1 in the next section shows how to connect a diagnostic lead set to a TPG output connector. *Be sure to connect the white wire to the lower-left pin.*

5. Hold down any front-panel key and power up the logic analyzer. The Main Diagnostic menu is displayed (see Figure 1-5). The menu will indicate a keyboard failure because of the power-up method.

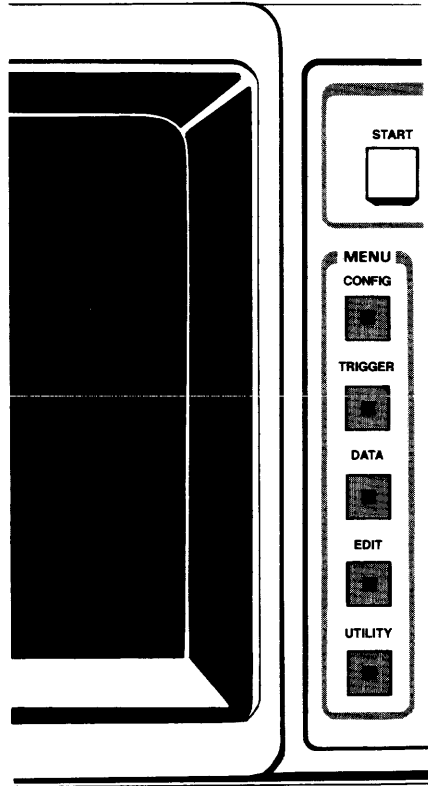
### NOTE

*If the logic analyzer displays RAMPACK FAIL when you power-up with a RAM pack installed, the pack may not be initialized. Follow the initialization instructions described under this message in Table 1-1.*

6. Touch the TEST ALL MODULES soft key, then press the START key on the front panel to begin the tests. When the tests are completed, a PASS or FAIL status message is displayed for each module. FAIL messages are displayed in highlighted video.
7. Connect the TPG to an untested acquisition card, then select that card in the MODULE field. Touch the TEST THE SELECTED MODULE soft key, then press START. When the test is complete, a PASS or FAIL message is displayed for the tested card. Repeat this procedure until all cards are tested.

If a failure occurs, re-run the test to ensure that the failure is valid. A module that previously failed but now passes will indicate the failure history with a highlighted PASS message. Refer failed acquisition cards and the attached probe(s) to a qualified service technician for repair.

2



DEMONSTRATION

DEMONSTRATION

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## DEMONSTRATION

This section provides you with a button-pushing tour of the features available in the 1240 and 1241 Logic Analyzers. Follow these "cookbook" procedures if you want to push some buttons without getting lost. If you prefer learning theory before experimenting, skip ahead to Sections 3-7.

### SIMPLE EXAMPLE: A QUICK ACQUISITION

The following short procedure causes the logic analyzer to collect data asynchronously at 20 ns intervals on one timebase when a trigger condition of FF is detected.

**Required Equipment.** This example requires your logic analyzer to be equipped with at least one 9-channel card. No external system is required; input signals are obtained from the internal Test Pattern Generator (TPG). The TPG produces a 63-state repetitive pattern on nine data lines and one clock output.

You will need a 1240 or 1241 Logic Analyzer with at least:

- (1) 1240D1 9-Channel Acquisition Card
- (1) P6460 Data Acquisition Probe, with diagnostic lead set <sup>1</sup>

#### Probe Connection.

1. Connect the data acquisition probe to the 9-channel card in slot 0.
2. Connect the diagnostic lead set to the probe. (Refer to Figure 2-1.)
3. Connect the other end of the diagnostic lead set to the left (front) TPG connector. The white wire goes down and toward the front of the instrument.

#### Power—up.

4. Plug in the logic analyzer and turn on the MAIN POWER SWITCH on the back panel. (Refer to Figure 1-3.)
5. Press the DC POWER pushbutton on the front panel.
6. Refer to Figure 2-2 and verify that the instrument powers up to the Operation Level menu. After power-up, this menu is accessed using the CONFIG menu key just to right of the screen on the front panel. (If the Main Diagnostic menu appears, the logic analyzer has failed its power-up diagnostics. Refer to the *1240/1241 Service Manual* or contact your nearest Tektronix Service Center for assistance.)

#### Setting Input Thresholds.

7. Touch the MEMORY CONFIG soft key at the top of the screen.
8. Turn the SCROLL knob *counter-clockwise* one click until TPG appears in the CARD THRESHOLD field.

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<sup>1</sup> The Test Pattern Generator can only be used with the P6460 Data Acquisition Probe.

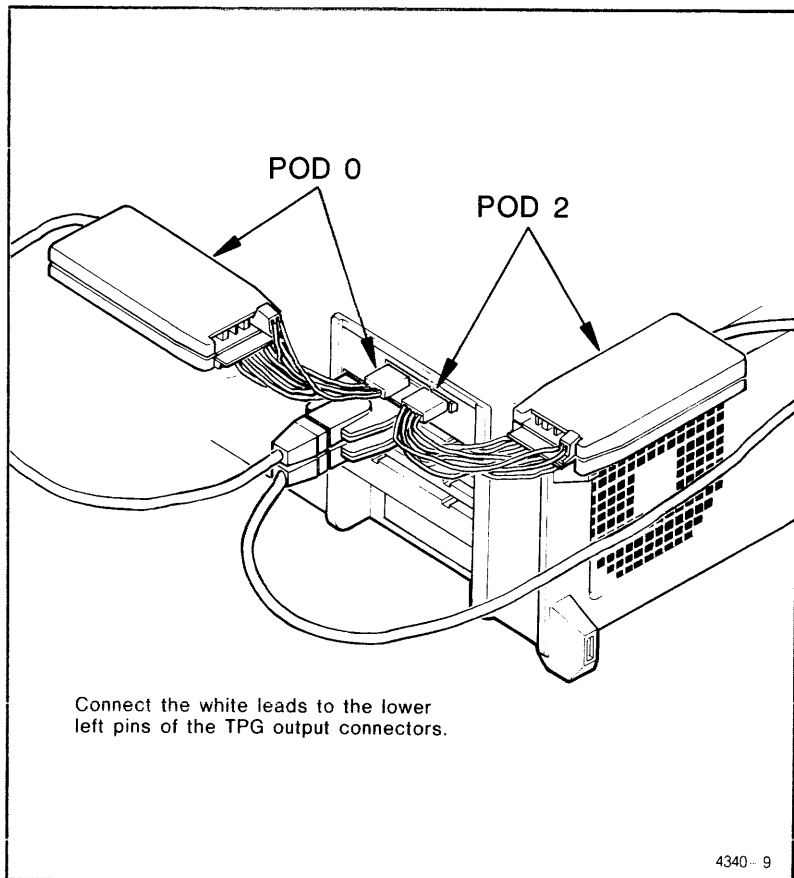
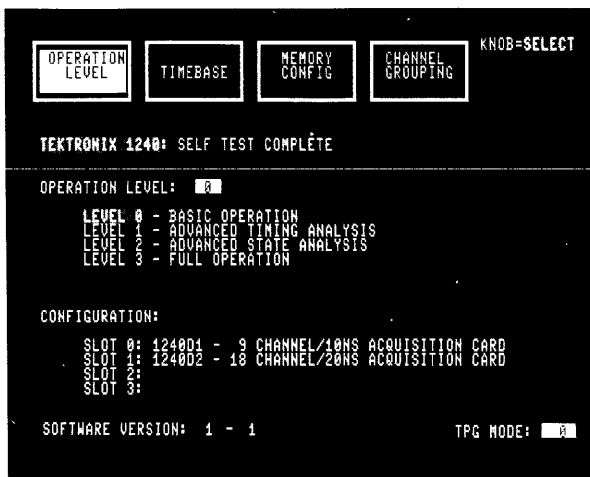


Figure 2-1. TPG outputs and how diagnostic lead sets connect to them.

**Defining the Trigger Condition.** This example relies on default values in the other CONFIG menus, Timebase and Channel Grouping, so you do not have to change anything in those menus. But if you would like to look at those default settings, push the TIMEBASE and CHANNEL GROUPING soft keys and take a look before proceeding to the next step.

9. Press the TRIGGER key. This takes you to the Trigger Spec menu so you can define an event.
10. Press F twice. This enters FF as the event which will cause a trigger. The logic analyzer contains two independent event recognizers, the GLOBAL and the SEQUENTIAL. You are leaving the GLOBAL EVENT recognizer OFF, and using only one level of the 14-level SEQUENTIAL EVENT recognizer for this simple acquisition.



4340-10

Figure 2-2. Power-up display with one 9-channel and one 18-channel acquisition card installed.



4340-11

Figure 2-3. Data acquired at 20 ns ASYNC after triggering on FF in the TPG pattern.



**Acquiring Data.**

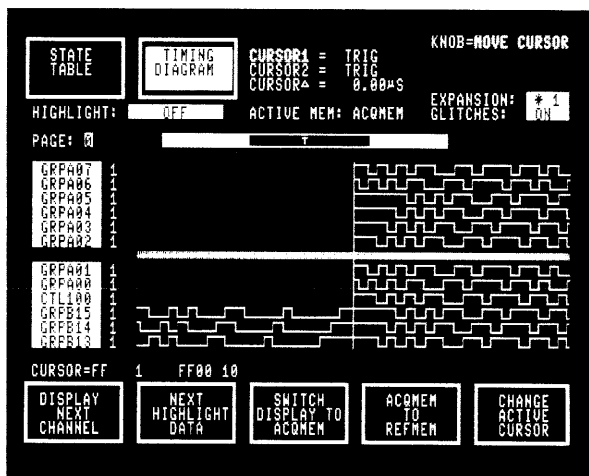
11. Press the START key and observe a data acquisition. The data display when the acquisition is complete will look like Figure 2-3.

*NOTE*

*The examples in this section were generated using a 1240 Logic Analyzer equipped with one 9-channel card and one 18-channel card. If your instrument has a different number of acquisition cards, you will have a different number of data display columns and fields than are shown in these examples. Some screen displays are slightly different for the 1241 Logic Analyzer.*

**Timing Diagram Display.**

12. Press the TIMING DIAGRAM soft key. The display changes to a timing diagram that looks like Figure 2-4.



4340 - 12

**Figure 2-4. Timing diagram display of data acquired at 20 ns ASYNC after triggering on FF in the TPG pattern.**

## A MORE COMPLICATED EXAMPLE: TWO TIMEBASES AND DEMULTIPLEXING

The previous example showed a simple method for acquiring meaningful timing data, but it relied heavily on power-up default parameters. The following example is longer and will allow you to set more of the instrument parameters yourself. It also demonstrates several of the logic analyzer's more advanced features, such as dual timebase operation and demultiplexing. In this example, you acquire data asynchronously at 50 ns intervals on one timebase, while you use the other timebase synchronously to demultiplex different data.

**Required Equipment.** This example requires your logic analyzer to be equipped with at least one 9-channel and one 18-channel acquisition card. No external system is required; input signals are obtained from the internal Test Pattern Generator (TPG). The TPG produces two 63-state repetitive patterns, each of which is available on nine data lines and one clock output.

You will need a 1240 or 1241 Logic Analyzer with at least:

- (1) 1240D1 9-Channel Acquisition Card
- (1) 1240D2 18-Channel Acquisition Card
- (2) P6460 Data Acquisition Probes, with diagnostic lead sets

### Probe Connection.

1. Connect one probe to the 9-channel card in slot 0.
2. Connect another probe to the even-numbered (front) connector of the first 18-channel card.
3. Connect diagnostic lead sets to both probes.
4. Connect the lead set from the 9-channel card to the left (front) TPG connector. Refer to Figure 2-1. Make sure the white wire goes down and to the front of the instrument.
5. Connect the lead set from the 18-channel card to the right (rear) TPG connector. Refer to Figure 2-1.

### Power-up.

6. Plug in the logic analyzer and turn on the MAIN POWER SWITCH on the back panel. (Refer to Figure 1-3.)
7. Press the DC POWER pushbutton on the front panel.
8. Refer to Figure 2-2 and verify that the instrument powers up to the Operation Level menu. After power-up, this menu is accessed using the CONFIG key just to right of the screen on the front panel. (If the Main Diagnostic menu appears, the logic analyzer has failed its power-up diagnostics. Refer to the *1240/1241 Service Manual* or contact your nearest Tektronix Service Center for assistance.)

### Operation Level and TPG Mode.

9. Turn the SCROLL knob until a **3** appears in the OPERATION LEVEL select field. Note that the list below indicates a change from **LEVEL 0** to **LEVEL 3**. We now have the full feature set of the instrument available.
10. Using the CURSOR keys, move the blinking field cursor to the TPG MODE select field.

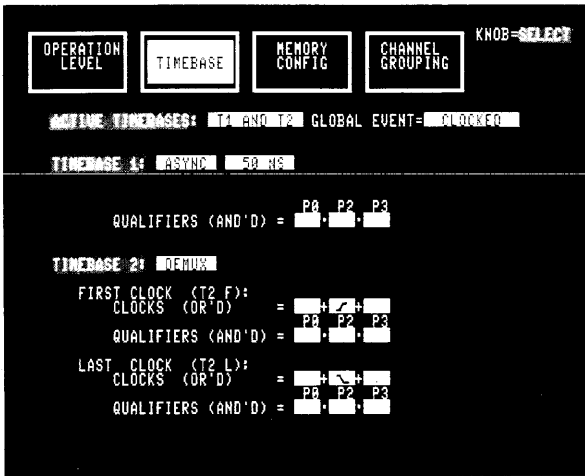
11. Turn the SCROLL knob until a **1** appears. This selects a Test Pattern Generator output which is clocked internally at 6 MHz and contains glitches in the output.

### Setting Up the Timebases.

12. Press the TIMEBASE soft key at the top of the display. Use the SCROLL knob to select **T1 AND T2** as the active timebases.
13. Move the cursor down once and change the period of the asynchronous TIMEBASE 1 from **20 NS** to **50 NS**. This selection gives you several locations of asynchronous data for each synchronous one.
14. Move the cursor down to the first TIMEBASE 2 select field. This field contains the word **SYNC**, its power-up default value. Select **DEMUX** using the knob or SELECT keys. With this timebase you will acquire data from a single set of lines. But, by using different clock edges, you will demultiplex this data into two different areas of acquisition memory and display it with different labels. (The TPG output data is not really multiplexed, but pretend that it is for the purpose of this exercise.)
15. Move the cursor down once to the first select field for CLOCKS (OR'D) in the FIRST CLOCK (T2 F) row. Turn the SCROLL knob until the select field for the clock edge polarity of pod P0 is blank. The default for all timebases is the rising edge of pod 0. Since your first 9-channel card (pod 0) is being used asynchronously, the pod 0 clock will not be used. For the 18-channel card that you will use for demultiplexing, select edges of the clock associated with the even numbered pod of that card.
16. Move the cursor to the right until it is in the select field of the pod that corresponds to the location of the first 18-channel card. Turn the SCROLL knob to select the rising edge of that clock. With this choice we are selecting the rising edge of the TPG clock as the storage strobe for collecting the data we will later label ADDR.
17. Move the cursor down until it is in the corresponding CLOCKS (OR'D) field of the LAST CLOCK (T2 L) row.
18. Turn the SCROLL knob to select the falling edge of this clock. You are selecting the falling edge of the TPG clock, obtained through the even-numbered pod of the 18-channel card, as the timebase for collecting the data you will later label DATA.
19. Move the cursor to the left until it is in the select field for P0 (T2 L).
20. Turn the SCROLL knob until a blank appears (neither edge is selected).
21. Compare the screen with Figure 2-5 to verify what you have done so far.

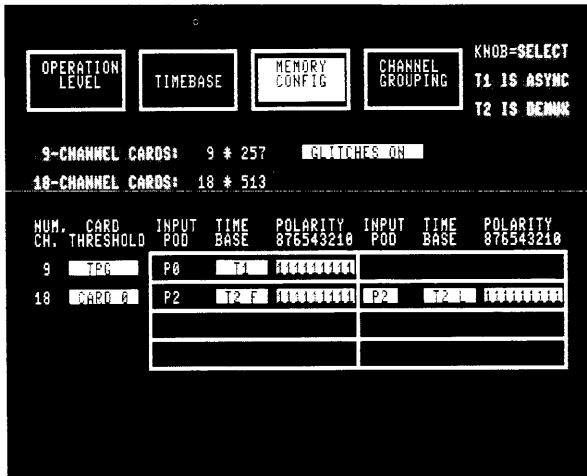
### Setting Input Thresholds.

22. Press the MEMORY CONFIG soft key at the top of the display. The blinking cursor is in the CARD THRESHOLD select field for the first 9-channel card.
23. Turn the SCROLL knob *counter-clockwise* one click until **TPG** appears. This sets the input threshold value to +3.70 Volts, to correspond to the Test Pattern Generator output levels. It is not necessary to change the value of any of the other cards because the default value of **CARD 0** means "the same as card 0."



4340-13

Figure 2-5. Setup of the Timebase menu for the second example.



4340-14

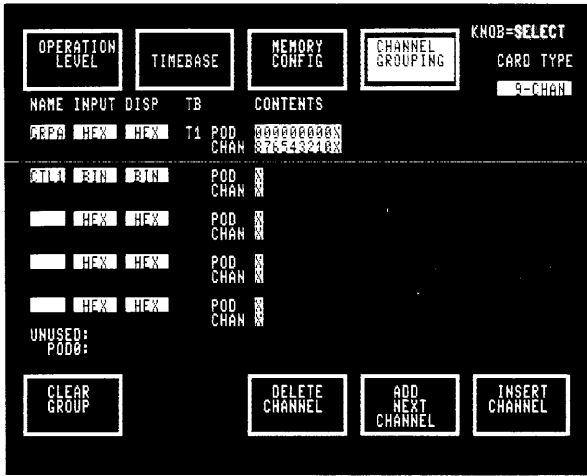
Figure 2-6. Setup of the Memory Config menu for the second example.

### Memory Configuration.

24. Move the cursor down to reach the leftmost TIMEBASE column of the first 18-channel card.
25. Turn the SCROLL knob to select **T2 F**, timebase two — *first*. This is the timebase that you defined in the Timebase menu as the rising edge of the TPG clock.
26. Move the cursor right to the INPUT POD select field (reverse video) on the right side of the screen.
27. Turn the SCROLL knob to select the *even* choice of pod. This is the same INPUT POD number shown in a non-select field on the left side of the same card. There are only two choices in this field: the odd, default value supports maximum channel width; the other value, the even choice you just selected, supports demultiplexing of 9 channels into 18.
28. Move the cursor to the right, to the second TIMEBASE column of the first 18-channel card.
29. Turn the SCROLL knob to select **T2 L**, timebase two - *last*. This is the timebase that you defined in the Timebase menu as the falling edge of the TPG clock.
30. Compare the screen with Figure 2-6 to verify what you have done so far.

**Channel Grouping.** Each TPG output connector contains a clock line and nine lines of data. The power-up default channel grouping for 9-channel cards is eight lines of data in one group with the control lines collected in a separate group. Because the TPG output is nine lines wide (plus a clock), you must move one line from the control group to the first data group. Likewise, the default arrangement of the 18-channel cards is 16 channels of data and 2 control lines. Because you will be doing demultiplexing, you will want to rearrange these lines into two 9-wide groups.

31. Press the CHANNEL GROUPING soft key at the top of the display.
32. Press the NEXT key three times to move the cursor to the CONTENTS column of the display.
33. Press the INSERT CHANNEL soft key at the bottom of the screen. Notice that  $\frac{x}{x}$  appears to the left of the CONTENTS field.
34. Press the **0** data entry key. Note that the top X changes to a 0, and that the cursor is now over the bottom X.
35. Press the **8** data entry key. You have now defined **GRPA** as including all nine data channels of pod 0.
36. Observe the CONTENTS column of the group labeled **CTL1**. Note that  $\frac{x}{x}$  has replaced the  $\frac{0}{8}$  that used to be on the left. When you inserted channel 8 of pod 0 into **GRPA**, the logic analyzer automatically removed it from its previous group.
37. If your logic analyzer has more than one 9-channel card, move the cursor down to the groups associated with these other cards and press the CLEAR GROUP soft key. Each time, press the X key on the front panel to confirm that you really want to do this.
38. Move the cursor down to the **CTL1** group. Press the CLEAR GROUP soft key. Press X to confirm that action. Compare the screen to Figure 2-7 to check what you have done.

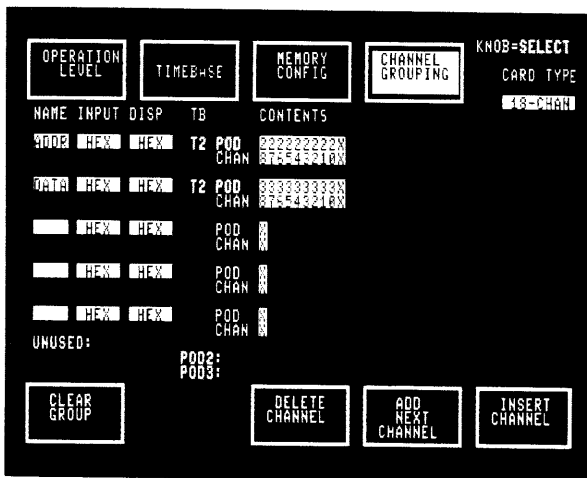


4340-15

Figure 2-7. Setup of the 9-channel portion of the Channel Grouping menu for the second example.

39. Move the cursor up to the CARD TYPE select field (which currently contains **9-CHAN**). Turn the SCROLL knob until it reads **18-CHAN**. The screen now contains grouping assignments for the lines from 18-channel cards.
40. Press the NEXT key once. The cursor will move to the first select field in the NAME column. (This will be **GRPB** if there is only one 9-channel card installed, **GRPC** if there are two 9-channel cards installed, and **GRPD** if there are three 9-channel cards installed.)
41. Press the CLEAR GROUP soft key and X to confirm that action.
42. Turn the SCROLL knob *counter-clockwise* until an **A** appears in the first character location. Move the cursor to the right once. Turn the SCROLL knob until the character **D** appears. Move the cursor to the right once again. Turn the SCROLL knob until the character **D** appears here too. Move the cursor to the right again and turn the SCROLL knob to obtain an **R**. You have defined a group name as **ADDR**.
43. Press the NEXT cursor key three times to move out to the CONTENTS column.
44. Press the numeric key which corresponds to the even-numbered pod of the first 18-channel card in your instrument. (For instruments with only one 9-channel card, this is **2**. For instruments with two 9-channel cards, this is **4**. For instruments with three 9-channel cards, this is **6**.) Then press the **8** key.
45. Press the ADD NEXT CHANNEL soft key *eight* times. You have now defined a group of nine channels as **ADDR**. These should be the nine channels associated with the even-numbered pod of the first 18-channel card.
46. Press the NEXT key twice to move to the second field in the NAME column. Using the SCROLL knob and the cursor, change this name to read **DATA**. (As in step 42.)
47. Press the CLEAR GROUP soft key and X to confirm that action.

48. Move the cursor to the right, to the INPUT radix column of the **DATA** group. Turn the knob until this field contains **HEX** (if it does not already). Move the cursor to the right, to the DISP (display radix) column of the **DATA** group. Turn the knob until this field contains **HEX** (if it does not already).
49. Move the cursor to the right, to the CONTENTS column of the **DATA** group.
50. Press the numeric key which corresponds to the odd-numbered pod of the first 18-channel card in your instrument. (For instruments with only one 9-channel card, this is **3**. For instruments with two 9-channel cards, this is **5**. For instruments with three 9-channel cards, this is **7**.) Then press the **8** key.
51. Press the ADD NEXT CHANNEL soft key *eight* times. You have now defined a group of nine channels as **DATA**. This group will receive demultiplexed data from the odd-numbered pod of the first 18-channel card.
52. Use the CLEAR GROUP soft key to clear all of the groups below **DATA**. Each time, press the X key on the front panel to confirm that you really want to do this.
53. Compare the screen with Figure 2-8 to verify what you have done so far.

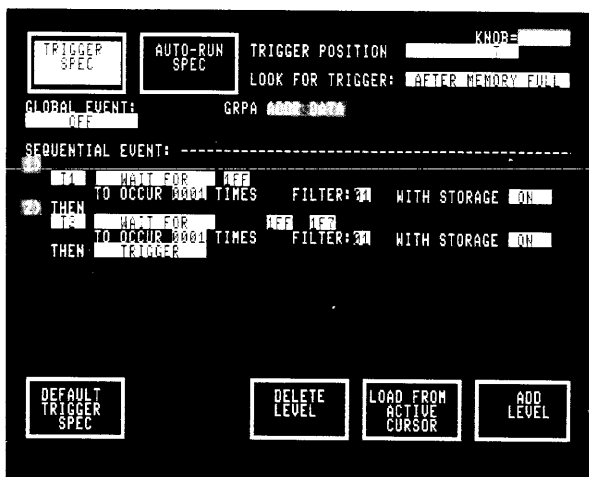


4340-16

Figure 2-8. Setup of the 18-channel portion of the Channel Grouping menu for the second example.

### Specifying the Trigger Condition.

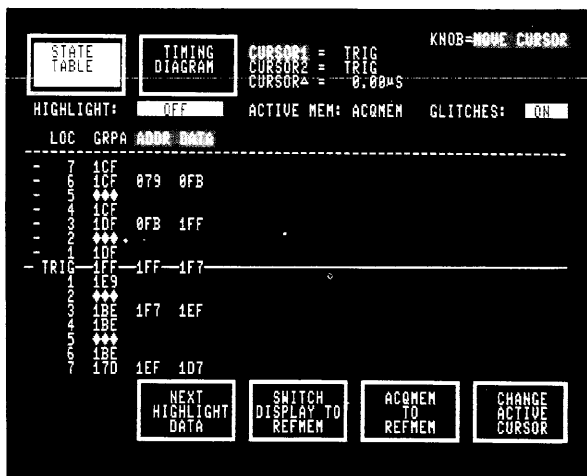
54. Press the TRIGGER key. Then press the CURSOR *up* key three times to move the blinking cursor to the TRIGGER POSITION select field. Use the knob to move the **T** to the right end of the bar graph. This positions the trigger near the end of memory.
55. Move the cursor down *three* times and to the right *once*, to the **XXX**'s in the sequential event recognizer. Enter **1FF** in this field.



4340-17

Figure 2-9. Setup of the Trigger Spec menu for the second example.

56. Press the ADD LEVEL soft key. Move the cursor to the left and change T1 to T2. This level will look for an occurrence of data on timebase 2 after a 1FF occurs on timebase 1.
57. Move the cursor to the right twice and enter 1FF 1F7. This is the value that will now cause the instrument to trigger.
58. Compare the screen with Figure 2-9 to verify what you have done.



4340-18

Figure 2-10. Data display of TPG output triggered on a sequential event recognizer value of 1FF on timebase 1, followed by a 1FF, 1F7 on timebase 2.



### Acquiring Data.

59. Press the START key in the EXECUTE area of the front panel. Within a few seconds, the screen should display data around the TRIG location and the lamp in the DATA key should light. The displayed data should look like that in Figure 2-10. Refer to Section 8 for more information about the TPG.

**Scrolling and Cursors.** Until now you have used the SCROLL knob to make selections in the select fields. In the data display frames, however, the SCROLL knob has a different function. Now it moves the active cursor between data locations and the data itself onto and off of the screen. This is indicated in the upper right corner of the screen. Field selections can now only be made using the SELECT keys.

60. Turn the SCROLL knob *counter-clockwise*. This is the direction of negative location numbers (those that were acquired before the trigger). Note the minus signs at the far left of the display. Continue moving the cursor until it is over location - 10. Note that the trigger location is now near the bottom of the screen.
61. Press the CHANGE ACTIVE CURSOR soft key at the bottom of the screen. Notice that the data moved, putting the new active cursor (cursor 2) in the middle of the screen.
62. Move cursor 2, the dotted cursor, down to (positive) location 10. Note that the location of each cursor is shown at the top of the screen. Notice too that the time difference between these two locations is also shown. In this case it is 1.00  $\mu$ s.

### Glitch Display ON and OFF (State Table).

63. Move the blinking field cursor to the GLITCHES select field with the NEXT key.
64. Press either SELECT key. Note that the selection in the GLITCHES field alternates between ON and OFF. Continue pressing either SELECT key while watching the data. Notice that rows of glitch symbols (◆) appear and disappear as GLITCHES are selected and de-selected. Leave the GLITCHES OFF.

**Timing Diagram Display.** When you first acquired data, the logic analyzer presented it in *state table* form, however, it can also display data in *timing diagram* form.

65. Press the TIMING DIAGRAM soft key. Note the reverse video area to the left of the traces. These are the group and line number identifications of the displayed traces.
66. Note the three vertical lines in the middle of the screen. The one in the center, composed of dots and dashes, is the trigger position. The one on the left is cursor 1, the one you moved to location - 10. The one on the right is cursor 2, the one you moved to location +10.
67. Look at the cursor data in the top center of the screen. Notice that CURSOR 2 is highlighted, indicating that this is the active cursor.
68. Turn the SCROLL knob back and forth. Notice that the active cursor moves and several different things happen on the screen. At the top of the screen the location number is changing. On the left side of the data display, ones and zeroes reflect the status of the data on the displayed lines at the location of the active cursor. On the lower left of the screen, just above the soft keys, is a hexadecimal readout of all of the *valid* data at this location. Note that this readout includes traces which are not displayed, as well as those on the screen. Move the cursor back and forth over a large distance. Notice that the synchronous, 18-channel data is only displayed there part of the time, since it is only valid on the less frequent T2 clocks.

**Expanding the Timing Diagram.**

69. The 1240's blinking field cursor is in the EXPANSION field. Use the SELECT keys to change the horizontal-magnification factor of the display. Leave the EXPANSION factor at \*2. The 1241's blinking field cursor is in the EXPAND field. The two available fields control horizontal and vertical magnification of the display. Leave the EXPAND factors at \*2 and \*1.

**Glitch Display ON and OFF (Timing Diagram).**

70. Move the blinking cursor to the GLITCHES field.
71. Press either SELECT key several times and notice the effect on the display. Those bars that appear and disappear are glitch indicators. Remember that you chose a TPG output that included glitches. Leave the GLITCHES field ON.

**Measuring Time Using the Cursors.**

72. Move the active cursor (Cursor 2) to a location containing glitches. Note that glitch symbols appear in the binary data at the left of the display and in the hexadecimal data at the lower left of the display.
73. Press the CHANGE ACTIVE CURSOR soft key. Cursor 1 is now the active cursor again. Move Cursor 1 to the same location as Cursor 2. Check to ensure that  $CURSOR \Delta = 0.00 \mu s$ .
74. Move Cursor 1 left until it is positioned over the first glitch on any of the data channels. Repeat this process nine more times (ten times total). The cursor's new location is the tenth occurrence of glitches away from Cursor 2. Observe that the  $CURSOR \Delta = 1.65 \mu s$  or  $1.70 \mu s$ . Since this is ten times the interval between sets of glitches, and glitches occur at the frequency of the TPG clock, this is the expected interval from a TPG having a period of 168 ns ( $\pm 1\%$ ) in the 6-MHz-with-glitches mode.

**Search Pattern Entry.**

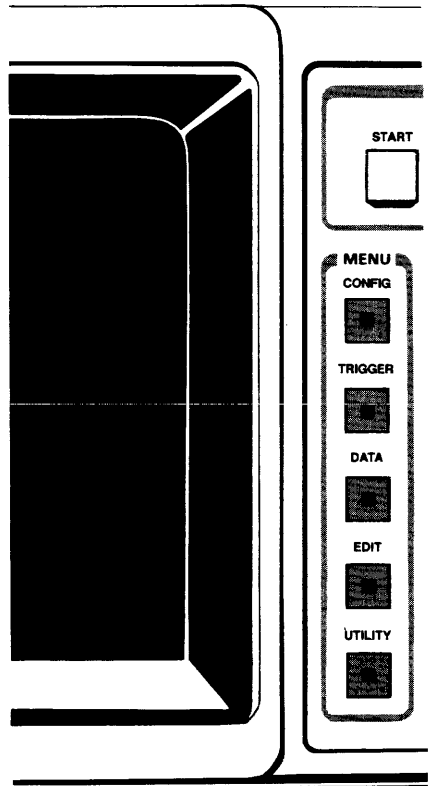
75. Press the EDIT key.
76. Move the cursor up once, to the ENTER DATA FOR field, and replace T1 ONLY with T1 AND T2 by pressing the SELECT *down* key once.
77. Move the cursor down and to the right, to the ADDR field, and enter 1FF.
78. Press the DATA key. Because you were looking at a timing diagram when you left this menu, that timing diagram is still present when you return. Press the STATE TABLE soft key to return to a state table display.
79. Move the blinking field cursor to the HIGHLIGHT field and press the SELECT key to highlight PATTERNS.
80. Press the NEXT HIGHLIGHT DATA soft key. Notice that the active cursor moves to the next occurrence of the pattern 1FF in the ADDR column.

**Storing a Setup.**

81. Press the UTILITY key.
82. Use the SCROLL knob and the CURSOR keys to enter your initials in the FILENAME field.

83. Move the blinking cursor to the right to the STORED IN field. Turn the SCROLL knob. There is only room for one setup in nonvolatile memory (**NVM**). (Three setups can be stored in internal **RAM**, but that is volatile.)
84. Press the STORE NEW FILE soft key.
85. Turn off the instrument and turn it on again. Press the UTILITY key. Notice that there are two files, the one with your initials and INIT. Both contain your setup. That is because the logic analyzer automatically stores the current setup when power is turned off or fails. When someone else uses your instrument and turns it off, their setup will be in INIT and, if they didn't replace it, your setup will still be in the file with your initials.
86. To recover the file with your initials, turn the knob *counter-clockwise* until a **1** appears in the SELECTED field. Press the LOAD FILE soft key, then the X key to confirm. You can now look back through the other menus and verify that the logic analyzer remembered how you set it up.

3



CONFIG

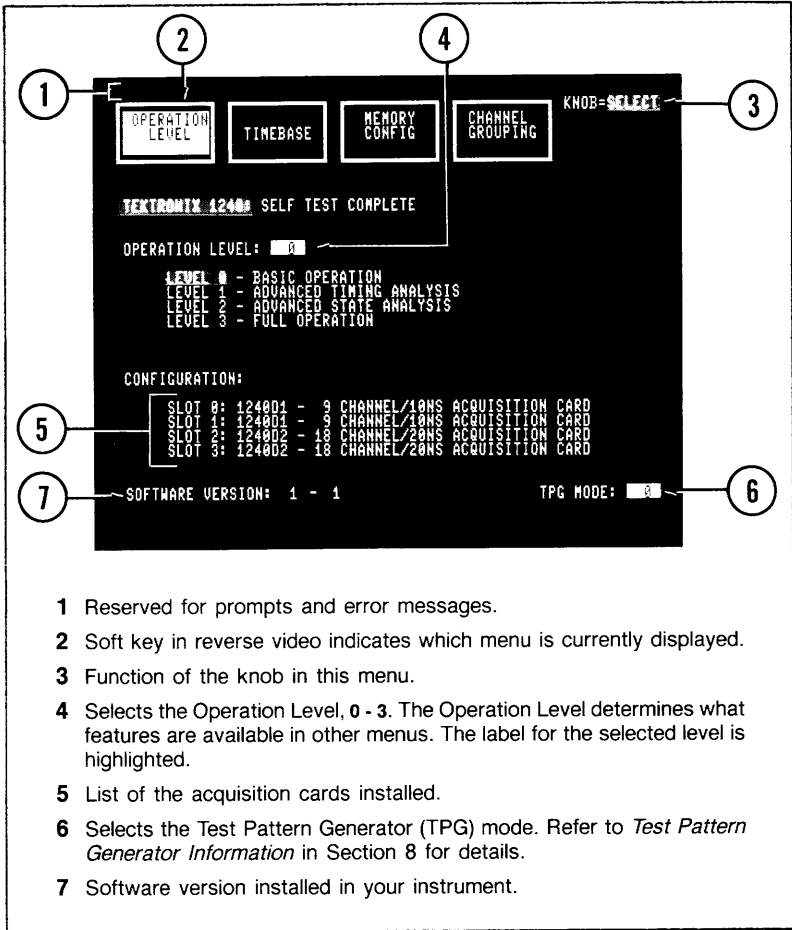
OPERATION LEVEL .....	3-1
TIMEBASE .....	3-2
Active Timebases .....	3-2
Global Event Recognizer Clocked/Unlocked .....	3-3
Asynchronous Timebase .....	3-3
10 ns Acquisition .....	3-3
Glitches .....	3-4
Qualification .....	3-4
Synchronous Timebase .....	3-4
Demultiplexing .....	3-7
MEMORY CONFIG .....	3-10
Pods Acquiring Data .....	3-10
Memory Width vs. Depth .....	3-10
Glitch Storage .....	3-11
Pod-Timebase Assignments .....	3-11
Demultiplexing .....	3-14
INPUT POD Field .....	3-14
TIMEBASE Field .....	3-14
CHANNEL GROUPING .....	3-18
Grouping Basics .....	3-18
Group Name, Input Radix, Display Radix .....	3-18
POD/CHAN Pairs .....	3-18
Guidelines for Entering POD/CHAN Pairs .....	3-21
Building Groups .....	3-23
CLEAR GROUP .....	3-23
DELETE CHANNEL .....	3-23
ADD NEXT CHANNEL .....	3-23
INSERT CHANNEL .....	3-23
Channel Grouping Defaults .....	3-23
Demultiplexing .....	3-24

The CONFIG key on the front panel allows you to access the Operation Level, Memory Config, Timebase, and Channel Grouping menus. These menus work together to determine how the logic analyzer acquires and stores data.

## OPERATION LEVEL

The 1240 and 1241 Logic Analyzers display the Operation Level menu at power-up. See Figure 3-1 for a 1240 menu display.

The four levels are: 0 (Basic Operation), 1 (Advanced Timing Analysis), 2 (Advanced State Analysis), and 3 (Full Operation). Level 0 supports most state and timing analysis applications. Levels 1 and 2 have extra features that provide more flexibility and problem-solving power than is available under Level 0. All features are available in Level 3. An overview of the differences between the levels is provided in Table 8-10 in the *Reference Information* section.



4340-22

**Figure 3-1. 1240 Operation Level menu power-up default display.** The instrument displays this menu at power-up. The blinking cursor must reside in a field before changes can be made to that field. Move the cursor from one field to another with the CURSOR keys. Highlighted areas are for information only and cannot be accessed by the cursor.

The field at the bottom of the menu allows you to select the mode of operation for the Test Pattern Generator (TPG). The TPG is a useful learning aid for the beginning user as well as a valuable tool for instrument verification. It allows the beginning user to get familiar with the logic analyzer without having to connect to an actual system under test. The TPG simulates a data source by sending data patterns to two sets of pins located directly above the probe connections on the right side panel of the instrument. Probes connected to these pins acquire data just as they would from a system under test.

Refer to *Test Pattern Generator Information* in Section 8 for a description of the TPG modes, a listing of the patterns, and TPG timing information.

#### NOTE

*When you acquire data from the TPG, you must set the THRESHOLD fields to **TPG** for cards connected to the TPG outputs. Refer to Figure 3-6 in the description of the Memory Config menu for information about the THRESHOLD field.*

## TIMEBASE

The Timebase menu specifies the number and type of timebases that can be used to control data acquisition. The power-up default condition is one asynchronous timebase with a 20 ns period and no clock qualification.

#### NOTE

*Timebase specifications are set up in this menu, but **pod-timebase assignments made in the Memory Config menu determine what timebases are actually used.** Refer to Pod-Timebase Assignments later in this section under the description of the Memory Config menu.*

## ACTIVE TIMEBASES

The 1240 and 1241 Logic Analyzers can acquire data using one or two timebases. In Operation Levels 2 and 3, the selection in the ACTIVE TIMEBASES field determines the number of timebases (see callout 1 in Figure 3-2). The selections are **T1 ONLY**, **T2 ONLY**, and **T1 AND T2**. Selecting **T1 AND T2** lets you acquire data simultaneously from two sources with different clock rates.

In Operation Levels 0 and 1, T1 is the only available timebase; the ACTIVE TIMEBASES field is not displayed.

You can specify T1 to be an **ASYNC** (asynchronous) or **SYNC** (synchronous) timebase; T2 may be **SYNC** or **DEMUX**. The **DEMUX** selection customizes T2 for demultiplexing; see *Demultiplexing* later in this section for more information. Detailed clock qualification is available for all three timebase types.

## GLOBAL EVENT RECOGNIZER CLOCKED/UNCLOCKED

Generally, logic analyzers test the trigger condition only against data present on the probe tips at the sample point. The 1240 and 1241 Logic Analyzers can recognize events regardless of when they occur. In other words, an event does not have to coincide with a sample point in order for the logic analyzer to trigger on it. The only requirement is that the data be present for the amount of time defined by the global event filter period. (The global event filter specifies the amount of time data must be present at the probe tips to be considered an event. Refer to *Global Event Recognizer* in Section 4 for more information about the filter.) This feature applies to the global event recognizer<sup>1</sup> and is controlled by the GLOBAL EVENT = **CLOCKED/UNCLOCKED** field in the Timebase menu (see callout 2 in Figure 3-2).

The GLOBAL EVENT = **CLOCKED/UNCLOCKED** field is displayed when the Operation Level is 1 or 3. The **CLOCKED** selection means that only events coinciding with a sample point are compared to the global event recognizer. When you choose **UNCLOCKED**, data from the system under test is continuously compared to the global event recognizer; the global event can be satisfied by any event that meets or exceeds the global event filter period.

Figure 3-3 demonstrates the **UNCLOCKED** selection. Use **UNCLOCKED** when you want to be able to trigger on an event that happens between occurrences of the sample clock.

Data is not stored in acquisition memory unless it occurs at a sample point. Therefore when using **UNCLOCKED**, it is possible to trigger on an event that does not get stored. This is demonstrated in Figure 3-3. To see the event, reacquire with a faster clock.

## ASYNCHRONOUS TIMEBASE

Only timebase T1 can be **ASYN**. Refer to the top portion of Figure 3-2 for descriptions of the fields that define an asynchronous timebase.

The default asynchronous clock period is **20 NS**; other selections are available from **10 NS** to **1 S**. The 10 ns period is not always available; see *10 ns Acquisition*, next.

**10 ns Acquisition.** The **10 NS** selection for the ASYNC clock period is only available if:

- At least one 9-channel card (1240D1) is installed.
- All 18-channel cards (1240D2) are assigned to timebase T2 in the Memory Config menu (requires Operation Level 2 or 3).
- Glitch storage is disabled (**GLITCHES OFF** selected in the Memory Config menu).

If 9- and 18-channel cards are installed, use the following procedure to change to a setup that supports 10 ns acquisition:

1. In the Operation Level menu, select Level 2 or 3.
2. In the Timebase menu, select ACTIVE TIMEBASES: **T1 AND T2**. Select TIMEBASE 1: **ASYN**.
3. In the Memory Config menu, select **GLITCHES OFF**. Select **T2** in the TIMEBASE field for each 18-channel card.

---

<sup>1</sup> The global event recognizer is specified in the Trigger Spec menu. It is called "global" because you can specify an event using values for all connected channels (regardless of the timebase they are associated with), and because it is in effect during the entire acquisition. Refer to *Global Event Recognizer* in Section 4 for more information.



4. In the Timebase menu, select **10 NS** for the asynchronous clock period.
5. Connect the clock lead of any probe's pod that is specified in the T2 clock equation to an active signal compatible with the selected threshold of that probe.

If no 18-channel cards are installed, the **10 NS** selection is available if **GLITCHES OFF** is selected in the Memory Config menu.

**Glitches.** Glitches can be acquired only on 9-channel cards. In addition, glitch acquisition requires a timebase selection of T1 ASYNC and a clock period of at least 20 ns (glitches cannot be acquired on T2 or with a synchronous timebase); GLOBAL EVENT = **CLOCKED** must be selected. Finally, **GLITCHES ON** must be selected in the Memory Config menu (see callout 4 in Figure 3-6.)

**Qualification.** Each pod has one clock/qualifier line. The logic analyzer determines clock qualification by ANDing together the C/Q line from each pod. For each C/Q line, you can select 1 or 0 (for signals above or below the acquisition card threshold set in the Memory Config menu), or a blank (no qualification). The logic analyzer samples data only when the qualifier conditions are true.

Clock qualification for T1 is not available when both T1 and T2 are active and T1 is ASYNC 10 NS. When these selections are made, the T1 qualifier fields are not displayed.

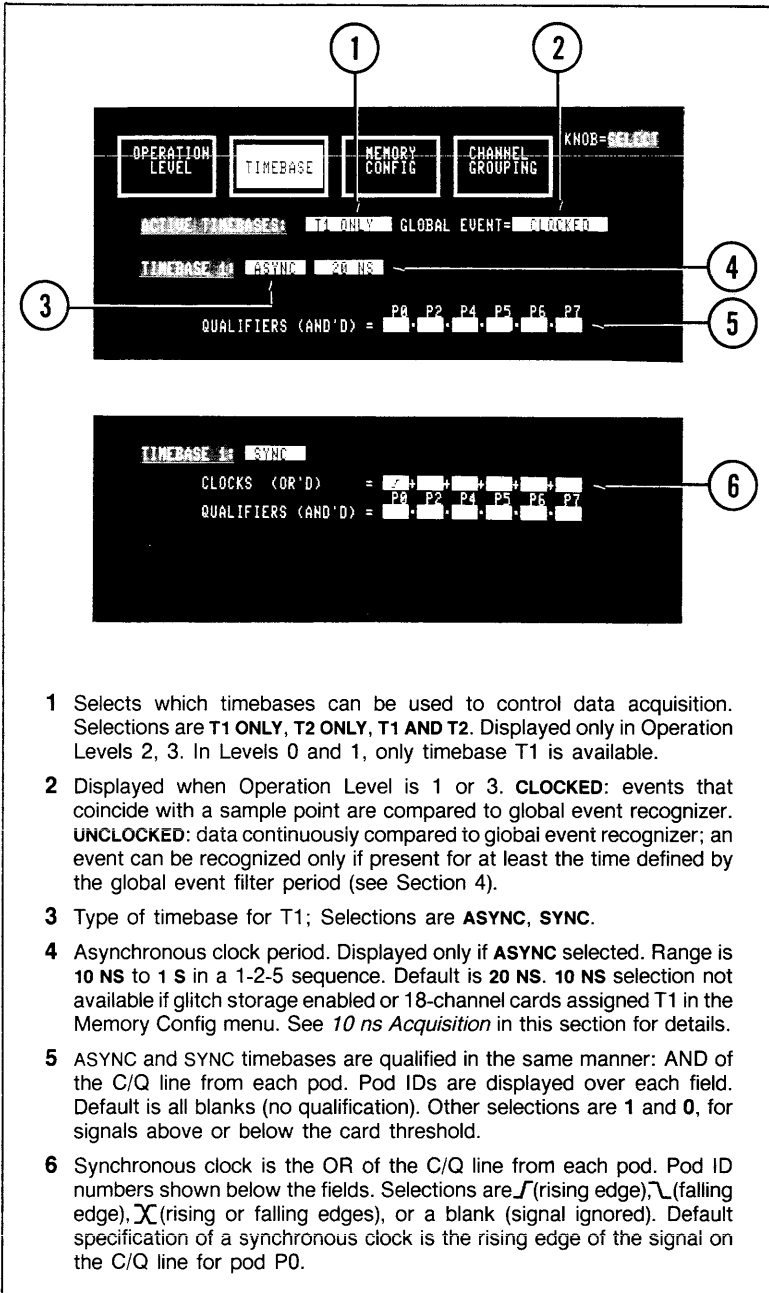
## SYNCHRONOUS TIMEBASE

Both T1 and T2<sup>2</sup> can be **SYNC**. The second portion of Figure 3-2 shows the fields used to define and qualify a synchronous timebase.

A synchronous timebase is specified as the logical OR of the transitions on the clock/qualifier line from each pod. For each C/Q line, you can select  $\uparrow$  (rising edge),  $\downarrow$  (falling edge),  $\times$  (rising or falling edges), or a blank (signal ignored). The default synchronous timebase is the rising edge of the signal on the pod P0 C/Q line (see callout 6 in Figure 3-2).

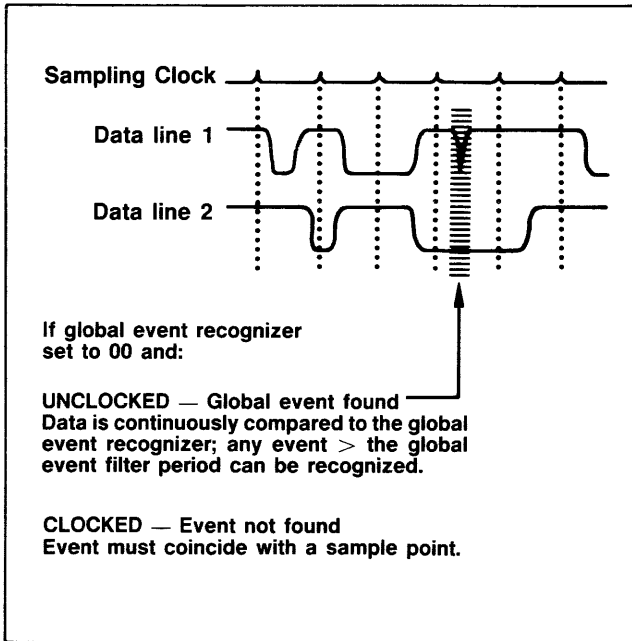
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<sup>2</sup> T2 is available only in Operation Levels 2 and 3.



- 1 Selects which timebases can be used to control data acquisition. Selections are **T1 ONLY**, **T2 ONLY**, **T1 AND T2**. Displayed only in Operation Levels 2, 3. In Levels 0 and 1, only timebase T1 is available.
- 2 Displayed when Operation Level is 1 or 3. **CLOCKED**: events that coincide with a sample point are compared to global event recognizer. **UNCLOCKED**: data continuously compared to global event recognizer; an event can be recognized only if present for at least the time defined by the global event filter period (see Section 4).
- 3 Type of timebase for T1; Selections are **ASYNC**, **SYNC**.
- 4 Asynchronous clock period. Displayed only if **ASYNC** selected. Range is **10 NS** to **1 S** in a 1-2-5 sequence. Default is **20 NS**. **10 NS** selection not available if glitch storage enabled or 18-channel cards assigned T1 in the Memory Config menu. See *10 ns Acquisition* in this section for details.
- 5 ASYNC and SYNC timebases are qualified in the same manner: AND of the C/Q line from each pod. Pod IDs are displayed over each field. Default is all blanks (no qualification). Other selections are **1** and **0**, for signals above or below the card threshold.
- 6 Synchronous clock is the OR of the C/Q line from each pod. Pod ID numbers shown below the fields. Selections are  $\uparrow$  (rising edge),  $\downarrow$  (falling edge),  $\times$  (rising or falling edges), or a blank (signal ignored). Default specification of a synchronous clock is the rising edge of the signal on the C/Q line for pod P0.

Figure 3-2. Timebase menu: specifying an ASYNC or a SYNC timebase.



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**Figure 3-3. Demonstration of Global Event Recognizer UNLOCKED.** In this example, the global event recognizer is set to 00. This event will be recognized (shaded area) only if the global event recognizer is UNLOCKED. If the global event recognizer is CLOCKED, the 00 event will not be found because it does not occur at a sample point.

Synchronous and asynchronous timebases are qualified in the same manner: as the logical AND of the C/Q line from each pod (see callout 5 in Figure 3-2).

**NOTE**

*Pod clock/qualifier lines are used to specify synchronous clocks and to determine clock qualification. C/Q lines are independent of data lines; any C/Q line can be used to specify or qualify any timebase. A given C/Q line can be used simultaneously in several specifications. The C/Q line operates normally even if a pod's data lines are not stored due to memory chaining (see Memory Config for details).*

## DEMULPLEXING

Many systems transmit two types of data on the same lines at different times (such as address and data information on a bus). The 1240 and 1241 Logic Analyzers have a demultiplexing capability and can separate this information so that each type of data can be studied independently.

Demultiplexing occurs when: 1) a set of data channels is sampled by two different timebases, and 2) the data acquired at different times is stored in different areas of memory. Use the Timebase menu to set up the timebases for the first step of the process. The rest of the conditions are specified in the Memory Config menu and are discussed later in this section.

The **DEMUX** selection customizes T2 for demultiplexing. **DEMUX** defines T2 as the combination of separate, synchronous clocks named T2 First (T2 F) and T2 Last (T2 L). The logic analyzer forms the storage clock for T2 by alternately recognizing T2 F then T2 L.<sup>3</sup> T2 F defines the synchronous clock that drives the first data from a multiplexed bus. T2 L defines the synchronous clock that drives the second data on the bus. Figure 3-4 describes the menu fields that are displayed when you select **DEMUX**.

T2 F and T2 L must alternate. Symmetrical, phase-shifted clocks (as shown in Case 1 of Figure 3-5) naturally alternate. If the clocks do not alternate (as in Case 2 of Figure 3-5), the logic analyzer discards clock occurrences until they do. **Data is not stored until both T2 F and T2 L have occurred.**

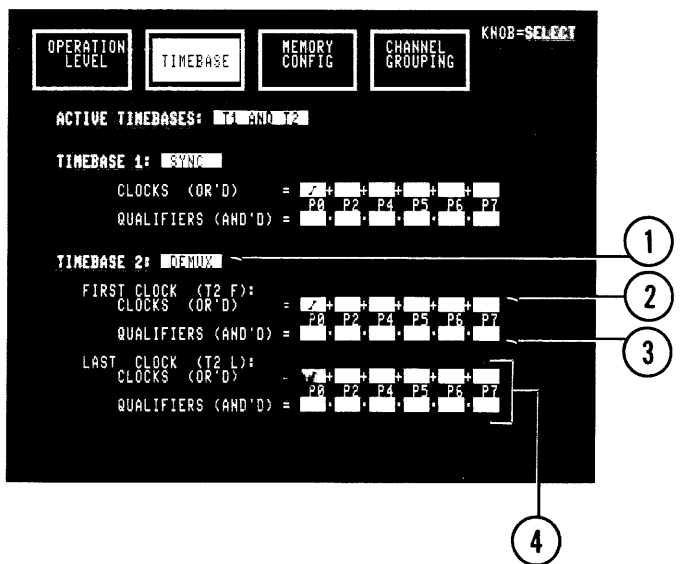
T2 DEMUX is not the only demultiplexing method. Instead of T2 F and T2 L, you can use T1 (ASYN or SYNC) and T2 SYNC. This method is demonstrated in Case 3 of Figure 3-5.

### NOTE

*The only menus that distinguish between T2 F and T2 L are the Timebase and Memory Config menus. All other menus refer to these clocks collectively as T2.*

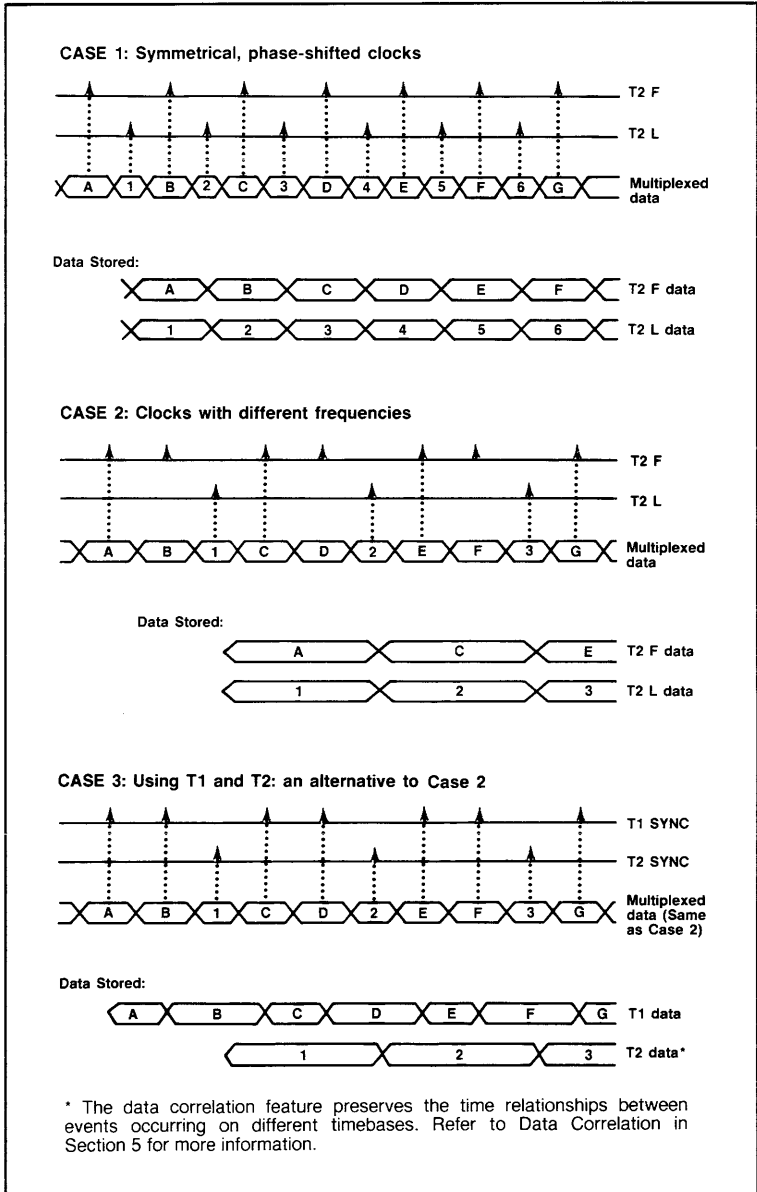
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<sup>3</sup> At least 10 ns is required between T2 F and T2 L and at least 20 ns between T2 L and T2 F; see Table 8-5, Electrical Specifications.



- 1 Type of timebase for T2; selections are **SYNC** and **DEMUX**. **DEMUX** defines T2 as the combination of two separate synchronous clocks, T2 F and T2 L.
- 2 Defines T2 F, first synchronous clock of T2 DEMUX. All synchronous clocks are defined in the same manner: the OR of the C/Q line from each pod. Selections are  $\uparrow$  (rising edge),  $\downarrow$  (falling edge),  $\times$  (rising or falling edges), or a blank (signal ignored). Default specification is the rising edge of the signal on the C/Q line for pod P0.
- 3 ANDed clock qualification for T2 F; one select field per installed pod. Default is all blanks (no qualification); other selections are **1** and **0**.
- 4 Defines T2 L, second synchronous clock of T2 DEMUX.

**Figure 3-4. Timebase menu: description of T2 DEMUX fields.** The DEMUX selection is available only for timebase T2.



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**Figure 3-5. Setting up timebases for demultiplexing, three examples.** When timebase T2 is set to DEMUX, it is a combination of two separate, synchronous clocks, T2 F and T2 L. The logic analyzer alternately recognizes T2 F then T2 L. Case 3 uses dual timebases (T1 and T2) to demultiplex data that was missed in Case 2.

## MEMORY CONFIG

### PODS ACQUIRING DATA

The arrangement of rectangles in the tabular portion of the menu (see Figure 3-6) corresponds to the pattern of pod attachments on the right side-panel of the logic analyzer. Each rectangle represents one pod. Since a 9-channel acquisition card uses one pod, each 9-channel card has only one rectangle in the display; 18-channel cards have two adjacent rectangles. The fields displayed inside a rectangle identify the pod and define how it acquires data.

Data is acquired only with pods whose IDs are displayed under the INPUT POD columns (callout 7 in Figure 3-6). If a specific Pod ID is not displayed, then the logic analyzer is not set to acquire data with that pod, even if it is physically attached to an acquisition card.

To determine the ID of a specific pod, just press the button on the back edge of the pod's plastic case. The Pod ID will be displayed on the top line of the screen.

### MEMORY WIDTH VS. DEPTH

The 1240 and 1241 Logic Analyzers store the data supplied by each pod in a separate area of acquisition memory; call it a "memory segment." Since a 9-channel card uses only one pod, all data acquired by a 9-channel card is stored in one memory segment. Data acquired by an 18-channel card is stored in two memory segments, one for each pod.

How much information is stored in each memory segment is controlled by the 9-channel and 18-channel width vs. depth fields <sup>4</sup> (see callouts 2 and 3 in Figure 3-6). The first value in each field is the number of channels acquiring data (width); <sup>5</sup> the second value is the number of samples stored per channel (depth). The depth of one memory segment is 513 samples. <sup>6</sup> To state this another way: the basic number of samples stored per pod is 513.

In Operation Level 0, the width vs. depth fields are fixed at basic values; each pod supplies data to fill one memory segment. In Levels 1 - 3, the available selections vary with the number and type of acquisition cards installed (refer to Tables 3-1 and 3-2). Selections with larger depth values "chain" memory segments together to store more data per channel.

As you can see in Tables 3-1 and 3-2, at least two 9-channel or two 18-channel cards are required for memory chaining. Memory in 9-channel cards cannot be chained to memory in 18-channel cards. Since the amount of memory in each acquisition card is fixed, width values must decrease as depth values increase. Smaller width values indicate that fewer pods are supplying data.

---

<sup>4</sup> If your instrument has just one type of acquisition card, only the width vs. depth field for that card type is displayed.

<sup>5</sup>  $\text{Width} \div 9 = \text{number of pods supplying data.}$

<sup>6</sup> If **GLITCHES ON** is selected, 9-channel card memory depth is halved, but each data sample includes glitch information. See *Glitch Storage* later in this section for more information.

The tabular portion of the menu is rearranged as you change the memory width vs. depth fields. The depth of the rectangles for each pod indicates how much memory is reserved for data from that pod. In Figure 3-6, the width vs. depth selections are set so that each pod will supply data to fill one memory segment. Figure 3-7 illustrates chained memory for two 9-channel cards. Notice that the rectangle for pod P0 is twice as deep as it was in Figure 3-6. Also notice that pod P2 is not displayed. This arrangement shows that the 9-channel width vs. depth selection chained the memory for pods P0 and P2 together to double the number of samples stored per channel for pod P0. The data lines from P2 are not used.<sup>7</sup>

## GLITCH STORAGE

Glitches can be acquired only on 9-channel cards. In addition, the logic analyzer can acquire glitches only if you select **T1 ASYNC**, a clock rate of at least 20 ns, and **GLOBAL EVENT = CLOCKED** in the Timebase menu. Glitch storage is enabled by the **GLITCHES ON/OFF** field to the right of the 9-channel width vs. depth field in the Memory Config menu (see callout 4 in Figure 3-6). When you select **GLITCHES ON**, glitch information is stored for each data sample acquired.

**GLITCHES ON** also enables glitch triggering; you must select **GLITCHES ON** to be able to enter the glitch symbol (◆) in the event recognizers in the Trigger Spec menu (see Section 4).

When glitch storage is on, the depth of each 9-channel card memory segment is halved, and the minimum asynchronous clock period is 20 ns.

## POD-TIMEBASE ASSIGNMENTS

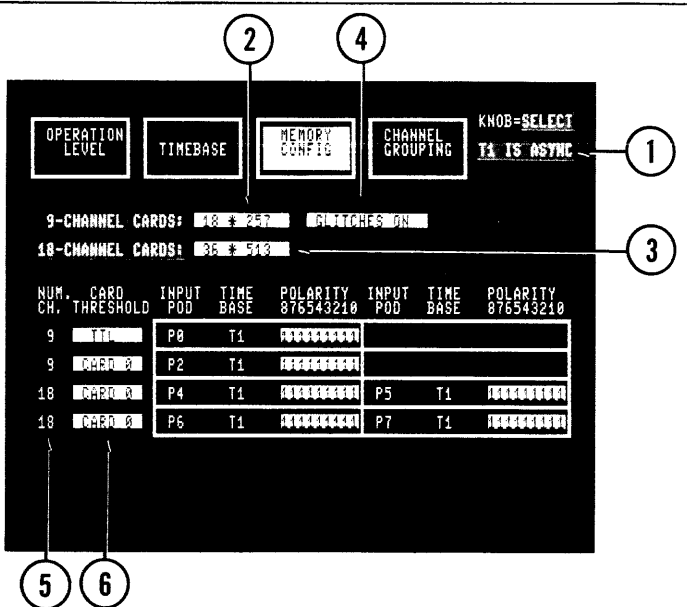
A timebase name is listed in the **TIMEBASE** column of each rectangle (see callout 8 in Figure 3-6). The logic analyzer uses this timebase with the listed pod to clock data into acquisition memory. *Timebases are specified in the Timebase menu, but the fields in the TIMEBASE column of the Memory Config menu determine how timebases are actually used.*

In Operation Levels 0 and 1, all pods are clocked by T1; no other timebase selections are available. In Levels 2 and 3, the available selections depend on the number and type of timebases specified in the Timebase menu. If both T1 and T2 are active or if T2 is DEMUX, the entries in the **TIMEBASE** column become select fields and are displayed in reverse video. Table 3-3 lists the available timebase selections; any timebase can be assigned to any pod.

A reminder of what timebases are currently specified in the Timebase menu is displayed in highlighted video in the upper-right corner of the Memory Config menu (see callout 1 in Figure 3-6).

<sup>7</sup> Data lines from chained pods are not active, but the C/Q lines operate normally. The threshold selection displayed to the left of a chained pod only applies to the C/Q line.



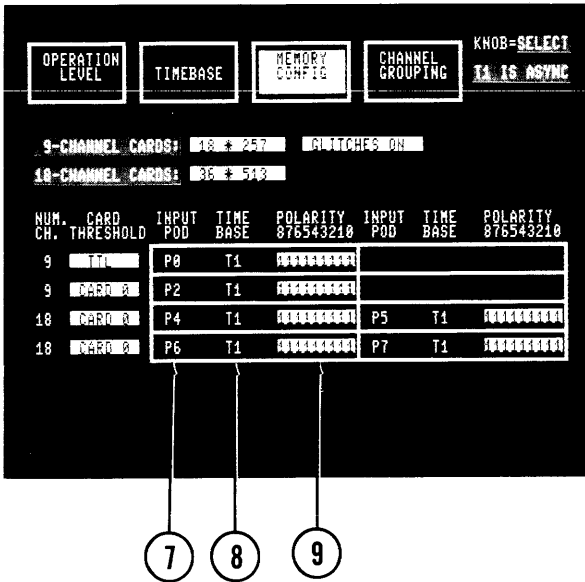


- 1 Reminder of how timebases are set up in the Timebase menu.
- 2 Acquisition memory width vs. depth for 9-channel cards. Appears if at least one 9-channel card is installed. First value is the number of channels to be stored (width); second value is the number of samples stored per channel (depth). Values are fixed in Level 0. In Levels 1-3, values vary with the number of cards installed; see Table 3-1. If **GLITCHES ON** is selected (callout 4), 9-channel memory depth is halved.
- 3 Acquisition memory width vs. depth for 18-channel cards. Appears if at least one 18-channel card is installed. Values are fixed in Level 0. In Levels 1-3, values vary with the number of cards installed; see Table 3-2.
- 4 Glitch storage (9-channel cards only). Selections are **GLITCHES ON** and **GLITCHES OFF**. If glitch storage is on, 9-channel memory depth is halved but each data sample includes glitch information.
- 5 Number of channels on each installed card (card type).
- 6 Card threshold voltage, one field for each installed card. Used with POLARITY fields to determine logic levels for incoming data. Selections include **TTL**, **-ECL**, **TPG** (used with the Test Pattern Generator), and a range of voltages between **+6.35 V** and **-6.35 V** in 50 mV increments. Cards in slots 1-3 also have a **CARD 0** selection which matches the threshold already set for card 0 and lets you quickly change several cards to the same threshold. (When a fixed-threshold probe is attached to a card, the threshold of the probe is used. The THRESHOLD field can still be changed, but the selection has no effect.)

(cont.)

Figure 3-6. Memory Config default display. This default setup occurs when the logic analyzer is equipped with two 9-channel and two 18-channel acquisition cards.

(cont.)



- 7 INPUT POD. Data from the pod is clocked into memory according to the timebase shown. Becomes a select field for odd-numbered pods of 18-channel cards when T1 and T2 are active or when T2 is DEMUX.
- 8 Timebase used to clock data from the pod into memory. Timebases are specified in the Timebase menu, but this field determines how timebases are actually used. Entries in this column become select fields when T1 and T2 are active or when T2 is DEMUX; see Table 3-3 for selections.
- 9 Channel Polarity. Applied to the card threshold to determine the logic level of incoming signals. Nine digits correspond to pod leads 8-0. A 1 indicates positive-true logic; negative-true logic is indicated by 0. If a signal is above the threshold voltage and the polarity of that lead is 1, the signal is "true," and the value of the signal is 1. Under the same conditions but a polarity of 0, the signal is "false," with a value of 0. Polarity is applied at the probe tip; therefore, changes to this field do not affect display of previously acquired data.

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Figure 3-6. Memory Config default display (cont.).

## DEMULPLEXING

To demultiplex different types of data off one set of channels, you need to be able to clock the channels with two different timebases and store the data acquired at different times in different areas of memory. For every nine channels to be demultiplexed, you will need one 18-channel card or two 9-channel cards. T2 DEMUX or two timebases are required, so the Operation Level must be 2 or 3. Refer to *Demultiplexing* in the description of the Timebase menu earlier in this section for information on setting up the timebase(s). The rest of the conditions can be set up very quickly in the Memory Config menu with the INPUT POD and TIMEBASE fields. Figure 3-8 shows a sample Memory Config setup for demultiplexing using one 18-channel card.

Demultiplexing is most efficient with 18-channel cards because only one pod needs to be connected to the data source. Only one pod is necessary because of the special feature of the INPUT POD field. To demultiplex with 9-channel cards, you must connect two pods to the data source.

**INPUT POD Field.** When T1 and T2 are active or when T2 is DEMUX, the INPUT POD field for the odd-numbered pod of each 18-channel card is a reverse video select field. Selections are the IDs for both pods connected to that 18-channel card. For demultiplexing, select the even-numbered Pod ID. This selection causes data from a single pod to be stored in different areas of memory.

**TIMEBASE Field.** When T1 and T2 are active or when T2 is DEMUX, all TIMEBASE entries are select fields; Table 3-3 lists the available selections. For demultiplexing, assign one timebase selection (such as T2 F) to one area of memory and another timebase selection (such as T2 L) to the other area of memory. Callout 3 in Figure 3-8 shows an example demultiplexing setup using T2 DEMUX and an 18-channel card.

**Table 3-1**  
**MEMORY WIDTH VS. DEPTH SELECTIONS**  
**FOR 9-CHANNEL CARDS**  
 (Operation Levels 1 - 3) <sup>a</sup>.

Number of 9-ch cards	Width vs. Depth <sup>b</sup>	Pods Acquiring Data
1	9 * 513	0
2	18 * 513 9 * 1025	0, 2 0
3	27 * 513 9 * 1537	0, 2, 4 0
4	36 * 513 18 * 1025 9 * 2049	0, 2, 4, 6 0, 4 0

<sup>a</sup> In Operation Level 0, 9-channel width vs. depth is not a select field. With glitch storage off, standard memory depth is 513 samples.

<sup>b</sup> If glitch storage is on, acquisition memory depth is halved but each data sample includes glitch information.

**Table 3-2**  
**MEMORY WIDTH VS. DEPTH SELECTIONS FOR 18-CHANNEL CARDS**  
 (Operation Levels 1 - 3)<sup>a</sup>

# 18-Ch Cards	Width vs. Depth	Pods Acquiring Data With:			
		0 9-Ch Cards	1 9-Ch Card	2 9-Ch Cards	3 9-Ch Cards
1	18 * 513	0/1	2/3	4/5	6/7
2	36 * 513	0/1, 2/3	2/3, 4/5	4/5, 6/7	—
	18 * 1025	0/1	2/3	4/5	—
3	54 * 513	0/1, 2/3, 4/5	2/3, 4/5, 6/7	—	—
	18 * 1537	0/1	2/3	—	—
4	72 * 513	0/1, 2/3, 4/5, 6/7	—	—	—
	36 * 1025	0/1, 4/5	—	—	—
	18 * 2049	0/1	—	—	—

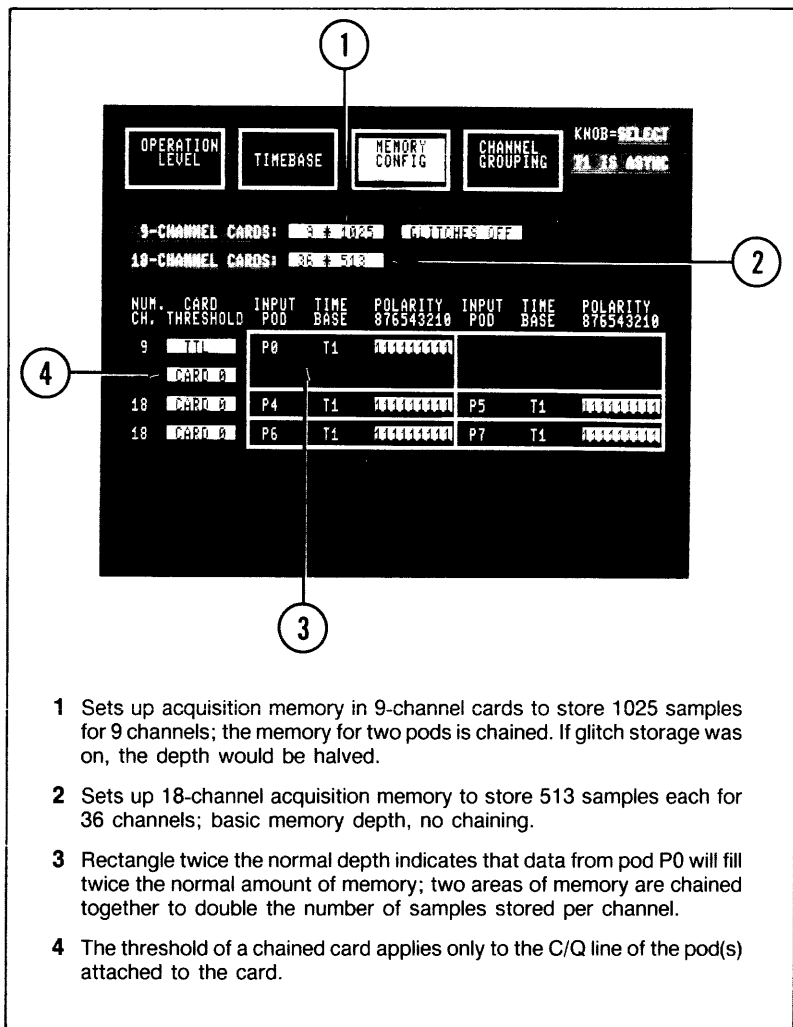
<sup>a</sup> In Operation Level 0, 18-channel width vs. depth is not a select field. Standard memory depth is 513 samples.

**Table 3-3**  
**TIMEBASE SELECTIONS FOR**  
**POD-TIMEBASE ASSIGNMENTS IN THE MEMORY CONFIG MENU**  
 (Operation Levels 2 and 3)<sup>a</sup>

Active Timebases <sup>b</sup>	T2 is <sup>b</sup>	Timebase Selections
T1 ONLY	—	T1
T2 ONLY	SYNC DEMUX	T2 T2 F, T2 L
T1 AND T2	SYNC DEMUX	T1, T2 T1, T2 F, T2 L

<sup>a</sup> In Operation Levels 0 and 1, all pods are assigned T1; no other selections are available.

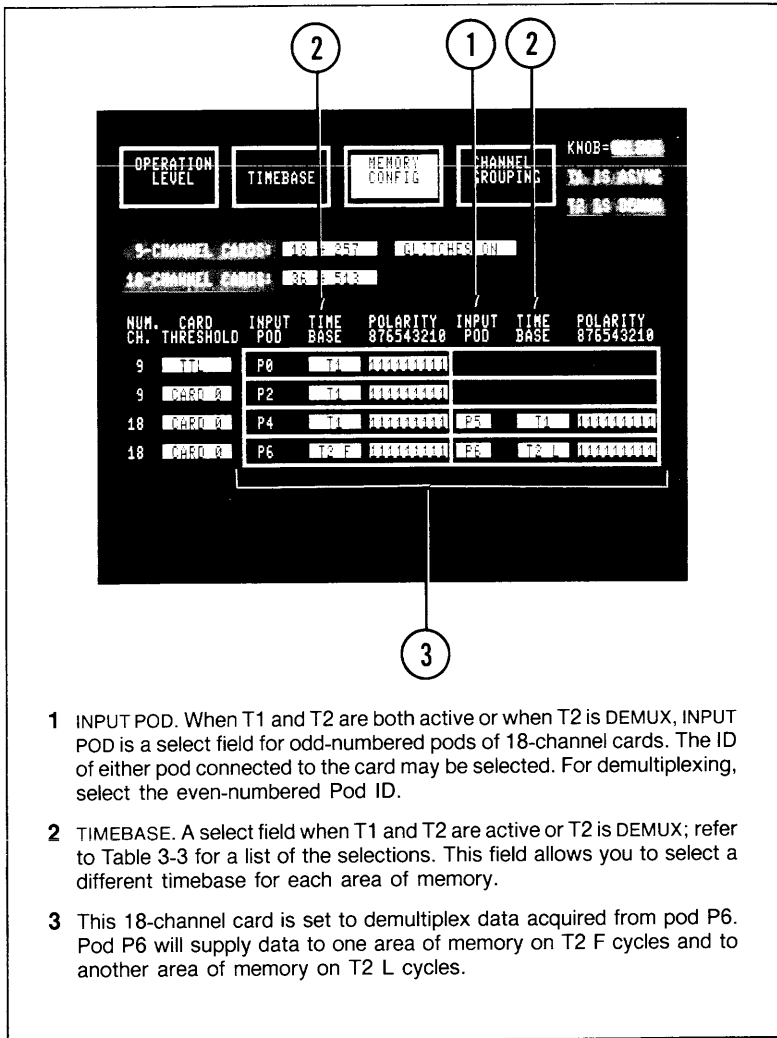
<sup>b</sup> Determined in Timebase menu.



- 1 Sets up acquisition memory in 9-channel cards to store 1025 samples for 9 channels; the memory for two pods is chained. If glitch storage was on, the depth would be halved.
- 2 Sets up 18-channel acquisition memory to store 513 samples each for 36 channels; basic memory depth, no chaining.
- 3 Rectangle twice the normal depth indicates that data from pod P0 will fill twice the normal amount of memory; two areas of memory are chained together to double the number of samples stored per channel.
- 4 The threshold of a chained card applies only to the C/Q line of the pod(s) attached to the card.

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**Figure 3-7. Memory Config display illustrating memory chaining.** This display shows memory from two 9-channel cards chained together to increase the number of samples stored per channel for pod P0. The depth of the rectangles in the display changes as you change the width vs. depth; the size of each rectangle is a visual indicator of how many samples will be stored for each pod.



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**Figure 3-8. Memory Config example demultiplexing setup.** This example uses T2 DEMUX and one 18-channel card. Each rectangle in the display represents an area of acquisition memory. The INPUT POD field identifies which pod supplies data to that area of memory. The TIMEBASE field determines when the pod will sample data.

## CHANNEL GROUPING

Use this menu to organize channels from 9- and 18-channel cards into groups for data entry and display purposes. A "group" is a collection of channels from one card type.

If your 1240 or 1241 Logic Analyzer is equipped with at least one 9-channel and one 18-channel card, a select field labeled CARD TYPE is displayed in the upper right portion of the screen. This field allows you to select 9- or 18-channel grouping. Grouping principles are the same for both card types.

The default grouping arrangement displayed when you first enter this menu is based on the current setup of the Memory Config menu. Figure 3-9 describes the default settings for 9-channel grouping when two 9-channel cards are installed (Memory Config setup shown in Figure 3-6). Variations in the default settings due to different instrument configurations are discussed later in this section under *Channel Grouping Defaults*. Figure 3-10 shows default 18-channel grouping based on the Memory Config demultiplexing setup shown in Figure 3-8.

You can specify a total of 10 groups, five groups using channels from 9-channel cards and five groups using channels from 18-channel cards. The maximum group size is 36 channels.

### NOTE

*The default grouping arrangements are in effect the first time you access Channel Grouping. These defaults are based on the current Memory Config setup. You can rearrange the grouping to suit your needs using the procedures described in the following paragraphs. Be aware that changes to the Memory Config menu may affect the grouping arrangement. See Table 8-3 for details.*

## GROUPING BASICS

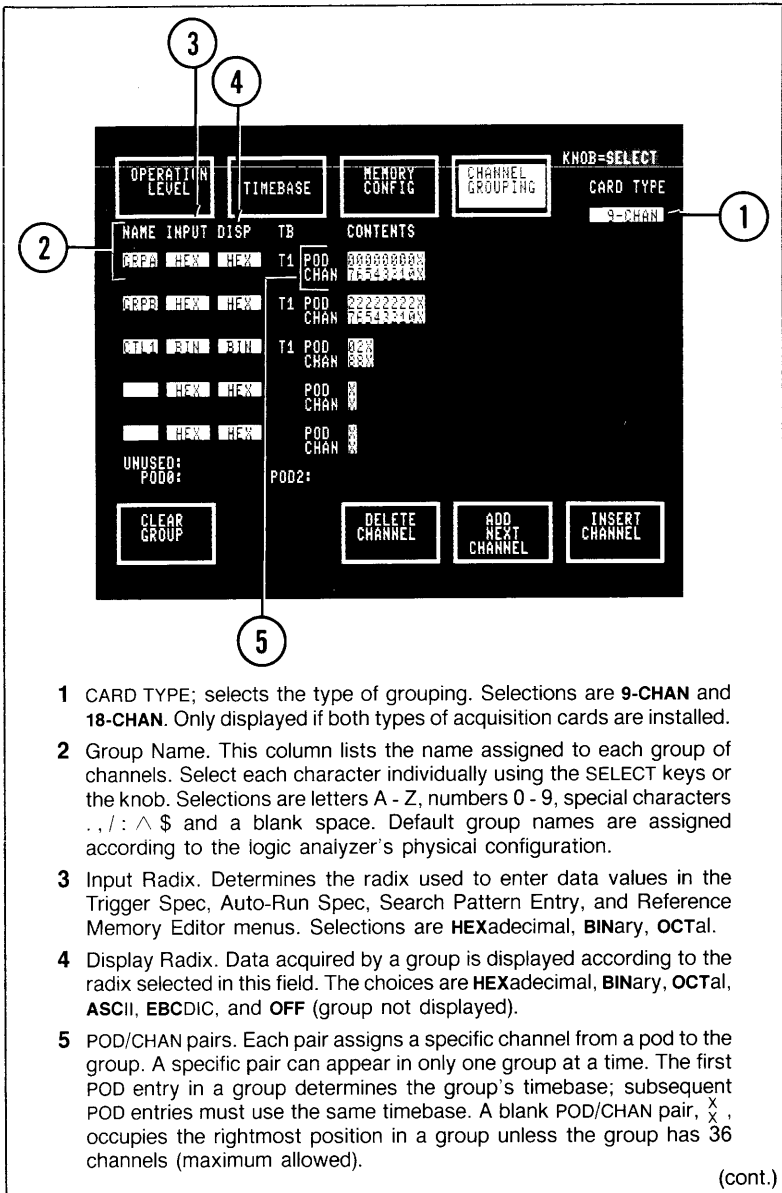
**Group Name, Input Radix, Display Radix.** A group is identified in other menus by the characters entered in the NAME field. The available characters are letters A - Z, numbers 0 - 9, special characters . , / : ^ \$ and a blank space. A group name is four characters long; use the knob or the SELECT keys to enter each character individually.

Data values in the Trigger Spec, Auto-Run Spec, Search Pattern Entry, and Reference Memory Editor menus are entered according to the input radix. Choices for input radix are **HEX**adecimal, **BIN**ary, and **OCT**al.

Data acquired by a group of channels is displayed according to the group's display radix. The selections available are **HEX**adecimal, **OCT**al, **BIN**ary, **ASCII**, **EBCDIC**, and **OFF** (group not displayed). To display data acquired by a group of channels, the logic analyzer applies the selected display radix starting with the least significant (right-most) channel and working toward the most significant channel. If the number of channels in a group is not a multiple of the number of channels used to form one digit of the display radix, the missing channels are assumed to be 0. Refer to Table 3-4.

**POD/CHAN Pairs.** Groups are built with Pod/Channel pairs. Each pair assigns a specific channel from a pod to the group. As seen in Figure 3-9, a POD/CHAN pair is one digit in the POD field and the digit directly beneath it in the CHAN field.

Near the bottom of the display is a list, labeled UNUSED, showing the pod numbers that can be used for grouping and the channels in each pod that are not currently assigned to a group. If you delete channels from a group, clear an entire group, or change a pod-timebase assignment in the Memory Config menu, the unused channels appear in this list.



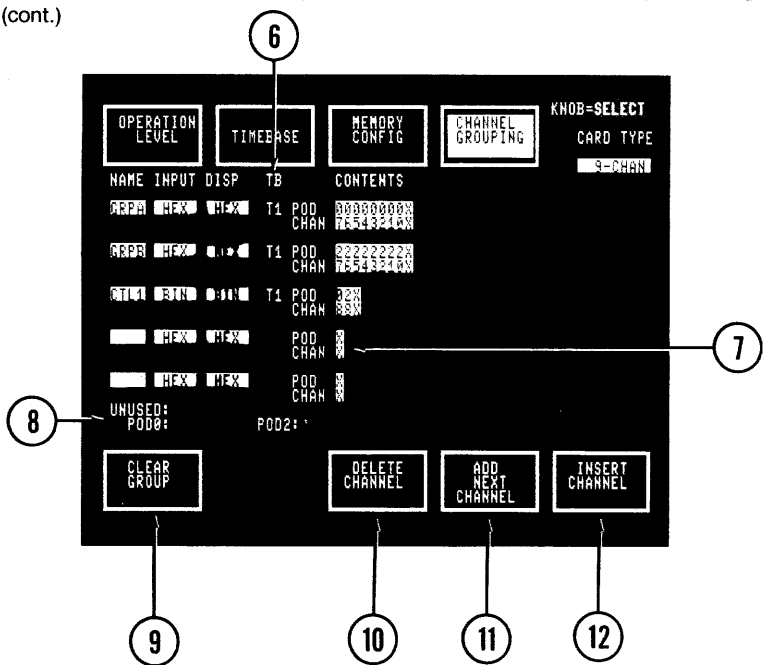
- 1 CARD TYPE; selects the type of grouping. Selections are **9-CHAN** and **18-CHAN**. Only displayed if both types of acquisition cards are installed.
- 2 Group Name. This column lists the name assigned to each group of channels. Select each character individually using the SELECT keys or the knob. Selections are letters A - Z, numbers 0 - 9, special characters ., /: ^ \$ and a blank space. Default group names are assigned according to the logic analyzer's physical configuration.
- 3 Input Radix. Determines the radix used to enter data values in the Trigger Spec, Auto-Run Spec, Search Pattern Entry, and Reference Memory Editor menus. Selections are **HEX**adecimal, **BIN**ary, **OCT**al.
- 4 Display Radix. Data acquired by a group is displayed according to the radix selected in this field. The choices are **HEX**adecimal, **BIN**ary, **OCT**al, **ASCII**, **EBCDIC**, and **OFF** (group not displayed).
- 5 POD/CHAN pairs. Each pair assigns a specific channel from a pod to the group. A specific pair can appear in only one group at a time. The first POD entry in a group determines the group's timebase; subsequent POD entries must use the same timebase. A blank POD/CHAN pair,  $\frac{x}{x}$ , occupies the rightmost position in a group unless the group has 36 channels (maximum allowed).

(cont.)

**Figure 3-9. Default 9-channel grouping when two 9-channel cards are installed.** Channel grouping is closely related to the Memory Config setup. This display is based on the 9-channel portion of the Memory Config setup shown in Figure 3-6.



(cont.)



- 6** Group Timebase; timebase associated with each group. When the first pod number is entered in the POD field, the timebase associated with that pod in the Memory Config menu is displayed in the TB column. When T2 is displayed in this column, it is shown in highlighted video. (These are informational fields only; they cannot be accessed by the field cursor.)
- 7** Unused group.
- 8** UNUSED List. Pod numbers and the channels in each pod that are not currently assigned to a group. In this display, all channels are assigned.
- 9** Deletes the group containing the blinking field cursor. All channels assigned to the deleted group appear in the UNUSED list. No action is taken until you confirm the operation by pressing the X key.
- 10** Deletes the POD/CHAN pair at the location of the field cursor; the channel is added to the UNUSED list.
- 11** Adds a new POD/CHAN pair to the right of the pair where the field cursor is located. The new pair has the same POD value as the preceding pair, but the next lower CHAN value.
- 12** Inserts  $\begin{matrix} X \\ \chi \end{matrix}$  to the left of the field cursor. The POD and CHAN characters can then be changed to other values.

Figure 3-9. Default 9-channel grouping when two 9-channel cards are installed (cont.).

Valid POD entries are pod numbers shown in the UNUSED list, and X (no pod specified). The UNUSED list is based on pod numbers for that card type in the Memory Config menu.

The first non-X POD entry for a group determines the timebase for the group. Subsequent POD selections for the group must use the same timebase. This is a concern only in Operation Levels 2 and 3, where more than one timebase can be specified. In Levels 0 and 1, all groups use timebase T1. When T2 is displayed in the TB column, it is shown in highlighted video (see callout 2 in Figure 3-10). POD labels for groups associated with T2 are also highlighted. *In all other menus where group names are displayed, group names associated with timebase T2 are highlighted.*

Valid CHAN entries are 0 - 8 and X (no channel assigned). Look in the UNUSED list at the bottom of the display for the channels in each pod that are not yet assigned to a group.

**Guidelines for Entering POD/CHAN Pairs.** A specific POD/CHAN pair can appear in only one group. If you enter a pair already assigned to another group, the logic analyzer deletes that channel from the original group.

The digits for a POD/CHAN pair are linked. When a POD or CHAN entry is changed, its companion digit changes to X. If you do not replace the X with digit that is valid, the pair is equivalent to  $\frac{X}{X}$ . When you enter a POD digit, the blinking field cursor moves to the CHAN digit below. Entering a CHAN digit moves the field cursor to the next POD field to the right (the cursor does not move if there are no more POD/CHAN pairs to the right).

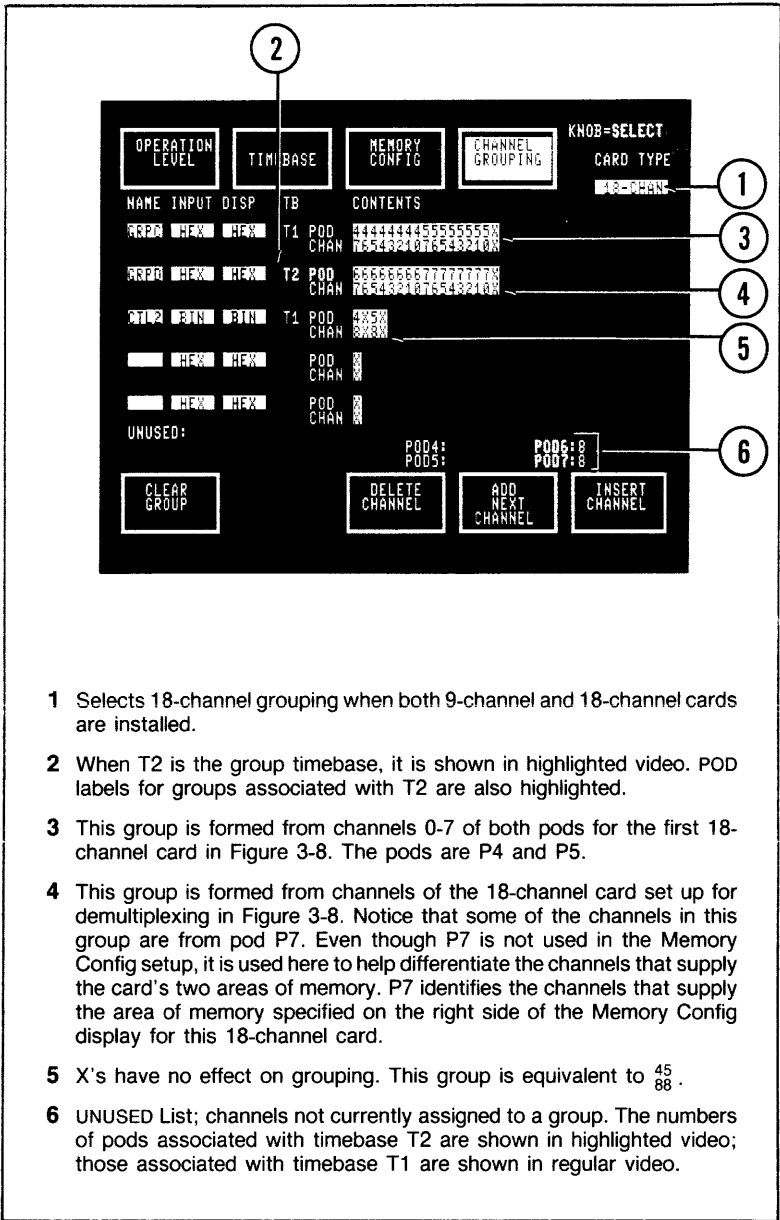
Each group has at least one POD/CHAN pair. If no specific digits are entered, the pair is blank,  $\frac{X}{X}$ . A blank POD/CHAN pair always occupies the rightmost position in a group unless the group has 36 channels (maximum). If you enter values in the rightmost pair, the logic analyzer adds to the right another  $\frac{X}{X}$  pair.

X's have no effect on grouping. For example:  $\frac{00X0XX00X}{87X65X420X}$  is equivalent to  $\frac{00000}{87620}$ .

**Table 3-4  
APPLYING THE DISPLAY RADIX TO ACQUIRED DATA**

Display Radix	# channels to form 1 displayed digit	Examples: different radices applied to a group of 13 channels
HEXadecimal	4	000 <sup>a</sup> +1 1001 0100 1011 = 194B
OCTal	3	00+1 100 101 001 011 = 14513
BINary	1	1100101001011 = 1100101001011
ASCII	8 (msb ignored)	000+11001 01001011 = EM K
EBCDIC	8	000+11001 01001011 = EM

<sup>a</sup> Implied leading zeros.



- 1 Selects 18-channel grouping when both 9-channel and 18-channel cards are installed.
- 2 When T2 is the group timebase, it is shown in highlighted video. POD labels for groups associated with T2 are also highlighted.
- 3 This group is formed from channels 0-7 of both pods for the first 18-channel card in Figure 3-8. The pods are P4 and P5.
- 4 This group is formed from channels of the 18-channel card set up for demultiplexing in Figure 3-8. Notice that some of the channels in this group are from pod P7. Even though P7 is not used in the Memory Config setup, it is used here to help differentiate the channels that supply the card's two areas of memory. P7 identifies the channels that supply the area of memory specified on the right side of the Memory Config display for this 18-channel card.
- 5 X's have no effect on grouping. This group is equivalent to  $\frac{45}{88}$ .
- 6 UNUSED List; channels not currently assigned to a group. The numbers of pods associated with timebase T2 are shown in highlighted video; those associated with timebase T1 are shown in regular video.

**Figure 3-10. Sample 18-channel grouping arrangement.** These default groups are based on the 18-channel portion of the Memory Config setup shown in Figure 3-8. In Figure 3-8, the second 18-channel card is set up for demultiplexing.

## BUILDING GROUPS

**CLEAR GROUP.** Touch this soft key to delete the group containing the blinking field cursor. All channels assigned to the deleted group appear in the UNUSED list at the bottom of the display. The remaining POD/CHAN pair is  $\frac{X}{X}$ . The TB (Timebase) field is cleared, but the NAME, INPUT, and DISP fields are unchanged. After you touch this soft key, the message PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT) is displayed at the top of the screen. The group is not deleted unless you press the X key on the front panel.

**DELETE CHANNEL.** Touch this soft key to delete the POD/CHAN pair at the location of the field cursor. If the pair specifies a channel, the deleted channel is added to the UNUSED list.

**ADD NEXT CHANNEL.** This soft key lets you quickly create groups with sequential CHAN values. ADD NEXT CHANNEL creates a new POD/CHAN pair to the right of the position of the field cursor. The new pair has the same POD value as the previous pair, but with the next lower CHAN value. For example: the field cursor is on 8 in the group  $\frac{4X}{8X}$ . Touch ADD NEXT CHANNEL twice to create  $\frac{444X}{876X}$ .

The cursor can also be positioned on an  $\frac{X}{X}$  pair immediately to the right of a valid POD/CHAN pair. You get the same results as described above if you position the field cursor on one of the X's in  $\frac{4X}{8X}$  and press the soft key twice.

Channels added with this method are deleted from other groups if necessary. No channels can be added with this soft key after a CHAN entry of 0.

**INSERT CHANNEL.** This soft key inserts a new POD/CHAN pair, initialized to  $\frac{X}{X}$ , immediately to the left of the field cursor. For example: the cursor is positioned on 2 in the group  $\frac{02X}{88X}$ . After you touch INSERT CHANNEL, the group appears as  $\frac{0X2X}{8X8X}$ .

## CHANNEL GROUPING DEFAULTS

The 1240 and 1241 Logic Analyzers create default 9- and 18-channel grouping arrangements from the current setup in the Memory Config menu. For 9-CHAN grouping, channels 0-7 from each pod assigned to a 9-channel card are placed in a separate group. Channel 8 from each of these pods is placed in a group named CTL1. Figure 3-9 shows this arrangement.

For 18-CHAN grouping, channels 0-7 from both pods assigned to an 18-channel card are placed in a separate group (a group like this has 16 channels). Channel 8 from each of these pods is placed in a group named CTL2.

For both 9-CHAN and 18-CHAN grouping, channels from the lowest-numbered pod make up the first group.

There is a maximum of six default groups, named GRPA, GRPB, GRPC, GRPD, CLT1, and CTL2. The methods used to create CTL1 and CTL2 are described above. How groups GRPA-GRPD are assigned can be best explained with examples. Example 1: For an instrument equipped with one 9-channel and one 18-channel card, GRPA will be the name assigned to the first group in 9-CHAN grouping. The only other group in 9-CHAN is CTL1. In 18-CHAN grouping, the first group will be named GRPB, and the remaining group will be CTL2. Example 2: In an instrument with four 18-channel cards, the first 18-CHAN group is named GRPA, and the next three groups are GRPB, GRPC, then GRPD. GRPA is made up of channels 0-7 from pods P0 and P1. Similarly, groups GRPB - GRPD have channels 0-7 from pods P2 and P3, P4 and P5, and P6 and P7. The last group is CTL2. In this case there is no 9-channel grouping because no 9-channel cards are installed.

Input and display radices for all groups *except* CTL1 and CTL2 are HEX. Input and display radices for CTL1 and CTL2 are BIN.

## DEMULTIPLEXING

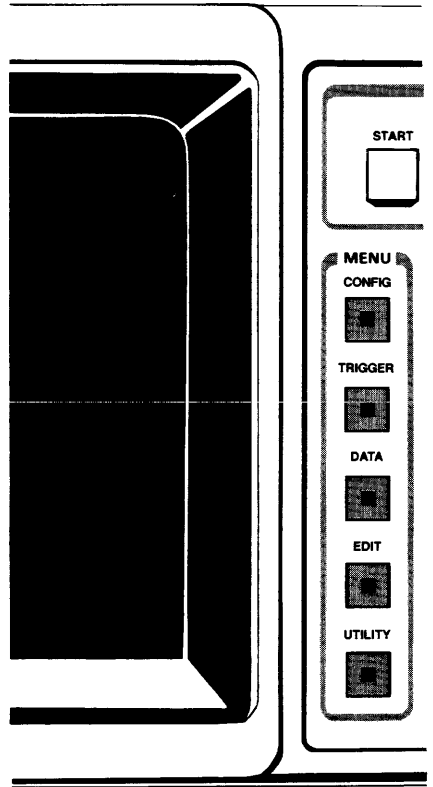
As you read these paragraphs, refer to Figure 3-8, callout 3, and Figure 3-10, callout 4.

When you use an 18-channel card for demultiplexing, you need to connect only one probe (pod) to the data source. This probe always has an even-numbered pod ID (see Figure 3-8). The 1240 and 1241 Logic Analyzers store data acquired with this probe in the 18-channel card's two areas of memory.

In the 18-channel grouping setup, the logic analyzer must be able to refer to the same probe channels in two different ways: one method identifies data in the first area of memory, and the other method identifies data in the second area of memory. Since the even-numbered pod ID can be used for only one method, another pod ID must be used to identify data in the other area of memory. The 1240 and 1241 logic Analyzers solve this problem by using the even-numbered pod ID to identify data in the first area of memory (left side of the Memory Config display); the card's odd-numbered pod ID identifies data in the area of memory on the right side of the Memory Config display. Refer to Figure 3-10, callout 4, for an example. (The odd-numbered pod ID is for labeling purposes only; that pod is not involved in demultiplexing and does not have to be connected to the instrument.)

Pod IDs 6 and 7 are shown in the same group in Figure 3-10 because this demultiplexing setup uses timebases T2 F and T2 L. The Channel Grouping menu does not differentiate between T2 F and T2 L; both are labeled T2. If you demultiplex with T1 and T2, the pod IDs must be in different groups because they are associated with different timebases. (Remember that each channel in a given group must use the same timebase.)

4



TRIGGER

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The TRIGGER key on the front panel allows you to access the Trigger Spec(ification) and the Auto-Run Spec(ification) menus. These menus allow you to define the triggering characteristics of the logic analyzer.

## TRIGGER SPEC

This menu allows you to specify the event or sequence of events that causes the 1240 or 1241 Logic Analyzer to trigger. An "event" is the set of 1's and 0's received by the instrument on a cycle of the timebase.<sup>1</sup> The logic analyzer compares each event to the specifications entered in this menu. When there is a match, the event is "recognized."

Two separate event recognizers are available in this menu: the global event recognizer and the sequential event recognizer. The event recognizers can operate simultaneously or either one can be disabled. When they are used together, the trigger setup is a logic OR condition: either event recognizer can generate the trigger. A RESET command in either event recognizer re-starts the trigger search in both sections.

The global event recognizer specifies a single event. It is called "global" because you can specify an event using all connected channels (regardless of the timebase they are associated with), and because this event is in effect during the entire acquisition. Refer to *Global Event Recognizer* later in this section for more information.

The sequential event recognizer is composed of up to 14 "sequence levels," where each level specifies an event. When the condition specified in a level is recognized, the logic analyzer either advances to the next level, jumps to a specified level, triggers, or resets. If the last level is reached and satisfied, the final action in the sequence (**TRIGGER**, **RESET**, **DO NOTHING**) is executed. Each level can be associated with only one timebase. Refer to *Sequential Event Recognizer* later in this section for more information.

### NOTE

*Only one trigger is executed, even if both event recognizers are in use and/or two timebases are active.*

## TRIGGER POSITION

The TRIGGER POSITION field allows you to position the trigger in acquisition memory (see Table 4-1 and callout 1 in Figure 4-1). Data stored before the trigger is called pre-trigger data; data after the trigger is post-trigger data.

Memory depth varies with the number of acquisition cards installed, the operation level in effect, the use of memory chaining, and glitch storage enabled or disabled. Table 4-1 lists the number of post-trigger acquisition cycles for all trigger positions and memory depths.

The LOOK FOR TRIGGER field (callout 2 in Figure 4-2) determines when the logic analyzer will accept a trigger. Selections are **AFTER MEMORY FULL** and **IMMEDIATELY**. If you choose **AFTER MEMORY FULL**, the logic analyzer accepts a trigger only after the required amount of pre-trigger data is acquired.

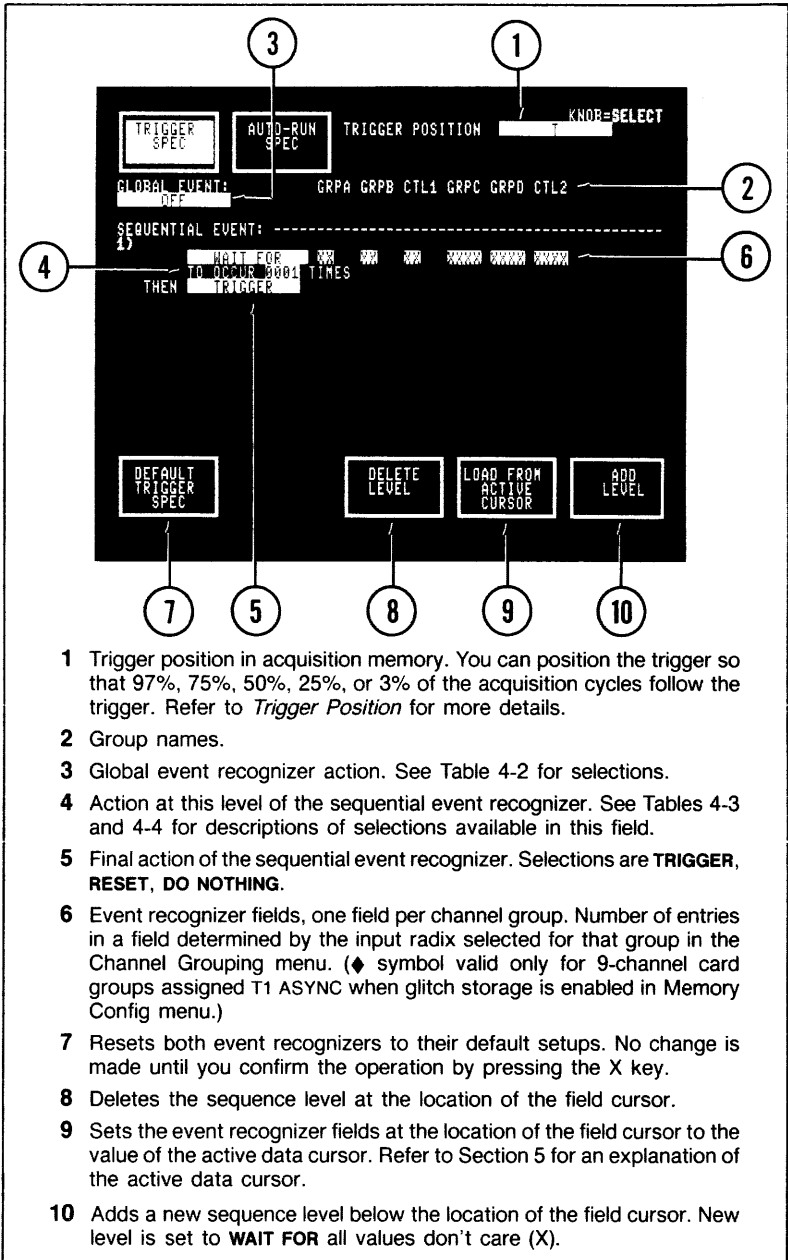
If the trigger event is found before the pre-trigger requirement is satisfied, the trigger search is reset. When enough pre-trigger data has been acquired, the logic analyzer accepts the next trigger event and marks it as the trigger in the data display.

---

<sup>1</sup> The timebase period is specified in the Timebase menu. The CARD THRESHOLD and POLARITY fields in the Memory Config menu determine if an incoming signal is a 1 or a 0.

If you select GLOBAL EVENT = **UNLOCKED** in the Timebase menu, the global event recognizer can recognize any event that is present for the amount of time defined by the global event filter period. The event does not have to coincide with a sample point. See *Global Event Recognizer* later in this section for details.





- 1 Trigger position in acquisition memory. You can position the trigger so that 97%, 75%, 50%, 25%, or 3% of the acquisition cycles follow the trigger. Refer to *Trigger Position* for more details.
- 2 Group names.
- 3 Global event recognizer action. See Table 4-2 for selections.
- 4 Action at this level of the sequential event recognizer. See Tables 4-3 and 4-4 for descriptions of selections available in this field.
- 5 Final action of the sequential event recognizer. Selections are **TRIGGER**, **RESET**, **DO NOTHING**.
- 6 Event recognizer fields, one field per channel group. Number of entries in a field determined by the input radix selected for that group in the Channel Grouping menu. (♦ symbol valid only for 9-channel card groups assigned T1 ASYNC when glitch storage is enabled in Memory Config menu.)
- 7 Resets both event recognizers to their default setups. No change is made until you confirm the operation by pressing the X key.
- 8 Deletes the sequence level at the location of the field cursor.
- 9 Sets the event recognizer fields at the location of the field cursor to the value of the active data cursor. Refer to Section 5 for an explanation of the active data cursor.
- 10 Adds a new sequence level below the location of the field cursor. New level is set to **WAIT FOR** all values don't care (X).

4340-32

**Figure 4-1. Power-up default Trigger Spec menu display.** The global event recognizer is disabled, and the sequential event recognizer is set to trigger on the first event that occurs after the required amount of pre-trigger data is acquired (see *Trigger Position* for pre-trigger details).

When you select **IMMEDIATELY**, the trigger is enabled for the first event sampled; pre-trigger data acquisition is not required. (If you select **IMMEDIATELY** and the first event sampled meets the trigger conditions, the acquisition memory reserved for pre-trigger data will be empty.)

The LOOK FOR TRIGGER field is not displayed in Operation Level 0, but the **AFTER MEMORY FULL** selection is in effect.

Table 4-1  
TRIGGER POSITIONS BASED ON MEMORY SIZE

Menu Selections	Number of cycles from TRIG to end of memory for different memory depths					
	Memory Depths: <sup>a</sup>					
	257	513	769	1025	1537	2049
[ T ]	241	497	737	993	1489	1985
[ T ]	193	385	577	769	1153	1537
[ T ]	129	257	385	513	769	1025
[ T ]	65	129	193	257	385	513
[ T ]	17	17	33	33	49	65

<sup>a</sup> Memory depth is not selectable in Operation Level 0. The standard fixed depth is 513 cycles; 257 is the depth for 9-channel cards when glitch storage is enabled.

## EXTERNAL TRIGGER OUT

The 1240 and 1241 Logic Analyzers supply a signal to the EXT TRIG OUT BNC on the back panel whenever the trigger event is found.

In most Auto-Run conditions, you can select the EXT TRIG OUT signal to be PULSED or LATCHED (see *Auto-Run Spec* later in this section). If you are not using Auto-Run and taking only single acquisitions, the signal is always pulsed (high for at least 80 ns).

The screenshot shows a terminal display for a trigger specification. At the top, there are buttons for 'TRIGGER SPEC' and 'AUTO-RUN SPEC'. The 'TRIGGER POSITION' is set to 'KNOR=SELECT'. Below this, the 'LOOK FOR TRIGGER:' field is set to 'AFTER MEMORY FULL'. The 'GLOBAL EVENT:' section shows 'TRIGGER' set to 'ON' and various channel names (GRP A, GRP B, CTL1, GRPC, GRPD, CTL2) with their respective filter settings. The 'SEQUENTIAL EVENT:' section lists five levels (1) through (5). Each level has a sequence of events (e.g., '1) OR', '2) THEN', '3) THEN', '4) ELSE', '5) ELSE') with associated filter settings and storage options. Callout 1 points to the 'TRIGGER' field. Callout 2 points to the 'LOOK FOR TRIGGER:' field. Callout 3 points to the '1) OR' event. Callout 4 points to the '4) ELSE' event. Callout 5 points to the 'DELETE LEVEL' button at the bottom.

- Group names. Names associated with T2 are highlighted.
- When trigger will be accepted. Selections are **AFTER MEMORY FULL** (trigger accepted only after required amount of pre-trigger data is acquired) and **IMMEDIATELY**.
- Sequence level timebase assignment; selections T1 and T2. A sequence level can be associated with only one timebase. When T1 and T2 are active, this field is displayed for each level. The selection determines which groups are displayed in the event value fields. For example: in level 1 in this display, only groups associated with T1 are displayed; in level 2, only groups associated with T2 are displayed.
- Symbol for truncated data. Event recognizer fields are truncated to the left and/or right when all channels cannot be shown on the display. Use the left/right cursor keys to move truncated data onto the screen.
- \$ indicates that the input radix was changed and the original value of the digit was a mix of numbers, X's, or ♦'s that cannot be displayed cleanly in the new radix.

4340-33

**Figure 4-2. Two-timebase Trigger Spec display.** The global event recognizer can search for an event that combines data from both timebases. Each level in the sequential event recognizer is associated with one timebase (T1 or T2); therefore, only groups associated with the selected timebase are displayed in the event value fields. A sequence can be up to 14 levels deep but not all levels can be displayed on the screen at one time. Use the cursor keys to move to undisplayed levels.

## GLOBAL EVENT RECOGNIZER

**Overview.** The global event recognizer specifies a single event. This event can specify channels from one or both timebases. Table 4-2 describes the action selections available in the global event recognizer, plus associated fields. Figures 4-1 and 4-2 show different global event setups.

The global event can be inverted with an **ON NOT** selection (see Table 4-2). With **ON NOT**, the global event action is performed when any value other than the specified value is recognized. The global event statement **TRIGGER IF NOT A** actually means **TRIGGER IF (anything but A)**. For example, a global event recognizer set to **TRIGGER ON NOT AA** would trigger when it recognized any value other than AA.

Glitch requirements are *not* inverted when you select **ON NOT**. For example, if the global event is **TRIGGER ON NOT F♦**, a trigger will occur when any value other than F is recognized on the first set of four channels and a glitch occurs on at least one channel in the second set of four channels. For the global event **TRIGGER ON ♦♦♦♦**, a trigger will occur when a glitch is recognized on at least one channel in the total set of channels.

### NOTE

*ON NOT XXXX (event value of all don't cares) specifies an event that will never occur.*

**Filter.** The global event recognizer does not recognize an event unless the event is present for the amount of time defined by the global event filter. An event is accepted if it is present for an amount of time  $\geq N \times T$ , where N is the value in the FILTER field and T is the value in the ON field. Detailed filter specifications are included in Table 8-5 in Section 8.

Selections in the FILTER field are **1-16**; selections in the ON field are **T1** (when timebase T1 is active), **T2** (when timebase T2 is active), and **10NS**. The **10NS** selection is usually used with the GLOBAL EVENT = **UNCLOCKED** selection (see *Clocked/Unlocked*, next) to monitor input events independent of the sample clock.

Use the filter to reject events below a certain duration. For example: **FILTER 9 ON T1** (T1 set to 50 ns) rejects any event less than 450 ns in duration.

How the logic analyzer applies the filter to data depends on whether edge or level event recognition is in effect. See *Edge vs. Level Event Recognition* later in this section for details.

### NOTE

*A NOT action negates the value of the Global Event (looks for anything but the specified value) before it is applied to the filter. For example, START TIMER ON NOT A, FILTER: 05 means that any combination of 5 consecutive values other than A will start the timer. If any of the 5 values is A, the search continues for 5 consecutive values that are not A.*

**Clocked/Unlocked.** The GLOBAL EVENT = **CLOCKED/UNCLOCKED** field in the Timebase menu (see Figure 3-2) determines when events are compared to the global event recognizer. The **CLOCKED** selection means that only events that coincide with sample points are compared to the global event recognizer. When you choose **UNCLOCKED**, data from the system under test is continuously compared to the global event recognizer. The global event can be satisfied by any event that meets the global event filter (see *Filter*, previous).

**Table 4-2**  
**GLOBAL EVENT RECOGNIZER ACTIONS AND ASSOCIATED FIELDS**

Action Selections	Associated Fields
<b>OFF</b> — global event recognizer disabled.	None.
<b>TRIGGER</b> — trigger when global event is true.	<p><b>ON/ON NOT</b> — event is true when the sampled data equals/does not equal the event value</p> <p>Event Value <sup>a</sup> — entered by channel group in the input radix specified in the Channel Grouping menu.</p> <p><b>FILTER:</b> — number of timebase periods the global event must be true before it can be recognized. Selections are 1-16. Displayed only if Operation Level is 1 or 3.</p> <p><b>ON</b> — timebase for <b>FILTER</b> field. Selections are <b>10NS</b> or <b>T1</b> (when timebaseT1 active), <b>T2</b> (when timebase T2 active).</p>
<b>RESET</b> — re-start trigger search in both event recognizers when global event is true.	<b>ON/ON NOT</b> , Event Value, <b>FILTER: ON</b> (described above)
<b>STORE</b> — allow data storage only while global event is true.	<b>ON/ON NOT</b> , Event Value (described above)
<p><b>START TIMER</b> <sup>b</sup> — timer starts when global event is true; stops when logic analyzer triggers, or you press <b>STOP</b>. Timer value is displayed in appropriate units at the top of the data display.</p> <p><b>TIME WHILE</b> <sup>b</sup> — timer starts when global event is true; stops when event is false. Timer continues if event comes true again. Final value is cumulative time the event was true before LA triggered, or you pressed <b>STOP</b>.</p>	<p><b>ON/ON NOT</b>, Event Value, <b>FILTER: ON</b> (described above)</p> <p><b>TRIGGER, RESET</b> — final action taken when termination value for timer is reached (see <b>IF TIMER</b> description below).</p> <p><b>DO NOTHING</b> — no action taken based on timer value.</p> <p><b>IF TIMER =</b> — termination value for timer. Perform action (<b>TRIGGER, RESET</b>) if this value is reached. Numeric field; range is 10 ns to 999,999,999,990 ns (about 17 minutes).</p>
<b>INCR CNTR</b> <sup>b</sup> — counter increments once every time global event is true. Counter runs until logic analyzer triggers, or you press <b>STOP</b> . Final counter value is shown as number of events at top of data display.	<p><b>ON/ON NOT</b>, Event Value, <b>FILTER: ON</b> (described above)</p> <p><b>TRIGGER, RESET</b> — final action taken when termination value for event counter is reached (see <b>IF COUNT</b> description below).</p> <p><b>DO NOTHING</b> — no action taken based on counter value.</p> <p><b>IF COUNT =</b> — termination value for counter. Perform action (<b>TRIGGER, RESET</b>) if this value is reached. Numeric field; range is 1 to 99,999,999,999 events.</p>

<sup>a</sup> The glitch symbol (◆) is a valid entry only for 9-channel card groups assigned T1 ASYNC when glitch storage is enabled in Memory Config menu and the global event recognizer is CLOCKED.

<sup>b</sup> When a reset occurs, the counter/timer functions return to 0 then continue. The accumulated count or time is lost.

**Table 4-3**  
**SEQUENTIAL EVENT RECOGNIZER ACTIONS AND ASSOCIATED FIELDS**

Action Selections	Associated Fields
<p><b>WAIT FOR, WAIT FOR NOT</b> — stay in current sequence level until the defined event is/is not true, then advance to the next level.</p>	<p>Timebase <sup>a</sup> — selections are T1 and T2. Selection determines which groups are displayed in the event value fields.</p> <p>Event Value <sup>b</sup> — entered by channel group in the input radix specified in the Channel Grouping menu.</p> <p>TO OCCUR <b>nnnn</b> TIMES — value <b>nnnn</b> specifies how many times the event must be true before the logic analyzer advances to next sequence level. Range is 1 - 9999 events.</p> <p>FILTER — number of timebase periods an event must be true before it can be recognized. Selections are 1-16. Displayed only if Operation Level is 1 or 3.</p> <p>WITH STORAGE — storage qualification. Selections are <b>ON</b> and <b>OFF</b>. With ON, data is stored while the sequence level is in effect. Displayed only in Operation Levels 2 or 3. Not displayed if timebase is T1 ONLY, ASYNC 10NS.</p>
<p><b>TRIGGER IF, TRIG IF NOT</b> — trigger if data from current acquisition cycle satisfies/does not satisfy the defined event; otherwise, advance to the next level.</p>	<p>Timebase, Event Value, FILTER, WITH STORAGE (described above)</p>
<p><b>RESET IF, RESET IF NOT</b> — restart both event recognizers (and set counter/timer to 0) if data from current acquisition cycle satisfies/does not satisfy defined event; otherwise, advance to next level.</p>	<p>Timebase, Event Value, FILTER, WITH STORAGE (described above)</p>
<p><b>JUMP IF, JUMP IF NOT</b> — jump to level specified in TO LEVEL field if data from the current acquisition cycle satisfies/does not satisfy the defined event; otherwise, advance to the next level.</p>	<p>Timebase, Event Value, FILTER, WITH STORAGE (described above)</p> <p>TO LEVEL: — jump to this level when jump action is performed. Selections are 1-E. A jump to an undefined level causes a trigger.</p>
<p><b>DELAY</b> — delay specified number of timebase periods, then advance to the next level.</p>	<p>Timebase, WITH STORAGE (described above)</p> <p><b>nnnn</b> CLOCKS — number of timebase periods to delay. Range is 1-9999.</p>
<p><b>TRIGGER, RESET, DO NOTHING</b> — final action of the sequential event recognizer.</p>	<p>WITH STORAGE (described above) — displayed when DO NOTHING is the final action.</p>

<sup>a</sup> Displayed for every level when T1 and T2 are active. Two-timebase operation is available only in Operation Levels 2 and 3.

<sup>b</sup> The glitch symbol (◆) is valid only for 9-channel card groups assigned T1 ASYNC when glitch storage is enabled in Memory Config menu and the global event recognizer is CLOCKED.

**Counter/Timer.** The counter/timer functions (INCR CNTR, START TIMER, and TIME WHILE) only count or time events that satisfy the global filter requirements and match the global event value (global event true). The final value is displayed in appropriate units in the top, right corner of the data display (see Figures 5-1 and 5-5 for examples).

INCR CNTR increments the counter by one every time the global event is true. The count stops when the logic analyzer triggers or you press STOP.

START TIMER starts the timer at the first occurrence of the global event. The timer runs until the logic analyzer triggers or you press STOP.

TIME WHILE times how long the global event was true from the start of the trigger search until the logic analyzer triggers or you press STOP. TIME WHILE starts the timer each time the global event is true and stops it when the event is false. The final value is the cumulative time the global event was true.

The counter/timer returns to zero, then restarts, whenever a RESET command occurs in the sequential event recognizer. It is also reset if the trigger event is found but the pre-trigger requirement has not been met (refer to *Trigger Position*, previous).

**Storage Qualification.** The STORE selection provides storage qualification for the global event recognizer. Storage (data) qualification makes the most of available acquisition memory space by storing only the events you are interested in.

When you select **STORE ON**, an event is stored in memory only if it satisfies the global filter and matches the global event value. If you select **STORE ON NOT**, an event is stored only if it satisfies the global filter and is *different* from the global event value.

If timebase T1 is ASYNC 10 NS, STORE has no effect on storage of T1 data — all T1 data is stored. Even though there is no T1 storage qualification under these timebase conditions, you can use the T1 channel values to help determine storage qualification for T2 data.

#### NOTE

*Remember that when the event recognizers are used together, they are OR'd. Data is stored if the STORE action is true in the global event recognizer, or if a level with storage ON is in effect in the sequential event recognizer.*

## SEQUENTIAL EVENT RECOGNIZER

**Overview.** The sequential event recognizer can have up to 14 levels, numbered 1 - E. The actions available at each level and their associated fields are summarized in Table 4-3.

Except for **WAIT FOR**, **WAIT FOR NOT**, and **DELAY**, all sequence actions are in effect for one acquisition cycle.<sup>2</sup> If the event specified on the level is satisfied during that cycle, the action is performed. If not, control advances to the next level. Table 4-4 summarizes the transfer of control from level to level of the sequential event recognizer.

Each level can be associated with only one timebase. When timebases T1 and T2 are active,<sup>3</sup> a select field is displayed at each level so you can specify which timebase applies. Only channel groups associated with the selected timebase are displayed in the event field. Refer to Figure 4-2; notice that at each level, the event value is composed only of groups that use the selected timebase, and the spaces for the other groups are blank.

<sup>2</sup> This assumes a FILTER value of 1. If the FILTER value is greater than 1, the sequence action could be in effect for more than one cycle.

<sup>3</sup> T2 can be specified only in Operation Levels 2 and 3.

## NOTE

*The entire event value will be blank if you select a timebase that has no pods assigned in the Memory Config menu. All blanks is the same as an event value of all don't cares. Since any data value will satisfy this event value, the sequence action is performed when a clock signal for that timebase is received during that level of the sequence. For example: if a sequence level is T1 WAIT FOR (all groups blank) THEN TRIGGER, the logic analyzer will trigger when the first T1 clock occurs after the sequence reaches this level.*

Each sequential event action, except **DELAY**, can be inverted with a NOT action (**WAIT FOR NOT**, **JUMP IF NOT**, etc.; see Tables 4-3 and 4-4). With a NOT action, the sequence action is performed when any value other than the specified value is recognized. The sequential event statement **JUMP IF NOT A** actually means **JUMP IF (anything but A)**. For example, a sequential event recognizer set to **JUMP IF NOT AA** would cause a jump from this level when any value other than AA was recognized.

Glitch requirements are *not* inverted when you select a NOT action. For example, if the sequential event is **RESET IF NOT 5♦**, the reset action will be performed when any value other than 5 (hex, in this example) is recognized on the first set of four channels and a glitch occurs on at least one channel in the second set of four channels. For the sequential event **RESET IF ♦♦♦♦**, the reset action will be performed when a glitch is recognized on at least one channel in the total set of channels.

## NOTE

*A NOT action negates the value of the Sequential Event (looks for anything but the specified value) before it is applied to the filter. A NOT action with an event value of all don't cares (X) specifies an event that will never occur.*

**Filter.** The sequential event recognizer does not recognize an event unless the event is present for the amount of time defined by the filter for that sequence level. An event is accepted if it is present for an amount of time  $\geq N \times T$ , where N is the value in the FILTER field and T is the value in the ON field. Detailed filter specifications are included in Table 8-5 in Section 8.

How the logic analyzer applies the filter to data depends on whether edge or level event recognition is in effect. See *Edge vs. Level Event Recognition*, following, for details.

## NOTE

*A NOT action negates the value of the Sequential Event (looks for anything but the specified value) before it is applied to the filter. For example, JUMP IF NOT A, FILTER: 05 means that any combination of 5 consecutive values other than A will cause a jump action. If any of the 5 values is A, the jump is not performed.*

**Storage Qualification.** In Operation Levels 2 and 3, the WITH STORAGE field is displayed in each level of the sequential event recognizer. (It is also displayed when DO NOTHING is the final sequence action.) Selections are **ON** and **OFF**. If you select ON, the logic analyzer stores data in memory while that level of the sequence is in effect. If you select OFF, data is *not stored* while that level is in effect.



For example: you want to store only the instructions in a specific subroutine. The subroutine starts with AAAA and ends with FFFF. The first sequence level is WAIT FOR AAAA, WITH STORAGE OFF. The next sequence level is WAIT FOR FFFF, WITH STORAGE ON, THEN TRIGGER. No data is stored while waiting for AAAA to occur. When AAAA does occur, the sequential event recognizer moves to the next sequence level. Data is stored while waiting for FFFF; when FFFF occurs, the logic analyzer triggers. A reset is generated every time an event is found that matches the trigger condition. Therefore, the sequential event recognizer restarts at level 1 when the logic analyzer triggers. Level 1 turns storage OFF; no other data besides the subroutine is stored.

The WITH STORAGE field is not displayed if the active timebase is T1 ONLY, ASYNC 10 NS.

**NOTE**

*The trigger search is restarted in both event recognizers whenever: 1) a RESET command is executed in either event recognizer, or 2) the logic analyzer finds an event that matches the trigger condition.*

Whenever a reset or trigger occurs, the sequential event recognizer restarts at level 1. Keep this in mind when you use storage qualification; restarting the trigger search could change your qualification scheme. For example: refer to the subroutine example above. Suppose a reset occurs in the global event recognizer while the logic analyzer is waiting for FFFF (storage is ON). The sequential event recognizer immediately restarts at level 1, and storage is turned OFF. The rest of the subroutine is not stored. Data storage will start again only if AAAA reoccurs.

**NOTE**

*Remember that when the event recognizers are used together, they are OR'd. Data is stored if the STORE action is true in the global event recognizer, or if a level with storage ON is in effect in the sequential event recognizer.*

**Table 4-4  
SUMMARY OF SEQUENTIAL EVENT RECOGNIZER ACTIONS**

<b>Action</b>	<b>Event Found this Acquisition Cycle</b>	<b>Event Not Found this Acquisition Cycle</b>
WAIT FOR WAIT FOR NOT	advance to next level do nothing	do nothing advance to next level
TRIGGER IF TRIG IF NOT	trigger advance to next level	advance to next level trigger
RESET IF RESET IF NOT	reset advance to next level	advance to next level reset
JUMP IF JUMP IF NOT	jump advance to next level	advance to next level jump
DELAY (not event oriented)	n/a	n/a

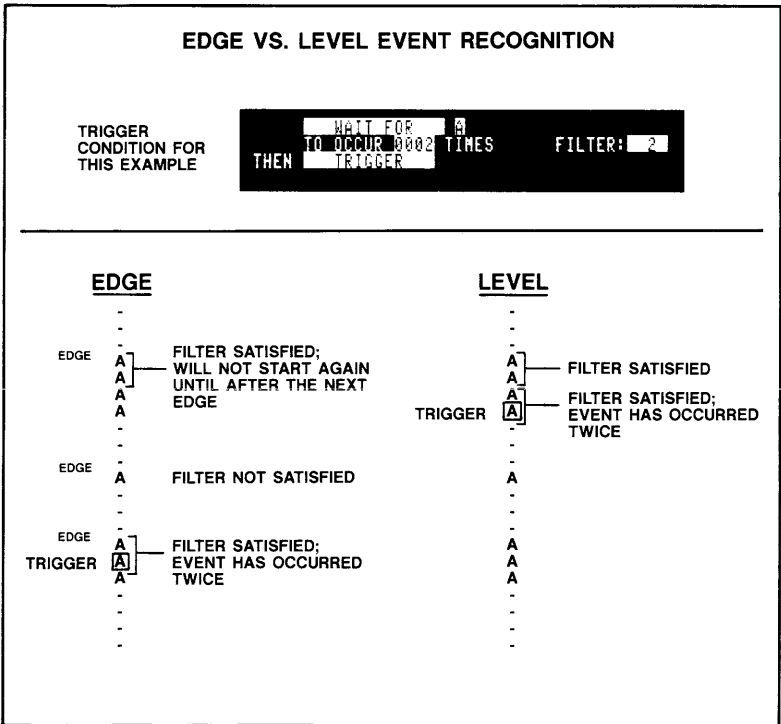
### EDGE vs. LEVEL EVENT RECOGNITION

Global and sequential event recognizer actions (except **STORE** and **DELAY**) are not performed unless the specified event satisfies the filter conditions. How the filter is applied depends on whether edge or level event recognition is in effect.

Figure 4-3 illustrates the difference between the two types of event recognition. Most Trigger Spec setup conditions support level event recognition. The setup conditions that determine edge event recognition are listed in Table 4-5.

**Level.** Level event recognition is based on the state of the inputs at the clock edge. When the valid event occurs, the filter counts the required number of successive cycles the event is present. If the filter is satisfied, the event is recognized and the filter resets and starts over. If the filter is not satisfied and the event becomes invalid, the filter resets and waits for the event to occur again.

Level event recognition is always in effect if the event value is all don't cares (Xs) or if the timebase (for global events, the FILTER timebase) is synchronous.



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**Figure 4-3. Difference between edge and level event recognition.** In edge event recognition, the filter is applied only after a transition occurs from event invalid to event valid. Level recognition is based on the state of the inputs at the sample point.

**Edge.** In edge event recognition, the filter is applied after the word recognizer indicates that the data has made the transition to the state specified in the event value fields. In Figure 4-3, data transitions that satisfy the word recognizer are marked with the word "edge." If the filter is satisfied, the specified event is recognized as having occurred once. If the trigger condition requires that the event be recognized more than once, the filter is reset but not applied until another transition occurs from an event invalid condition to event valid.

Three conditions cause the word recognizer to indicate that a data transition has occurred:

- a data transition satisfies the word recognizer, or
- an acquisition is started while input data satisfies a word recognizer, or
- a change is made from a sequential event level in which the sequential word recognizer is not satisfied to a level in which the word recognizer is satisfied.

The last two conditions would cause the logic analyzer to incorrectly perceive a data transition unless the sequential event recognizer was set to first WAIT FOR NOT (Event) TO OCCUR 1 TIME, then WAIT FOR (Event) TO OCCUR (N) TIMES. This setup assures that the logic analyzer recognizes only valid data transitions.

Refer to Table 4-5 for a list of the setup conditions that determine edge event recognition. Unless these conditions are met, level event recognition is in effect.

**Table 4-5**  
**CONDITIONS THAT DETERMINE EDGE EVENT RECOGNITION <sup>a</sup>**

Event Recognizer	Conditions
GLOBAL	FILTER timebase is 10 NS and Event value is <b>not</b> all X
	FILTER timebase is T1 and T1 is ASYNC and Event value is <b>not</b> all X
SEQUENTIAL	Sequence level timebase is T1 and T1 is ASYNC and Sequence level event value is <b>not</b> all X

<sup>a</sup> Level event recognition is in effect if these conditions are not met.

## BUILDING A SEQUENCE

The soft keys at the bottom of the menu allow you to build a sequence of levels in the sequential event recognizer, return to the default trigger setup, or quickly copy an event value from memory.

**DEFAULT TRIGGER SPEC.** Touch this soft key to return both event recognizers to their default setups. After you touch this key, the following confirmation message is displayed on the top line of the screen: PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT). Press the X key to confirm the return to default; press any other key on the front panel to cancel the operation.

**DELETE LEVEL.** Touch this soft key to delete the sequence level at the location of the blinking field cursor. If there is only one level, touching this soft key completely deletes the sequential event recognizer.

**LOAD FROM ACTIVE CURSOR.** This soft key is valid only if the field cursor is positioned in an event field. When you touch this soft key, the event at the location of the field cursor is loaded with the same data as the location in active memory where the active data cursor is positioned. Active memory is the type of memory (acquisition or reference memory) last displayed. Refer to Section 5 for a description of the active data cursor.

Recall from the *Channel Grouping* description in Section 3 that displayed data and event recognizer input data can have different radices. If the display radix is different from the input radix, the data at the active cursor is converted to the input radix. The radix is changed, not the value of the data.

**ADD LEVEL.** Touch this soft key to add a new sequence level below the location of the field cursor. The new sequence level is initialized to the default values (WAIT FOR, all don't cares).

## STARTING THE TRIGGER SEARCH & EVALUATING STATUS DISPLAYS

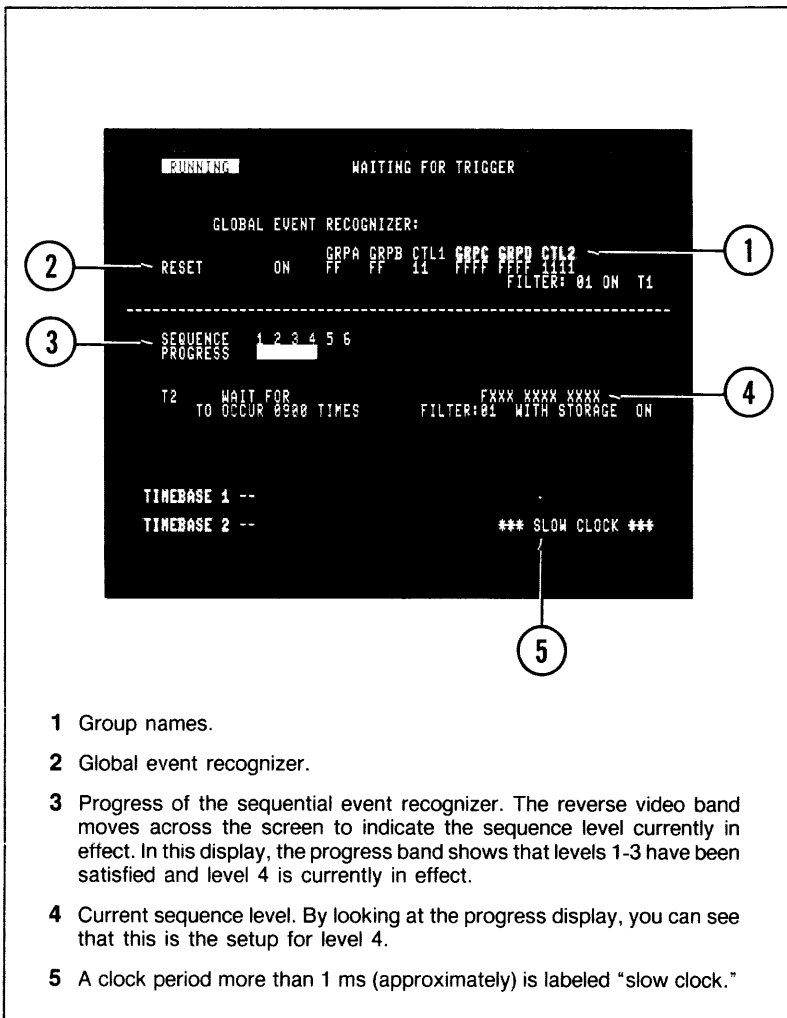
Press the START key on the front panel to begin the search for the trigger condition specified in the Trigger Spec menu.

After you press START, the 1240 and 1241 Logic Analyzers display information on the status of the trigger search (WAITING FOR TRIGGER status display, see Figure 4-4). This status information is updated until a trigger is found or you press the STOP key.

The TRIGGERED status display (see Figure 4-5) is shown after the trigger occurs or after you press STOP. This display stays on the screen until all remaining locations in acquisition memory are filled.

When memory is filled, the top line of the screen changes to PROCESSING DATA. This display remains on the screen while the logic analyzer formats the acquired data for display. When processing is complete, the acquired data is displayed in State Table or Timing Diagram format, whichever was last used.

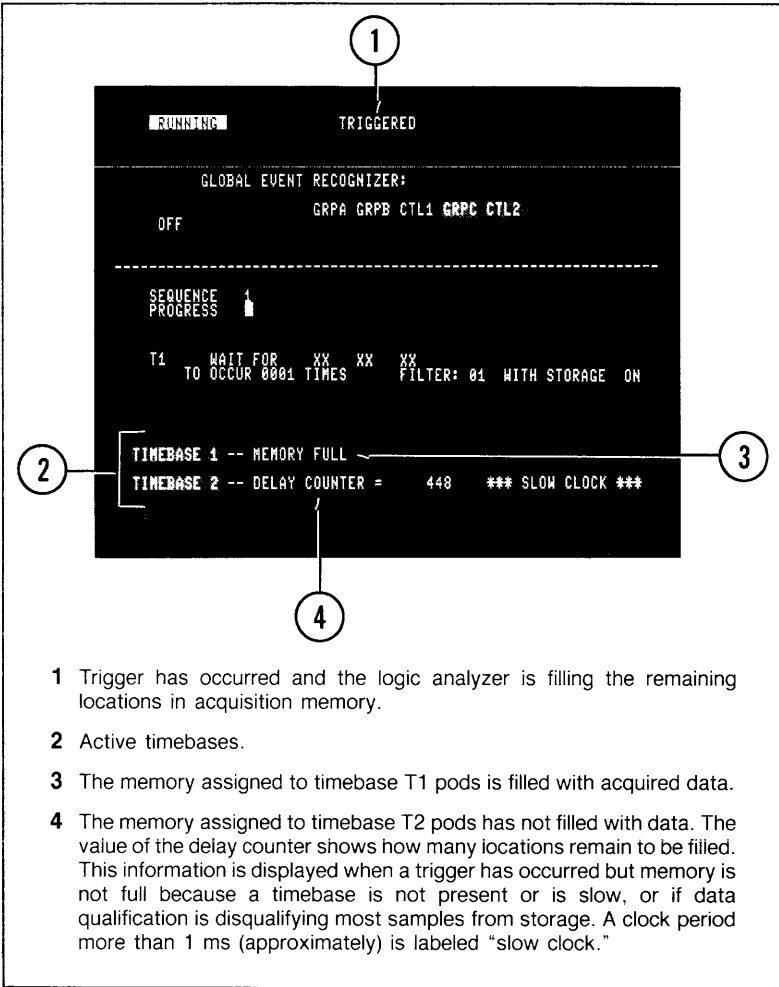
The status displays have no changeable fields. They are informational fields only.



- 1 Group names.
- 2 Global event recognizer.
- 3 Progress of the sequential event recognizer. The reverse video band moves across the screen to indicate the sequence level currently in effect. In this display, the progress band shows that levels 1-3 have been satisfied and level 4 is currently in effect.
- 4 Current sequence level. By looking at the progress display, you can see that this is the setup for level 4.
- 5 A clock period more than 1 ms (approximately) is labeled "slow clock."

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**Figure 4-4. WAITING FOR TRIGGER status display.** After you press the START key on the front panel, the 1240 displays information on the status of data acquisition.



- 1 Trigger has occurred and the logic analyzer is filling the remaining locations in acquisition memory.
- 2 Active timebases.
- 3 The memory assigned to timebase T1 pods is filled with acquired data.
- 4 The memory assigned to timebase T2 pods has not filled with data. The value of the delay counter shows how many locations remain to be filled. This information is displayed when a trigger has occurred but memory is not full because a timebase is not present or is slow, or if data qualification is disqualifying most samples from storage. A clock period more than 1 ms (approximately) is labeled "slow clock."

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**Figure 4-5. TRIGGERED status display.** This display is shown after the trigger has been found and while the logic analyzer is filling the remaining locations in acquisition memory. Without a slow clock, memory is filled too rapidly for this display to be read. When memory is filled, the top line of the screen changes to PROCESSING DATA.

## AUTO-RUN SPEC

This menu lets you set up the 1240 or 1241 Logic Analyzer to make repeated data acquisitions without manual starts. The specifications in this menu are used only if the data acquisition process is started with the AUTO key on the front panel.

The four Auto-Run conditions are: **COMPARE ACQMEM TO REFMEM**, **CONTINUOUS TRIGGER OUT**, **TRIGGER IN**, and **STORE AFTER TRIGGER**. Figure 4-6 illustrates the **COMPARE ACQMEM TO REFMEM** menu display; displays for the other three Auto-Run conditions are shown in Figure 4-7.

After you press AUTO, the logic analyzer displays status information on the progress of data acquisition. The status displays for **CONTINUOUS TRIGGER OUT**, **TRIGGER IN**, and **STORE AFTER TRIGGER** are similar to the display shown in Figure 4-4 except that the title of the Auto-Run condition is displayed on the second line of the screen. The **COMPARE ACQMEM TO REFMEM** status displays are special versions of the State Table and Timing Diagram data displays; see Figures 4-8 and 4-9.

### NOTE

*Auto-Run setups do not specify trigger conditions. They determine what action the logic analyzer takes when the trigger specified in the Trigger Spec menu occurs.*

## COMPARE ACQMEM TO REFMEM

In this Auto-Run condition, the 1240 or 1241 Logic Analyzer searches for the trigger specified in the Trigger Spec menu. When the trigger event is found, the logic analyzer fills acquisition memory, compares acquisition memory to reference memory, then takes action depending on whether the memories are equal or unequal. The three possible actions are: **DISPLAY AND REACQUIRE** (display acquisition memory and restart the trigger search), **DISCARD AND REACQUIRE** (discard the current acquisition, saving the previous one, and restart the trigger search), or **DISPLAY AND STOP** (stop and display acquisition memory).

The fields associated with **COMPARE ACQMEM TO REFMEM** are described in Figure 4-6.

The **COMPARE ACQMEM TO REFMEM** status displays are special versions of the State Table and Timing Diagram displays; see Figures 4-8 and 4-9.

The ACQ# field in the upper-right corner of the State Table or Timing Diagram display shows the number of acquisitions since you pressed AUTO. The number is incremented even if acquired data is not displayed.

When the trigger event specified in the Trigger Spec menu is found, a signal is supplied to the EXT TRIG OUT BNC. You can select this signal to be **PULSED** (high for at least 80 ns) or **LATCHED** (high until next acquisition starts).

### NOTE

*The selected data in acquisition memory must be identical to the corresponding data in reference memory, including time relationships between two-timebase data, for the memories to be considered equal.*

*If the data in REFMEM was acquired with different parameters than the current setup, ACQMEM and REFMEM are always unequal.*

*If glitch display is off, memory comparisons are based on the actual contents of memory and not on what may be displayed. See Glitch Display in Section 5 for more information.*

## CONTINUOUS TRIGGER OUT

In this Auto-Run condition, the 1240 or 1241 Logic Analyzer continuously searches for the trigger specified in the Trigger Spec menu. When the trigger is found, the search restarts, and the logic analyzer supplies a signal to the EXT TRIG OUT BNC (on the back panel, see Figure 1-3) for at least 80 ns.

Press the STOP key on the front panel to stop this auto-acquisition method. The data that occurred immediately before the STOP keystroke is displayed.

The menu display for **CONTINUOUS TRIGGER OUT** is shown in Figure 4-7.

## TRIGGER IN

In this Auto-run condition, the 1240 or 1241 Logic Analyzer continuously searches for the trigger conditions specified in the Trigger Spec menu. The EXT TRIG input is sampled after an event occurs (on the probe tip) that satisfies the trigger conditions necessary to cause a trigger. If the EXT TRIG IN signal is true 50 - 150 ns after the trigger event is true, the logic analyzer triggers, stops, and displays stored data. If the EXT TRIG IN signal is false, the trigger search continues. Table 4-6 summarizes the actions associated with the different combinations of the trigger event and the EXT TRIG IN signal.

When the trigger event specified in the Trigger Spec menu is found, the logic analyzer supplies a signal to the EXT TRIG OUT BNC. You can select this signal to be **PULSED** (high for at least 80 ns) or **LATCHED** (high until next acquisition starts). See Table 8-5 for the specifications of the EXT TRIG OUT and IN signals.

The menu display for **TRIGGER IN** is shown in Figure 4-7. **TRIGGER IN** can be used to link two logic analyzers for triggering on very wide data words or on time-related sequences.

**Table 4-6**  
**TRIGGER IN: COMBINATIONS OF EXT TRIG IN/OUT BNCs**

Trigger Event <sup>a</sup>	EXT TRIG IN	Logic Analyzer Action
Not Found	False	Continue trigger search
Not Found	True	Continue trigger search
Found	False	Restart trigger search
Found	True	Trigger, stop, and display data

<sup>a</sup> Specified in the Trigger Spec menu. Signal to the EXT TRIG OUT BNC goes true when the trigger event is found.



TRIGGER SPEC    AUTO-RUN SPEC    KNOB=SELECT

1    AUTO-RUN CONDITION: COMPARE ACQMEM TO REFMEM

WHEN EQUAL    DISPLAY AND REACQUIRE

WHEN NOT EQUAL    DISPLAY AND STOP

COMPARISON PARAMETERS:

GROUPS:    GRP A    GRP B    CTL1    GRP C    GRP D    CTL2

MASK:    00    00    11    0000    0000    1111

4

COMPARISON LIMITS:    FIXED

LIMITS:    255    526

5

AUDIBLE TRIGGER INDICATOR:    OFF

EXTERNAL TRIGGER OUT BNC    PULSED    ON TRIGGERS

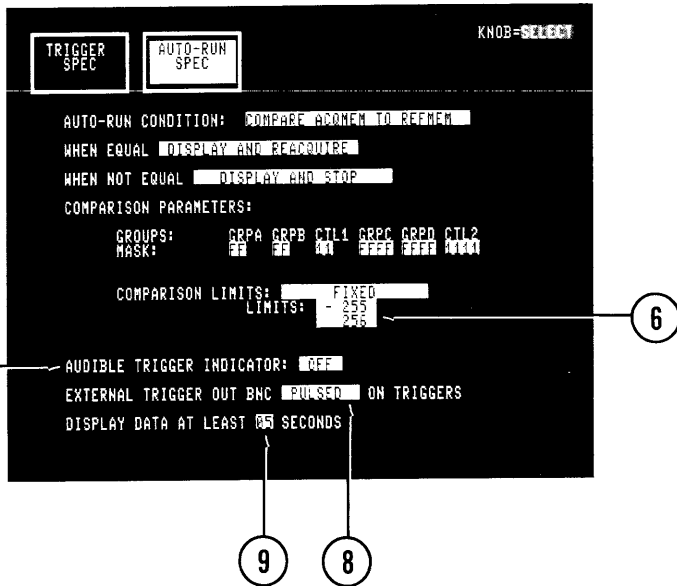
DISPLAY DATA AT LEAST    35    SECONDS

- Logic Analyzer searches for the trigger specified in the Trigger Spec menu; when the trigger event is found, acquisition memory is compared to reference memory. The resulting action taken depends on whether the memories are equal or unequal.
- Actions to be taken when the memories are equal or unequal. Selections are: **DISPLAY AND REACQUIRE**, **DISCARD AND REACQUIRE** (new acquisitions discarded, last acquisition displayed when the logic analyzer triggers or is stopped), and **DISPLAY AND STOP**.
- Group names.
- Mask fields, one per group; specify which channels will be compared. Enter mask digits in the input radix for each group. Choose each digit so that binary 1's are in equivalent positions of those channels you want to include in the comparison, and binary 0's are in positions of channels you want to exclude. Don't care (X) is the same as 0 (channel not compared). Default is all channels compared.
- Determines how much of acquisition memory is compared to reference memory. Selections are **FIXED** and **BETWEEN CURSORS**. With **FIXED**, comparison is limited to the acquisition memory locations between (and including) the values shown in the LIMITS fields. With **BETWEEN CURSORS**, the comparison is limited to the memory locations between (and including) the current positions of data cursors 1 and 2.

(cont.)

**Figure 4-6.** Menu display for the COMPARE ACQMEM TO REFMEM Auto-Run condition. The selected data in acquisition memory must be identical to the corresponding data in reference memory, including time relationships between two-timebase data, for the memories to be considered equal.

(cont.)



- 6 If you select **FIXED** in the preceding field, these lines are select fields. Selections for each field range from **-4095** to **+4095**.

If you select **BETWEEN CURSORS** in the preceding field, these lines display the current locations of data cursors 1 and 2. The cursor positions are the limits of the comparison. The cursor positions can be changed during auto-acquisition, but movement may be slow. Refer to Section 5 for a complete description of the data cursors.

It is possible that not all memory locations between the specified limits will contain data. Locations at which neither memory has data are always equal. Locations at which only one memory has data are never equal.

- 7 **AUDIBLE TRIGGER ON/OFF**. If you select **ON**, a tone is generated when the trigger specified in the Trigger Spec menu is found and memory has filled.
- 8 Selects the duration of the signal supplied on the EXT TRIG OUT BNC. Selections are **PULSED** (signal high for at least 80 ns) and **LATCHED** (signal high until next acquisition starts).
- 9 Used with **DISPLAY AND REACQUIRE** (see callout 2) to determine the minimum time between acquisitions. Values are **00** to **99** seconds.

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Figure 4-6. Menu display for the COMPARE ACQMEM TO REFMEM Auto-Run condition (cont.).

## STORE AFTER TRIGGER

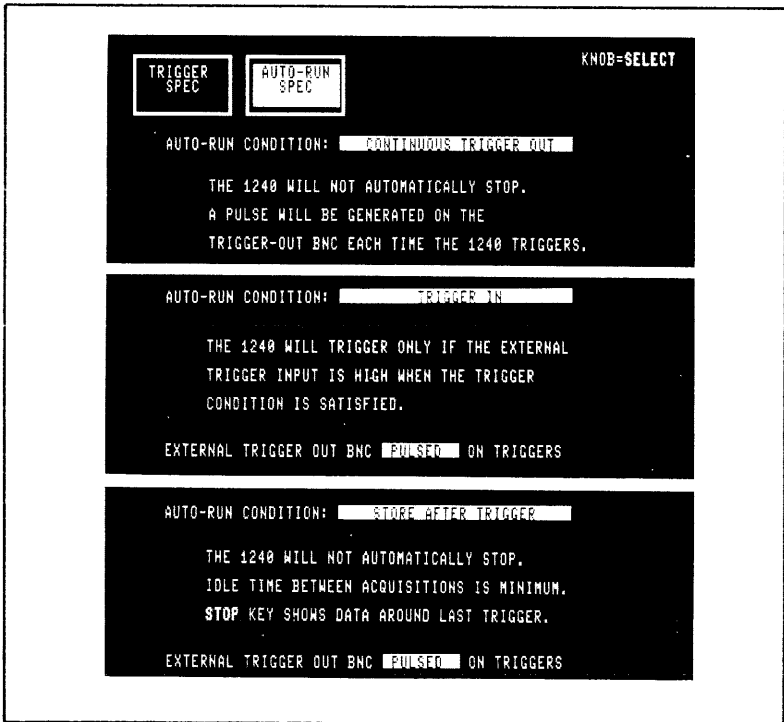
In this Auto-Run condition, the 1240 or 1241 Logic Analyzer continuously searches for the trigger specified in the Trigger Spec menu. When you press STOP, the data stored as a result of the last trigger is displayed.

If no trigger has occurred or if a trigger has occurred but acquisition memory is not full (timebase may be slow), the current contents of acquisition memory is displayed.

The menu display for **STORE AFTER TRIGGER** is shown in Figure 4-7.

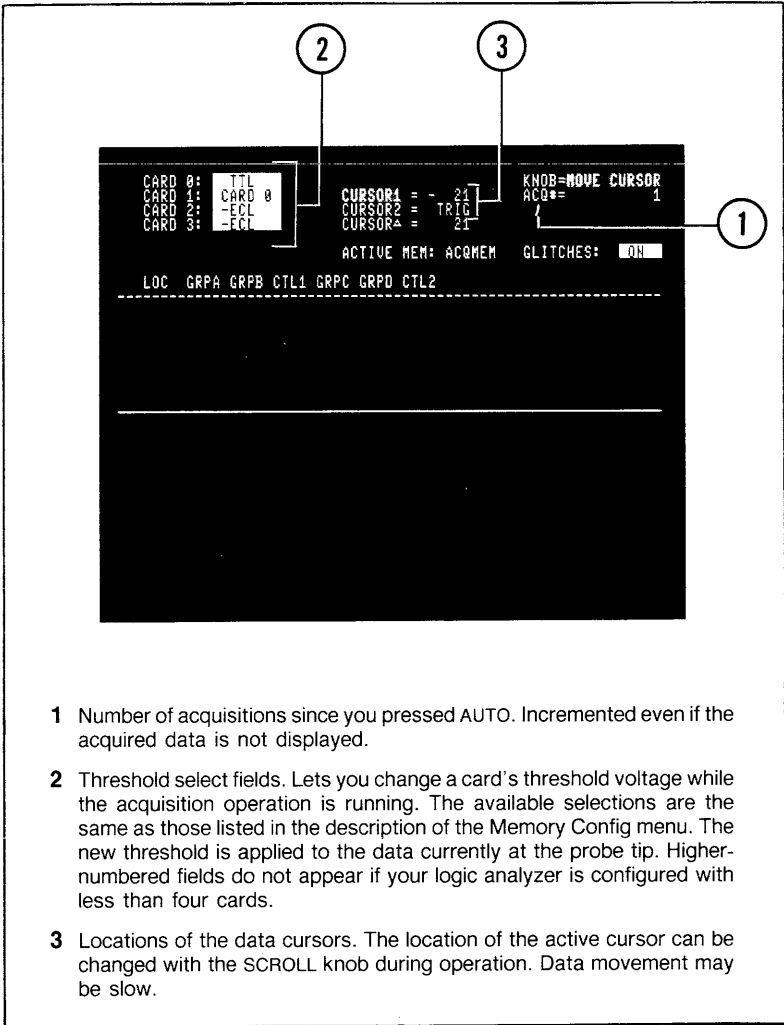
**STORE AFTER TRIGGER** lets you continuously sample the system under test at the point defined by the Trigger Spec menu. For example: your prototype system suffers intermittent system crashes, and you determine that the error occurs after some point BB. Set the Trigger Spec menu to trigger on BB, then change to the Auto-Run Spec menu. Select **STORE AFTER TRIGGER**, then press AUTO. Every time the logic analyzer finds BB, it triggers and fills acquisition memory. Let the logic analyzer run until the next system crash, then press STOP. Acquisition memory from the last trigger will show data around the error.

When the trigger event specified in the Trigger Spec menu is found, the logic analyzer supplies a signal to the EXT TRIG OUT BNC. You can select this signal to be **PULSED** (high for at least 80 ns) or **LATCHED** (high until next acquisition starts).



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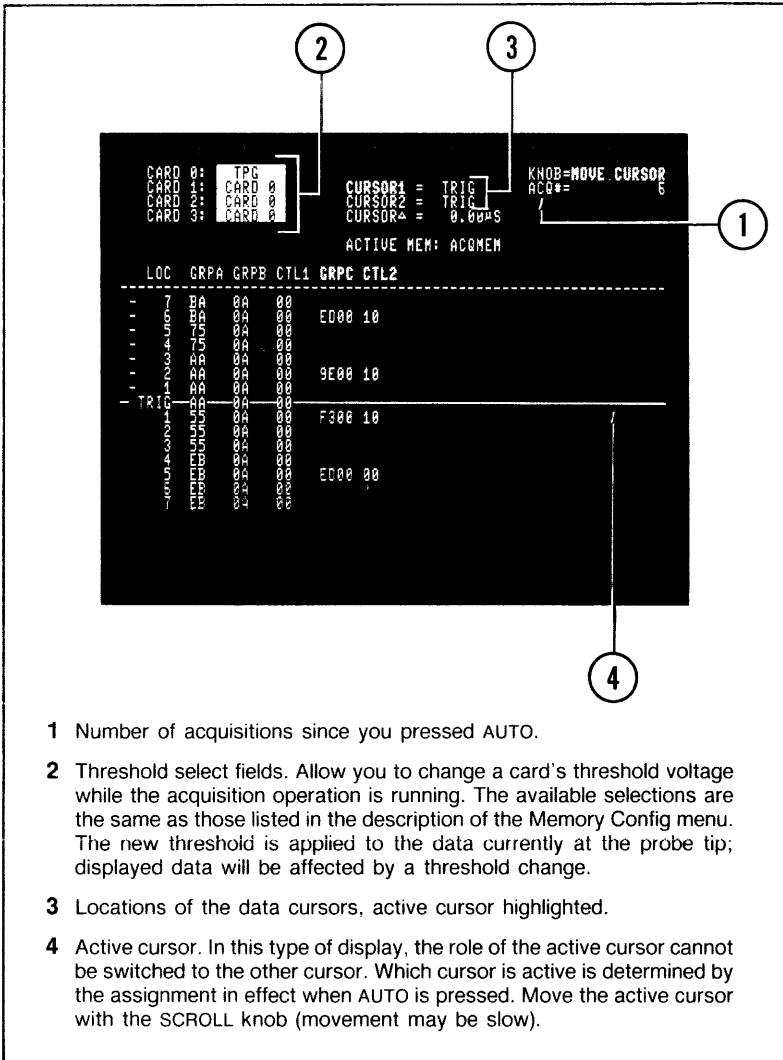
**Figure 4-7. Menu displays for the CONTINUOUS TRIGGER OUT, TRIGGER IN, and STORE AFTER TRIGGER Auto-Run conditions.** At each trigger, the logic analyzer supplies a signal to the EXT TRIG OUT BNC on the back panel. The signal can be **PULSED** (signal high for at least 80 ns) or **LATCHED** (signal high until next acquisition starts).



- 1 Number of acquisitions since you pressed AUTO. Incremented even if the acquired data is not displayed.
- 2 Threshold select fields. Lets you change a card's threshold voltage while the acquisition operation is running. The available selections are the same as those listed in the description of the Memory Config menu. The new threshold is applied to the data currently at the probe tip. Higher-numbered fields do not appear if your logic analyzer is configured with less than four cards.
- 3 Locations of the data cursors. The location of the active cursor can be changed with the SCROLL knob during operation. Data movement may be slow.

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**Figure 4-8. Status display for COMPARE ACQMEM TO REFMEM actions DISPLAY AND STOP, DISCARD AND REACQUIRE.**

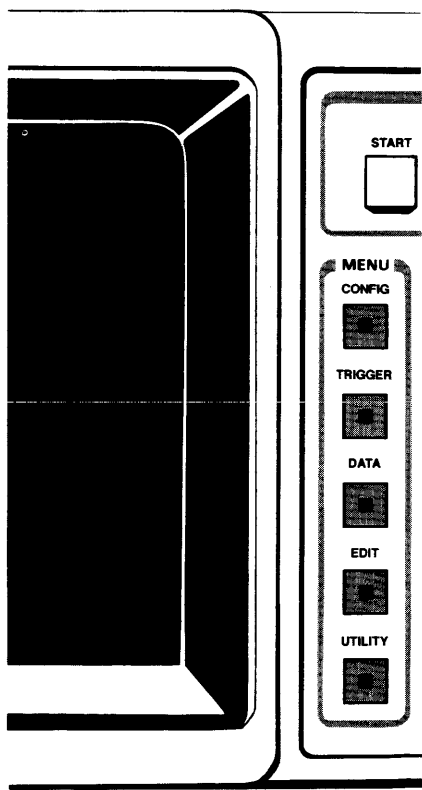


- 1 Number of acquisitions since you pressed AUTO.
- 2 Threshold select fields. Allow you to change a card's threshold voltage while the acquisition operation is running. The available selections are the same as those listed in the description of the Memory Config menu. The new threshold is applied to the data currently at the probe tip; displayed data will be affected by a threshold change.
- 3 Locations of the data cursors, active cursor highlighted.
- 4 Active cursor. In this type of display, the role of the active cursor cannot be switched to the other cursor. Which cursor is active is determined by the assignment in effect when AUTO is pressed. Move the active cursor with the SCROLL knob (movement may be slow).

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**Figure 4-9. Status display for COMPARE ACQMEM TO REFMEM, DISPLAY AND REACQUIRE action.** The bottom half of the display is shown in State Table or Timing Diagram format, depending on which data display format was last used. Moving the cursor affects the comparison limits if BETWEEN CURSORS is selected.

5



DATA

DATA

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Press the DATA key on the front panel to access the State Table and Timing Diagram data display formats. Both formats can display acquisition memory or reference memory.

The first time after power-up that the 1240 or 1241 Logic Analyzer acquires data and stops, it automatically displays the data in the State Table format. As more acquisitions are taken, the logic analyzer displays data in either the State Table or Timing Diagram format, depending on which was last used. Change the data display format by touching the appropriate soft key at the top of the screen.

Figures 5-1 and 5-3 show sample State Table displays; Figures 5-5, 5-6, and 5-7 show sample Timing Diagrams. The other figures in this section illustrate specific data display characteristics.

## COMMON DATA DISPLAY FEATURES

**Data Scrolling and Cursor Control.** Data scrolling is controlled by two data cursors: Cursor 1 and Cursor 2. The cursors are displayed as horizontal lines running through a text line in the State Table and as vertical lines across the timing traces in the Timing Diagram. In both displays, Cursor 1 is a solid line and Cursor 2 is a dotted line. The data cursors are controlled by the SCROLL knob and the CHANGE ACTIVE CURSOR soft key at the bottom of the screen.

One cursor is "active" and the other is "inactive"; either Cursor 1 or Cursor 2 may be the active cursor. The location of the active cursor determines what data is displayed on the screen. The active cursor never leaves the screen; therefore, only data surrounding the active cursor is displayed. To display a different portion of memory, move the active cursor with the SCROLL knob. The scrolling operation wraps around the end of memory in either direction.

Touch the CHANGE ACTIVE CURSOR soft key at the bottom of the screen to transfer the role of active cursor to the other cursor.

The location of each cursor is displayed at the top of the screen. The label for the active cursor is highlighted. The cursor positions are the number of memory cycles or locations (labeled LOC in the State Table) the cursors are offset from the trigger. Memory locations preceding the trigger are assigned negative values; locations after the trigger are positive. At power-up, both cursors are positioned at the trigger.

The line below the cursor locations is CURSOR  $\Delta$  (difference between the cursors). CURSOR  $\Delta$  is a time value if: T1 is ASYNC with no clock qualification, data qualification (STORE) is not used in the global event recognizer, and Cursors 1 and 2 are both positioned on memory locations within the bounds of the asynchronous data. If these conditions are met, CURSOR  $\Delta$  is a time value in units of the asynchronous clock period (see callout 2 in Figure 5-1). Use this feature to measure the time between two events.

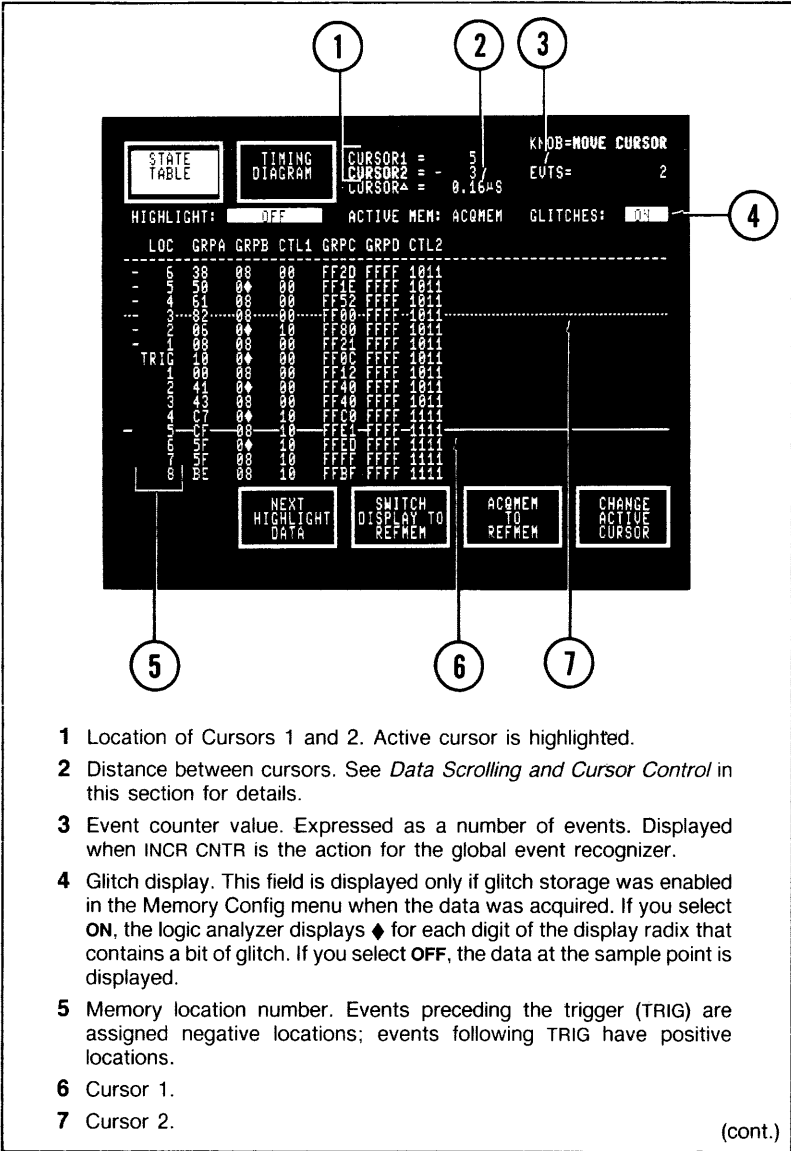
If any of the conditions listed above are not met, CURSOR  $\Delta$  is expressed as the number of memory locations between the cursors.

**Trigger Display.** The trigger location in the State Table is marked by the letters TRIG in the LOC (memory location) column. In the Timing Diagram, the trigger is marked by a broken vertical line across the timing traces.

If you press the STOP key before a trigger has occurred, the last (most recently acquired) location in acquisition memory is the "stop trigger." This location is labeled STOP in the State Table. All other memory locations are negative in relation to a stop trigger.

If a cursor is positioned at the trigger, the cursor location display at the top of the screen is TRIG (or STOP).





- 1 Location of Cursors 1 and 2. Active cursor is highlighted.
- 2 Distance between cursors. See *Data Scrolling and Cursor Control* in this section for details.
- 3 Event counter value. Expressed as a number of events. Displayed when INCR CNTR is the action for the global event recognizer.
- 4 Glitch display. This field is displayed only if glitch storage was enabled in the Memory Config menu when the data was acquired. If you select ON, the logic analyzer displays ♦ for each digit of the display radix that contains a bit of glitch. If you select OFF, the data at the sample point is displayed.
- 5 Memory location number. Events preceding the trigger (TRIG) are assigned negative locations; events following TRIG have positive locations.
- 6 Cursor 1.
- 7 Cursor 2.

(cont.)

**Figure 5-1. One-timebase State Table display with glitches.** A ♦ symbol indicates that glitch information was stored for at least one bit of the digit. The location of the active cursor determines which data is displayed. Move the active cursor with the SCROLL knob. The label of the active cursor is highlighted at the top of the screen. Touch the CHANGE ACTIVE CURSOR soft key to assign the active role to the other data cursor. Data is displayed in the radices selected in the Channel Grouping menu.



**Glitch Display.** The GLITCHES ON/OFF field is displayed only if glitch storage was enabled in the Memory Config menu when the displayed data was acquired. See callout 4 in Figure 5-1 and callout 13 in Figure 5-5.

If you select GLITCHES ON in the State Table, the logic analyzer displays the special diamond-shaped glitch character (◆) for each digit of the display radix for which glitch information was stored. It is not necessary for all bits of the digit to be glitch; the glitch character is displayed for the digit if any bit is glitch information.

If you select GLITCHES ON in the Timing Diagram, a glitch is displayed as a wide, intensified rising edge (see Figure 5-5).

If you select GLITCHES OFF, the data at the sample point is displayed instead of the glitch symbol. (GLITCHES OFF disables glitch highlighting; see *Highlighting* in this section.)

#### NOTE

*ACQMEM to REFMEM comparisons in Auto-Run and highlighting for patterns and memory differences are based on the actual contents of memory and not on what may be displayed if glitch display is off.*

**Data Correlation.** The 1240 and 1241 Logic Analyzers display data in the order it occurred at the probe tip. The data correlation feature preserves the time relationship between events, including events occurring on different timebases.

Figure 5-2 illustrates the data correlation feature. The State Table and Timing Diagram displays in the figure are based on the sample waveforms. Each waveform represents one channel of data. In this example, one channel is clocked by T1 ASYNC and the other by T2 SYNC.

To interpret the order in which events occurred from a two-timebase State Table or Timing Diagram display, remember this convention:

*If a T2 event occurs after a T1 event and before any other event, the logic analyzer displays both events at the same memory location. In all other cases, there is one event per location.*

A sample two-timebase State Table display is shown in Figure 5-3.

To cover gaps in timing diagram traces, the logic analyzer displays information extrapolated from the last valid data. In Figure 5-2, extrapolated data is shown by lighter-weight lines. In an actual Timing Diagram, you can differentiate extrapolated data from valid data by using the T1 VALID or T2 VALID highlighting selections (see *Highlighting*, next, for more information). See Figure 5-6 for a sample two-timebase Timing Diagram display.

**Highlighting.** Highlighting accents data displays by shading the background of selected data locations. The shaded locations (color shading in the 1241) make analysis of acquired data much easier. In the State Table display, data that meets the highlight requirements is marked by highlighted LOC numbers. In the Timing Diagram, vertical bars of highlighting across all displayed traces mark locations that meet the highlighting requirements (see Figure 5-6 for an example). The selections available in the HIGHLIGHT field are:

- **OFF** — no highlighting.
- **MEM DIFFS** — highlight differences between acquisition and reference memory.
- **GLITCHES** — highlight glitches. Glitch display must be on (GLITCHES ON selected). In the Timing Diagram, a location is highlighted only if a glitch is present in a currently displayed trace.

- **PATTERNS** — highlight the first location of all occurrences of the search pattern. The search pattern is specified in the Search Pattern Entry menu. See *Searching for a Data Pattern*, next, for more information.
- **T1 VALID** — highlight a location if it has valid T1 data.
- **T2 VALID** — highlight a location if it has valid T2 data.

Touch the NEXT HIGHLIGHT DATA soft key at the bottom of the screen to move the active cursor to the first location of the next highlighted data. The active cursor does not move if there is no data in memory that meets the highlight requirements. This function wraps around the end of memory if necessary.

#### NOTE

*The T1 VALID and T2 VALID highlighting selections are useful in the Timing Diagram when data for two timebases is displayed (see Figure 5-6).*

*Highlighting for patterns and memory differences is based on the actual contents of memory and not on what may be displayed if glitch display is off. For example: if you select GLITCHES OFF and HIGHLIGHT: MEM DIFFS, areas that appear to be the same in both memories can be highlighted if the actual memories (containing glitch information) are different.*

**Searching for a Data Pattern.** The Search Pattern Entry menu in the EDIT menu group (see Section 6) allows you to specify a pattern of 1 - 8 consecutive memory locations. If you select **PATTERNS** in the highlighting field of the State Table or Timing Diagram, the logic analyzer highlights the first location of each pattern occurrence on the screen. In the State Table, LOC numbers are highlighted. In the Timing Diagram, a location is highlighted by a vertical bar across all displayed traces.

The default search pattern is one line of all don't cares (X). This pattern matches all values, including no data.

#### NOTE

*The pattern function operates only if PATTERN SEARCH ENABLED is selected in the Search Pattern Entry Menu.*

**Acquisition Memory (ACQMEM) and Reference Memory (REFMEM).** Acquisition and reference memory can both be displayed in State Table and Timing Diagram formats. When the logic analyzer displays acquisition memory, a soft key at the bottom of the screen is labeled SWITCH DISPLAY TO REFMEM. Touch this soft key to display reference memory. When reference memory is displayed, this soft key is labeled SWITCH DISPLAY TO ACQMEM. The ACTIVE MEMORY field is displayed below the cursor readout (see callout 9 in Figure 5-1 and callout 12 in Figure 5-5). This field serves as a reminder of which memory (ACQMEM or REFMEM) is currently displayed. ACTIVE MEMORY is an informational field; it cannot be accessed by the field cursor.

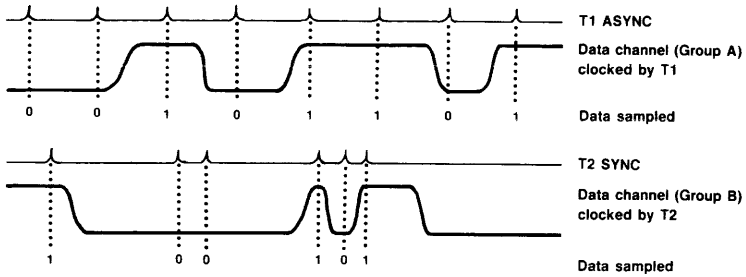
The ACQMEM TO REFMEM soft key at the bottom of the screen allows you to copy acquisition memory to reference memory. After you touch this key, PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT) is displayed at the top of the screen. When you press X, reference memory is overwritten by a copy of acquisition memory; the previous contents of REFMEM cannot be retrieved.

The power-up default acquisition memory contains all zeros; default reference memory contains a fixed random pattern.

#### NOTE

*The positions of the data cursors do not change when you change memories or perform a new acquisition.*

**EVENTS AT THE PROBE TIP**



The following convention is used when displaying data acquired with two timebases:

If a T2 event occurs after a T1 event and before any other event, the two events are displayed at the same memory location (LOC). In all other cases, there is one event per location.

**STATE TABLE**

LOC	A	B
58	0	1
59	0	0
60	1	0
61	0	0
62	0	1
63	1	0
64	0	1
65	1	1
66	1	0
67	0	1
68	1	1

The convention that is described at left allows you to reconstruct from the display the order of events at the probe tip:

A T1 (Group A) event followed by a T2 (Group B) event, then two consecutive T1 events followed by two consecutive T2 events.

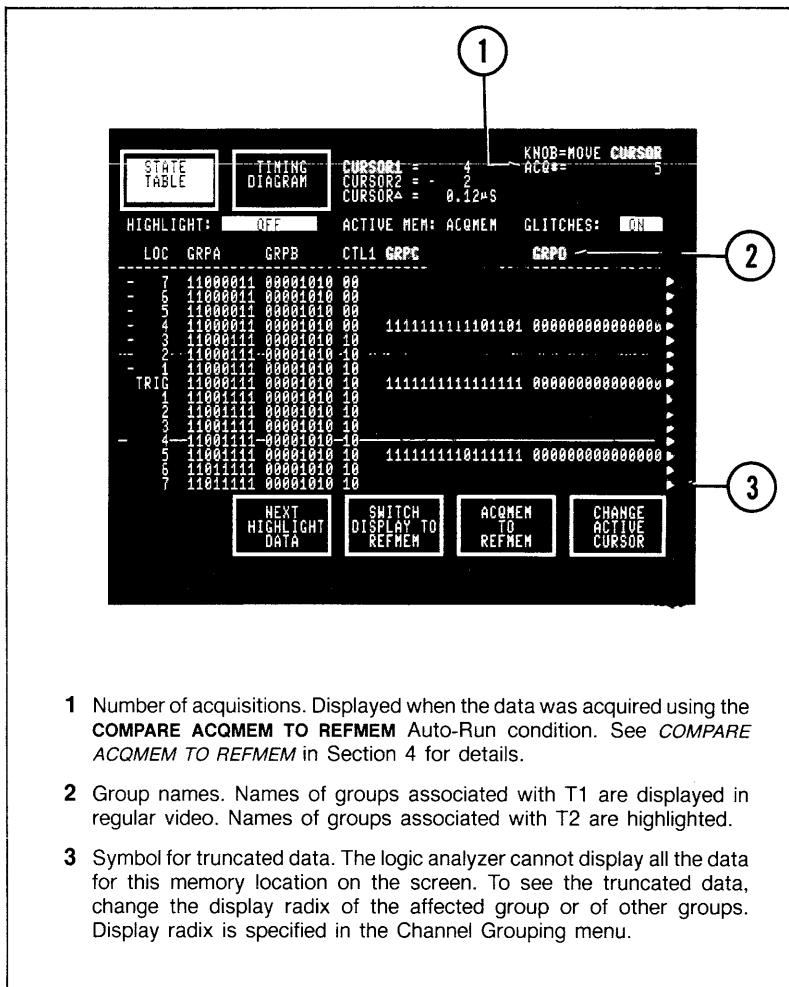
**TIMING DIAGRAM**



The logic analyzer prevents gaps in timing traces by extrapolating last valid data. In this example, extrapolated data is shown by lighter-weight lines.

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**Figure 5-2. Explanation of the data correlation feature.** If a T2 event occurs after a T1 event and before any other event, the logic analyzer displays both events at the same memory location.



- 1 Number of acquisitions. Displayed when the data was acquired using the **COMPARE ACQMEM TO REFMEM** Auto-Run condition. See *COMPARE ACQMEM TO REFMEM* in Section 4 for details.
- 2 Group names. Names of groups associated with T1 are displayed in regular video. Names of groups associated with T2 are highlighted.
- 3 Symbol for truncated data. The logic analyzer cannot display all the data for this memory location on the screen. To see the truncated data, change the display radix of the affected group or of other groups. Display radix is specified in the Channel Grouping menu.

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**Figure 5-3. Two-timebase State Table display with truncated data.** If a T1 and a T2 event are displayed on the same line, you know the T1 event occurred before (or at the same time as) the T2 event. See *Data Correlation* for details.

**Memory Configuration Requirements.** Two setup parameters from the Memory Config menu are stored with each acquisition and reference memory: memory width vs. depth, and pod-timebase assignments. An acquisition or reference memory that differs from the current setup in one or both of these parameters cannot be displayed. An error message is displayed that describes the first incompatibility found. (Refer to Section 8 for a description of all error messages.) For example: if REFMEM was stored with a 9-channel memory width vs. depth of 9\*257 samples, it can be displayed only if the current 9-channel memory width vs. depth selection is also 9\*257. If the current width vs. depth selection is not 9\*257, the error message displayed is CONFIG ERROR: REFMEM 9 CHANNEL CARDS ARE 9 BY 257.

These two Memory Config parameters also affect the search pattern set up in the Search Pattern Entry menu. When you leave Memory Config after changing any of these parameters, the logic analyzer restructures the search pattern to match the new configuration. Refer to Table 8-3 for a description of the changes.

**Blank Areas in the Data Display.** Blank areas in the State Table can be caused by one or more of the following conditions:

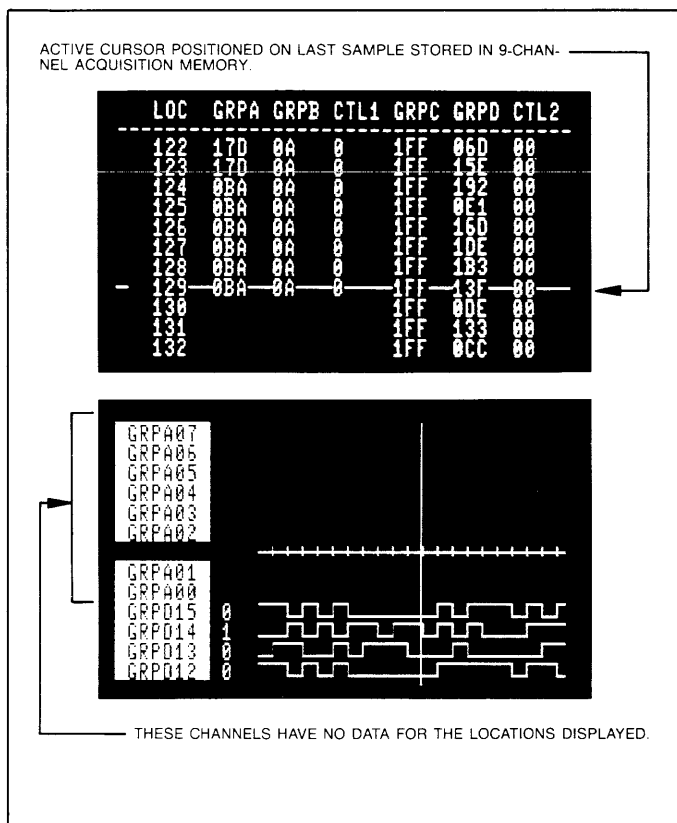
- A difference in the 9-channel and 18-channel acquisition memory depths. The sample State Table display in Figure 5-4 shows the active cursor positioned on the last data sample in 9-channel acquisition memory. Beyond this sample, the screen is blank for 9-channel groups but data continues to be displayed for 18-channel groups.
- Certain trigger conditions combined with the LOOK FOR TRIGGER **IMMEDIATELY** selection in the Trigger Spec menu. See *Trigger Position* in Section 4 for details.
- Active cursor positioned out of the bounds of stored data.<sup>1</sup> Any movement of the SCROLL knob will move the active cursor to the closest location with valid data.
- Correlation of a two-timebase acquisition. For example: in Figure 5-3, the blanks between occurrences of timebase T2 data indicate intervals where there was activity on timebase T1 but none on T2.

Blank areas in the Timing Diagram can be caused by the first three conditions described above, plus:

- A PAGE setting with channels that have no data for the locations displayed. The sample Timing Diagram display in Figure 5-4 illustrates this condition. In this display, channels GRPA07 - GRPA00 have no data for the locations displayed. Refer to *PAGE Field* later in this section for more information.

---

<sup>1</sup> ACQMEM and REFMEM can be different lengths; the length of ACQMEM can vary between acquisitions. If you display a memory with fewer locations than the previously displayed memory, the active cursor may be positioned on a blank location. Any movement of the SCROLL knob causes the logic analyzer to move the active cursor to the closest location with valid data.



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**Figure 5-4. Some causes of blank areas in the data displays.** The blank area in the State Table display in this example is caused by a difference in 9- and 18-channel acquisition memory depths. The blank area in the Timing Diagram is caused by channels with no data for the locations displayed. See *Blank Areas in the Data Display* for a description of other causes of blank areas.

## FEATURES SPECIFIC TO THE STATE TABLE

**Data Display Truncation.** The 1240 and 1241 Logic Analyzers cannot display all the data for a memory location if some combinations of instrument configuration and display radix are used. For these cases, the data is truncated at the right edge of the screen and the truncation symbol (▶) is displayed as the rightmost character (see callout 3 in Figure 5-3).

To see the truncated data, you must change the display radix of one or more groups in the Channel Grouping menu. You can take a group out of the display by changing its display radix to OFF, or you can decrease the number of digits displayed by selecting a higher display radix.



## FEATURES SPECIFIC TO THE TIMING DIAGRAM

**1240 EXPANSION Field.** In the 1240 Logic Analyzer, change the horizontal magnification of the Timing Diagram display by changing the value in the EXPANSION field (see callout 4 in Figure 5-5). The available selections are \*1, \*2, \*5, \*10, and \*20. When \*1 is selected, each trace shows 204 data samples. Each trace shows 11 data samples when \*20 is selected.

**1241 EXPAND Field.** In the 1241 Logic Analyzer, you can change both horizontal and vertical magnification of the Timing Diagram display (see callouts 4 and 5 in Figure 5-6). Selections for horizontal magnification are \*1, \*2, \*5, \*10, and \*20. Selections for vertical magnification are \*1 and \*2. Trace height of the displayed waveforms is doubled in the \*2 vertical expand mode (see callout 4 in Figure 5-7). To accommodate this expanded display, soft keys and some information and select fields are removed from the top and bottom of the screen display. To restore a full screen display, select \*1 for the vertical expand field.

### NOTE

*Operator error messages (normally displayed at the top of the screen) are not displayed when the Timing Diagram's vertical expand field is set to the \*2 selection. Return the display to the \*1 selection before making subsequent acquisitions in order to avoid missing error messages (such as NO VALID DATA ACQUIRED or NO HIGHLIGHTED LOCATIONS OCCUR) that may be generated but cannot be displayed when \*2 is selected.*

**Memory Window.** Above the timing traces is a memory window showing which part of acquisition or reference memory is displayed. (see callout 11 in Figure 5-5). The window shifts if data is scrolled (active cursor moved to a different area of memory). Window size decreases as the expansion factor increases. A "T" is displayed in the field to show the location of the trigger event. If you press the STOP key before the trigger is found, the T is displayed at the far right of the memory window.

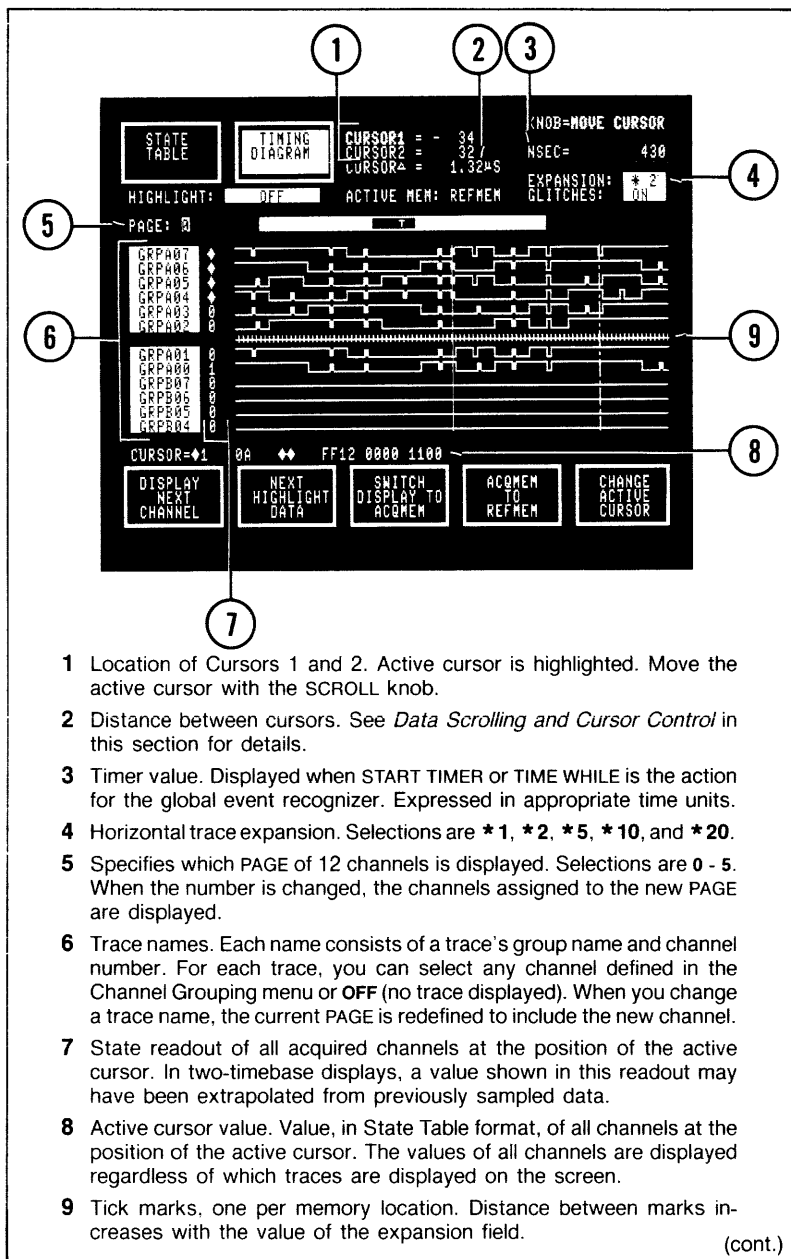
**PAGE Field.** The 1240 and 1241 Logic Analyzers can display traces for 12 channels at a time, but the total number of channels may be much larger. The PAGE field allows you to group channels for display and provides a method for quickly recalling a specific group of channels to the screen.

There are six PAGE displays, numbered 0-5. Each PAGE consists of 12 traces. PAGE 0 is displayed the first time you access the Timing Diagram; use the data entry keys to enter a different PAGE number. When the number is changed, the traces associated with the new PAGE are displayed.

A reverse video select field to the left of each trace contains the trace's group name and the position of that trace (channel) within the group. You can select any channel assigned to a group in the Channel Grouping menu or OFF (no trace). This feature allows you to alter any PAGE to suit your needs. When you select a new channel, the trace corresponding to that channel is displayed, and the current PAGE is redefined to include the new channel. The number displayed next to the group name identifies a specific channel by its position in the group as seen in the Channel Grouping menu. For example: an eight-channel group named DATA is defined in the Channel Grouping menu as <sup>000222X</sup>32103210X. Trace DATA07 refers to the most significant (leftmost) channel: channel 3 of pod 0. Trace DATA00 refers to the least significant (rightmost) channel: channel 0 of pod 2. Trace DATA04 refers to channel 0 of pod 0.

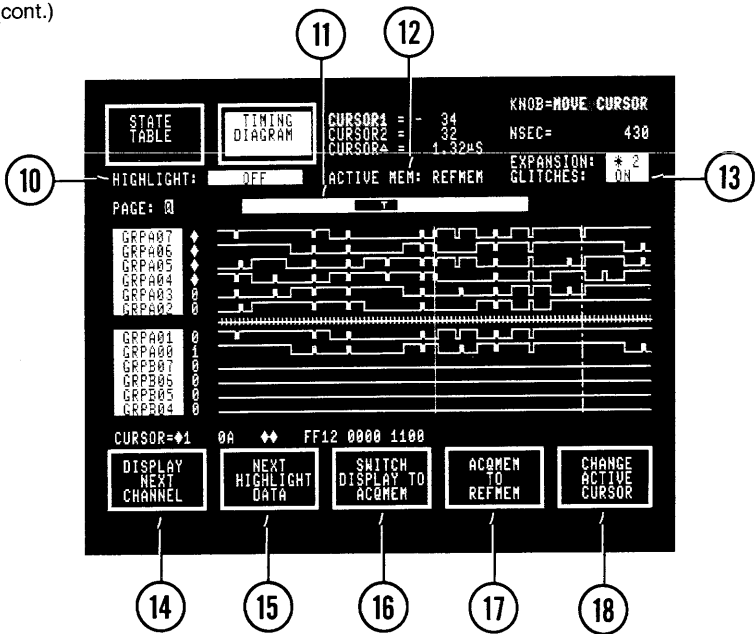
The DISPLAY NEXT CHANNEL soft key at the bottom of the screen allows you to quickly build a set of descending channel numbers. Each time you touch the soft key, the trace for the next lower channel in that group is displayed, and the blinking field cursor moves down to the next field. For example: To change the last six channels of the PAGE shown in Figure 5-5 to channels GRPB07 - GRPB02, move the blinking field cursor to trace GRPA01, then use the SELECT keys to choose GRPB07. Now touch DISPLAY NEXT CHANNEL five times.

The logic analyzer creates six default PAGE trace sets from the power-up default grouping arrangement in the Channel Grouping menu. The first channel in PAGE 0 is the most significant channel in GRPA. The remaining channels in GRPA are displayed sequentially and are followed by the channels in GRPB (most significant channel first) until PAGE 0 is full. The next GRPB channel is the first channel in PAGE 1. This pattern continues through subsequent PAGEs until all channels are assigned. The pattern repeats as necessary until all six PAGEs are defined. The default PAGE 0 for a 1240 or 1241 equipped with two 9-channel cards is displayed in Figures 5-5 and 5-6.



**Figure 5-5. 1240 Timing Diagram display with glitches.** In the Timing Diagram, glitches are displayed as a wide, intensified rising edge. The trigger is marked by a broken vertical line across the traces. Cursor 1 is a solid vertical line; Cursor 2 is a dotted vertical line.

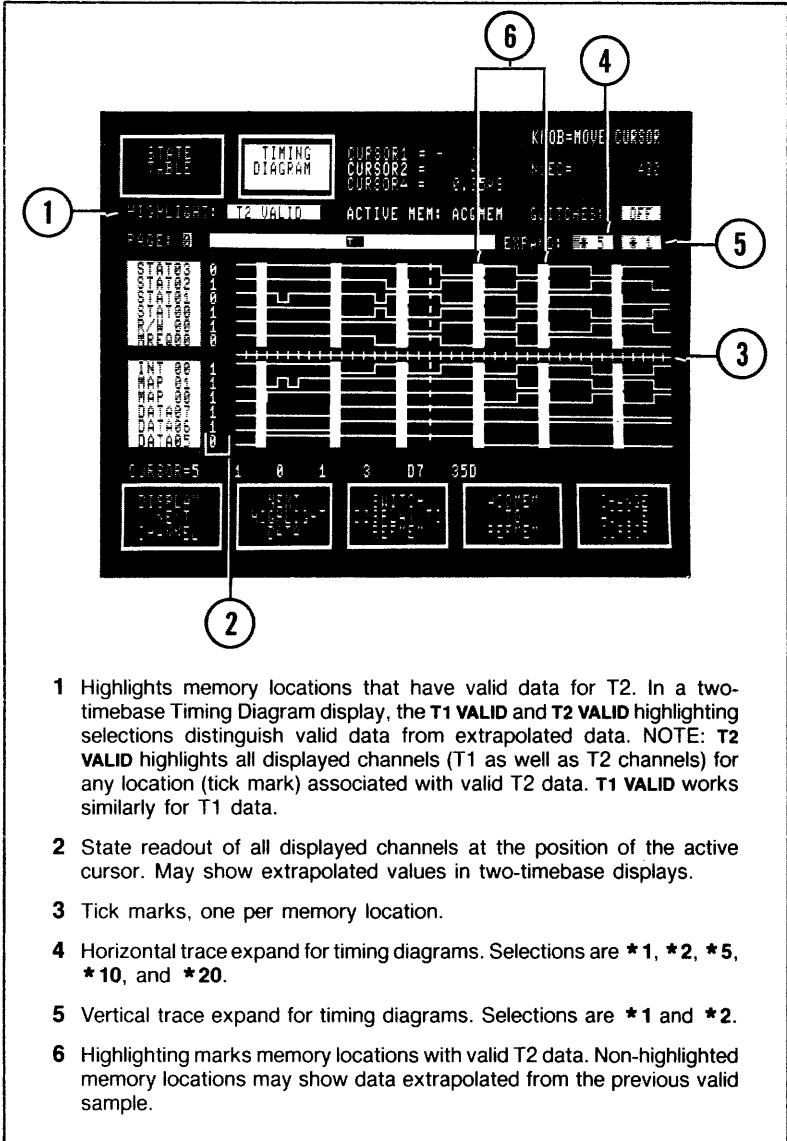
(cont.)



- 10** Determines the type of data to be displayed with highlighted video. Selections are OFF, MEM DIFFS, PATTERNS, GLITCHES, T1 VALID, and T2 VALID. See *Highlighting* in this section for details.
- 11** Memory window; shows area of memory displayed. T marks trigger.
- 12** Memory currently displayed (ACQMEM or REFMEM).
- 13** Glitch display. This field is displayed only if the data was acquired with glitch storage enabled in the Memory Config menu. If you select ON, each glitch is displayed as a wide, intensified rising edge. If you select OFF, the data value at the sample point is displayed.
- 14** Valid only when the blinking field cursor is in a trace name field (callout 6). Displays the next-lower channel name below the field cursor.
- 15** Moves the active cursor to the first location of the next occurrence of highlighted data.
- 16** Displays the other memory (ACQMEM or REFMEM). When ACQMEM is displayed, the label for this soft key changes to SWITCH DISPLAY TO REFMEM. The cursor positions do not change.
- 17** Copies the contents of acquisition memory into reference memory, overwriting the previous REFMEM contents. No action is taken unless you confirm the operation by pressing the X key.
- 18** Transfers the role of active cursor to the other cursor. If the other cursor is not onscreen, the display changes to show the data around it.

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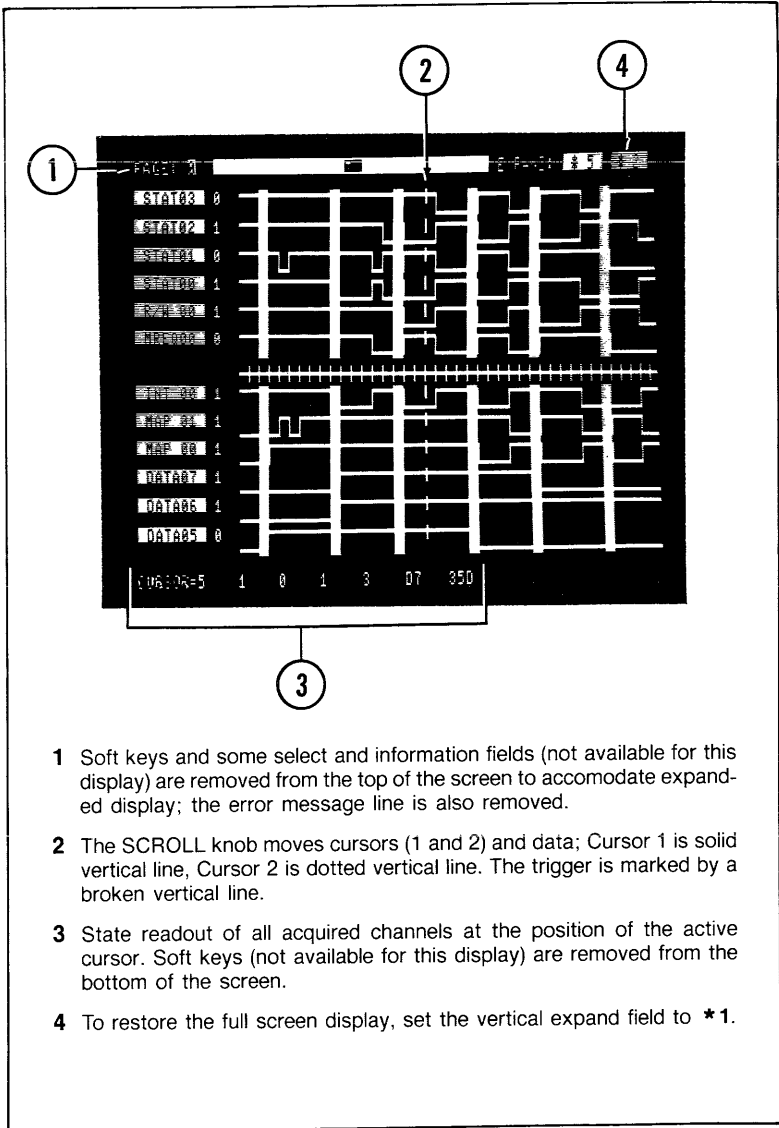
Figure 5-5. 1240 Timing Diagram display with glitches (cont.).



- 1 Highlights memory locations that have valid data for T2. In a two-timebase Timing Diagram display, the T1 VALID and T2 VALID highlighting selections distinguish valid data from extrapolated data. NOTE: T2 VALID highlights all displayed channels (T1 as well as T2 channels) for any location (tick mark) associated with valid T2 data. T1 VALID works similarly for T1 data.
- 2 State readout of all displayed channels at the position of the active cursor. May show extrapolated values in two-timebase displays.
- 3 Tick marks, one per memory location.
- 4 Horizontal trace expand for timing diagrams. Selections are \*1, \*2, \*5, \*10, and \*20.
- 5 Vertical trace expand for timing diagrams. Selections are \*1 and \*2.
- 6 Highlighting marks memory locations with valid T2 data. Non-highlighted memory locations may show data extrapolated from the previous valid sample.

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Figure 5-6. 1241 Timing Diagram display of data acquired with two timebases. To prevent gaps in the timing traces, the 1240 and 1241 Logic Analyzers display values extrapolated from the last valid data. A state readout of all acquired channels is displayed to the left of the traces. This readout shows the value of each channel at the position of the active cursor, including any extrapolated values. Use the T1 VALID or T2 VALID highlighting selections to distinguish between valid and extrapolated data in two-timebase displays.

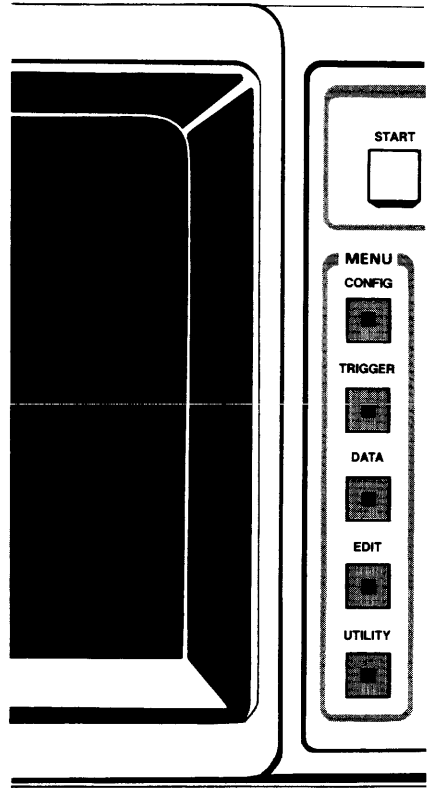


- 1 Soft keys and some select and information fields (not available for this display) are removed from the top of the screen to accommodate expanded display; the error message line is also removed.
- 2 The SCROLL knob moves cursors (1 and 2) and data; Cursor 1 is solid vertical line, Cursor 2 is dotted vertical line. The trigger is marked by a broken vertical line.
- 3 State readout of all acquired channels at the position of the active cursor. Soft keys (not available for this display) are removed from the bottom of the screen.
- 4 To restore the full screen display, set the vertical expand field to \*1.

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**Figure 5-7. 1241 Timing Diagram with the vertical expand field set to \*2.** When the 1241's vertical expand feature is set to \*2, the height of displayed timing traces doubles. Soft keys and some select and information fields are removed to accommodate the expanded display.

6



EDIT

SEARCH PATTERN ENTRY ..... 6-1  
    EDIT LINE VALUE Field ..... 6-1  
    CLEAR PATTERN ..... 6-1  
    DELETE LINE ..... 6-4  
    ADD LINE ..... 6-4  
    LOAD FROM ACTIVE CURSOR ..... 6-4  
REFERENCE MEMORY EDITOR ..... 6-5

Press the EDIT key on the front panel to access the Search Pattern Entry and the Reference Memory Editor menus. These menus provide methods for manipulating data in memory.



## SEARCH PATTERN ENTRY

A search pattern consists of 1 to 8 lines of data in State Table format. The default pattern is one line with all values set to don't care (X); this setting matches any value, including no data.

The search pattern is used by the pattern highlighting function in the DATA menus. This function operates only if PATTERN SEARCH **ENABLED** is selected in the Search Pattern Entry menu (see callout 3 in Figure 6-1). Whenever the 1240 or 1241 Logic Analyzer applies the search pattern to stored data, the message APPLYING SEARCH PATTERN — PLEASE WAIT is displayed at the top of the screen. If PATTERN SEARCH **ENABLED** is selected and you make a change to the search pattern then change to another menu, the new pattern is applied. If you do not need the pattern feature, select PATTERN SEARCH **DISABLED**.

Data lines in the pattern are displayed in the center of the menu (see Figure 6-1). Data is displayed according to the output radices specified in the Channel Grouping menu. A horizontal line across the screen marks the location of the "search data cursor" (see callout 6 in Figure 6-1). Move the search data cursor through the pattern with the SCROLL knob.

### NOTE

*The search data cursor is specific to this menu and is not related to the data cursors controlled in the State Table or Timing Diagram.*

**EDIT LINE VALUE Field.** The value of the pattern line at the location of the search data cursor is displayed in the EDIT LINE VALUE field (see callout 5 in Figure 6-1). Data in these fields is displayed using input radices. If the input and output radices for a group are different, the text displayed in the EDIT LINE and at the location of the search data cursor will be different even though the value is the same.<sup>1</sup>

Use the data entry keys to modify the data in the EDIT LINE as required. As you enter changes, the pattern line at the location of the search cursor is updated.

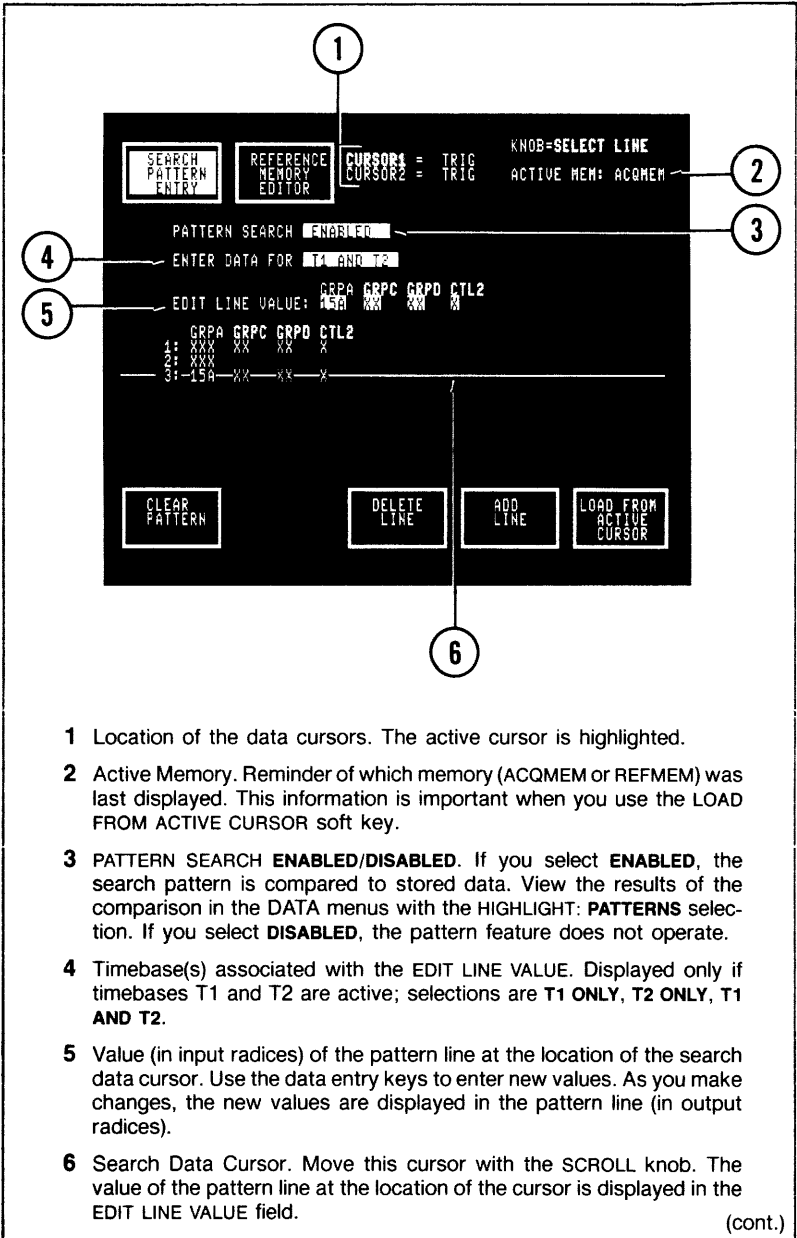
The ENTER DATA FOR field (see callout 4 in Figure 6-1) controls the timebase(s) associated with the EDIT LINE VALUE. This field is only displayed if both timebases T1 and T2 are active. Selections are **T1 ONLY**, **T2 ONLY**, and **T1 AND T2**. As you move the search data cursor, this field is updated to reflect the timebase(s) associated with each pattern line. For example: if you move the search data cursor to a pattern line with both T1 and T2 data, this field displays **T1 AND T2**. If you then change this field to **T1 ONLY**, the data for groups associated with T2 is deleted from the EDIT LINE VALUE.

With certain grouping setups, all channels cannot be displayed on the EDIT LINE at once. The truncation symbol (▶) will be displayed. Move the truncated channels onto the screen with the cursor keys. If the search pattern lines are truncated, you must change the display radix of one or more channel groups to see the truncated data.

The \$ symbol is displayed in the EDIT LINE if glitch and non-glitch channels are combined into one digit of the input radix.

**CLEAR PATTERN.** Touch this soft key to return the search pattern to the default setup: one line with all values set to don't care. When you touch this soft key, PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT) is displayed at the top of the screen. The pattern is not cleared until you press the X key on the front panel.

<sup>1</sup> Octal-Hex-ASCII and Octal-Hex-EBCDIC conversion charts are included in Section 8.

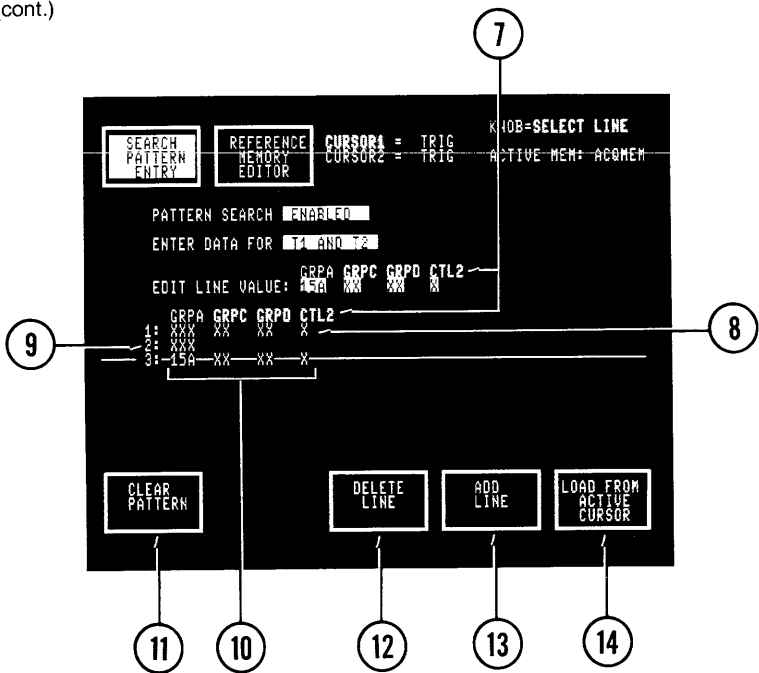


- 1 Location of the data cursors. The active cursor is highlighted.
- 2 Active Memory. Reminder of which memory (ACQMEM or REFMEM) was last displayed. This information is important when you use the LOAD FROM ACTIVE CURSOR soft key.
- 3 PATTERN SEARCH **ENABLED/DISABLED**. If you select **ENABLED**, the search pattern is compared to stored data. View the results of the comparison in the DATA menu with the HIGHLIGHT: **PATTERNS** selection. If you select **DISABLED**, the pattern feature does not operate.
- 4 Timebase(s) associated with the EDIT LINE VALUE. Displayed only if timebases T1 and T2 are active; selections are **T1 ONLY**, **T2 ONLY**, **T1 AND T2**.
- 5 Value (in input radices) of the pattern line at the location of the search data cursor. Use the data entry keys to enter new values. As you make changes, the new values are displayed in the pattern line (in output radices).
- 6 Search Data Cursor. Move this cursor with the SCROLL knob. The value of the pattern line at the location of the cursor is displayed in the EDIT LINE VALUE field.

(cont.)

**Figure 6-1. Sample Search Pattern Entry menu display.** A search pattern consists of 1 to 8 lines of data in State Table format. The pattern in this display will match any three consecutive memory locations where the second location has only T1 data, and the third location has 15A in GPRA.

(cont.)



- 7 Group names. Groups associated with timebase T2 are highlighted.
- 8 This pattern line matches any value, including no data.
- 9 This pattern line matches any memory location with only T1 data; it will not match any location with T2 data.
- 10 This line matches any memory location with the specified T1 data. The pattern will not match if this location does not immediately follow a location with only T1 data (see callout 9).
- 11 Returns the search pattern to the default setup: one line with all values set to don't care. PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT) is displayed at the top of the screen when you touch this soft key. The pattern is not cleared until you press the X key.
- 12 Deletes the line at the location of the search data cursor.
- 13 Adds a new line to the pattern below the position of the search data cursor. The new line has the same data as the preceding line. The search data cursor moves down to the new line.
- 14 Loads the EDIT LINE VALUE with the same data as the location in active memory where the active data cursor is positioned.

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Figure 6-1. Sample Search Pattern Entry menu display (cont.).

**DELETE LINE.** Touch this soft key to delete the line at the location of the search data cursor. Deleting the only line in a pattern is the same as touching the CLEAR PATTERN soft key.

**ADD LINE.** Touch this soft key to add a new line to the pattern below the position of the search data cursor. The new line will have the same data as the preceding line. The search data cursor moves down to the new line and its value appears in the EDIT LINE.

**LOAD FROM ACTIVE CURSOR.** Touch this soft key to load the EDIT LINE with the same data as the location in active memory where the active data cursor is positioned. Active memory is the type of memory last displayed. For example: if you want a value from reference memory to be part of the pattern, the active data cursor must be positioned on that location and reference memory must be the last memory displayed. A line at the top of the menu shows whether acquisition memory (ACQMEM) or reference memory (REFMEM) is active (see callout 2 in Figure 6-1). The cursor display at the top of the menu shows the locations of data cursors 1 and 2; the active cursor is highlighted. (Refer to Section 5 for a complete description of the data cursors.)

This operation lets you build patterns from data in memory without writing down or trying to remember the data. (Select PATTERN SEARCH **DISABLED** while you are building the pattern to keep the pattern from being applied every time you switch to the DATA displays to move the active data cursor. Enable pattern search when the pattern is complete.)

## REFERENCE MEMORY EDITOR

Use this menu to change data values in reference memory. You can also move the trigger event to a different location. It is not possible to add or delete locations, change channel values to don't care, or change the number or type of timebases for which data is valid.

Reference memory locations are displayed in the center of the menu <sup>2</sup> (see Figure 6-2) using the output radices specified in the Channel Grouping menu. Only locations around the active data cursor are displayed. The active cursor is controlled in this menu just like it is in the State Table or Timing Diagram: move the cursor with the SCROLL knob, and change the active role to the other cursor with the CHANGE ACTIVE CURSOR soft key. The cursor display at the top of the menu shows the locations of cursors 1 and 2 and the distance between them (CURSOR Δ);<sup>3</sup> the active cursor is highlighted.

The EDIT LINE VALUE (see callout 1 in Figure 6-2) shows the value of the memory location at the position of the active cursor. The value is displayed in the input radices specified for each group. If the input and output radices are different for a channel group, the text for that group in the EDIT LINE VALUE will be different from the text shown in the memory location, even though the value is the same.

Use the data entry keys to make changes in the EDIT LINE VALUE. As you make changes, the location in reference memory is updated. Don't care (X) is not a valid entry. The glitch symbol (◆) is valid only for 9-channel card groups assigned T1 ASYNC, and when glitch storage is enabled in the Memory Config menu.

With certain grouping setups, all channels cannot be displayed on the EDIT LINE VALUE at once. In these cases, the truncation symbol (▶) will be displayed. Move the truncated channels onto the screen with the cursor keys. If the reference memory data is truncated, you must change the display radix of one or more channel groups to see the truncated data.

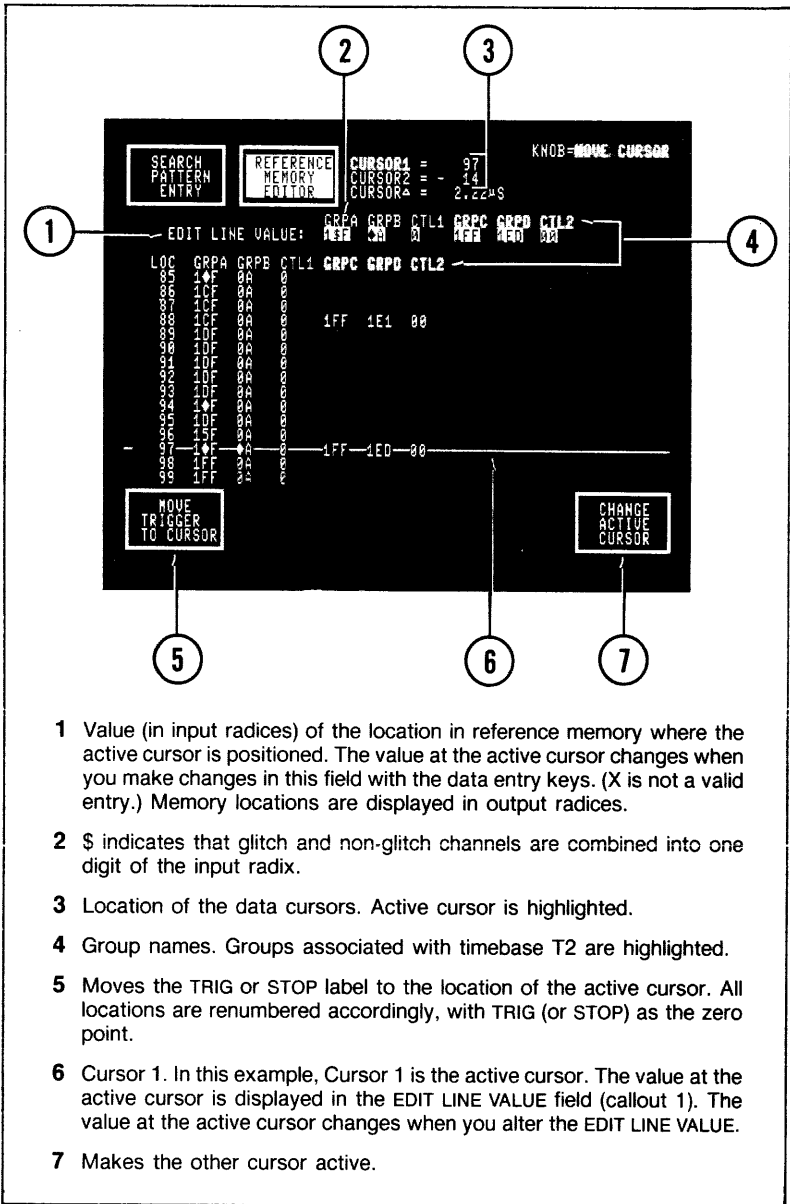
The MOVE TRIGGER TO CURSOR soft key transfers the TRIG or STOP <sup>4</sup> label to the location of the active cursor. The new TRIG or STOP location is the zero point, and all other locations are renumbered accordingly. This operation does not rearrange memory locations; it renumbers them from a new starting point. This feature is useful when you want to change the trigger to other data in reference memory, then use the COMPARE ACQMEM TO REFMEM Auto-Run condition to compare data around the new trigger. It is also useful when you want to highlight memory differences with the memories aligned at a new location.

---

<sup>2</sup> Reference memory is not displayed if the memory width vs. depth and pod-timebase selections in effect when the memory was stored are not the same as the selections in the current setup. Refer to *Memory Configuration Requirements* in Section 5 for more information.

<sup>3</sup> Refer to *Data Scrolling and Cursor Control* in Section 5 for more information about CURSOR Δ.

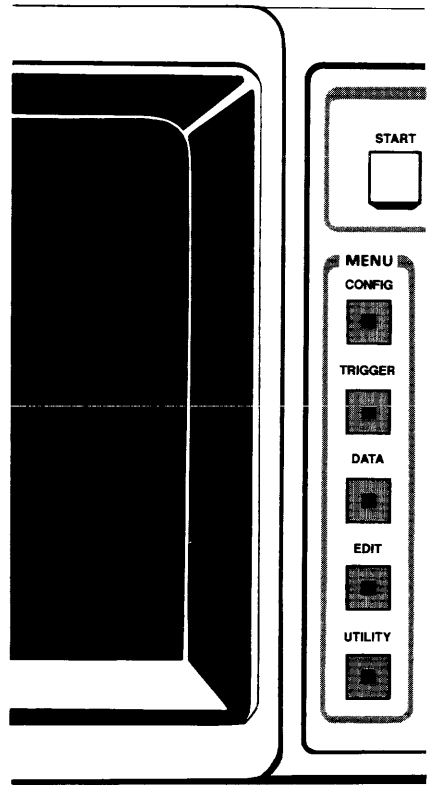
<sup>4</sup> If you press the STOP key before the trigger occurs, the last location in acquisition memory is labeled STOP.



- 1 Value (in input radices) of the location in reference memory where the active cursor is positioned. The value at the active cursor changes when you make changes in this field with the data entry keys. (X is not a valid entry.) Memory locations are displayed in output radices.
- 2 \$ indicates that glitch and non-glitch channels are combined into one digit of the input radix.
- 3 Location of the data cursors. Active cursor is highlighted.
- 4 Group names. Groups associated with timebase T2 are highlighted.
- 5 Moves the TRIG or STOP label to the location of the active cursor. All locations are renumbered accordingly, with TRIG (or STOP) as the zero point.
- 6 Cursor 1. In this example, Cursor 1 is the active cursor. The value at the active cursor is displayed in the EDIT LINE VALUE field (callout 1). The value at the active cursor changes when you alter the EDIT LINE VALUE.
- 7 Makes the other cursor active.

**Figure 6-2. Sample Reference Memory Editor menu display.** This menu displays reference memory in State Table format. The EDIT LINE VALUE field lets you change the data at the location of the active cursor.

7



UTILITY

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**COMM PORT CONTROL**

(Refer to the documentation provided with the COMM pack for complete operating information.)

**ROM PACK MENU**

(Refer to the documentation provided with the ROM pack. Not all ROM packs provide menus.)

The UTILITY key lets you access the Storage Memory Manager menu. If a COMM pack is installed, a COMM Port Control menu is also available. Another menu may be available if a ROM pack is installed.



## STORAGE MEMORY MANAGER

### NOTE

*ROM and RAM packs can be installed or removed while power is on or off. If power is on, the Storage Memory Manager menu must be displayed on the screen, and you must press the LOAD NEW PACK soft key immediately after installing or removing the pack. This soft key ensures that the 1240 and 1241 Logic Analyzers use the pack properly. It also resets the logic analyzer for normal operation after a pack is removed. (If you are exchanging one pack for another, you only need to press LOAD NEW PACK once, after the second pack is installed.)*

This menu controls storage and retrieval of setups in nonvolatile memory and internal RAM, storage and retrieval of setups and reference memories in RAM packs, and retrieval of setups and reference memories from ROM packs.

Figure 7-1 describes the basic fields in the Storage Memory Manager menu when no pack is installed. Figure 7-2 describes the menu when a RAM pack is installed. Refer to *Options and Accessories* in Section 8 for a list of the ROM packs and nonvolatile RAM packs available for the 1240 and 1241 Logic Analyzers.

When you store a setup, all information from the following menus is included: Operation Level, Timebase, Memory Config, Channel Grouping, Trigger Spec, and Auto-Run Spec. Timing Diagram PAGE information is also stored with each setup.

### STORING FILES

Use the NEW FILE VALUES information at the top of the menu to identify the file to be stored. The FILENAME can be up to six characters; select each character individually with the SCROLL knob. The selection in the FILETYPE field describes the type of information to be stored: the current **SETUP**, the current contents of **ACQMEM**, or the current contents of **REFMEM**. (**ACQMEM** and **REFMEM** are selections only when a RAM pack is installed.) The STORED IN field lets you select the area of memory in which to store the file: **NVM** (nonvolatile memory), **RAM** (internal RAM), and **PACK** (available only if a nonvolatile RAM pack is installed).

Press the STORE NEW FILE soft key to store the file described by the NEW FILE VALUES fields. The soft key is displayed in reverse video until the operation is complete.

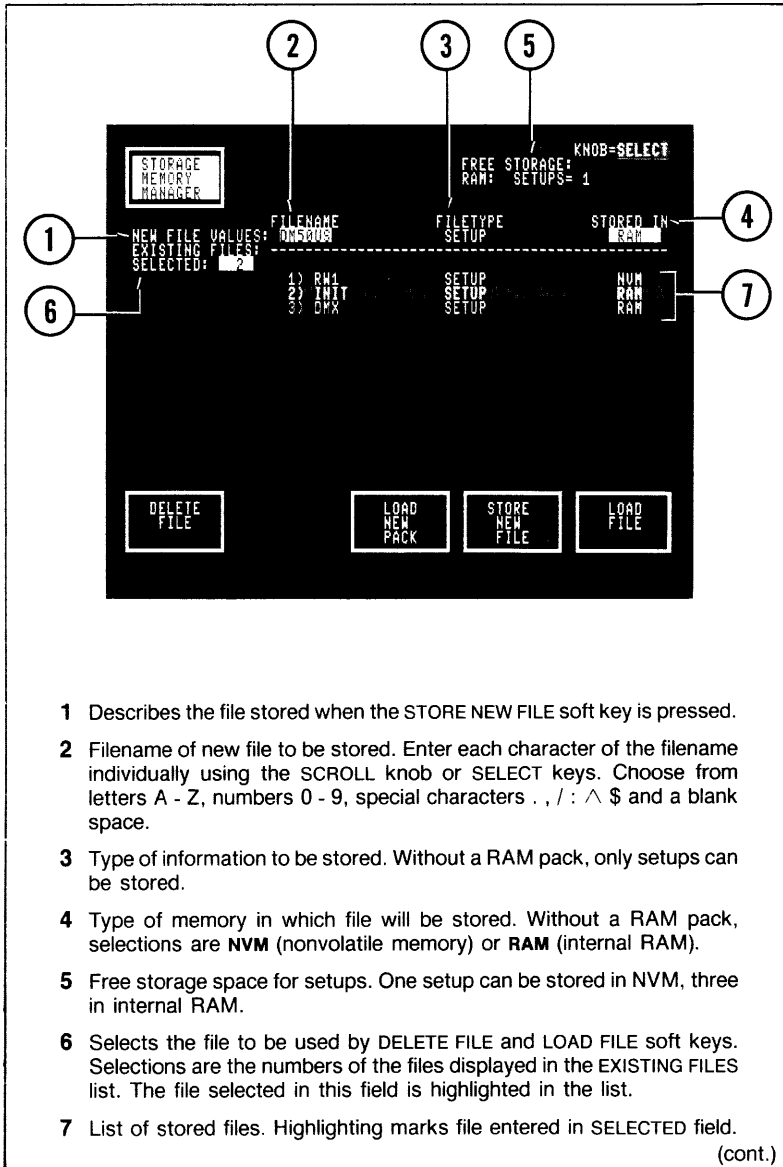
### RETRIEVING FILES

The EXISTING FILES list describes all stored files (see callout 7 in Figure 7-1). If a RAM or ROM pack is installed, files stored on the pack are included in the list (see Figure 7-2). Select the number of the file you want in the SELECTED field (notice that the description of the selected file is highlighted), then press the LOAD FILE soft key. After you press this key, the top line of the screen displays PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT). The file is not loaded until you press the X key. The soft key is displayed in reverse video until the operation is complete.

SETUP files change the current logic analyzer setup; REFMEM files are loaded into reference memory.

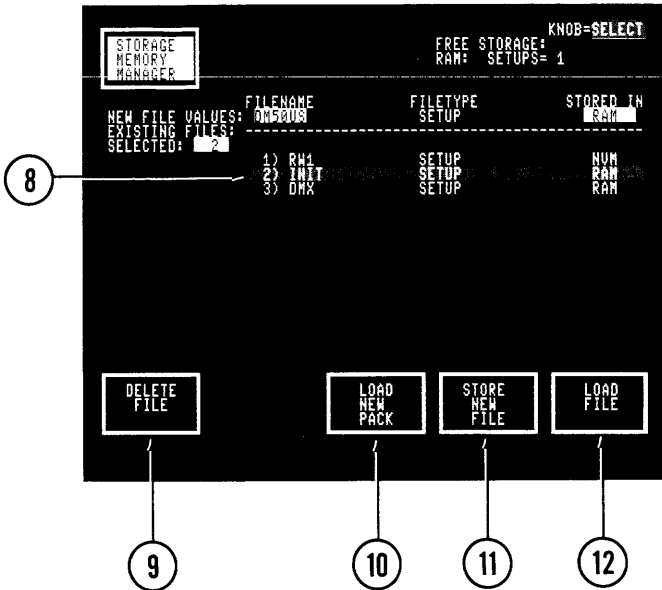
### INIT

When the logic analyzer is turned off or there is a power failure, the current setup is stored in nonvolatile memory. The next time the logic analyzer is powered up, this setup is labeled INIT and is transferred to internal RAM. At power-up, the default setup is in effect, but you can restore the previous setup by accessing this menu and loading INIT.



**Figure 7-1. Sample Storage Memory Manager display without a RAM or ROM pack.** The INIT file contains the setup in effect the last time the logic analyzer was powered down. To restore this setup, select the number of the INIT file in the SELECTED field then press the LOAD FILE soft key.

(cont.)



- 8 INIT is the setup that was in effect the last time the logic analyzer was powered down.
- 9 Deletes the selected file from memory. File is not deleted until you verify the operation by pressing the X key.
- 10 Resets the logic analyzer for normal operation after a pack is removed. **IMPORTANT:** If you install or remove a ROM or RAM pack while power is on, the Storage Memory Manager menu must be displayed on the screen. Touch LOAD NEW PACK immediately after installing or removing the pack.
- 11 Stores file described in NEW FILE VALUES (callout 1).
- 12 Loads selected file into the logic analyzer. The file is not loaded until you confirm the operation by pressing the X key.

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Figure 7-1. Sample Storage Memory Manager display without a RAM or ROM pack (cont.).

## NONVOLATILE MEMORY

The 1240 and 1241 Logic Analyzers automatically store the current setup in nonvolatile memory so that the last-used setup is not lost at power-down or during a power failure. (See the previous description of INIT for more information.) Besides the current setup, the logic analyzer can store one other setup in nonvolatile memory. Store the current setup in this memory space by selecting **NVM** in the STORED IN field then pressing the STORE NEW FILE soft key. If a file already exists in NVM and you press STORE NEW FILE for another file, the top line of the screen will display PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT). If you confirm the operation, the new file will overwrite the file previously stored in NVM.

## INTERNAL RAM

The logic analyzer can store three setups in an extended area of internal RAM. INIT takes up one of these so there is space for two of your setups. (INIT can be deleted if you need all the available storage space.) The amount of free RAM storage is displayed at the top of the menu (see callout 5 in Figure 7-1). This memory space is volatile; stored information is lost when the logic analyzer is powered down. To store a setup in internal RAM, select **RAM** in the STORED IN field.

If three setups are already stored in internal RAM and you press the STORE NEW FILE soft key for another setup, the message MEMORY FULL: DELETE AN EXISTING FILE FROM INTERNAL RAM is displayed at the top of the screen.

## EPROM PACKS

*If you install or remove an EPROM pack while power is on, the Storage Memory Manager menu must be displayed on the screen. Be sure to touch LOAD NEW PACK immediately after installing or removing the pack.*

You can use the Storage Memory Manager menu to load setups and reference memories into the logic analyzer from an EPROM pack. (Other special file types are possible; these types are determined by the pack.) A description of each file stored in the pack is displayed in the EXISTING FILES list. Each of these files is labeled PACK in the STORED IN column.

New files cannot be stored in an EPROM pack, and existing files cannot be deleted.

## RAM PACKS

*If you install or remove a RAM pack while power is on, the Storage Memory Manager menu must be displayed on the screen. Be sure to touch LOAD NEW PACK immediately after installing or removing the pack.*

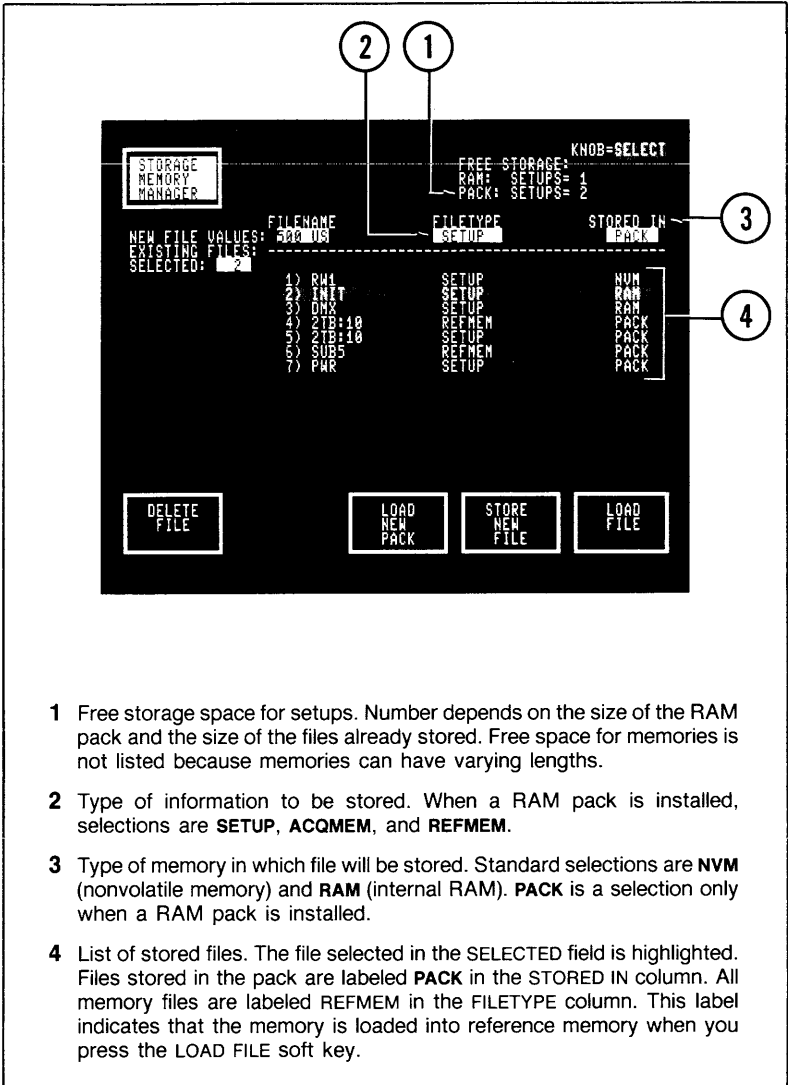
You can store, retrieve, or delete setups and memories from a RAM pack.<sup>1</sup>

Descriptions of the files stored in the pack are displayed in the EXISTING FILES list (see Figure 7-2). Each RAM pack file is labeled PACK in the STORED IN column.

When a pack is installed, the amount of free storage for setups is displayed at the top of the menu (see callout 1 in Figure 7-2). The number of setups that can be stored varies with the size of the RAM pack and the size of the files already stored. Free space for memories is not displayed because memories can vary in length.

Acquisition and reference memories can be stored in a RAM pack, but all memories are listed as REFMEMS in the EXISTING FILES list. The REFMEM label indicates that the file is loaded into reference memory when you press the LOAD FILE soft key. The file is not loaded until you verify the operation with the X key.

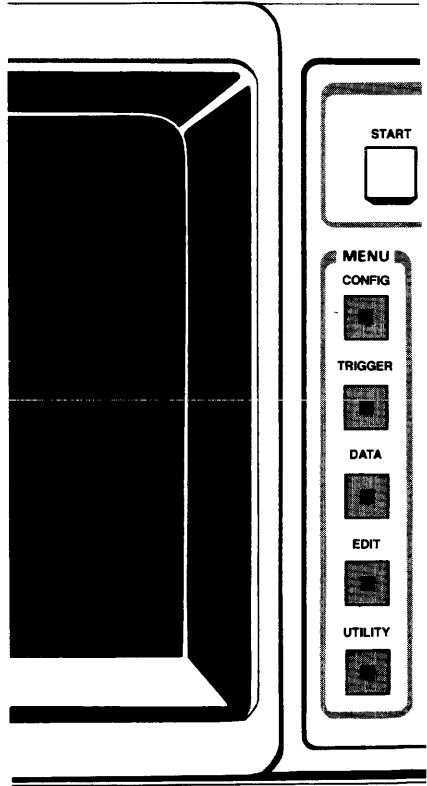
<sup>1</sup> ROM packs can provide other file types besides setups and memories (e.g., a file from a Performance Analysis ROM Pack). If a special file is stored in the logic analyzer from a previously-installed ROM pack, an appropriate selection is available in the FILETYPE field. This file can be stored in a RAM pack.



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**Figure 7-2. Sample Storage Memory Manager display when a RAM pack is installed.** A RAM pack allows you to store, retrieve, and delete setups and memories. **IMPORTANT:** If you install or remove a RAM pack while power is on, the Storage Memory Manager menu must be displayed on the screen. Touch **LOAD NEW PACK** immediately after installing or removing the pack.

8



REFERENCE  
INFORMATION

REFERENCE  
INFORMATION

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## EFFECTS OF MENU CHANGES

The 1240 and 1241 Logic Analyzers do not allow illegal setup conditions to exist. As a result, changes you make in one menu may affect selections available in other menus. Tables 8-1 to 8-4 list the crucial changes and their effects.

The logic analyzer changes entries in other menus only when you **exit** the altered menu. If you make a change then reverse it before leaving the menu, no change is made to other menus.

**Table 8-1**  
**EFFECTS OF CHANGES TO THE OPERATION LEVEL MENU**

If You Change:	EFFECTS ON OTHER MENUS ARE:
<p><b>To Level 0 from higher levels</b></p>	<p><b>MEMORY CONFIG:</b> Memory width vs. depth select fields are changed to fixed values that indicate no memory chaining. These values depend on the number of 9-channel and 18-channel acquisition cards installed; refer to Tables 3-1 and 3-2.</p> <p><b>TRIGGER SPEC:</b> The LOOK FOR TRIGGER field is not displayed. The logic analyzer will accept a trigger only after the required amount of pre-trigger data (determined by the TRIGGER POSITION field) has been acquired.</p>
<p><b>To Levels 0 or 1 from higher levels</b></p>	<p><b>TIMEBASE:</b> The ACTIVE TIMEBASES field is not displayed, and the logic analyzer uses only timebase T1. Timebase T2 fields are not displayed.</p> <p><b>MEMORY CONFIG:</b> The INPUT POD and TIMEBASE fields are changed to fixed values; no selections are available. T1 is assigned to all pods.</p> <p><b>CHANNEL GROUPING:</b> All groups are assigned T1.</p> <p><b>TRIGGER SPEC:</b> T1 is assigned to all levels of the sequential event recognizer, and the timebase select field in each sequence level is no longer displayed. WITH STORAGE fields are not displayed in the sequential event recognizer.</p> <p><b>SEARCH PATTERN ENTRY:</b> All lines of the pattern are set to T1, and the ENTER DATA FOR field is not displayed.</p>
<p><b>To Levels 0 or 2 from 1 or 3</b></p>	<p><b>TIMEBASE:</b> GLOBAL EVENT = <b>CLOCKED/UNCLOCKED</b> field is not displayed. Events are compared to the global event recognizer only if they coincide with a sample point (CLOCKED).</p> <p><b>TRIGGER SPEC:</b> The FILTER fields in both event recognizers are not displayed. To be recognized, an event must be present for at least one timebase period.</p>



**Table 8-2**  
**EFFECTS OF CHANGES TO THE TIMEBASE MENU**

If You Change:	EFFECTS ON OTHER MENUS ARE:
<b>Active Timebases</b>	MEMORY CONFIG: Each obsolete timebase assignment is changed to the legal value. For example: if you change ACTIVE TIMEBASE from <b>T1 AND T2</b> to <b>T2 ONLY</b> , all timebase assignments in Memory Config are changed to T2.
<b>Active Timebase to T1 ONLY</b>	MEMORY CONFIG: INPUT POD fields on the right side of the display are set to the odd-numbered pod.  CHANNEL GROUPING: All groups are assigned T1.  TRIGGER SPEC: T1 is assigned to all levels of the sequential event recognizer. The FILTER timebase in the global event recognizer is changed to T1.  SEARCH PATTERN ENTRY: All lines of the search pattern are set to T1.
<b>Active Timebase to T2 ONLY</b>	MEMORY CONFIG: If T2 is SYNC, INPUT POD fields on the right side of the display are set to the odd-numbered pod.  CHANNEL GROUPING: All groups are assigned T2.  TRIGGER SPEC: T2 is assigned to all levels of the sequential event recognizer. All glitch entries are changed to don't care (X). The FILTER timebase in the global event recognizer is changed to T2.  SEARCH PATTERN ENTRY: All lines of the search pattern are set to T2.
<b>T1 to SYNC</b>	TRIGGER SPEC: All glitch entries are set to don't care.
<b>T2 to SYNC</b>	MEMORY CONFIG: All T2 L and T2 F timebase assignments are changed to T2.
<b>T2 to DEMUX</b>	MEMORY CONFIG: All T2 timebase assignments are changed to T2 L.
<b>T1 to ASYNC 10 NS when T1 and T2 are active</b>	TIMEBASE: T1 qualifier fields are not displayed. The logic analyzer does not support clock qualification for T1 when T1 and T2 are active and T1 is ASYNC 10 NS.
<b>T1 to ASYNC 10 NS when T1 ONLY is selected</b>	TRIGGER SPEC: WITH STORAGE fields in the sequential event recognizer are not displayed.
<b>GLOBAL EVENT field to UNLOCKED</b>	TRIGGER SPEC: All glitch entries in the global event recognizer are set to don't care (X).

**Table 8-3**  
**EFFECTS OF CHANGES TO THE MEMORY CONFIG MENU**

If You Change:	EFFECTS ON OTHER MENUS ARE:
<b>Memory width to a smaller number of channels</b>	<p>CHANNEL GROUPING: Deleted channels are removed from all groups.</p> <p>TRIGGER SPEC: Deleted channels are removed from both event recognizers.</p> <p>AUTO-RUN SPEC: If you are using the COMPARE ACQMEM TO REFMEM condition, the deleted channels are removed from the mask field.</p> <p>SEARCH PATTERN ENTRY: The deleted channels are removed from the search pattern.</p>
<b>Pod-Timebase assignments</b>	<p>TIMEBASE: If T1 is ASYNC with a 10 ns period and you assign T1 to any pod connected to an 18-channel card, the clock period is changed to 20 ns.</p> <p>CHANNEL GROUPING: If the pod-timebase change affects all channels in a group, the group is assigned the new timebase; no channels are deleted. If the change affects only some of the channels in a group, those channels are deleted from groups and appear in the UNUSED list.</p> <p>TRIGGER SPEC: If a pod's timebase assignment changes from an ASYNC to a SYNC timebase, all glitch entries for channels from that pod are changed to don't care (X). If the pod-timebase change affects only some of the channels in a group, those channels are deleted from both event recognizers.</p> <p>AUTO-RUN SPEC: If the pod-timebase change affects only some of the channels in a group, those channels are deleted from the MASK fields in COMPARE ACQMEM TO REFMEM.</p> <p>SEARCH PATTERN ENTRY: If the pod-timebase change affects only some of the channels in a group, those channels are deleted from all lines of the search pattern.</p>
<b>GLITCHES to OFF</b>	TRIGGER SPEC: All glitch entries are set to don't care.
<b>GLITCHES to ON</b>	TIMEBASE: If T1 is ASYNC with a period of 10 ns, the period is changed to 20 ns.

**Table 8-4**  
**EFFECTS OF CHANGES TO THE CHANNEL GROUPING MENU**

If You Change:	EFFECTS ON OTHER MENUS ARE:
<b>Group definition by deleting or re-arranging channels</b>	<p>TRIGGER SPEC: Event recognizer values for the affected channels are removed or rearranged to correspond to the new group definitions.</p> <p>AUTO-RUN SPEC: If you are using the COMPARE ACQ-MEM TO REFMEM condition, MASK field values for the affected channels are removed or rearranged.</p> <p>TIMING DIAGRAM: Channels that are deleted or moved in Channel Grouping are turned <b>OFF</b> in the Timing Diagram PAGE displays.</p> <p>SEARCH PATTERN ENTRY: Values for the affected channels are removed from, or rearranged in, all search pattern lines.</p>

**Table 8-5**  
**1240 & 1241 ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirements	Supplemental Information
SAFETY General		Complies with the requirements of UL 1244, IEC 348, and CSA 556B.
CRT		VDE (German X-radiation law).
PRIMARY POWER INPUT		
115 VAC operation		90 V - 132 V
230 VAC operation		180 V - 250 V
Frequency		48 to 63 Hz
Power		500 VA max., 7 A max.
1240 VIDEO OUT		Conforms to RS170
GLOBAL EVENT		Event consists of inputs from all groups.
Filter, global event UNLOCKED		An event is not recognized unless it is accepted by the global filter. These specifications are based on a logic analyzer equipped with P6460 Data Acquisition Probes.

**Table 8-5 (cont.)**  
**1240 & 1241 ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirements	Supplemental Information
GLOBAL EVENT (cont.) Separate 1240D1 and 1240D2 events When N = 1: min. guaranteed event accepted  When N = 2-16: max. guaranteed event rejected min. guaranteed event accepted  Mixed 1240D1 and 1240D2 events max. guaranteed event rejected min. guaranteed event accepted	Timebase period + 6 ns  $(N-1) \times T - 8 \text{ ns}$ $(N \times T) + 2 \text{ ns}$  $(N-1) \times T - 8 \text{ ns}$ $(N \times T) + 20 \text{ ns}$	N is value of FILTER field; selections are 1-16. T is value of ON field (filter timebase); selections are T1 (when T1 active), T2 (when T2 active), and 10NS.      N = 2-16 N = 1-16
Filter, global event CLOCKED  Accept 1240D1 &/or 1240D2 events	N x T	N is value of FILTER field; selections are 1-16. T is value of ON field (filter timebase) and selection (T1, T2, 10NS) is same as sample clock. Filtered event becomes valid on Nth contiguous valid acquisition event.  Combined 1240D1 and 1240D2 ASYNC acquisition requires additional 2 ns word width.
STORE ON action T1 event or T2 event T1 event and T2 event	clocked: Store data if event true for 20 ns or more.  Store data for a timebase if both events meet indiv. timebase spec. and the other timebase event is valid for 10 ns after storage clock.  40 ns	unclocked: Data valid $\pm 12 \text{ ns} - 20 \text{ ns}$ with respect to data clock  Data valid $\pm 12 \text{ ns} - 20 \text{ ns}$ with respect to data clock
RESET		Counter/timer reset takes 100 ns prior to restart.
TRIGGER		Trigger position is within one stored clock of event causing trigger. If reset and trigger occur together, a trigger occurs.  When AFTER MEMORY FULL is the trigger position, a trigger before memory is full causes a reset.  If the counter/timer causes a trigger at the same time that the sequential event causes a reset, the logic analyzer will trigger and the counter/timer will be set to 0.
COUNTER/TIMER COUNT mode INCR CNTR	One count per valid evt.	Range is 1 to 99,999,999,999 events
TIME mode TIME WHILE	Accuracy, start to stop: $\pm 20 \text{ ns}$	Timer value truncated to 4 digits. Filter clk. must equal sample clk.

**Table 8-5 (cont.)**  
**1240 & 1241 ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirements	Supplemental Information
SEQUENTIAL EVENT		
Filter, accept event	N x T	Event may consist only of groups assigned the same timebase. N is value of the FILTER field; selections are 1-16. T is the period of the active timebase for that level.
Sequence level execution rate	30 ns	Time after sequential event occurs before next level is allowed.
RESET action	40 ns	Reset from sequential event to timer not guaranteed if sequential event has SYNC timebase. Reset from sequential event to counter only guaranteed if both seq. and global events use same filter clock.
Storage qualification	30 ns	WITH STORAGE field; selections are ON and OFF.
TO OCCUR nnnn TIMES	One count per valid event	Count of valid evts. before seq. evt. is satisfied; range is 1 - 9,999.
Delay (nnnn CLOCKS)	Delays up to 9,999 system clocks	Count of clocks before sequential event is satisfied.
EXT TRIG OUT		
Vout high (open)		50 $\Omega$ source Z
Vout high (50 $\Omega$ )		3.8 V min.
Vout low (either)		1.9 V min.
		0.6 V max., at 7 mA
Pulse width		70 ns min., 120 ns max.
Delay; probe tip clock to trigger out		65 ns min. 90 ns max.
EXT TRIG IN		
Input resistance		1 M $\Omega$ $\pm$ 1%
Input capacitance		37 pF $\pm$ 5 pF
V-input, max.		$\pm$ 20 V
Acceptance window		Window length = 100 ns; window starts 50 ns after clock that causes trigger.
x1 Probes and 50 $\Omega$ terminated coax.		
Input threshold		1.4 V $\pm$ 100 mV
Minimum pulse ampl.		1.8 V high, 1.0 V low
Minimum pulse width		20 ns
x10 Probes		
Input threshold		1.4 V $\pm$ 500 mV
Minimum pulse ampl.		2.4 V high, 0.6 V low
Minimum pulse width		30 ns
Minimum slew rate		5 V/ $\mu$ s
Time between triggers for linked LAs		Slave trigger within 60 ns of master trigger
T2 DEMUX CONTROL		
Phase Delay between first phase (T2 F) and last phase (T2 L)	10 ns min.	Only first occurrence of next phase is valid. Successive clocks without an intervening alternate phase are ignored.

**Table 8-5 (cont.)**  
**1240 & 1241 ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirements	Supplemental Information
T2 DEMUX CONTROL (cont.) Phase delay between last phase (T2 L) and first phase (T2 F)	20 ns min.	
ASYNCH TIMEBASE		10 ns to 1 s in 1-2-5 increments (0.01% average accuracy)
TWO TIMEBASE CORRELATION Resolution of precedence between timebases.	10 ns	The LA can resolve the difference between a T1 and a T2 event if they occur 10 ns or more apart. If < 10 ns from each other, the timebase previously indicated as occurring first is indicated as occurring last.

**Table 8-6**  
**1240 & 1241 ENVIRONMENTAL SPECIFICATIONS**

Characteristic	Description
1240 Temperature Maximum operating Minimum operating Non-operating	+55°C -10°C -62°C to +85°C
1241 Temperature Maximum operating Minimum operating Non-operating	+50°C -0°C -55°C to +75°C
1240 Humidity	95% to 97% relative humidity (Five 24 hr. cycles at 30°C to 60°C, instrument must reside in ≤ 70% relative humidity for two hours before and during operation)
1241 Humidity	90% to 95% relative humidity (Five 24 hr. cycles at 30°C to 60°C, instrument must reside in ≤ 70% relative humidity for two hours before and during operation)
1240/1241 Altitude Operating Non-operating	4.5 km (15,000 ft.) 15 km (50,000 ft.)
1240 Vibration, operating Displacement Frequency range	0.64 mm (0.025 inch) 10 to 55 Hz
1241 Vibration, operating Displacement Frequency range	0.64 mm (0.025 inch) 10 to 55 Hz
1240/1241 Shock	30 G's, halfsine, 11 ms duration, 18 shocks total, 3 on each face

**Table 8-7**  
**1240 & 1241 PHYSICAL SPECIFICATIONS**

Characteristic	Description
1240 Weight	12.0 kg (26.5 lbs.)
1241 Weight	12.7 kg (28.0 lbs.)
1240/1241 Overall Dimensions	
Height (handle folded back)	19.7 cm (7.8 inches)
Width (including handle)	36.8 cm (14.5 inches)
Length (including protective front cover)	49.8 cm (19.6 inches)
Length (handle extended)	57.6 cm (22.7 inches)

**Table 8-8**  
**1240D1 ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirements	Supplemental Information
MEMORY CONFIGURATION		
Width		9 stored data channels; 1 non-stored clock/qualifier chan.
Depth		Glitches On / Glitches Off
no chaining		257           513
2 1240D1s chained		513          1025
3 1240D1s chained		769          1537
4 1240D1s chained		1025         2049
TIMEBASE GENERATION		
Clock Input		
Pulse Width	8 ns min.	
Period	20 ns min.	
Amplitude	± 350 mV min. above and below programmed threshold	Min. time between OR'd clks is 25 ns
Qualifier Input		
Setup time	11 ns max.	
Hold time	0 ns max.	Values based on 1240D1 equipped with P6460 Data Acquisition Probe. Single selected qualifier driven.
SYNCHRONOUS OPERATION		
Data, all channels		Uses signals specified by operator in Timebase menu. Can be used with all timebases.
Setup time	7 ns	Data word width = 14 ns min. Setup and hold values based on 1240D1 equipped with P6460 Data Acquisition Probe.
Hold time	0.5 ns with T1 sourced from same 1240D1 card	4 ns setup time for single channel driven
Amplitude	± 350 mV min. above and below programmed threshold	2 ns hold time if data acquired on one acq. card and clk. on the other.

**Table 8-8 (cont.)**  
**1240D1 ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirements	Supplemental Information
SYNC Events Global event for all channels  Sequential event for all channels		At max. SYNC rate, any input event meeting setup and hold times and min. word width. At max. SYNC rate, recognize any input event meeting setup and hold times and min. word width. Up to 14 different events, one per sequence level.
ASYNCHRONOUS OPERATION Data min. word width guar. to be sampled	Timebase period + 6 ns	Timebase period + 8 ns with 1240D2; N samples of word requires $(N \times T) + 6$ ns min. word width $((N \times T) + 8$ ns with 1240D2)
Glitch Capture Glitch width   Glitch amplitude	$\pm 350$ mV above and below programmed threshold	6 ns at threshold (single chan.) at max. glitch/data transition rate of 30 ns Glitch may be detected as both glitch & data if transition occurs within 2 ns of sample clk.
ASYNC Events Global event, all chans. min. data word width guar. to be sampled Clocked (1, 0, X, $\blacklozenge$ ) Unclocked (1, 0, X)	Timebase period + 6 ns  16 ns min.	N samples of word requires $(N \times T) + 6$ ns min. word width $((N \times T) + 8$ ns with 1240D2) Timebase period + 8 ns with 1240D2 Min. width of valid event when global filter = 1 at 10NS and no 1240D2 channels specified
Sequential Event (1, 0, X)	Timebase period + 6 ns	Timebase period + 8 ns with 1240D2
PROBE THRESHOLD Threshold range   Accuracy	$\pm 0.5\% \pm 65$ mV	Selectable from +6.35 to -6.35 V in 50 mV increments; also includes preset values for TTL (+1.4 V), TPG (+3.70 V), -ECL (-1.30 V)

**Table 8-9**  
**1240D2 ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirements	Supplemental Information
MEMORY CONFIGURATION Width		18 stored data channels; 2 non-stored clock/qualifier chans.
Depth no chaining 2 1240D2s chained 3 1240D2s chained 4 1240D2s chained		513 1025 1537 2049



**Table 8-9 (cont.)**  
**1240D2 ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirements	Supplemental Information
<b>TIMEBASE GENERATION</b> Clock Input Pulse Width Period Amplitude	8 ns min. 20 ns min. $\pm 350$ mV min. above and below programmed threshold	Min. time between OR'd clocks is 25 ns
<b>Qualifier Input</b> Setup time Hold time	11 ns max. 0 ns max.	Single, selected qualifier driven. Values based on 1240D2 equipped with P6460 Data Acq. Probes.
<b>SYNCHRONOUS OPERATION</b> Data, all channels Setup time Hold time Amplitude	12 ns 0 ns $\pm 350$ mV min. above and below programmed threshold	Uses signals specified by operator in Timebase menu. Can be used with all timebases. Setup and hold values based on a 1240D2 equipped with P6460 Data Acqui- sition Probes.
<b>SYNC Events</b> Global event for all channels Sequential event for all channels		At max. SYNC rate, any input event meeting setup and hold times. At max. SYNC rate, recognize any input event meeting setup and hold times. Up to 14 different events, one per sequence level.
<b>ASYNCHRONOUS OPERATION</b> Data min. word width guaranteed to be sampled	Timebase period + 6 ns	Timebase period + 8 ns with 1240D1; N samples of word re- quires $(N \times T) + 6$ ns min. word width $((N \times T) + 8$ ns with 1240D1)
<b>ASYNCH Events</b> Global evt., all chans. min. data word width guar. to be sampled Clocked (1, 0, X) Unclocked (1, 0, X)	Timebase period + 6 ns 16 ns min.	N samples of word requires $(N \times T) + 6$ ns min. word width $((N \times T) + 8$ ns with 1240D2) Data stored may be different than that recognized by event recogni- zer; Timebase period + 8 ns with 1240D1 Minimum width of valid event when global filter = 1 at 10NS and no 1240D1 channels specified
<b>Sequential Event</b> (1, 0, X)	Timebase period + 6 ns	Timebase period + 8 ns with 1240D1
<b>PROBE THRESHOLD</b> Threshold range Accuracy	$\pm 0.5\% \pm 65$ mV	Selectable from +6.35 to -6.35 V in 50 mV increments; also includes preset values for TTL (+1.4 V), TPG (+3.70 V), -ECL (-1.30 V)

## ERROR AND PROMPT MESSAGES

ALL AVAILABLE LEVELS ARE DEFINED: CHANGE AN EXISTING LEVEL	You tried to use the ADD LEVEL soft key when all 14 sequence levels are defined.
ALL AVAILABLE LOCATIONS DEFINED: CHANGE AN EXISTING LOCATION	You tried to add a new line to the search pattern when all eight lines (maximum) are already defined.
APPLYING SEARCH PATTERN — PLEASE WAIT	This message is displayed whenever the search pattern is applied to memory. The function can take several seconds to complete.
CANNOT EDIT AN EMPTY REFMEM	This message is displayed when you try to access the Reference Memory Editor menu when the current REFMEM contains no data.
	The following five error messages can occur whenever you display ACQMEM or REFMEM, use the COMPARE ACQMEM TO REFMEM Auto-Run condition, or press the LOAD FROM ACTIVE CURSOR soft key.
CONFIG ERROR: (ACQMEM/REFMEM) ABSENT MEMORIES ARE (list of pod numbers)	Memory to be displayed was downloaded from a ROM or RAM pack or from a remote controller, and was acquired on a logic analyzer configured differently than the current instrument setup. Pod numbers listed correspond to the unused memory segments in the downloaded memory. (Refer to <i>Memory Width vs. Depth</i> in Section 3 for a definition of memory segment.) The downloaded memory cannot be displayed unless the LA's configuration is changed.
CONFIG ERROR: (ACQMEM/REFMEM) 9 CHANNEL CARDS ARE (width) BY (depth)	Memory to be displayed was stored with different 9-channel width vs. depth parameters than the current instrument setup.
CONFIG ERROR: (ACQMEM/REFMEM) 18 CHANNEL CARDS ARE (width) BY (depth)	Memory to be displayed was stored with different 18-channel width vs. depth parameters than the current instrument setup.
CONFIG ERROR: (ACQMEM/REFMEM) T1 MEMORIES ARE: (list of pod numbers)	Memory to be displayed was stored with different T1-pod assignments than the current instrument setup.
CONFIG ERROR: (ACQMEM/REFMEM) T2 MEMORIES ARE: (list of pod numbers)	Memory to be displayed was stored with different T2-pod assignments than the current instrument setup.
DIRECTORY FULL: DELETE AN EXISTING FILE FROM THE RAM PACK	This message is displayed when the area of the RAM pack reserved for storing file names is full, and you tried to store another file.

(cont.)

DON'T CARE INVALID IN THE REFMEM	Don't care (X) is not a valid character in the Reference Memory Editor menu.
GLITCH CAPTURE NOT ENABLED	You cannot enter a glitch symbol in the Trigger Spec or Search Pattern Entry menus when <b>GLITCHES OFF</b> is selected in the Memory Config menu. You cannot edit a glitch into reference memory if <b>GLITCHES OFF</b> was selected when the REFMEM data was acquired.
GLITCH INVALID IN A MASK FIELD	The glitch symbol is not a valid entry for the MASK fields in the COMPARE ACQMEM TO REFMEM Auto-Run condition.
GLITCH INVALID ON 18-CHANNEL CARD	You tried to enter the glitch symbol for a channel acquired by an 18-channel card. An 18-channel card cannot acquire glitches.
GLITCH INVALID WITH SYNCHRONOUS TIMEBASE	You tried to enter the glitch symbol for a group that is assigned a synchronous timebase.
GLITCH INVALID WITH UNLOCKED GLOBAL EVENT RECOGNIZER	You tried to enter the glitch symbol in the global event recognizer when GLOBAL EVENT = <b>UNLOCKED</b> is selected in the Timebase menu.
GROUP FULL: CANNOT INSERT CHANNEL	You touched INSERT CHANNEL for a group that already has the maximum of 36 channels.
HIGHLIGHTING OFF	You touched NEXT HIGHLIGHT DATA but the HIGHLIGHT field is set to <b>OFF</b> .
INVALID CHANNEL NUMBER	You tried to enter a value other than 0-8 or X in a CHAN field.
INVALID CHECKSUM: PACK IGNORED	The verification routine that runs when you press the LOAD NEW PACK soft key found a checksum error in the newly installed ROM pack.
INVALID CHECKSUM: "X" INIT'S PACK, ANY OTHER HARD KEY IGNORES IT	When you install a RAM pack and touch the LOAD NEW PACK soft key, this message is displayed if the pack verification routine detects a checksum error. Press X to clear and format the pack for use. This message is normal when a new, unused RAM pack is installed.
INVALID INPUT FOR BINARY RADIX INVALID INPUT FOR OCTAL RADIX	You tried to enter a digit too large for the selected radix. Valid binary values are 0 and 1; valid octal values are 0-7.
INVALID INPUT FOR PARTIAL DIGIT	You entered a number too large to fit in the number of bits remaining in the digit. For example: if a group is made up of 10 channels and the input radix is HEX, the input fields for this group will have three digits. The largest value you can enter is 3FF. If you try to enter 4-F for the high-order digit, this error message is displayed.

(cont.)

INVALID OPERATION: FILE TYPE NOT RECOGNIZED	You can store special file types (created by ROM packs) into a RAM pack. This message is displayed when you try to load a special file from a RAM pack and the logic analyzer no longer contains the internal parameters set up by the ROM pack to use the special file. Refer to the ROM pack manual for complete details.
INVALID OPERATION: FILES CANNOT BE DELETED FROM A ROM PACK	You tried to delete a file stored in a ROM pack. New files cannot be added to ROM packs, and existing files cannot be deleted.
INVALID OPERATION: NO FILES TO (DELETE/LOAD)	You touched LOAD FILE or DELETE FILE in the Storage Memory Manager menu when there were no files in the EXISTING FILES list.
INVALID POD NUMBER	The number you tried to enter in the POD field corresponds to a pod that either does not exist, is not assigned to the type of card you are building groups for, or has a different timebase than that already defined for the group.
INVALID SETUP: INCONSISTENT DATA OR HARDWARE REQUIREMENTS	Before a setup is loaded into the logic analyzer from a ROM or RAM pack, it is tested for certain conditions. This message is displayed when you press LOAD FILE and the setup does not pass the verification tests. This might happen if the setup is based on a different LA configuration or if the file is corrupt.
MEMORY FULL: DELETE AN EXISTING FILE FROM ....	You pressed the STORE NEW FILE soft key and there is not enough storage space remaining in the selected storage area.
MEMORIES CAN ONLY BE STORED INTO A RAM PACK	You pressed STORE NEW FILE in the Storage Memory Manager menu with a FILETYPE of ACQ-MEM or REFMEM, but the selection in the STORED IN field was not PACK.
MOVE FIELD CURSOR TO A CHANNEL SELECTION FIELD	You touched DISPLAY NEXT CHANNEL in the Timing Diagram when the field cursor was not in a channel selection (trace name) field.
MOVE FIELD CURSOR TO A GROUP DEFINITION FIELD	You pressed CLEAR GROUP with the field cursor positioned on the CARD TYPE field.
MOVE FIELD CURSOR TO A POD OR CHAN FIELD	You tried to use DELETE CHANNEL, ADD NEXT CHANNEL, or INSERT CHANNEL when the field cursor was not on a POD or CHAN field.
MOVE FIELD CURSOR TO A SEQUENCE LEVEL	You tried to delete a level of the sequential event recognizer when the field cursor was not positioned in a level.
MOVE FIELD CURSOR TO AN ASSIGNED CHANNEL	You touched the ADD NEXT CHANNEL soft key when the field cursor was positioned on an undefined channel (POD and/or CHAN value of X).

(cont.)

MOVE FIELD CURSOR TO AN EVENT RECOGNIZER GROUP FIELD	You touched LOAD FROM ACTIVE CURSOR in the Trigger Spec menu when the field cursor was not positioned in an event recognizer value field.
NO DATA TO EDIT IN CURRENT GROUPING	This message is displayed in the Reference Memory Editor menu when the logic analyzer has acquired data but has no grouping information for those channels and, therefore, cannot display the data.
NO GROUPS DEFINED: CANNOT EXIT MENU	You cannot exit the Channel Grouping menu if all groups are unspecified (all channels in the UN-USED list).
NO HIGHLIGHTED LOCATIONS OCCUR	You touched NEXT HIGHLIGHT DATA and no data meeting the highlight requirements was found.
NO SUCCESSOR TO CHANNEL 0	You tried to add another channel to a group with the ADD NEXT CHANNEL soft key when the field cursor was positioned on a CHAN value of 0.
NO VALID DATA ACQUIRED	This error message and blank display can be caused by either of these reasons: <ol style="list-style-type: none"> <li>1. No data was acquired; acquisition memory is empty. This can occur if the sampling clock is SYNC and no clocks occur. It can also occur if you use clock and/or storage qualification to reject all clocks and/or data.</li> <li>2. Current clock setup violates the logic analyzer's clock specifications. (Data is acquired, but it is not valid.) For example: The clock specifications are violated when you clock the LA faster than 20 ns SYNC. The clock specifications can also be violated if you change the card threshold during the COMPARE ACQMEM TO REFEMEM Auto-Run mode, and the clock line is noisy.</li> </ol>
OPERATION IN PROGRESS — PLEASE WAIT	This message is displayed when you store or load a memory file in the Storage Memory Manager menu. Storing and loading operations can take several seconds to complete.
PATTERN SEARCH DISABLED	You selected pattern highlighting in the State Table or Timing Diagram but the PATTERN SEARCH <b>DISABLED</b> selection is currently in effect in the Search Pattern Entry menu.
PRESS "STOP" TO TERMINATE ACQUISITION	The five MENU keys and STOP are the only valid key inputs while the logic analyzer is acquiring data. When you press one of the MENU keys, acquisition stops, and the LA displays the last menu accessed in that menu group. When you press STOP, acquisition stops, and the LA displays data in state table or timing diagram format. During COMPARE ACQMEM TO REFEMEM status display operations, only STOP is valid.

(cont.)

PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT)	This is not an error message. It is displayed when you touch a soft key that requires verification before the action is taken.
SELECTED FILETYPE CAN ONLY BE STORED INTO A RAM PACK	The file to be stored is an ACQMEM, REFMEM, or special file type (from a previously-installed ROM pack) but the selected storage area is not <b>PACK</b> . Nonvolatile memory and internal RAM can store only instrument setups; memories and other special file types can only be stored in a RAM pack.
UNKNOWN PACK TYPE: PACK IGNORED	The verification routine that runs when you touch the LOAD NEW PACK soft key did not recognize the newly installed ROM pack as a valid logic analyzer pack. This occurs if the ROM pack is not a 1240/1241 pack, or if it is defective.
UNKNOWN RAM PACK: "X" INITIS PACK, ANY OTHER HARD KEY IGNORES IT	When you install a RAM pack and touch the LOAD NEW PACK soft key, this message is displayed if the pack verification routine cannot identify the pack. Press the X key on the front panel to clear and format the pack for use. This message is normal when a new, unused RAM pack is installed.
USE 0-9	You tried to enter a non-decimal value into a decimal field.
USE 0 OR 1	You tried to enter a number other than 0 or 1 in a POLARITY field.
USE 1-E	You tried to enter something besides 1-E in the TO LEVEL field (displayed when JUMP IF/JUMP IF NOT is selected in the sequential event recognizer).
USE SELECT KEYS	You tried to use the data entry keys to enter a value into a field controlled by the SELECT keys.
WARNING: 10 NS INVALID - GLITCH ENABLED and/or 18 CHANNEL CARD USES T1	The 10 NS selection for T1 ASYNC is not available because glitch storage is enabled in the Memory Config menu, and/or an 18-channel card is assigned to T1. For 10 ns acquisition, glitch storage must be disabled, and all 18-channel cards must be assigned T2. Refer to <i>10 ns Acquisition</i> in Section 3 for more information.
WARNING: JUMP TO UNDEFINED LEVEL CAUSES TRIGGER	You entered the number of a level not currently defined in the sequential event recognizer into the TO LEVEL field (displayed when JUMP IF/JUMP IF NOT is selected).
WARNING: MAXIMUM VALUE USED	This message is displayed if you try to enter too large a numeric value into certain fields. The logic analyzer sets the field to its maximum value.

(cont.)

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WARNING: MINIMUM VALUE USED	You tried to enter a numeric value that was lower than the acceptable minimum for a field. The logic analyzer sets the field to its minimum value.
WARNING: SETUP INFORMATI- ON IN OTHER MENUS WILL BE LOST	This message is displayed when you change the Operation Level to a lower number and the existing setup was specified under a higher number. Refer to Table 8-1 for a description of the possible changes.
WARNING: T1 STORAGE QUALIFICATION DISABLED AT 10 NS	This message is displayed in the Trigger Spec menu when T1 is ASYNC 10 NS, and you select STORE in the global event recognizer. The logic analyzer does not support storage qualification for T1 channels at 10 ns. At 10 ns, all T1 data is stored.

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## DIFFERENCES BETWEEN OPERATION LEVELS

Table 8-10  
DIFFERENCES BETWEEN THE OPERATION LEVELS

Level	Timebase Menu	Memory Config Menu	Trigger Spec Menu
0	Only T1  CLOCKED/UNCLOCKED not displayed	No Chaining	LOOK FOR TRIGGER and FILTER fields not displayed.  WITH STORAGE fields not displayed in se- quential event recog- nizer.
1	Only T1	Full Operation	WITH STORAGE fields not displayed in se- quential event recog- nizer.
2	T1 , T2 CLOCKED/UNCLOCKED not displayed	Full Operation	FILTER fields not displayed.
3	Full Operation	Full Operation	Full Operation



## TEST PATTERN GENERATOR INFORMATION

The 1240 and 1241 Logic Analyzer's test pattern generator (TPG) simulates a data source by sending a data pattern of 63 unique values to the two sets of pins located above the probe connections on the right side panel of the instrument. A different pattern is available from both TPG outputs; these patterns are listed below in Tables 8-11 and 8-12.

The TPG MODE field in the Operation Level menu (see Section 3) lets you select how the patterns will be clocked and whether the patterns will contain glitches. Table 8-13 describes the characteristics of the different TPG modes. Mode 0 is the power-up default. Figures 8-1 and 8-2 explain the clock and data outputs for the different modes.

When you acquire data from the TPG, you must set the THRESHOLD fields for the cards connected to the TPG outputs to **TPG**. This selection sets the card input threshold to +3.70 V, to correspond with the TPG output levels.

### NOTE

*The TPG can only be used with the P6460 Data Acquisition Probe.*

*The TPG is only guaranteed to operate properly within the temperature range +20° C to +30° C.*

**Table 8-11**

**TPG PATTERN FROM LEFT CONNECTOR**

1FF	1AE	071	186
1BE	15D	0A2	10C
17D	0FB	145	018
0BA	1B6	0CB	030
175	16D	1D7	061
0AA	09A	1EF	082
155	134	19E	104
0EB	069	13C	008
196	092	079	010
12C	124	0B2	020
059	049	165	041
0F3	0D3	08A	0C3
1A6	1E7	114	1C7
14D	18E	028	1CF
0DB	11C	051	1DF
1F7	038	0E3	

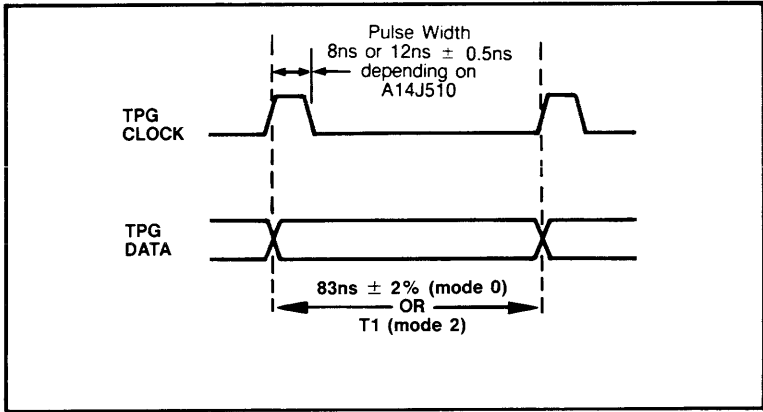
**Table 8-12**

**TPG PATTERN FROM RIGHT CONNECTOR**

1FF	175	18E	030
1F7	0EB	114	061
1EF	1DF	028	0C3
1D7	1B6	059	186
1AE	16D	0BA	10C
155	0D3	17D	010
0AA	1A6	0F3	020
15D	14D	1E7	041
0B2	092	1CF	082
165	124	196	104
0CB	049	12C	008
19E	09A	051	018
134	13C	0A2	038
069	071	145	079
0DB	0E3	08A	0FB
1BE	1C7	11C	

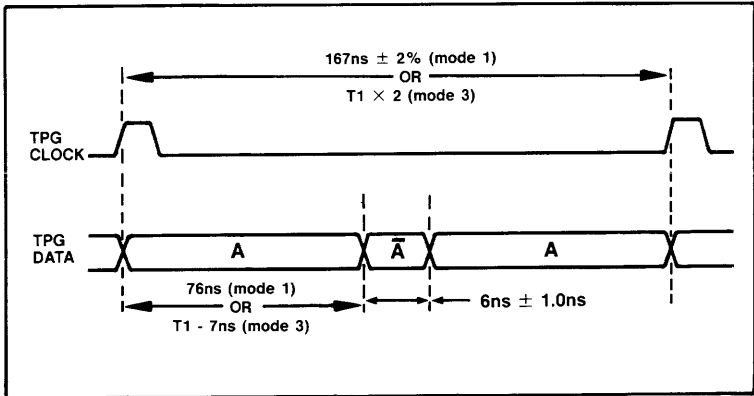
**Table 8-13**  
**TPG MODES**

Mode	With Glitches	Clocked At
0	No	12 MHz
1	Yes	6 MHz
2	No	T1
3	Yes	T1 ÷ 2



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**Figure 8-1. Mode 0 and mode 2 TPG outputs.** In mode 0, the clock is derived from a 12 MHz oscillator which is internal to the TPG. In mode 2, the clock source is timebase T1 (specified in the Timebase menu); the TPG output is only valid when T1 is less than or equal to 50 MHz.



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**Figure 8-2. Mode 1 and mode 3 TPG outputs.** In mode 1, the clock is derived from a 12 MHz oscillator which is internal to the TPG. Alternate clock cycles are used to produce glitches, so the actual frequency of the output is 6 MHz. In mode 3, the clock source is timebase T1 (specified in the timebase menu) and the output period is  $T1 \times 2$ . The TPG output is only valid when T1 is less than or equal to 20 ns.

## OCTAL-HEX-ASCII CONVERSION CHART

OCT	HEX	ASC	OCT	HEX	ASC	OCT	HEX	ASC	OCT	HEX	ASC
000	00	NUL	040	20	SP	100	40	@	140	60	`
001	01	SOH	041	21	!	101	41	A	141	61	a
002	02	STX	042	22	"	102	42	B	142	62	b
003	03	ETX	043	23	#	103	43	C	143	63	c
004	04	EOT	044	24	\$	104	44	D	144	64	d
005	05	ENQ	045	25	%	105	45	E	145	65	e
006	06	ACK	046	26	&	106	46	F	146	66	f
007	07	BEL	047	27	'	107	47	G	147	67	g
010	08	BS	050	28	(	110	48	H	150	68	h
011	09	HT	051	29	)	111	49	I	151	69	i
012	0A	LF	052	2A	*	112	4A	J	152	6A	j
013	0B	VT	053	2B	+	113	4B	K	153	6B	k
014	0C	FF	054	2C	,	114	4C	L	154	6C	l
015	0D	CR	055	2D	-	115	4D	M	155	6D	m
016	0E	SO	056	2E	.	116	4E	N	156	6E	n
017	0F	SI	057	2F	/	117	4F	O	157	6F	o
020	10	DLE	060	30	0	120	50	P	160	70	p
021	11	DC1	061	31	1	121	51	Q	161	71	q
022	12	DC2	062	32	2	122	52	R	162	72	r
023	13	DC3	063	33	3	123	53	S	163	73	s
024	14	DC4	064	34	4	124	54	T	164	74	t
025	15	NAK	065	35	5	125	55	U	165	75	u
026	16	SYN	066	36	6	126	56	V	166	76	v
027	17	ETB	067	37	7	127	57	W	167	77	w
030	18	CAN	070	38	8	130	58	X	170	78	x
031	19	EM	071	39	9	131	59	Y	171	79	y
032	1A	SUB	072	3A	:	132	5A	Z	172	7A	z
033	1B	ESC	073	3B	;	133	5B	[	173	7B	{
034	1C	FS	074	3C	<	134	5C	\	174	7C	!
035	1D	GS	075	3D	=	135	5D	]	175	7D	}
036	1E	RS	076	3E	>	136	5E	^	176	7E	~
037	1F	US	077	3F	?	137	5F	_	177	7F	DEL

## OCTAL-HEX-EBCDIC CONVERSION CHART

OCT	HEX	EBC	OCT	HEX	EBC	OCT	HEX	EBC	OCT	HEX	EBC
000	00	NUL	100	40	SP	200	80		300	C0	{
001	01	SOH	101	41		201	81		301	C1	A
002	02	STX	102	42		202	82	a	302	C2	B
003	03	ETX	103	43		203	83	b	303	C3	C
004	04	PF	104	44		204	84	c	304	C4	D
005	05	HT	105	45		205	85	d	305	C5	E
006	06	LC	106	46		206	86	e	306	C6	F
007	07	DEL	107	47		207	87	f	307	C7	G
010	08	GE	110	48		210	88	g	310	C8	H
011	09	RLF	111	49		211	89	h	311	C9	I
012	0A	SMM	112	4A	. c	212	8A	i	312	CA	J
013	0B	VT	113	4B	<	213	8B		313	CB	K
014	0C	FF	114	4C	>	214	8C		314	CC	L
015	0D	CR	115	4D	(	215	8D		315	CD	M
016	0E	SO	116	4E	+	216	8E		316	CE	N
017	0F	SI	117	4F	!	217	8F		317	CF	O
020	10	DLE	120	50	&	220	90		320	D0	P
021	11	DC1	121	51		221	91	j	321	D1	Q
022	12	DC2	122	52		222	92	k	322	D2	R
023	13	TM	123	53		223	93	l	323	D3	
024	14	RES	124	54		224	94	m	324	D4	L
025	15	NL	125	55		225	95	n	325	D5	M
026	16	BS	126	56		226	96	o	326	D6	N
027	17	IL	127	57		227	97	p	327	D7	O
030	18	CAN	130	58		230	98	q	330	D8	
031	19	EM	131	59		231	99	r	331	D9	R
032	1A	CC	132	5A	!	232	9A		332	DA	
033	1B	CU1	133	5B	\$	233	9B		333	DB	
034	1C	IFS	134	5C	*	234	9C		334	DC	
035	1D	IGS	135	5D	)	235	9D		335	DD	
036	1E	IRS	136	5E	:	236	9E		336	DE	
037	1F	IUS	137	5F	;	237	9F		337	DF	
040	20	DS	140	60	-	240	A0		340	E0	\
041	21	SOS	141	61	/	241	A1	~	341	E1	/
042	22	FS	142	62		242	A2		342	E2	S
043	23		143	63		243	A3	s	343	E3	T
044	24	BYP	144	64		244	A4	t	344	E4	U
045	25	LF	145	65		245	A5	u	345	E5	V
046	26	ETB	146	66		246	A6	v	346	E6	W
047	27	ESC	147	67		247	A7	w	347	E7	X
050	28		150	68		250	A8	x	350	E8	Y
051	29		151	69		251	A9	y	351	E9	Z
052	2A	SM	152	6A	:	252	AA	z	352	EA	
053	2B	CU2	153	6B	;	253	AB		353	EB	
054	2C		154	6C	%	254	AC		354	EC	
055	2D	ENQ	155	6D		255	AD		355	ED	
056	2E	ACK	156	6E	\	256	AE		356	EE	
057	2F	BEL	157	6F	?	257	AF		357	EF	
060	30		160	70		260	B0		360	F0	0
061	31		161	71		261	B1		361	F1	1
062	32	SYN	162	72		262	B2		362	F2	2
063	33		163	73		263	B3		363	F3	3
064	34	PN	164	74		264	B4		364	F4	4
065	35	RS	165	75		265	B5		365	F5	5
066	36	UC	166	76		266	B6		366	F6	6
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## OPTIONS AND ACCESSORIES

### Options

- Option A1, Universal Euro Plug, 220V/6A
- Option A2, United Kingdom Plug, 240V/6A
- Option A3, Australian Plug, 240V/6A
- Option A4, North American Plug, 240V/10A
- Option A5, Switzerland Plug, 220V/6A

### Standard Accessories

- 1 Accessory Pouch, 016-0707-00
- 1 Operator's Manual, 070-4340-01
- 5 Reference Guides, 070-4641-01
- 1240 Seminar Workbook, 062-6926-00
- 1 Power Cord, 161-0104-00
- 1 Front Panel Cover, 200-2780-00
- 2 Diagnostic Lead Sets, 012-0556-00

### Optional Accessories

#### Acquisition Cards:

- 1240D1, 9-channel Acquisition Card and one P6460 acq. probe
- 1240D2, 18-channel Acquisition Card and two P6460 acq. probes

#### Data Acquisition Probes:

- P6460 Data Acquisition Probe
- P6462 Fixed Threshold TTL Acquisition Probe

#### Scope Probes:

- P6120 x1 Scope Probe, 010-6120-00
- P6105 x10 Encoded Scope Probe, 010-6105-00

#### COMMUNICATION PACKS:

- 1200C01, RS232C COMM Pack
- 1200C02, GPIB COMM Pack
- 1200C11, Parallel Printer COMM Pack

#### Memory Packs:

- 12RS01, Nonvolatile 8K RAM Pack
- 12RS02, Nonvolatile 64K RAM Pack
- 12RS11, 32K EPROM Pack (empty)
- 12RS12, 32K EPROM Pack (blank)

#### Documentation:

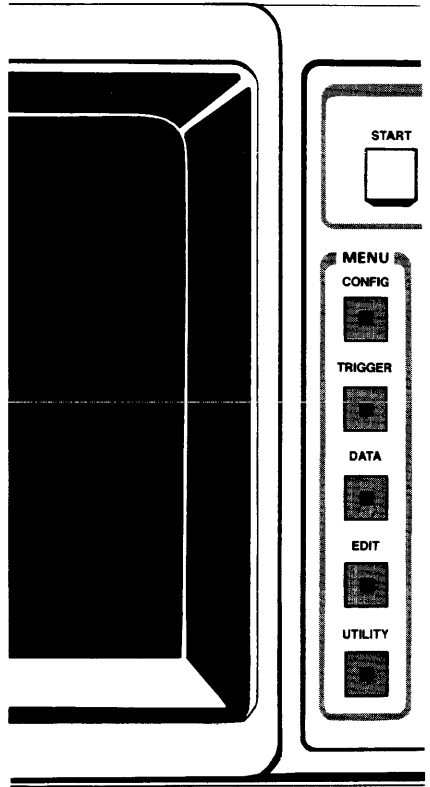
- Empty half-size binder for optional accessory documentation, 062-6927-00
- 1240 Microprocessor Analysis Workbook, 062-7470-00

#### Service Accessories:

- Service Maintenance Kit, 067-1103-03
  - includes: 1240 Service Manual with 1241 Service Addendum
  - 12RD01, 1240 Diagnostic ROM Pack
  - Diagnostic Lead Sets
  - Extender Cards
- 1240 Service Manual (two volumes), 062-7124-02
- 1241 Service Addendum, 070-5378-00
- 12RD01, 1240 Diagnostic ROM Pack
- Diagnostic Lead Set, 012-0556-00
- Trigger, Display, and Processor Extender Card, 670-7539-02
- Acquisition Extender Card, 670-8567-00

**ROM Packs:**

12R01, Performance Analysis ROM Pack  
12RC01, Printer Support ROM Pack  
12RC02, Master/Slave Support ROM Pack  
12RM01, 8080 Mnemonics ROM Pack  
12RM02, 8085 Mnemonics ROM Pack  
12RM03, 8086 Mnemonics ROM Pack  
12RM04, 8088 Mnemonics ROM Pack  
12RM05, 80186 Mnemonics ROM Pack  
12RM06, 80188 Mnemonics ROM Pack  
12RM21, 6800 Mnemonics ROM Pack  
12RM22, 6802 Mnemonics ROM Pack  
12RM23, 6808 Mnemonics ROM Pack  
12RM24, 6809 Mnemonics ROM Pack  
12RM25, 68000 Mnemonics ROM Pack  
12RM26, 68008 Mnemonics ROM Pack  
12RM27, 68010 Mnemonics ROM Pack  
12RM41, Z80 Mnemonics ROM Pack  
12RM42, Z8001/3 Mnemonics ROM Pack  
12RM43, Z8002/4 Mnemonics ROM Pack  
12RM62A, F9450 (1750A MIL STD) Mnemonics ROM Pack  
12RM63, 6502 Mnemonics ROM Pack  
12RM71, NSC800 Mnemonics ROM Pack



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## MANUAL CHANGE INFORMATION

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Product Group 57

THIS IS A PLACEMENT PAGE PACKAGE

1. Add the designated page to your manual before the Color Display tab page.
2. Keep this cover sheet in the Change Information section at the back of your manual for a permanent record.