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PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

2445/2465
OPTION 06 and OPTION 09
COUNTER/TIMER/TRIGGER
and
WORD RECOGNIZER
SERVICE

INSTRUCTION MANUAL

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found. For maximum and minimum input voltage see Table 1-2.

Symbols as Marked on Equipment

DANGER — High voltage.

Protective gound (earth) terminal.

ATTENTION — Refer to manual.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

Use the Proper Fuse

To avoid fire hazard, use only a fuse of the correct type, voltage rating and current rating as specified in the parts list for your product.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

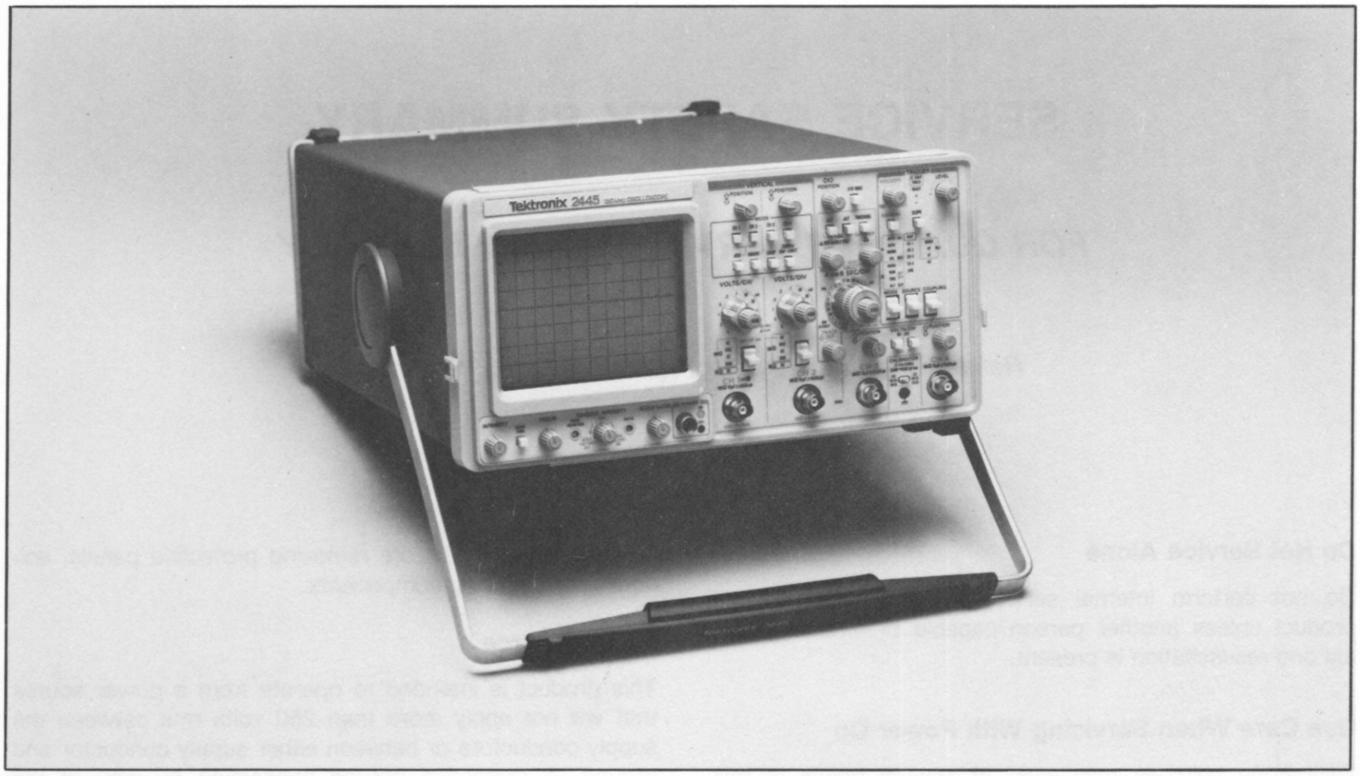
Use Care When Servicing With Power On

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



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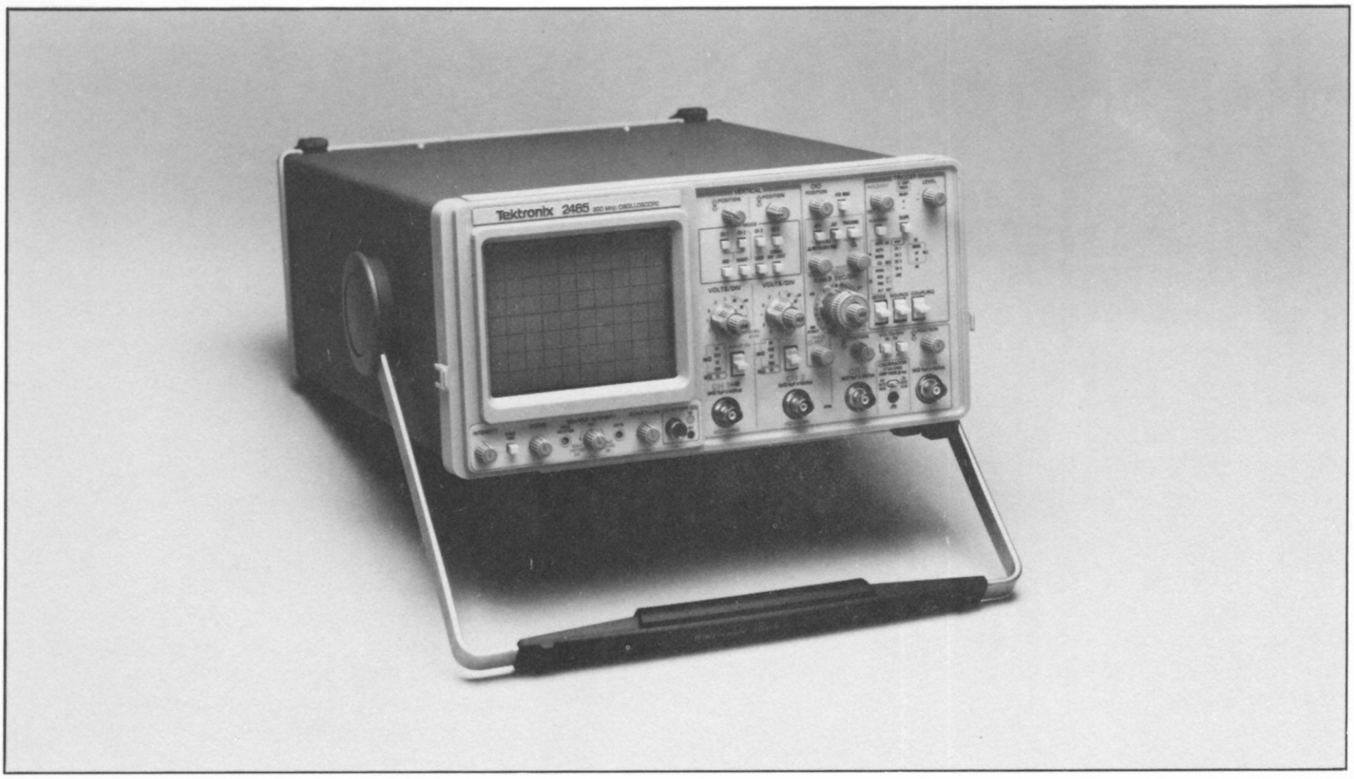
The 2445 Option 06 and Option 09 Oscilloscope.



4631-02

The 2465 Option 06 and Option 09 Oscilloscope.

SPECIFICATION

INTRODUCTION

The Counter/Timer/Trigger (Option 06) and Counter/Timer/Trigger with Word Recognizer (Option 09) add the following four capabilities to the TEKTRONIX 2445 and 2465 Oscilloscopes:

1. Precision time-interval measurement.
2. Event and frequency counting.
3. Delay-by-events triggering.
4. Logic triggering.

The 17-bit Word Recognizer probe of Option 09 extends the capabilities of these functions. The functions described in this manual which use the Word Recognizer require the Word Recognizer Option 09 and the 17-bit Word Recognizer probe.

The Counter/Timer/Trigger and Counter/Timer/Trigger with Word Recognizer options use the 2445 and 2465 alphanumeric crt readout to display configuration menus and function results.

The oscilloscope operators manual should be consulted for operating information regarding the 2445 and 2465 instruments. The operation and specifications of functions not described in this manual remain unchanged.

There are currently no options available for the C/T/T and WR. Also, Option 11 (rear panel probe-power connectors), described in the 2465 manuals, and Option 09 (Word Recognizer), described in this manual, are not available in the same instrument.

In addition to the standard instrument's standard accessories, the following standard accessories are provided with each instrument containing the 2445/2465 Option 06 Counter/Timer/Trigger:

1 2445/2465 Option 06 and Option 09 Counter/Timer/Trigger and Word Recognizer Operators Manual.

1 2445/2465 Option 06 and Option 09 Counter/Timer/Trigger and Word Recognizer Reference Card

1 2445/2465 Option 06 and Option 09 Counter/Timer/Trigger and Word Recognizer Reference Guide

Each instrument containing the Word Recognizer is provided with the following standard accessories in addition to those mentioned for the Counter/Timer/Trigger:

1 P6407 Word Recognizer Probe package.

The following optional accessory is also available for these options:

1 2445/2465 Option 06 and Option 09 Counter/Timer/Trigger and Word Recognizer Service Manual

DESCRIPTION OF FUNCTIONS

Precision Time-Interval Measurements

Precision delay and precision delta-time measurements are made possible by a precision timer which directly measures the time interval between the start of the A Sweep and the start of the B Sweep. Direct measurement capability operates when the B Sweep is triggerable after delay as well as in RUN AFT DLY. Direct measurement increases resolution and accuracy.

Only one of the four functions provided by the Counter/Timer/Trigger Option (Precision Time-Interval Measurement, Event Counting, Delay-by-Events Triggering, and Logic Triggering) can be active at a given time with the exception that precision time measurements are available with the Logic Trigger function when the B Sweep is triggered by the Word Recognizer.

When timing measurements are requested while a conflicting Counter/Timer/Trigger (C/T/T) function is operating, the timing measurement is displayed with the accuracy and resolution associated with a 2445/2465 instrument not equipped with the Counter/Timer/Trigger Option. The word **SET** following the time measurement indicates this condition.

Pulse-width measurement is made easier by Alternate Slope (ALT SLP) mode. When this mode is selected, the delayed sweep controlled by the Δ REF OR DLY POS control triggers on the slope indicated by the SLOPE indicator, and the delayed sweep controlled by the Δ control triggers on the opposite slope.

Event Counting (COUNT)

The Event-Counting function has three modes: Frequency, Period, and Totalize. Either the A Trigger events or the 17-bit Word Recognizer (WR) events (if the Option 09 Word Recognizer is present) can be counted.

Delay-by-Events (DLY/EVTS)

The Delay-by-Events function adds the ability to delay a sweep by a number of events, rather than by an absolute time interval. Either the A or the B Sweep can be delayed; the delay period begins when a "Start" event occurs, and the duration of the delay is determined by a number of occurrences of a "Delaying" event. The sweep to be delayed, the "Start" event, the "Delaying" event, and the number of occurrences of the "Delaying" event are all operator selected.

Logic Trigger (LOGIC-TRIG)

This function adds logic-triggering capabilities. The A Sweep can trigger on any of the following:

1. The logical AND of the A and the B triggers going TRUE.
2. The logical OR of the A and the B triggers going TRUE.
3. The occurrence of a word recognized by the Word Recognizer.

The B sweep can trigger on the word recognized by the Word Recognizer.

Word Recognizer

The 17-bit Word Recognizer detects any 17-bit digital word, either synchronously with an external clock or asynchronously. Word occurrences may be counted for frequency, period, or totalize measurements. A word can trigger either the A or B Sweep, or the word can be a delaying event in the Delay-by-Events function. The Word Recognizer probe is shown in Figure 1-1.

PERFORMANCE CONDITIONS

Except as noted in Tables 1-1 through 1-4 of this manual, the electrical, environmental, and mechanical characteristics of Option 06 and 09 instruments are identical to those specified in the respective 2445 and 2465 Oscilloscope Operators manuals.

The electrical characteristics are valid when the instrument has been adjusted at an ambient temperature between +20 and +30°C, has had a warm-up period of at least 20 minutes, and is operated at an ambient temperature between −15 and +55°C (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

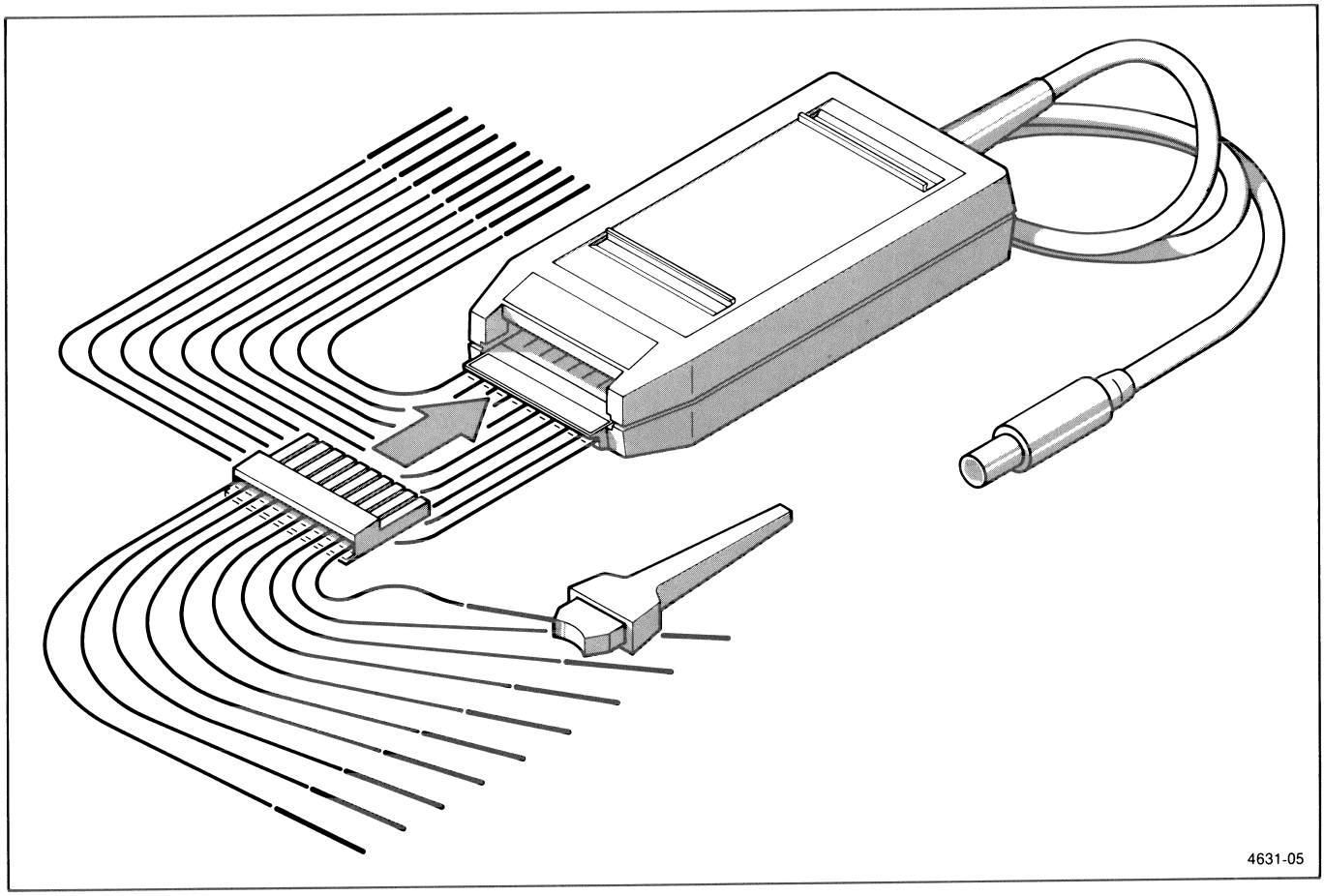


Figure 1-1. The Word Recognizer probe.

Table 1-1

Counter/Timer/Trigger Electrical Characteristics

Characteristics	Performance Requirements
SIGNAL INPUT SPECIFICATIONS FOR COUNT, DELAY-BY-EVENTS, AND LOGIC TRIGGER FUNCTIONS EXCLUDING WORD RECOGNIZER	
Maximum Input Frequency	⩾150 MHz.
Minimum Width of High or Low State of Input Signal	<3.3 ns.
Sensitivity	
DC to 50 MHz (0.5 Hz to 50 MHz for Frequency and Period)	
CH 1 and CH 2	1.5 divisions.[a]
CH 3 and CH 4	0.75 division.[a]
50 MHz to 150 MHz	
CH 1 and CH 2	4.0 divisions.[a]
CH 3 and CH 4	2.0 divisions.[a]
FREQUENCY	
RANGES	**RANGE** — **LSD[b] [c]** 1 Hz — 100 nHz 10 Hz — 1 μHz 100 Hz — 10 μHz 1 kHz — 100 μHz 10 kHz — 1 mHz 100 kHz — 10 mHz 1 MHz — 100 mHz 10 MHz — 1 Hz 100 MHz — 10 Hz 150 MHz — 100 Hz
Auto Ranging	Upranges at 100% of full scale; downranges at 9% of full scale.[c] Full scale corresponds to the value given in the Range column. The maximum displayed value for any range is the Range value minus the LSD value.
Accuracy	±[Resolution + (Frequency X TBE)] Hz.
Time Base Error (TBE)	10 ppm. Less than 5 ppm per year drift.[c]
Resolution	$\frac{1.4 \times \text{Frequency}^2 \times \text{TJE}}{N} + \text{LSD}^c$
Display Update Rate	Twice per second or twice the period of the input signal, whichever is slower.[c]

[a]Performance Requirement not checked in manual (except Frequency—using CH 1).

[b]Least significant digit.

[c]Performance Requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
PERIOD	
RANGES	**RANGE** — **LSD[c]** 10 ns — 1 fs 100 ns — 10 fs 1 μs — 100 fs 10 μs — 1 ps 100 μs — 10 ps 1 ms — 100 ps 10 ms — 1 ns 100 ms — 10 ns 1 s — 100 ns 2 s — 1 μs
Minimum Period	<6.7 ns[c]
Auto Ranging	Upranges at 100% of full scale; downranges at 9% of full scale.[c] Full scale corresponds to the value given in the Range column. The maximum displayed value for any range is the Range value minus the LSD value.
Accuracy	± [Resolution + (TBE X Period)].[c]
Resolution	± [LSD + (1.4 X TJE)/N][c]
Display Update Rate	Twice per second or twice the period of the input signal, whichever is slower.[c]
TOTALIZE	
Maximum Count	9999999.[c]
Display Update Rate	Twice per second or once per event, whichever is slower.[c]
DELAY BY EVENTS	
Maximum Event Count	4194303.[c]
Minimum Time from Start Signal to Any Delay Event	4 ns.[c]
LOGIC TRIGGER	
Minimum Function True Time	4 ns.
Minimum Function False Time	4 ns.[c]

[c]Performance Requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
	DELAY TIME
Run After Delay Accuracy	LSD[d] + [0.0012 X (A SEC/DIV)] + [0.03 X (B Time/Div)[e] + A Trigger Level Error + 50 ns.[c] When the A Sweep is triggered by the Word Recognizer in synchronous mode, add 100 ns for probe delay; in asynchronous mode, add 200 ns for probe delay. **NOTE** *Due to changes in the amount of trace that is visible before the trigger point, caused by changes in intensity and the Z axis, the C/T/T and the base instrument measure Delay Time from different points.*
Maximum Measurable Delay Time	9.95 times the A SEC/DIV setting.[c]
Triggerable After Delay Accuracy	LSD[d]+ [10 ppm X (measured interval)] + TJE + A Trigger Level Error + B Trigger Level Error + 0.5 ns.[c] If the A and B Sweeps are triggered from different channels, then add 0.5 ns for channel-to-channel mismatch. When the A Sweep is triggered by the Word Recognizer in synchronous mode, add 100 ns for probe delay; in asynchronous mode, add 200 ns for probe delay.
Minimum Measurable Delay Time	70 ns.
Display Update Rate	In Auto Resolution, twice per second or once for every sweep, whichever is slower.[c] In 1 ns, 100 ps, and 10 ps resolution modes, the update rate depends on the A SEC/DIV setting and the trigger repetition rate.

[c]**Performance Requirement not checked in manual.**

[d]**See Table 2-2.**

[e]**B time/div includes SEC/DIV, X10 MAG, and VAR.**

Table 1-1 (cont)

Characteristics	Performance Requirements
DELTA TIME	
Run After Delay Accuracy	LSD[d] + [0.0008 X (A SEC/DIV)] + [0.01 X (B Time/Div)[e]] + 83 ps.[c] When the A Sweep is triggered by the Word Recognizer in synchronous mode, add 1 ns for probe jitter; in asynchronous mode, add 20 ns for probe jitter.
Triggerable After Delay Accuracy Superimposed Delta Time	LSD[d] + [0.01 X (B Time/Div)[e]] + [10 ppm X (A SEC/DIV)] + [10 ppm X (measured interval)] + 50 ps + TJE.[c] If CH 3 or CH 4 is one channel of a two-channel measurement, add 0.5 ns for channel-to-channel delay mismatch.
Non-superimposed Delta Time	LSD[d] + $\lvert t_{r_{REF}} - t_{r_{DELT}} \rvert$[f] + TJE + [(0.005 div) X ($1/SR_{REF}$ + $1/SR_{DELT}$)] + [10 ppm X (A SEC/DIV)] + [10 ppm X (measured interval)] + 50 ps. If A and B sweeps are triggered from different channels, add 0.5 ns for channel-to-channel mismatch + [0.5 div X ($1/SR_{REF}$ + $1/SR_{DELT}$)] for trigger offset.
Minimum Displayable Delta Time	0 s.[c]
Maximum Displayable Delta Time	± 9.95 times the A SEC/DIV setting.[c]
Display Update Rate	In Auto Resolution, twice per second or once for every four sweeps, whichever is slower.[c] In 1 ns, 100 ps, and 10 ps resolution modes, the update rate depends on the A SEC/DIV setting and the trigger repetition rate.
ALTERNATE SLOPE	
Accuracy	Same as DELTA TIME Triggerable After Delay.[c]
Minimum Displayable Width	1 ns.[c]
Maximum Displayable Width	9.95 times the A SEC/DIV setting.[c]

[c]Performance Requirement not checked in manual.

[d]See Table 2-2.

[e]B time/div includes SEC/DIV, X10 MAG, and VAR.

[f]This term assumes the trigger points are between the 10% and 90% points of the waveforms. Fall time is expressed as a negative risetime.

Table 1-1 (cont)

Characteristics	Performance Requirements

DEFINITIONS

A Trigger Level Error = (A Trigger Level Readout Error)/SR_A.

B Trigger Level Error = (B Trigger Level Readout Error)/SR_B.

$t_{r_{REF}}$ = risetime, reference trigger signal.

$t_{r_{DELT}}$ = risetime, delta trigger signal.

SR_A = slew rate at trigger point, A sweep trigger signal in div/sec.

SR_B = slew rate at trigger point, B sweep trigger signal in div/sec.

SR_{REF} = slew rate at trigger point, reference trigger signal in div/sec.

SR_{DELT} = slew rate at trigger point, delta trigger signal in div/sec.

TJE = trigger jitter error.

= (Trigger Jitter)/$\sqrt{N}$.

For delay or delta time, disregarding noise in the signal, this term contributes <1 LSD if the slew rate is greater than 0.03 vertical div/ns or if the slew rate is greater than 30000 vertical div/horizontal div.

Trigger Jitter = $\sqrt{(\text{Reference Trigger Signal Jitter})^2 + (\text{Delta Trigger Signal Jitter})^2 + (\text{A Sweep Trigger Signal Jitter})^2}$.

Reference Trigger Signal Jitter = $(e_{n_S} + e_{n_{REF}})/SR_{REF}$.

= 0 for Frequency mode.

e_{n_S} = scope noise in div.

= 0.05 div for HF REJ trigger coupling.

= 0.1 div for DC trigger coupling, 5 mV to 5 V sensitivity.

= 0.15 div for DC trigger coupling, 2 mV sensitivity.

$e_{n_{REF}}$ = reference signal rms noise in div.

Delta Trigger Signal Jitter = $(e_{n_S} + e_{n_{DELT}})/SR_{DELT}$.

= 0 for Frequency or Delay mode.

$e_{n_{DELT}}$ = delta signal rms noise in div.

A Trigger Signal Sweep Jitter = $(e_{n_S} + e_{n_A})/SR_A$.

e_{n_A} = A sweep trigger signal rms noise in div.

Table 1-1 (cont)

Characteristics	Performance Requirements
When the Word Recognizer supplies a trigger in synchronous mode, the trigger jitter of the associated trigger signal is <1 ns; in asynchronous mode, the associated trigger signal jitter is <20 ns.	
N = number of averages during measurement interval.	
= see Table 2-2 for Delay or Delta Time.	
= (measured frequency) X (Measurement Interval) for Frequency or Period.	
Measurement Interval = 0.5 s or two periods of measured signal, whichever is greater.	

[a]Performance Requirement not checked in manual (except Frequency—using CH 1).

[b]Least significant digit.

[c]Performance Requirement not checked in manual.

[d]See Table 2-2.

[e]B time/div includes SEC/DIV, X10 MAG, and VAR.

[f]This term assumes the trigger points are between the 10% and 90% points of the waveforms. Fall time is expressed as a negative risetime.

Table 1-2

Word Recognizer Electrical Characteristics

Characteristics	Performance Requirements
SYNCHRONOUS MODE	
Data Setup Time W_0—W_{15} and Q	25 ns.
Data Hold Time W_0—W_{15} and Q	0 ns.
Minimum Clock Pulse Width	
High	20 ns.
Low	20 ns.
Minimum Clock Period	50 ns.[a]
Delay from Selected Clock Edge to Word Out from C/T/T	$\leq$ 55 ns.
ASYNCHRONOUS MODE	
Maximum Trigger Frequency	10 MHz.[a]
Minimum Coincidence Between Data Inputs (D_0—D_{15} & Q) Resulting in a Trigger	$<$ 85 ns.
Maximum Coincidence Between Any Two Data Inputs (D_0—D_{15} & Q) Without Producing a Trigger	$>$ 20 ns.
Delay from Input Word Coincidence to Word Out	$\leq$ 140 ns.
INPUTS AND OUTPUTS	
Input Voltages	
Minimum Input Voltage 	−0.5 V.[a]
Maximum Input Voltage 	5.5 V.[a]
Maximum Input Low Voltage	0.6 V.[a]
Minimum Input High Voltage	2.0 V.[a]
WORD RECOG OUT	
High	$>$ 2.5 V LSTTL output.[a]
Low	$<$ 0.5 V LSTTL output.[a]
Input High Current	20 μA.[a]
Input Low Current	−0.6 mA.[a]

[a]Performance Requirement not checked in manual.

Table 1-3

Environmental Characteristics

Characteristics	Performance Requirements
All Items	Same as the 2445 and 2465 Oscilloscopes without the C/T/T Option.

Table 1-4

Mechanical Characteristics

Characteristics	Description
Weight	
With Power Cord, Cover, Pouch, Test Leads, Probes, Operators Manual, and Options, Including Word Recognizer Probe	< 12.0 kg (26.4 lb).
Word Recognizer Probe	0.27 kg (0.6 lb).
Domestic Shipping Weight	< 17.6 kg (38.8 lb).
P6407 Probe Dimensions	
Length	
Body	11.4 cm (4.5 in).
Cable	2 m (6.6 ft).
Width	5.6 cm (2.2 in).
Height	2.21 cm (0.87 in).

OPERATING INFORMATION

PREPARATION FOR USE

OPERATING CONSIDERATIONS

A GATE OUT Termination

To prevent measurement errors, of as much as ±2.0 ns in Precision Delay and ±0.5 ns in Precision Delta Time, the A GATE OUT signal must not be terminated in less than 10 kΩ.

POWER-UP TESTS

Before initially turning on power to the instrument, read Section 2, "Preparation for Use," in the oscilloscope operators manual and follow the safety and precautionary information described there.

The power-up tests, automatically performed each time the oscilloscope is turned on, verify both the oscilloscope circuitry and the option circuitry. Tests, specifically applicable to Option 06 and Option 09, are integrated into the power-up tests of the host oscilloscope, and the tests consist of two main parts: Kernel tests and Confidence tests.

A power-up test failure will either flash the A SWP TRIG'D indicator or display a diagnostic message in the crt readout. Pressing in the A/B/MENU switch (**A/B TRIG** in the crt readout) may place the instrument into a usable mode. Even if the instrument then functions adequately for your particular requirement, it should be referred to a qualified service technician for repair of the problem as soon as possible.

CONTROLS, CONNECTORS, AND INDICATORS

The controls, connectors, and indicators used in the operation of the Option 06 Counter/Timer/Trigger and Option 09 Counter/Timer/Trigger with Word Recognizer are described in this section, along with any controls whose function is affected by these options. For details about the controls used to operate the standard oscilloscope, refer to the respective instrument operators manual. There are no controls added to the front panel to accommodate these options, but the B TRIGGER MODE indicator group has two extra positions, MENU and ALT SLP.

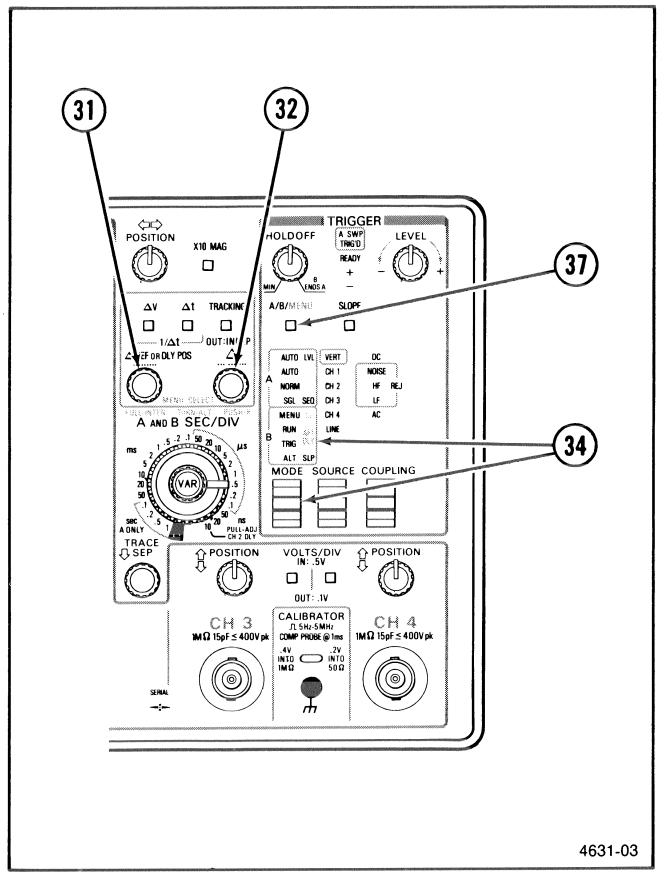


Figure 2-1. Counter/Timer/Trigger and Word Recognizer controls.

Refer to Figure 2-1 for the location of the controls and indicators described in this section. The circled item numbers are the same as the corresponding items discussed in Section 3 of the standard instrument operators manual.

FRONT PANEL CONTROLS

(31) **Δ REF OR DLY POS Control**—This control is used for configuration menu selection and menu-mode configuration (for details see "Menu Mode Function Selection" which follows).

(32) **Δ Control**—This control is used for configuration menu selection and menu-mode configuration (for details see "Menu Mode Function Selection" which follows).

(34) **TRIGGER MODE Switch and Indicators**—The A TRIGGER MODE switch and indicators are the same as in the standard instrument. Two new positions are added to the B TRIGGER MODE switch indicators:

MENU—When this mode is entered, the readout displays various menus which permit Counter/Timer/Trigger and Word Recognizer functions to be selected and configured.

ALT SLP—In this mode, when the A AND B SEC/DIV knobs are unlocked, the instrument makes a precision time-interval measurement between alternate B sweeps which are triggered on opposite slopes of the waveform.

(37) **A/B/MENU Switch**—If an A Trigger indicator is illuminated and the SEC/DIV switches are locked together, pressing the switch activates MENU mode. On instruments that do not contain the Counter/Timer/Trigger, this control is labeled A/B TRIG.

REAR PANEL

The rear panel is identical to that of the standard instrument, except that when the Word Recognizer Option is installed, the Word Recognizer Probe and the WORD RECOG OUT connectors are installed in the same locations used by the Probe Power connectors of Option 11 (see Figure 2-2).

(54) **Word Recognizer Probe Connector**—Connects the 17-Bit Word Recognizer Probe to the instrument.

(55) **Word RECOG OUT Connector**—Provides an LSTTL-compatible, positive-going pulse when the Word Recognizer detects the selected word.

READOUT DISPLAYS

Bottom-Row Readout Displays

The readout displays along the bottom row of the crt are not affected by the Counter/Timer/Trigger and the Word Recognizer except for additions to the Diagnostics menu.

Top-Row Readout Displays

The top row of the crt readout is shared according to the following priority:

1. Menus occupy the entire top row.

2. Delta and Delay displays appear in the right-hand field of the display.

3. Event-Counting (COUNT), Delay-by-Events (DLY/EVTS), and Logic-Trigger (LOGIC TRIG) displays (excluding the WR Logic-Trigger display) appear in the right-hand field if the field is not occupied by a Delta or Delay display; otherwise, the displays appear in the left-hand field.

4. Word-Recognizer displays appear in the left-hand field of the display.

5. The trigger-level readout appears in the left-hand field.

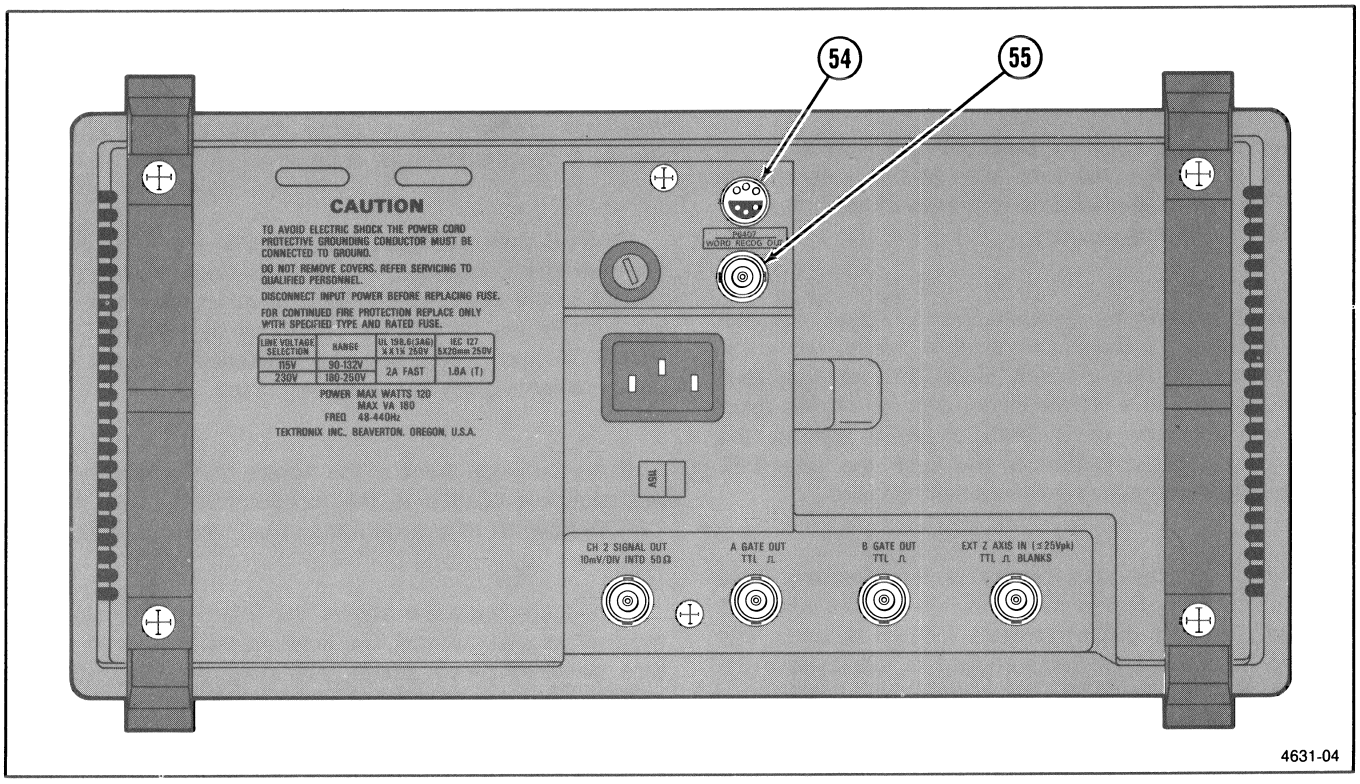


Figure 2-2. Rear Panel Word Recognizer connectors.

OPERATING PROCEDURES

Consult the 2445 and 2465 Operators manuals for basic operating information and techniques that should be considered before attempting to make any measurements with your instrument.

PRECISION TIME-INTERVAL MEASUREMENTS

Time-Interval Measurements

The Counter/Timer/Trigger Option has no effect on cursor measurements except that Δt and $1/\Delta t$ measurements with cursors are available when the B Sweep is delayed by events.

Precision Delay-Time and Precision Delta-Time Operation

Operating procedures for precision delay-time and delta-time functions are the same as the operating procedures for delay-time and delta-time functions in a 2445 or 2465 instrument without the C/T/T Option.

Whenever the display for precision time-interval measurements is updated, the last letter of the units symbol blinks. The displayed resolution is selectable (see "Resolution Selection" in this section).

When a conflicting Counter/Timer/Trigger function (Delay-by-Events or Event Counting) is active, the precision time-interval measurement function is not available, but it is replaced by a time measurement having the resolution and accuracy of a 2445 or 2465 without the Counter/Timer/Trigger Option. In this case, the word **SET** appears following the time-measurement display.

The **SET** display also occurs during precision time measurements any time a control switch or delta control is operated. The **SET** display remains for two seconds, and then the precision time measurement is displayed if it's available; e.g.:

starting display:	**DLY 213.3693ms**
delta control rotated:	**DLY 198.1ms SET**
final display:	**DLY 197.8849ms**

If the measurement is not available, one of the following messages is displayed to indicate why:

AVERAGING	More sweeps are required for the selected measurement resolution.
NO A TRIGGER	No A Trigger event was received.
MISSING B TRIG	At least one A Sweep occurred without a B Trigger event during the A Sweep.

B Triggered After Delay Mode

The C/T/T Option allows precision time measurements even while in the B TRIG AFT DLY mode. The B Trigger controls operate in the same manner with the C/T/T Option as in a 2445 or 2465 not equipped with the option.

An instrument with a C/T/T measures the time from the start of the A Sweep to the start of the B Sweep, whether the B Trigger MODE is RUN AFT DLY or TRIG AFT DLY. The measurement gives delay times directly when B Sweep is operated without delta time.

When B Sweep is used with delta time or 1/delta time, the instrument measures the interval from the start of A Sweep to the start of B Sweep. A measurement is made for each of the two delays controlled by the Δ REF OR DLY POS and Δ controls. The difference between these measurements gives the delta-time result.

If the transition times of the signals being measured are not negligible relative to the measurement, rotate the B SEC/DIV switch to provide a magnified view of the signals.

This magnified view shows the intersection points of the two delayed sweeps. The time interval measured is the time between these points. Adjusting the B TRIGGER LEVEL and the VERTICAL POSITION selects various intersection points. When making a dual-channel delta-time measurement, if the points of interest can not be made to intersect by the LEVEL and POSITION controls, the points can be forced to intersect by reducing the displayed amplitude of the signal that appears later in the display and then readjusting the LEVEL and POSITION controls.

The relative accuracies of delta-time and delay-time measurements using cursors (delta time only), RUN AFT DLY, and TRIG AFT DLY vary as the measured time interval varies. Figure 2-3 shows the relative accuracies for delta-time measurements. Relative accuracies for delay-time measurements are shown in Figure 2-4.

The B Trigger-After-Delay mode is deselected when the Channel 2 Delay-Adjust function is selected.

Alternate Slope Mode Selection

Alternate Slope mode measures the time interval between two points on opposite slopes of a waveform. The delayed sweep controlled by the Δ REF OR DLY POS control triggers on the slope indicated by the SLOPE indicator, while the delayed sweep controlled by the Δ control triggers on the opposite slope.

To select the Alternate Slope mode of Precision Delta Time:

1. Unlock the SEC/DIV knobs.

2. If an A TRIGGER MODE indicator is illuminated, push the A/B/MENU switch.

3. Repeatedly press the B TRIGGER MODE switch down and release it until the ALT SLP MODE indicator is illuminated.

4. Select the desired B Trigger Source and Coupling.

5. Adjust the B TRIGGER LEVEL to the desired trigger point.

6. Rotate the Δ controls until intensified zones appear on the desired slopes.

7. If the transition times of the signal being measured are not negligible to the measurement, rotate the B SEC/DIV control to a faster sweep speed to magnify the view of the signal. The time interval is measured between the points where the two delayed sweeps intersect. Adjusting the B TRIGGER LEVEL moves the area of intersection.

The Alternate Slope function is deselected when the Channel 2 Delay-Adjust function is selected.

MENU MODE FUNCTION SELECTION

Event-Counting, Delay-by-Events, Logic-Trigger functions, and Resolution selection are selected from a menu. To select one of these functions:

1. Enter MENU mode by one of the two following methods:

   a. If an A TRIGGER MODE indicator is illuminated:

      (1) Press the A/B/MENU select switch to illuminate a B TRIGGER MODE indicator.

      (2) If the MENU indicator is not illuminated, push the TRIGGER MODE switch up to select MENU.

   b. If a B TRIGGER MODE indicator is illuminated, push the TRIGGER MODE switch up until MENU is selected.

2. The Main Menu is displayed on the crt:

COUNT DLY/EVTS LOGIC–TRIG RES

3. Turn either the Δ or the Δ REF OR DLY POS control to move the dotted-line cursor under the desired function.

4. Push the TRIGGER MODE switch up to display the Configuration Menu for the selected function.

5. See appropriate function descriptions which follow for further Menu information.

To remove the Menu display without activating a function, press any one of the following controls:

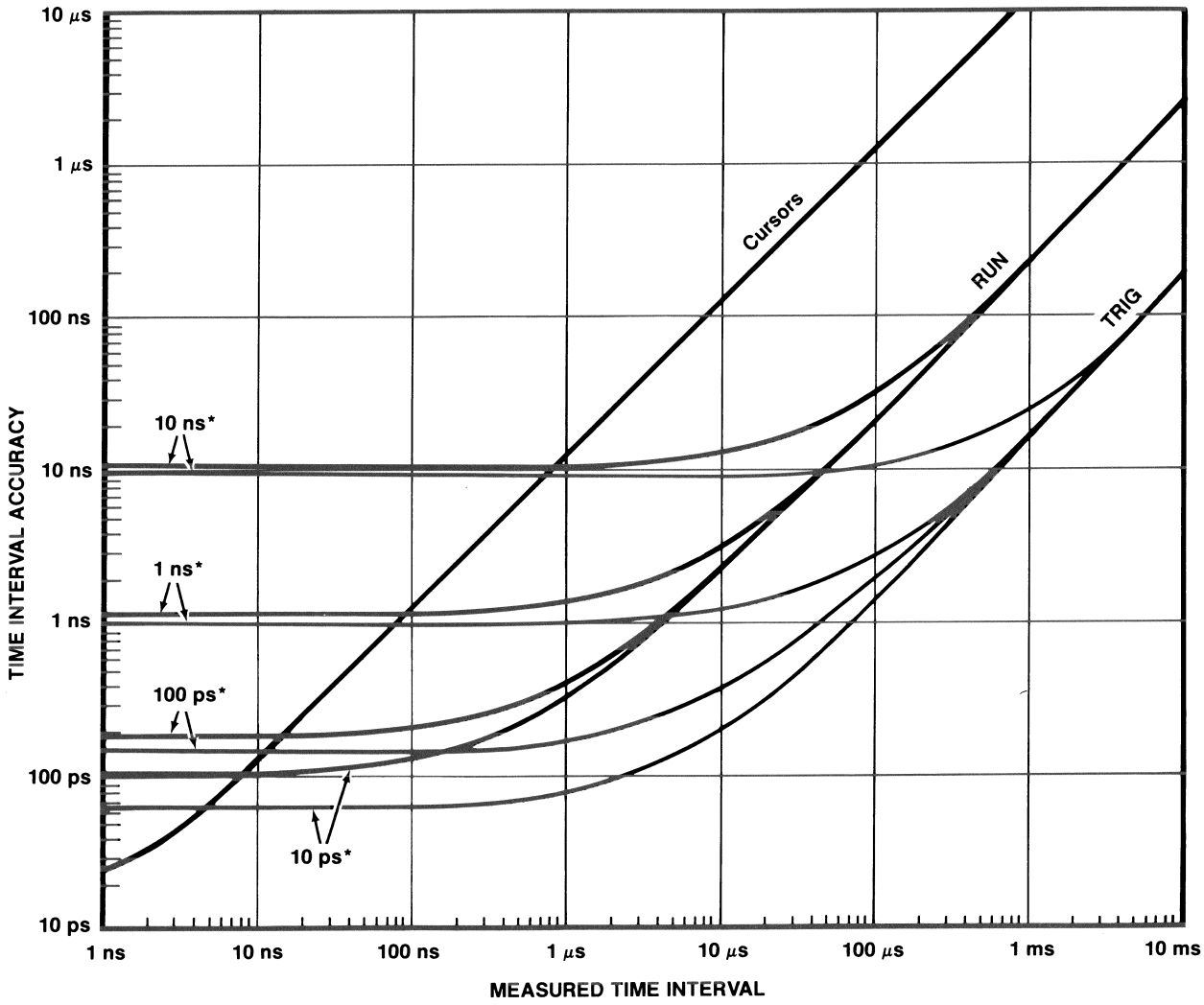
1. TRIGGER MODE switch down.

2. A/B/MENU switch.

3. Δt switch.

4. ΔV switch.

Any MENU function (Event-Counting, Delay-by-Events, or Logic-Trigger) is deselected when the Channel 2 Delay-Adjust function is activated.



CONDITIONS:

1) Input signal is 5 vertical divisions with a 2 ns risetime.
2) Measured times are 4 horizontal divisions.
3) TJE is negligible for slew rates greater than 0.1 div/ns.
4) For all B Sweep modes, the beginning and end of the measured interval are visually superimposed.

* Selected resolution. See "Resolution Selections" table for resolutions corresponding to trigger rates with AUTO resolution.

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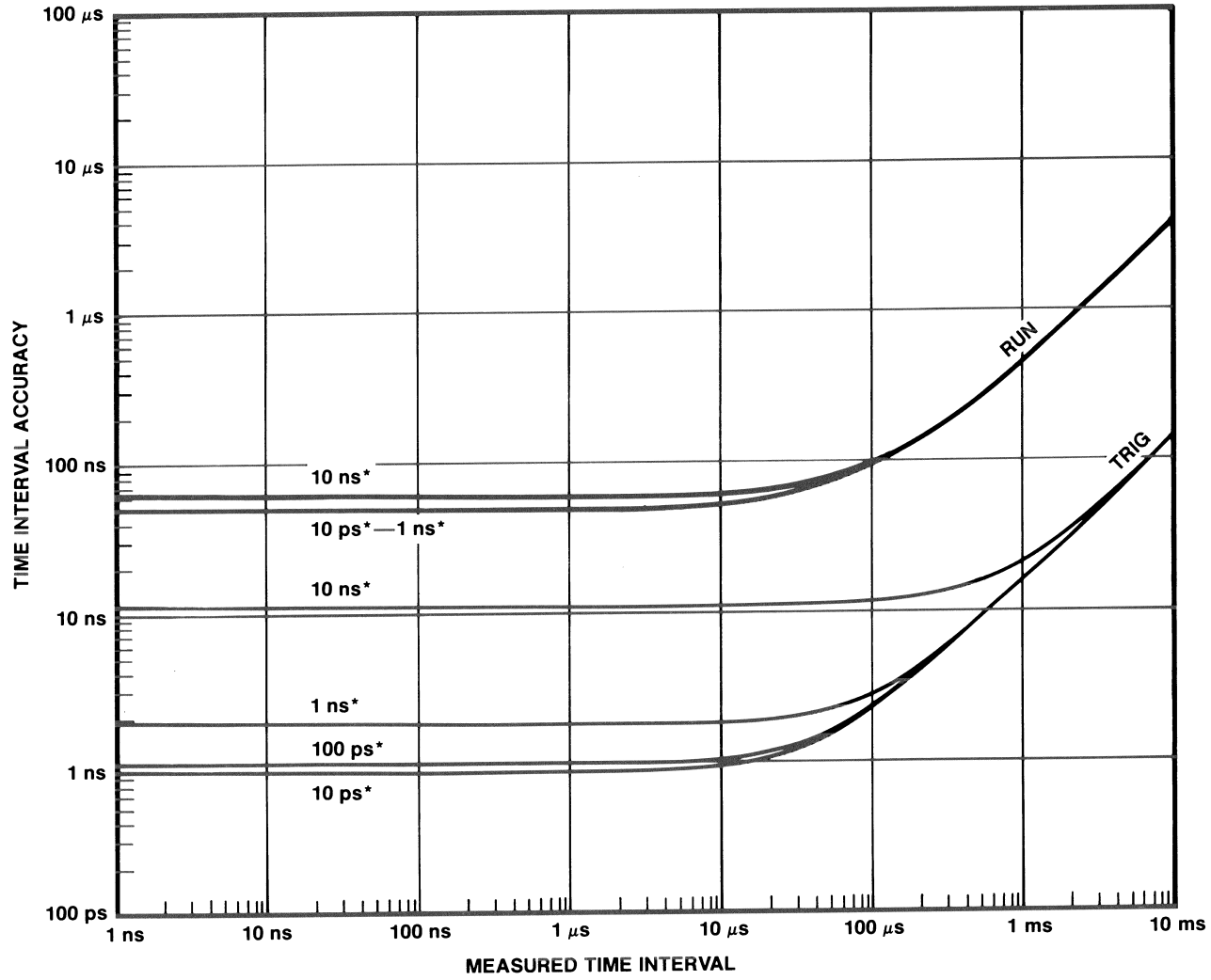
Figure 2-3. Delta Time relative accuracies.



CONDITIONS:

1) Input signal is 5 vertical divisions with a 2 ns risetime.
2) Measured times are 4 horizontal divisions.
3) TJE is negligible for slew rates greater than 0.1 div/ns.

* Selected resolution. See "Resolution Selections" table for resolutions corresponding to trigger rates with AUTO resolution.

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Figure 2-4. Delay Time relative accuracies.

Event Counting (COUNT)

To activate Event Counting from the Main menu:

1. After using a delta control to underline COUNT in the main menu and pushing the TRIGGER MODE switch up, the Count Configure menu is displayed. If the instrument contains the Word Recognizer Option, the Count Configure menu is:

MODE<FREQ PERIOD TOT> EVT<A WR>

The MODE field allows selection of either FREQuency, PERIOD, or TOTalize. The EVT field allows selection of the event that the selected mode operates on. Either the A Trigger events (A) or the Word Recognizer events (WR) can be selected. While counting Word Recognizer events, the A Sweep is triggered by the Word Recognizer event.

If the instrument does not contain the Word Recognizer Option, the Count Configure menu is:

MODE<FREQ PERIOD TOT> EVT=A TRIG

2. Turn the Δ REF OR DLY POS control to underline the field to be configured (i.e., MODE or EVT). Then turn the Δ control to underline the selection for that field. If only one underline is shown, either control may be turned.

3. When the configuration is correct, push the TRIGGER MODE switch up. If Word Recognizer has been selected as the event, the Word Recognizer Configure Menu is displayed (see "Word Recognizer" in this section); otherwise, the function is activated.

NOTE

When counting high-frequency signals, readjustment of the Trigger Level may be required to eliminate jitter of the displayed waveform.

4. If Totalize mode is active, the displayed count is reset by moving any front panel switch.

5. To deselect any function and exit MENU mode:

a. If the MENU indicator is not illuminated, push the A/B/MENU switch.

b. Push the TRIGGER MODE switch down.

Any of the following actions will also deselect an active Count mode:

a. Selecting an A Trigger Source of LINE.

b. Selecting an A Trigger Mode of SGL SEQ.

c. If the Count event is the Word Recognizer, selecting AUTO LVL for the A Trigger Mode (the Main menu will be displayed).

d. If the Totalize mode is active, selecting AUTO or AUTO LVL for the A Trigger Mode (the Main menu will be displayed).

Delay-by-Events (DLY/EVTS)

The Delay-by-Events function allows the selection of the sweep to be delayed, the starting event, and the delaying event. The combinations available are shown in Table 2-1.

To activate the Delay-by-Events function from the Main menu:

1. After using a delta control to underline DLY/EVTS in the Main menu and pushing the TRIGGER MODE switch up, the Delay-by-Events Configure menu will be displayed. If the instrument contains the Word Recognizer Option, the Delay-by-Events Configure menu is:

SWP<A B> START<A WR> DLY BY<B WR>

If the instrument does not contain the Word Recognizer (WR), the Delay-by-Events Configure menu is:

SWP<A B> START=A DLY BY B

The sweep to be delayed, either A or B, is selected from the SWP field. If the B Sweep is selected to be delayed, the START field is limited to only the A Trigger event. The event which will start the delay is selected from the START field. Either the A Trigger event (A) or the Word Recognizer event (WR) can be selected. If the Word Recognizer is selected as the START event, SWP defaults to A. The event counted to give the desired delay is selected from the EVT field. Either the B Trigger event (B) or the Word Recognizer event (WR) can be selected.

2. Turn the Δ REF OR DLY POS control to underline the field to be configured (i.e., SWP, START or EVT). Then turn the Δ control to underline the selection for that field.

Table 2-1

Delay-by-Events Combinations

Sweep to be Delayed	Start Event	Delaying Event	Results
A	A Trigger	B Trigger	Delay begins when the A Trigger event occurs; the A Sweep runs after the selected number of B Trigger events.
A	Word Recognizer	B Trigger	Delay begins when a recognized word occurs; the A Sweep runs after the selected number of B Trigger events.
A	A Trigger	Word Recognizer	Delay begins when the A Trigger event occurs; the A Sweep runs after the selected number of words are recognized.
A	Word Recognizer	Word Recognizer	The A Sweep runs after the selected number of words are recognized.
B	A Trigger	B Trigger	Delay begins when the A Sweep is triggered by the A Trigger event; the B Sweep runs after the selected number of B Trigger events, if the A Sweep has not terminated.
B	A Trigger	Word Reconizer	Delay begins when the A Sweep is triggered by the A Trigger event; the B Sweep runs after the selected number of words are recognized, if the A Sweep has not terminated.

3. When the configuration is correct, push the TRIGGER MODE switch up. If Word Recognizer was selected, the Word Recognizer Configure menu is displayed (see "Word Recognizer" in this section); otherwise, the function is activated.

If B Sweep Delay-by-Events is selected and the SEC/DIV knobs are locked, the message **PULL SEC/DIV** appears instead of the Delay-by-Events display.

While the function is active, the number of occurrences of the Delaying event required to trigger the delayed sweep is displayed along with a letter identifying the sweep being delayed by events; e.g.:

A DBE 1234567

The number of occurrences can be changed if the Delay-by-Events display is on the right side of the crt. The display is on the right side of the crt if no higher priority function such as Δt is also selected.

To change the number of events:

Turn the Δ REF OR DLY POS control to underline a digit of the number. Turn the Δ control to alter the underlined character's value. If a digit is incremented from 9 to 0 (nine to ten), the digit to its left is incremented; if a digit is decremented from 0 to 9 (ten to nine), the digit to its left is decremented. If a digit is incremented to its maximum permissible value and all the digits to its left are at their maximum value, the underline moves to the next digit to the right. If a digit is decremented to 0 and all digits to its left are 0 (displayed as spaces), then the cursor moves to the next digit to the right.

If B Sweep Delay-by-Events is displayed and either Δt or 1/Δt is selected, cursors are also displayed. The word **SET** in the cursor's display is replaced with **BSW** to indicate that the displayed time is referenced to the B Sweep.

4. To deselect any function and exit MENU mode:

a. If the MENU indicator is not illuminated, push the A/B/MENU switch.

b. Push the TRIGGER MODE switch down.

If the A Sweep is delayed by events, selecting AUTO or AUTO LVL Trigger Mode for the A Trigger will deselect Delay-by-Events and display the Main menu.

NOTE

When the time between the start event and the delaying event is less than 4 ns, whether or not the delaying event will be counted is ambiguous. In most cases, the ambiguity can be resolved by choosing appropriate trigger slopes for the start and delaying events.

Logic Trigger

To activate the Logic Trigger function from the Main menu:

1. After using a delta control to underline **LOGIC-TRIG** in the Main menu and pushing the TRIGGER MODE switch up, the Logic-Trigger-Configure menu will be displayed. If the instrument contains the Word Recognizer Option, the Logic-Trigger-Configure menu is:

SWP:TRIG <A:A·B A:A+B A:WR B:WR>

The sweep (SWP) to be triggered and the source (TRIG) of the trigger are both selected from this menu. The selections are:

A:A·B = The A Sweep is triggered when the logical AND of the A and B Triggers becomes TRUE.

A:A+B = The A Sweep is triggered when the logical OR of the A and B Triggers becomes TRUE.

A:WR = The A Sweep is triggered when the Word Recognizer detects the selected word.

B:WR = The B Sweep is triggered when the Word Recognizer detects the selected word.

NOTE

The trigger is TRUE if + SLOPE is selected and the trigger-source voltage is more positive than the trigger level, or if − SLOPE is selected and the trigger-source voltage is more negative than the trigger level.

When the B Sweep is triggered by the Word Recognizer, delay time and delta time are measured by the crystal-controlled timer, but when any other Logic-Trigger function is active, delay-time and delta-time measurements are limited to the capabilities of the 2445 or 2465 without the C/T/T Option.

If the instrument does not contain the Word Recognizer Option, the Logic-Trigger-Configure menu is:

TRIG A SWEEP BY <A·B A+B>

2. Turn either delta control to move the underline cursor to the desired selection.

3. When the configuration is correct, push the TRIGGER MODE switch up. If Word Recognizer has been selected, the Word-Recognizer-Configuration menu is displayed (see "Word Recognizer" in this section); otherwise, the function is activated.

If the Word Recognizer is selected in Logic-Trigger mode, the Word Recognizer display takes the place of the respective trigger-level display.

While a Logic-Trigger function other than WR is active, one of the following Logic-Trigger displays is normally displayed on the right half of the crt readout. It is displayed on the left half of the crt readout if a delta or delay function is also active:

A SWP A·B and **A SWP A+B**

4. To deselect any function and exit MENU mode:

a. If the MENU indicator is not illuminated, push the A/B/MENU switch.

b. Push the TRIGGER MODE switch down.

Selecting AUTO LVL A Trigger Mode while any Logic Trigger function other than B Sweep triggered by the Word Recognizer (B:WR) is active results in the function being deselected and the Main menu being displayed.

Resolution Selection

Four resolutions are available for Delay Time, Delta Time, and 1/Delta Time precision measurements. In AUTO, the display update rate is either every 1/2 second or every time a measurement sample is available, whichever is greater. For 1 ns, 100 ps, and 10 ps resolution, the display is updated only when enough sweeps have occurred to display the indicated resolution. For low sweep repetition rates, the time interval between updates is noticeably long. Table 2-2 lists the displayed resolution for each resolution selection and the number of sweeps (N) required for each measurement.

Table 2-2
Resolution Selections

A SEC/DIV[a]	Selected Resolution	LSD	N
10 ns to 1 s	AUTO	See AUTO RESOLUTION	See AUTO RESOLUTION
10 ns to 5 μs	10 ps	10 ps	$>10^6$
	100 ps	100 ps	$>10^4$
	1 ns	1 ns	>100
10 μs to 50 μs	10 ps or 100 ps	100 ps	$>10^4$
	1 ns	1 ns	>100
100 μs to 500 μs	10 ps to 1 ns	1 ns	>100
1 ms to 5 ms	10 ps to 1 ns	10 ns	>1
10 ms to 50 ms	10 ps to 1 ns	100 ns	>1
100 ms to 500 ms	10 ps to 1 ns	1 μs	>1
1 s	10 ps to 1 ns	10 μs	>1

AUTO RESOLUTION

A SEC/DIV[a]	Trigger Repetition Rate	LSD	N
10 ns to 2 μs	>20kHz	100 ps	$>10^4$
10 ns to 2 μs	200 Hz to 20 kHz	1 ns	>100
5 μs to 200 μs	>200 Hz	1 ns	>100
10 ns to 200 μs	<200 Hz	10 ns	>1
500 μs to 5 ms	Any	10 ns	>1
10 ms to 50 ms	Any	100 ns	>1
100 ms to 500 ms	Any	1 μs	>1
1 s	Any	10 μs	>1

[a]2445 A SEC/DIV settings range from 20 ns to 1 s. 2465 A SEC/DIV settings range from 10 ns to 500 ms.

To activate the Resolution Selection function from the Main menu:

1. After using either delta control to underline **RES** in the Main menu and pushing the TRIGGER MODE switch up, the Resolution Selection menu is displayed:

RESOLUTION <AUTO 1ns 100ps 10ps>

2. Turn either delta control to underline the desired resolution.

3. Push the TRIGGER MODE switch up when the configuration is correct.

Word Recognizer Configuration

The Word-Recognizer-Configuration menu is used to set the Word Recognizer's radix and clock parameters. When Word Recognizer (WR) is selected for use by a menu function and the TRIGGER MODE switch is pushed up to exit the Function-Configuration menu, the Word-Recognizer-Configuration menu is displayed:

RADIX<BIN OCT HEX> CLOCK<↑ ↓ X>

The Word Recognizer's configuration is displayed in the radix selected from the RADIX field. The choices are binary (BIN), octal (OCT), and hexadecimal (HEX).

The clock edge, used to acquire data in the Word Recognizer, is selected from the clock field. The choices are:

↑ = rising edge of clock.

↓ = falling edge of clock.

X = no clock used (asynchronous mode).

To set the Word Recognizer's parameters:

1. Select the Word Recognizer in a Function-Configuration menu.

2. Exit the function's menu by pushing up on the TRIGGER MODE switch. The Word-Recognizer-Configuration menu is then displayed.

3. Turn the Δ REF OR DLY POS control to underline the field to be configured (i.e., RADIX or CLOCK). Turn the Δ control to underline the selection for that field.

4. When the configuration is correct, push the TRIGGER MODE switch up to activate the function.

When a menu function uses the Word Recognizer, the status of the Word Recognizer is displayed in the following format:

tcq word

The t is the trigger selected (A or B); the c is the clock mode, rising (↑) or falling (↓) edge, or asynchronous (X); the q is the qualifier bit; and 'word' is a value displayed in the selected radix.

The Δ REF OR DLY POS control is turned to underline the clock mode, qualifier, or a digit of the word. The Δ control changes the selection for the underlined field.

If some bits of a hexadecimal or octal digit are irrelevant (don't care or 'X') the digit is ambiguous. Ambiguous digits are displayed as question marks; e.g.:

A↑0 11XX XXX1	A↑0 1?X077	A↑0 ??3F
... 0011 1111	...	...
BIN	OCT	HEX

When the status of the Word Recognizer and the event count for Delay-by-Events are both displayed, the Δ REF OR DLY POS control will move the selection cursor across both fields.

WORD OUT SIGNAL

The WORD OUT signal, at a BNC connector on the rear panel, is high when the selected word is recognized. This signal is valid after the Word Recognizer word has been defined using the C/T/T menu. The signal remains valid even if the menu function is not in use. The relation of the word coincidence relative to other signals can be observed by connecting the WORD OUT signal to one vertical channel and using the remaining vertical channels for the other signals.

The WORD OUT signal is delayed after the clock transition in synchronous mode or after the recognized coincidence in asynchronous mode. Because of this delay, the signal transition which generates the trigger cannot be displayed by the oscilloscope when the oscilloscope is triggered by the Word Recognizer or when the oscilloscope is triggered by the WORD OUT signal.

CONTROLLING INSTRUMENT FUNCTIONS WITH THE GPIB

This information pertains to controlling the 2445 and 2465 Oscilloscopes containing Counter/Timer/Trigger (Option 06), or the Counter/Timer/Trigger with the Word Recognizer (Option 09) via the IEEE-488-1978 digital interface (commonly referred to as the General Purpose Interface Bus, or GPIB). This information applies only if the instrument also contains the GPIB (Option 10) interface.

NOTE

If either the Counter/Timer/Trigger or Word Recognizer option is not contained in the instrument, reference to it in a GPIB command will cause an SRQ error.

The 2445/2465 Option 10 GPIB Operators Manual should be consulted for a complete description of remote control of oscilloscope functions by way of the GPIB.

A complete description of additional commands for controlling the Counter/Time/Trigger Option and the Counter/Timer/Trigger with the Word Recognizer Option is listed in Table 2-3 and Table 2-4 respectively.

NOTE

C/T/T measurements are requested with the CTSend command. DELAy? and DTIme? queries, which are common to the 2445/2465 without the C/T/T Option, return settings, ***not*** *measurements.*

Table 2-3

Counter/Timer/Trigger GPIB Commands

C/T/T Measurement Commands

Header	Argument	Argument	Comments
CTRdy?			Query response is 1 if a C/T/T measurement is available, 0 if not. This flag is always valid regardless of the OPC state. If no measurement function is active, or a measurement function is suspended due to another option using the display, an option-not-in-correct-mode SRQ error is sent.
CTSend?	IMMediate WAIt		This command is used to request any one of the following measurements: FREQuency, PERiod, TOTalize, Delay, Delta Time, or 1/Delta Time. The measurement returned is that generated by the currently operating function. The format of the returned measurment is <nr3>. The "?" following CTSend is optional and does not affect the operation of the command. If the currently available measurement is invalid, an error code is returned in place of the normal measurement. The error codes are: 1.0E+99 for a missing B trigger. 1.0E+98 for a missing A trigger. 1.0E+97 when the time being measured in a 1/Δt mode is less than 1% of full scale. 1.0E+96 for Totalize mode overflow. If no measurement function (count, precision delta, or delay) is active, or a measurement function is suspended due to another option using the display, an option-is-not-in-correct-mode SRQ error is sent. Any given measurement is only sent once. The current measurement is always sent immediately if it has not already been sent once. The argument following CTSend controls the manner in which the instrument responds when a measurement is in progress and no current measurement is available to send. CTSend with no argument defaults to WAIt for a measurement. If a measurement is not available and the IMMediate argument is received, a null message (talked with nothing to say) is sent. If a measurement is not available and the IMMediate argument is not received, the instrument will not respond until a new measurement has been acquired.

Table 2-3 (cont)

Header	Argument	Argument	Comments
OPC	ON OFF		This is an extension of the main instrument's OPC command. When OPC is ON, an SRQ is generated when a C/T/T measurement is completed. Generation of SRQ can be turned off by the RQS OFF command. The EVENT? query, as described in the 2445/2465 GPIB Operators Manual, may be used to determine the status of the C/T/T Option. The event code, returned through the EVENT? query, may be used to determine if a C/T/T measurement is complete (event code 778) even when RQS is OFF. However, the event code is only available when OPC is ON. Once the event code is generated, to indicate a measurement is available, SRQs and the event code are not generated again on measurement completion until a measurement has been read. The event code is generated only on completion of the next measurement after a measurement is read via the GPIB.
		C/T/T Setup Commands	
BTRigger	MODe:	ALTSlope RUN TRIGGerable	This command is an extension of the BTRigger MODe: command of the Main instrument. RUN and TRIGGerable function the same as in the main instrument. Setting mode to ALTSlope or TRIGGerable will conflict with any Count, Delay-by-Events, or Logic-Trigger mode, and a setting-conflict SRQ error is sent.
BTRigger?	MODe		Query response is identical to the Main instrument BTRigger? response except that MOD: ALTS can be sent.
COUNt	EVEnt: MODe:	ATRigger WREcognizer FREquency TOTal PERIod	This command configures the Count function. If the Word Recognizer Option is not installed and If EVEnt: WRE is received, an option-not-installed SRQ error is sent.
COUNt?	EVEnt MODe		Query response is: COUN MOD: string, EVE: string or COUN arg: string if an argument is given in the query.
CTT	COUNt DBEvents LTRigger OFF RESET		This command will either turn on a C/T/T function or turn off any active C/T/T function. Selecting any function will turn off any other selected function. Functions cannot be active at the same time. B TRIGGER MODE is set to RUN AFT DLY. CTT RESET resets any counter or precision measurement currently in progress.
CTT?			Query response is: CTT string, where "string" is the current C/T/T function.

Table 2-3 (cont)

Header	Argument	Argument	Comments
DBEvents	COUNt:	<nr1>	This command configures the Delay-by-Events function. The format of <nr1> is a positive integer in the range 1-4194303 inclusive. If a number is received that is out of range or noninteger, a numeric-argument SRQ error is sent.
	EVEnt:	BTRigger WREcognizer	If the Word Recognizer Option is not installed and if EVEnt:WREcognizer or STArt: WREcognizer is received, an option-not-installed SRQ error is sent.
	STArt:	ATRigger WREcognizer	Selecting STArt: WREcognizer sets SWEep to ASWeep.
	SWEep:	ASWeep BSWeep	Selecting SWEep: BSWeep sets STArt to ATRigger.
DBEvents:	COUNt EVEnt STArt SWEep		Query response is: DBE SWE: string, STA: string, EVE: string, COUN: <nr1>, or DBE arg: string if an argument is given in the query.
ID?			This query is an extension of the ID? query of the main instrument. Query returns CTT:FVn for the C/T/T's portion of [string:FV<nr1>,] (see 2445/2465 Option 10 GPIB Option Operators Manual); where <nr1> is the version number of the C/T/T Option.
LTRigger	ASWeep:	AANdb AORb WREcognizer	This command configures the Logic-Trigger function If the Word Recognizer Option is not installed and if either the ASW: WRE, or BSW: WRE command is received, then an option-not-installed SRQ error is sent.
	BSWeep:	WREcognizer	
LTRigger?			Query response is: LTR ASW: string or LTR BSW: WRE.
RESolution	AUTO R1Ns R100ps R10Ps		This command sets the resolution of precision measurements.
RESolution?			Query response is : RES string.

Table 2-4
Word Recognizer GPIB Commands

Header	Argument	Argument	Comments
WREcognizer	CLOck:	ASYnch DNClock UPClock	This command configures the Word Recognizer.
	RADix:	BINary HEX OCTal	The RADix: argument only controls the format of the Word Recognizer settings display on the crt.
	WORd:	<ASCII binary data>	The format of ASCII binary data is #Y followed by 17 digits, where each digit may be either 0, 1, or X (don't care). Spaces may be used anywhere to separate groups of digits. The option will accept ASCII binary data command arguments without the #Y prefix. The following are all valid and equivalent: WOR: #Y1 00X01X10 0X0X110X, WOR: #Y100X01X100X0X110X, WOR: 1 00X0 1X10 0X0X 110X, WOR: #Y1 0 0X0 1X1 00X 0X1 10X The order of the digits is: qualifer bit, then a 16-bit wod in most-significant to least-significant bit order. All 17 digits must be sent. If an error is detected in the ASCII binary data argument, a command-argument SRQ error is sent. If the Word Recognizer Option is not installed and any word recognizer command or query is received, an option-not-installed SRQ error is sent.
WREcognizer?	CLOck RADix WORd		Query response is: WRE RAD: string, CLO: string, WOR:<ASCII binary data>. An example of the output format of WRE? WOR is: WOR: #Y1 00X01X10 0X0X110X.

OPERATOR'S CHECKS

INTRODUCTION

To verify the operation and accuracy of your instrument before making measurements, perform the following check procedures. If indications specified in these procedures cannot be obtained, refer the instrument to a qualified service technician.

Before proceeding with these instructions, refer to "Preparation for Use" in this section and in Section 2 of the standard instrument's Operators manual.

Verify that the POWER switch is OFF (push button out); then plug the power cord into a power outlet.

NOTE

The initial setup, all verifications, and each step within them must be performed in the sequence presented and in their entirety to ensure that control settings are correct for the following step.

INITIAL SETUP

1. Press in the POWER switch button (ON) and allow the instrument to warm up for 20 minutes.

2. If an A TRIGGER MODE indicator is illuminated, push the A/B/MENU switch.

3. Push the TRIGGER MODE switch down to deactivate any MENU selected function.

4. Set instrument controls to obtain a baseline trace as follows:

Vertical

CH 1 POSITION	Midrange
MODE	CH 1
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	10 mV
CH 1 Input Coupling	1 MΩ DC

Horizontal

A AND B SEC/DIV	Locked together at 50 ms
SEC/DIV VAR	Calibrated detent
POSITION	Midrange
X10 MAG	Off (button out)
Δt and ΔV	Off (press and release until readout display disappears)

Trigger

HOLDOFF	Fully counterclockwise
LEVEL	Midrange
A MODE	AUTO
A and B SOURCE	VERT
A and B COUPLING	DC
A and B SLOPE	+

5. Adjust the INTENSITY, READOUT INTENSITY, and FOCUS controls for desired display and readout brightness and best trace definition.

6. Connect a 10X probe to the CH 1 OR X input connector and connect the probe tip the the CALIBRATOR output.

7. Adjust the Vertical and Horizontal POSITION controls to position the trace within the graticule area.

8. Adjust the A TRIGGER LEVEL to 0.200 V.

FREQUENCY VERIFICATION

1. Enter MENU mode (see "Menu Mode Function Selection" in this section).

2. Use the Δ REF OR DLY POS control to underline **COUNT**.

3. Push up on the TRIGGER MODE switch.

4. Use the Δ REF OR DLY POS control to underline **MODE**.

5. Use the Δ control to underline **FREQ**.

6. If the instrument contains the Word Recognizer Option:

a. Use the Δ REF OR DLY POS control to underline **EVT**.

b. Use the Δ control to underline **A**.

7. Push up on the TRIGGER MODE switch.

8. Verify the displayed frequency is between 9.99 Hz and 10.01 Hz.

9. Exit Menu mode (see "Menu Mode Function Selection" in this section).

DELAY VERIFICATION

1. Select AUTO Resolution (see "Resolution Selection" in this section).

2. Set the A AND B SEC/DIV switches to 0.5 μs.

3. Pull out the B SEC/DIV switch.

4. Set the B TRIGGER MODE to TRIG AFT DLY.

5. Adjust the B TRIGGER LEVEL to 0.200 V.

6. Move the intensified zone as far left as possible using the Δ REF OR DLY POS control.

7. Verify the displayed delay is between 989.5 ns and 1010.5 ns.

DELTA VERIFICATION

1. Select the delta time mode using the Δt switch.

2. Move the intensified zone as far left as possible using the Δ REF OR DLY POS control.

3. Move the second intensified zone two divisions to the right of the first intensified zone using the Δ control.

4. Verify the displayed delta time is between 999.0 ns and 1001.0 ns.

5. Deselect the delta time mode using the Δt switch.

6. Lock together the A AND B SEC/DIV switch.

DELAY-BY-EVENTS

1. Set the A TRIGGER SLOPE to −.

2. Enter Menu mode.

3. Use the Δ REF OR DLY POS control to underline **DLY/EVTS**.

4. Push up on the TRIGGER MODE switch.

5. Use the Δ REF OR DLY POS and Δ controls to select SWP B, START A, DLY BY B (see "Delay-by-Events" in this section).

6. Push up on the TRIGGER MODE switch.

7. Pull out the B SEC/DIV switch.

8. Use the Δ REF OR DLY POS and the Δ controls to set the number of delaying events to 1.

9. Verify that the intensified zone moves to each succeeding rising edge as the delaying event count is changed to 2, 3, 4, and 5.

THEORY OF OPERATION

INTRODUCTION

SECTION ORGANIZATION

This section contains a functional circuit description of the Option 06 Counter/Timer/Trigger (C/T/T) and Option 09 Counter/Timer/Trigger with Word Recognizer (WR) circuitry for the 2445 and 2465 Oscilloscopes. The discussion begins with an overview of option functions and continues with detailed explanations of each major circuit. Reference is made to supporting schematic and block diagrams which aid in understanding the text. These diagrams show interconnections between parts of the circuitry, identify circuit components, list specific component values, and show interrelationships with the standard oscilloscope.

The block and schematic diagrams are located in the tabbed "Diagrams" section at the rear of this manual. The particular schematic diagram associated with each circuit description is identified in the text, and the diagram number is shown (enclosed within a diamond symbol) on the tab of the appropriate foldout page. For the best understanding of the circuit being described, refer to both the applicable schematic and block diagrams.

DIGITAL LOGIC CONVENTIONS

Digital logic circuits perform many functions within the instrument. The operation of these circuits is represented by specific logic symbology and terminology. Logic-function descriptions contained in this manual use the positive-logic convention. The specific voltages which constitute a HI or a LO vary between individual devices. For specific device characteristics, refer to the manufacturer's data book.

GENERAL CIRCUIT DESCRIPTION

Before individual circuits are discussed in detail, a general block-level discussion is provided to aid in understanding overall operation of the option circuitry. A simplified block diagram of the option, showing basic interconnections, is shown in Figure 7-2. The diamond-enclosed numbers in the blocks refer to the schematic diagrams at the rear of this manual in which the corresponding circuitry is located. Throughout this discussion, standard oscilloscope refers to the 2445 and 2465 Oscilloscopes without option circuitry.

The activities of the options are directed by the microprocessor contained in the standard oscilloscope. The microprocessor, under the control of firmware present in the options, monitors each option's functions and sets up the operating modes according to instructions received.

While executing the control program, the microprocessor retrieves previously stored calibration constants and front-panel settings and, as necessary, places program-generated data in temporary storage for later use. The electrically alterable read-only memory (EAROM), random access memory (RAM), and ultraviolet erasable programmable read-only memory (EPROM) contained in the Buffer and option circuit boards provide these storage locations.

BUFFER BOARD

The option circuit board connects to the standard oscilloscope through the Buffer circuit board. The Buffer board performs the following functions:

1. Buffers and modifies the timing of the microprocessor bus.
2. Distributes the microprocessor bus, power supplies, and analog signals from the standard oscilloscope to the options.
3. Provides additional ROM for interfacing options to the standard instrument.
4. Provides an EAROM for options use.
5. Provides a mechanical interface.

The microprocessor control bus, address bus, and data bus are buffered by Buffer board circuitry. Microprocessor bus timing for the options is modified by buffers on the Buffer board to make bus timing compatible with the options. The EAROM bus allows the microprocessor to access the option EAROM located on the Buffer board. Address bus decoding allows individual circuits to be addressed.

These signal paths are used for communications between the options and the standard oscilloscope and involve both data and control signals. The standard oscilloscope circuitry uses them to control the options. The options use them to send information to the standard oscilloscope for display and to control the standard oscilloscope.

C/T/T BOARD

The C/T/T board utilizes signals from the standard instrument and the Word Recognizer to produce accurate measurements for display. Functionally the C/T/T circuitry is divided into four blocks:

1. Microprocessor interface.
2. Time base.
3. Counters and gating.
4. Word Recognizer interface and control.

The microprocessor interface contains the bus buffers, memory, registers, and address decoding that allows the microprocessor in the standard oscilloscope to control the option.

The time base contains the Oscillator and Phase-Locked Loop circuitry which provides the 131 MHz reference clock for the counters and the 5.24 MHz clock used by the counter-reloading state machine for the Delay-by-Events functions.

The Complex Counter integrated circuit (IC) is configured as three counters. The least significant bits of each counter are contained in the gate array.

For the counting and timing functions, the microprocessor initializes the circuitry by writing to registers. The contents of the registers, in turn, cause the proper input signals to be selected and applied to the counters through level shifting and multiplexing circuitry. Once the system is initialized, the microprocessor allows the counters to start when they see the proper edge of the selected start signal. When the selected edge of the stop signal is detected, the counters stop and the microprocessor reads the counters, calculates, and then displays the measurement. The process is then repeated.

The procedure just described is different in Totalize mode. In Totalize, the count is read and displayed by the microprocessor while counting is actively occurring. The count is reset from the front panel.

Logic Trigger functions use the Gate Array to perform logic functions on the A and B triggers. The result of the logical combination triggers the standard instrument.

WORD RECOGNIZER

The Word Recognizer provides an external 17-bit combinational trigger input to the C/T/T. Input data matching states are individually selectable via the oscilloscope front panel to match either a logic 0, 1, or don't care (X). Either a rising or falling clock edge may be selected as the active edge in synchronous mode.

Control Register

The Control Register is a serial input, parallel output register, controlled by the microprocessor, that controls the circuitry in the Word Recognizer probe. Desired input match bits (WDATA) are clocked into the Control Register by WCLOCK. Forty clocks after a data bit is shifted into the Control Register, it appears on the DATA RTRN output. This output is used to:

1. Detect if the WR is plugged into the oscilloscope.
2. Detect if the shift register was clocked extra times by static or other transients.
3. Perform diagnostic tests of WR circuitry.

Seventeen control register bits (don't cares) determine if the input gating will allow the 17 input signals to reach the Comparator. Seventeen other control register bits determine whether the Comparator will look for a matching HI or LO on the corresponding input from the input gating. When all data inputs from the input gating match the control register bits, the Comparator sends a LO to the Synchronizer and the Output Multiplexer.

Synchronizer and Output Multiplexer

The Synchronizer synchronizes the Comparator's output with the external clock input (C). A control bit selects the active edge of the Synchronizer's clock input.

The Output Multiplexer selects either the Synchronizer's output or the Comparator's output to pass on to the C/T/T. One bit of the Control Register selects either synchronous or asynchronous mode. If asynchronous mode is selected, the Output Multiplexer transfers the Comparator's output via the $\overline{\text{WORD}}$ signal to the C/T/T. If synchronous mode is selected, the Output Multiplexer selects the Synchronizer's output instead of the Comparator's output to pass on to the C/T/T. In the C/T/T, the $\overline{\text{WORD}}$ signal is sent to the WORD RECOG OUT connector and also to the Level Shifting and Multiplexing circuitry where it can be selected as one of the trigger events.

DETAILED CIRCUIT DESCRIPTION

INTRODUCTION

The following discussion provides detailed information concerning the electrical operation and circuit relationships of the 2445 and 2465 Buffer board, Counter/Timer/Trigger, and Word Recognizer circuitry. Unique circuitry is described in detail, while circuits common in the electronics industry are not. The descriptions are accompanied by supporting illustrations and tables.

BUFFER BOARD DIGITAL DISTRIBUTION

The Buffer Board Digital Distribution circuitry (see Diagram 20) interconnects the standard oscilloscope and the C/T/T board. Most of the microprocessor signals are buffered and have their timing modified. In addition, some of the memory used for option functions is included on the Buffer board.

Electrically Alterable ROM

Nonvolatile storage for the calibration constants and power-down settings is provided by EAROM U4207. By using different clock sources, the microprocessor is able to select either EAROM U2008 in the standard oscilloscope or Buffer board EAROM U4207. The clock source for the Buffer board EAROM comes from U2308 pin 5 (see Diagram 2 in the standard oscilloscope service manual). Mode control inputs C1 and C3 are interchanged between the two EAROMs to prevent data contention. A TTL-to-MNOS level shift of the clock signal is provided by Q4201. For additional information on EAROM operation, consult the "Theory of Operation" section of the standard oscilloscope service manual.

Address Decoding

Gates U4240A and U4240C partially decode the address bus. Enable BVMA U4240C pin 8 is HI for addresses from 1000-7FFF (this and all other address references are in hexadecimal), the address space used by the options including the Buffer board.

Enable $\overline{\text{BUFEN}}$ U4250C pin 8 is LO for the address space of 1000-1FFF. Address strobe $\overline{\text{LOWAD}}$ is active LO for the address space of XFFC-XFFF (where X is a don't care). These decoded address signals are used in selecting ROM U4260 on the Buffer board and disabling data bus buffer U4255.

Buffer Board ROM

Buffer board ROM U4260 is used to interface the option to the standard oscilloscope. Its output enable (at pin 20) is $\overline{\text{ROMEN}}$. The signals $\overline{\text{ROMEN}}$ and $\overline{\text{BUFEN}}$ are the same if P4256 is present. With $\overline{\text{ROMEN}}$ and $\overline{\text{BUFEN}}$ the same, the Buffer board ROM address space is 1000-1FFF. Whenever the Buffer board ROM is addressed, shift register U4275 (that controls the data bus buffer) is reset by $\overline{\text{ROMEN}}$. This prevents the Buffer board data bus buffer and the Buffer board ROM from driving the microprocessor side of the data bus at the same time.

With Option 01 (DMM) to the 2445 and 2465 installed, P4256 is not installed. In this case $\overline{\text{BUFEN}}$ is further decoded by circuitry in the DMM. The $\overline{\text{ROMEN}}$ signal produced makes the Buffer board ROM active over the address space of 1000-1FFB.

Bus Buffers

The 10MHz clock signal of the standard oscilloscope is buffered by U4265D. The buffered clock (B10MHZ) clocks shift register U4275 and is also sent to the options.

The $\overline{\text{E}}$ clock, $\overline{\text{RESET}}$, VMA, and R/$\overline{\text{W}}$ are buffered by latch U4225. The pull-up on U4225 pin 12 allows $\overline{\text{RESET}}$ and $\overline{\text{E}}$ to pass through the latch unmodified. The buffered E clock is delayed >30 ns by R4265, C4265, and U4265C. This delayed BE clock latches $\overline{\text{VMA}}$, R/$\overline{\text{W}}$ (U4225) and the address bus (U4235 and U4245), which provides extra hold time on these signals for the options.

Data Bus Buffer

Data bus buffer U4255 is a bidirectional bus driver that is controlled by the signals on pin 1 and pin 19. Pin 1 controls the direction of data flow through the buffer, and pin 19 turns the drivers on and off. When pin 1 is HI, the buffer is configured to drive data from the microprocessor to the options. Conversely, when pin 1 is LO, the buffer is configured to drive data from an option to the microprocessor. Pin 1 is HI, except when the microprocessor is reading data from an option.

Signals on pin 1 and pin 19 coordinate the states of U4255 so that data bus contention never occurs. Buffer U4255 drives two buses: the bus between U4255 and the Control board of the standard oscilloscope, and the bus between U4255 and the options. Both of these must be kept free of contentions (i.e., it is not allowed for more than one device to drive the bus at the same time). These two buses will be examined individually.

The bus between the Control board and U4255 is driven by the Control board during a write bus cycle, driven by the Control board during a read cycle from non-option space (0000-0FFF and 8000-FFFF), driven by U4255 during a read cycle from option space (2000-7FFF), and driven by U4260 during a read from Buffer board ROM (1000-1FFF). The Control board changes its drivers from output to input on the rising edge of E (this is the HI-true E, not the LO-true $\overline{E}$ used by the option) when going from a write to a read cycle. It changes from input to output on the falling edge of R/W when going from a read to a write cycle. Data buffer U4255 drives the Control board data bus only when BVMA and BR/$\overline{W}$ are both true; i.e., a read cycle from the option is being performed. This is done by driving U4255 pin 1 from BVMA NANDed with BR/$\overline{W}$ (after passing through a delay consisting of two cycles of the 10 MHz clock). Pin 19 of U4255 is driven by $\overline{E}$ delayed for two cycles of the 10 MHz clock. This two-cycle delay ensures that U4255 will be driving the Control board data bus only in a read cycle from option address space, during a time interval starting after the rising edge of E and ending after the falling edge of E. A delay of two cycles of the 10 MHz clock is necessary to guarantee that the Control board data bus drivers have turned off before U4255 starts driving the bus. This is a period of time when the Control board never drives the data bus during a read cycle. Shift register stages in U4275 are cleared by $\overline{ROMEN}$, forcing U4255 pin 19 HI while Buffer board ROM is being read.

The bus between U4255 and the options must be driven by U4255 during a write cycle to the options (2000-7FFF) and may be driven by an option only during a read cycle from the option (2000-7FFF). Bus driver U4255 actually drives the bus to the option during all cycles except read cycles from 1000-7FFF. The bus is driven by an option only while E is true during an option read cycle. Address bus driver U4255 drives the bus during an option write cycle while U4255 pin 19 is LO, but in this case pin 19 is delayed from $\overline{E}$ only by one cycle of the 10 MHz clock, driving the data to the options as soon as it is available from the microprocessor.

C/T/T CIRCUITRY

Counter/Timer/Trigger circuitry is divided functionally into the microprocessor interface, time base, counters and gating, and the Word Recognizer interface and control. The circuitry is shown on Diagram 26.

Microprocessor Interface

The microprocessor interface contains the circuitry that allows the microprocessor in the standard oscilloscope to control the option.

DATA BUS BUFFER. Bi-directional buffer U5940 buffers the data bus and has two control inputs. Direction control (pin 1) is provided by the microprocessor's buffered read/write signal BR/$\overline{W}$. The buffer is enabled at pin 19 whenever the C/T/T is selected and an address in the 4000-7FFF range is generated.

OPTION SELECT REGISTER. Whenever there is a write to an address in the 7FC0 to 7FFF range, data bus line BBD7 is latched by the Option Select flip-flop (U6252A). When the Option Select flip-flop is set, the C/T/T circuitry responds to addresses in the 4000-7FFF range. When the flip-flop is reset, the C/T/T only responds to microprocessor bus signals in the range of 7FC0-7FFF (the Option Select flip-flop).

MEMORY AND I/O DECODERS. The upper 128 bytes of C/T/T address space are decoded by U5942. The upper half of these locations enable the Option Select flip-flop. The lower 64 addresses are further decoded by address decoder U5950 to allow addressing of individual C/T/T I/O devices. While U5942 allows selection of C/T/T I/O devices, it also prevents (through U6150A) EPROM U5930 from appearing on the bus at these locations.

Address decoder U5950 decodes the option I/O space. Address space for C/T/T I/O devices extends from 7F80 to

7FBF. Due to incomplete address bus decoding, each output of this decoder appears eight times in the address space. A memory map of the C/T/T Option is shown in Table 3-1.

Table 3-1

C/T/T and WR Memory Map

Address	Device Description
4000-7F7F	ROM
7F80-7F83	Gate Array register 2 (MCA-2), write only
7F84-7F87	Gate Array register 1 (MCA-1), write only
7F88-7F8B	Gate Array register 3 (MCA-3), write only
7F8C-7F8F	Not used
7F90-7F91	Complex Counter data register (AM-RD), read only
7F92-7F93	Complex Counter status register (AM-RS), read only
7F94-7F95	Complex Counter data register (AM-WD), write only
7F96-7F97	Complex Counter command register (AM-WC), write only
7F98-7F9B	Gate Array status, read only
7F9C-7F9F	Hardware Control register 1 (HW-1), write only
7FA0-7FBF	Images of the above registers
7FC0-7FFF	Option Select register

HARDWARE REGISTER 1. Hardware Register 1 (U5952) is written to by the microprocessor. Four of its outputs control multiplexing of signals to the Gate Array. The other four outputs are control data inputs to the Gate Array.

STATUS REGISTER. Register U6250 is a 3-state bus driver. This register is read by the microprocessor to determine the status of the WR and the Gate Array. The Gate Array status (O0, O1, O2) is first converted to TTL by U6290 before being sent to U6250.

PAGED EPROM. A 32k-byte EPROM provides storage for C/T/T firmware. Since the option is allowed only 16k-bytes of address space, an output of the Complex Counter (U6140 pin 2) divides the EPROM address space into two 16k-byte pages. The EPROM is enabled (pin 20) when the Option Select flip-flop is set and addresses from 4000-7FFF appear on the address bus. Except for the top 128 bytes of C/T/T address space (the address space used by the Option Select Register), the EPROM outputs are enabled over the same address range (4000-7F7F).

Time Base

The Time Base consists of an oscillator, divider, and phase-locked loop. It generates the clocks used by the rest of the circuitry.

OSCILLATOR. The TTL-compatible 13.10669 MHz oscillator (Q5921 and Q5920) performs two functions:

1. It provides the Gate Array with a clock for the Delay-by-Events End-of-Sweep Counter-Reloading state machine.

2. It provides a 1.310669 MHz reference to the Phase-Locked Loop through divider U5910.

DIVIDER. Divider U5910 divides the 13.10669 MHz clock by 2.5, 5, and 10. Complex Counter U6140 uses the 2.62134 MHz (U5910 pin 8), while the Phase-Locked Loop uses the 1.310669 MHz output (U5910 pin 12) as a reference. The 5.24267 MHz output goes to the Gate Array as the state machine clock.

PHASE-LOCKED LOOP. The Phase-Locked Loop consists of phase comparator U6010, loop filter U6230, voltage controlled oscillator (VCO) U6120, and divider U6130.

Phase comparator U6010 has two 1.310669 MHz inputs. The first (pin 1) is the divided output of the 13.10669 MHz oscillator, while the second (pin 3) is the divided output of the VCO. The output of the phase comparator (pins 5 and 10) goes to the loop filter. A voltage reference (pin 8) is also supplied by the phase comparator to the loop filter. The phase comparator adjusts the frequency of the VCO so that the falling edges of the reference and feedback inputs of the phase comparator are coincident.

Loop filter U6230 is an active filter. Resistor R6232 and capacitor C6232 make up the filter's feedback path. Buffered address bit 0, through R6222, injects about one cycle of phase jitter into the loop to reduce aliasing effects.

Voltage-controlled oscillator U6120 provides a 131.0669 MHz reference to the Gate Array for frequency and time

measurements. The output is also divided by 100 by U6130 and fed back to the phase comparator. Voltage-variable-capacitor CR6210 and inductor L6210 are the external tank circuit for the oscillator, with CR6210 also being the oscillator's tuning element.

Counters and Gating

The Counters and Gating Circuitry contains the Level Shifting and Multiplexing circuitry. It also contains the counters (Gate Array and the Complex Counter) and trigger driver circuitry of the option. The circuitry is discussed as it applies to each input signal; then the counters are discussed.

The A Trigger Status ($\overline{TSA}$) comes from the standard oscilloscope (P6221 pin 2) as an active LO signal driven from a current sink. The standard oscilloscope either sinks 10 mA or presents an open circuit on the line. The signal path to the C/T/T is approximately 75 Ω. Termination on the line is controlled by register HW-1 (U5952 pin 16). If U5952 pin 16 is HI, the termination is 75 Ω to +2.3 V. If pin 16 is LO, the termination is 22K to +5 V.

The 75 Ω termination results in $\overline{TSA}$ being converted to ECL levels (with ECL powered between +5 V and ground) and sent to the Gate Array. For 75 Ω, U5952 pin 16 is HI and holds Q5980 off. Diode CR5970 is reverse biased putting +3 V on the base of Q5981. With +3 V on its base, Q5981 is allowed to conduct. Resistor R5970 and the emitter resistance of Q5981 combine to provide the 75 Ω termination to +2.3 volts. The drive from $\overline{TSA}$ makes the base of Q5982 swing between +4 V and +5 V. Emitter follower Q5982 provides the ECL drive to the Gate Array (U6180 pin 36) and to the multiplexer (U6070 pin 13). The output of U5990A is also kept HI by the HI at U5952 pin 16. This blocks the return path to the standard instrument for $\overline{TSA}$ (P4221 pin 2 to pin 3).

The 22 kΩ termination results in $\overline{TSA}$ being looped through the C/T/T and sent back to the standard oscilloscope (P4221 pin 3). As far as the standard oscilloscope is concerned, the C/T/T does not affect the $\overline{TSA}$ signal.

For 22 kΩ termination, U5952 pin 16 is LO. This turns on Q5980, terminating $\overline{TSA}$ through 22 kΩ. Diode CR5970 is now on, keeping Q5981 off (the 470 kΩ resistor on its emitter prevents Q5981 from turning completely off), preventing $\overline{TSA}$ from reaching the Gate Array and multiplexer. With U5952 pin 16 LO, U5990A allows $\overline{TSA}$ to return to the standard oscilloscope.

The B Trigger Status ($\overline{TSB}$) also comes from the standard oscilloscope (P4221 pin 8). This signal is treated basically the same as $\overline{TSA}$ except:

1. It doesn't go to multiplexer U6070.
2. It has its own multiplexer consisting of Q6091 and Q6092 which selects either $\overline{TSB}$ or $\overline{WORD}$ from the WR, and sends one of them to the Gate Array.
3. There is a 10 kΩ pull up to +15 V on the collector of Q5983 to compensate for the drop through Q6092.

The A Sweep Gate ($\overline{SGA}$) is an active LO TTL signal from the standard oscilloscope (P4221 pin 14). A voltage divider converts it to ECL before it reaches the Gate Array (U6180 pin 33).

The B Sweep Gate ($\overline{SGB}$) is also an active LO TTL signal from the standard oscilloscope (P4221 pin 11). It is also converted to ECL by a voltage divider before it reaches the Gate Array (U6180 pin 8).

The A Hold Off (AHO) and the B Hold Off (BHO) come to the C/T/T (P4221 pin 20 and pin 24) as ECL signals requiring no level shifting. However, AHO is pulled up and clamped to +5 V to compensate for the loading of U6070. Both AHO and BHO go to multiplexer U6070. The AHO signal also goes to the multiplexer through an RC delay (C5961 and R6060). The multiplexer sends the selected hold off signal to the hold off (HO) input of the Gate Array (U6180 pin 2). The HO input of the Gate Array can be forced HI by the microprocessor through U6140 pin 40 and Q6292 to reset the Gate Array trigger hardware.

Delay Select ($\overline{DS}$) is an active LO TTL signal from the standard oscilloscope (P4221 pin 17). Resistors R6172, R6050, and R6277 convert $\overline{DS}$ to ECL and balance currents through CR6170. Balancing the currents reduces cross talk from $\overline{DS}$ on the Gate Array inputs, improving the accuracy of delta-time measurements.

Because gate array U6180 uses emitter coupled logic (ECL), most signals that leave the Gate Array are converted to TTL, and signals entering the Gate Array are converted to ECL. The Gate Array has 9 ECL inputs controlled by the microprocessor: D0, D1, D2, D3, D4, D5, G1, G2, and G3. Each input signal is shifted to ECL by a resistive divider.

Complex counter U6140 has 5 outputs. Four of the outputs (O2, O3, O4, and O5) are controlled by the microprocessor independently of the rest of the IC. The outputs control memory paging, hold off selection, enabling of the B trigger status, and the WR clock respectively. Output O1 is used in Delay-by-Events modes to tell the Gate Array that the terminal count (TC) has been reached. To make certain TC is seen by the Gate Array, TC is latched by U6252B until HO arrives.

GATE ARRAY AND COMPLEX COUNTER. Both the Gate Array (U6180) and the Complex Counter (U6140) are complex multi-function microprocessor-controlled devices. The discussion that follows will describe the basic interconnection of the Gate Array and the Complex Counter. Specific setups for each C/T/T mode are located in accompanying tables.

The circuitry is connected to form three counters. Counter A contains a total of 38 bits; Counter B, 37 bits; and Counter C, 17 bits. Counter use for each mode is shown in Table 3-2. The least significant bits of each counter are in the Gate Array. The emitter-coupled pair (Q6290 and Q6291 for counter A) between the ICs connects the least significant bits of the counters in the Gate Array to the most significant bits of the counters in the Complex Counter. The emitter-coupled pair also converts the Gate Array's ECL signals to TTL for the Complex Counter.

Both the Gate Array and the Complex Counter contain registers which the microprocessor uses to set up the desired operating mode. Hardware Register 1 (HW-1) and two of the Gate Array registers (MCA-1 and MCA-2) are used to select the desired input signals and function. In all modes the microprocessor will initialize the hardware before the function starts. For each function, the content of each register is shown in Table 3-3. The values are hexadecimal except for register MCA-1 where only bits 3 and 2 are shown. Bit 3 enables A AUX TRIG and bit 2 enables B AUX TRIG.

The input signals applied to the Gate Array for each C/T/T mode are shown in Table 3-4. If either the 131 MHz or 5.24 MHz clocks are used by a mode, an "x" appears in its respective column.

Table 3-5 shows the signals used by and buffered by the C/T/T Option for each particular mode. Signals used or buffered by the C/T/T are shown in the "From WR" and "From Standard Instrument" columns. Those signals that are buffered by but not used by the C/T/T in a particular mode and affect the standard instrument are denoted by an *. Signals being produced by or buffered by the C/T/T for each particular mode are shown in the "To Standard Instrument" column.

In Delta Time all three counters are used. Counter A counts cycles of the 131 MHz clock during delay 0. Counter B counts cycles of the 131 MHz clock during delay 1. Counter C counts the number of sweeps that occur. All three counters start counting on the leading edge of the A Sweep Gate ($\overline{SGA}$). On the leading edge of the B Sweep Gate all counters stop counting. When the counters stop, the microprocessor reads the counters and calculates the Delta Time. The microprocessor can then reinitialize the hardware and restart the procedure.

Table 3-2
Counter Use

Mode	A	B	C	Start	Stop
Frequency	131 MHz clock	Frequency being counted		A and B start on selected edge of B	A and B stop on selected edge of B
Totalize		Frequency being counted		MODE switch	Count is reset by movement of any front-panel switch
Delay Time	131 MHz clock		Sweeps	A starts with the A sweep gate	A stops with the B sweep gate
Delta Time	131 MHz clock during delay 0	131 MHz clock during delay 1	Sweeps	A and B start with the A sweep gate	A and B stop with the B sweep gate
Delay-by-Events	Events			Hardware controlled	Hardware controlled

Delay-by-Events mode differs from the other modes by having the Delay-by-Events Counter-Reloading State machine in the Gate Array reload and reenable counter A (the only counter used in Delay-by-Events) at the end of the A sweep. At the end of the delay, the Gate Array also generates $\overline{\text{A AUX TRG}}$ or $\overline{\text{B AUX TRG}}$ to trigger the selected sweep.

Frequency mode uses Counter A and Counter B. Counter A counts the 131 MHz clock while Counter B counts cycles of the unknown signal. Both counters are started and stopped on the selected edge of the unknown signal being measured.

Totalize mode only uses Counter B. The unknown signal is counted by Counter B. The count in B is displayed after being read while counting is actively occurring. When counting is started or restarted, the B Trigger level is run to both its minimum and maximum levels to force a clock edge to enable the count circuitry. This may generate an extra count. If an extra count occurs, it is removed by the microprocessor.

Boolean Trigger mode uses the Gate Array to perform the selected logic function on the A and B triggers. The result of the logical combination of the triggers is sent to the standard instrument as the signal $\overline{\text{A AUX TRG}}$.

WORD RECOGNIZER CIRCUITRY

Word Recognizer circuitry is divided into the following functional blocks: Control Register, Input Gating, Comparator, Output Multiplexer, and Synchronizer. The circuitry is located on Diagram 28. Connector P2732 connects the C/T/T and the WR probe.

Control Register

This 40-bit register consists of five cascaded eight-bit serial input, parallel output shift registers (U6330, U6325, U6420, U6430, and U6425). Pin 2 of U6330 is the Word Recognizer serial data (WDATA) input. The WR clock (WCLOCK) connects to pin 8 of each IC making up the register. Pull up resistor R6492 converts WCLOCK to CMOS input levels. The Control Register's first 36 bits are control bits. The last four control register bits are used to detect extra shifts. The last bit of the Control Register is always set HI, while the preceding three control register bits are set LO. If there are one, two, or three extra control clocks, DATA RTRN (U6425 pin 13) will be LO. A LO DATA RTRN signal indicates, to the microprocessor, an erroneous set up. Table 3-6 lists the function, setup states, and location of each bit of the Control Register.

Table 3-3
Control Register Setup

HW-1	MCA-1	MCA-2	C/T/T Mode
00	00	00	Inactive
C0	08	10	Boolean AND
C0	04	10	Boolean AND, free run
C0	08	00	Boolean OR
C0	04	00	Boolean OR, free run
01	08	08	Word Recognizer, A Sweep
01	04	08	Word Recognizer, A Sweep, free run
03	04	08	Word Recognizer, B Sweep
C0	08	05	A Delay-by-Events (ADBE), start=A, events=B
80	08	05	ADBE, start=A, events=WR
41	08	05	ADBE, start=WR, events=B
01	08	0D	ADBE, start=WR, events=WR
C2	04	04	B Delay-by-Events (BDBE), start=A, events=B
82	04	0C	BDBE, start=A, events=WR
40	00	00	Freq/Totalize A (actually B)
01	08	09	Freq/Totalize WR
00	00	02	Precision Delay
00	00	13	Precision 1/Delta Time
00	00	03	Precision 1/Delta Time with ALT SLP

Table 3-4
Gate Array Inputs

131 MHz	5.24 MHz	$\overline{\text{EXT}}$	$\overline{\text{ATS}}$	$\overline{\text{BTS}}$	$\overline{\text{ASG}}$	$\overline{\text{BSG}}$	HO	$\overline{\text{DS}}$	C/T/T Mode
									Inactive
			$\overline{\text{TSA}}$	$\overline{\text{TSB}}$			AHOD		Boolean AND
			$\overline{\text{TSA}}$	$\overline{\text{TSB}}$			AHOD		Boolean OR
		$\overline{\text{WORD}}$					AHOD		Word trig, A Sweep
		$\overline{\text{WORD}}$					BHO		Word trig, B Sweep
	x	$\overline{\text{TSA}}$		$\overline{\text{TSB}}$			AHOD		ADBE, start=A, events=B
	x	$\overline{\text{TSA}}$		$\overline{\text{WORD}}$			AHOD		ADBE, start=A, events=WR
	x	$\overline{\text{WORD}}$		$\overline{\text{TSB}}$			AHOD		ADBE, start=WR, events=B
	x	$\overline{\text{WORD}}$					AHOD		ADBE, start=WR, events=WR
	x		$\overline{\text{TSA}}$	$\overline{\text{TSB}}$			AHO		BDBE, start=A, events=B
	x	$\overline{\text{WORD}}$	$\overline{\text{TSA}}$				AHO		BDBE, start=A, events=WR
x				$\overline{\text{TSB}}$					Frequency A (actually B)[a]
				$\overline{\text{TSB}}$					Totalize A (actually B)[a]
x		$\overline{\text{WORD}}$							Frequency WR
		$\overline{\text{WORD}}$							Totalize WR
x					$\overline{\text{SGA}}$	$\overline{\text{SGB}}$			Precision Delay Time
x					$\overline{\text{SGA}}$	$\overline{\text{SGB}}$		$\overline{\text{DS}}$	Precision Delta Time
x					$\overline{\text{SGA}}$	$\overline{\text{SGB}}$		$\overline{\text{DS}}$	Precision 1/Delta Time
x					$\overline{\text{SGA}}$	$\overline{\text{SGB}}$		$\overline{\text{DS}}$	Precision Delta Time, ALT SLP
x					$\overline{\text{SGA}}$	$\overline{\text{SGB}}$		$\overline{\text{DS}}$	Precision 1/Delta Time, ALT SLP

[a] B trigger is the same as A trigger and the B events are counted in this mode.

Table 3-5
Signals To/From C/T/T for C/T/T Modes

From WR	From Standard Instrument							To Standard Instrument				C/T/T Mode
$\overline{\text{WORD}}$	$\overline{\text{TSA}}$	$\overline{\text{TSB}}$	$\overline{\text{SGA}}$	$\overline{\text{SGB}}$	AHO	BHO	$\overline{\text{DS}}$	$\overline{\text{AAT}}$[a]	$\overline{\text{BAT}}$[a]	$\overline{\text{TSA}}$	$\overline{\text{TSB}}$	
	*	*								x	x	Inactive
	x	x			x			x				Boolean AND
	x	x			x				x			Boolean AND, free run
	x	x			x			x				Boolean OR
	x	x			x				x			Boolean OR, free run
x	*	*			x			x		x	x	Word trig, A Sweep
x	*	*			x				x	x	x	Word trig, A Sweep, free run
x	*	*				x			x	x	x	Word trig, B Sweep
	x	x			x			x				ADBE, start=A, events=B
x	x	*			x			x			x	ADBE, start=A, events=WR
x	*	x			x			x		x		ADBE, start=WR, events=B
x	*	*			x			x		x	x	ADBE, start=WR, events=WR
	x	x			x				x			BDBE, start=A, events=B
x	x	*			x				x		x	BDBE, start=A, events=WR
	*	x								x		Freq/ Totalize A (actually B)[b]
x	*	*								x	x	Freq/ Totalize WR
	*	*	x	x						x	x	Precision Delay Time
	*	*	x	x			x			x	x	Precision Delta Time

Table 3-5 (cont)
Signals To/From C/T/T for C/T/T Modes

From WR	From Standard Instrument							To Standard Instrument				C/T/T Mode
WORD	TSA	TSB	SGA	SGB	AHO	BHO	DS	AAT[a]	BAT[a]	TSA	TSB	
	*	*	x	x			x			x	x	Precision 1/Delta Time
	*	*	x	x			x			x	x	Precision Delta Time, ALT SLP
	*	*	x	x			x			x	x	Precision 1/Delta Time, ALT SLP

[a]AAT and BAT are actually A AUX TRG and B AUX TRG.

[b]B trigger is the same as A trigger, and the B events are counted in this mode.

Table 3-6
Control Register Setup

IC	Pin	Function	Word Recognizer Status Display[a]	Control Register Bit[a]
U6330	3	Data input 8 match bit	0	H
			1	L
			X	H
U6330	4	Data input 9 match bit	0	H
			1	L
			X	H
U6330	5	Data input 10 match bit	0	H
			1	L
			X	H
U6330	6	Data input 11 match bit	0	H
			1	L
			X	H
U6330	10	Data input 12 match bit	0	H
			1	L
			X	H
U6330	11	Data input 13 match bit	0	H
			1	L
			X	H
U6330	12	Data input 14 match bit	0	H
			1	L
			X	H
U6330	13	Data input 15 match bit	0	H
			1	L
			X	H

[a]X = don't care, H = high, and L = low.

Table 3-6 (cont)

IC	Pin	Function	Word Recognizer Status Display[a]	Control Register Bit[a]
U6325	3	Data input 8 input enable	0	H
			1	H
			X	L
U6325	4	Data input 9 input enable	0	H
			1	H
			X	L
U6325	5	Data input 10 input enable	0	H
			1	H
			X	L
U6325	6	Data input 11 input enable	0	H
			1	H
			X	L
U6325	10	Data input 12 input enable	0	H
			1	H
			X	L
U6325	11	Data input 13 input enable	0	H
			1	H
			X	L
U6325	12	Data input 14 input enable	0	H
			1	H
			X	L
U6325	13	Data input 15 input enable	0	H
			1	H
			X	L

Table 3-6 (cont)

IC	Pin	Function	Word Recognizer Status Display[a]	Control Register Bit[a]
U6420	3	Data input 0 input enable	0 1 X	H H L
U6420	4	Data input 1 input enable	0 1 X	H H L
U6420	5	Data input 2 input enable	0 1 X	H H L
U6420	6	Data input 3 input enable	0 1 X	H H L
U6420	10	Data input 4 input enable	0 1 X	H H L
U6420	11	Data input 5 input enable	0 1 X	H H L
U6420	12	Data input 6 input enable	0 1 X	H H L
U6420	13	Data input 7 input enable	0 1 X	H H L
U6430	3	Data input 0 match bit	0 1 X	H L H
U6430	4	Data input 1 match bit	0 1 X	H L H
U6430	5	Data input 2 match bit	0 1 X	H L H
U6430	6	Data input 3 match bit	0 1 X	H L H
U6430	10	Data input 4 match bit	0 1 X	H L H

Table 3-6 (cont)

IC	Pin	Function	Word Recognizer Status Display[a]	Control Register Bit[a]
U6430	11	Data input 5 match bit	0 1 X	H L H
U6430	12	Data input 6 match bit	0 1 X	H L H
U6430	13	Data input 7 match bit	0 1 X	H L H
U6425	3	Qualifier input enable	0 1 X	L L H
U6425	4	Qualifier match bit	0 1 X	L H H
U6425	5	Clock edge set	↑ ↓ X	L H X
U6425	6	Synchronous/ Asynchronous set	↑ ↓ X	H H L
U6425	10			L
U6425	11			L
U6425	12			L
U6425	13	(first bit sent by C/T/T)		H

[a]X = don't care, H = high, and L = low.

Input Gating

The Input Gating circuitry determines whether or not an input reaches the Comparator.

When don't care is selected for an input, that input is prevented from reaching the Comparator by the Input Gating circuitry. Input gating is performed on data inputs D0-D15 by NAND gates U6310, U6315, U6405, and U6409.

Input gating on the qualifier input is performed by OR gate U6335C. The resistors in series with the qualifier and data inputs provide over-voltage protection for the WR circuitry.

When a NAND gate's don't care input (from the Control Register) is HI, the NAND gate's output will be the inverse of its data input. When a NAND gate's don't care input is LO (don't care), its output is HI, preventing the input data from reaching the Comparator. When the don't care input bit (from the Control Register) for OR gate U6335C pin 10 is LO, its output will equal the qualifier input (Q). When the OR gate's don't care input bit is HI (don't care) the OR gate output will be HI, preventing the qualifier input from reaching the Comparator.

Comparator

The comparison between the data inputs, the qualifier, and their match bits (from the Control Register) is done by the Comparator (U6320, U6415, U6435A, and U6335D). Each comparator input pair is connected to a data and match control line. Comparator U6320 compares data inputs D8-D15 with their control register match bits. Since U6320 pin 1 is tied LO, the IC is always enabled, and the output pin 19 will go LO when all of its input pairs match.

When the Q input equals its control register match bit, pin 3 of U6435 goes LO enabling U6415. Comparator U6415 compares inputs D0-D7 with their control register match bits. When the IC is enabled, its output will go LO when all its input pairs match. The output of both comparators is ORed together by U6335D. Its output (pin 11) will be LO when all comparator input pairs (data and match bit) are equal.

Output Multiplexer

Gating of either the synchronous output signal or the asynchronous comparator output signal to $\overline{\text{WORD}}$ is done by the Output Multiplexer (U6356).

The synchronous output signal is input to the multiplexer on pin 8 of U6356C. The asynchronous comparator output is input to the multiplexer on pin 11 of U6356D. The synchronous control line (Control Register bit 35) goes to pin 12 of U6356D and through resistor R6336 to the base of Q6334. The resistor, transistor, and R6340 form an inverter. When the synchronous control line is HI the transistor is on and saturated. When the synchronous control line is LO the transistor is cut off. When the synchronous control line is HI, U6356C is enabled and the synchronous output U6350A pin 5 is gated to the paralleled $\overline{\text{WORD}}$ driver U6356A and U6356B. When the synchronous control line is LO, the asynchronous gate U6356D is enabled, gating the asynchronous comparator output (U6335D pin 11) to the paralleled $\overline{\text{WORD}}$ driver U6356A and U6356B. The filter between U6356D and U6356A and U6356B slows HI-going edges between U6356 output pin 13 and the NOR gate inputs by between 35 to 60 ns. The LO-going edge is transferred much faster.

Synchronizer

The Synchronizer synchronizes the Comparator's output with the external clock input (C). A bit of the Control Register selects the active edge of the Synchronizer's clock input.

Clock edge selection is performed by U6435B. When edge select is LO (U6435B pin 4), the output clock (U6435B pin 6) will equal the input clock (U6435B pin 5). When edge select is HI, the output clock will be the inverse of the input clock. This insures that synchronizer flip-flop U6350A will always see a rising edge clock.

Synchronizer flip-flop U6350A produces a LO (true) output when input pin 2 is LO on the rising edge of the clock (pin 3). Pin 5 is set back HI when the flip-flop set input (pin 4) is pulsed LO (true). The set input is driven by U6335A. When U6350A pin 5 is LO, the set input will go LO on the falling edge of the clock (U6335A pin 1). Since this makes U6350A pin 5 HI, the set input will return HI (false) readying the synchronizer flip-flop for the next active clock edge.

PERFORMANCE CHECK AND CALIBRATION PROCEDURES

INTRODUCTION

This section contains the Option 06 (Counter/Timer/Trigger) and Option 09 (Counter/Timer/Trigger with Word Recognizer) portion of the instrument's performance check and calibration procedures. The "Performance Check Procedure" is used to check the instrument's performance against the requirements listed in the "Specification" (Section 1). The "Calibration Procedure" is used to restore optimum performance or return the options to conformance with its "Performance Requirements" as listed in the "Specification" (Section 1).

Instrument performance should be checked after every 2000 hours of operation or once each year if used infrequently. A more frequent interval may be necessary if the instrument is subjected to harsh environments or severe usage. The results of these periodic checks will determine the need for recalibration.

Before performing these procedures, ensure that the LINE VOLTAGE SELECTOR switch is set for the ac power source being used (see "Preparation for Use" in Section 2 of the standard instrument's service manual). Connect the instrument to be checked and the test equipment to an appropriate power source.

LIMITS AND TOLERANCES

The tolerances given in these procedures are valid for an instrument that is operating in and has been previously calibrated at an ambient temperature between −15°C and +55°C. The instrument also must have had at least a 20 minute warm-up period. To assure instrument performance, perform all steps in the following procedures at the same ambient temperature. When performing option checks and calibration, it is assumed that the standard instrument meets all of its "Performance Requirements" as stated in the "Specification" (Section 1) of the standard instrument's service manual.

PERFORMANCE CHECK PROCEDURE

This procedure is used to verify proper operation of the options and may be used to determine the need for calibration. This check may also be used as an acceptance test and as a preliminary troubleshooting aid. Perform all steps, both in the sequence presented and in their entirety, to ensure that control settings are correct for the following step.

PREPARATION

Removing the wrap-around cabinet is not necessary to perform this procedure. All checks are made using the operator-accessible front- and rear-panel controls and connectors.

Test equipment listed in Table 4-1 is required to perform this procedure. Since detailed operating instructions for the test equipment are not provided in this procedure, refer to the appropriate test-equipment instruction manual if additional information is required. To assure accurate measurements, it is important that test equipment used for making these checks meet or exceed the specifications described in Table 4-1. When considering use of equipment other than that recommended, use the "Minimum Specification" column to determine whether available test equipment will suffice.

Turn the oscilloscope on by pressing in the POWER button. Check that it enters its normal operating mode and that no error message is displayed on the crt. If an error message is present, have the instrument repaired or calibrated by a qualified service technician before performing this procedure.

Table 4-1

Test Equipment Required

Item No. and Description	Minimum Specification	Examples of Suitable Test Equipment
1. Pulse Generator (2 required)	Frequency: 10 MHz. Pulse width: 50 ns. Pulse width accuracy: 5%. Positive trigger input, 1 V to 5 V into 50 Ω. Positive trigger output, 1 V into 50 Ω. Variable pulse duration.	TEKTRONIX PG 502 Pulse Generator.[a]
2. Time-Mark Generator	Markers: 10 ns to 2 s in a 1-2-5 sequence. Accuracy: ±0.00005%.	TEKTRONIX TG 501A Option 01 Time Mark Generator.[a]
3. Leveled Sinewave Generator	Frequency: 250 kHz to 250 MHz. Accuracy: ± 1 LSD of generator's indicated frequency.	TEKTRONIX SG 503 Leveled Sinewave Generator.[a]
4. BNC Cable (4 required)	Impedance: 50 Ω. Length: 42 in.	Tektronix Part Number 012-0057-01.
5. T connector (2 required)	Connectors: BNC.	Tektronix Part Number 103-0030-00.
6. Adaptor	Connectors: BNC-male-to-subminiature-probe tip.	Tektronix Part Number 013-0195-00.
7. Adaptor (2 required)	Connectors: BNC-male-to-dual-binding post.	Tektronix Part Number 103-0035-00.

[a]Requires a TM 5000-Series power-module mainframe.

COUNTER/TIMER/TRIGGER CHECKS

Initial Control Settings

Control settings not listed do not affect the procedure.

VERTICAL MODE	
CH 1, CH 2, CH 3, CH 4, ADD, and INVERT	Off (buttons out)
CHOP/ALT	ALT (button out)
20 MHz BW LIMIT	Off (button out)
VOLTS/DIV	
CH 1 and CH 2	0.5 V
CH 1 and CH 2 VAR	In detent
CH 3 and CH 4	0.1 V (buttons out)
Input Coupling	
CH 1 and CH 2	50 Ω DC
A and B SEC/DIV	10 ns (knobs locked)
A and B SEC/DIV VAR	In detent
X10 MAG	Off (button out)
Δt and ΔV	Off (press and release until associated readout is off)
TRACKING	Off (button out)
TRACE SEP	Fully CW
TRIGGER	
HOLDOFF	Fully CCW
A and B LEVEL	Midrange
A and B SLOPE	+ (plus)
A MODE	AUTO LVL
B MODE	RUN AFT DLY
A and B SOURCE	VERT
A and B COUPLING	DC
MENU Functions	OFF

1. Check Maximum Input Frequency at Minimum Sensitivity

a. Connect the leveled sinewave generator's output via a 50 Ω cable to the CH 1 input connector.

b. Set generator to produce a 150 MHz, 4 division display.

c. Push the A/B/MENU switch to enter MENU mode.

d. Turn either delta control to underline **COUNT**.

e. Push the TRIGGER MODE switch up.

f. Turn the Δ REF OR DLY POS control to underline **MODE**.

g. Turn the Δ control to underline **FREQ**.

h. Turn the Δ REF OR DLY POS control to underline **EVT**.

i. Turn the Δ control to underline event **A**.

j. Push the TRIGGER MODE switch up to enter Frequency mode.

k. Push the TRIGGER MODE switch up to reinitialize the auto-trigger level.

l. CHECK—Reading is between 149 MHz and 151 MHz and is stable.

2. Check Minimum Sensitivity at 50 MHz

a. Set the generator to produce a 50.0 MHz, 1.3 division display.

b. Push the TRIGGER MODE switch up to reinitialize the auto trigger level.

c. CHECK—Reading is between 49.9 MHz and 50.1 MHz and is stable.

d. Disconnect the test equipment from the instrument.

3. Check Frequency Accuracy

a. Connect the time-mark generator output via a 50 Ω cable to the CH 1 input connector.

b. Set the generator to produce 10-ns time markers four divisions in amplitude.

c. Push the TRIGGER MODE switch up to reinitialize the auto-trigger level.

d. CHECK—Reading is between 99.9995 MHz and 100.0005 MHz.

4. Check Minimum Input Frequency

a. Set the time-mark generator to produce 2-s time markers.

b. Set:

CH 1 VOLTS/DIV	0.1 V
A TRIGGER MODE	NORM
A and B SEC/DIV	50 ms

c. Adjust the A TRIGGER LEVEL control for a stable trigger.

d. CHECK—Reading is between 499.9975 mHz and 500.0025 mHz.

e. Disconnect the test equipment from the instrument.

5. Check Delay Time

a. Set:

CH 1 VOLTS/DIV	0.5 V
CH 1 Input Coupling	GND
A and B SEC/DIV	10 ns
A TRIGGER MODE	AUTO

b. Connect the output of the time-mark generator via a 50 Ω cable to the positive trigger input of the pulse generator.

c. Connect the output of the pulse generator via a 50 Ω cable to the CH 1 input connector.

d. Set the time-mark generator to produce 10-ns time markers.

e. Set the pulse generator to produce a positive 5-ns pulse when externally triggered.

f. Adjust the CH 1 POSITION control to center the Channel 1 display.

g. Set the CH 1 Input Coupling switch to 50 Ω DC.

h. Adjust the pulse generator to produce a 2.5 division peak-to-peak display, centered about ground.

i. Adjust the A TRIGGER LEVEL control for a readout of 0.00 V.

j. Pull out the B SEC/DIV switch.

k. Push the A/B/MENU switch.

l. Set the B TRIGGER MODE switch to TRIG AFT DLY.

m. Adjust the B TRIGGER LEVEL control for a readout of 0.00 V.

n. Turn the Δ REF OR DLY POS control counterclockwise until the intensified zone stops moving to the left.

o. CHECK—Reading is either 59.5 ns to 60.5 ns or 69.5 ns to 70.5 ns.

6. Check Delta Time Accuracy

a. Set the B TRIGGER MODE switch to MENU.

b. Turn either delta control to underline **RES**.

c. Push the TRIGGER MODE switch up.

d. Turn either delta control to underline **10 ps**.

e. Push the TRIGGER MODE switch up.

f. Set the A and B SEC/DIV switches to 1 μs.

g. Push the TRIGGER MODE switch down to enter TRIG AFT DLY mode.

h. Set the time-mark generator to produce 1-μs time markers.

i. Set the pulse generator to produce a positive 0.5 μs pulse when externally triggered.

j. Push and release the Δt switch until the Delta Time readout appears.

k. Turn the Δ control to intensify the rising edge of the second square wave.

l. Turn the Δ REF OR DLY POS control to intensify the rising edge of the second square wave.

m. CHECK—Reading is between +0.00005 μs and −0.00005 μs.

n. Turn the Δ control to intensify the rising edge of the eleventh square wave.

o. CHECK—Reading is between 8.99990 μs and 9.00010 μs.

p. Set the A and B SEC/DIV switches to 0.1 ms.

q. Set the time-mark generator to produce 0.1-ms time markers.

r. Set the pulse generator to produce a positive 50 μs pulse when externally triggered.

s. Turn the Δ control to intensify the rising edge of the eleventh square wave.

t. Turn the Δ REF OR DLY POS control to intensify the rising edge of the second square wave.

u. CHECK—Reading is between +899.996 μs and +900.004 μs.

7. Verify Delay-by-Events

a. Lock together the A and B SEC/DIV knobs.

b. Set the A TRIGGER SLOPE switch to −.

c. Push the Δt switch until the Δt display disappears.

d. Push the A/B/MENU switch.

e. Use either delta control to underline **DLY/EVTS**.

f. Push the TRIGGER MODE switch up.

g. Use the Δ REF OR DLY POS and Δ controls to select SWP B, START A, and DLY BY B.

h. Push up on the TRIGGER MODE switch.

i. Pull out the B SEC/DIV switch.

j. Use the Δ REF OR DLY POS and the Δ controls to set the number of delaying events to 1.

k. VERIFY—That the intensified zone moves to each succeeding rising edge as the delaying event count is changed to 2, 3, 4, and 5.

8. Check Logic Trigger

a. Set the A and B SEC/DIV switches to 10 ns.

b. Set the pulse generator to produce a positive pulse of about 10 ns every 0.1 μs.

c. Set the B TRIGGER MODE switch to TRIG AFT DLY.

d. Set the B TRIGGER SOURCE switch to CH 1.

e. Set the B TRIGGER MODE switch to MENU.

f. Turn either delta control clockwise to underline **LOGIC-TRIG**.

g. Push the TRIGGER MODE switch up.

h. Turn the Δ control to underline **A:A·B**.

i. Push the TRIGGER MODE switch up.

j. Lock together the A and B SEC/DIV knobs.

k. Adjust the B TRIGGER LEVEL control for a readout of 0.00 V.

l. Push the A/B/MENU switch to illuminate an A TRIGGER MODE indicator.

m. Adjust the A TRIGGER LEVEL control for a readout of 1.00 V.

n. Set the CH 1 Input Coupling switch to GND.

o. Turn the CH 1 POSITION control to align the trace with the center horizontal graticule line; do not readjust the CH 1 POSITION control during the remainder of this step.

p. Set the CH 1 Input Coupling switch to 50 Ω DC.

q. Turn the HORIZONTAL POSITION control to align the rising edge of the displayed signal with the intersection of the second vertical graticule and the center horizontal graticule lines.

r. Decrease the duration of the pulse until decreasing the duration any further would produce an unstable display.

s. CHECK—Width of the pulse measured at the center horizontal graticule line is less than 4 ns.

t. Push the TRIGGER MODE switch up.

u. Push the TRIGGER MODE switch down.

9. Verify Alternate Slope

a. Set the pulse generator to produce a positive 50 ns pulse every 0.1 μs.

b. Push the TRIGGER MODE switch up to reinitialize the auto-trigger level.

c. Turn the A and B SEC/DIV switches to 0.2 μs.

d. Pull out the B SEC/DIV knob.

e. Push the A/B/MENU switch.

f. Set the B TRIGGER MODE switch to ALT SLP.

g. CHECK—The B Trigger Level readout is 0.00 V.

h. Push the TRIGGER SLOPE switch to illuminate the – SLOPE indicator.

i. Turn the HORIZONTAL POSITION control to center the display.

j. VERIFY—That the reference cursor intensifies the falling edge of a pulse.

k. VERIFY—That the Δ cursor intensifies the rising edge of a pulse.

l. Disconnect the test equipment from the instrument.

WORD RECOGNIZER CHECKS

1. Initial Setup

a. Set:

VERTICAL	
MODE	
CH 1, CH 2, and CH 3	On (buttons in)
VOLTS/DIV	
CH 1 and CH 2	2 V
CH 3	0.5 V
CH 4	0.1 V
HORIZONTAL	
A and B SEC/DIV	10 ns (knobs locked)
Δt and ΔV	Off (press and release until associated readout is off)
POSITION	Adjust so trigger point is at the third vertical graticule.
TRIGGER	
A SOURCE	CH 1
A MODE	AUTO LVL

b. Connect the + trigger output of pulse generator 1 via a 50 Ω cable to the + trigger input of pulse generator 2.

c. Connect the output of pulse generator 1 via a 50 Ω cable and T connector to the CH 1 input connector. Use the T connector at the CH 1 input.

d. Connect the output of pulse generator 2 via a 50 Ω cable and T connector to the CH 2 input connector. Use the T connector at the CH 2 input.

e. Connect the Word Recognizer probe to the P6407 input connector at the rear of the instrument.

f. Connect a BNC-male-to-dual-binding post adaptor to the T connector on the CH 1 input, and connect another BNC-male-to-dual-binding post adaptor to the T connector on the CH 2 input.

g. Connect a 4-inch bare wire (suitable for connecting a scope probe) to the red binding post of the adaptor connected to the CH 1 input.

h. Connect a 4-inch bare wire (suitable for connecting a scope probe) to the red binding post of the adaptor connected to the CH 2 input.

i. Connect a 2-inch bare wire (suitable for connecting a scope probe) to the black binding post of the adaptor connected to the CH 2 input.

j. Connect both ground leads from the Word Recognizer probe to the bare wire on the black binding post on the CH 2 input.

k. Connect the CH 3 input to the WORD RECOG OUT connector using a P6131 probe and a BNC-male-to-probe-tip adaptor.

l. Set pulse generator 1 to produce a positive 0.5 μs pulse every 1 μs.

m. Set pulse generator 2 to produce a positive 400 ns pulse when it receives an external trigger.

NOTE

The lowest point of the HI must not be lower than 2.0 V.

n. Set both pulse generators to produce pulses of +0.6 V LO and +2.0 V HI.

o. Push the A/B/MENU switch.

p. Use the Δ REF OR DLY POS control to underline **LOGIC-TRIG**.

q. Push up on the TRIGGER MODE switch.

r. Turn either delta control to underline **B:WR**.

s. Push up on the TRIGGER MODE switch.

t. Turn the Δ REF OR DLY POSITION control to underline **RADIX**.

u. Turn the Δ control to underline **HEX**.

v. Push up on the TRIGGER MODE switch.

w. Connect the clock (C) input of the Word Recognizer to the wire on the red binding post of the CH 1 input.

x. Connect the Q and W0-W15 inputs of the Word Recognizer to the wire on the red binding post of the CH 2 input.

2. Check Data Setup Time

a. For each test setup described in Table 4-2:

1. Vary (increase) the pulse duration of pulse generator 2 until the active edge of the channel 2 signal falls about 10 ns after the trigger edge of the channel 1 signal.

2. CHECK—Channel 3 is not displaying a signal.

3. Vary (decrease) the pulse duration of pulse generator 2, moving the active edge of the channel 2 signal to the left until channel 3 displays a stable signal.

4. Push the Δt switch.

5. Turn the Δ REF OR DLY POS control to align the delta reference cursor with the first edge of the channel 2 signal.

6. Turn the Δ control to align the delta cursor with the first edge of the channel 1 signal.

7. CHECK—Reading is ≤ 25 ns.

8. Push the Δt switch.

Table 4-2

Data Setup Time Checks

Polarity		Word Recognizer Word Definition	A TRIGGER SLOPE
Pulse Generator 1	Pulse Generator 2		
+	+	↓-0-0000	−
+	−	↓-1-FFFF	−
−	−	↑-1-FFFF	+
−	+	↑-0-0000	+

Table 4-3

Data Hold Time Checks

Polarity		Word Recognizer Word Definition	A TRIGGER SLOPE
Pulse Generator 1	Pulse Generator 2		
+	+	↓-1-FFFF	−
+	−	↓-0-0000	−
−	−	↑-0-0000	+
−	+	↑-1-FFFF	+

3. Check Data Hold Time

a. For each test setup described in Table 4-3:

1. Vary the pulse duration of pulse generator 2 until the first edge of the channel 2 signal falls about 10 ns after the trigger edge of the channel 1 signal.

2. CHECK—A stable signal is displayed on channel 3.

3. Vary the pulse duration of pulse generator 2, moving the first edge of the channel 2 signal to the left until channel 3 no longer displays a stable signal.

4. Push the Δt switch.

5. Turn the Δ REF OR DLY POS control to align the delta reference cursor with the first edge of the channel 2 signal.

6. Turn the Δ control to align the delta cursor with the first edge of the channel 1 signal.

7. CHECK—Reading is > 4 ns.

4. Check Minimum Clock Pulse Width

a. Set pulse generator 1 to produce a 5-ns positive pulse every 1 μs.

b. Push the A/B/MENU switch.

c. Push the TRIGGER MODE switch up to reinitialize the auto-trigger level.

d. Push the A/B/MENU switch.

e. For each test setup described in Table 4-4:

1. If there is not a stable signal displayed on channel 3, vary (increase) the pulse duration of pulse generator 1 until channel 3 displays a stable signal.

2. Push the Δt switch.

3. Turn the Δ REF OR DLY POS control to align the delta reference cursor with the leading edge of the channel 1 pulse.

4. Turn the Δ control to align the delta cursor with the trailing edge of the channel 1 pulse.

5. CHECK—Reading is ≤ 20 ns.

6. Push the Δt switch.

5. Check Delay from Selected Edge to WORD RECOG OUT

a. Set:

CH 3 VOLTS/DIV	0.1 V
A and B SEC/DIV	20 ns

b. Connect a P6131 probe to the CH 4 input connector and the probe tip to the wire on the red binding post of the CH 1 input.

c. Set pulse generator 1 to produce a 50-ns positive pulse every 5 μs.

d. Set the A TRIGGER SOURCE switch to CH 4.

e. For each test setup described in Table 4-5:

1. Push the Δt switch.

Table 4-4

Minimum Clock Pulse Width Checks

Polarity			
Pulse Generator 1	Pulse Generator 2	Word Recognizer Word Definition	A TRIGGER SLOPE
+	+	↓-X-XXXX	+
−	+	↓-X-XXXX	−

Table 4-5

Delay From Selected Edge to WORD RECOG OUT Checks

Polarity			
Pulse Generator 1	Pulse Generator 2	Word Recognizer Word Definition	A TRIGGER SLOPE
+	+	↑-X-XXXX	+
−	+	↓-X-XXXX	−

2. Turn the Δ REF OR DLY POS control to align the delta reference cursor with the active edge of the channel 4 signal.

3. Turn the Δ control to align the delta cursor with the rising edge of the channel 3 signal.

4. CHECK—Reading is ≤ 55 ns.

5. Push the Δt switch.

6. Check Word Recognition Delay

a. Set pulse generator 1 to produce a positive 0.5 μs pulse every 1 μs.

b. Disconnect the C input of the Word Recognizer from the wire on the red binding post of the CH 1 input.

c. Connect the Q and W0-W15 inputs of the Word Recognizer to the wire on the red binding post of the CH 1 input.

d. For each test setup described in Table 4-6:

1. Push the Δt switch.

2. Turn the Δ REF OR DLY POS control to align the delta reference cursor with the first edge of the channel 4 signal.

3. Turn the Δ control to align the delta cursor with the rising edge of the channel 3 signal.

4. CHECK—Reading is ≤ 140 ns.

5. Push the Δt switch.

e. Disconnect the probe on the CH 4 input.

7. Check Data Input Coincidence

a. Set pulse generator 1 to produce a positive 0.5 μs pulse every 1 μs.

b. Set pulse generator 2 to produce a negative 400 ns pulse when it receives an external trigger.

c. Set:

A and B SEC/DIV	20 ns
A TRIGGER SOURCE	CH 2
A TRIGGER SLOPE	−

d. Set the Word Definition of the Word Recognizer probe to BX0 0000.

e. Connect the Q and W0-W15 inputs of the Word Recognizer to the wire on the red binding post of the CH 2 input.

Table 4-6

Word Recognition Delay

Polarity		Word Recognizer Word Definition	A TRIGGER SLOPE
Pulse Generator 1	Pulse Generator 2		
+	+	X-1-FFFF	+
−	+	X-0-0000	−

f. Vary (increase) the pulse duration of pulse generator 2 until channel 3 displays a stable signal.

g. Push the Δt switch.

h. Turn the Δ REF OR DLY POS control to align the delta reference cursor with the falling edge of the channel 2 signal.

i. Turn the Δ control to align the delta cursor with the rising edge of the channel 2 signal.

j. CHECK—Reading is ≥ 20 ns and ≤ 85 ns.

k. Push the Δt switch.

l. Disconnect the test setup.

m. Push the TRIGGER MODE switch down.

CALIBRATION PROCEDURE

The "Calibration Procedure" is used to restore optimum performance or return the options to conformance with their "Performance Requirements" as listed in the "Specification" (Section 1). The options should be calibrated only when the standard instrument is known to meet its "Performance Requirements" as stated in the "Specification" section of its manual. Performing this procedure while the instrument's temperature is drifting may cause erroneous calibration settings.

Remove the wrap-around cabinet from the instrument as described in the "Maintenance" section of the standard instrument Service manual. Then set the CAL/NO CAL jumper P501 in the standard instrument to the CAL position (between pins 1 and 2).

Turn the oscilloscope on by pressing in the POWER button. Check that it enters its normal operating mode and that no error message is displayed on the crt. If an error message is present, have the instrument repaired or calibrated by a qualified service technician before performing this procedure.

COUNTER/TIMER/TRIGGER CALIBRATION PROCEDURE

Equipment Required (see Table 4-1):

Pulse Generator (Item 1)

Time-Mark Generator (Item 2)

BNC Cable (2 required) (Item 4)

Initial Oscilloscope Control Settings.

Control settings not listed do not affect the procedure.

Set:

VERTICAL MODE	
CH 1, CH 2, CH 3, CH 4, ADD, and INVERT	Off (buttons out)
CHOP/ALT	ALT (button out)
20 MHz BW LIMIT	Off (button out)
VOLTS/DIV	
CH 1 and CH 2	0.2 V
CH 1 and CH 2 VAR	In detent
CH 3 and CH 4	0.1 V (buttons out)
Input Coupling	
CH 1 and CH 2	50 Ω DC
A and B SEC/DIV	10 ns (knobs locked)
A and B SEC/DIV VAR	In detent
X10 MAG	Off (button out)
Δt and ΔV	Off (press and release until associated readout is off)
TRACKING	Off (button out)
TRACE SEP	Fully CW
TRIGGER	
HOLDOFF	Fully CCW
A and B LEVEL	Midrange
A and B SLOPE	+
A MODE	AUTO LVL
B MODE	RUN AFT DLY
A and B SOURCE	VERT
A and B COUPLING	DC

a. Connect the output of the time-mark generator via a 50 Ω cable to the positive trigger input of the pulse generator.

b. Connect the output of the pulse generator via a 50 Ω cable to the CH 1 input connector.

c. Set the pulse generator to produce a positive 0.5 μs pulse when externally triggered.

d. Set the time-mark generator to produce 1-μs time markers.

e. Adjust the pulse generator to produce a 5-division display centered about ground.

f. Push the TRIGGER SLOPE switch while holding in both the ΔV and Δt switches to access the Diagnostic Menu.

g. Repeatedly push the TRIGGER MODE switch up until the message **CT CAL 81** appears in the Diagnostic Menu of the crt readout.

NOTE

If the calibration feature is disabled (the CAL/NO CAL jumper is in the NO CAL position), CAL messages will not appear in the Diagnostic Menu of the crt readout.

h. Push the TRIGGER COUPLING switch up.

i. CHECK—The message **1 MHZ CH1 1VOLT PEAK TO PEAK** appears in the Diagnostic Menu of the crt readout.

j. Push up on the TRIGGER COUPLING switch to start the calibration routine.

NOTE

*If either the frequency of the signal generator or the frequency of the oscillator within the C/T/T is not within tolerance, the message **FREQ OUT OF LIMITS** will appear in the crt readout.*

*If the calibration routine is unable to calculate a delay offset calibration constant that is within tolerance, the message **OFFSET LIMIT** will appear in the crt readout.*

k. After about 10 seconds, the **DIAGNSTIC. PUSH A/B TRIG TO EXIT** message should appear in the Diagnostic Menu of the crt readout.

l. Push the A/B/MENU switch to exit the Diagnostic Menu.

m. Disconnect the test equipment from the instrument.

n. Return the CAL/NO CAL jumper to its NO CAL position and reinstall the instrument cabinet.

MAINTENANCE

This section contains information for troubleshooting the 2445 and 2465 Options 06 and 09, Counter/Timer/Trigger (C/T/T) and Word Recognizer (WR) options. Maintenance information contained in the standard instrument Service Manual still applies to maintenance of these options. To function properly, the option requires a working standard oscilloscope and Buffer board.

TROUBLESHOOTING

Preventive maintenance performed on a regular basis should reveal most potential problems before an instrument malfunctions. However, should troubleshooting be required, the following information is provided to facilitate location of a fault. In addition, the material presented in the "Theory of Operation" and "Diagrams" sections of this manual and the "Troubleshooting" section of the standard instrument's service manual may be helpful while troubleshooting.

GENERAL TROUBLESHOOTING PROCEDURE

The information presented here is intended to complement the information contained in the "Troubleshooting Procedures" part of the "Diagrams" section of the manual. Become familiar with the rest of the information in this section before proceeding with instrument troubleshooting. If the instrument will run the diagnostic routines as described in the "Diagnostic Routines" part of this section, perform the routines to help localize the instrument problems.

First make sure that the standard instrument functions properly. The option assembly will have to be removed to verify this. Then make sure that the Buffer board functions properly. To do this, the board will have to be connected to the standard instrument using the extender cables and all the option boards will have to be removed. Then verify that each option works properly by checking the operation of each option one at a time. Consult each option's service manual for operating and troubleshooting information and extender cable use. After all the options are working correctly, reassemble the instrument.

DIAGNOSTIC ROUTINES

Control of Diagnostic routines and their display format is the same as for the standard instrument.

Kernel Tests

The standard instrument's Kernel tests include checks to determine if the Buffer board and any options are present. A ROM checksum test is performed on the Buffer board and each option ROM contained in the instrument.

A failure of a Kernel test is considered "fatal" to the operation of the microprocessor system. Kernel test failures will result in an attempt to flash the front-panel TRIG'D indicator and illuminate certain other front-panel indicators with an error code. The code points to the failure area as indicated in Table 5-1. Tables 5-2 and 5-3 are used to determine the option and device numbers used in Table 5-1.

Even if a failure is reported, the A/B/MENU switch may be pushed (or the GPIB command NORM may be used) to try to resume normal instrument operation. However, because of the failure, operation of particular instrument functions is unpredictable.

Confidence Tests

Option 06 and 09 related Confidence tests, Exerciser routines, and their associated error codes are listed in Table 5-4. The error codes listed are in hexadecimal. For

each test number, any combination (through binary addition) of one or more of the listed error codes is possible. Option-related Confidence tests are performed automatically at power up if the Kernel tests are completed successfully. These tests may also be initiated by the operator from the Diagnostics Monitor by:

1. Pushing the TRIGGER SLOPE switch while holding in both the ΔV and Δt switches to access the Diagnostic Menu.

2. Select the desired test number by repeatedly pushing the TRIGGER MODE switch up, until the test number appears in the Diagnostic Menu of the crt readout.

3. Start the test procedure by pushing up on the TRIGGER COUPLING switch.

4. If a failure is reported in the Diagnostic Menu, refer the instrument to a qualified service technician.

5. When the procedure ends, exit the Diagnostic Menu by pushing the A/B/MENU select switch.

Table 5-1

Kernel Test Failure Codes

Failure Codes		Failing Device
Option	**Device**	
0	0	Control Board RAM U2496
0	1	Control Board ROM U2178
0	2	Control Board ROM U2378
0	3	Control Board ROM U2362
0	4	Control Board ROM U2162
1	1	GPIB Option ROM U4715
1	2	GPIB Option ROM U4710
1	4	GPIB Option RAM U4811
6	1	TV Option ROM U5565
7	1	DMM Option ROM U5280[a]
7	2	DMM Option ROM U5281[a]
8	1	CTT Option ROM U5930
F	1	Buffer Board ROM U4260

[a]When only one ROM is used, either device code indicates ROM U5281 is the failing device.

EAROM TEST (BU TEST 01). Checks EAROM to verify its contents and the interface circuitry.

Read/Write Test—The contents of one location are read, modified, and then reread to verify functioning of the device interface.

Test checks: EAROM input and output lines, EAROM mode control, EAROM reading and writing, and EAROM clock.

Checksum Test—The contents of locations containing calibration constants and power-down settings are checksummed using a spiral-add technique. The result is compared to the contents of location 0.

Test checks: EAROM addressing and EAROM contents.

Table 5-2

Front-Panel LED Option Codes

Option Code				Option	Option
CH 1 TRIGGER SOURCE LED (bit 3)	**CH 2 TRIGGER SOURCE LED (bit 2)**	**CH 3 TRIGGER SOURCE LED (bit 1)**	**CH 4 TRIGGER SOURCE LED (bit 0)**	**Number (in hex)**	**Name**
OFF	OFF	OFF	OFF	0	Standard Instrument
OFF	OFF	OFF	ON	1	GPIB (Option 10)
OFF	ON	ON	OFF	6	TV (Option 05)
OFF	ON	ON	ON	7	DMM (Option 01)
ON	OFF	OFF	OFF	8	C/T/T (Option 06)
ON	OFF	OFF	OFF	8	WR (Option 09)
ON	ON	ON	ON	F	Buffer Board

Table 5-3

Front-Panel LED Device Codes

Device Codes			Device Number
Ready LED (bit 2)	+ SLOPE LED (bit 1)	− SLOPE LED (bit 0)	
OFF	OFF	OFF	0
OFF	OFF	ON	1
OFF	ON	OFF	2
OFF	ON	ON	3
ON	OFF	OFF	4
ON	OFF	ON	5
ON	ON	OFF	6
ON	ON	ON	7

CALIBRATION CONSTANT TEST (CT TEST 81). Checks the C/T/T calibration constants to see if they are within set limits.

GATE ARRAY I/O PATH TEST (CT TEST 82). Checks the I/O paths into and out of the Gate Array. The tested circuitry includes Hardware Register 1 and the ECL-to-TTL level shifters and data buffers.

The Gate Array is written to six times; each time one data line is HI and the others are LO. After each write, the data is read back and checked.

Table 5-4

Diagnostic and Exerciser Routines

Routine Type	Test Number	Routine Name	Error Code	Error Code Meaning
Buffer Test	F1	EAROM Test	X8	Bad read after write.
			1X	Bad checksum.
C/T/T and WR Test	81	Calibration constant test.	01	Delay Offset constant out of limit. Recalibrate the C/T/T.
			02	Clock Frequency constant out of limit. Recalibrate the C/T/T.
	82	Gate Array (U6180) I/O path test.	01	Gate Array bit 0 Read/Write error. Check U6180, R6162, U6290C, U6250, and U5950.
			02	Gate Array bit 1 Read/Write error. Check U5952, U6180, U6290A, U6250, U5950, and R6160.
			04	Gate Array bit 2 Read/Write error. Check U5952, U6180, U6290B, U6250, U5950, and R6176.
			08	Gate Array bit 3 Read/Write error. Check U5952, U6180, U6290C, U6250, U5950, and R6260.
			10	Gate Array bit 4 Read/Write error. Check U5952, U6180, U6290A, U6250, U5950, and R6261.
			20	Gate Array bit 5 Read/Write error. Check U5952, U6180, U6290B, U6250, U5950, and R6161.

Table 5-4 (cont)

Routine Type	Test Number	Routine Name	Error Code	Error Code Meaning
	83	Complex Counter (U6140) I/O path test.	08	Complex counter bit 0 Read/Write error. Check U6140, U5950, and for U5930 pin 22 stuck LO.
			09	Complex counter bit 1 Read/Write error. Check U6140, U5950, and for U5930 pin 22 stuck LO.
			0B	Complex counter bit 2 Read/Write error. Check U6140, U5950, and for U5930 pin 22 stuck LO.
			0C	Complex counter bit 3 Read/Write error. Check U6140, U5950, and for U5930 pin 22 stuck LO.
			0D	Complex counter bit 4 Read/Write error. Check U6140, U5950, and for U5930 pin 22 stuck LO.
			0E	Complex counter bit 5 Read/Write error. Check U6140, U5950, and for U5930 pin 22 stuck LO.
			0F	Complex counter bit 6 Read/Write error. Check U6140, U5950, and for U5930 pin 22 stuck LO.
			10	CLK A path error. Check U6140, U6180, Q6290, Q6291, and U5950.
			20	GATE A path error. Check U6140, U6180, Q6273, Q6271, and U5950.

Table 5-4 (cont)

Routine Type	Test Number	Routine Name	Error Code	Error Code Meaning
	84	Gate Array (U6180) trigger path tests.	0C	Boolean OR trigger failed to generate a sweep on the rising edge of $\overline{ATS}$. Check U6180, Q5981, Q5982, Q5983, Q6090, Q6092, Q6091, U5952, and U6070.
			0D	Boolean OR trigger generated multiple sweeps on rising edge of $\overline{ATS}$. Check U6180, U6070, HO, and $\overline{MT}$.
			0E	Boolean OR trigger generated sweep on falling edge of $\overline{ATS}$. Check R5981 and look for glitch on $\overline{ATS}$.
			10	Boolean OR trigger failed to generate a sweep on rising edge of $\overline{BTS}$. Check $\overline{BTS}$ into U6180.
			14	Boolean AND trigger failed. There were no sweeps but one was expected. Check U6180, and HO into U6180.
			15	Boolean AND trigger generated multiple sweeps. Check HO into U6180.
			16	Sweep occurred on rising edge of $\overline{EXT}$ when driven from $\overline{ATS}$. Check for a glitch on $\overline{EXT}$ into U6180.
			17	Multiple sweeps occurred on rising edge of $\overline{EXT}$ when driven from $\overline{ATS}$. Check HO into U6180 and look for a glitch on $\overline{EXT}$ into U6180.
			18	Expected sweep did not occur on $\overline{EXT}$ when driven from $\overline{ATS}$. Check both HO and $\overline{EXT}$ into U6180.
			19	Multiple sweeps occurred, only one was expected, when $\overline{EXT}$ was driven from $\overline{ATS}$. Check HO into U6180.
			40	Either the $\overline{ATS}$ to $\overline{TSA}$ or the $\overline{BTS}$ to $\overline{TSB}$ signal path is bad. Check the trigger status from and to the Main board, Q5981, Q5980, U5990A, Q5983, Q6093, U5990D, and U5952.

Table 5-4 (cont)

Routine Type	Test Number	Routine Name	Error Code	Error Code Meaning
	85	Counters, Phase Locked Loop, and Oscillator test.	01	Top byte of 131 MHz counter too low. Check U6180 pin 40.
			02	Top byte of 2.65 MHz counter too low. Check Q5920, Q5921, U6140 pin 4, and U6140.
			04	Phase Locked Loop not locked. Check Phase Locked Loop.
			08	Wrong oscillator frequency. Check Y5910 and associated circuitry.
	86	Delay-by-Events circuitry test.	01	In Trigger After Delay mode with the delay time set shorter than the delay, a sweep was produced. Check $\overline{\text{B AUX TRIG}}$ and HO at U6180.
			02	In Trigger After Delay mode with the delay time set longer than the delay, there was no sweep. Check $\overline{\text{B AUX TRG}}$ and HO at U6180 and output O1 at U6140.
			04	BHO path into Gate Array stuck low.
			08	Forced HO (U6140 pin 40) doesn't work. Check U6140 pin 40 and associated circuitry.
			10	Complex counter (U6140) reset sequence fails.
			20	AHO turn off too slow. Check R5962.

Table 5-4 (cont)

Routine Type	Test Number	Routine Name	Error Code	Error Code Meaning
	87	Delta Time measurement test.	01	$\overline{BSG}$ to Gate Array bad.
			02	$\overline{DS}$ to Gate Array bad.
			04	Delay difference is bad. Check the stability of the 131.0669 MHz clock.
			08	Counter C contains a bad count.
			10	Counter B contains a bad count. Check CLKB path between U6180 and U6140.
			18	Counter A contains a bad count. Failure should be caught by earlier tests.
			20	Clock C or $\overline{ASG}$ path bad.
			40	Clock B path bad.
Buffer Exerciser	F1	Option Identification.	None	
	F2	Page Selection.	None	
Exerciser	02	EAROM Examine.	None	
Word Recognizer Exerciser	81	Word Recognizer Probe Exerciser	None	

COMPLEX COUNTER I/O PATH TEST (CT TEST 83). Checks the I/O paths to and from the Complex Counter. The test involves circuitry in the Gate Array, Complex Counter, and the CLK A-to-S1 and GATE A-to-G1 signal paths between the Gate Array and Complex Counter. The only IC not involved in earlier tests is U6140.

Each data bit, starting with D0, is set HI and written to U6140. This data is read back in order while recording errors. The CLK A-to-S1 and the GATE A-to-G1 interfaces between U6180 and U6140 are then checked. Counters 1 and 2 of U6140 count CLK A and GATE A respectively. The Gate Array is initialized to cycle both GATE A and CLK A. Counters 1 and 2 of U6140 are then checked to see if they received the count.

GATE ARRAY TRIGGER PATH TEST (CT TEST 84). Checks the following signal paths: $\overline{TSA}$ to and from the Buffer board, $\overline{TSB}$ to and from the Buffer board, the three AHO paths to the Gate Array, the $\overline{EXT}$ inputs, and the $\overline{A\ AUX\ TRG}$ output. This test also checks to see if the AHO paths clear the A AUX TRG output between sweeps. Circuitry not involved in earlier tests includes U6070 and the circuitry in the $\overline{TSA}$ and $\overline{TSB}$ to U6180 signal paths.

This test is performed with the triggers set to fast compare. The trigger status inputs are manipulated by changing the A and B trigger levels. Both the A and B trigger status pass-through paths are checked in both the HI and LO states. With the trigger status inputs in ECL mode (status inputs to U6180), the $\overline{ATS}$ and $\overline{BTS}$ inputs, the $\overline{EXT}$ input, and the $\overline{A\ AUX\ TRG}$ output are checked with the C/T/T in LOGIC AND, LOGIC OR, and simulated external trigger modes. Then each AHO path is checked to see if it clears $\overline{A\ AUX\ TRG}$ between sweeps.

COUNTER, PHASE LOCKED LOOP, AND OSCILLATOR TEST (CT TEST 85). Checks the time base by comparing the count in two of the counters after about 20 ms. One counter is counting the 131 MHz Phase Locked Loop clock; the other counter counts the 2.62 MHz clock. The count in the 131 MHz counter should contain 50 times the count contained in the 2.62 MHz counter. The count in the 2.62 MHz counter must be within 1000 parts per million of the correct value, referenced to the 6802 clock.

DELAY-BY-EVENTS CIRCUITRY TEST (CT TEST 86). Checks the Delay-by-Events circuitry, BHO input, $\overline{\text{B AUX TRG}}$ output, the HO output of the complex counter, and the $\overline{\text{TC}}$ input to the Gate Array.

This test uses the B Sweep Delayed-by-Time mode, where the A Trigger is the starting event and 131 MHz clocks are the delaying event. The oscilloscope is run in the B Sweep Triggerable-After-Delay mode with the B Delay set at half sweep. The delay-by-events time is set shorter than the B Delay; a Delay Sweep should not occur. The time is then set longer than the B Delay; a Delayed Sweep should occur. Checks are also made to see that Delay-by-Events mode resets and that $\overline{\text{B AUX TRG}}$ clears between sweeps. During one sweep, auto holdoff is exerted; a Delay Sweep should not occur. In a Delay-by-Events test, holdoff turn-off time is checked.

DELTA TIME MEASUREMENT TEST (CT TEST 87). Makes a one-sample (two-sweep) Delta Time measurement. Checks $\overline{\text{ASG}}$, $\overline{\text{BSG}}$, $\overline{\text{DS}}$, and the three counters in the Gate Array and Complex Counter.

The sweeps are triggered by grounding the A Trigger input and then changing the A Trigger level. Each time the 3.3 ms interrupt occurs, the levels are changed. The reference delay is set to 800 ns (~ 105 clocks) and the delta delay is set to 400 ns (~ 52 clocks). When the sample is taken, the difference between the two counters must be within two counts of 52.

Exerciser Routines

Operation of Exerciser routines is the same as for the standard instrument. The Exerciser routines allow the operator to set and examine various bytes of control data used in determining option function.

OPTION IDENTIFICATION (BU EXER F1). This routine displays across the top line of the crt readout, the option designator for all installed options. Option designators are listed in Table 5-5.

Table 5-5

Option Designators

Option	Option Designator
Buffer Board	BU
GPIB	GP
TV	TV
DMM	DM
Counter/Timer/Trigger	CT
Counter/Timer/Trigger and WR	CT

PAGE SELECTION (BU EXER F2). This routine continuously selects and deselects each of the option page registers.

EAROM EXAMINE (EXER 02). This is the standard instrument EAROM Examine routine. Locations 64 (hex) to C7 (hex) access the Buffer Board EAROM.

WORD RECOGNIZER EXERCISER (CT EXER 81). This routine continuously exercises the Word Recognizer Data line by repeatedly sending a HI followed by 39 LOs over the WDATA signal line, to the Word Recognizer probe.

EXTENDER CABLE USE

Extender Cable Kit

An extender cable kit, which can be ordered from Tektronix, Inc., is needed when troubleshooting an instrument containing options. The kit is used when troubleshooting the standard instrument by itself or when connecting a removed option assembly to the standard instrument for troubleshooting purposes.

Table 5-6 lists all cables contained in the kit (Tektronix Part Number 020-1075-00). In addition to the cables, the kit contains 12 zero-ohm jumpers (Tektronix Part Number 131-0993-00). The procedures that follow reference the cables by numbers as shown in column one. See Figure 5-1 for a pictorial representation of each cable to aid in cable identification.

Table 5-6

Extender Cables

Cable Number	Tektronix Part Number	Option Usage
1	175-7183-00	All
2	175-7184-00	All
3	175-9178-00	All
4	175-9181-00	All
5	175-7215-00	GPIB
6	175-9179-00	GPIB
7	175-9182-00	GPIB
8	175-9175-00	TV
9	175-9180-00	TV
10	175-9183-00	TV
11	175-9174-00	TV, C/T/T
12	175-7932-00	WR
13	175-9176-00	C/T/T
14	175-9177-00	C/T/T

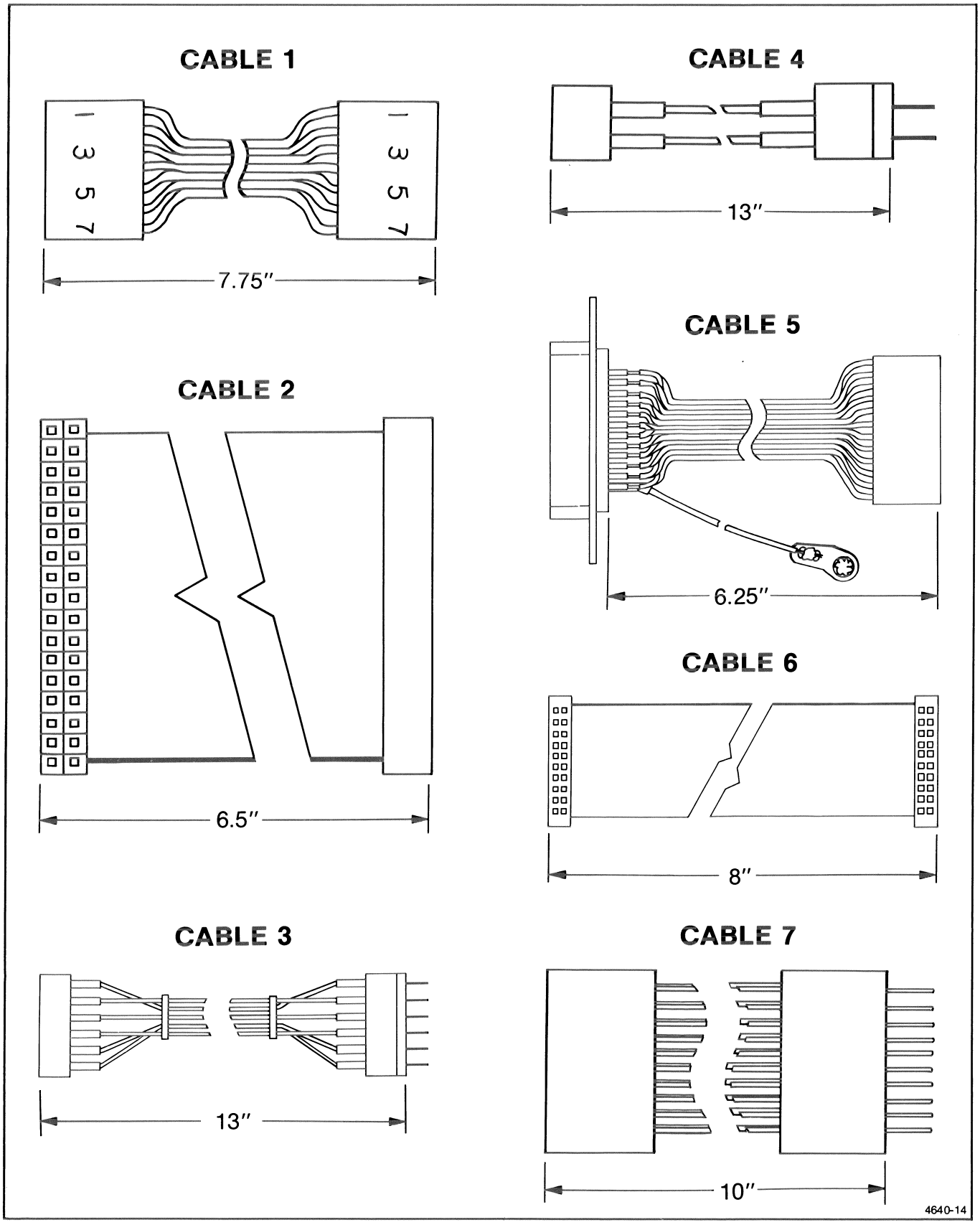


Figure 5-1. Option extender cables.

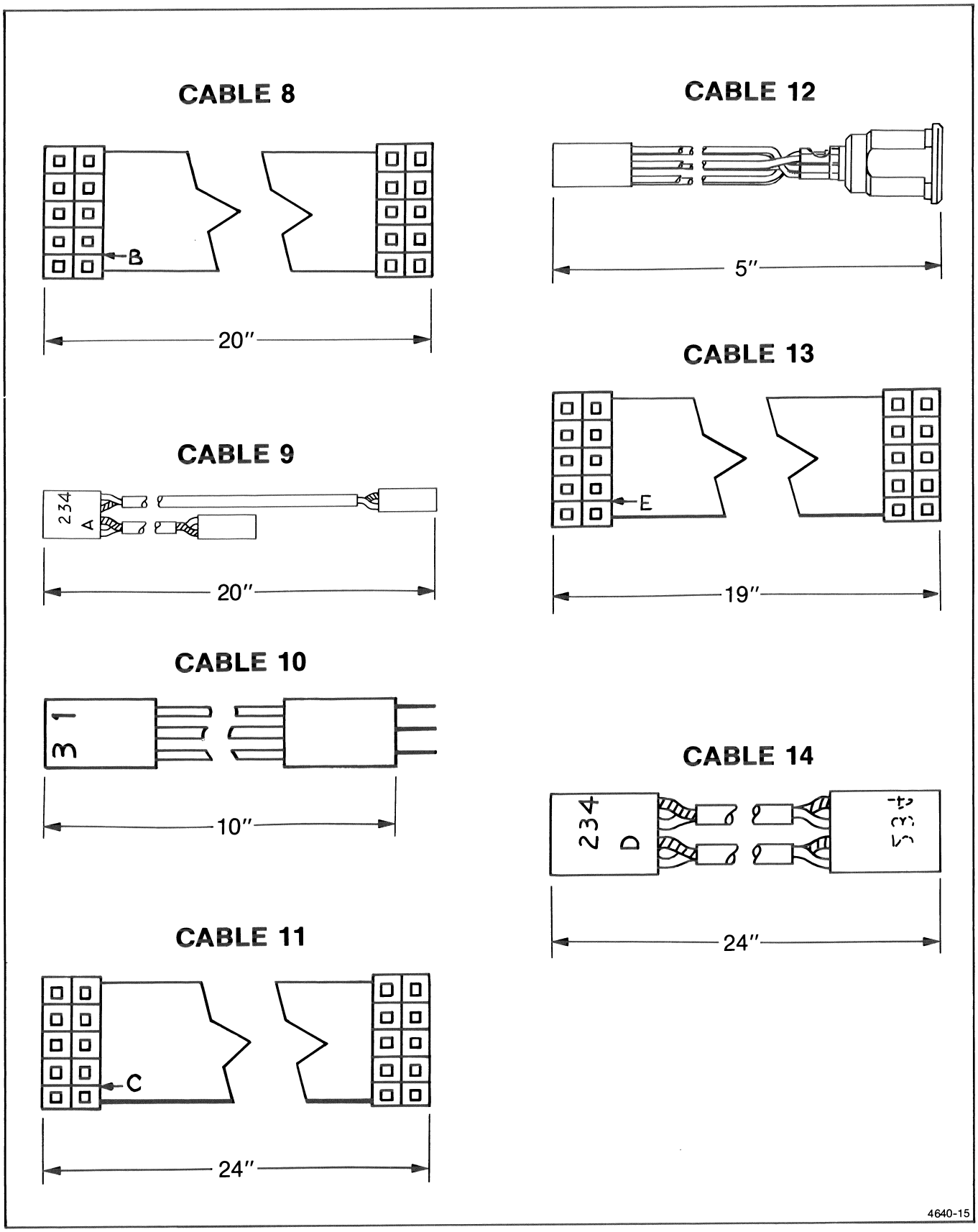


Figure 5-1 (cont). Option extender cables.

Instrument Troubleshooting Without Options

When it is desired to troubleshoot the standard instrument with the option assembly removed, perform the following steps to complete the signal paths required for operation of the standard instrument circuitry. Note that all the steps will not necessarily be performed, depending on which options were included in the instrument.

NOTE

In the following steps, P100, P101, and P102 are all located on the Main board in the standard instrument.

1. If the instrument contained the GPIB Option, use Cable 7 to connect front-panel cable connector P4256 and Control-board connector P651.

2. If the instrument contained the TV Option, connect pins 1 and 2 of P100 and pins 9 and 10 of P100, using the extender cable kit jumpers.

3. If the instrument contained the TV or C/T/T Options, connect pins 3 and 4 of P102 and pins 7 and 8 of P102, using the extender cable kit jumpers.

4. If the instrument contained the C/T/T Option, connect pins 1 and 3 of P101 and pins 6 and 8 of P101, using the extender cable kit jumpers.

Instrument Troubleshooting With Options

To operate the instrument and its options with the option assembly removed for troubleshooting, the assembly is placed upside down and to the right of the standard instrument (see Figure 5-2). The arrows represent the extender cables that are connecting the option assembly and the standard instrument.

Connecting all the extender cables is not required for each option. Column three in Table 5-6 lists which extender cables are used to connect and operate a particular option whose operation is in question. Cable number and Buffer board-standard instrument interconnection information for the C/T/T and WR options are shown in Figure 5-3. The "Troubleshooting Procedures" in the "Diagrams" section of this manual contain information about cable usage during the troubleshooting session.

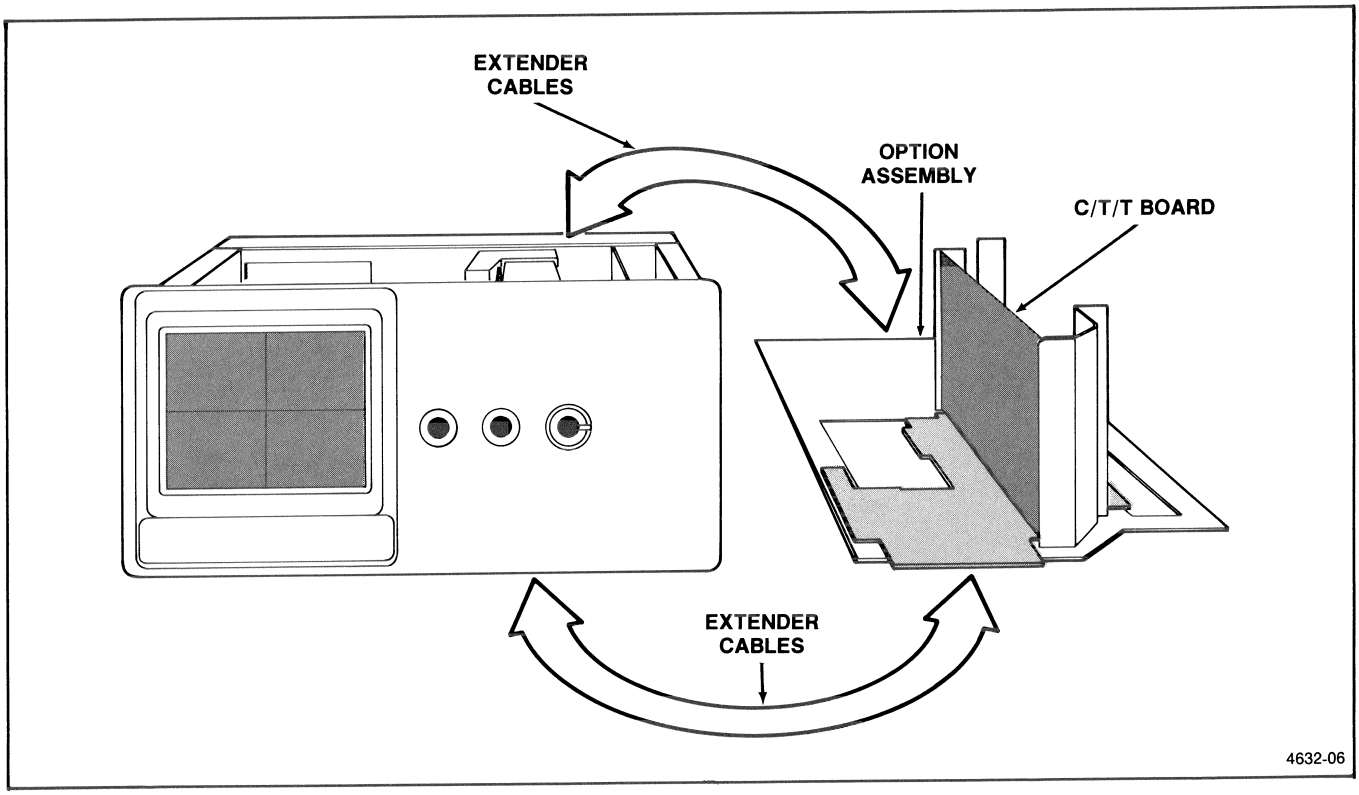


Figure 5-2. Orientation of assemblies when using extender cables.

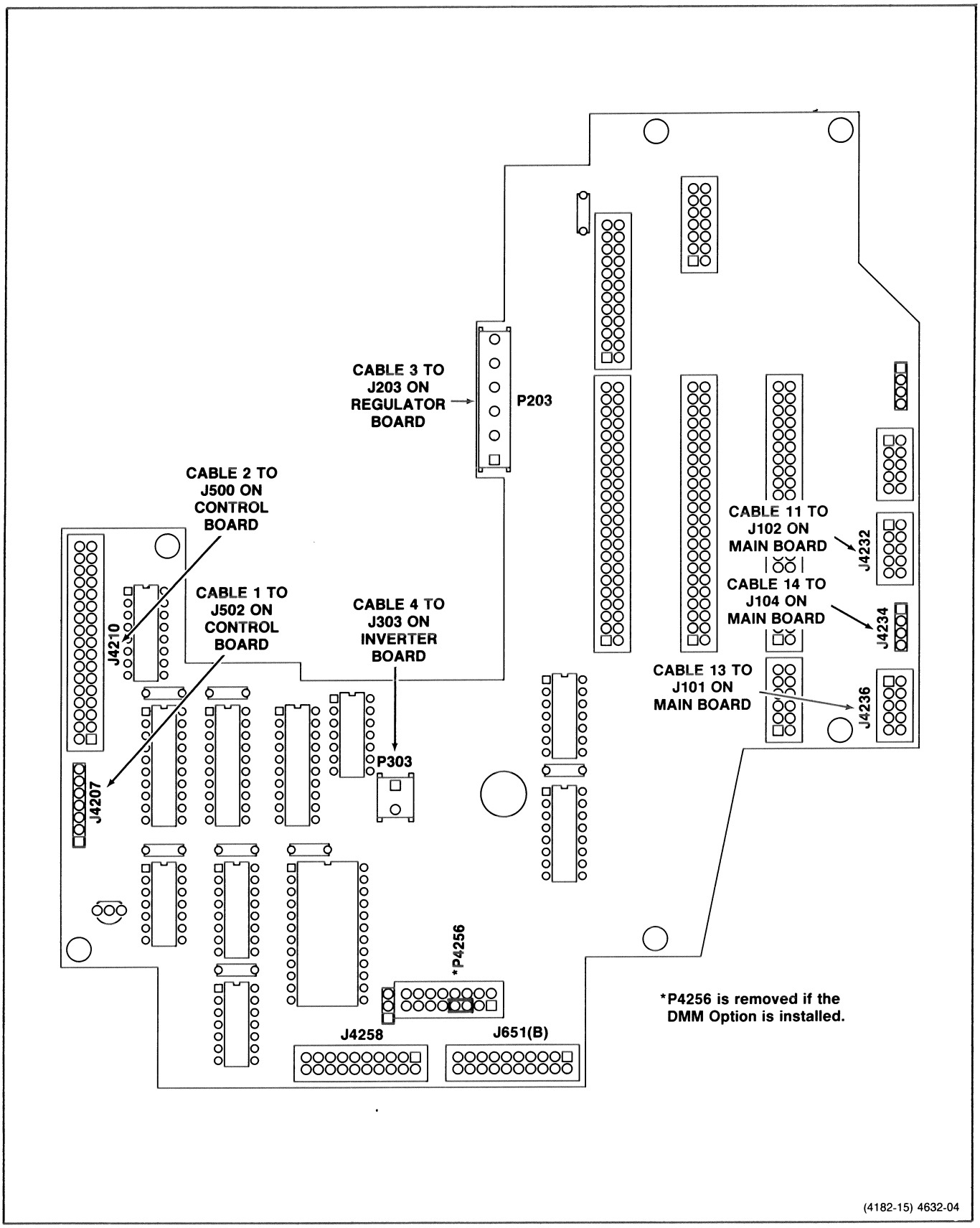


Figure 5-3. Extender cable connection points for troubleshooting.

CORRECTIVE MAINTENANCE

Corrective maintenance for these options is the same as for the standard instrument unless stated otherwise in this section.

REMOVAL AND REPLACEMENT INSTRUCTIONS

The C/T/T and WR Option board and the Buffer board may be removed for repair or replacement using the following procedures. Before beginning any procedure, read the information at the beginning of the "Removal and Replacement Instructions" section in the standard instrument manual. If additional options are installed in the instrument, consult that particular option's service manual for removal and replacement information that may impact the following procedures.

C/T/T and WR Board Removal

Removal of the C/T/T and WR board for repair or replacement is accomplished by:

1. Perform the "Cabinet Removal" procedure as outlined in the manual.

2. Perform the first six steps of the "Top-Cover Plate Removal" procedure as outlined in the "Removal and Replacement Instructions" in the standard instrument service manual.

3. Remove the two top securing screws located at the right-center portion of the top-cover plate.

4. Disconnect the cables at the left edge of the Buffer board (P101, P102, and P104).

5. Lift the top-cover plate above the instrument approximately 2 inches.

6. Disconnect two cables at the right-front edge of the Buffer board (P4207 and P4210).

7. Disconnect the Word Recognizer cable (P5990) and the WORD RECOG OUT cable (P5991) from the C/T/T and WR board.

8. Lift and rotate the option assembly about the front panel until the assembly is almost upside down.

9. Disconnect two cables at the front edge of the Buffer board (P4258 and P651).

10. Remove the C/T/T and WR board from the option assembly by lifting it straight out from the Buffer board. Note the option assembly slot that the C/T/T and WR board is removed from for installation reference.

CAUTION

When securing the option assembly back into the main instrument, be sure that the connector cables are indexed correctly. Also check that the cables are not crimped and that P203 and P303 are seated correctly in their connectors. The two circuit board retainers located along the right edge of the top-cover plate should securely engage the Readout board.

To reinstall the C/T/T and WR board and option assembly into the standard instrument, perform the reverse of the preceding steps.

Buffer Board Removal

Removal of the Buffer board for repair or replacement is accomplished by:

1. Perform the preceding "C/T/T and WR Board Removal" procedure.

2. Remove the five securing screws that attach the Buffer board to the Vertical Board support.

3. Remove the Buffer board from the top-plate cover and option assembly.

To reinstall the Buffer board and option assembly into the standard instrument, perform the reverse of the preceding steps.

Word Recognizer Probe Disassembly

Disassembly of the Word Recognizer Probe for repair or replacement is accomplished by:

1. If the cable from the Word Recognizer probe is connected to the instrument, disconnect it from the oscilloscope rear panel.

2. If the 10-wide combs are connected to the probe, disconnect them from the probe by pulling them straight out of the probe body.

3. Remove the four screws securing the probe covers.

4. Remove the probe covers.

5. Remove the two Word Recognizer boards by holding the board that contains J6300 and pulling the other board straight to the front toward J6300.

6. Remove P6370 by pulling it straight back between J6380 and J6385.

To reassemble the Word Recognizer probe, perform the reverse of the preceding steps, making certain that the probe cover with D8 to D15 markings covers the board containing J6300.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

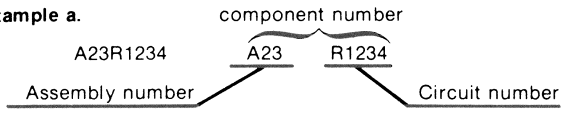
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

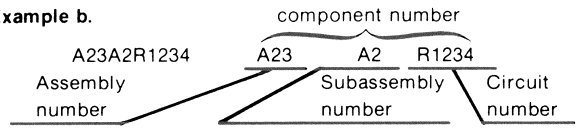
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
0000M	SONY/TEKTRONIX CORPORATION	P O BOX 14, HANEDA AIRPORT	TOKYO 149, JAPAN
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
01536	CAMCAR DIV OF TEXTRON INC. SEMS PRODUCTS UNIT	1818 CHRISTINA ST.	ROCKFORD, IL 61108
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
06383	PANDUIT CORPORATION	17301 RIDGELAND	TINLEY PARK, IL 60477
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
27264	MOLEX, INC.	2222 WELLINGTON COURT	LISLE, IL 60532
33096	COLORADO CRYSTAL CORPORATION	2303 W 8TH STREET	LOVELAND, CO 80537
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
76493	BELL INDUSTRIES, INC., MILLER, J. W., DIV.	19070 REYES AVE., P O BOX 5825	COMPTON, CA 90224
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
91836	KINGS ELECTRONICS CO., INC.	40 MARBLEDALE ROAD	TUCKAHOE, NY 10707
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341
T1319	MORELLIS Q & D PLASTICS	1812 16TH AVE	FOREST GROVE OR 97116
T1557	TEKA PRODUCTS, INC.	45 SALEM ST.	PROVIDENCE, RI 02907

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				ASSEMBLIES		
A1	670-7276-XX			CKT BOARD ASSY:MAIN	80009	670-7276-01
	----- -----			(2465 OPT.06,09-SEE MANUAL 070-3831-00)		
A1	670-7285-XX			CKT BOARD ASSY:MAIN	80009	670-7285-01
	----- -----			(2445 OPT.06,09-SEE MANUAL 070-3829-00)		
A20	670-7830-01			CKT BOARD ASSY:BUFFER	80009	670-7830-01
A20	----- -----			(2445/2465 OPT.06 AND/OR OPT. 09 ONLY)		
A20	670-7830-04			CKT BOARD ASSY:BUFFER	80009	670-7830-04
A20	----- -----			(2445/2465 COMBO OF OPT.05 & OPT. 06		
A20	----- -----			AND/OR OPT.09)		
A27	670-7997-01			CKT BOARD ASSY:COUNTER/TIME/TRIGGER	80009	670-7997-01
	----- -----			(2445/2465 OPTION 06 ONLY)		
A32	670-7999-00			CKT BOARD ASSY:WORD RECOGNIZER PROBE #1	80009	670-7999-00
	----- -----			(2445/2465 OPTION 09 ONLY)		
A33	670-7998-01			CKT BOARD ASSY:WORD RECOGNIZER PROBE #2	80009	670-7998-01
	----- -----			(2445/2465 OPTION 09 ONLY)		
A20	670-7830-01			CKT BOARD ASSY:BUFFER	80009	670-7830-01
A20	----- -----			(2445/2465 OPT.06 AND/OR OPT. 09 ONLY)		
A20	670-7830-04			CKT BOARD ASSY:BUFFER	80009	670-7830-04
A20	----- -----			(2445/2465 COMBO OF OPT.05 & OPT. 06		
A20	----- -----			AND/OR OPT.09)		
A20C4215	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4215	----- -----			OPT.06 AND/OR OPT.09 ONLY)		
A20C4215	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	80009	281-0909-00
A20C4215	----- -----			(OPT.05,OPT.06 AND/OR OPT.09 COMBO)		
A20C4224	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4224	----- -----			(OPT.06 AND/OR OPT.09 ONLY)		
A20C4224	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	80009	281-0909-00
A20C4224	----- -----			(OPT.05,OPT.06 AND/OR OPT.09 COMBO)		
A20C4240	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4240	----- -----			(OPT.06 AND/OR OPT.09 ONLY)		
A20C4240	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	80009	281-0909-00
A20C4240	----- -----			(OPT.05,OPT.06 AND/OR OPT.09 COMBO)		
A20C4241	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4241	----- -----			(OPT.06 AND/OR OPT.09 ONLY)		
A20C4241	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	80009	281-0909-00
A20C4241	----- -----			(OPT.05,OPT.06 AND/OR OPT.09 COMBO)		
A20C4255	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4255	----- -----			(OPT.06 AND/OR OPT.09 ONLY)		
A20C4255	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	80009	281-0909-00
A20C4255	----- -----			(OPT.05,OPT.06 AND/OR OPT.09 COMBO)		
A20C4260	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4260	----- -----			(OPT.06 AND/OR OPT.09 ONLY)		
A20C4260	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	80009	281-0909-00
A20C4260	----- -----			(OPT.05,OPT.06 AND/OR OPT.09 COMBO)		
A20C4265	283-0764-00			CAP.,FXD,MICA D:22PF,+1-0.5PF,500V	0000M	283-0764-00
A20C4270	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4270	----- -----			(OPT.06 AND/OR OPT.09 ONLY)		
A20C4270	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	80009	281-0909-00
A20C4270	----- -----			(OPT.05,OPT.06 AND/OR OPT.09 COMBO)		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20C4280	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4280	----- -----			(OPT.06 AND/OR OPT.09 ONLY)		
A20C4280	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	80009	281-0909-00
A20C4280	----- -----			(OPT.05,OPT.06 AND/OR OPT.09 COMBO)		
A20J651	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A20J651	----- -----			(QUANTITY OF 20)		
A20J4203	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A20J4203	----- -----			(QUANTITY OF 3)		
A20J4207	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A20J4207	----- -----			(QUANTITY OF 7)		
A20J4210	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A20J4210	----- -----			(QUANTITY OF 34)		
A20J4220	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
A20J4220	----- -----			(QUANTITY OF 14)		
A20J4221	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
A20J4221	----- -----			(QUANTITY OF 24)		
A20J4228	131-2919-00			CONN,RCPT,ELEC:HEADER,1 X 4,0.1 SPACING	00779	87232-4
A20J4230	131-2920-00			CONN,RCPT,ELEC:HEADER,2 X 5,0.1 SPACING	00779	86479-3
A20J4232	131-2920-00			CONN,RCPT,ELEC:HEADER,2 X 5,0.1 SPACING	00779	86479-3
A20J4234	131-2919-00			CONN,RCPT,ELEC:HEADER,1 X 4,0.1 SPACING	00779	87232-4
A20J4236	131-2920-00			CONN,RCPT,ELEC:HEADER,2 X 5,0.1 SPACING	00779	86479-3
A20J4238	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
A20J4238	----- -----			(QUANTITY OF 12)		
A20J4240A	131-1742-00			TERMINAL,PIN:0.662 L X 0.025 SQ PH BRS	22526	48283-086
A20J4240A	----- -----			(QUANTITY OF 40)		
A20J4240B	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
A20J4240B	----- -----			(QUANTITY OF 4)		
A20J4242	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
A20J4242	----- -----			(QUANTITY OF 44)		
A20J4243	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
A20J4243	----- -----			(QUANTITY OF 44)		
A20J4256	131-1742-00			TERMINAL,PIN:0.662 L X 0.025 SQ PH BRS	22526	48283-086
A20J4256	----- -----			(QUANTITY OF 2)		
A20J4258	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A20J4258	----- -----			(QUANTITY OF 20)		
A20J4330	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A20J4330	----- -----			(QUANTITY OF 14)		
A20J4330	131-1742-00			TERMINAL,PIN:0.662 L X 0.025 SQ PH BRS	22526	48283-086
A20J4330	----- -----			(QUANTITY OF 2)		
A20P203	131-2924-00			CONN,RCPT,ELEC:HEADER,1 X 6,0.2 SPACING	27264	10-51-1061
A20P303	131-2923-00			CONN,RCPT,ELEC:HEADER,1 X 2,0.2 SPACING	27264	10-51-1021
A20Q4201	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A20R4200	321-0085-00			RES.,FXD,FILM:75 OHM,1%,0.125W	91637	MFF1816G75R00F
A20R4201	321-0085-00			RES.,FXD,FILM:75 OHM,1%,0.125W	91637	MFF1816G75R00F
A20R4202	321-0122-00			RES.,FXD,FILM:182 OHM,1%,0.125W	91637	MFF1816G182R0F
A20R4203	321-0105-00			RES.,FXD,FILM:121 OHM,1%,0.125W	01121	ORD BY DESCR
A20R4204	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A20R4205	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R4206	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A20R4207	321-0105-00			RES.,FXD,FILM:121 OHM,1%,0.125W	01121	ORD BY DESCR
A20R4208	321-0122-00			RES.,FXD,FILM:182 OHM,1%,0.125W	91637	MFF1816G182R0F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20R4210	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A20R4224	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R4265	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20U4207	156-1566-00			MICROCIRCUIT,DI:EPROM,100 X 14	80009	156-1566-00
A20U4225	156-1318-00			MICROCIRCUIT,DI:4-BIT BISTABLE LATCH SCR	01295	SN74LS375
A20U4235	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A20U4235	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A20U4240	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A20U4245	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A20U4250	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A20U4255	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A20U4260	160-1833-05			MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM	80009	160-1833-05
A20U4265	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A20U4275	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A20U4280	156-0866-02			MICROCIRCUIT,DI:13 INP NAND GATES,SCRN	80009	156-0866-02

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A27	670-7997-01			CKT BOARD ASSY:COUNTER/TIMER/TRIGGER	80009	670-7997-01
A27C5920	281-0757-00			CAP.,FXD,CER DI:10PF,20%,100V	72982	8035-D-COG-100G
A27C5921	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C5922	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A27C5923	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A27C5924	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A27C5940	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C5950	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C5960	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A27C5961	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A27C5980	281-0811-00			CAP.,FXD,CER DI:10PF,10%,100V	96733	R2911
A27C5981	281-0811-00			CAP.,FXD,CER DI:10PF,10%,100V	96733	R2911
A27C5990	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A27C5991	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6020	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6021	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6030	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A27C6040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6080	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A27C6081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6110	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6111	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6112	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A27C6113	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6120	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6130	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6160	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A27C6170	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A27C6192	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6230	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6231	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6260	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6270	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27C6290	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A27CR5960	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A27CR5961	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A27CR5970	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A27CR6020	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A27CR6162	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A27CR6170	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A27CR6190	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A27CR6210	152-0269-00			SEMICOND DEVICE:SILICON,VAR V CAP.,4V,33PF	04713	SMV1263
A27CR6211	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A27J5990	131-3058-00			CONN RCPT,ELEC:HEADER,RTANG,2 X 3,0.1 CTR	00779	1-86479-5
A27J5991	131-2921-00			CONN RCPT,ELEC:HEADER,1 X 2,0.1 SPACING	00779	1-86479-3
A27J6135	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A27J6144	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A27L5990	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A27L6030	108-0245-00			COIL,RF:3.9UH	76493	B6310-1

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A27L6210	108-0606-00			COIL,RF:37NH	80009	108-0606-00
A27P4221	131-2890-00			CONN,RCPT,ELEC:CKT BD,HORIZ,2 X 12,0.1 SP	00779	86063-8
A27P4240	131-2887-00			CONN,RCPT,ELEC:CKT BD,HORIZ,2 X 22,0.100SP	00779	1-86063-8
A27P5990	131-0993-00			BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
A27Q5920	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A27Q5921	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A27Q5961	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A27Q5970	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A27Q5980	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q5981	151-0424-00			TRANSISTOR:SILICON,NPN	04713	SPS8246
A27Q5982	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A27Q5983	151-0424-00			TRANSISTOR:SILICON,NPN	04713	SPS8246
A27Q6090	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A27Q6091	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6092	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6093	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6190	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6191	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6270	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6271	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6272	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6273	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6274	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6290	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6291	151-0188-00			TRANSISTOR:PNP,SI,TO-92	T0058	2N3906
A27Q6292	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A27R6292	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A27R5921	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R5950	315-0113-00			RES.,FXD,CMPSN:11K OHM,5%,0.25W	01121	CB1135
A27R5951	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A27R5952	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A27R5960	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A27R5961	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A27R5962	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R5963	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A27R5964	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A27R5970	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A27R5971	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A27R5972	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A27R5973	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A27R5980	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A27R5981	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A27R5982	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A27R5983	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A27R5984	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A27R5985	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A27R5990	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A27R5991	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A27R5992	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A27R5993	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A27R6020	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235

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A27R6021	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6022	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6042	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A27R5050	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A27R6060	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6062	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A27R6063	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A27R6064	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A27R6081	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A27R6083	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A27R6084	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A27R6085	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A27R6090	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A27R6091	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A27R6092	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A27R6093	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A27R6094	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A27R6121	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6160	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6161	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6162	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6163	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6164	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6165	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A27R6166	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6170	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6172	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6173	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6174	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A27R6175	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6176	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6177	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A27R6178	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A27R6191	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A27R6192	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A27R6193	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A27R6194	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A27R6195	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A27R6197	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A27R6198	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A27R6199	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A27R6222	315-0823-00			RES.,FXD,CMPSN:82K OHM,5%,0.25W	01121	CB8235
A27R6230	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A27R6231	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
A27R6232	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6233	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6245	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A27R6250	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	01121	106A103
A27R6251	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6252	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A27R6260	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6261	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A27R6262	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A27R6263	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A27R6264	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A27R6266	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A27R6267	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A27R6270	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A27R6271	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A27R6273	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A27R6274	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A27R6275	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A27R6276	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A27R6277	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A27R6290	321-0157-00			RES.,FXD,FILM:422 OHM,1%,0.125W	91637	MFF1816G422R0F
A27R6291	321-0066-00			RES.,FXD,FILM:47.5 OHM,1%,0.125W	91637	MFF1816G47R50F
A27R6293	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A27R6294	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A27U5910	156-0656-02			MICROCIRCUIT,DI:DECADE COUNTER,BURN-IN	01295	SN74LS90
A27U5930	160-2298-00			MICROCIRCUIT,DI:32768 X 8 EPROM,PRGM		
A27U5940	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A27U5942	156-0866-02			MICROCIRCUIT,DI:13 INP NAND GATES,SCRN	80009	156-0866-02
A27U5950	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A27U5952	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A27U5990	156-1340-01			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	02735	CD4071BFX
A27U6010	156-0124-02			MICROCIRCUIT,DI:PHASE/FREQ DETECTOR,SCRN	80009	156-0124-02
A27U6070	156-1795-00			MICROCIRCUIT,DI:DUAL 4 TO 1 MUX,SCRN	04713	MC10H174
A27U6120	156-0266-00			MICROCIRCUIT,LI:EMITTER COUPLED OSCILLATOR	04713	MC1648P/L
A27U6130	156-1248-00			MICROCIRCUIT,DI:PRESCALER/DIVIDE BY 100	80009	156-1248-00
A27U6140	156-1550-00			MICROCIRCUIT,DI:SYSTEM TIMING CONTROLLER	34335	AM9513(PCTB OR D
A27U6150	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A27U6152	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A27U6230	156-1134-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	02735	CA3140EX
A27U6250	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	01295	SN74LS367NP3
A27U6252	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A27U6290	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A27W6210	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A27Y5910	158-0269-00			XTAL UNIT,QTZ:13.10669 MHZ	33096	OBD

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A32	670-7999-00			CKT BOARD ASSY:WORD RECOGNIZER PROBE #1	80009	670-7999-00
A32C6303	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A32C6334	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A32C6338	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A32CR6330	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	01295	1N4152R
A32CR6335	152-0664-00			SEMICOND DEVICE:SWITCHING,SI,70V	50434	5082-2800
A32CR6340	152-0664-00			SEMICOND DEVICE:SWITCHING,SI,70V	50434	5082-2800
A32J6300	131-3046-00			TERM SET,PIN:HEADER,1 X 10,0.155 SPACING	22526	OBD
A32J6370A	131-1425-00			TERM SET,PIN:(36) 0.025 SQ RTANG,0.150L	22526	65521-136
A32J6370B	131-1426-00			TERM SET,PIN:(36) 0.025 SQ RTANG,0.25L	22526	65524-136
A32J6380	131-3045-00			CONN,RCPT,ELEC:CKT BD,RTANG,1 X 5,0.1 SP		
A32J6385	136-0547-00			CONNECTOR,RCPT,:6 PIN,FEMALE	00779	1-380949-6
A32L6354	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A32Q6334	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A32R6301	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6302	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6303	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6304	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6305	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6306	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6307	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6308	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6325	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A32R6330	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A32R6336	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A32R6340	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A32R6350	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A32U6310	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A32U6315	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A32U6320	156-0441-00			MICROCIRCUIT,DI:8 BIT IDENTITY COMPARATOR	07263	74F521
A32U6325	156-0572-02			MICROCIRCUIT,DI:8 BIT SERIAL IN/PRL OUT,SE	27014	MM74C164JA+
A32U6330	156-0572-02			MICROCIRCUIT,DI:8 BIT SERIAL IN/PRL OUT,SE	27014	MM74C164JA+
A32U6335	156-1724-00			MICROCIRCUIT,DI:QUAD 2 INPUT OR GATE,SCRN	04713	74F32(ND OR JD)
A32U6350	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A32U6356	156-1743-00			MICROCIRCUIT,DI:QUAD 2 INPUT NOR GATE	07263	74F02(PCQR OR DC

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A33	670-7998-00			CKT BOARD ASSY:WORK RECOGNIZER PROBE #2	80009	670-7998-00
A33C6410	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A33C6440	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A33J6400	131-3046-00			TERM SET,PIN:HEADER,1 X 10,0.155 SPACING	22526	OBD
A33P6380	131-3153-00			TERM SET,PIN:(36)0.025 SQ,RTANG,0.22 L	T1557	082-3643-RS20
A33P6385	131-3153-00			TERM SET,PIN:(36)0.025 SQ,RTANG,0.22 L	T1557	082-3643-RS20
A33R6400	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6401	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6402	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6403	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6404	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6405	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6406	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6407	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6408	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A33R6432	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A33R6443	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A33U6405	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A33U6409	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A33U6415	156-0441-00			MICROCIRCUIT,DI:8 BIT IDENTITY COMPARATOR	07263	74F521
A33U6420	156-0572-02			MICROCIRCUIT,DI:8 BIT SERIAL IN/PRL OUT,SE	27014	MM74C164JA+
A33U6425	156-0572-02			MICROCIRCUIT,DI:8 BIT SERIAL IN/PRL OUT,SE	27014	MM74C164JA+
A33U6430	156-0572-02			MICROCIRCUIT,DI:8 BIT SERIAL IN/PRL OUT,SE	27014	MM74C164JA+
A33U6435	156-1800-00			MICROCIRCUIT,DI:QUAD 2 INPUT EXCLUSIVE OR	07263	74F86(PCQR OR DC

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

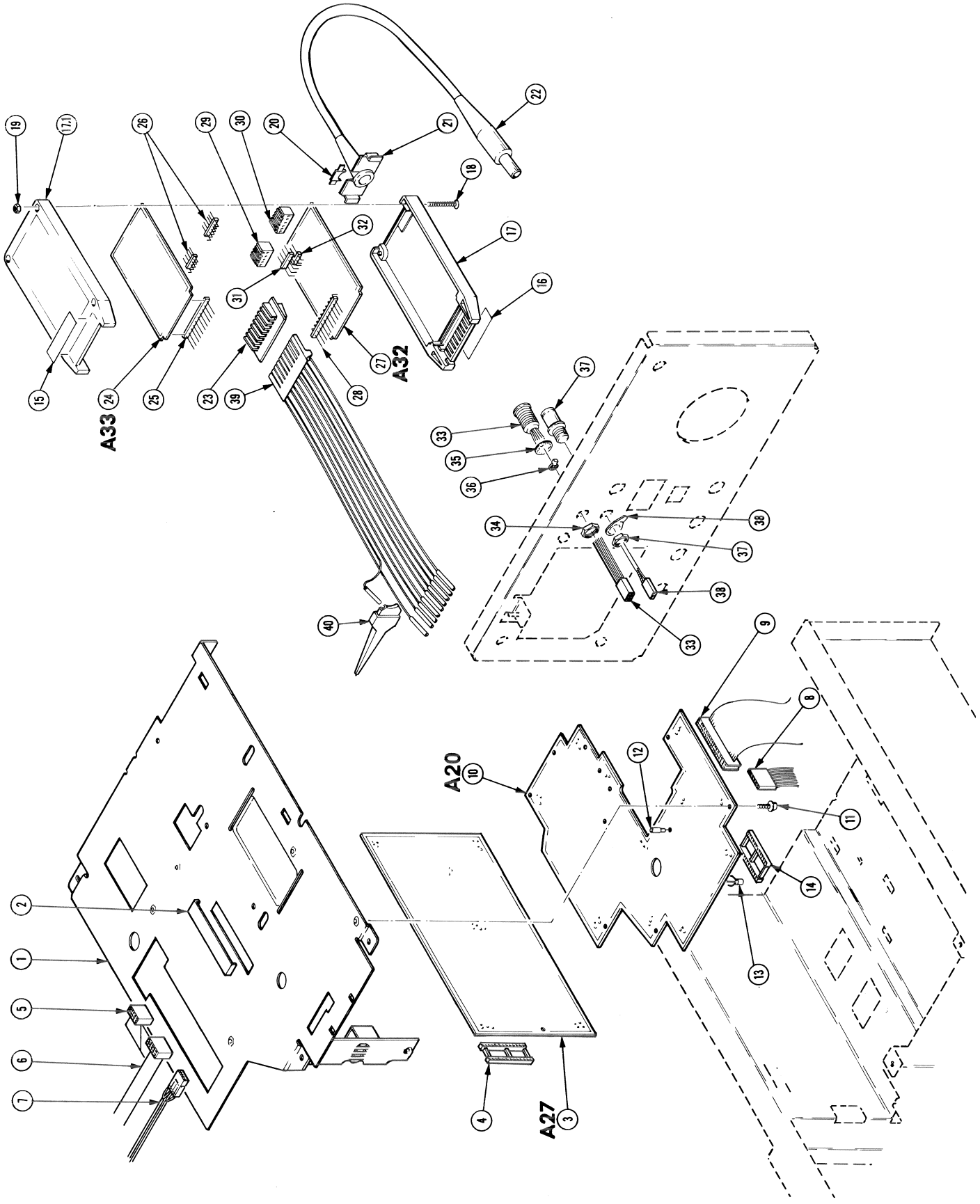
Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-	----- -----			1		COUNTER/TIMER/TRIGGER,OPT.06 2445/2465		
-1	407-1473-00			1		.BRACKET,SUPPORT:CKT BD,ALUMINUM	80009	407-1473-00
-2	200-2871-00			1		.COVER,ELEC CONN:PLASTIC	T1319	ORD BY DESCR
	129-1032-00	B020000	B021649	1		.SPACER,POST:6.75L W/6-32 INT THD		
	----- -----			-		(2445 ONLY)		
	361-1286-00	B021650		1		.SPACER,BRACKET:7.5L,POLYCARBONATE,BLACK		
	----- -----			-		(2445 ONLY)		
	129-1032-00	B020000	B022909	1		.SPACER,POST:6.75L W/6-32 INT THD		
	----- -----			-		(2465 ONLY)		
	361-1286-00	B022910		1		.SPACER,BRACKET:7.5L,POLYCARBONATE,BLACK		
	----- -----			-		.(2465 ONLY)		
-3	----- -----			1		.CKT BOARD ASSY:BOUNTER TIMER TRIGGER		
	----- -----			-		.(SEE A27 REPL)		
-4	136-0755-00			1		..SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-5	175-7927-00			1		.CA ASSY,SP,ELEC:10,28 AWG,11.0 L,RIBBON	22526	81246-002
	----- -----			-		.(BUFFER BOARD TO MAIN BOARD AT POSITION C		
-6	175-7929-00			1		.CA ASSY,SP,ELEC:4,26 AWG,18.0 L,RIBBON	22526	81064-004
	----- -----			-		.(BUFFER BOARD TO MAIN BOARD AT POSITION D		
-7	175-7928-00			1		.CA ASSY,SP,ELEC:10,28 AWG,18.75 L,RIBBON	80009	175-7928-00
	----- -----			-		.(BUFFER BOARD TO MAIN BOARD AT POSITION E		
-8	175-7183-00			1		.CA ASSY,SP,ELEC:7,22 AWG,7.75 L,RIBBON	80009	175-7183-00
-9	175-7184-00			1		.CA ASSY,SP,ELEC:34,28 AWG,6.5 L,RIBBON	80009	175-7184-00
-10	----- -----			1		.CKT BOARD ASSY:BUFFER(SEE A20 REPL)		
						**********(ATTACHING PARTS)**********		
-11	211-0711-00			5		.SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	----- -----			-		.BUFFER BOARD ASSY INCLUDES:		
-12	361-1252-00			5		..SPACER,CKT BD:0.1 ID X 0.188 OD X 0.185		
-13	136-0751-00			1		..SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-14	131-0993-00			1		..BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
	214-3474-00			1		..HEAT SINK,ELEC:ALUMINUM,ANODIZED & DYE B		
	----- -----			1		WORD RECOGNIZER,OPT.09 2445/2465		
	010-6407-01			1		.PROBE,WORD RECO:P6407,W/ACCESSORIES	80009	010-6407-01
	010-6407-00			1		..PROBE,WORD RECO:P6407	80009	010-6407-00
	334-0001-00			1		...MARKER,IDENT:MKD WORD RECOGONIZER IN/OU		
-15	334-5200-00			1		...MARKER,IDENT:MKD WORD RECOGNIZER PROBE		
-16	334-5201-00			1		...MARKER,IDENT:MKD WORD RECOGNIZER PROBE		
-17	380-0710-00			1		...HOUSING,PROBE:POLYCARB,SLATE GRAY,LOWER	80009	380-0710-00
-17.1	380-0711-00			1		...HOUSING,PROBE:POLYCARB,SLATE GRAY,UPPER	80009	380-0711-00
						******(ATTACHING PARTS FOR EACH HOUSING)**		
-18	211-0318-00			4		...SCREW,MACHINE:4-40 X 0.75,FLH,100 DEG	93907	ORD BY DESCR
-19	210-0408-00			4		...NUT,PLAIN,HEX.:6-32 X 0.312 INCH,BRS	73743	3040-402
						**********(END ATTACHING PARTS)*********		
-20	358-0675-00			1		...STRAIN RLF,CA:UPPER		
-21	358-0347-00			1		...STRAIN RLF,CA:LOWER,PLASTIC		
-22	175-8853-01			1		...CA ASSY,SP,ELEC:6/26 AWG,81.0 L,8-N	80009	175-8853-01
-23	361-0758-01			1		...SPACER,PROBE:ACETAL,SLATE GRAY	80009	361-0758-01
-24	----- -----			1		...CKT BOARD ASSY:WORD RECOGNIZER PROBE #2		
	----- -----			-		...(SEE A33 REPL)		
-25	----- -----			1		....TERM SET,PIN:HEADER,1 X 10,0.15 SPACIN		
	----- -----			-		....(SEE A33J6400 REPL)		
-26	----- -----			AR		....CONTACT,SET ELEC:R ANGLE,0.250 L,STRIP		
	----- -----			-		....(SEE A33P6380,P6385 REPL)		
-27	----- -----			1		...CKT BOARD ASSY:WORD RECOGNIZER PROBE #1		
	----- -----			-		...(SEE A32 REPL)		
-28	----- -----					....TERM SET,PIN:HEADER,1 X 10,0.15 SP,RTA		
	----- -----			-		....(SEE A32J6300 REPL)		
-29	----- -----			1		....CONN RCPT,ELEC:CKT BD,RTANG,1 X 5,0.1		
	----- -----			-		....(SEE A32J6380 REPL)		
-30	----- -----			1		....CONN,RCPT,ELEC:CKT BD,RTANG,1 X 5,0.1		
	----- -----			-		....(SEE A32J6385 REPL)		
-31	----- -----			AR		....CONTACT SET,ELEC:RTANG,10.150 L		
	----- -----			-		....(SEE A32J6370 A REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-32	----- -----			AR		....CONTACT SET,ELEC:RTANG,0.250 L(3 WIDE)		
	----- -----			-		....(SEE A32J3708 REPL)		
-33	175-7932-00			1		.CA ASSY,SP,ELEC:6,26 AWG,15.0 L,9-N	80009	175-7932-00
						**********(ATTACHING PARTS)**********		
-34	220-0006-00			1		.NUT,PLAIN,HEX:12MM X 1MM		
-35	210-0021-00			1		.WASHER,LOCK:INTL,0.476 ID X 0.60"OD ST	78189	1222-01-00-0541C
	----- -----			1		.(FURNISHED WITH CONN/CABLE ASSY)		
						**********(END ATTACHING PARTS)**********		
-36	346-0120-00			1		.STRAP,TIEDOWN:5.5 L MIN,PLASTIC	06383	SST 1.5M
-37	131-0103-00			1		.CONN,RCPT,ELEC:BNC,FEMALE	91836	K79-304M06
	131-1343-00			1		.TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
-38	175-7931-00			1		.CABLE ASSY,RF:50 OHM COAX,4.25 L	80009	175-7931-00
	333-2877-00			1		.PANEL,FRONT:	80009	333-2877-00
	----- -----			-		.(2445/2465 OPT.06 ONLY)		
	333-2993-00			1		.PANEL,FRONT:	80009	333-2993-00
	----- -----			-		.(2445 OPT.06 & OPT.09 COMBINED)		
	333-2994-00			1		.PANEL,FRONT:2445 OPT.05/06 OPT COMBO	80009	333-2994-00
	----- -----			-		.(2445 OPT.05 & OPT. 06 COMBINED)		
	333-2990-00			1		.PANEL,FRONT:	80009	333-2990-00
	----- -----			-		.(2465 OPT.06 & OPT. 09 COMBINED)		
	333-2991-00			1		.PANEL,FRONT:2465 OPT.05/06 COMBO	80009	333-2991-00
	----- -----			-		.(2465 OPT. 05 & OPT.06 COMBINED)		
						STANDARD ACCESSORIES		
	010-6407-00			1		PROBE,WORD RECO:P6407	80009	010-6407-00
-39	012-0747-00			2		..LEAD SET,ELEC:10 WIDE,25 CML	80009	012-0747-00
-40	206-0222-00			20		TIP,PROBE:MICROCIRCUIT TEST	80009	206-0222-00
	070-4631-00			1		MANUAL,TECH:OPERATORS,2445/2465	80009	070-4631-00
	070-5366-00			1		CARD,INFO:REF,CTT OPT & WORD REC MENU	80009	070-5366-00
	070-4181-00			1		MANUAL,TECH:REFERENCE,2445/2465	80009	070-4181-00
						OPTIONAL ACCESSORIES		
	070-4632-00					MANUAL,TECH:SERVICE,2445/2465	80009	070-4632-00


A33
A32
A20
A27

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

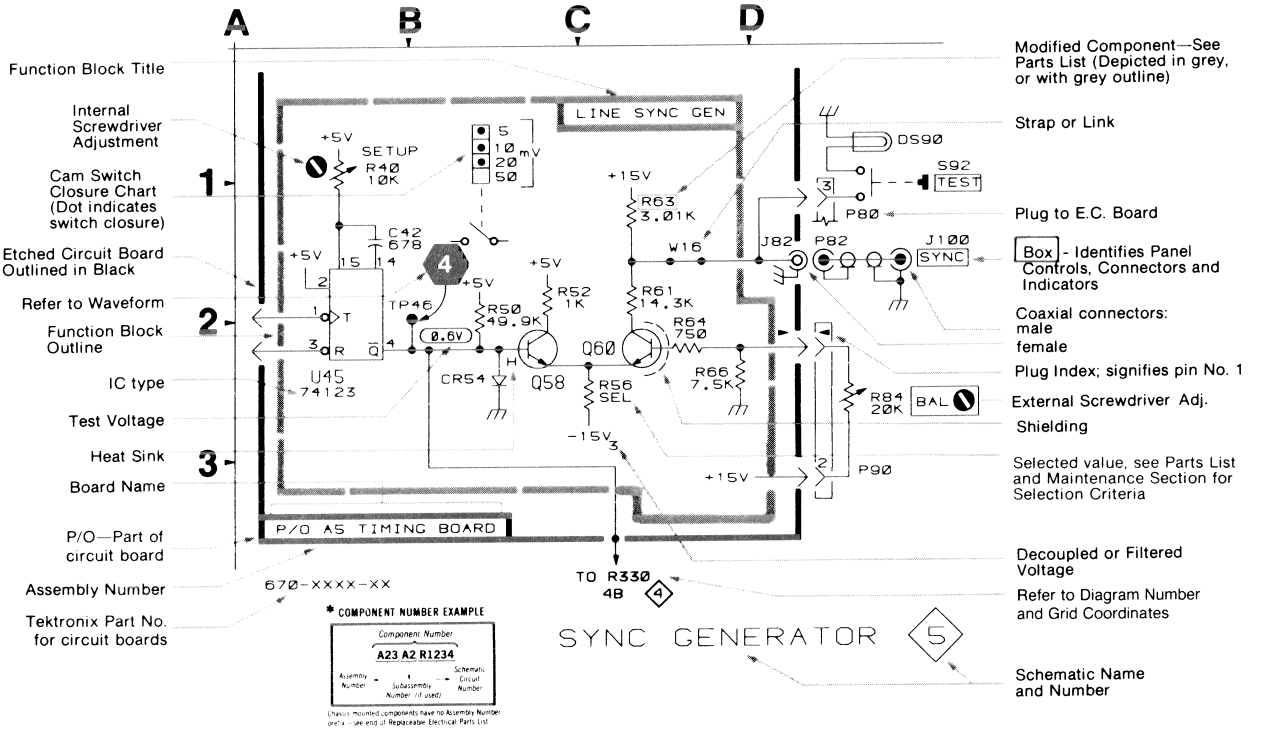
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

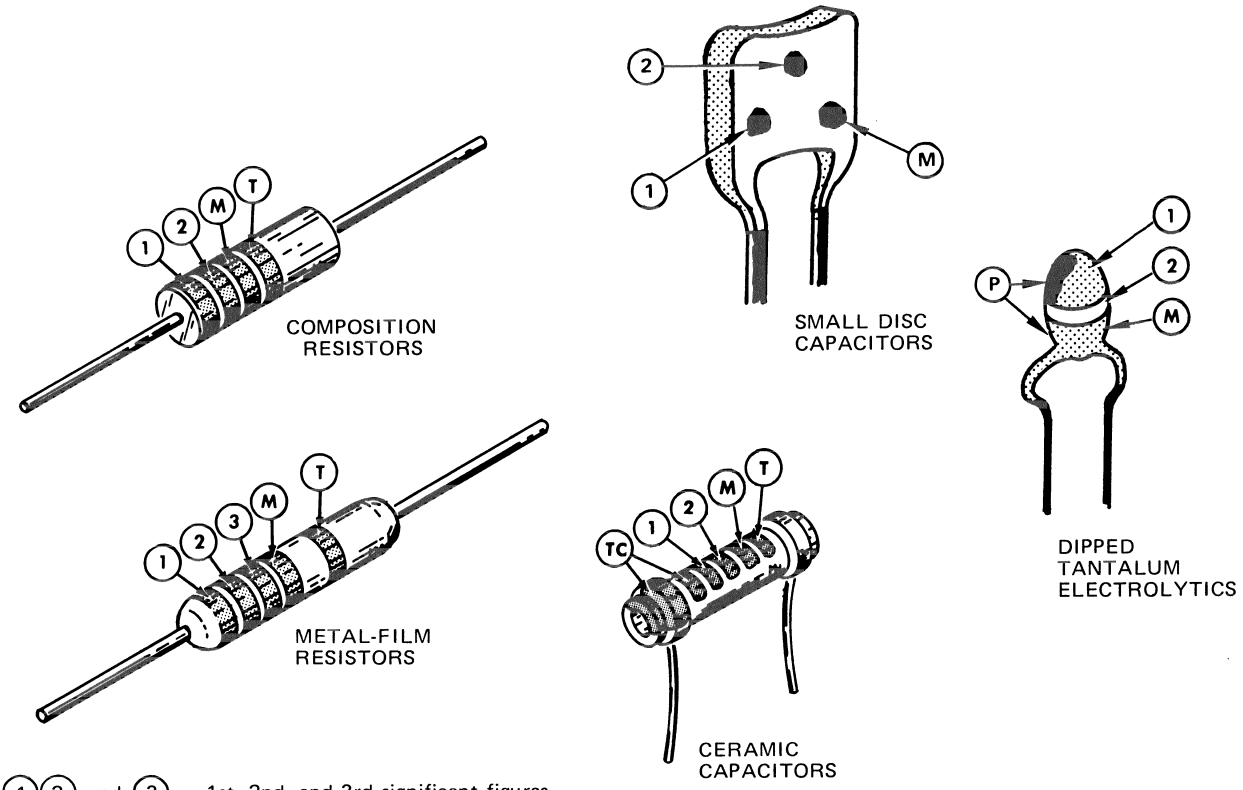
Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



COLOR CODE



(1) (2) and (3) – 1st, 2nd, and 3rd significant figures

(M) –multiplier (T) –tolerance

(TC) –temperature coefficient

(P) –polarity and voltage rating

(T) and/or (TC) color code may not be present on some capacitors

COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER	TOLERANCE	MULTIPLIER	TOLERANCE		
					over 10 pF	under 10 pF	
BLACK	0	1	---	1	±20%	±2 pF	4 VDC
BROWN	1	10	±1%	10	±1%	±0.1 pF	6 VDC
RED	2	10^2 or 100	±2%	10^2 or 100	±2%	---	10 VDC
ORANGE	3	10^3 or 1 K	±3%	10^3 or 1000	±3%	---	15 VDC
YELLOW	4	10^4 or 10 K	±4%	10^4 or 10,000	+100% –9%	---	20 VDC
GREEN	5	10^5 or 100 K	±½%	10^5 or 100,000	±5%	±0.5 pF	25 VDC
BLUE	6	10^6 or 1 M	±¼%	10^6 or 1,000,000	---	---	35 VDC
VIOLET	7	---	±1/10%	---	---	---	50 VDC
GRAY	8	---	---	10^{-2} or 0.01	+80% –20%	±0.25 pF	---
WHITE	9	---	---	10^{-1} or 0.1	±10%	±1 pF	---
GOLD	–	10^{-1} or 0.1	±5%	---	---	---	---
SILVER	–	10^{-2} or 0.01	±10%	---	---	---	---
NONE	–	---	±20%	---	±10%	±1 pF	---

(1861-20A)4206-31

Figure 7-1. Color code for resistors and capacitors.

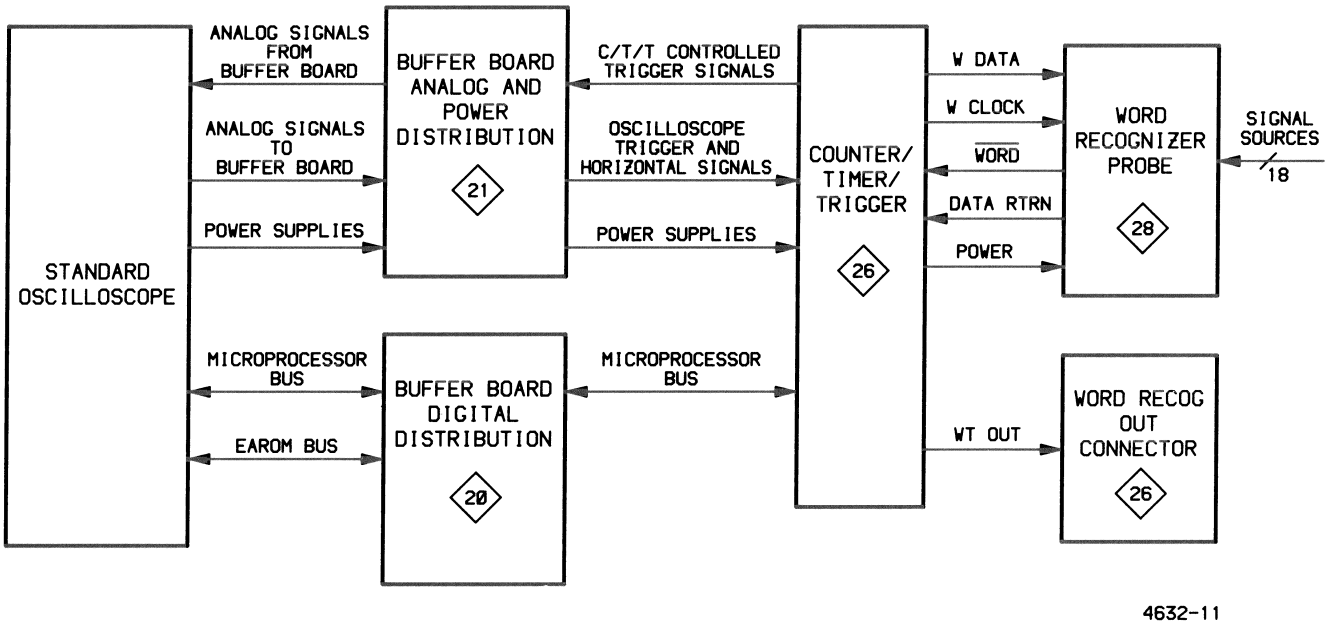


Figure 7-2. Simplified block diagram.

2445/2465 Option 06 and Option 09 Service

To identify any component mounted on a circuit board and to locate that component in the appropriate schematic diagram

1. Locate the Circuit Board Illustration

a. In the instrument identify the Assembly Number of the circuit board in question. The Assembly Number is usually printed on the upper left corner of the circuit board on the component side.

b. In the manual locate and pull out tabbed page whose title corresponds with the Assembly Number of the circuit board. Circuit board assembly numbers and board nomenclature are printed on the back side of the tabs (facing the rear of the manual).

2. Determine the Circuit Num

a. Compare the circuit boa the desired component l tion.

b. Scan the table adjacent t find the Circuit Number

c. Determine the Schemat component is located.

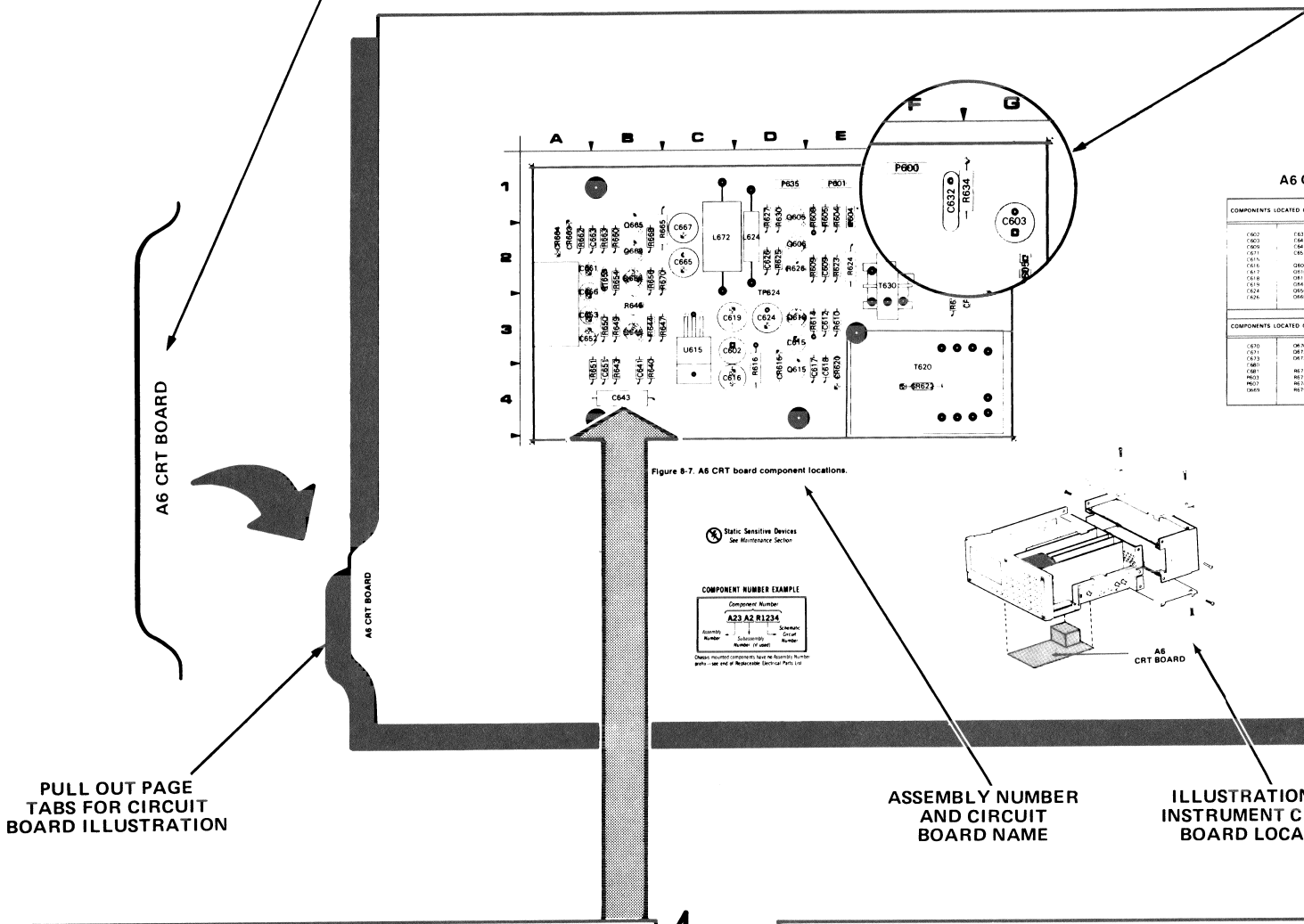


Figure 8-7. A6 CRT board component locations.

4. Determine the Circuit Board Illustration and Compo Location

a. From the schematic diagram, determine the As Number of the circuit board on which the compo mounted. This information is boxed and located in a of the heavy line that distinguishes the board outl

b. Scan the Component Location Table for the As Number just determined and find the Circuit Numbe desired component.

c. Under the BOARD LOCATION column, read th coordinates for the desired component.

5. Locate the Component on the Circuit Board

a. In the manual, locate and pull out the tabbed page whose title and Assembly Number correspond with the desired circuit board. This information is on the back side of the tabs.

b. Using the Circuit Number and grid coordinates, locate the component on the Circuit Board Illustration.

c. In the circuit board location illustration, determine the location of the circuit board in the instrument.

d. Find the circuit board in the instrument and compare it with its illustration in the manual to locate the desired component on the board.

Figure 7-3. Locating components on schematic diagrams

the Circuit Number

re the circuit board with its illustration and locate ired component by area and shape on the illustra-

ie table adjacent to the Circuit Board Illustration and e Circuit Number of the desired component.

ine the Schematic Diagram Number in which the nent is located.

3. L

a

b

A6 CRT BOARD

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 10

C602	C632	Q668	R625
C603	C641		R626
C609	C643	R604	R627
C671	C651	R605	R630
C615		R608	R632
C616	Q606	R609	
C617	Q610	R610	
C618	Q615	R614	
C619	Q645	R616	
C624	Q656	R623	
C626	Q665	R624	

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 11

C670	Q670	R677	
C671	Q672	R679	
C673	Q673	R680	
C680			
C681	R671	U617	
P603	R673	U618	
P607	R674	U619	
Q669	R675		

COMPONENT LOCATION TABLE

CRT CIRCUIT DIAGRAM 10

A6 ASSEMBLY

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C602	2C	3C	Q656	2F	2B
C603	1C	1G	Q665	1G	1B
C609	4E	2E	Q668	2G	2B
C612	7C	3E			
C615	7C	3D	R604	4C	1E
C616	2C	3C	R605	5D	1E
C617	7D	3D	R608	4E	1D
C618	7E	3E	R609	4E	2D
C619	6E	3C	R610	7B	3E
C624	4F	3D	R614	7C	3D
C626	7G	2D	R616	1C	3D
C632	8G	1F	R623	4D	2E
C643	3D	4B	R625	7F	2D
C651	3E	3B	R626	7F	2D
		3B	R627	7G	1D
			R630	4F	1D
Q606	4E	2D			
Q610	7C	3D	TP624	3B	2D
Q615	7D	3D			
Q645	3E	3B	U615	1D	3C

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L635	51	CHASSIS	V635	6J	CHASSIS

MANUAL BINDER

ILLUSTRATION FOR INSTRUMENT CIRCUIT BOARD LOCATION

MANUAL BINDER

tion and Component

etermine the Assembly which the component is d and located in a corner es the board outline.

Table for the Assembly he Circuit Number of the

column, read the grid onent.

ematic diagrams and circuit board illustrations.

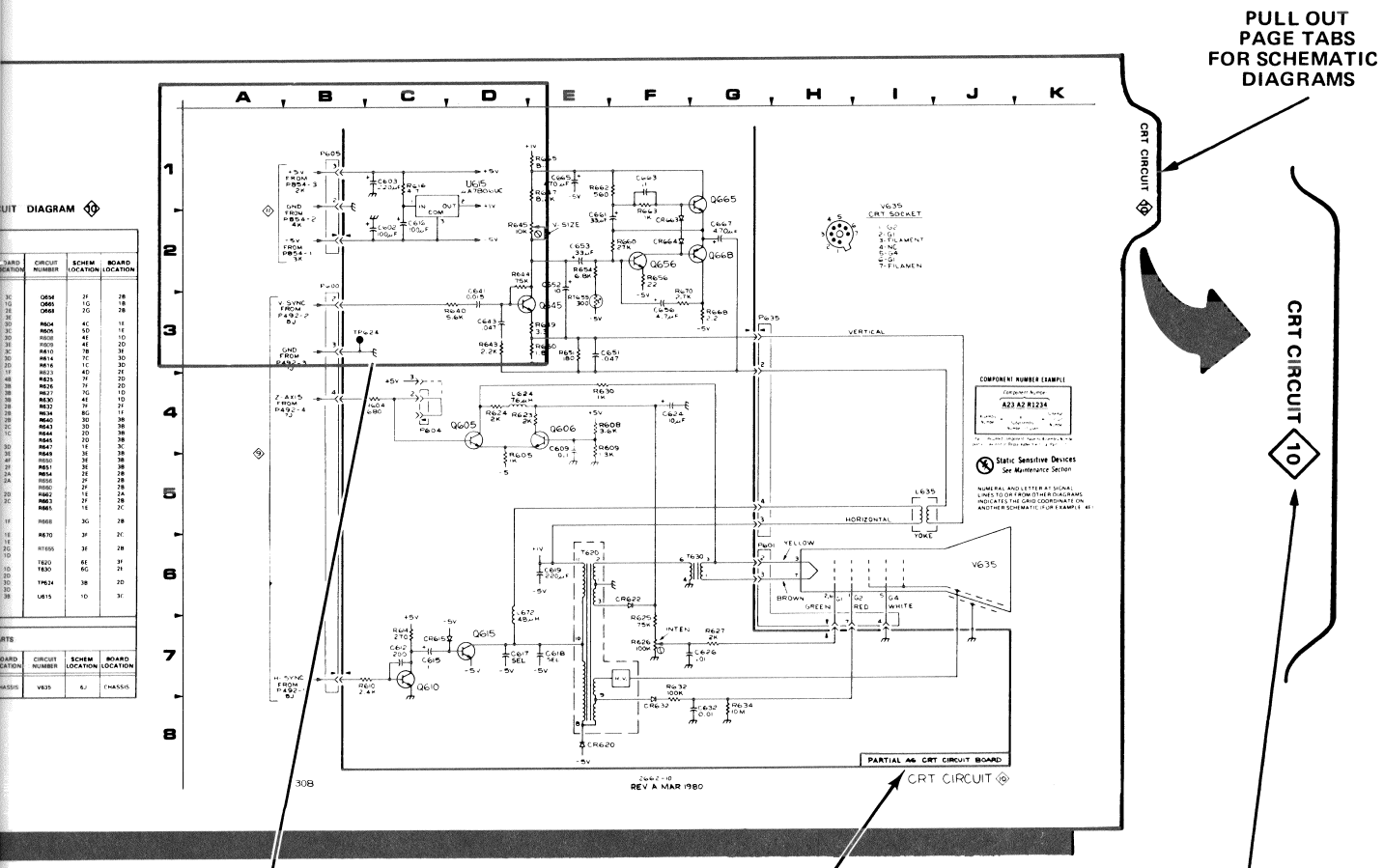
3. Locate the Component on the Schematic Diagram

a. Locate and pull out tabbed page whose number and title correspond with the Schematic Diagram Number just determined in the table. Schematic diagram nomenclature and numbers are printed on the front side of the tabs (facing the front of the manual).

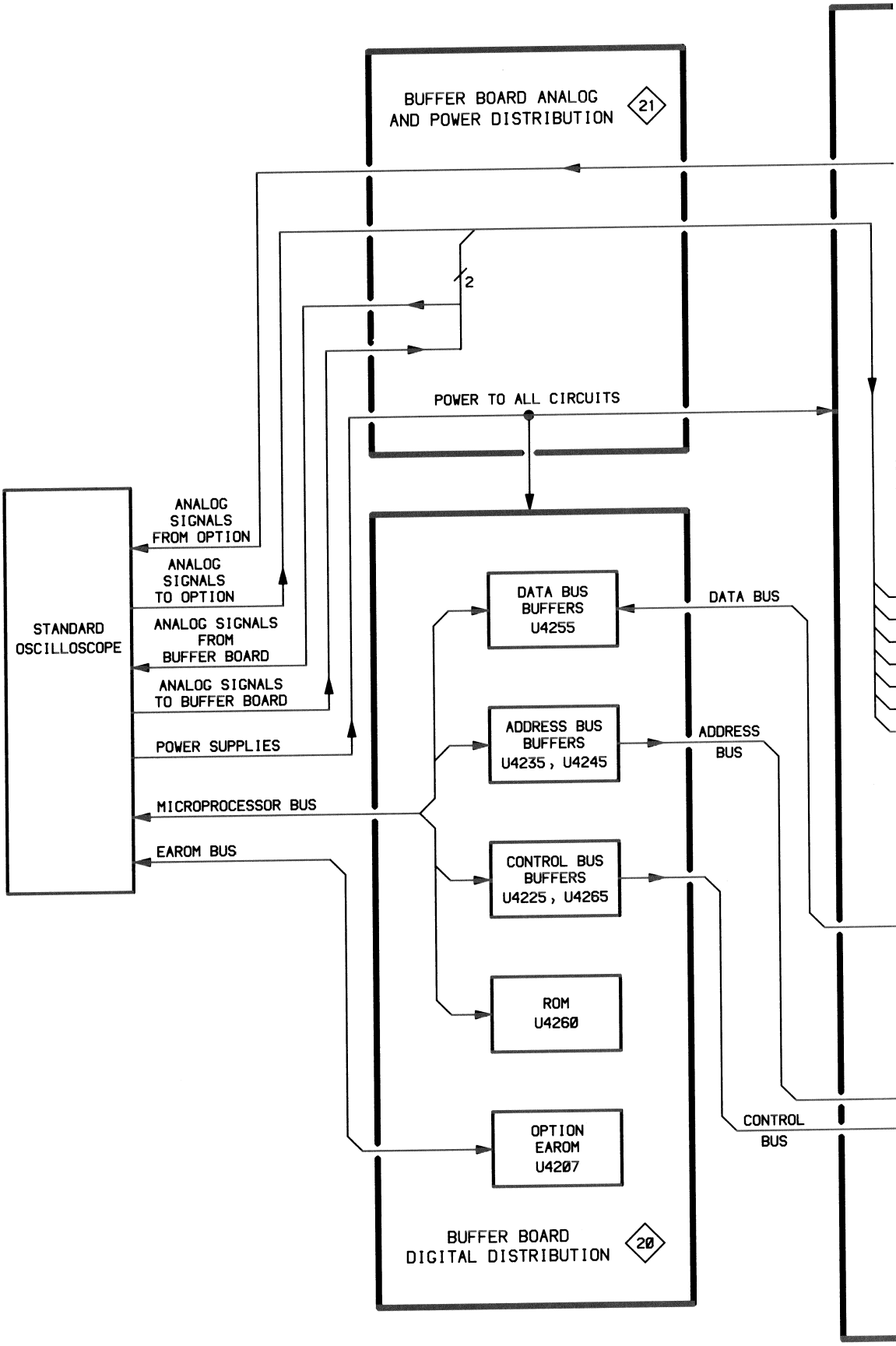
b. Scan the Component Location Table adjacent to the schematic diagram and find the Circuit Number of the desired component.

c. Under the SCHEM LOCATION column, read the grid coordinates for the desired component.

d. Using the Circuit Number and grid coordinates, locate the component on the schematic diagram.



(3516-81)4206-33


BUFFER BOARD ANALOG
AND POWER DISTRIBUTION
21
2
POWER TO ALL CIRCUITS
STANDARD
OSCILLOSCOPE
ANALOG
SIGNALS
FROM OPTION
ANALOG
SIGNALS
TO OPTION
ANALOG SIGNALS
FROM
BUFFER BOARD
ANALOG SIGNALS
TO BUFFER BOARD
POWER SUPPLIES
MICROPROCESSOR BUS
EAROM BUS
DATA BUS
BUFFERS
U4255
DATA BUS
ADDRESS BUS
BUFFERS
U4235, U4245
ADDRESS
BUS
CONTROL BUS
BUFFERS
U4225, U4265
ROM
U4260
OPTION
EAROM
U4207
CONTROL
BUS
BUFFER BOARD
DIGITAL DISTRIBUTION
20

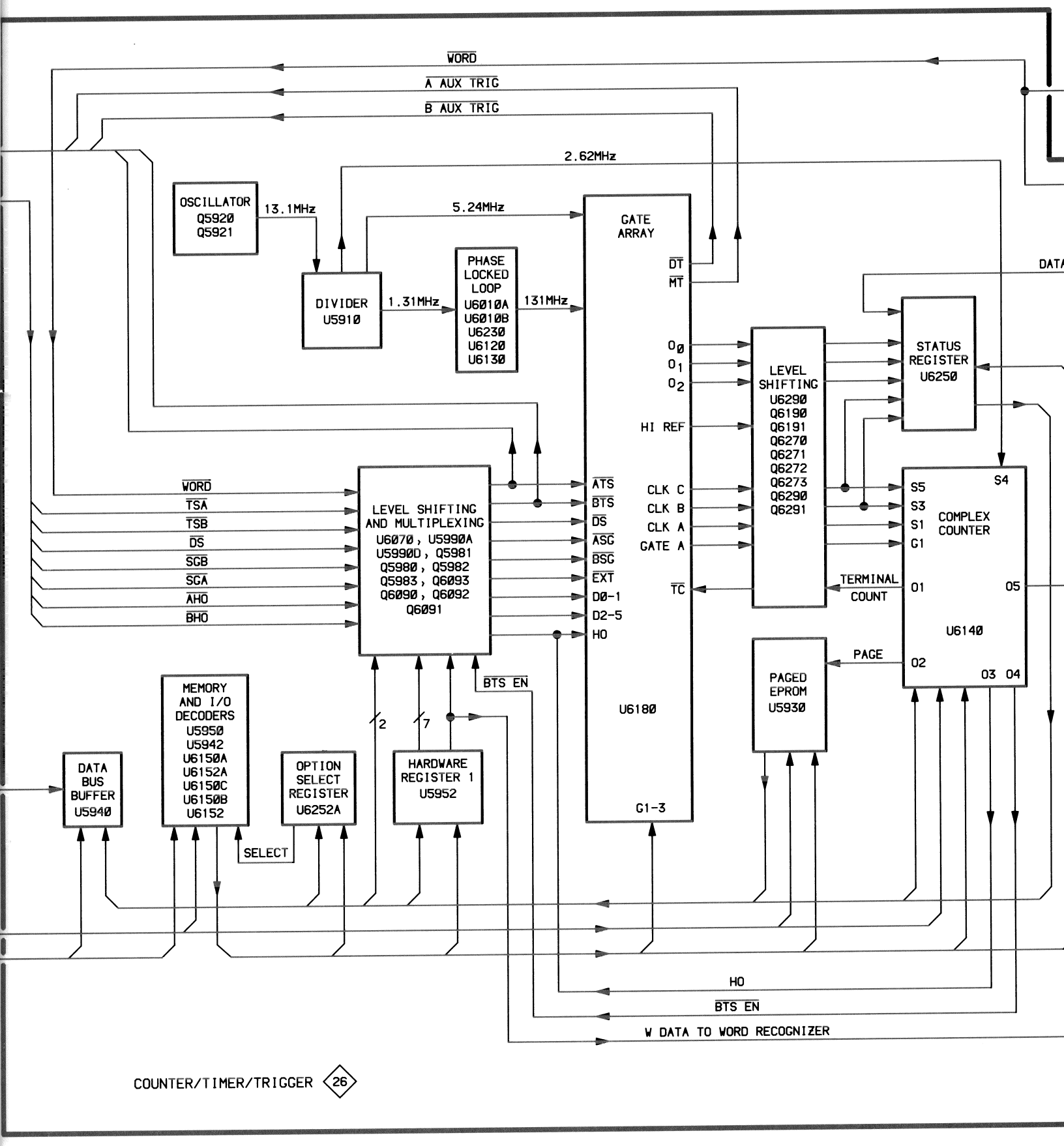
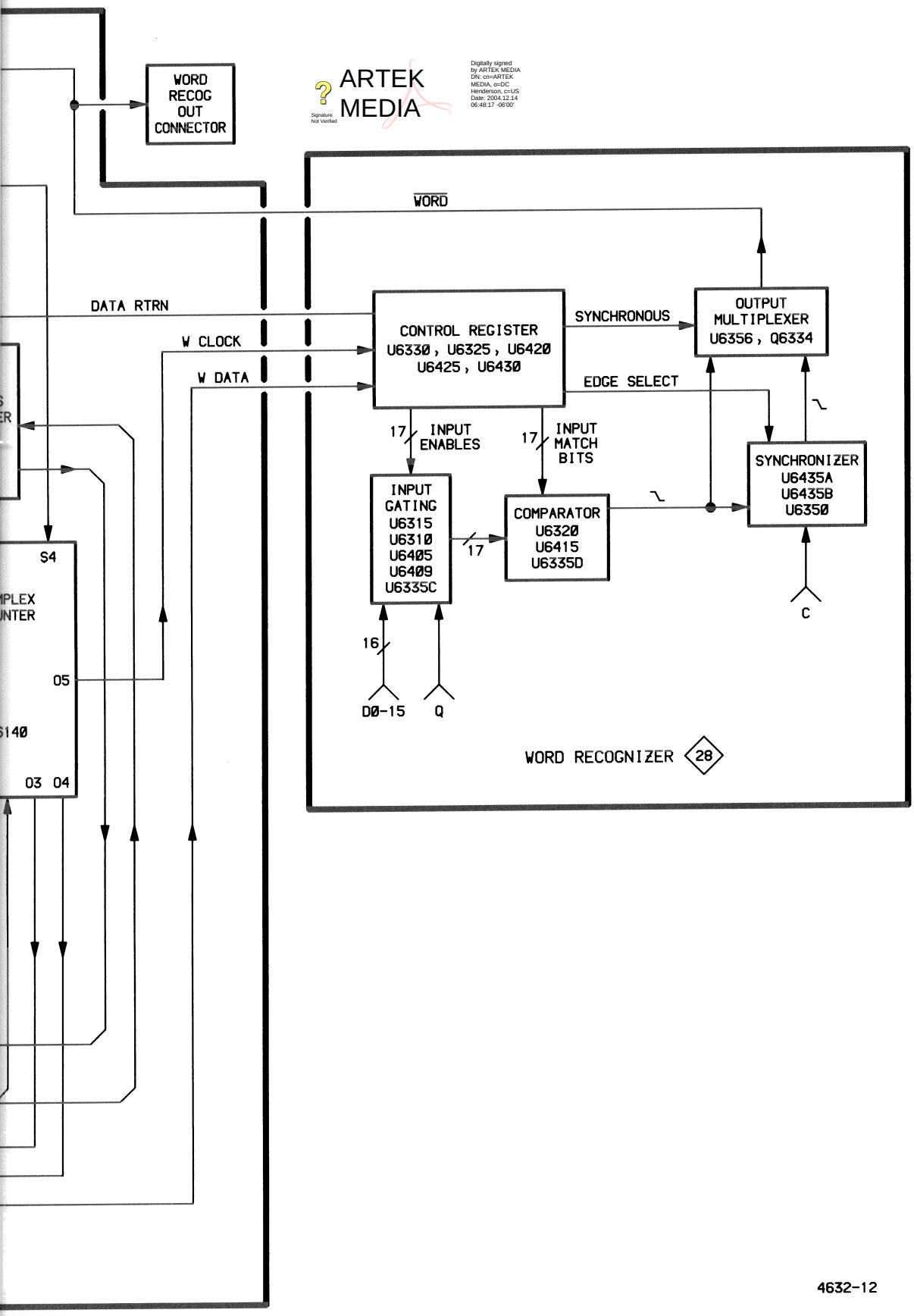


Figure 7-4. Detailed block diagram.



4632-12

DETAILED BLOCK DIAGRAM FIG. 7-4

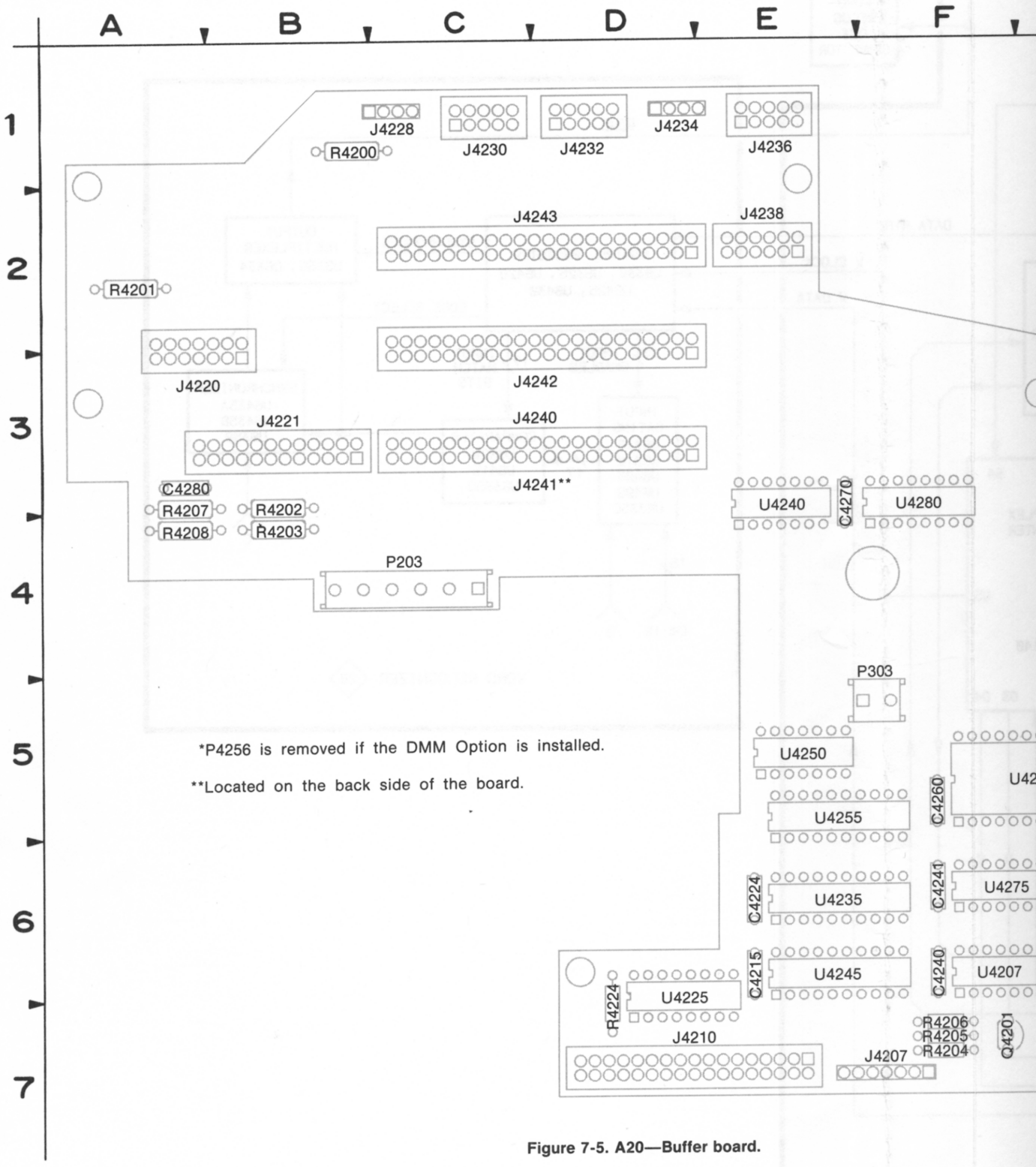
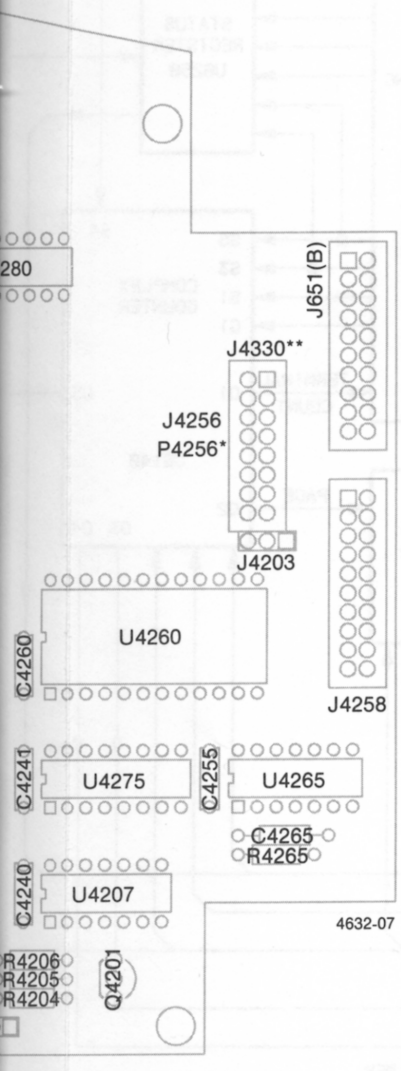
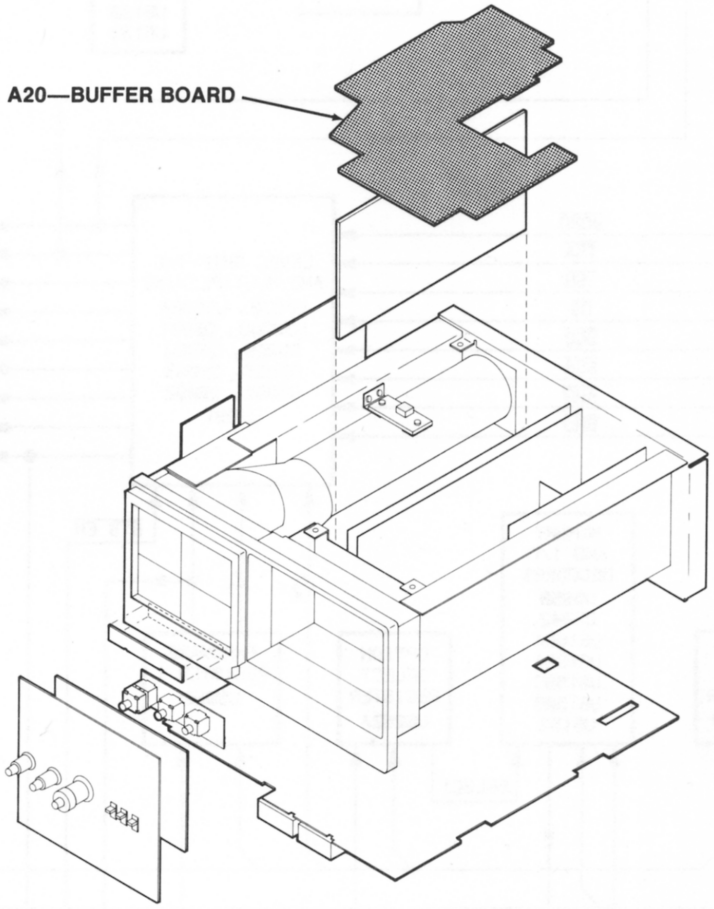


Figure 7-5. A20—Buffer board.

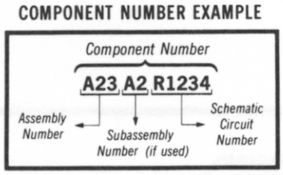
F G H





Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A20—BUFFER BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C4215	21	J4238	21	R4203	21	U4250	20
C4224	21	J4240	20	R4204	20	U4250	20
C4240	21	J4240	21	R4205	20	U4250	20
C4241	21	J4241	20	R4206	20	U4250	21
C4255	21	J4241	21	R4207	21	U4255	20
C4260	21	J4242	20	R4208	21	U4255	21
C4265	20	J4242	21	R4224	20	U4260	20
C4270	21	J4243	20	R4265	20	U4260	21
C4280	21	J4243	21	U4207	20	U4265	20
J651(B)	21	J4256	20	U4207	20	U4265	20
J4203	21	J4258	21	U4225	20	U4265	20
J4207	20	J4330	20	U4225	21	U4265	20
J4210	20	J4330	21	U4235	20	U4265	21
J4220	21	P203	21	U4235	21	U4275	20
J4221	21	P303	21	U4240	20	U4275	21
J4228	21	P4256	20	U4240	20	U4280	20
J4230	21	Q4201	20	U4240	20	U4280	21
J4232	21	R4200	21	U4240	21		
J4234	21	R4201	21	U4245	20		
J4236	21	R4202	21	U4245	21		

BUFFER BOARD DIGITAL DISTRIBUTION 20

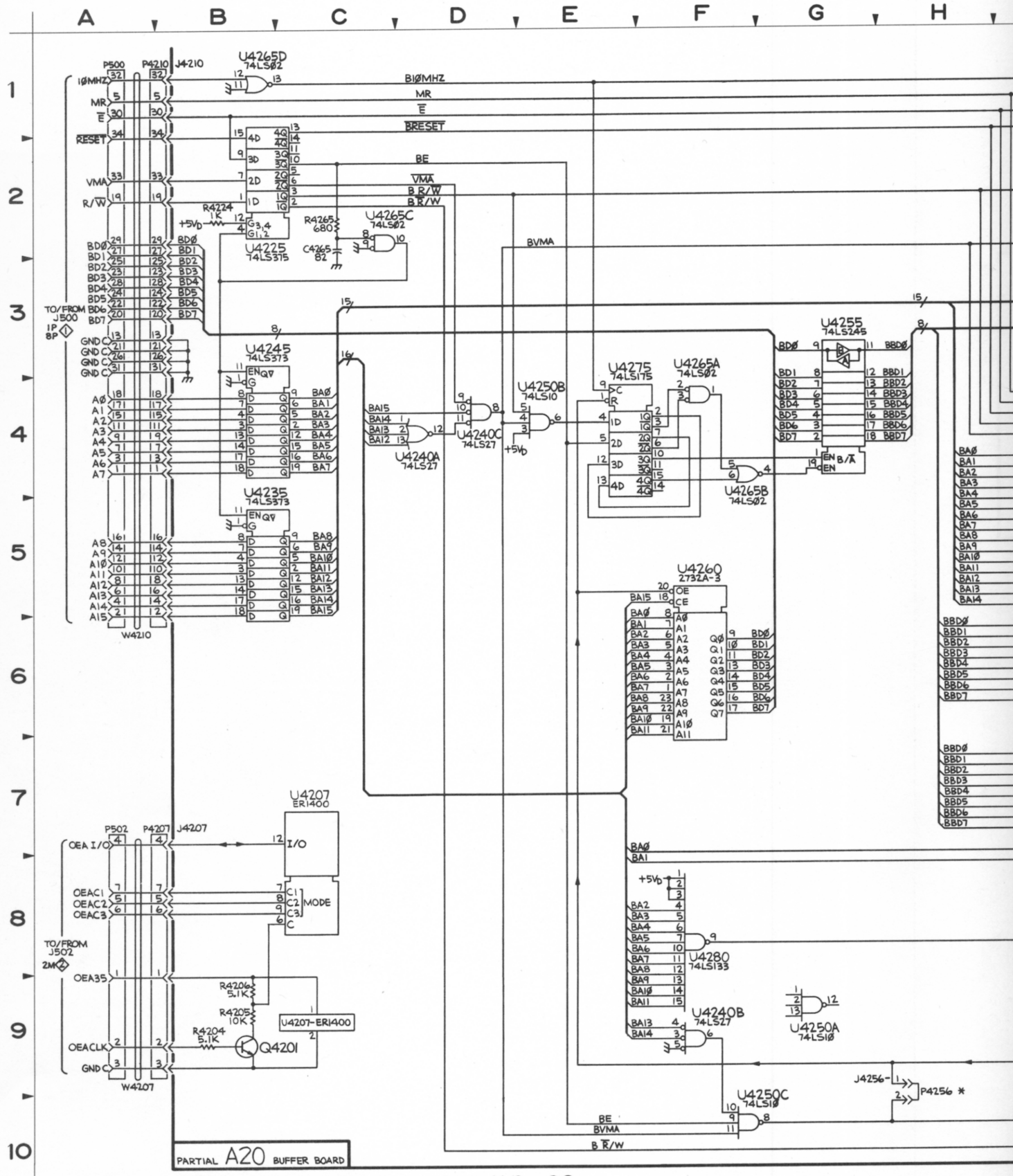
ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C4265	2C	6G	P4256	10H	4G	U4207	7C	6F	U4250C	10F	5E
						U4207	9C	6F	U4255	3G	5E
J4207	7B	7F	Q4201	9B	7F	U4225	2B	7D	U4260	5F	5G
J4210	1B	7D				U4235	4B	6E	U4265A	3F	6G
J4240	3L	3D	R4204	9B	7F	U4240A	4D	3E	U4265B	4F	6G
J4241	3J	3D	R4205	9B	7F	U4240B	9F	3E	U4265C	2C	6G
J4242	3N	3D	R4206	9B	7F	U4240C	4D	3E	U4265D	1B	6G
J4243	1S	2D	R4224	2B	7D	U4245	3B	6E	U4275	3E	6F
J4256	9G	4G	R4265	2C	6G	U4250A	9G	5E	U4280	8F	3F
J4330	7J	4G				U4250B	4E	5E			

Partial A20 also shown on diagram 21.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P500	1A	CHASSIS	P4207	7A	CHASSIS	W4207	9A	CHASSIS			
P502	7A	CHASSIS	P4210	1A	CHASSIS	W4210	6A	CHASSIS			



2445/2465 OPTIONS 06 AND 09

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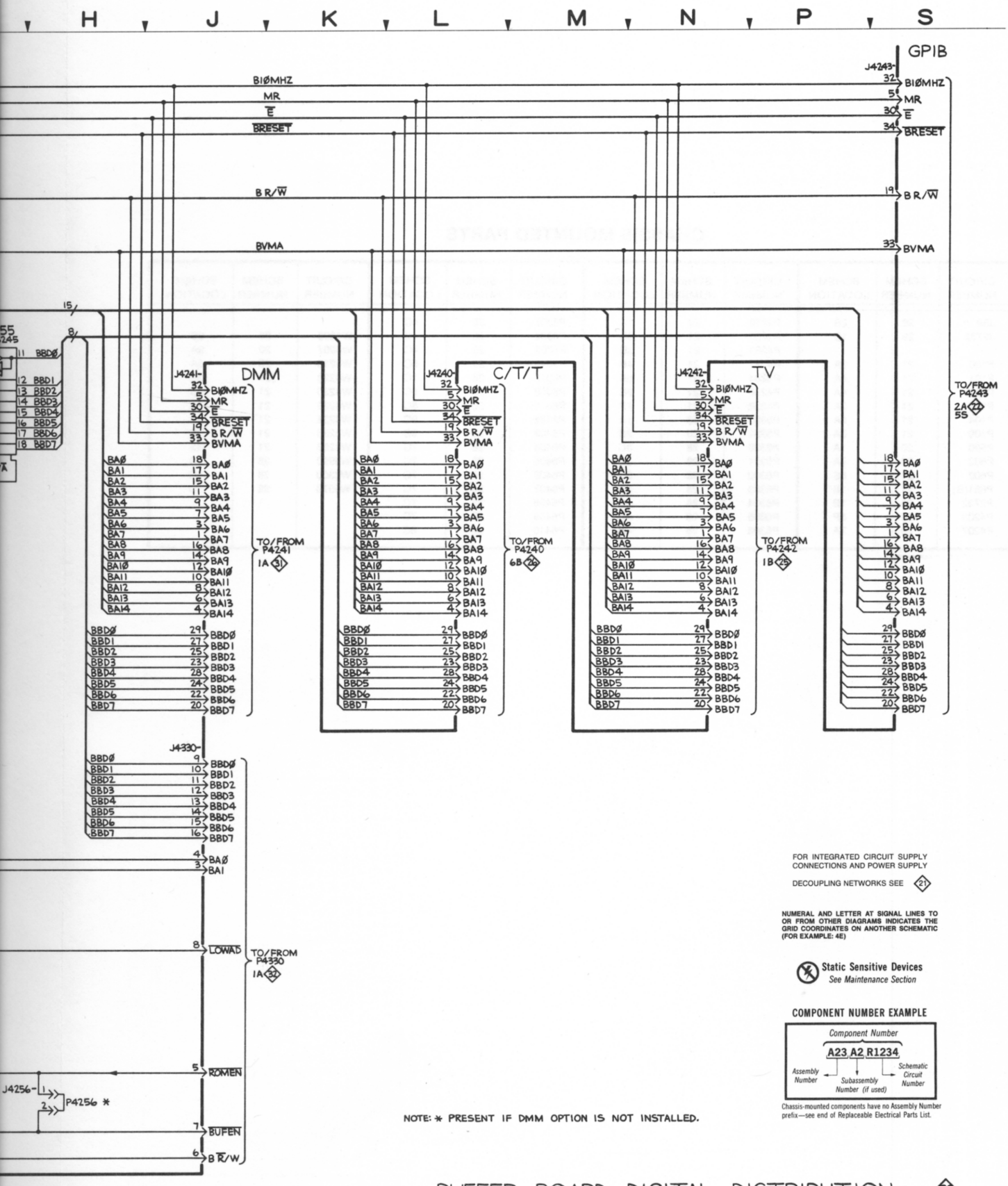

FOR INTEGRATED CIRCUIT SUPPLY CONNECTIONS AND POWER SUPPLY DECOUPLING NETWORKS SEE 21

NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

NOTE: * PRESENT IF DMM OPTION IS NOT INSTALLED.

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BUFFER BOARD DIGITAL DISTRIBUTION 20

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION
J59	26	2S	P4210	20	1A	P6307	28	4C			
J2732	28	1B	P4228	21	3B	P6308	28	4C	W4203	21	9S
			P4230	21	3B	P6309	28	4C	W4207	20	9A
P100	21	3A	P4232	21	4B	P6310	28	5C	W4210	20	6A
P101	21	6A	P4234	21	5B	P6370	28	1C	W4228	21	3B
P102	21	4A	P4236	21	6B	P6400	28	6C	W4230	21	4B
P103	21	3A	P4258	21	1P	P6401	28	8C	W4232	21	5B
P104	21	5A	P5990	28	1A	P6402	28	8C	W4234	21	6B
P109	21	3A	P5991	26	2S	P6403	28	8C	W4236	21	7B
P500	20	1A	P6300	28	3C	P6404	28	7C	W4258	21	3S
P502	20	7A	P6301	28	3C	P6405	28	7C	W5990	28	1B
P602	21	8S	P6302	28	3C	P6406	28	7C	W6300	28	5C
P651(B)	21	1S	P6303	28	3C	P6407	28	7C	W6370	28	2C
P2732	28	1B	P6304	28	4C	P6408	28	7C			
P4203	21	8P	P6305	28	4C	P6409	28	7C			
P4207	20	7A	P6306	28	4C	P6410	28	6C			

BUFFER BOARD ANALOG AND POWER DISTRIBUTIONS 21

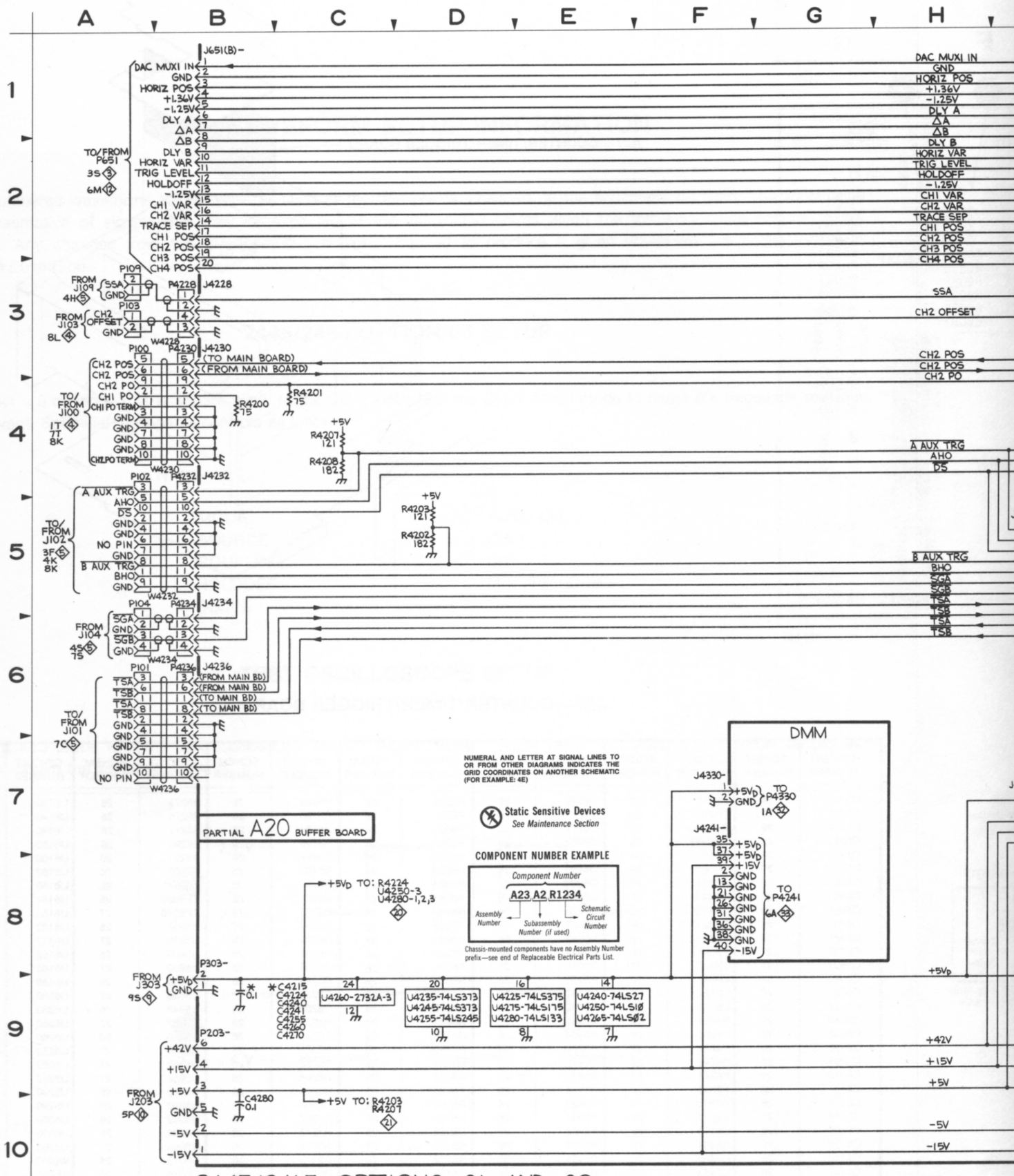
ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C4215	9C	6E	J4221	5J	3B	J4330	7F	4G	U4225	9D	7D
C4224	9C	6E	J4228	3B	1C				U4235	9D	6E
C4240	9C	6F	J4230	3B	1C	P203	9B	4C	U4240	9E	3E
C4241	9C	6F	J4232	4B	1D	P303	8B	5F	U4245	9D	6E
C4255	9C	6G	J4234	5B	1D				U4250	9E	5E
C4260	9C	5F	J4236	6B	1E	R4200	4B	1B	U4255	9D	5E
C4270	9C	3E	J4238	5P	2E	R4201	4C	2A	U4260	9C	5G
C4280	10B	3A	J4240	7J	3D	R4202	5D	3B	U4265	9E	6G
			J4241	7F	3D	R4203	5D	4B	U4275	9D	6F
J651(B)	1B	4G	J4242	7L	3D	R4207	4C	3A	U4280	9D	3F
J4203	8P	5G	J4243	6P	2D	R4208	4C	4A			
J4220	5L	3A	J4258	1P	5G						

Partial A20 also shown on diagram 20.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P100	3A	CHASSIS	P602	8S	CHASSIS	P4234	5B	CHASSIS	W4230	4B	CHASSIS
P101	6A	CHASSIS	P651(B)	1S	CHASSIS	P4236	6B	CHASSIS	W4232	5B	CHASSIS
P102	4A	CHASSIS	P4203	8P	CHASSIS	P4258	1P	CHASSIS	W4234	6B	CHASSIS
P103	3A	CHASSIS	P4228	3B	CHASSIS				W4236	7B	CHASSIS
P104	5A	CHASSIS	P4230	3B	CHASSIS	W4203	9S	CHASSIS	W4258	3S	CHASSIS
P109	3A	CHASSIS	P4232	4B	CHASSIS	W4228	3B	CHASSIS			



2445/2465 OPTIONS 06 AND 09

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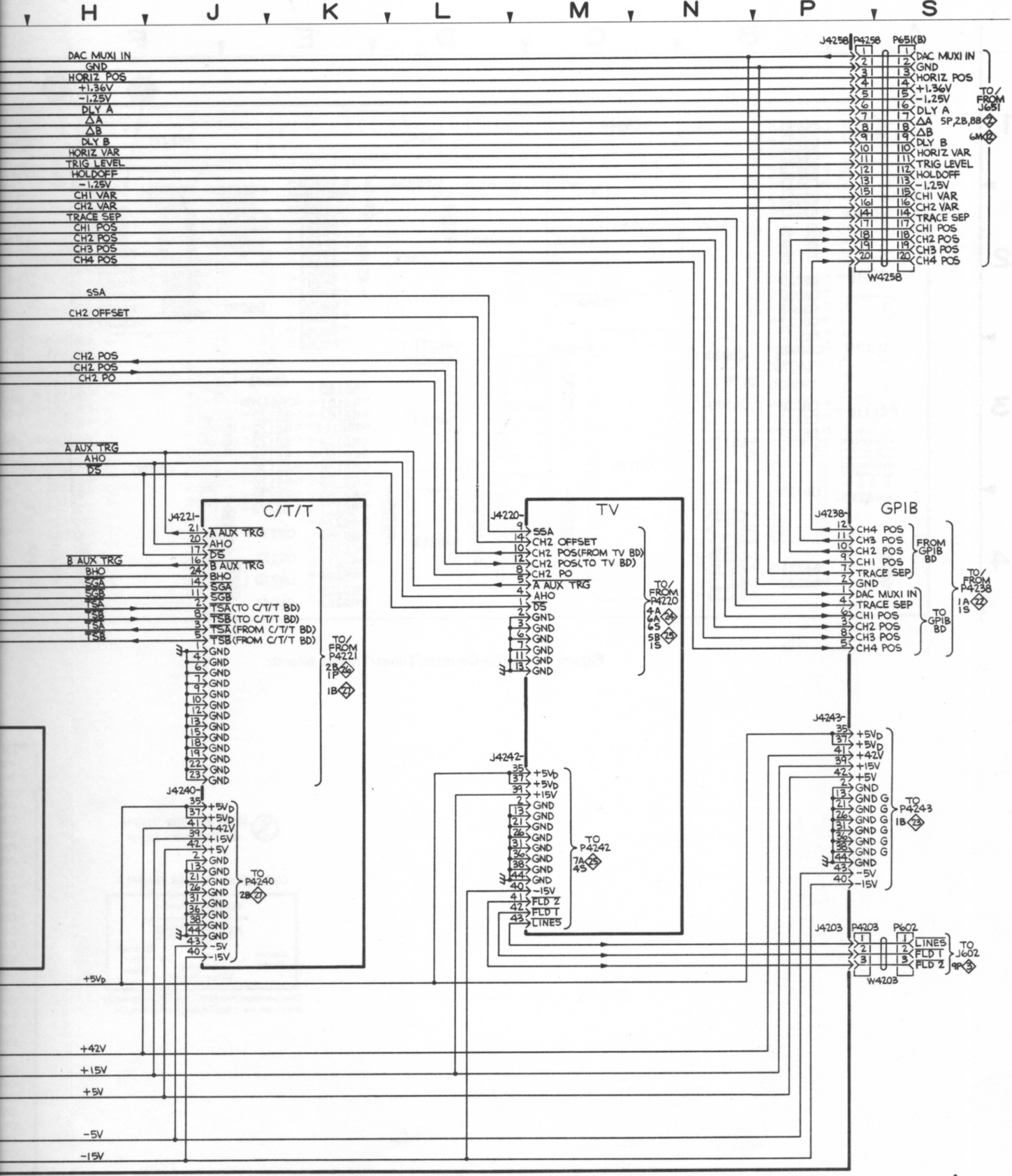


4632-16

BUFFER BOARD ANALOG AND POWER DISTRIBUTIONS 21

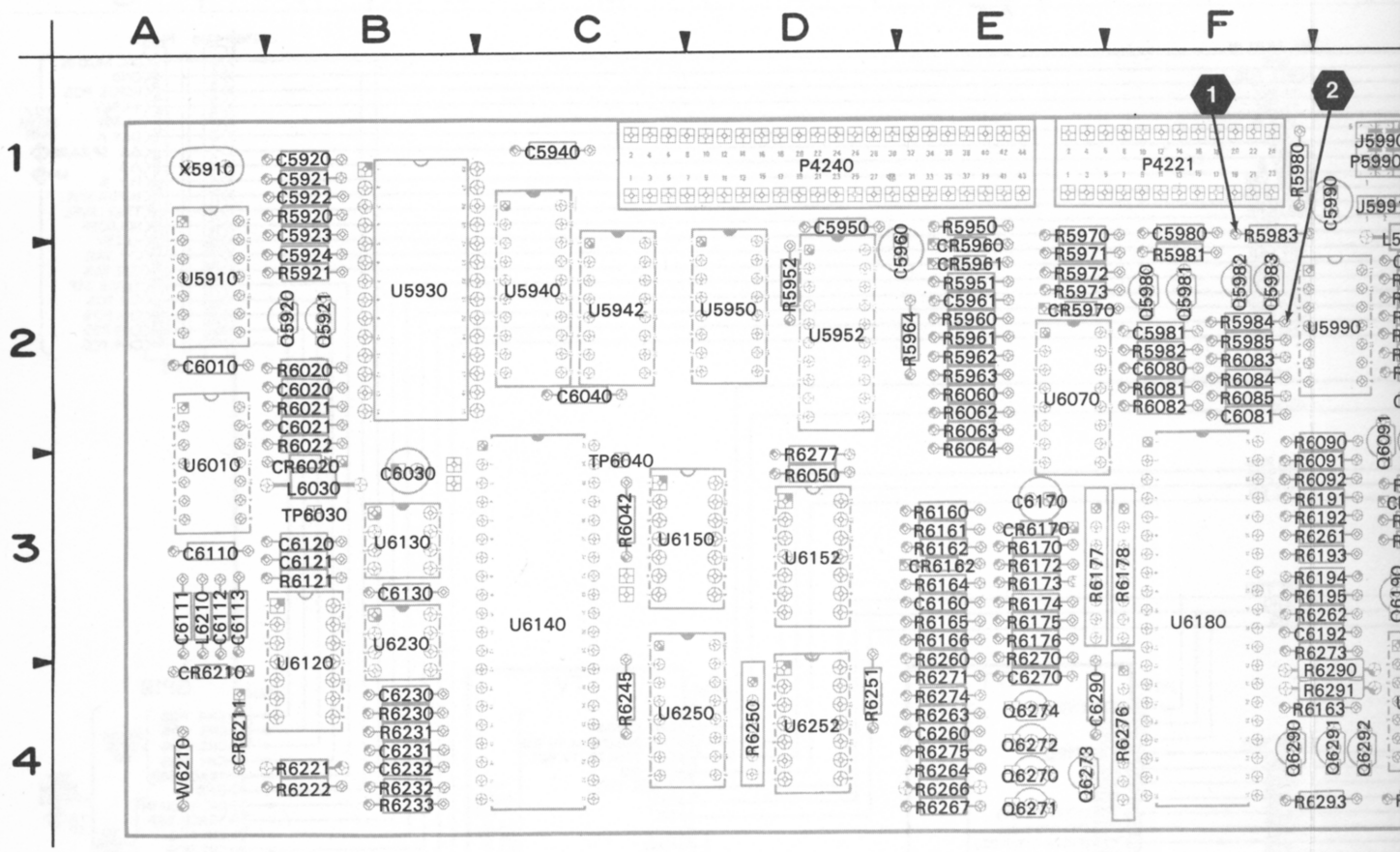
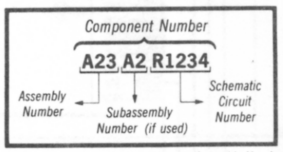


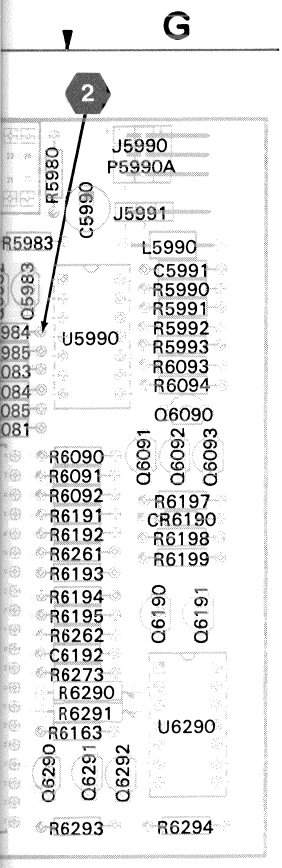
Figure 7-6. A27—Counter/Timer/Trigger board.

Static Sensitive Devices
See Maintenance Section

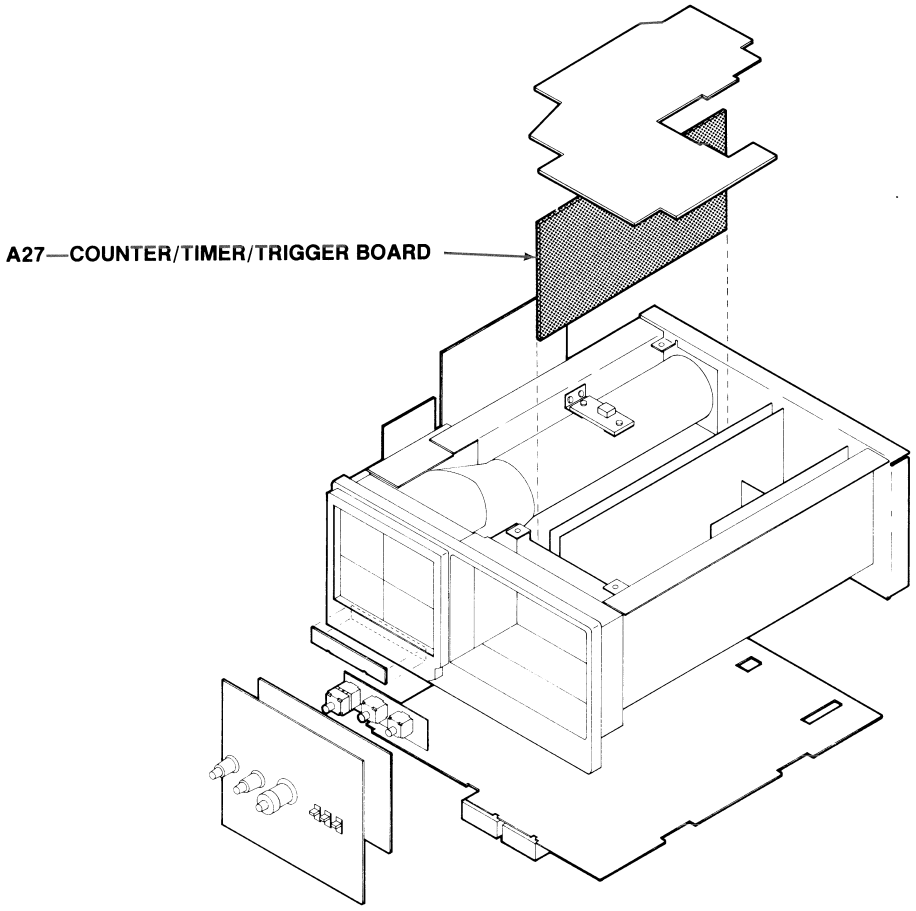
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



4632-08



A27—COUNTER/TIMER/TRIGGER BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C5920	26	C6270	27	Q6270	26	R6022	26	R6192	26	R6276	26	U6130	27
C5921	27	C6290	26	Q6271	26	R6042	26	R6193	26	R6276	26	U6140	26
C5922	26	CR5960	26	Q6272	26	R6050	26	R6194	26	R6277	26	U6140	27
C5923	26	CR5961	26	Q6273	26	R6060	26	R6195	26	R6290	26	U6150	26
C5924	26	CR5970	26	Q6274	26	R6062	26	R6197	26	R6291	26	U6150	26
C5940	27	CR6020	26	Q6290	26	R6063	26	R6198	26	R6293	26	U6150	26
C5950	27	CR6162	26	Q6291	26	R6064	26	R6199	26	R6294	26	U6150	27
C5960	27	CR6170	27	Q6292	26	R6081	26	R6221	26	TP6030	26	U6152	26
C5961	26	CR6190	26	R5920	26	R6082	26	R6222	26	TP6040	27	U6152	26
C5980	26	CR6210	26	R5921	26	R6083	26	R6230	26	U5910	26	U6152	26
C5981	26	CR6211	26	R5950	26	R6084	26	R6231	26	U5910	27	U6152	26
C5990	27	J5990	26	R5951	26	R6085	26	R6232	26	U5930	26	U6152	27
C5991	27	J5991	26	R5952	26	R6090	26	R6233	26	U5930	27	U6180	26
C6010	27	L5990	27	R5960	26	R6091	26	R6245	26	U5940	26	U6180	27
C6020	27	L6030	27	R5961	26	R6092	26	R6250	26	U5940	27	U6230	26
C6021	26	L6210	26	R5962	26	R6093	26	R6250	26	U5942	26	U6230	27
C6030	27	P4221	26	R5963	26	R6094	26	R6251	26	U5942	27	U6250	26
C6040	27	P4221	26	R5964	26	R6121	26	R6260	26	U5950	26	U6250	27
C6080	26	P4221	27	R5970	26	R6160	26	R6261	26	U5950	27	U6252	26
C6081	27	P4240	26	R5971	26	R6161	26	R6262	26	U5952	26	U6252	26
C6110	26	P4240	27	R5972	26	R6162	26	R6263	26	U5952	27	U6252	27
C6111	26	P5990	26	R5973	26	R6163	26	R6264	26	U5990	26	U6290	26
C6112	26	Q5920	26	R5980	26	R6164	26	R6266	26	U5990	26	U6290	26
C6113	27	Q5921	26	R5981	26	R6165	26	R6267	26	U5990	26	U6290	26
C6120	26	Q5980	26	R5982	26	R6166	26	R6270	26	U5990	26	U6290	26
C6121	27	Q5981	26	R5983	26	R6170	26	R6271	26	U5990	27	U6290	27
C6130	26	Q5982	26	R5984	26	R6172	26	R6273	26	U6010	26	W6210	27
C6160	26	Q5983	26	R5985	26	R6173	26	R6274	26	U6010	26	X5910	26
C6170	27	Q6090	26	R5990	26	R6174	26	R6275	26	U6010	27		
C6192	27	Q6091	26	R5991	26	R6175	26	R6276	26	U6070	26		
C6230	26	Q6092	26	R5992	26	R6176	26	R6276	26	U6070	27		
C6231	27	Q6093	26	R5993	26	R6177	26	R6276	26	U6120	26		
C6232	26	Q6190	26	R6020	26	R6178	26	R6276	26	U6120	27		
C6260	27	Q6191	26	R6021	26	R6191	26	R6276	26	U6130	26		

TEST WAVEFORM SETUP INFORMATION

The numbered waveforms below were obtained at the test points indicated on the schematic diagram. The waveforms are representative of signals that may be expected at the associated points when the following setup conditions are observed. Any changes from the given setup conditions required to produce a given waveform are noted with that waveform illustration.

2445/2465 OPTION 06 SETUP

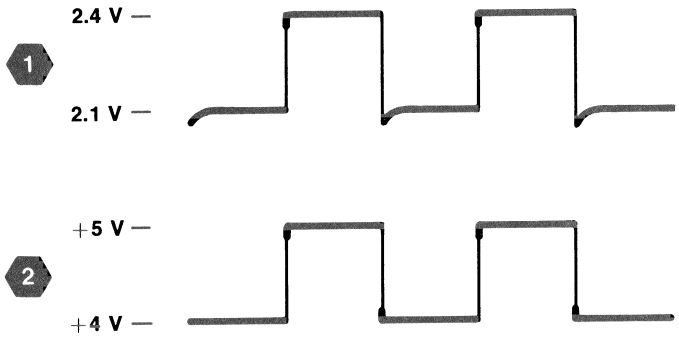
Connect a 6 division, 1 MHz square wave to the CH 2 input. Set the C/T/T Menu mode to count the frequency of the A Trigger event. Set initial front-panel controls as follows:

Trigger

MODE	AUTO LVL
SOURCE	CH 1
COUPLING	DC
HOLDOFF	MIN (Fully CCW)
SLOPE	+

TEST OSCILLOSCOPE SETUP

Using a X10 probe with the test oscilloscope, set its Trigger Slope, Trigger Level, Volts/Div, and Time/Div ranges as required to obtain the indicated displays.



COUNTER/TIMER/TRIGGER 26

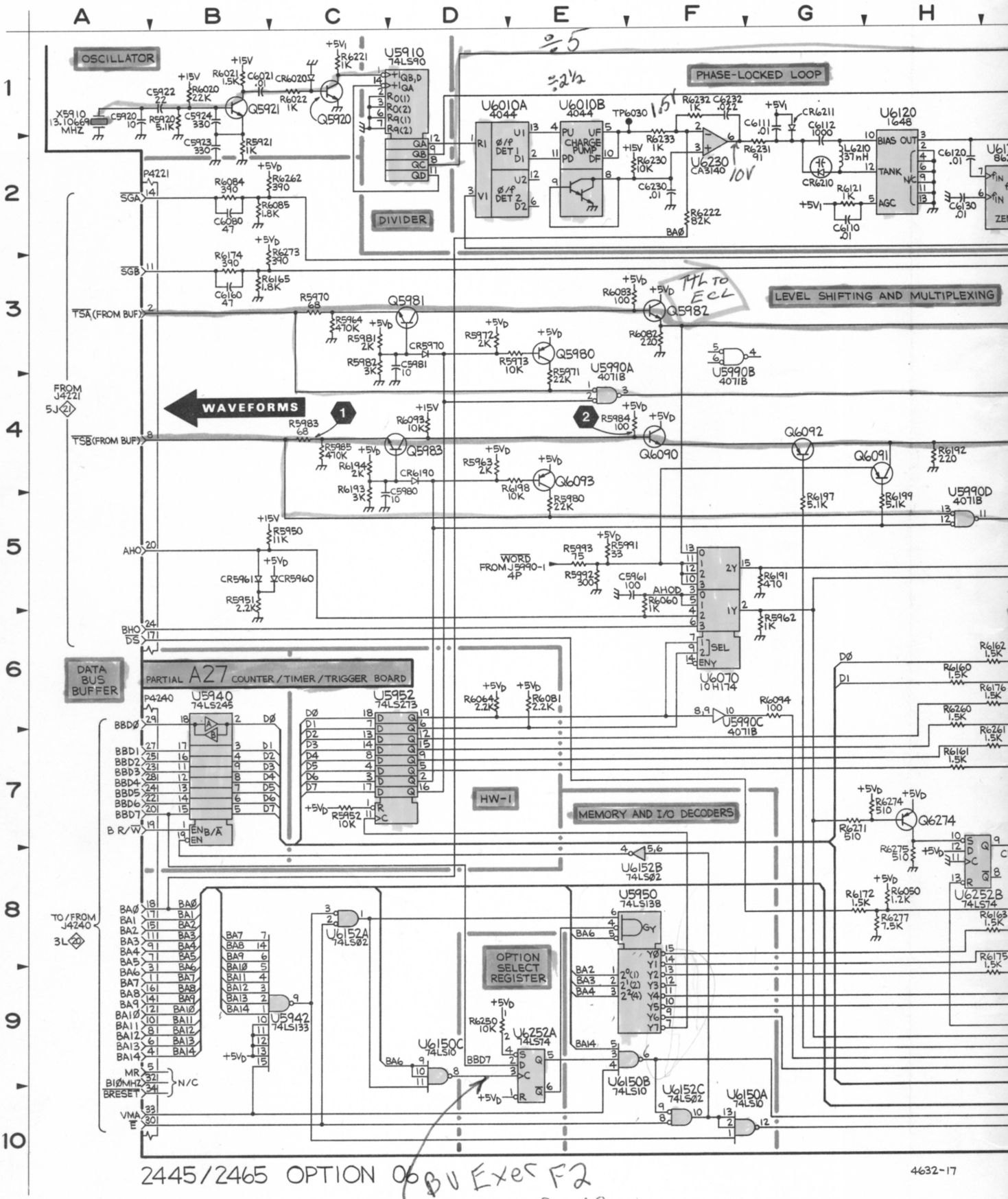
ASSEMBLY A27

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C5920	1A	1B	Q6270	5L	4E	R6093	4D	2G	R6276C	5K	4F
C5922	1B	1B	Q6271	7L	4E	R6094	6G	2G	R6276D	6K	4F
C5923	2B	1B	Q6272	5L	4E	R6121	2G	3B	R6276E	4L	4F
C5924	1B	2B	Q6273	7L	4E	R6160	6H	3E	R6276F	4L	4F
C5961	5F	2E	Q6274	7H	4E	R6161	7H	3E	R6276G	7K	4F
C5980	4D	1F	Q6290	6L	4F	R6162	6J	3E	R6277	8H	3D
C5981	3D	2F	Q6291	6L	4G	R6163	8J	4G	R6290	4L	4G
C6021	1B	2B	Q6292	7P	4G	R6164	3P	3E	R6291	4L	4G
C6080	2B	2F				R6165	3C	3E	R6293	6L	4G
C6110	2G	3A	R5920	1B	1B	R6166	5L	3E	R6294	6L	4G
C6111	1G	3A	R5921	2B	2B	R6170	8J	3E			
C6112	1G	3A	R5950	5C	1E	R6172	8G	3E	TP6030	1E	3B
C6120	2H	3B	R5951	5B	2E	R6173	8J	3E			
C6130	2H	3B	R5952	7C	2D	R6174	2B	3E	U5910	1D	2A
C6160	3B	3E	R5960	2L	2E	R6175	8J	3E	U5930	8S	2B
C6230	2F	4B	R5961	2L	2E	R6176	6J	3E	U5940	6B	2C
C6232	1F	4B	R5962	6G	2E	R6177	7J	3E	U5942	9C	2C
C6290	4L	4E	R5963	4D	2E	R6178	5J	3F	U5950	8F	2D
			R5964	3C	2E	R6191	5G	3G	U5952	6D	2D
CR5960	5C	2E	R5970	3C	2E	R6192	4H	3G	U5990A	3E	2G
CR5961	5B	2E	R5971	3E	2E	R6193	4C	3G	U5990B	4F	2G
CR5970	3D	2E	R5972	3D	2E	R6194	4C	3G	U5990C	6F	2G
CR6020	1C	3B	R5973	3E	2E	R6195	5L	3G	U5990D	5H	2G
CR6162	8J	3E	R5980	5E	1F	R6197	5G	3G	U6010A	1D	3A
CR6190	4D	3G	R5981	3C	2F	R6198	4E	3G	U6010B	1E	3A
CR6210	2G	4A	R5982	3C	2F	R6199	5H	3G	U6070	6F	2E
CR6211	1G	4A	R5983	4C	1F	R6221	1C	4B	U6120	1H	4B
			R5984	4E	2F	R6222	2F	4B	U6130	2J	3B
J5990	2S	1G	R5985	4C	2F	R6230	2F	4B	U6140	6N	3C
J5991	2S	1G	R5990	2P	2G	R6231	2G	4B	U6150A	10F	3C
			R5991	5E	2G	R6232	1F	4B	U6150B	9E	3C
L6210	2G	3A	R5992	5E	2G	R6233	2F	4B	U6150C	9D	3C
			R5993	5E	2G	R6245	7N	4C	U6152A	8C	3D
P4221	1S	1F	R6020	1B	2B	R6250	3N	4D	U6152B	8F	3D
P4221	2B	1F	R6021	1B	2B	R6250	9D	4D	U6152C	10F	3D
P4240	6B	1D	R6022	1C	2B	R6251	6L	4D	U6152D	2P	3D
P5990A	3S	1G	R6042	8N	3C	R6260	6H	4E	U6180	7K	3F
			R6050	8H	3D	R6261	7J	3G	U6230	2F	3B
Q5920	1C	2B	R6060	5F	2E	R6262	2C	3G	U6250	3S	4C
Q5921	1B	2B	R6062	1L	2E	R6263	1J	4E	U6252A	9E	4D
Q5980	3E	2F	R6063	2L	2E	R6264	5L	4E	U6252B	8H	4D
Q5981	3D	2F	R6064	6D	3E	R6266	6L	4E	U6290A	4M	4G
Q5982	3F	2F	R6081	6E	2F	R6267	7L	4E	U6290B	4M	4G
Q5983	4D	2F	R6082	3F	2F	R6270	1J	4E	U6290C	3M	4G
Q6090	4F	2G	R6083	3E	2F	R6271	7G	4E	U6290D	3M	4G
Q6091	4H	2G	R6084	2B	2F	R6273	2C	3G			
Q6092	4G	2G	R6085	2C	2F	R6274	7H	4E	X5910	1A	1A
Q6093	4E	2G	R6090	1J	2G	R6275	8H	4E			
Q6190	5L	3G	R6091	2J	3G	R6276A	4L	4F			
Q6191	5L	3G	R6092	7P	3G	R6276B	6K	4F			

Partial A27 also shown on diagram 27.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J59	2S	CHASSIS	P5991	2S	CHASSIS						



2445/2465 OPTION 06 BU Exer F2

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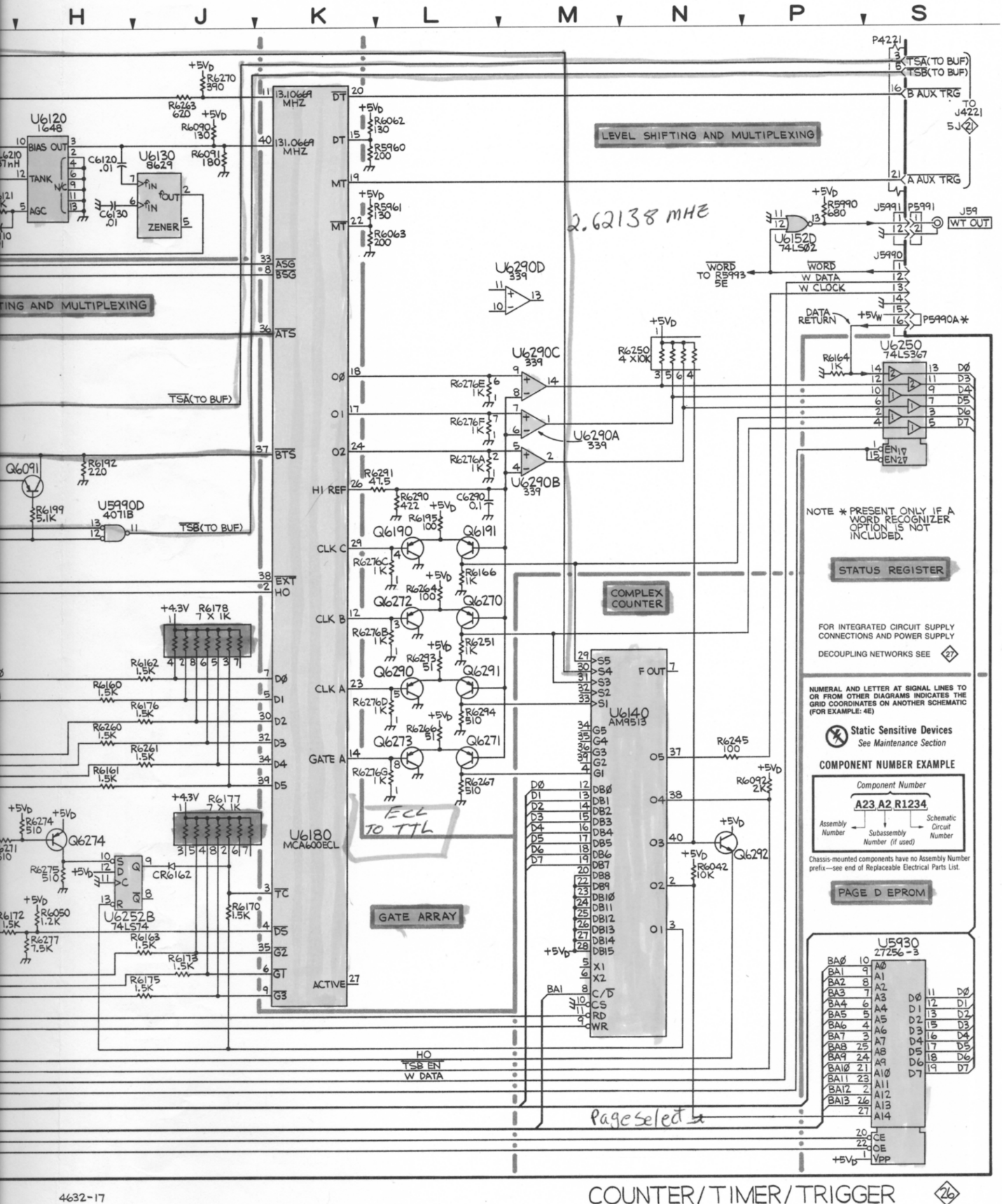
ECL on this Page operates In Positive Levels



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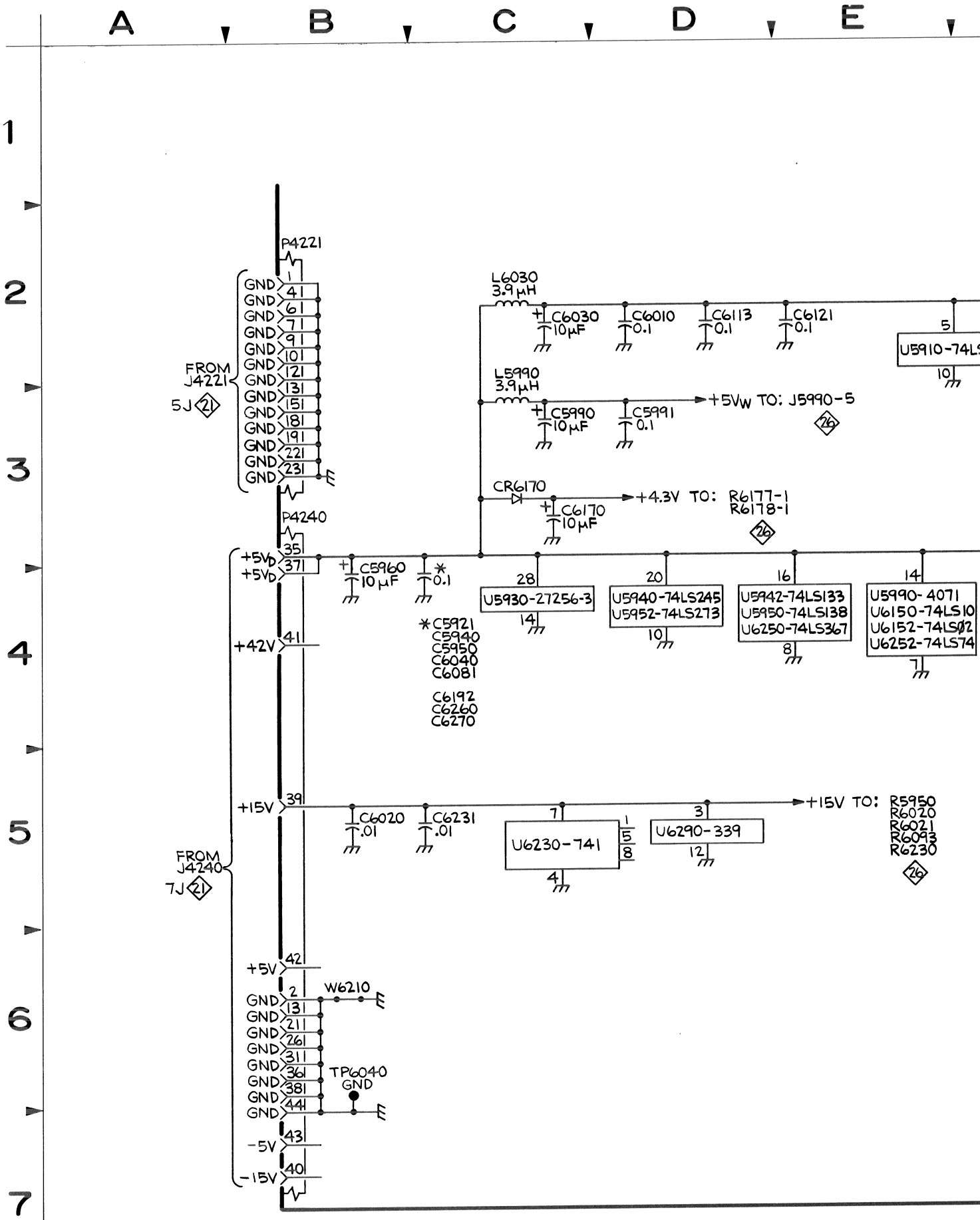
COUNTER/TIMER/TRIGGER 26

POWER DISTRIBUTION 27

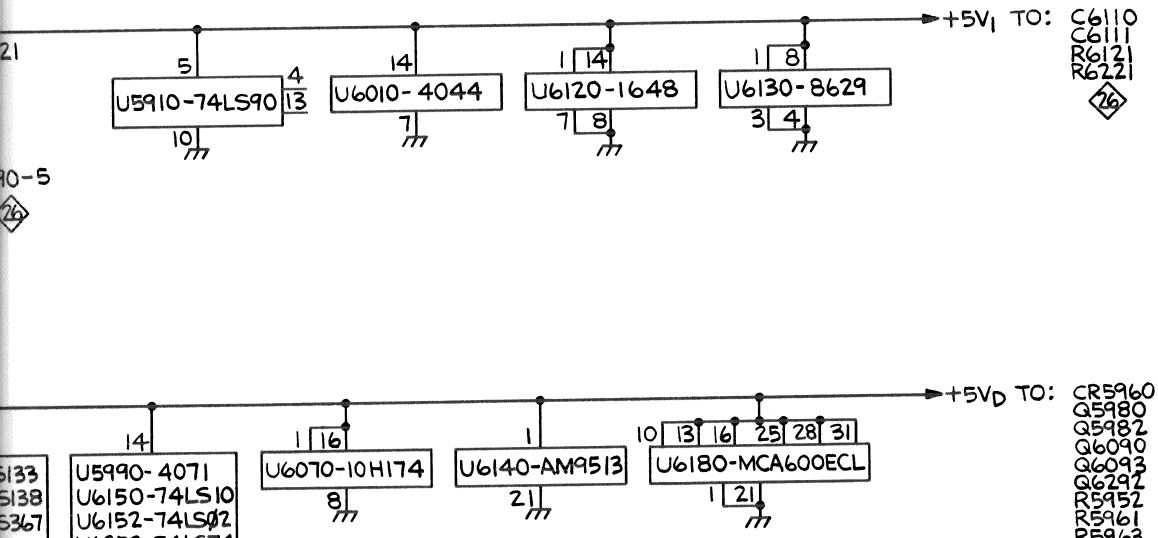
ASSEMBLY A27

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C5921	4C	1B	C6170	3C	3E	TP6040	6B	3C	U6140	4G	3C
C5940	4C	1C	C6192	4C	3G				U6150	4E	3C
C5950	4C	1D	C6231	5C	4B	U5910	2E	2A	U6152	4E	3D
C5960	4B	2E	C6260	4C	4E	U5930	4C	2B	U6180	4G	3F
C5990	3C	1G	C6270	4C	4E	U5940	4D	2C	U6230	5C	3B
C5991	3D	2G				U5942	4D	2C	U6250	4D	4C
C6010	2D	2A	CR6170	3C	3E	U5950	4D	2D	U6252	4E	4D
C6020	5B	2B				U5952	4D	2D	U6290	5D	4G
C6030	2C	3B	L5990	2C	2G	U5990	4E	2G			
C6040	4C	2C	L6030	2C	3B	U6010	2F	3A	W6210	6B	4A
C6081	4C	2F				U6070	4F	2E			
C6113	2D	3A	P4221	2B	1F	U6120	2G	4B			
C6121	2E	3B	P4240	3B	1D	U6130	2H	3B			

Partial A27 also shown on diagram 26.



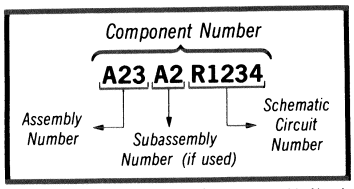
2445/2465 OPTION 06(COUNTER/TIMER/TR



NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

PARTIAL A27 COUNTER/TIMER/TRIGGER BOARD

C/T/T POWER DISTRIBUTION 27

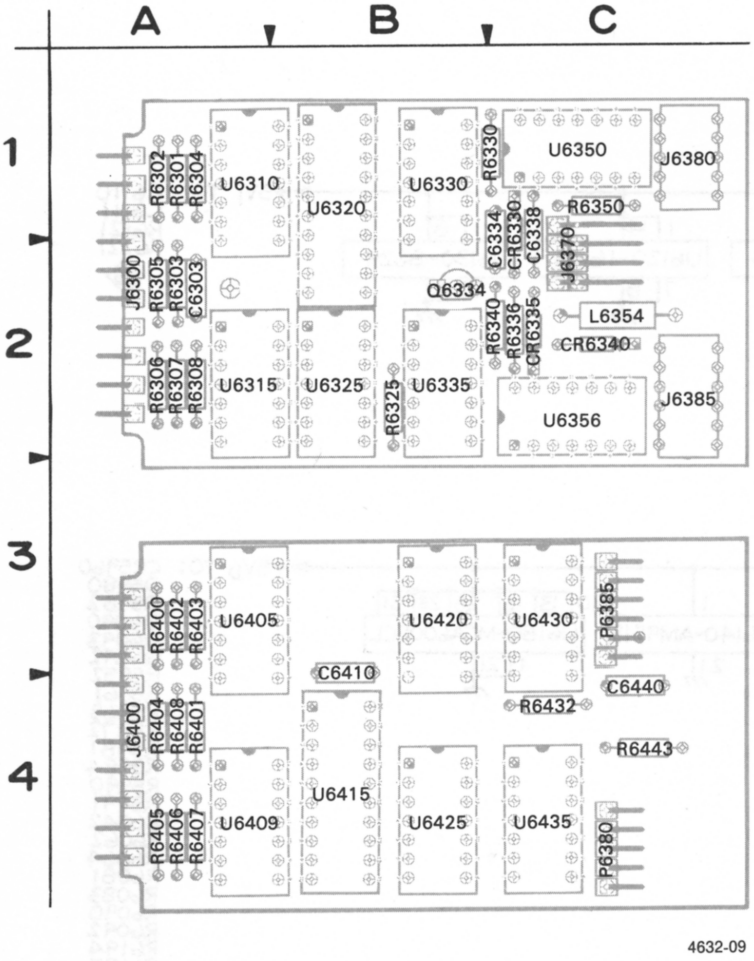
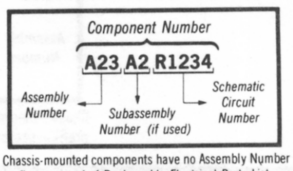


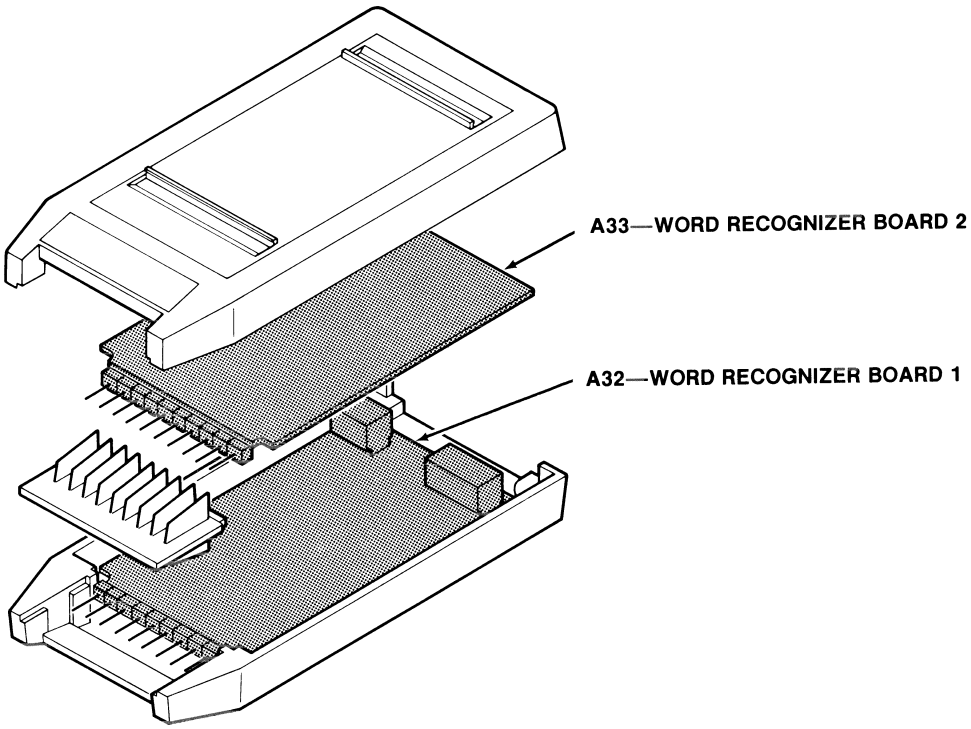
Figure 7-7. A32—Word Recognizer board 1 (top), and A33—Word Recognizer board 2 (bottom).

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A33—WORD RECOGNIZER BOARD 2
A32—WORD RECOGNIZER BOARD 1

A32—WORD RECOGNIZER BOARD 1

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C6303	28	R6301	28	U6310	28	U6330	28
C6334	28	R6302	28	U6310	28	U6335	28
C6338	28	R6303	28	U6310	28	U6335	28
CR6330	28	R6304	28	U6310	28	U6335	28
CR6335	28	R6305	28	U6315	28	U6335	28
CR6340	28	R6306	28	U6315	28	U6335	28
J6300	28	R6307	28	U6315	28	U6350	28
J6370	28	R6308	28	U6315	28	U6350	28
J6380	28	R6325	28	U6315	28	U6350	28
J6380	28	R6330	28	U6320	28	U6356	28
J6385	28	R6336	28	U6320	28	U6356	28
J6385	28	R6340	28	U6325	28	U6356	28
L6354	28	R6350	28	U6325	28	U6356	28
Q6334	28	U6310	28	U6330	28	U6356	28

A33—WORD RECOGNIZER BOARD 2

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C6410	28	R6404	28	U6405	28	U6425	28
C6440	28	R6405	28	U6409	28	U6430	28
J6400	28	R6406	28	U6409	28	U6430	28
P6380	28	R6407	28	U6409	28	U6435	28
P6380	28	R6408	28	U6409	28	U6435	28
P6385	28	R6432	28	U6409	28	U6435	28
P6385	28	R6443	28	U6415	28	U6435	28
R6400	28	U6405	28	U6415	28	U6435	28
R6401	28	U6405	28	U6420	28		
R6402	28	U6405	28	U6420	28		
R6403	28	U6405	28	U6425	28		

WORD RECOGNIZER 28

ASSEMBLY A32

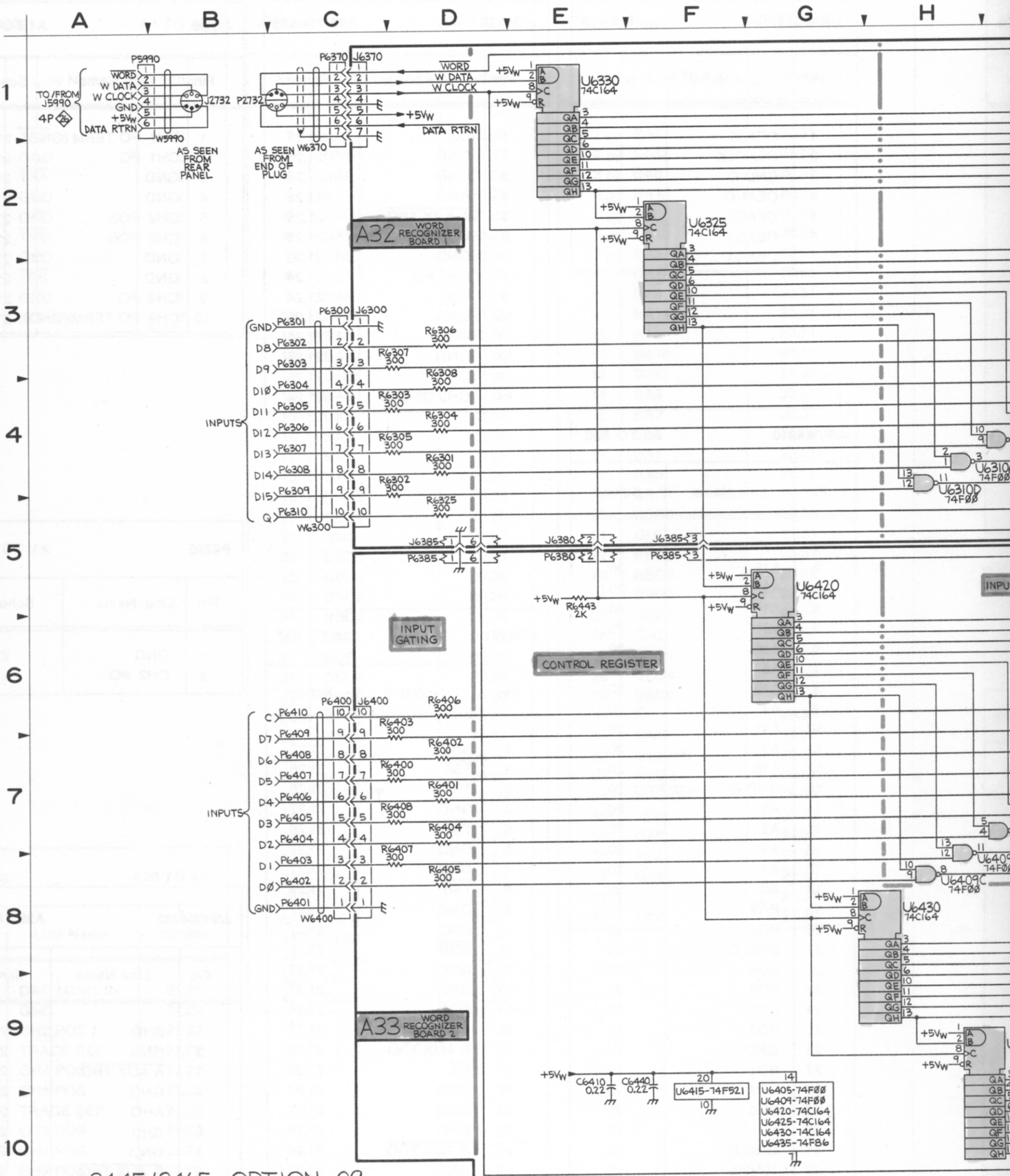
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C6303	1N	2A	Q6334	5S	2B	U6310A	4J	1A	U6335A	3P	2B
C6334	1N	2C				U6310B	4J	1A	U6335B	4N	2B
C6338	3S	2C	R6301	4D	1A	U6310C	4J	1A	U6335C	4M	2B
			R6302	4D	1A	U6310D	5H	1A	U6335D	4M	2B
CR6330	2S	2C	R6303	4D	2A	U6310	1S	1A	U6335	2S	2B
CR6335	3P	2C	R6304	4D	1A	U6315A	3K	2A	U6350A	4P	1C
CR6340	2P	2C	R6305	4D	2A	U6315B	3K	2A	U6350B	3N	1C
			R6306	3D	2A	U6315C	4K	2A	U6350	2S	1C
J6300	3C	2A	R6307	3D	2A	U6315D	4K	2A	U6356A	2S	2C
J6370	1C	2C	R6308	3D	2A	U6315	1S	2A	U6356B	4S	2C
J6380	5E	1C	R6325	5D	2B	U6320	1P	1B	U6356C	4S	2C
J6380	5N	1C	R6330	2S	1C	U6320	3L	1B	U6356D	2P	2C
J6385	5D	2C	R6336	4P	2C	U6325	1S	2B	U6356	2S	2C
J6385	5F	2C	R6340	4S	2C	U6325	2F	2B			
			R6350	2P	1C	U6330	1E	1B			
L6354	2P	2C				U6330	2S	1B			

ASSEMBLY A33

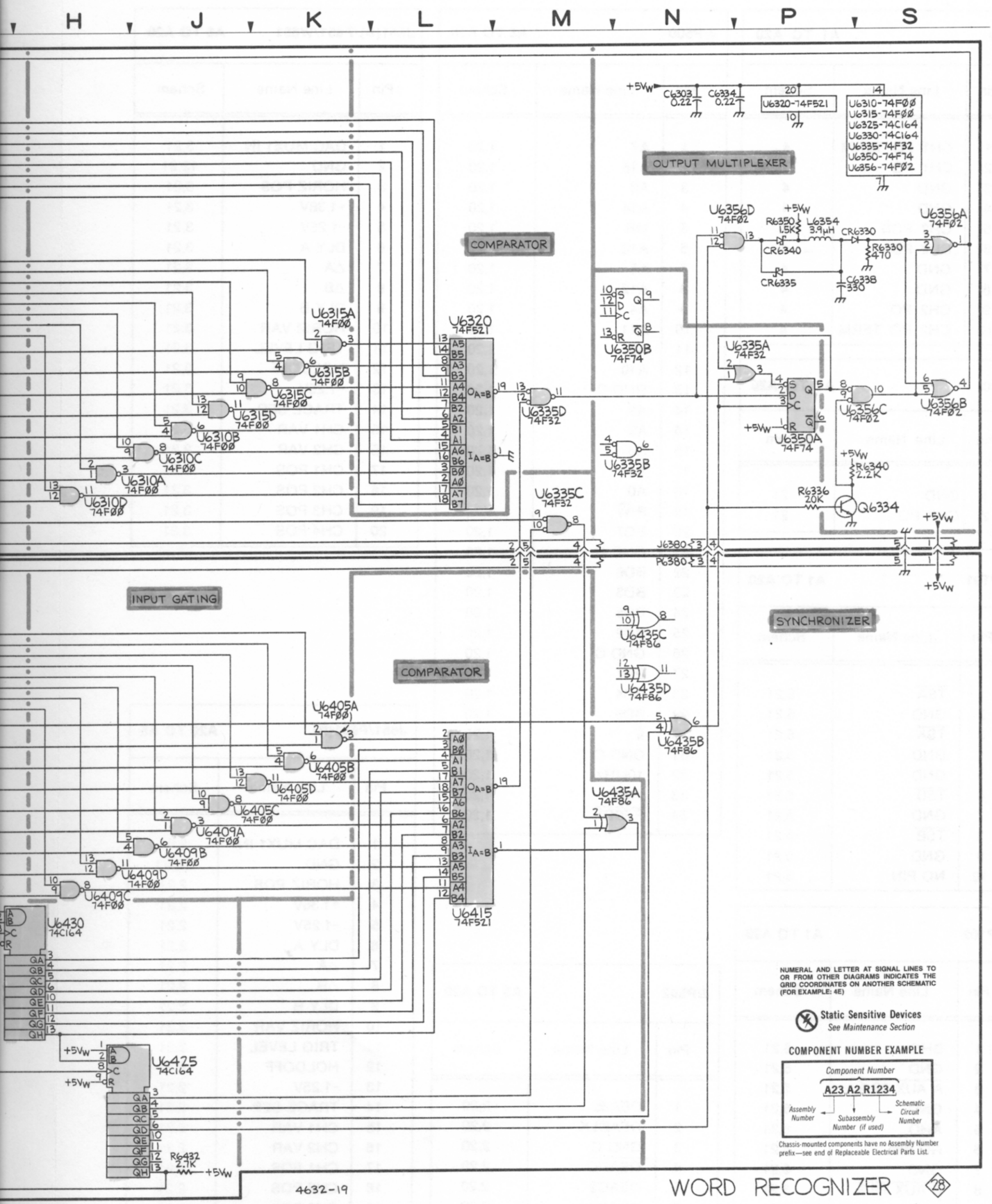
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C6410	9E	3B	R6402	7D	3A	U6405C	7K	3A	U6425	10G	4B
C6440	9F	4C	R6403	6D	3A	U6405D	7K	3A	U6425	9J	4B
			R6404	7D	4A	U6405	10G	3A	U6430	10G	3C
J6400	6C	4A	R6405	8D	4A	U6409A	7J	4A	U6430	8H	3C
			R6406	6D	4A	U6409B	7J	4A	U6435A	7M	4C
P6380	5E	4C	R6407	7D	4A	U6409C	8H	4A	U6435B	7N	4C
P6380	5N	4C	R6408	7D	4A	U6409D	8J	4A	U6435C	6N	4C
P6385	5D	3C	R6432	10J	4C	U6409	10G	4A	U6435D	6N	4C
P6385	5F	3C	R6443	5E	4C	U6415	10F	4B	U6435	10G	4C
						U6415	8L	4B			
R6400	7D	3A	U6405A	6K	3A	U6420	10G	3B			
R6401	7D	4A	U6405B	7K	3A	U6420	5G	3B			

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2732	1B	CHASSIS	P6304	4C	CHASSIS	P6400	6C	CHASSIS	P6408	7C	CHASSIS
			P6305	4C	CHASSIS	P6401	8C	CHASSIS	P6409	7C	CHASSIS
P2732	1B	CHASSIS	P6306	4C	CHASSIS	P6402	8C	CHASSIS	P6410	6C	CHASSIS
P5990	1A	CHASSIS	P6307	4C	CHASSIS	P6403	8C	CHASSIS			
P6300	3C	CHASSIS	P6308	4C	CHASSIS	P6404	7C	CHASSIS	W5990	1B	CHASSIS
P6301	3C	CHASSIS	P6309	4C	CHASSIS	P6405	7C	CHASSIS	W6300	5C	CHASSIS
P6302	3C	CHASSIS	P6310	5C	CHASSIS	P6406	7C	CHASSIS	W6370	2C	CHASSIS
P6303	3C	CHASSIS	P6370	1C	CHASSIS	P6407	7C	CHASSIS	W6400	8C	CHASSIS



2445/2465 OPTION 09



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WORD RECOGNIZER 28

J100 — **A1 TO A20**

Pin	Line Name	Schem
1	CH1 PO TERM	4
2	CH1 PO	4
3	GND	4
4	GND	4
5	CH2 POS	4
6	CH2 POS	4
7	GND	4
8	GND	4
9	CH2 PO	4
10	CH2 PO TERM	4

P100 — **A1 TO A20**

Pin	Line Name	Schem
1	GND	21
2	CH2 PO	21

J/P101 — **A1 TO A20**

Pin	Line Name	Schem
1	$\overline{\text{TSA}}$	5,21
2	GND	5,21
3	$\overline{\text{TSA}}$	5,21
4	GND	5,21
5	GND	5,21
6	$\overline{\text{TSB}}$	5,21
7	GND	5,21
8	$\overline{\text{TSB}}$	5,21
9	GND	5,21
10	NO PIN	5,21

J/P102 — **A1 TO A20**

Pin	Line Name	Schem
1	BHO	5,21
2	GND	5,21
3	$\overline{\text{A AUX TRG}}$	5,21
4	GND	5,21
5	AHO	5,21
6	NO PIN	5,21
7	GND	5,21
8	$\overline{\text{B AUX TRG}}$	5,21
9	GND	5,21
10	$\overline{\text{DS}}$	5,21

J/P500 — **A5 TO A20**

Pin	Line Name	Schem
1	A7	1,20
2	A15	1,20
3	A6	1,20
4	A14	1,20
5	MR	1,20
6	A13	1,20
7	A5	1,20
8	A12	1,20
9	A4	1,20
10	A11	1,20
11	A3	1,20
12	A10	1,20
13	GND C	1,20
14	A9	1,20
15	A2	1,20
16	A8	1,20
17	A1	1,20
18	A0	1,20
19	R/$\overline{\text{W}}$	1,20
20	BD7	1,20
21	GND C	1,20
22	BD6	1,20
23	BD3	1,20
24	BD5	1,20
25	BD2	1,20
26	GND C	1,20
27	BD1	1,20
28	BD4	1,20
29	BD0	1,20
30	$\overline{\text{E}}$	1,20
31	GND C	1,20
32	10MHz	1,20
33	VMA	1,20
34	$\overline{\text{RESET}}$	1,20

J/P502 — **A5 TO A20**

Pin	Line Name	Schem
1	OEA35	2,20
2	OEACLK	2,20
3	GND C	2,20
4	OEAI/O	2,20
5	OEAC2	2,20
6	OEAC3	2,20
7	OEAC1	2,20

J651(B)/P651/W651 — **A6 TO A20**

Pin	Line Name	Schem
1	DAC MUX1 IN	3,21
2	GND	12,21
3	HORIZ POS	3,21
4	+1.36V	3,21
5	-1.25V	3,21
6	DLY A	3,21
7	△A	3,21
8	△B	3,21
9	DLY B	3,21
10	HORIZ VAR	3,21
11	TRIG LEVEL	3,21
12	HOLDOFF	3,21
13	-1.25V	3,21
14	TRACE SEP	3,21
15	CH1 VAR	3,21
16	CH2 VAR	3,21
17	CH1 POS	3,21
18	CH2 POS	3,21
19	CH3 POS	3,21
20	CH4 POS	3,21

J651/P651(B) — **A20 TO A5**

Pin	Line Name	Schem
1	DAC MUX1 IN	2,21
2	GND	12,21
3	HORIZ POS	2,21
4	+1.36V	2,21
5	-1.25V	2,21
6	DLY A	2,21
7	△A	2,21
8	△B	2,21
9	DLY B	2,21
10	HORIZ VAR	2,21
11	TRIG LEVEL	2,21
12	HOLDOFF	2,21
13	-1.25V	2,21
14	TRACE SEP	2,21
15	CH1 VAR	2,21
16	CH2 VAR	2,21
17	CH1 POS	2,21
18	CH2 POS	2,21
19	CH3 POS	2,21
20	CH4 POS	2,21

J/P/W4207		A5 TO A20
Pin	Line Name	Schem
1	OEA35	20
2	OEACLK	20
3	GND C	20
4	OEAI/O	20
5	OEAC2	20
6	OEAC3	20
7	OEAC1	20

J/P4220		A20 TO A25
Pin	Line Name	Schem
1	$\overline{DS}$	21,25
2	GND	21,25
3	GND	21,25
4	AHO	21,25
5	$\overline{A\ AUX\ TRG}$	21,25
6	GND	21,25
7	GND	21,25
8	CH2 PO	21,24
9	SSA	21,24
10	GND	21,25
11	GND	21,25
12	GND	21,25
13	GND	21,25
14	CH2 OFFSET	21,24

J4230		A1 TO A20
Pin	Line Name	Schem
1	CH1 PO TERM (GND)	21
2	CH1 PO	21
3	GND	21
4	GND	21
5	CH2 POS	21
6	CH2 POS	21
7	GND	21
8	GND	21
9	CH2 PO	21
10	CH2 PO TERM (GND)	21

J/P/W4210		A5 TO A20
Pin	Line Name	Schem
1	A7	20
2	A15	20
3	A6	20
4	A14	20
5	MR	20
6	A13	20
7	A5	20
8	A12	20
9	A4	20
10	A11	20
11	A3	20
12	A10	20
13	GND C	20
14	A9	20
15	A2	20
16	A8	20
17	A1	20
18	A0	20
19	R/$\overline{W}$	20
20	BD7	20
21	GND C	20
22	BD6	20
23	BD3	20
24	BD5	20
25	BD2	20
26	GND C	20
27	BD1	20
28	BD4	20
29	BD0	20
30	$\overline{E}$	20
31	GND C	20
32	10MHz	20
33	VMA	20
34	$\overline{RESET}$	20

P4230		A1 TO A20
Pin	Line Name	Schem
1	GND	21
2	CH2 PO	21

J/P4221		A20 TO A27
Pin	Line Name	Schem
1	GND	21,27
2	$\overline{TSA}$	21,26
3	$\overline{TSA}$	21,26
4	GND	21,27
5	$\overline{TSB}$	21,26
6	GND	21,27
7	GND	21,27
8	$\overline{TSB}$	21,26
9	GND	21,27
10	GND	21,27
11	$\overline{SGB}$	21,26
12	GND	21,27
13	GND	21,27
14	$\overline{SGA}$	21,26
15	GND	21,27
16	$\overline{B\ AUX\ TRG}$	21,26
17	$\overline{DS}$	21,26
18	GND	21,27
19	GND	21,27
20	AHO	21,26
21	$\overline{A\ AUX\ TRG}$	21,26
22	GND	21,27
23	GND	21,27
24	BHO	21,26

J/P/W4232		A20 TO A1
Pin	Line Name	Schem
1	BHO	21
2	GND	21
3	$\overline{A\ AUX\ TRG}$	21
4	GND	21
5	AHO	21
6	GND	21
7	GND	21
8	$\overline{B\ AUX\ TRG}$	21
9	GND	21
10	$\overline{DS}$	21

J/P/W4236		A1 TO A20
Pin	Line Name	Schem
1	$\overline{\text{TSA}}$	21
2	GND	21
3	$\overline{\text{TSA}}$	21
4	GND	21
5	GND	21
6	$\overline{\text{TSB}}$	21
7	GND	21
8	$\overline{\text{TSB}}$	21
9	GND	21
10	NO PIN	21

J/P4238		A20 TO A23
Pin	Line Name	Schem
1	DAC MUX1 IN	21,22
2	GND	21,22
3	CH2 POS	21,22
4	TRACE SEP	21,22
5	CH4 POS	21,22
6	CH1 POS	21,22
7	TRACE SEP	21,22
8	CH3 POS	21,22
9	CH1 POS	21,22
10	CH2 POS	21,22
11	CH3 POS	21,22
12	CH4 POS	21,22

J/P4240		A20 TO A27
Pin	Line Name	Schem
1	BA7	20,26
2	GND	21,27
3	BA6	20,26
4	BA14	20,26
5	MR	20,26
6	BA13	20,26
7	BA5	20,26
8	BA12	20,26
9	BA4	20,26
10	BA11	20,26
11	BA3	20,26
12	BA10	20,26
13	GND	21,27
14	BA9	20,26
15	BA2	20,26
16	BA8	20,26
17	BA1	20,26
18	BA0	20,26
19	BR/$\overline{\text{W}}$	20,26
20	BBD7	20,26
21	GND	21,27
22	BBD6	20,26
23	BBD3	20,26
24	BBD5	20,26
25	BBD2	20,26
26	GND	21,27
27	BBD1	20,26
28	BBD4	20,26
29	BBD0	20,26
30	$\overline{\text{E}}$	20,26
31	GND	21,27
32	B10MHz	20,26
33	BVMA	20,26
34	$\overline{\text{BRESET}}$	20,26
35	$+5V_D$	21,27
36	GND	21,27
37	$+5V_D$	21,27
38	GND	21,27
39	+15V	21,27
40	−15V	21,27
41	+42V	21,27
42	+5V	21,27
43	−5V	21,27
44	GND	21,27

J/P/W4241		A20 TO A29
Pin	Line Name	Schem
1	BA7	20,31
2	GND	21,33
3	BA6	20,31
4	BA14	20,31
5	MR	20,31
6	BA13	20,31
7	BA5	20,31
8	BA12	20,31
9	BA4	20,31
10	BA11	20,31
11	BA3	20,31
12	BA10	20,31
13	GND	21,33
14	BA9	20,31
15	BA2	20,31
16	BA8	20,31
17	BA1	20,31
18	BA0	20,31
19	BR/$\overline{\text{W}}$	20,31
20	BBD7	20,31
21	GND	21,33
22	BBD6	20,31
23	BBD3	20,31
24	BBD5	20,31
25	BBD2	20,31
26	GND	21,33
27	BBD1	20,31
28	BBD4	20,31
29	BBD0	20,31
30	$\overline{\text{E}}$	20,31
31	GND	21,33
32	B10MHz	20,31
33	BVMA	20,31
34	$\overline{\text{BRESET}}$	20,31
35	$+5V_D$	21,33
36	GND	21,33
37	$+5V_D$	21,33
38	GND	21,33
39	+15V	21,33
40	−15V	21,33

J/P4242		A20 TO A25
Pin	Line Name	Schem
1	BA7	20,25
2	GND	21,25
3	BA6	20,25
4	BA14	20,25
5	MR	20,25
6	BA13	20,25
7	BA5	20,25
8	BA12	20,25
9	BA4	20,25
10	BA11	20,25
11	BA3	20,25
12	BA10	20,25
13	GND	21,25
14	BA9	20,25
15	BA2	20,25
16	BA8	20,25
17	BA1	20,25
18	BA0	20,25
19	BR/$\overline{W}$	20,25
20	BBD7	20,25
21	GND	21,25
22	BBD6	20,25
23	BBD3	20,25
24	BBD5	20,25
25	BBD2	20,25
26	GND	21,25
27	BBD1	20,25
28	BBD4	20,25
29	BBD0	20,25
30	$\overline{E}$	20,25
31	GND	21,25
32	B10MHz	20,25
33	BVMA	20,25
34	$\overline{BRESET}$	20,25
35	+5V$_D$	21,25
36	GND	21,25
37	+5V$_D$	21,25
38	GND	21,25
39	+15V	21,25
40	-15V	21,25
41	$\overline{FLD2}$	21,25
42	$\overline{FLD1}$	21,25
43	$\overline{LINES}$	21,25
44	GND	21,25

J/P4243		A20 TO A23
Pin	Line Name	Schem
1	BA7	20,22
2	GND	21,23
3	BA6	20,22
4	BA14	20,22
5	MR	20,22
6	BA13	20,22
7	BA5	20,22
8	BA12	20,22
9	BA4	20,22
10	BA11	20,22
11	BA3	20,22
12	BA10	20,22
13	GND G	21,23
14	BA9	20,22
15	BA2	20,22
16	BA8	20,22
17	BA1	20,22
18	BA0	20,22
19	BR/$\overline{W}$	20,22
20	BBD7	20,22
21	GND G	21,23
22	BBD6	20,22
23	BBD3	20,22
24	BBD5	20,22
25	BBD2	20,22
26	GND G	21,23
27	BBD1	20,22
28	BBD4	20,22
29	BBD0	20,22
30	$\overline{E}$	20,22
31	GND G	21,23
32	B10MHz	20,22
33	BVMA	20,22
34	$\overline{BRESET}$	20,22
35	+5V$_D$	21,23
36	GND G	21,23
37	+5V$_D$	21,23
38	GND G	21,23
39	+15V	21,23
40	-15V	21,23
41	+42V	21,23
42	+5V	21,23
43	-5V	21,23
44	GND	21,23

J/P/W4258		A20 TO A5
Pin	Line Name	Schem
1	DAC MUX1 IN	21
2	GND	21
3	HORIZ POS	21
4	+1.36V	21
5	-1.25V	21
6	DLY A	21
7	△A	21
8	△B	21
9	DLY B	21
10	HORIZ VAR	21
11	TRIG LEVEL	21
12	HOLDOFF	21
13	-1.25V	21
14	TRACE SEP	21
15	CH1 VAR	21
16	CH2 VAR	21
17	CH1 POS	21
18	CH2 POS	21
19	CH3 POS	21
20	CH4 POS	21

J/P4330		A20 TO A30
Pin	Line Name	Schem
1	+5V$_D$	21,32
2	GND	21,32
3	BA1	20,32
4	BA0	20,32
5	$\overline{ROMEN}$	20,32
6	B$\overline{R}$/W	20,32
7	$\overline{BUFEN}$	20,32
8	$\overline{LOWAD}$	20,32
9	BBD0	20,32
10	BBD1	20,32
11	BBD2	20,32
12	BBD3	20,32
13	BBD4	20,32
14	BBD5	20,32
15	BBD6	20,32
16	BBD7	20,32

J/P4800	A2
Pin	L
1	DI
2	DI
3	DI
4	DI
5	DI
6	DI
7	DI
8	DI
9	EO
10	RE
11	DA
12	GN
13	NR
14	GN
15	ND
16	GN
17	IFC
18	GN
19	SR
20	GN
21	AT
22	GN
23	GN
24	GN

J/P4800 A23 TO GPIB CONNECTOR

Pin	Line Name	Schem
1	DIO1	22
2	DIO5	22
3	DIO2	22
4	DIO6	22
5	DIO3	22
6	DIO7	22
7	DIO4	22
8	DIO8	22
9	EOI	22
10	REN	22
11	DAV	22
12	GND G	22
13	NRFD	22
14	GND G	22
15	NDAC	22
16	GND G	22
17	IFC	22
18	GND G	22
19	SRQ	22
20	GND G	22
21	ATN	22
22	GND G	22
23	GND	22
24	GND G	22

J/P5290 A20 TO A29

Pin	Line Name	Schem
1	BA7	31
2	GND	33
3	BA6	31
4	BA14	31
5	MR	31
6	BA13	31
7	BA5	31
8	BA12	31
9	BA4	31
10	BA11	31
11	BA3	31
12	BA10	31
13	GND	33
14	BA9	31
15	BA2	31
16	BA8	31
17	BA1	31
18	BA0	31
19	BR/$\overline{W}$	31
20	BBD7	31
21	GND	33
22	BBD6	31
23	BBD3	31
24	BBD5	31
25	BBD2	31
26	GND	33
27	BBD1	31
28	BBD4	31
29	BBD0	31
30	$\overline{E}$	31
31	GND	33
32	B10MHz	31
33	BVMA	31
34	$\overline{\text{BRESET}}$	31
35	$+5V_D$	33
36	GND	33
37	$+5V_D$	33
38	GND	33
39	+15V	33
40	−15V	33

J/P/W5990 A27 TO WORD RECOGNIZER CONNECTOR

Pin	Line Name	Schem
1	$\overline{\text{WORD}}$	26,28
2	WDATA	26,28
3	WCLOCK	26,28
4	GND	26,28
5	$+5V_W$	26,28
6	DATA RETURN	26,28

J/P/W6370 WORD RECOGNIZER CONNECTOR TO A32

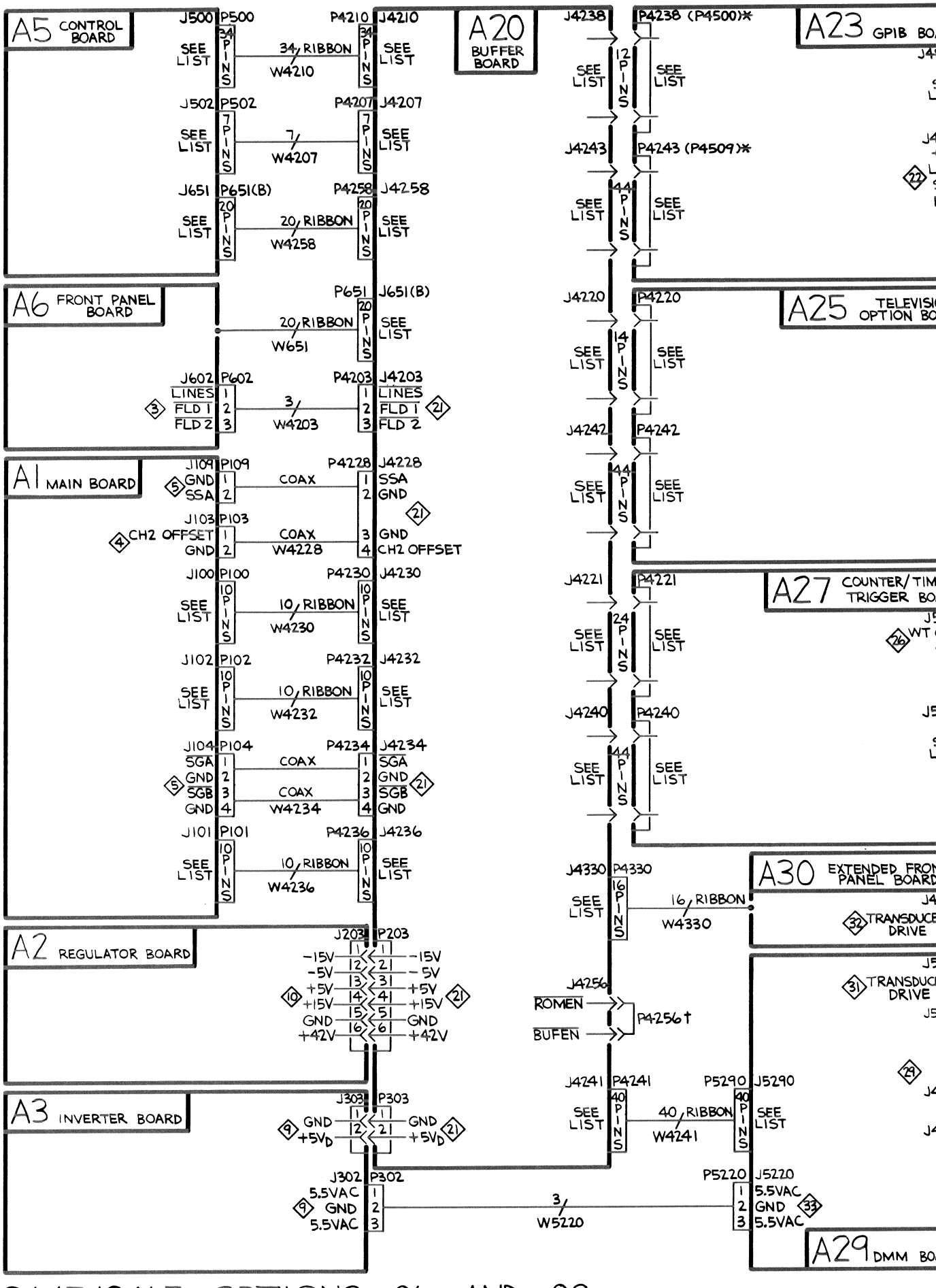
Pin	Line Name	Schem
1	$\overline{\text{WORD}}$	28
2	WDATA	28
3	WCLOCK	28
4	GND	28
5	$+5V_W$	28
6	DATA RETURN	28
7	GND	28

J/P6380 A32 TO A33

Pin	Line Name	Schem
1	$+5V_W$	28
2	WCLOCK	28
3	SYNCH	28
4	GATED CLOCK	28
5	GND	28

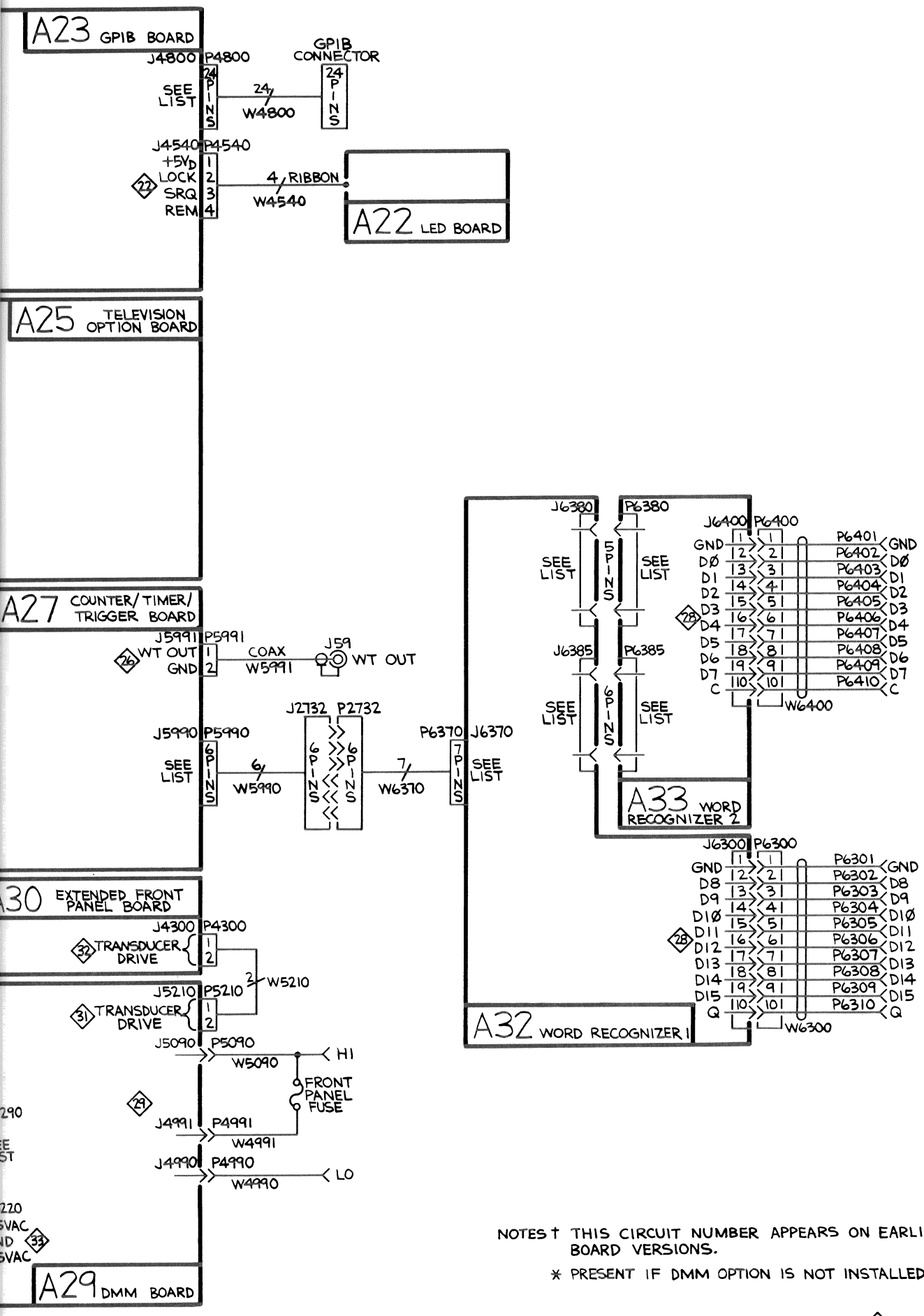
J/P6385 A32 TO A33

Pin	Line Name	Schem
1	GND	28
2	$\overline{\text{LOW BYTE EQUAL}}$	28
3	SERIAL DATA	28
4	GATED Q	28
5	Q DONT CARE	28
6	DATA RETURN	28



2445/2465 OPTIONS 06 AND 09

4632-20

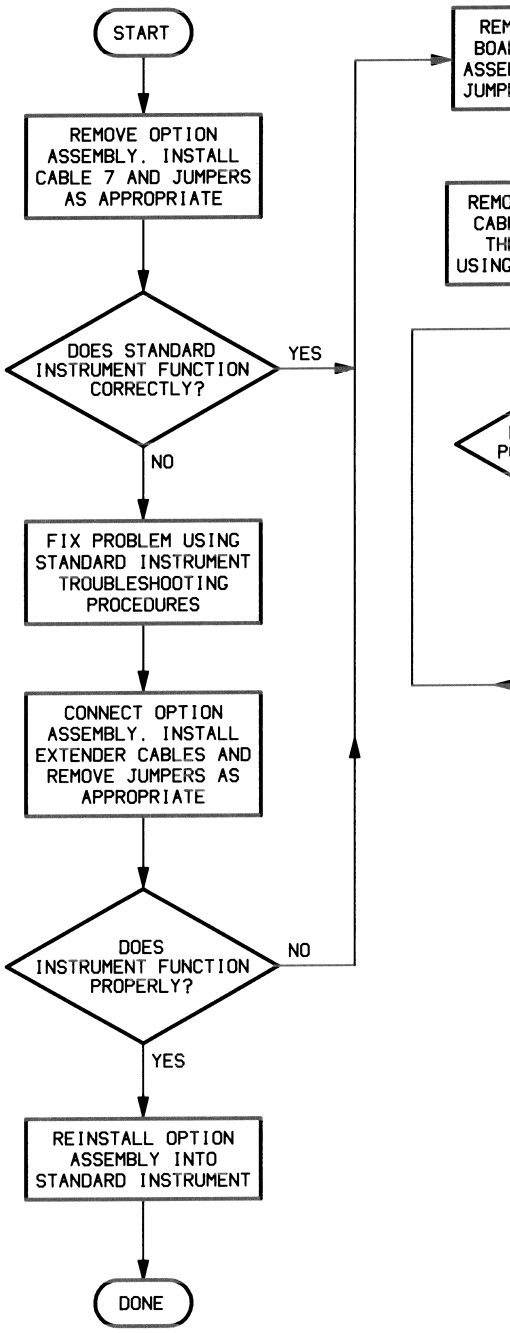


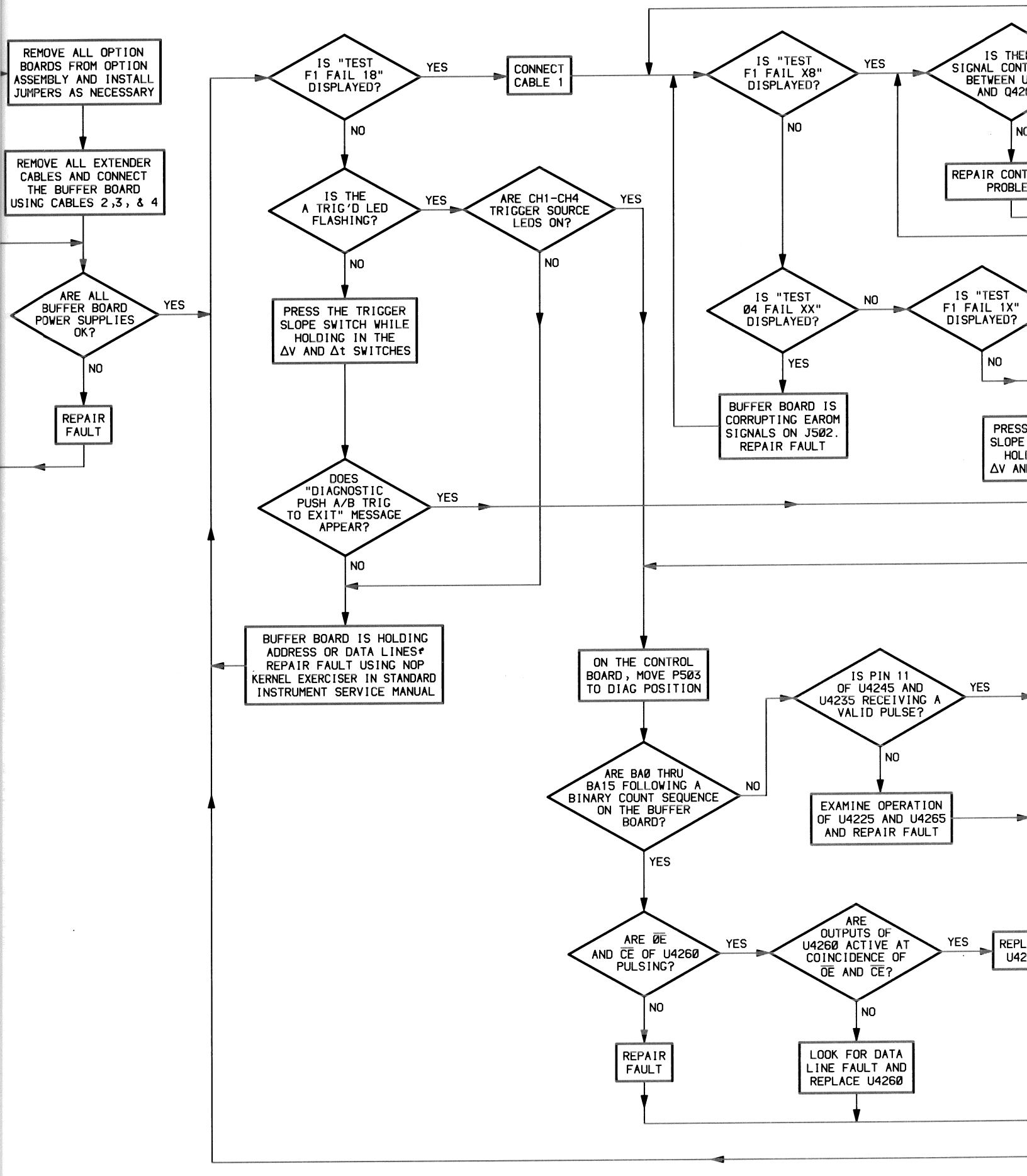
NOTES † THIS CIRCUIT NUMBER APPEARS ON EARLIER BOARD VERSIONS.

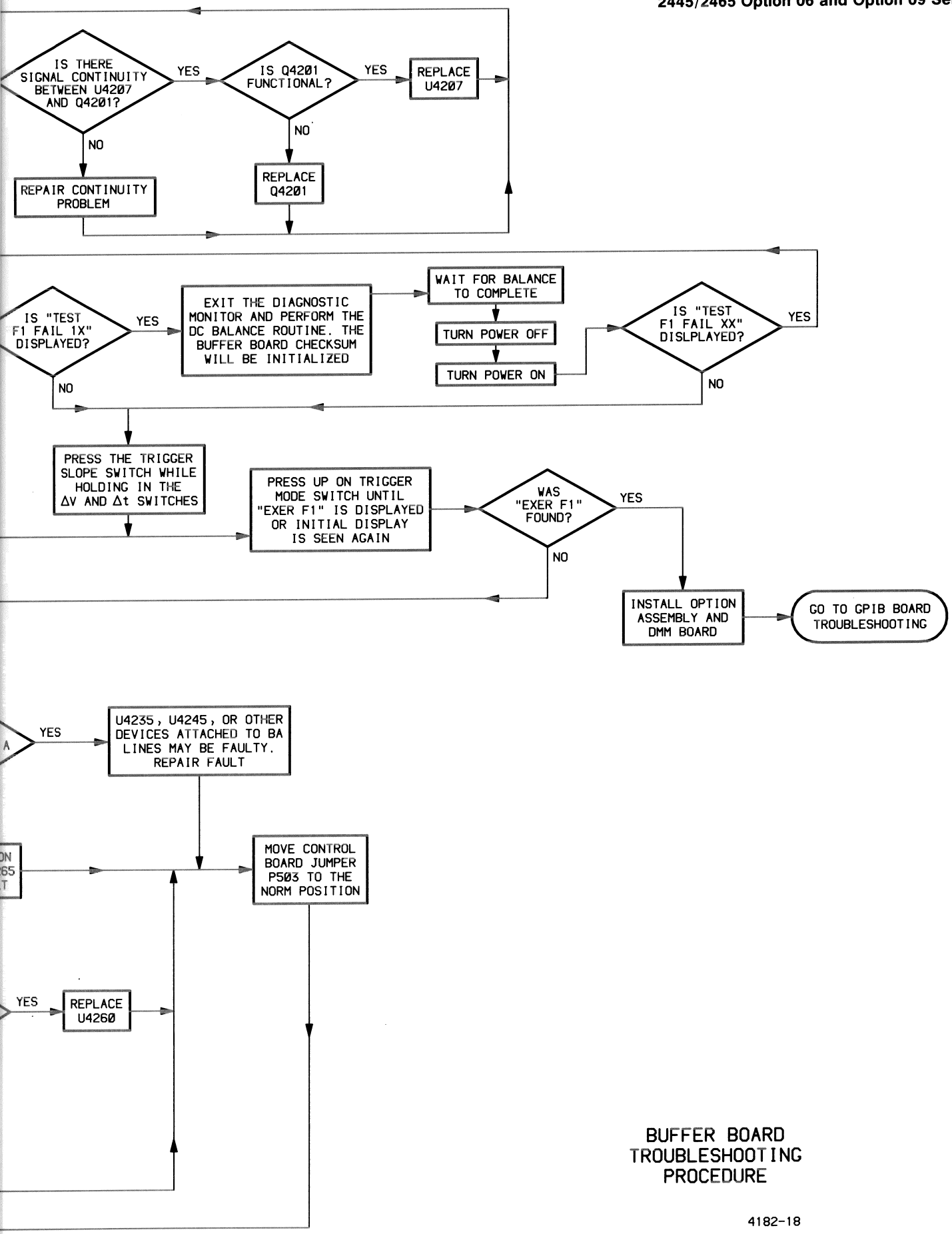
* PRESENT IF DMM OPTION IS NOT INSTALLED.

4632-20

INTERCONNECTION DIAGRAM 34

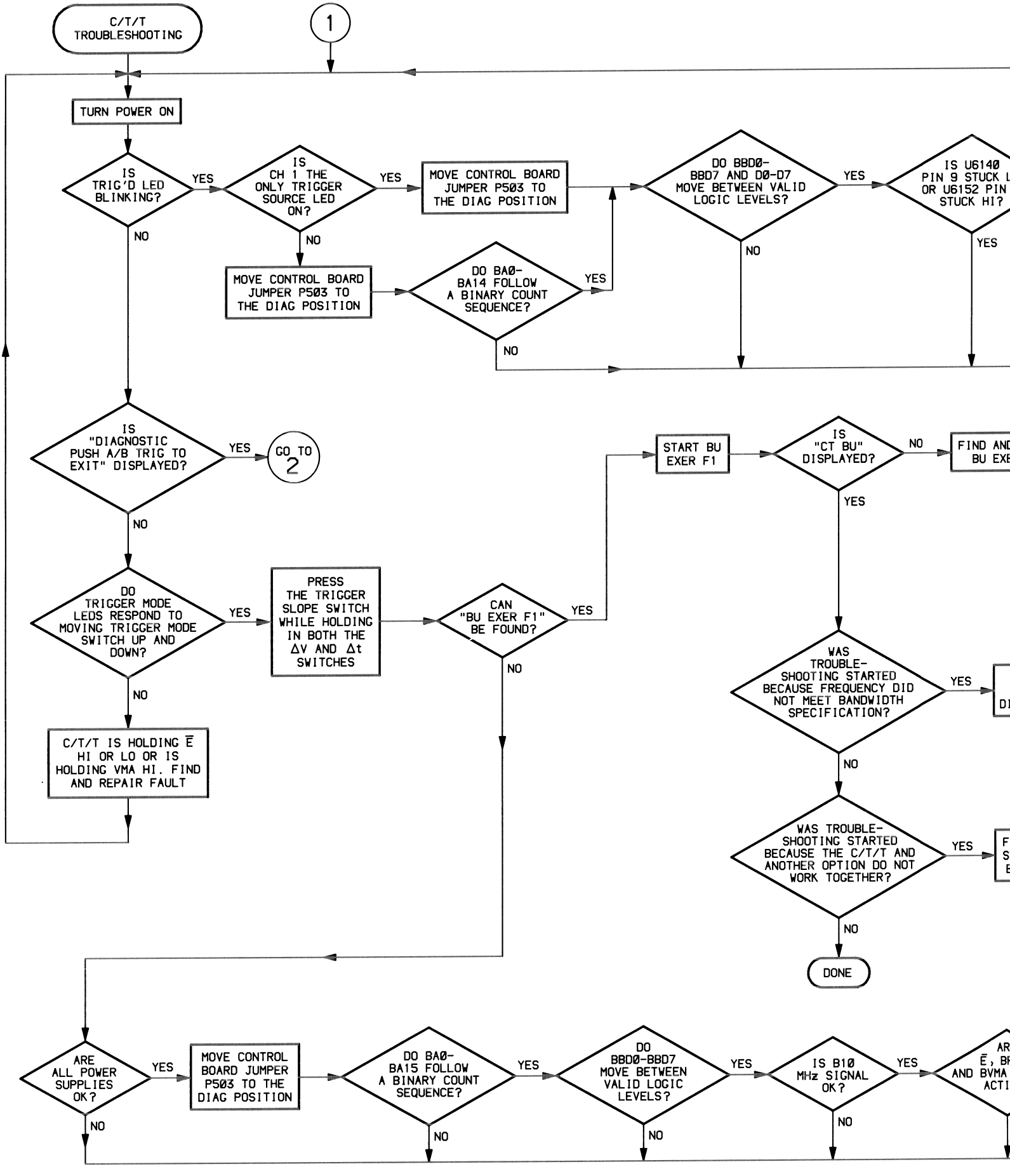

START
REMOVE OPTION ASSEMBLY. INSTALL CABLE 7 AND JUMPERS AS APPROPRIATE
DOES STANDARD INSTRUMENT FUNCTION CORRECTLY?
YES
NO
FIX PROBLEM USING STANDARD INSTRUMENT TROUBLESHOOTING PROCEDURES
CONNECT OPTION ASSEMBLY. INSTALL EXTENDER CABLES AND REMOVE JUMPERS AS APPROPRIATE
DOES INSTRUMENT FUNCTION PROPERLY?
NO
YES
REINSTALL OPTION ASSEMBLY INTO STANDARD INSTRUMENT
DONE

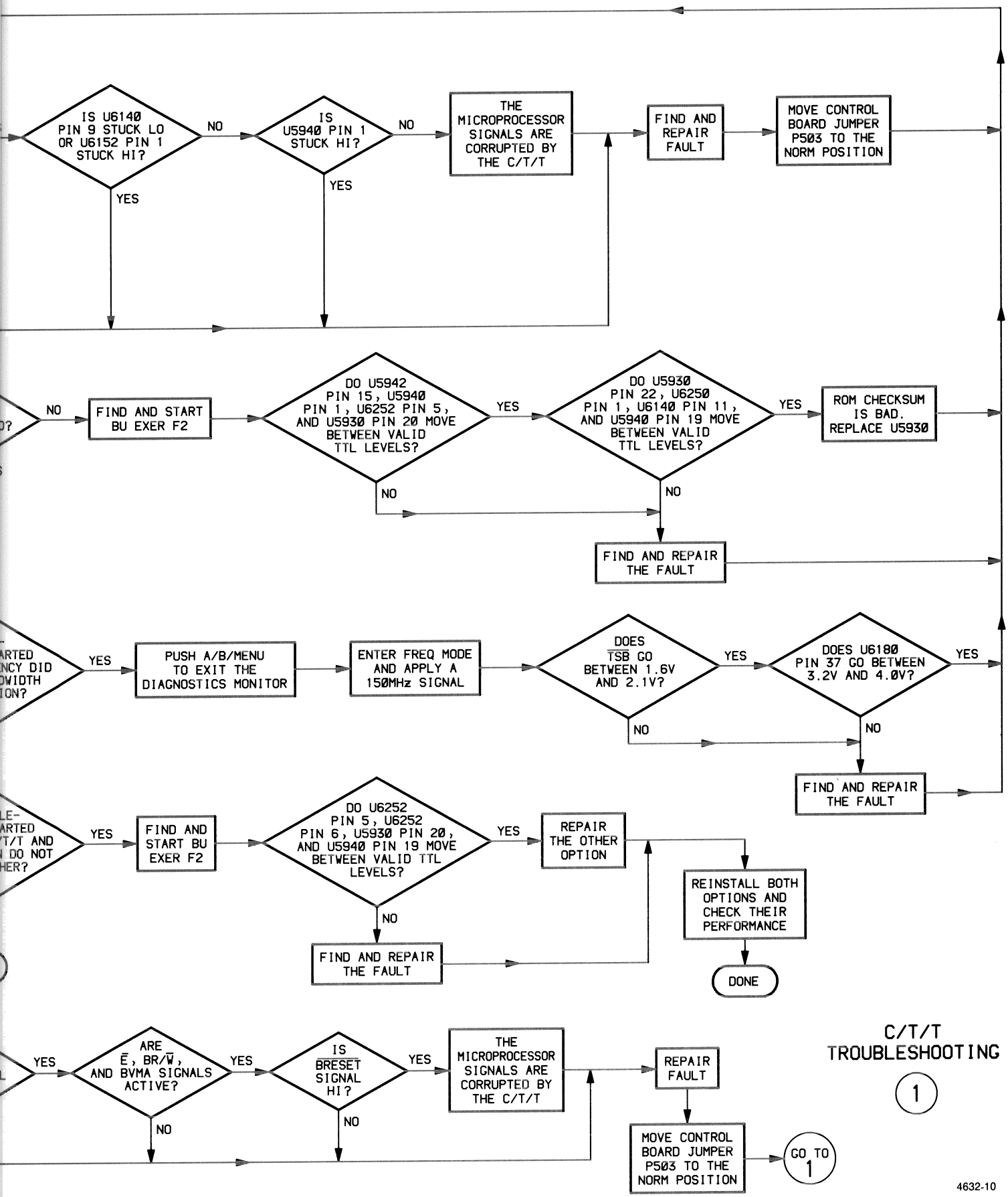

REMOVE ALL OPTION BOARDS FROM OPTION ASSEMBLY AND INSTALL JUMPERS AS NECESSARY
REMOVE ALL EXTENDER CABLES AND CONNECT THE BUFFER BOARD USING CABLES 2,3, & 4
ARE ALL BUFFER BOARD POWER SUPPLIES OK?
YES
NO
REPAIR FAULT
IS "TEST F1 FAIL 18" DISPLAYED?
YES
NO
CONNECT CABLE 1
IS THE A TRIG'D LED FLASHING?
YES
NO
ARE CH1-CH4 TRIGGER SOURCE LEDS ON?
YES
NO
PRESS THE TRIGGER SLOPE SWITCH WHILE HOLDING IN THE ΔV AND Δt SWITCHES
DOES "DIAGNOSTIC PUSH A/B TRIG TO EXIT" MESSAGE APPEAR?
YES
NO
BUFFER BOARD IS HOLDING ADDRESS OR DATA LINES. REPAIR FAULT USING NOP KERNEL EXERCISER IN STANDARD INSTRUMENT SERVICE MANUAL
IS "TEST F1 FAIL X8" DISPLAYED?
YES
NO
IS "TEST 04 FAIL XX" DISPLAYED?
NO
YES
IS "TEST F1 FAIL 1X" DISPLAYED?
NO
BUFFER BOARD IS CORRUPTING EAROM SIGNALS ON J502. REPAIR FAULT
ON THE CONTROL BOARD, MOVE P503 TO DIAG POSITION
ARE BA0 THRU BA15 FOLLOWING A BINARY COUNT SEQUENCE ON THE BUFFER BOARD?
NO
YES
IS PIN 11 OF U4245 AND U4235 RECEIVING A VALID PULSE?
YES
NO
EXAMINE OPERATION OF U4225 AND U4265 AND REPAIR FAULT
ARE $\overline{OE}$ AND $\overline{CE}$ OF U4260 PULSING?
YES
NO
REPAIR FAULT
ARE OUTPUTS OF U4260 ACTIVE AT COINCIDENCE OF $\overline{OE}$ AND $\overline{CE}$?
YES
NO
LOOK FOR DATA LINE FAULT AND REPLACE U4260



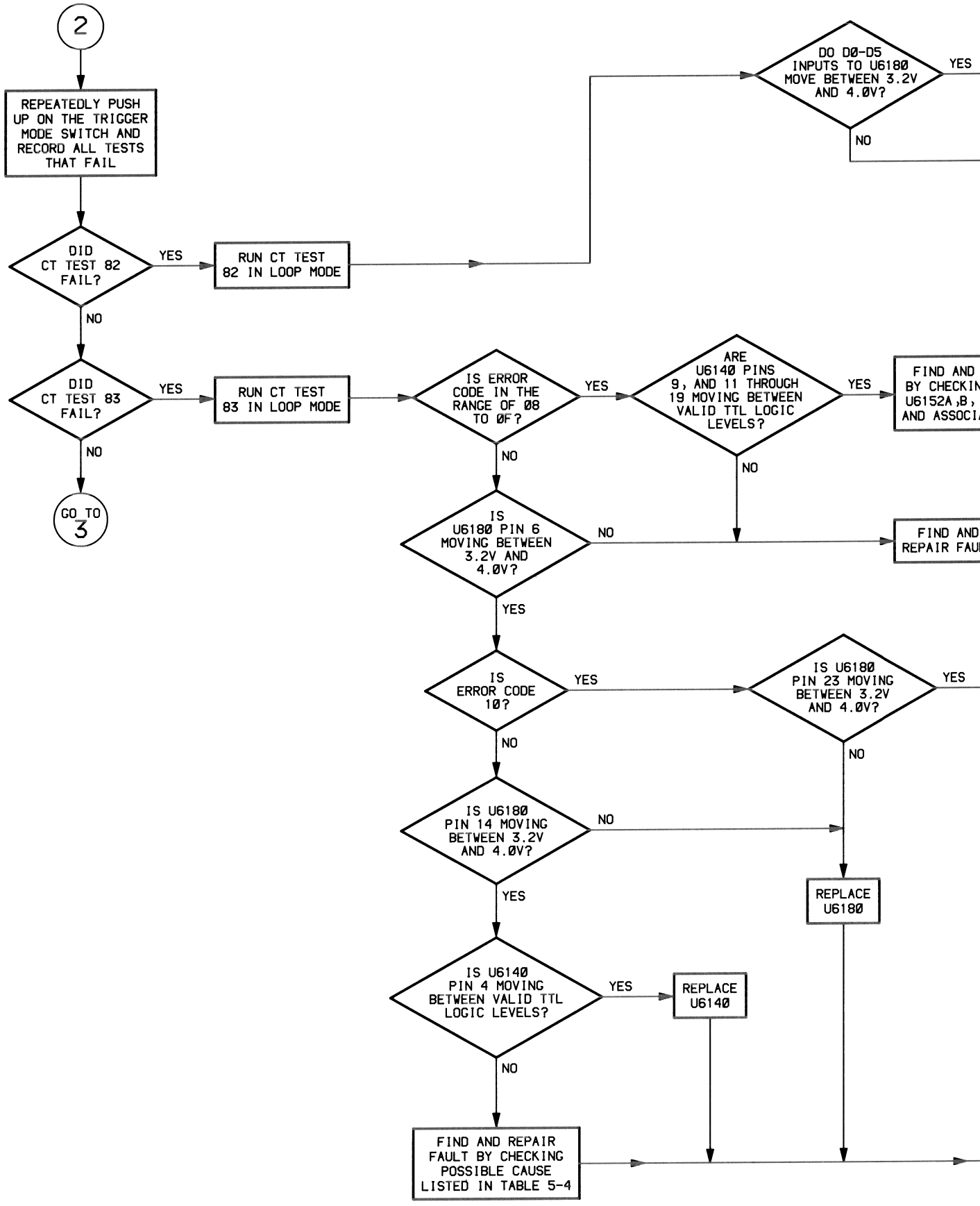
BUFFER BOARD TROUBLESHOOTING PROCEDURE

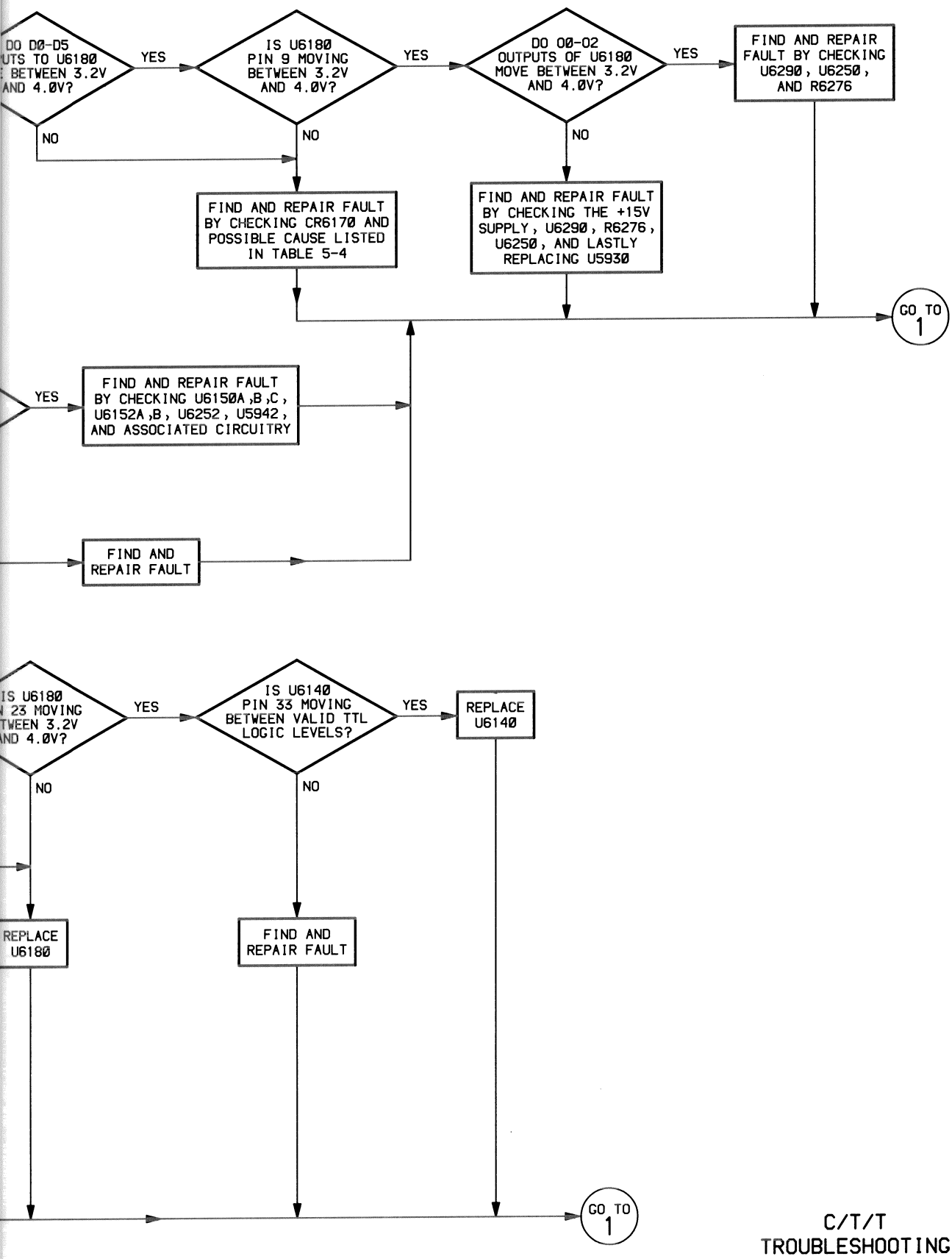
4182-18


C/T/T TROUBLESHOOTING
1
TURN POWER ON
IS TRIG'D LED BLINKING?
YES
IS CH 1 THE ONLY TRIGGER SOURCE LED ON?
YES
MOVE CONTROL BOARD JUMPER P503 TO THE DIAG POSITION
DO BBD0-BBD7 AND D0-D7 MOVE BETWEEN VALID LOGIC LEVELS?
YES
IS U6140 PIN 9 STUCK L OR U6152 PIN STUCK HI?
YES
NO
NO
MOVE CONTROL BOARD JUMPER P503 TO THE DIAG POSITION
DO BA0-BA14 FOLLOW A BINARY COUNT SEQUENCE?
YES
NO
IS "DIAGNOSTIC PUSH A/B TRIG TO EXIT" DISPLAYED?
YES
GO TO 2
NO
DO TRIGGER MODE LEDS RESPOND TO MOVING TRIGGER MODE SWITCH UP AND DOWN?
YES
PRESS THE TRIGGER SLOPE SWITCH WHILE HOLDING IN BOTH THE ΔV AND Δt SWITCHES
CAN "BU EXER F1" BE FOUND?
YES
START BU EXER F1
IS "CT BU" DISPLAYED?
NO
FIND AND BU EXE
YES
NO
C/T/T IS HOLDING Ē HI OR LO OR IS HOLDING VMA HI. FIND AND REPAIR FAULT
NO
WAS TROUBLE-SHOOTING STARTED BECAUSE FREQUENCY DID NOT MEET BANDWIDTH SPECIFICATION?
YES
DI
NO
WAS TROUBLE-SHOOTING STARTED BECAUSE THE C/T/T AND ANOTHER OPTION DO NOT WORK TOGETHER?
YES
F S E
NO
DONE
ARE ALL POWER SUPPLIES OK?
YES
NO
MOVE CONTROL BOARD JUMPER P503 TO THE DIAG POSITION
DO BA0-BA15 FOLLOW A BINARY COUNT SEQUENCE?
YES
NO
DO BBD0-BBD7 MOVE BETWEEN VALID LOGIC LEVELS?
YES
NO
IS B10 MHz SIGNAL OK?
YES
NO
AR Ē, BF AND BVMA ACTI


IS U6140 PIN 9 STUCK LO OR U6152 PIN 1 STUCK HI?
NO
YES
IS U5940 PIN 1 STUCK HI?
NO
YES
THE MICROPROCESSOR SIGNALS ARE CORRUPTED BY THE C/T/T
FIND AND REPAIR FAULT
MOVE CONTROL BOARD JUMPER P503 TO THE NORM POSITION
NO
FIND AND START BU EXER F2
DO U5942 PIN 15, U5940 PIN 1, U6252 PIN 5, AND U5930 PIN 20 MOVE BETWEEN VALID TTL LEVELS?
YES
DO U5930 PIN 22, U6250 PIN 1, U6140 PIN 11, AND U5940 PIN 19 MOVE BETWEEN VALID TTL LEVELS?
YES
ROM CHECKSUM IS BAD. REPLACE U5930
NO
NO
FIND AND REPAIR THE FAULT
YES
PUSH A/B/MENU TO EXIT THE DIAGNOSTICS MONITOR
ENTER FREQ MODE AND APPLY A 150MHz SIGNAL
DOES TSB GO BETWEEN 1.6V AND 2.1V?
YES
DOES U6180 PIN 37 GO BETWEEN 3.2V AND 4.0V?
YES
NO
NO
FIND AND REPAIR THE FAULT
YES
FIND AND START BU EXER F2
DO U6252 PIN 5, U6252 PIN 6, U5930 PIN 20, AND U5940 PIN 19 MOVE BETWEEN VALID TTL LEVELS?
YES
REPAIR THE OTHER OPTION
NO
FIND AND REPAIR THE FAULT
REINSTALL BOTH OPTIONS AND CHECK THEIR PERFORMANCE
DONE
YES
ARE Ē, BR/W, AND BVMA SIGNALS ACTIVE?
YES
IS BRESET SIGNAL HI?
YES
THE MICROPROCESSOR SIGNALS ARE CORRUPTED BY THE C/T/T
REPAIR FAULT
NO
NO
MOVE CONTROL BOARD JUMPER P503 TO THE NORM POSITION
GO TO 1
C/T/T TROUBLESHOOTING
1

4632-10

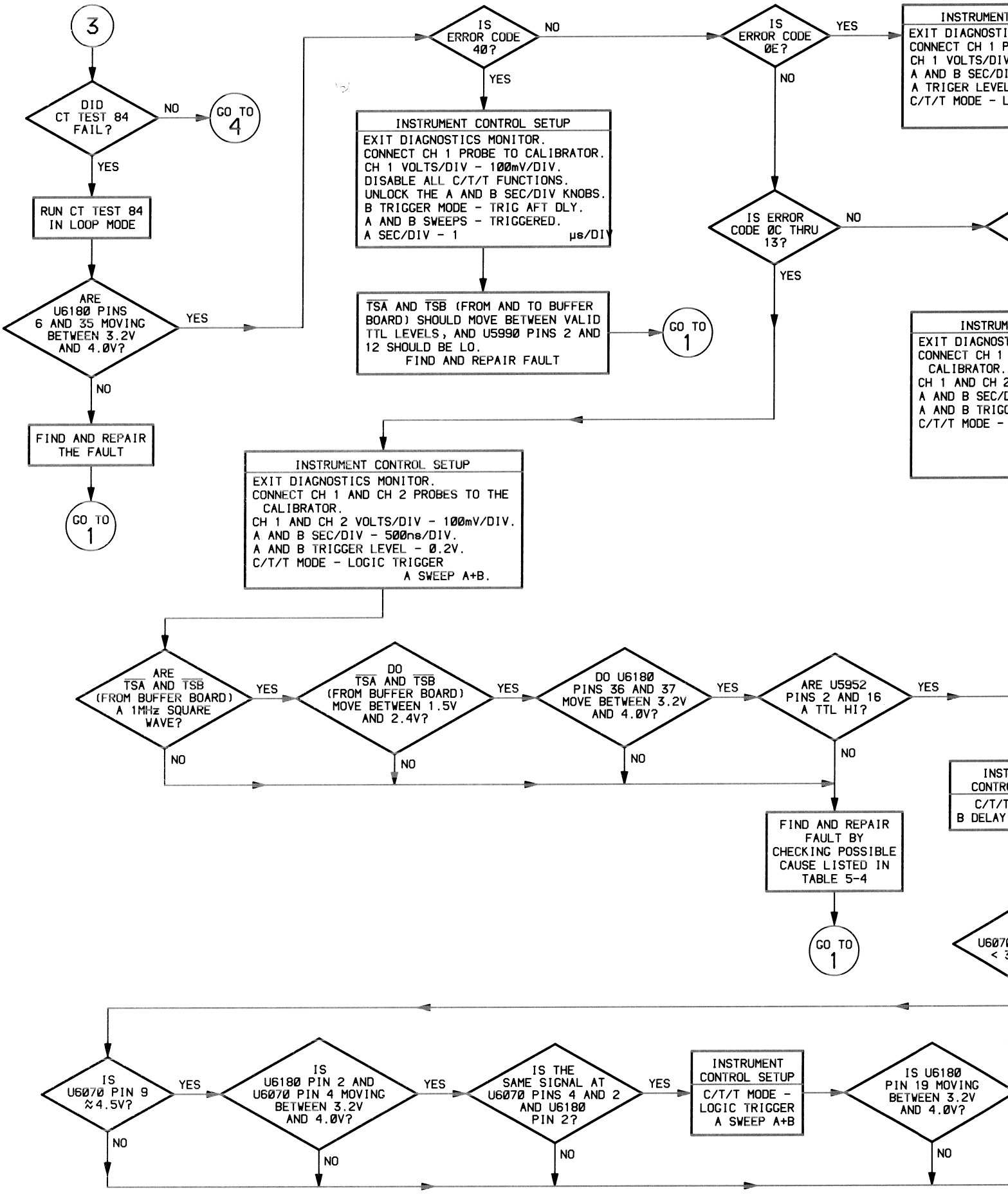

2
REPEATEDLY PUSH UP ON THE TRIGGER MODE SWITCH AND RECORD ALL TESTS THAT FAIL
DID CT TEST 82 FAIL?
YES
RUN CT TEST 82 IN LOOP MODE
NO
DID CT TEST 83 FAIL?
YES
RUN CT TEST 83 IN LOOP MODE
NO
GO TO 3
DO D0-D5 INPUTS TO U6180 MOVE BETWEEN 3.2V AND 4.0V?
YES
NO
IS ERROR CODE IN THE RANGE OF 08 TO 0F?
YES
ARE U6140 PINS 9, AND 11 THROUGH 19 MOVING BETWEEN VALID TTL LOGIC LEVELS?
YES
FIND AND
BY CHECKIN
U6152A,B,
AND ASSOCI
NO
NO
IS U6180 PIN 6 MOVING BETWEEN 3.2V AND 4.0V?
NO
FIND AND
REPAIR FAU
YES
IS ERROR CODE 10?
YES
IS U6180 PIN 23 MOVING BETWEEN 3.2V AND 4.0V?
YES
NO
NO
IS U6180 PIN 14 MOVING BETWEEN 3.2V AND 4.0V?
NO
REPLACE U6180
YES
IS U6140 PIN 4 MOVING BETWEEN VALID TTL LOGIC LEVELS?
YES
REPLACE U6140
NO
FIND AND REPAIR FAULT BY CHECKING POSSIBLE CAUSE LISTED IN TABLE 5-4

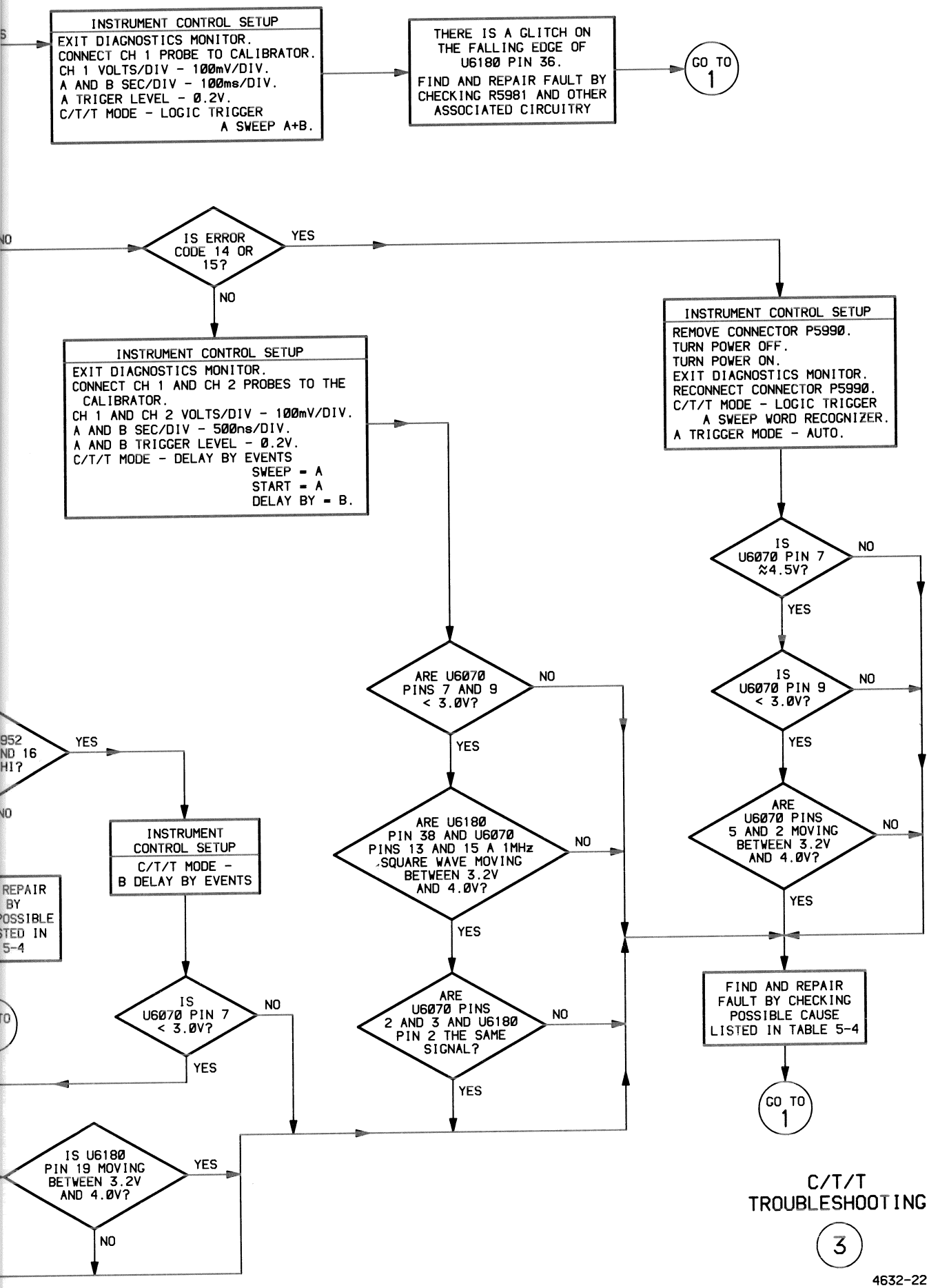


C/T/T TROUBLESHOOTING

2

4632-21

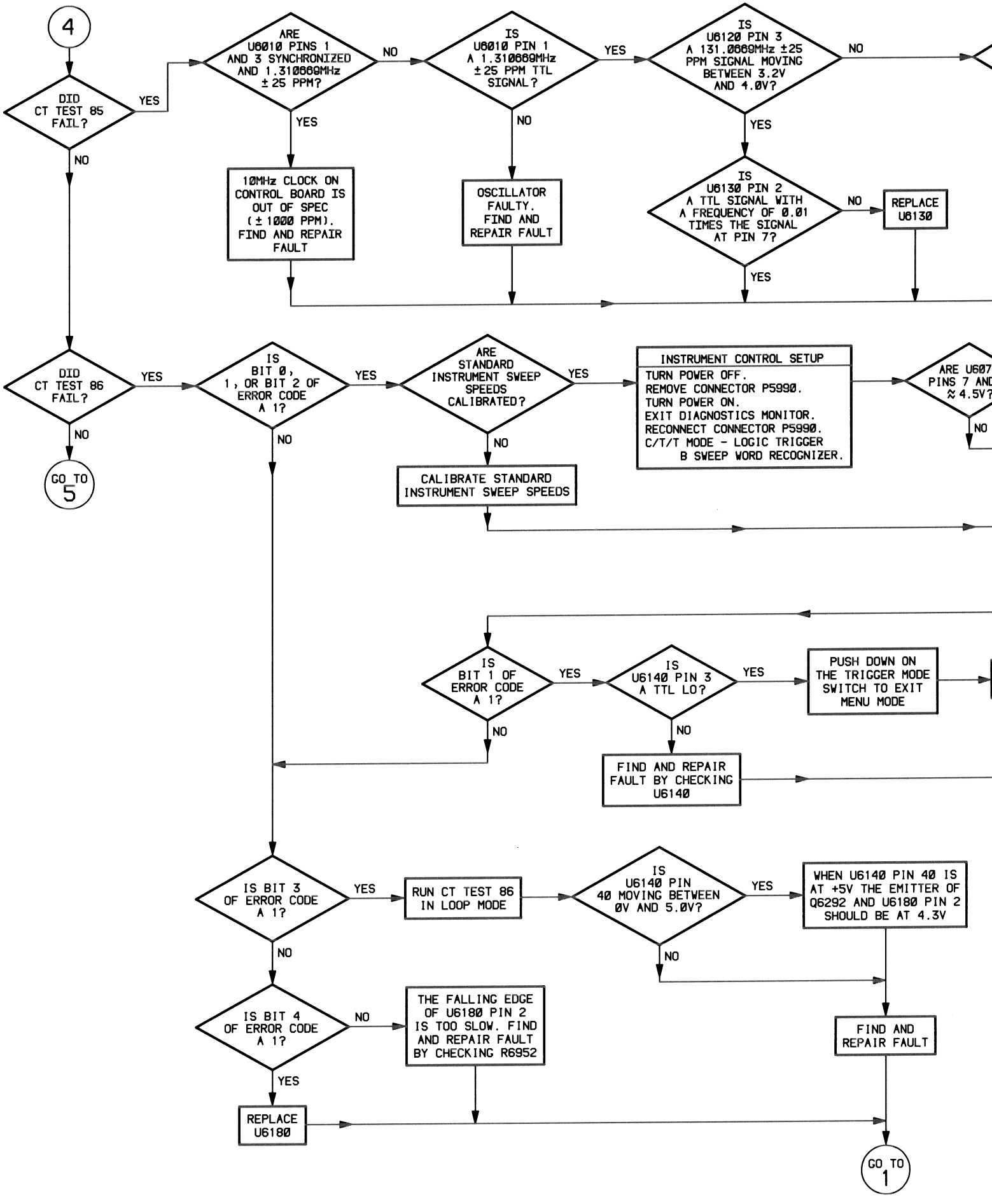

3
DID CT TEST 84 FAIL?
NO
GO TO 4
YES
RUN CT TEST 84 IN LOOP MODE
ARE U6180 PINS 6 AND 35 MOVING BETWEEN 3.2V AND 4.0V?
YES
NO
FIND AND REPAIR THE FAULT
GO TO 1
IS ERROR CODE 40?
NO
YES
INSTRUMENT CONTROL SETUP
EXIT DIAGNOSTICS MONITOR.
CONNECT CH 1 PROBE TO CALIBRATOR.
CH 1 VOLTS/DIV - 100mV/DIV.
DISABLE ALL C/T/T FUNCTIONS.
UNLOCK THE A AND B SEC/DIV KNOBS.
B TRIGGER MODE - TRIG AFT DLY.
A AND B SWEEPS - TRIGGERED.
A SEC/DIV - 1 µs/DIV
TSA AND TSB (FROM AND TO BUFFER BOARD) SHOULD MOVE BETWEEN VALID TTL LEVELS, AND U5990 PINS 2 AND 12 SHOULD BE LO.
FIND AND REPAIR FAULT
GO TO 1
IS ERROR CODE 0E?
YES
NO
INSTRUMENT
EXIT DIAGNOSTI
CONNECT CH 1 P
CH 1 VOLTS/DIV
A AND B SEC/DI
A TRIGER LEVEL
C/T/T MODE - L
IS ERROR CODE 0C THRU 13?
NO
YES
INSTRUM
EXIT DIAGNOST
CONNECT CH 1
CALIBRATOR.
CH 1 AND CH 2
A AND B SEC/D
A AND B TRIGG
C/T/T MODE -
INSTRUMENT CONTROL SETUP
EXIT DIAGNOSTICS MONITOR.
CONNECT CH 1 AND CH 2 PROBES TO THE CALIBRATOR.
CH 1 AND CH 2 VOLTS/DIV - 100mV/DIV.
A AND B SEC/DIV - 500ns/DIV.
A AND B TRIGGER LEVEL - 0.2V.
C/T/T MODE - LOGIC TRIGGER
A SWEEP A+B.
ARE TSA AND TSB (FROM BUFFER BOARD) A 1MHz SQUARE WAVE?
YES
NO
DO TSA AND TSB (FROM BUFFER BOARD) MOVE BETWEEN 1.5V AND 2.4V?
YES
NO
DO U6180 PINS 36 AND 37 MOVE BETWEEN 3.2V AND 4.0V?
YES
NO
ARE U5952 PINS 2 AND 16 A TTL HI?
YES
NO
INST
CONTR
C/T/T
B DELAY
FIND AND REPAIR FAULT BY CHECKING POSSIBLE CAUSE LISTED IN TABLE 5-4
GO TO 1
U607
< 3
IS U6070 PIN 9 ≈4.5V?
YES
NO
IS U6180 PIN 2 AND U6070 PIN 4 MOVING BETWEEN 3.2V AND 4.0V?
YES
NO
IS THE SAME SIGNAL AT U6070 PINS 4 AND 2 AND U6180 PIN 2?
YES
NO
INSTRUMENT CONTROL SETUP
C/T/T MODE - LOGIC TRIGGER A SWEEP A+B
IS U6180 PIN 19 MOVING BETWEEN 3.2V AND 4.0V?
NO

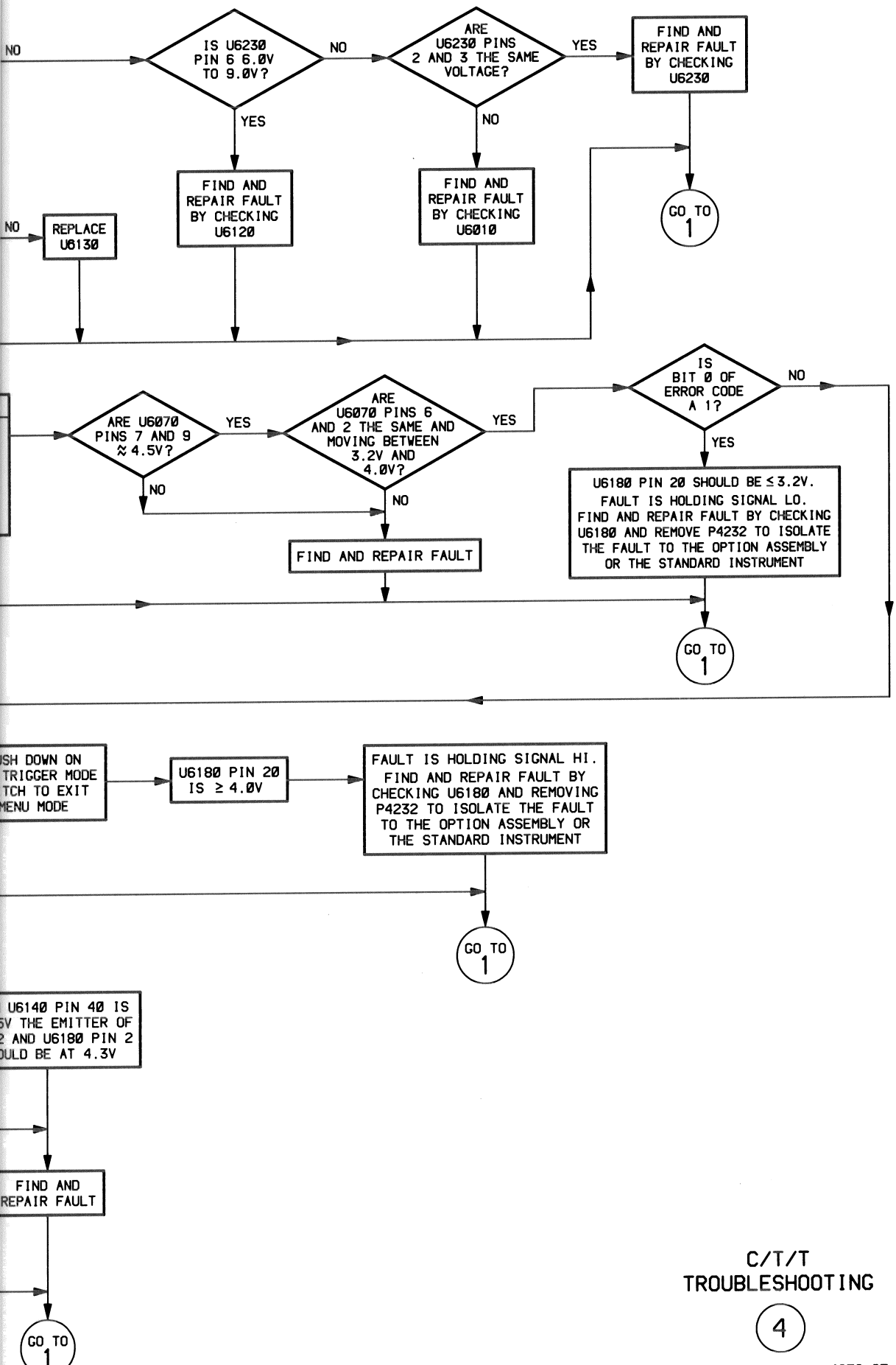


C/T/T TROUBLESHOOTING

3

4632-22

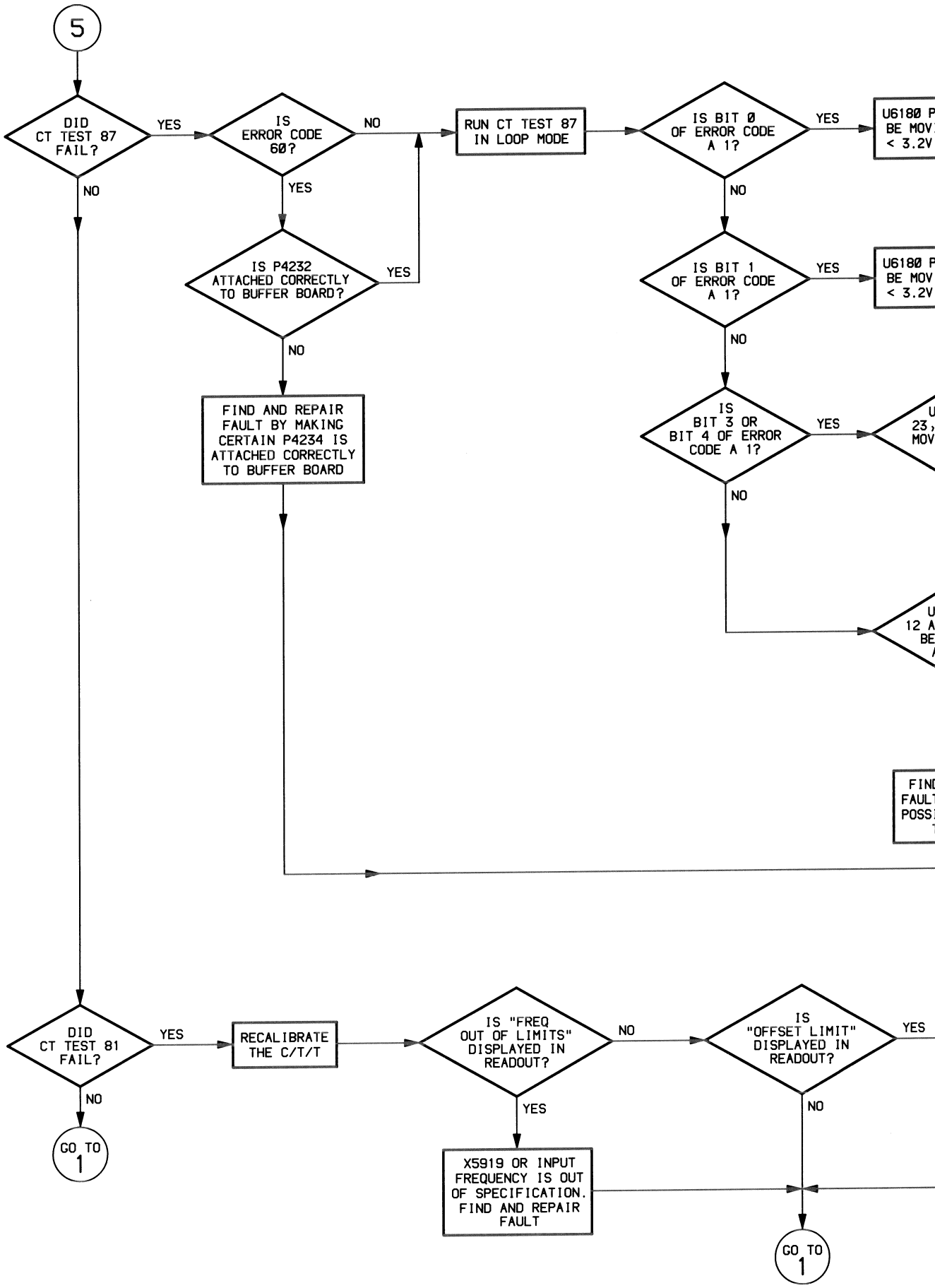

4
DID CT TEST 85 FAIL?
YES
NO
ARE U6010 PINS 1 AND 3 SYNCHRONIZED AND 1.310669MHz ±25 PPM?
NO
YES
10MHz CLOCK ON CONTROL BOARD IS OUT OF SPEC (±1000 PPM). FIND AND REPAIR FAULT
IS U6010 PIN 1 A 1.310669MHz ±25 PPM TTL SIGNAL?
YES
NO
OSCILLATOR FAULTY. FIND AND REPAIR FAULT
IS U6120 PIN 3 A 131.0669MHz ±25 PPM SIGNAL MOVING BETWEEN 3.2V AND 4.0V?
NO
YES
IS U6130 PIN 2 A TTL SIGNAL WITH A FREQUENCY OF 0.01 TIMES THE SIGNAL AT PIN 7?
NO
REPLACE U6130
YES
DID CT TEST 86 FAIL?
YES
NO
GO TO 5
IS BIT 0, 1, OR BIT 2 OF ERROR CODE A 1?
YES
NO
ARE STANDARD INSTRUMENT SWEEP SPEEDS CALIBRATED?
YES
NO
CALIBRATE STANDARD INSTRUMENT SWEEP SPEEDS
INSTRUMENT CONTROL SETUP
TURN POWER OFF.
REMOVE CONNECTOR P5990.
TURN POWER ON.
EXIT DIAGNOSTICS MONITOR.
RECONNECT CONNECTOR P5990.
C/T/T MODE - LOGIC TRIGGER
B SWEEP WORD RECOGNIZER.
ARE U607
PINS 7 AND
≈ 4.5V?
NO
IS BIT 1 OF ERROR CODE A 1?
YES
NO
IS U6140 PIN 3 A TTL LO?
YES
NO
PUSH DOWN ON THE TRIGGER MODE SWITCH TO EXIT MENU MODE
FIND AND REPAIR FAULT BY CHECKING U6140
IS BIT 3 OF ERROR CODE A 1?
YES
NO
RUN CT TEST 86 IN LOOP MODE
IS U6140 PIN 40 MOVING BETWEEN 0V AND 5.0V?
YES
NO
WHEN U6140 PIN 40 IS AT +5V THE EMITTER OF Q6292 AND U6180 PIN 2 SHOULD BE AT 4.3V
FIND AND REPAIR FAULT
IS BIT 4 OF ERROR CODE A 1?
NO
YES
THE FALLING EDGE OF U6180 PIN 2 IS TOO SLOW. FIND AND REPAIR FAULT BY CHECKING R6952
REPLACE U6180
GO TO 1

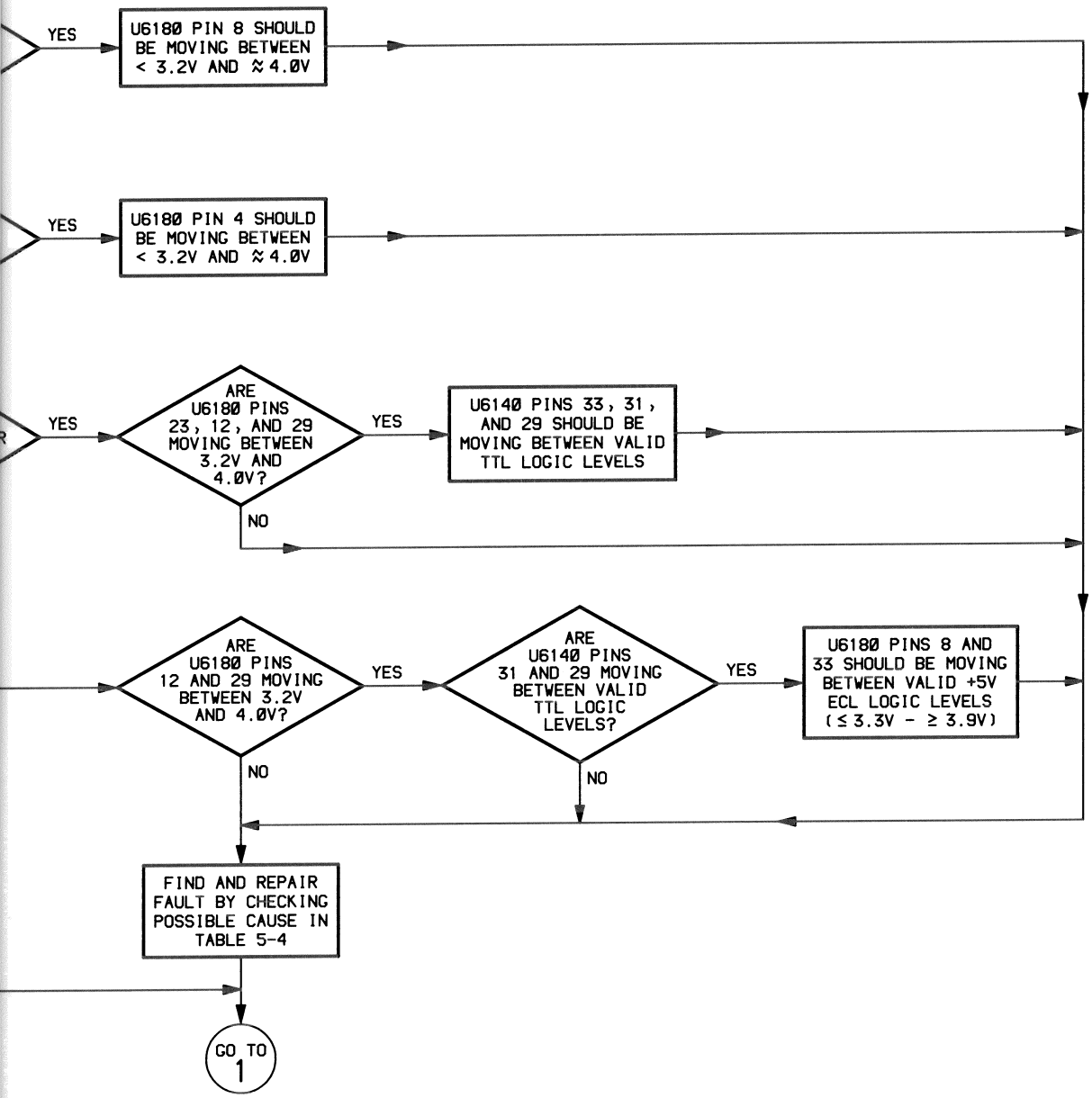


C/T/T TROUBLESHOOTING

4

4632-23


5
DID CT TEST 87 FAIL?
YES
NO
IS ERROR CODE 60?
NO
YES
IS P4232 ATTACHED CORRECTLY TO BUFFER BOARD?
YES
NO
FIND AND REPAIR FAULT BY MAKING CERTAIN P4234 IS ATTACHED CORRECTLY TO BUFFER BOARD
RUN CT TEST 87 IN LOOP MODE
IS BIT 0 OF ERROR CODE A 1?
YES
U6180 P
BE MOV
< 3.2V
NO
IS BIT 1 OF ERROR CODE A 1?
YES
U6180 P
BE MOV
< 3.2V
NO
IS BIT 3 OR BIT 4 OF ERROR CODE A 1?
YES
U
23,
MOV
NO
U
12 A
BE
FIND
FAULT
POSSI
DID CT TEST 81 FAIL?
YES
NO
GO TO 1
RECALIBRATE THE C/T/T
IS "FREQ OUT OF LIMITS" DISPLAYED IN READOUT?
NO
YES
X5919 OR INPUT FREQUENCY IS OUT OF SPECIFICATION. FIND AND REPAIR FAULT
IS "OFFSET LIMIT" DISPLAYED IN READOUT?
YES
NO
GO TO 1



C/T/T TROUBLESHOOTING

5

4632-24

APPENDIX A

GPIB COMMAND REFERENCE

Table A-1
Counter/Timer/Trigger GPIB Command Summary

C/T/T Measurement Commands		
Header	**Argument**	**Argument**
CTRdy?		
CTSend?	IMMediate WAIt	
OPC	ON OFF	
C/T/T Setup Commands		
BTRigger BTRigger?	MODe: MODe	ALTSlope RUN TRIGGerable
COUNt COUNt?	EVent: MODe: EVEnt MODe	ATRigger WREcognizer FREquency TOTal PERIod
CTT CTT?	COUNt DBEvents LTRigger OFF RESET	
DBEvents DBEvents?	COUNt: EVEnt: STArt: SWEep: COUNt EVEnt STArt SWEep	<nr1> BTRigger WREcognizer ATRigger WREcognizer ASWeep BSWeep

Table A-1 (cont)

Header	Argument	Argument
LTRigger LTRigger?	ASWeep: BSWeep:	AANdb AORb WREcognizer WREcognizer
RESolution RESolution?	AUto R1Ns R100ps R10Ps	

Table A-2
Word Recognizer GPIB Command Summary

Header	Argument	Argument
WREcognizer WREcognizer?	CLOck: RADix: WORd: CLOck RADix WORd	ASYnch DNClock UPClock BINary HEX OCTal <ASCII binary data>

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

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A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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MANUAL CHANGE INFORMATION

Date: 11-10-84 **Change Reference:** M55997

Product: 2445/2465 OPTIONS 06 & 09 SERVICE **Manual Part No.:** 070-4632-00

DESCRIPTION PG 38

EFFECTIVE SERIAL NUMBERS: **B025500 (2445 Oscilloscope)**
B028060 (2465 Oscilloscope)

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A20	670-7830-05	CKT BOARD ASSY: BUFFER (OPTION 01 WITH ANY COMBINATION OF OPTIONS 06, 09, OR 10)
A20	670-7830-08	CKT BOARD ASSY: BUFFER (OPTION 01 & 05, WITH ANY COMBINATION OF OPTIONS 06, 09, OR 10)
A20R4202	321-0132-00	RES,FXD,CMPSN: 232 OHM,5%,0.125W
A20R4203	321-0101-00	RES,FXD,CMPSN: 110 OHM,5%,0.125W
A20R4207	321-0101-00	RES,FXD,CMPSN: 110 OHM,5%,0.125W
A20R4208	321-0132-00	RES,FXD,CMPSN: 232 OHM,5%,0.125W

DIAGRAM CHANGES

DIAGRAM  BUFFER BOARD ANALOG & POWER DISTRIBUTION

Change R4202 (location 5D) to a 232Ω resistor.
Change R4203 (location 5D) to a 110Ω resistor.
Change R4207 (location 4C) to a 110Ω resistor.
Change R4208 (location 4C) to a 232Ω resistor.

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