MICROCOMPUTER SYSTEM MAINTENANCE

Several maintenance aids are built into the microcomputer system. These operating tests demonstrate correct performance or indicate the location of a problem, if any.

The switch settings that set up two of these tests are described first. These are followed by descriptions of the three tests.

In the first test, the microcomputer executes a self-test that verifies, as much as possible, correct operation. RAM, ROM, and interface adapters are checked. Any failure found is indicated by LEDs on the GPIB board.

The second test forces the microcomputer to cycle through all of its addresses. This test requires less of the system to run than does the first test, so it may be used to troubleshoot problems that disable the first test mode.

The third test exercises the instrument bus to isolate problems in data transfer between the microcomputer and the instrument.

Memory Board Option Switch

S1050 on the Memory board selects the microcomputer system test modes, as well as selecting some instrument options. Figure 6-26 shows the selections controlled by the individual switches of S1050.

The microcomputer reads these switches only at power-up. Any change in a switch position takes effect, when the instrument is next powered up.

Power-up Self Test

Normal instrument operation is selected by setting both switch 7 and switch 8 of S1050 closed. At power-up, the processor executes steps 1 and 2, the first part of step 3, and steps 4 and 5 of the Microcomputer System Test described below. If the first two steps in the test are successful, any problems in the other three steps are reported on the crt. Possible error messages are:

"RAM XX TESTS BAD. PUSH A BUTTON TO CONT."

"ROM XX TESTS BAD. PUSH A BUTTON TO CONT."

"ROM XX MISPLACED. PUSH A BUTTON TO CONT."

"TIMER TESTS BAD. PUSH A BUTTON TO CONT."

Cross-reference tables between the ROM and RAM numbers given in error messages (XX) and the circuit numbers of the parts are given in Table 6-8 and Table 6-9.

If the entire test is successful, the instrument initializes and begins normal operation.

Microcomputer System Test

The microcomputer system test is chosen by setting switch 8 of S1050 closed and switch 7 of S1050 open. The microcomputer reports the test results via the LEDs on the GPIB board rather than on the CRT, allowing this test to be performed when the display is inoperative. If a problem is found, the test stops and the problem is indicated by one of the LEDs on the GPIB board. If no problem is found, the system test takes two minutes.

The system test does not begin normal operation after the test is complete.

Addresses are specified as hexadecimal numbers in this description.

1. The microcomputer first verifies the check sum of the system ROM portion of U3050 on the Memory board. The check sum test uses no memory except for U3050. The correct ROM must be installed, the clock on the Processor board must be present, and the microcomputer system bus must be operating correctly.

If the correct check sum is not obtained, the routine halts and lights DS1047 on the GPIB board. If the test stops but does not light DS1047, and everything else seems to be in order, the Address Bus Test (described later in this section) should be performed.

2. The microcomputer next checks part of the processor interface to the instrument bus PIA, U1010, on the Processor board. If the test fails, the routine stops and lights DS1050 on the GPIB board. If the test succeeds, the processor assumes that the instrument bus interface is working, and displays "PROCESSOR SYSTEM TEST, PLEASE WAIT." on the crt.

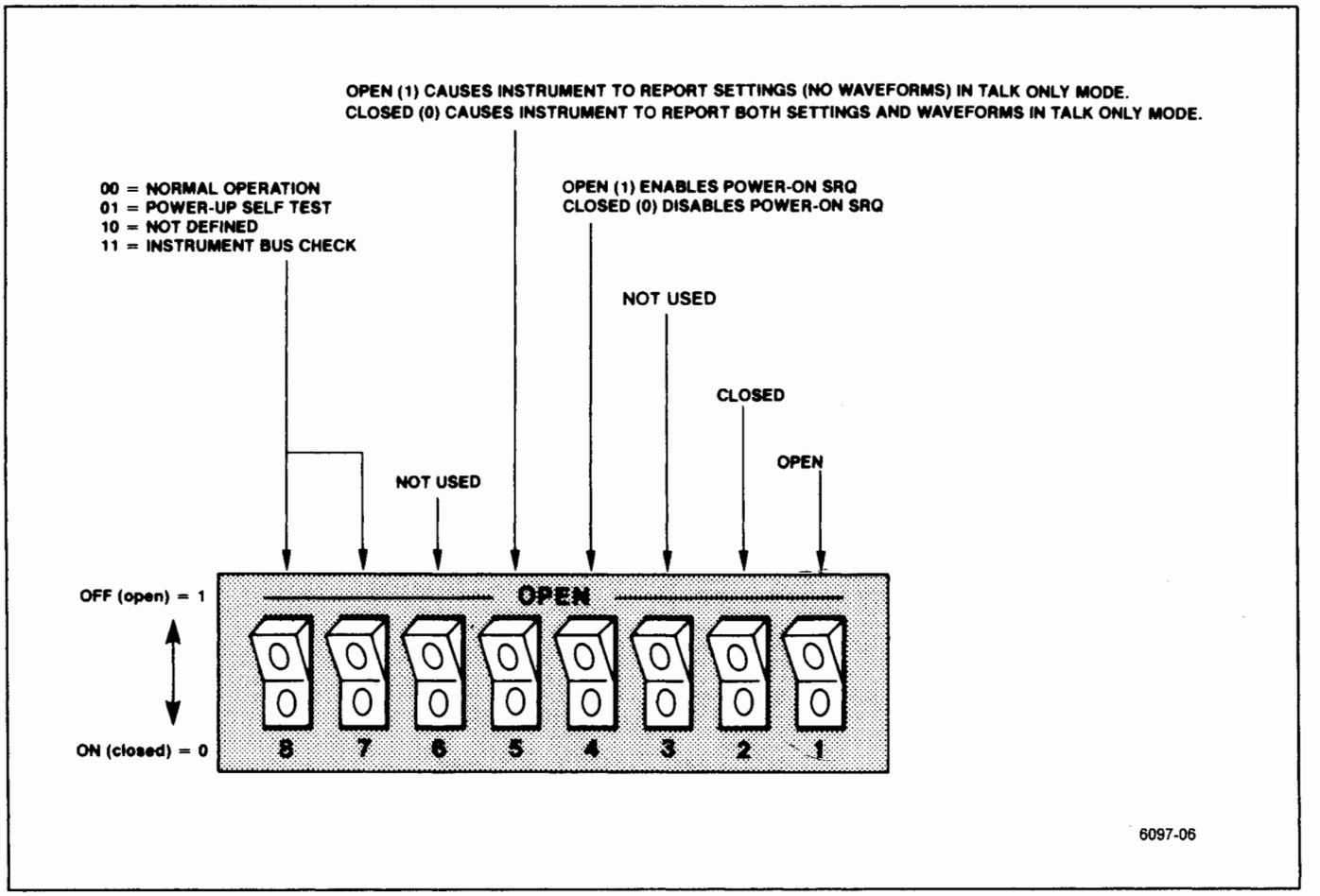


Figure 6-26. Options switch on the Memory board.

3. The microcomputer next checks RAM. The RAM test contains three parts. The first part performs a quick test of all volatile RAM (U1010 and U3020 on the Memory Board). The microcomputer loads the bit pattern 01010101 into a RAM location, reads the location, and compares what is returned to what was stored. The microcomputer then repeats this test with the pattern 10101010. This step does not rely on the RAM being good to execute.

If a reading error occurs, the microcomputer stops the test and pulses LED DS1048 on the GPIB board the number of times corresponding to the RAM that failed the test (refer to Table 6-8).

The second part of the test is a Moving Inversions test of all RAM (volatile and non-volatile). This test assumes that a few byes of the RAM are good. If a RAM fails this test, DS1048 on the Memory board is pulsed as described earlier.

Table 6-8
RAM TEST

RAM Number	RAM Socket	DS1048 Pulses
1	U1010	1
2	U3020	2
3	U1030	3
4	U1020	4

The third part of the test is similar to the first part. However, the memory contents are allowed to reside in memory for thirty seconds before being read back. The results are reported via DS1048.

4. The microcomputer next check sums all ROMs. The check sum stored in each ROM is compared to the check sum formed by the successive 16-bit spiral sum of each byte in the ROM, starting at the third location in the ROM. The ROM number coded into each ROM will cause an error if a ROM is installed in the wrong location.

The Tektronix part number is also coded into each ROM. If the part number suffix and its complement, which are stored in the fifth and sixth bytes of the ROM header, do not read as complements, the microcomputer assumes that no ROM is installed and does not attempt the checksum test.

If a bad or misplaced ROM is found, the microcomputer pulses DS1049 on the GPIB board N+1 times, where N is the number of the ROM in error (e.g., a bad ROM #3 will cause four pulses; refer to Table 6-9). Missing ROMs are reported as described in part 6.

Table 6-9
ROM TEST

ROM Number	ROM Socket	Board	DS1049 Pulses
0	U3060	A54 Memory	1
1	U3060	A56 Memory	2
2	U1010	A56 GPIB	3
3	U1010	A56 GPIB	4
4	U1020	A56 GPIB	5
5	U1020	A56 GPIB	6
6	U1025	A56 GPIB	7
7	U1025	A56 GPIB	8
8	U1035	A56 GPIB	9
9	U1035	A56 GPIB	10
10	U3015	A56 GPIB	11
11	U3015	A56 GPIB	12
12	U3020[a]	A56 GPIB	13
13	U3020[a]	A56 GPIB	14
14	U3030[a]	A56 GPIB	15
15	U3030[a]	A56 GPIB	16
16	U3050	A54 Memory	17
17	U3050	A54 Memory	18

5. The microcomputer next tests U2015, a timer chip on the Processor board. If any of the timers in U2015 result in time delays that are too short or too long, the test stops with LED DS1053 on the GPIB board lit.

[a] These chips are loaded on the GPIB board only when certain options are installed in the instrumenet.

6. The microcomputer resets the GPIA, U2050, on the GPIB board and checks to see that the GPIA is not addressed to talk or listen. The GPIA is set to the listen-only mode and checked to see that it is addressed to listen. The GPIA is then set to the talk-only mode and checked to see that it is addressed to talk. If any part of this step fails, the test stops and LED DS1052 on the GPIB board is lit.

If all steps in the test are successfully completed, the microcomputer lights LED DS1054 on the GPIB board. The LED is lit continuously if no empty ROM sockets are found, or pulsed the number of times corresponding to the number of empty ROM sockets found. If the number of pulses is greater than the number of absent ROMs, a ROM (or ROMs) was missed in step 4. Look for a problem on the chip-select line or on the "D7" data bus line.

If the microcomputer system passes the test, but does not control the instrument, run the Instrument Bus Check described later in this section.

Address Bus Test

Select the address bus test by moving jumper P3015 on the Processor board to the TEST position. This forces the 6808's data lines to hexadecimal 5F. As a result, the 6808 continuously executes a "CLR B" instruction, and repetitively cycles through all of its address space. There should be a known pattern on the microcomputer address and control lines and at the output of the address decoders. This allows qualified service personnel to correct problems that prevent the microcomputer from running its self-test.

The spectrum analyzer will not function while running this test.

Microcomputer Bus — As the microcomputer cycles through its address space, it toggles the address lines. The MSB, A15, has a period of approximately 1540 ms. Each line, A14 through A0, has a period half that of the previous line. Thus, the LSB A0 has a period of approximately 4.7 μs. High-order lines A15 through A12 are shown in Figure 6-27. Ignore the narrow pulses that may be evident during the low portion of each cycle.

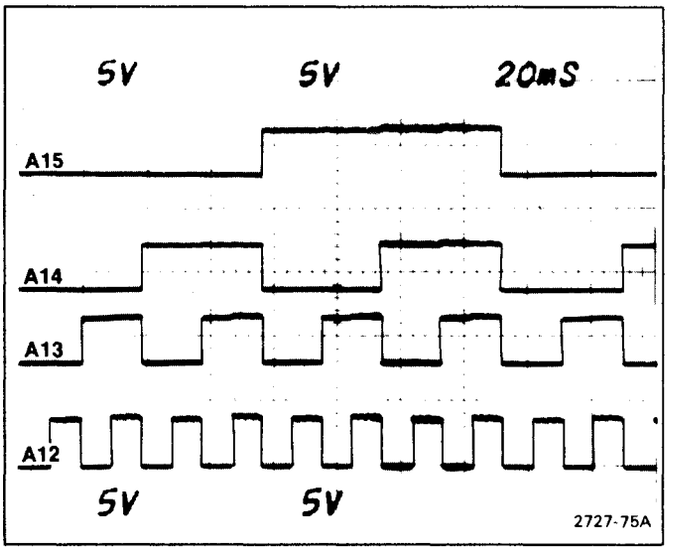


Figure 6-27. A15 through A12 in microcomputer test mode.

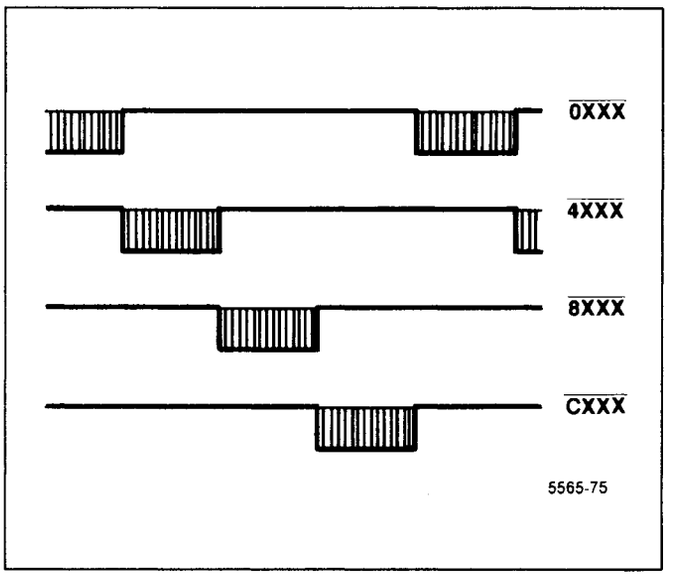


Figure 6-28. Four main block select outputs of address decoder U2045.

The data lines on the microprocessor side of U2025 on the Processor board are static; D7 and D5 are low, the others are high. The TEST position of P3015 disables U2025. On the bus side of this buffer, the data lines are driven by the various memory devices on the bus as they are addressed.

Examining the data lines can locate shorted or open lines; i.e., lines inactive at high, low, or in-between states or changing in unison, usually to indeterminate logic levels of +1 V to +2 V. A problem related to a particular device may be evident only while that device is addressed.

Memory Address Decoders — Address decoder U2045 on the Memory board sets its outputs low in turn to access blocks of memory space. The four main block-select outputs are shown in Figure 6-28.

U3025 on the Memory board decodes the RAM addresses. Because of the power-up condition of the bank select, only one of the non-volatile RAM chips will be selected. The RAM select outputs and their relationship to Oxxx(bar) is shown in Figure 6-29.

U3040 and U3045 on the Memory board decode the $\overline{I/O}$ select line and the select line for S1050. These signals are shown in Figure 6-30.

Ignore the narrow pulses evident during the time each output is asserted. The pulses result from address lines toggling between microcomputer cycles.

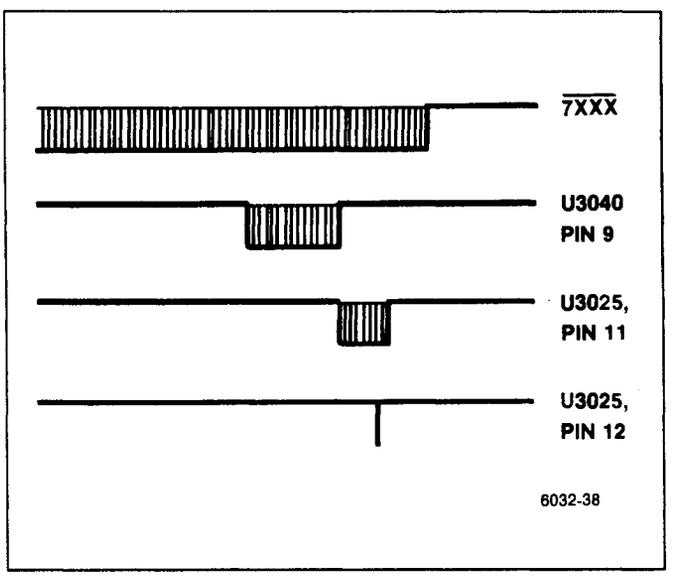


Figure 6-29. RAM select output in relation to 0XXX.

Processor Address Decoder — Address decoder U3035 on the Processor board decodes several chip-selects. Y0, Y1, Y5, and Y7 are shown in relation to the $\overline{I/O}$ line in Figure 6-31.

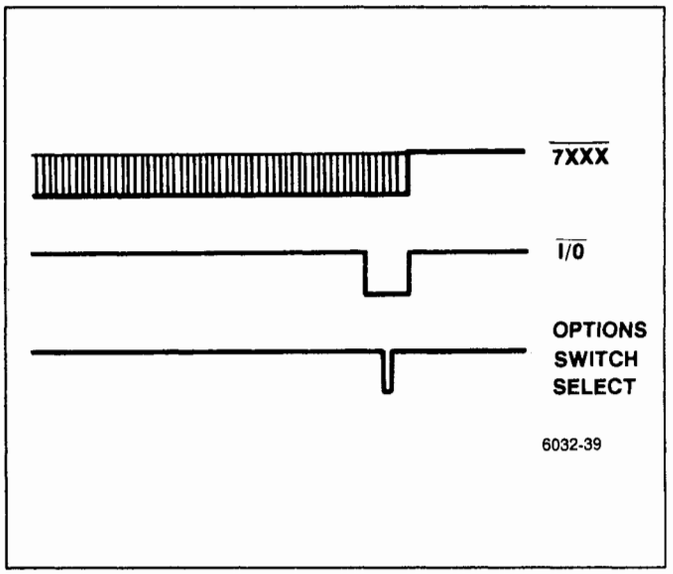


Figure 6-30. $\overline{I/O}$ and S1050 select lines in relation to 0XXX.

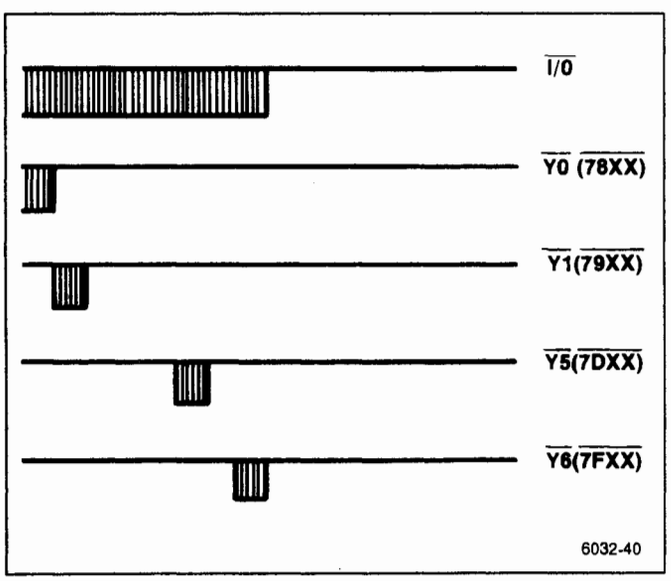


Figure 6-31. Chip selects Y0, Y1, Y5, and Y7 in relation to $\overline{I/O}$.

GPIB Board Address Decoders — Address decoder U1055 on the GPIB board sets its outputs low to select the GPIA, the GPIB address switch and the bank latch. Y2, Y4, and Y6 are shown in relation to $\overline{I/O}$ in Figure 6-32.

Clocks and Control Lines — The 6808 clock input line should be a square wave with a period of approximately 0.293 μs. The ϕ 2 output on pin 37 should have a period of approximately 1.17 μs. VMA, RESET, NMI, and R/W should be high. IRQ(bar) may be either high or low, depending on how assemblies on the instrument bus power up.

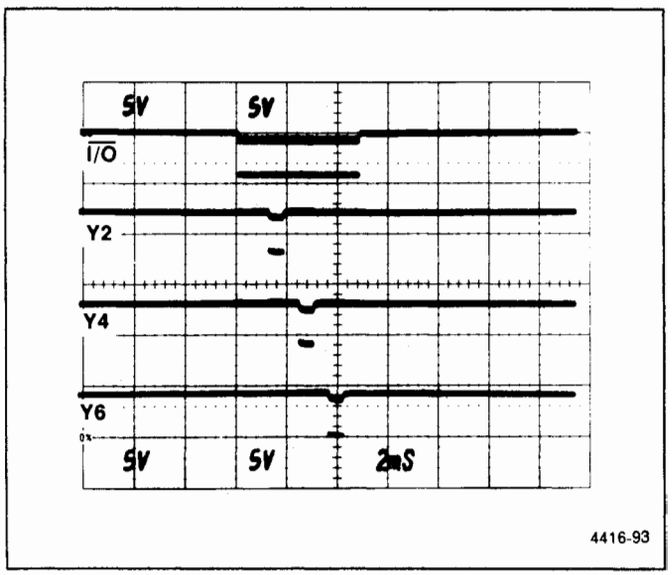


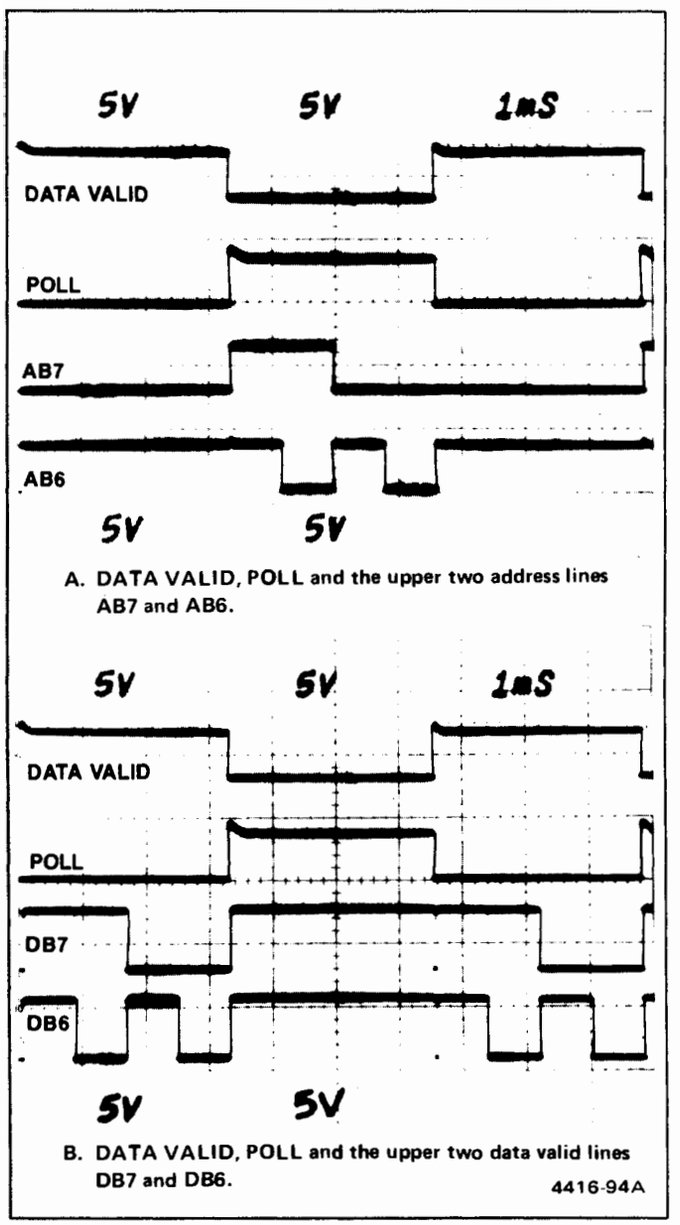
Figure 6-32. Chip selects Y2, Y4, and Y6 in relation to $\overline{I/O}$.

Instrument Bus Test

If the microcomputer performs the power-up self-test, but fails to properly control the instrument, the instrument bus interface may be faulty. Select the instrument bus test by setting the option switch as shown in Figure 6-26. The microcomputer continuously writes to the instrument bus in a repetitive manner, so the instrument does not operate normally.

The pattern on the instrument bus toggles DATA VALID and POLL and exercises the address and data lines. The address lines change when DATA VALID is low and the data lines change when DATA VALID is high. However, if an assembly on the bus is requesting service because of the way it powered up, DB0-DB4 may continue to change after DATA VALID goes low. In this case, an assembly or assemblies may respond to the high state of POLL and the changing state of AB7 and attempt to report status.

The pattern for the upper address and data lines is shown in Figure 6-33. From address or data line 7 to line 0, each line changes at twice the rate of the previous line, resulting in 128 cycles on the LSB lines. The initial pulse on the upper four data lines is not part of the +2 pattern and is not repeated on the lower four data lines. It is possible to discover open or shorted lines by comparing the patterns to those in Figure 6-33, checking that they divide by 2. Look for lines that stay high or low, change together or at wrong times in the pattern, or go to indeterminate logic levels (1 V to 2 V).



A. DATA VALID, POLL and the upper two address lines AB7 and AB6.

B. DATA VALID, POLL and the upper two data valid lines DB7 and DB6.

4416-94A

Figure 6-33. Instrument bus check.

TROUBLESHOOTING ON THE INSTRUMENT BUS

Instrument Bus Data Transfers

There are two commands and queries provided to aid troubleshooting of circuit functions controlled by the instrument bus. These circuits get data from the microcomputer or respond with data for the microcomputer. The ADDR command and ADDR query set and return the instrument bus address for the DATA command. The DATA command and DATA query set and return data on the instrument bus.

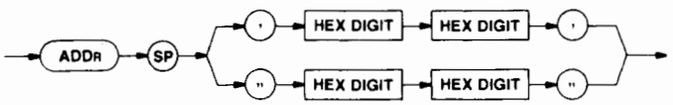
CAUTION

Because the DATA command changes the status of internal hardware, its use may prevent normal Spectrum Analyzer operation. Incorrect settings of some hardware could cause instrument damage.

These commands and queries are transmitted to the Spectrum Analyzer with the PRINT statement. The spectrum analyzer response to a query is input into a string variable with the INPUT statement. A string variable is formed by ending the variable name with a dollar sign ($). Examples: A$, X1$.

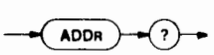
For the GPIB PRIMARY ADDRESS, enter the decimal equivalent of the spectrum analyzer rear-panel GPIB ADDRESS switch settings.

ADDR (instrument bus address) command



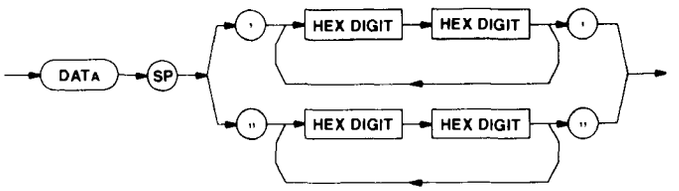
HEX DIGIT — A character in the sequence 0 through 9 and A through F that represents a hexadecimal digit. The two digits (in order) form a number to represent a location on the instrument bus used by following DATA commands. If a character is not a hexadecimal digit or part of a pair of digits, it is not used to execute the ADDR command, and an error is reported.

ADDR (instrument bus address) query



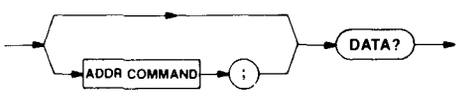
Response to ADDR query

DATA (instrument bus data) command



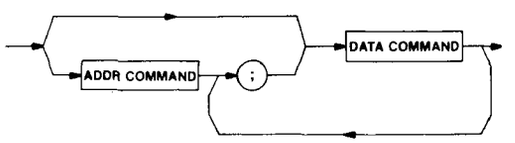
HEX DIGITS — As with ADDR, a pair of digits forms a hexadecimal number. The number is a data value to be sent on the instrument bus to the location specified by the last ADDR command. This allows internal spectrum analyzer parameters to be set for service; these parameters control functions by setting the status or mode of spectrum analyzer circuit assemblies. Up to 16 pairs of characters are accepted. If a character is not a hexadecimal digit or part of a pair of digits, the data byte formed by the pair is not executed and an error is reported. Also, an error is reported when data is sent to an invalid address.

DATA (instrument bus data) query



Response to DATA query

Combined ADDR command and DATA command



The address command may precede a data command or query to identify the instrument bus location as part of the same message.

Errors related to these commands are 41, invalid DATA or ADDR argument contents, and 42, DATA direction not compatible with ADDR direction.

Instrument Bus Registers

Registers provide the link between the instrument bus and microcomputer controlled functions. The registers are defined here in the same order as they appear in the Diagrams section. The definitions are provided to help in constructing DATA commands and interpreting responses to DATA queries.

The data is presented here as binary. In some cases a data value occupies the entire register width; for instance, a value in digital storage. In other cases, a single bit or group of bits in the register forms a code; for instance, the upper five bits in the sweep rate and mode register indicate the sweep time/division. The meaning of the data is not fully defined here; refer to the description of the circuit module in Section 5 for details.

To use the binary codes presented here with the DATA command and query statements, you must convert binary to hexadecimal. The binary code number 01001011 is used as an example in the following steps.

1. Group the lower four bits and the upper four bits (break the data byte in half).

   01001011 = 0100 1011

2. Convert each group of four bits to a hexadecimal digit. Hexadecimal digits range from 0 to F in the sequence 0123456789ABCDEF.

   0100 = 4
   1011 = B (i.e., 8+0+2+1=11, which is hexadecimal B)

3. Group the two hexadecimal digits together, keeping their respective places.

   4 and B make the two-digit hexadecimal number 4B

The information in Table 6-10 is separated by registers. The following information is related to the table information by leading alpha designators.

A. Variable Resolution (refer to diagram 20)

The microcomputer writes to two variable resolution registers. The data MSB steers the other bits that are defined into the desired register. When DB7 equals 1, it steers DB0 through DB2 to select the resolution bandwidth. When DB7 equals 0, it steers DB6 through DB0 to select the amount of gain added in the VR section and the band leveling gain (gain adjustment related to front-end response in each band). These two functions are addressed and set together by the same data byte.

B. Log and Video Amplifier (refer to diagram 23)

There are two registers that receive data from the microcomputer. One register controls video offset (78) and the other controls the display modes and the vertical scale factor (79).

C. Video Processor (refer to diagram 24)

Register 7C controls out-of-band clamping, video filtering, and leveling.

D. Digital Storage, Vertical (refer to diagram 25)

Registers 7A and FA on the Vertical Digital Storage board transfer display data to and from the microcomputer for spectrum analyzer GPIB operations. Register 7B controls digital storage functions.

E. Z-Axis & RF Interface (refer to digram 28)

Register 4F on the Z-Axis & RF Interface board enables Z-axis and RF attenuator control. Register CF reports power supply status.

F. Crt Readout (refer to diagram 30)

Register 5F controls crt readout and data steering. Register 2F accepts data from the microcomputer.

G. Sweep (refer to diagram 31)

The microcomputer writes to registers 0F and 1F to control sweep rate, mode, holdoff, interrupts, and triggering.

H. Span Attenuator (refer to diagram 32)

Registers 75 and 76 control the span attenuator.

I. 1st LO Driver (refer to diagram 33)

Register 72 controls functions on the 1st LO Driver board. Register 7E is added to make the PEAKing control programmable.

J. Preselector Driver (refer to diagram 34)

Register 77 controls functions on the Preselector Driver. The single bit DB3 responds on the data bus to indicate that the board is installed when the microcomputer performs a read at F7.

K. CENTER/MKR FREQUENCY Control (refer to diagram 35)

Register 70 is provided for control functions and register 71 is provided for data values for center frequency DAC(s). A read, F0, returns the results of a comparison of the DAC output voltage and a memory voltage.

L. Auxiliary Synthesizer Control (refer to diagram 37)

Register 7D accepts data to set the synthesizer chip, U4041, to output 200 MHz to 220 MHz in 400 kHz steps. Values of R, A, and N are given to determine the output frequency as given by the formula

$$f_{out} = (1/R)(NP+A)$$

where R, the reference division ratio, is set at 5 and P is the prescale value of 32. N values needed are 31 through 34, while A ranges from 0 to 31. (Table 6-11 shows the f_{out} results for given N and A values.)

M. Phase Lock (refer to diagram 39)

Register 73 accepts data to preload the divide-by-n counter and control the synthesizer. Successive reads from register F3 obtain status and counter outputs. After resetting the counter output register selector, three read cycles return status bits and counter bits in the most significant byte and remaining counter bits in following bytes.

N. Front Panel (refer to diagram 43)

Reading from F4 accesses the keyboard encoder and the CENTER/MKR FREQUENCY control encoder.

Table 6-10
INSTRUMENT BUS REGISTERS

Data Bits 7 6 5 4 3 2 1 0	Description
A. Variable Resolution (3F)	
	Resolution Bandwidth
1 x x x x 0 0 1	1 MHz Resolution Bandwidth
1 x x x x 0 1 0	100 kHz Resolution Bandwidth
1 x x x x 0 1 1	10 kHz Resolution Bandwidth
1 x x x x 1 0 0	1 kHz Resolution Bandwidth
1 x x x x 1 0 1	100 Hz Resolution Bandwidth
	Gain, Leveling
0 0 0 0 0 x x x	Band 1 Leveling
0 0 1 0 0 x x x	Band 2 Leveling
0 0 0 1 0 x x x	Band 3 Leveling
0 0 1 1 0 x x x	Band 4 Leveling
0 0 0 0 1 x x x	Band 5 Leveling
0 0 1 0 1 x x x	Band 6 Leveling
0 0 0 1 1 x x x	Band 7 Leveling
0 0 1 1 1 x x x	Band 8 Leveling
0 1 0 0 0 x x x	Band 9 Leveling
0 1 1 0 0 x x x	Band 10 Leveling
0 x x x x 0 0 0	0 dB Gain
0 x x x x 0 0 1	10 dB Gain
0 x x x x 1 0 0	20 dB Gain
0 x x x x 1 0 1	30 dB Gain
0 x x x x 1 1 1	40 dB Gain
B. Log & Video Amplifier	
	Video Offset (78)
DB7–DB0	LSB = 1/4 dB Total range = 63.75 dB
	Modes and Scale Factor (79)
1 x x x x x x x	Pulse stretcher on
0 x x x x x x x	Pulse stretcher off
x 1 x x x x x x	Identify offset on
x 0 x x x x x x	Identify offset off
x x 0 1 x x x x	Lin
x x 1 0 x x x x	Log
x x 0 0 x x x x	Full-screen deflection
DB3–DB0	Log vertical scale factor in dB/div

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
C. Video Processor (7C)	
0 1 1 x x x x x	Out-of-band clamp = no clamp
0 0 1 x x x x x	Out-of-band clamp = clamp upper 5 div
1 1 1 x x x x x	Out-of-band clamp = clamp lower div
0 1 0 x x x x x	Out-of-band clamp = clamp lower 5 div
x x x 0 0 0 0 x	Video filter off
x x x 0 0 0 1 x	Video filter 30 kHz
x x x 1 0 0 1 x	Video filter 3 kHz
x x x 1 1 0 1 x	Video filter 300 Hz
x x x 0 0 1 1 x	Video filter 30 Hz
x x x 1 0 1 1 x	Video filter 3 Hz
x x x 1 1 1 1 x	Video filter 0.3 Hz
x x x x x x x 1	Base-line leveling on
x x x x x x x 0	Base-line leveling off
D. Digital Storage	
	Horizontal Digital Storage Board
	7B
1 x x x x x x x	Digital Storage Acquisition Enable
0 x x x x x x x	Digital Storage Acquisition Disable
x 1 x x x x x x	Extended Address 2
x x 1 x x x x x	Extended Address 1
x x x 1 x x x x	Extended Address 0
x x x x 1 x x x	B–SAVE A on
x x x x 0 x x x	B–SAVE A off
x x x x x 1 x x	VIEW B on
x x x x x 0 x x	VIEW B off
x x x x x x 1 x	VIEW A on
x x x x x x 0 x	VIEW A off
x x x x x x x 1	SAVE A on
x x x x x x x 0	SAVE A off
Extended Address 2–0	Subaddress bits for Port 7A giving subaddresses 7–0. Addressing 7A.6 transfers the bus to the Vertical Digital Storage board.
	7A.0
DB1–DB7	Secondary Marker position bits
DB0	Secondary Marker trace bit

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
D. Digital Storage (cont)	
	Horizontal Digital Storage Board (cont)
	7A.1
DB8, DB9	Secondary Marker position bits
DB1	Secondary Marker trace bit
	7A.2
DB1–7	Primary Marker position bits
DB0	Primary Marker trace bit
	7A.3
DB8–9	Primary Marker position bits
DB1	Primary Marker trace bit
	7A.4
ADDR7–ADDR0	Digital Storage address bits
	7A.5
DB6	Transfers the bus to the Vertical Digital Storage board.
DB5	Determines if bus transfer is for a single cycle or until it is returned by the Vertical Digital Storage board.
DB4	Disable Update Marker
ADDR9, ADDR8	Loading ADDR7–0 reloads the last ADDR9,8
	7A.7
DB4–7	Primary Marker intensity bits
DB0–3	Secondary Marker intensity bits

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
D. Digital Storage (cont)	
	Horizontal Digital Storage Board (cont)
	FA
DB0–7	Digital Storage position bits
	FB
DB7	Always low to indicate that it is from the Horizontal Digital Storage board
DB0 & DB1	Digital Storage position bits
	Vertical Digital Storage Board
	FA
DB7–DB0	Data values from digital storage. A write to 7B initializes output to begin at the left of the trace and proceed to the right
	FB
DB7	Always high to indicate that it is from the Vertical Digital Storage board
	7A
DB7–DB0	Data values for digital storage. A write to 7B clears the address counter so values are stored for points on the display starting at the left and proceeding to the right in order
	7B
x 1 1 x x x x x	Peak/Average cursor in knob position
x 1 0 x x x x x	Peak/Average cursor in Peak position
x 0 1 x x x x x	Peak/Average cursor in Average position
x x x 1 x x x x	Max Hold on
x x x 0 x x x x	Max Hold off

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
E. Z-Axis & RF Interface	
	Z-Axis & RF Attenuator (4F)
1 x x x x x x x	Baseline clipper on
0 x x x x x x x	Baseline clipper off
x 1 x x x 1 x 1	0 dB RF attenuation
x 1 x x x 1 x 0	10 dB RF attenuation
x 0 x x x 1 x 1	20 dB RF attenuation
x 1 x x x 0 x 1	30 dB RF attenuation
x 1 x x x 0 x 0	40 dB RF attenuation
x 0 x x x 0 x 1	50 dB RF attenuation
x 0 x x x 0 x 0	60 dB RF attenuation
x x 1 x x x x x	829 MHz 2nd converter
x x 0 x x x x x	2 GHz 2nd converter
x x x 0 x x x x	RF INPUT
x x x x 0 x x x	100 ms to switch attenuator
	Power Supplies Status (CF)
x x x x x x 1 x	Fault
x x x x x x 0 x	Supplies okay
F. Crt Readout	
	Crt Control (5F)
1 x x x x x x x	Spectrum chop enable
0 x x x x x x x	Spectrum chop disable
x 1 x x x x x x	32 characters/line
x 0 x x x x x x	40 characters/line
x x 1 x x x x x	2 lines
x x 0 x x x x x	16 lines
x x x x 1 x x x	Max span dot on
x x x x 0 x x x	Max span dot off
x x x x x x 1 x	Address 2F contains an address
x x x x x x 0 x	Address 2F contains data
x x x x x x x 1	Readout enabled
x x x x x x x 0	Readout disabled to load readout
DB4	A8 (address bit 8)
DB2	A9 (address bit 9)

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
F. Crt Readout (cont)	
	Address/Data (2F)
DB7, DB6	If DB1 in 5F = 1 — A7, A6 of address. With A8 and A9 in 5F, they specify the line number (0–F).
DB5–DB0	If DB1 in 5F = 1 — A5–A0 of address. This specifies the character position in a line.
DB7	If DB1 in 5F = 0 — 1 = Character is a space 0 = Character is not a space
DB6	If DB1 in 5F = 0 — 1 = Skip a line 0 = Don't skip a line
DB5–DB0	If DB1 in 5F = 0 — Character code (lower 6 bits of ASCII)
G. Sweep	
	1F
1 x x x x x x x	Extended Address 1
x 1 x x x x x x	Extended Address 0
x x 1 x x x x x	Marker DAC/Ramp Generator
x x x x 1 x x x	Trigger Single Sweep
x x x x x 1 x x	Disable Sweep Gate
x x x x x x 1 x	Didsable Trigger
x x x x x x x 1	Abort Sweep
Extended Address 1 and Address 2	Subaddress bits for Port 0F giving subaddresses 3–0. Subaddresses 0 and 1 have the rest of the control bits not on Address 1F. Subaddresses 2 and 3 receive the 12 bits to set the DAC.

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
G. Sweep	
	Holdoff, Interrupt, Trigger (0F.0)
x x 0 0 x x x x	Short sweep holdoff
x x 0 1 x x x x	Medium sweep holdoff
x x 1 0 x x x x	Long sweep holdoff
x x x x 0 0 x x	Free run trigger mode
x x x x 0 1 x x	Internal trigger mode
x x x x 1 0 x x	External trigger mode
x x x x 1 1 x x	Line trigger mode
x x x x x x 1 x	Enable end-of-sweep interupt
x x x x x x x 1	Single Sweep Mode
	Sweep Rate and Mode (0F.1)
x x x 1 1 0 1 1	20 μs Time/Div
x x x 1 0 1 1 1	50 μs Time/Div
x x x 1 0 0 1 1	100 μs Time/Div
x x x 0 1 0 1 1	200 μs Time/Div
x x x 0 0 1 1 1	500 μs Time/Div
x x x 0 0 0 1 1	1 ms Time/Div
x x x 1 1 0 0 1	2 ms Time/Div
x x x 1 0 1 0 1	5 ms Time/Div
x x x 1 0 0 0 1	10 ms Time/Div
x x x 0 1 0 0 1	20 ms Time/Div
x x x 0 0 1 0 1	50 ms Time/Div
x x x 0 0 0 0 1	100 ms Time/Div
x x x 1 1 0 0 0	200 ms Time/Div
x x x 1 0 1 0 0	500 ms Time/Div
x x x 1 0 0 0 0	1 s Time/Div
x x x 0 1 0 0 0	2 s Time/Div
x x x 0 0 1 0 0	5 s Time/Div
x x x 0 0 0 0 0	10 s Time/Div
x x x 1 1 1 1 1	Manual
x x x 0 1 1 1 1	External
	0F.2 (U1045)
DB7-0	Marker DAC value bits
	0F.3 (U1035)
DB3-DB0	Marker DAC value bits
	9F
x x x 0 x x x x	Poll Bit

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
H. Span Attenuator	
	Span Magnitude (75)
DB7-DB0	Lower 8 bits of 10-bit attenuation code (000 is max attenuation)
	Span Magnitude and Attenuator (76)
1 x x x x x x x	Gain of U3032 is +1
0 x x x x x x x	Gain of U3032 is −1
x 0 0 x x x x x	×1.0 sweep decade attenuator
x 0 1 x x x x x	×0.1 sweep decade attenuator
x 1 0 x x x x x	×0.01 sweep decade attenuator
x x x 0 0 x x x	1st LO main coil output select and calibration
x x x 0 1 x x x	1st LO FM coil output select and calibration
x x x 1 0 x x x	2nd LO output select and calibration
DB2	For future use
DB1, DB0	Upper two bits of attenuation code

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
I. 1st LO Driver	
	1st LO Driver Functions (72)
1 x x x x x x x	Normal span mode
0 x x x x x x x	Max span mode
x 1 x x x x x x	Connect sweep voltage to driver
x 0 x x x x x x	Disconnect sweep voltage to driver
x x 1 x x x x x	Driver off (for degauss)
x x 0 x x x x x	Driver on
x x x 1 x x x x	Filter on at driver output (for unphase-locked narrow spans)
x x x 0 x x x x	Filter off at driver output
x x x x 1 x x x	External mixer disconnected
x x x x 0 x x x	External mixer connected (connected in bands 1–5 if external mixer selected; always connected in higher bands)
x x x x x 1 1 0	Internal mixer bias for Band 1
x x x x x 1 1 0	Internal mixer bias for Band 2
x x x x x 1 1 0	Internal mixer bias for Band 3
x x x x x 1 0 1	Internal mixer bias for Band 4
x x x x x 0 1 1	Internal mixer bias for Band 5
x x x x x 1 1 1	No internal mixer bias selected
	PEAKing Control (7E)
0 x x x x x x x	Steers DB4–DB0 to upper latch
x 0 x x x x x x	Steers DB5–DB0 to lower latch
DB5–DB0	1 sent to DB4 of upper latch disables front-panel PEAKing control; DB3–DB0 of upper latch and DB5–DB0 of lower latch form 10-bit input to DAC for programmable peaking voltage

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
J. Preselector Driver (77)	
0 1 x x x x x x	−conversion, 829 MHz offset
1 0 x x x x x x	+conversion, 829 MHz offset
0 0 x x x x x x	829 MHz IF not used
x x 1 x x x x x	Driver output filter on (for narrow spans)
x x 0 x x x x x	Driver output filter off
x x x 1 x x x x	Preselector switch
x x x 0 x x x x	LPF switch
x x x x 1 x x x	1st LO FM coil not swept
x x x x 0 x x x	1st LO FM coil swept
x x x x x 1 x x	Driver on
x x x x x 0 x x	Driver off (for degauss)
x x x x x x x 1	3rd harmonic 1st LO conversion
x x x x x x x 0	1st harmonic 1st LO conversion
K. CENTER/MKR FREQUENCY Control	
	Control (70)
1 x x x x x x x	1st LO storage gate open
0 x x x x x x x	1st LO storage gate closed
x 0 x x x x x x	Steers DAC data to 1st LO high byte
x x 0 x x x x x	Steers DAC data to 1st LO mid byte
x x x 0 x x x x	Steers DAC data to 1st LO low byte
x x x x 1 x x x	2nd LO storage gate open
x x x x 0 x x x	2nd LO storage gate closed
x x x x x 0 x x	Steers DAC data to 2nd LO high byte
x x x x x x 0 x	Steers DAC data to 2nd LO mid byte
x x x x x x x 0	Steers DAC data to 2nd LO low byte
	DAC Data (71)
DB7–DB0	Data for center frequency DAC(s) steered by control register
	CENTER/MKR FREQUENCY Control Read (F0)
DB7	1st LO DAC stored voltage comparator
DB0	2nd LO DAC stored voltage comparator

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
L. Auxiliary Synthesizer Control (7D)	
DB7–DB4	Synthesizer chip data (D3–D0)
DB2–DB0	Synthesizer chip addresses (A2–A0)
x x x x 1 x x x	VCO enable
x x x x 0 x x x	VCO disable
0 1 0 1 x 1 0 1 0 0 0 0 x 1 1 0 0 0 0 0 x 1 1 1	This section sets R, the reference divider to 5 yielding a 200 kHz reference frequency.
A A A A x 0 0 0	This section sets the value of A from 0 to 31
0 0 0 A x 0 0 1	LSB
N N N N x 0 1 0 0 0 N N x 0 1 1 0 0 0 0 x 1 0 0	This section sets N from 31 to 34 31=1111 32=0000 01 10 33=0001 34=0010 10 10
M. Phase Lock Control	
	Write (73)
1 x x x x x x x	Clocks data on DB0 into a latch
x x 1 x x x x x	Clears the counters
x x x 1 x x x x	Transfers DB0 serial data to control latch outputs
x x x x 1 x x x	Resets the counter output register selector
x x x x x x 1 x	Transfers DB0 serial data to synthesizer N latches
DB6	Gate mode latch
DB2	NVRAM switch latch
DB0	Serial data for control of synthesizer N latches
	Read (F3)—Most Significant Byte
1 x x x x x x x	Error voltage below a preset amount
x 1 x x x x x x	Error voltage above a preset amount
x x 1 x x x x x	Valid count is in counters
DB4–DB0	Upper five bits of counter output; the remaining 16 bits are in the following two bytes

Table 6-10 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
N. Front Panel	
	Reading Data From Switch Encoders (F4)
1 x x x x x x x	CENTER/MKR FREQUENCY down
0 x x x x x x x	CENTER/MKR FREQUENCY up
DB6–DB0	Switch codes (see Figure 7-33 in Section 7)

Table 6-11
AUXILIARY SYNTHESIZER VALUES AS A FUNCTION OF N AND A

N Value	A Value	F_{out} Result
31	8	200.0 MHz
31	9	200.2 MHz
31	10	200.4 MHz
31	11	200.6 MHz
31	12	200.8 MHz
31	13	201.0 MHz
31	14	201.2 MHz
31	15	201.4 MHz
31	16	201.6 MHz
31	17	201.8 MHz
31	18	201.0 MHz
31	19	202.2 MHz
31	20	202.4 MHz
31	21	202.6 MHz
31	22	202.8 MHz
31	23	203.0 MHz
31	24	203.2 MHz
31	25	203.4 MHz
31	26	203.6 MHz
31	27	203.8 MHz
31	28	204.0 MHz
31	29	204.2 MHz
31	30	204.4 MHz
31	31	204.6 MHz
32	0	204.8 MHz
32	1	205.0 MHz
32	2	205.2 MHz
32	3	205.4 MHz
32	4	205.6 MHz
32	5	205.8 MHz
32	6	206.0 MHz

Table 6-11 (cont)

N Value	A Value	F_{out} Result
32	7	206.2 MHz
32	8	206.4 MHz
32	9	206.6 MHz
32	10	206.8 MHz
32	11	207.0 MHz
32	12	207.2 MHz
32	13	207.4 MHz
32	14	207.6 MHz
32	15	207.8 MHz
32	16	208.0 MHz
32	17	208.2 MHz
32	18	208.4 MHz
32	19	208.6 MHz
32	20	208.8 MHz
32	21	209.0 MHz
32	22	209.2 MHz
32	23	209.4 MHz
32	24	209.6 MHz
32	25	209.8 MHz
32	26	210.0 MHz
32	27	210.2 MHz
32	28	210.4 MHz
32	29	210.6 MHz
32	30	210.8 MHz
32	31	211.0 MHz
33	0	211.2 MHz
33	1	211.4 MHz
33	2	211.6 MHz
33	3	211.8 MHz
33	4	212.0 MHz
33	5	212.2 MHz
33	6	212.4 MHz
33	7	212.6 MHz
33	8	212.8 MHz
33	9	213.0 MHz
33	10	213.2 MHz
33	11	213.4 MHz
33	12	213.6 MHz
33	13	213.8 MHz
33	14	214.0 MHz
33	15	214.2 MHz
33	16	214.4 MHz
33	17	214.6 MHz
33	18	214.8 MHz
33	19	215.0 MHz
33	20	215.2 MHz
33	21	215.4 MHz
33	22	215.6 MHz
33	23	215.8 MHz

Table 6-11 (cont)

N Value	A Value	F_{out} Result
33	24	216.0 MHz
33	25	216.2 MHz
33	26	216.4 MHz
33	27	216.6 MHz
33	28	216.8 MHz
33	29	217.0 MHz
33	30	217.2 MHz
33	31	217.4 MHz
34	0	217.6 MHz
34	1	217.8 MHz
34	2	218.0 MHz
34	3	218.2 MHz
34	4	218.4 MHz
34	5	218.6 MHz
34	6	218.8 MHz
34	7	219.0 MHz
34	8	219.2 MHz
34	9	219.4 MHz
34	10	219.6 MHz
34	11	219.8 MHz
34	12	220.0 MHz

Front-Panel Registers

Writing to register 74 loads data into shift registers that drive all the lights on the front panel, including the one for the crt graticule. Four 8-bit shift registers store the data, requiring eight writes of four bits each time (one bit for each register) to update the front-panel lights. Table 6-12 shows the order that data is entered to control the lights. A 0 turns on the light (except in the case of the crt graticule), and a 1 turns off the light.

Table 6-12
FRONT-PANEL REGISTERS
Writing Data to Shift Registers for Lights (74)
DB3=1 — initializes encoder at power up

Write Number	DB7	DB6	DB5	DB4	DB2	DB1	DB0
A	not used	not used	ΔF	SPAN/DIV	UNCAL	EXT	SAVE A
B	not used	not used	not used	MAX SPAN	AUTO RES	INT	VIEW A
C	THRESHOLD	not used	FREQ START/STOP		MIN NOISE	FREE RUN	VIEW B
D	BANDWIDTH	not used	not used	SHIFT	FREQUENCY	SINGLE SWEEP	B−SAVE A
E	SIGNAL TRACK	not used	READOUT	not used	2 DB/DIV	LINE	NARROW
F	not used	not used	BASELINE CLIP	ADDRESSED	10 DB/DIV	READY	WIDE
G	PULSE STRETCH	not used	Δ MKR	REF LVL	RESET TO LOCAL	FINE	LIN
H	PLOT	not used	not used	MAX HOLD	ZERO SPAN	GRAT ILLUM	TUNE CF/MKR

PROGRAM FOR MOVING STORED DATA FROM THE SPECTRUM ANALYZER TO TAPE AND RETURNING IT TO MEMORY

If either the Memory or GPIB boards are removed from the instrument, data stored in memory will be lost because the back-up battery on the GPIB board is disconnected. A Tektronix 4041 Computer, connected over the GPIB bus to the spectrum analyzer, will move this data to a tape and back into memory using the following program.

```
100  Integer a1,s1,t1,w1,i,v,y,z,v1
110  Print "Spectrum Analyzer Address is: ";
120  Input a1
130  Print
140  Print #a1:"RQS OFF"
150  Print "Save memory on tape? ";
160  Input b$
170  B$=seg$(b$,1,1)
180  If b$="y" or b$="Y" then goto 2000
190  Print
200  Goto 1000

1000 ! This routine moves data from TAPE to the SPECTRUM ANALYZER
1010 Print "Displays and Settings are on the following data files"
1020 Print "(3060 x 9 for displays, 1020 x 10 for settings)"
1030 Print
1040 Dir
1050 Print
1060 Print "Enter number of first data file 'FIL' :";
1070 Input t1
1080 Gosub 9000
1090 Print "Write over all Displays and Settings (0),"
1100 Print "Or write only in blank ..... memory (1):";
1110 Input y$
1120 If y$="0" or y$="1" then goto 1150
1130 Print """0"" or ""1"", Please: ";
1140 Goto 1110
1150 Y=val(y$)
```

```
1160 Delete var i$
1170 Dim i$ 700
1180 Print #a1:"SET?"
1190 Input #a1:i$
1200 W1=0
1210 Print #a1:"BVIEW OFF"
1220 Print
1230 Print
1240 For i=1 to 9
1250   Gosub 8000
1260   Gosub 6000
1270   If z=0 then goto 1300
1280   Print w1;"= Waveform from Data File FIL";t1
1290   Goto 1310
1300   Print w1;"= ..... not written. FIL";t1;"  not used."
1310   W1=w1+1
1320   T1=t1+1
1330   Next i
1340 S1=0
1350 Print
1360 Print
1370 Print
1380 For i=1 to 10
1390   Gosub 5000
1400   If z=0 then goto 1430
1410   Print s1;"= Settings from Data File ";t1
1420   Goto 1440
1430   Print s1;"= ..... not written. FIL";T1;"  not used"
1440   S1=s1+1
1450   T1=t1+1
1460   Next i
1470 Print #a1:i$
1480 Print
1490 Print
1500 Print
1530 Print
1540 Print "*** FINISHED ***"
1550 Goto 10000

2000 ! This routine moves data from the SPECTRUM ANALYZER to TAPE
2010 Delete var i$
2020 Dim i$ to 700
2030 Print #a1:"SET?"
2040 Input #a1:i$
2050 Dir
2060 Print
2070 Print "WARNING! This could overwrite existing files!"
2080 Print "Enter the Number of the last tape file: ";
2090 Input t1
2100 Gosub 9000
2110 Print
2120 Print
2130 Print #a1:"BVIEW OFF"
2140 W1=0
2150 For i=1 to 9
2160   Gosub 3000
2170   Gosub 7000
2180   If z=0 then goto 2210
2190   Print w1;"= Waveform sent to File FIL";t1
2200   Goto 2220
2210   Print w1;"= ..... skipped over. FIL";t1;" is empty"
```

```
2220   W1=w1+1
2230   T1=t1+1
2240   Next i
2250 Print #a1:i$
2260 ! Settings are sent to tape
2270 S1=0
2280 Print
2290 Print
2300 Print
2310 For i=1 to 10
2320   Gosub 4000
2330   If z=0 then goto 2360
2340   Print s1;"= Settings sent to File FIL";t1
2350   Goto 2370
2360   Print s1;"= ..... skipped over. FIL";t1;" is empty."
2370   S1=s1+1
2380   T1=t1+1
2390   Next i
2400 Print #a1:i$
2410 Print
2420 Print
2430 Print "*** FINISHED ***"
2440 Goto 10000
3000 ! Acquire Waveform and Settings.
3010 ! X9 is 500 point waveform, l$ is lower readout,
3020 ! m$ is upper readout, and e$ is an error message
3030 Delete var e$,h$,l$,m$,x9
3040 Z=0
3050 Dim h$ to 1100
3060 Integer x9 (1000)
3070 Dim l$ to 50,m$ to 50
3080 Print #a1:"SAVEA OFF;DRECAL A:",w1
3090 Print #a1:"ERR?"
3100 Input #a1:e$
3110 E$=seg(e$,5,2)
3120 If e$<>"62" then goto 3180
3130 V=0
3140 X9=0
3150 M$=""
3160 L$=""
3170 Goto 3280
3180 V=1
3190 Print #a1:"UPRDO?"
3200 Input #a1:m$
3210 Print #a1:"LORDO?"
3220 Input #a1:l$
3230 M$=seg$(m$,8,40)
3240 L$=seg$(l$,8,40)
3250 Print #a1:"WFM WFID:A,ENCDG:BIN;CURVE?"
3260 Input using "fa,+8%" dels "," #a1:h$,x9
3270 Z=1
3280 Return

4000 ! Remove memory settings (S$) from SPECTRUM ANALYZER
4010 Z=0
4020 Delete var s$
4030 Dim s$ to 700
4040 Print #a1:"RECALL ";s1
4050 Print #a1:"ERR?"
4060 Input #a1:e$
4070 E$=seg$(e$,5,2)
```

```
4080 If e$<>"62" then goto 4120
4090 V1=0
4100 S$="NULL"
4110 Goto 4170
4120 Print #a1:"SET?"
4130 Input #a1:s$
4140 Print #a1:"RQS OFF"
4150 V1=1
4160 Z=1
4170 Open #100:"FIL"&str$(t1)&"(OPE=REP,SIZ=1020)"
4180 Print #100:v1,s$
4190 Close 100
4200 Return

5000 ! Retrieve taped Settings (S$) and send to memory locations (S1)
5010 Z=0
5020 Delete var s$
5030 Dim s$ to 640
5040 Open #100:"FIL"&str$(t1)&"(ope=old)"
5050 Input #100:v1,s$
5060 If v1=0 then goto 5150
5070 If y=0 then goto 5120
5080 Print #a1:"RECALL ";s1;";RQS OFF;WAIT;ERR?"
5090 Input #a1:e$
5100 E$=seg(e$,5,2)
5110 If e$<>"62" then goto 5150
5120 Print #a1:s$
5130 Print #a1:"STORE ";s1;";RQS OFF"
5140 Z=1
5150 Close 100
5160 Return

6000 ! Send waveform (X9) & readouts (M$,L$) to memory location (W1)
6010 Z=0
6020 If v=0 then goto 6180
6030 If y=0 then goto 6080
6040 Print #a1:"SAVEA OFF;DRECAL A:";w1;";ERR?"
6050 Input #a1:e$
6060 E$=seg$(e$,5,2)
6070 If e$<>"62" then goto 6180
6080 Print #a1:"WAIT;TRI?"
6090 Input #a1:h$
6100 Print #a1:"RDOUT '";m$;"'"
6110 Print #a1:"RDOUT '";l$;"'"
6120 Print #a1:"WFM WFID:A,ENCDG:BIN;SIG;SAVEA ON"
6130 Wbyte atn(mta,32+a1),x9,eoi
6140 Wbyte atn (unt,unl)
6150 Print #a1:"DSTORE A:",w1
6160 Print #a1:h$
6170 Z=1
6180 Return

7000 ! Store readouts (M$,L$), and waveforms (X9) on TAPE File (T1)
7010 Open #100:"FIL"&str$(t1)&"(OPE=REP,SIZ=3060)"
7020 M$=m$
7030 L$=l$
7040 Print #100:v
7050 Print #100:m$
7060 Print #100:l$
7070 Print #100:x9
7080 Close 100
7090 Return
```

```
8000 ! Retrieves readouts (M$, L$), and waveform (X9) from TAPE
8010 ! From selected TAPE File (T1)
8020 Open #100:"FIL"&str$(t1)&(ope=old)"
8030 Delete var x9,m$,l$
8040 Integer x9 (1000)
8050 Dim m$ to 50,l$ to 50
8060 Input #100:v
8070 Input #100:m$
8080 Input #100:l$
8090 Input #100:x9
8100 Close 100
8110 Return

9000 ! This routine shows the contents of Memory displays and settings
9010 Print "Display Memory"
9020 Print "--------------"
9030 Print #a1:"RQS OFF"
9040 Delete var s$
9050 Dim s$ to 660
9060 Print #a1:"SET?"
9070 Input #a1:s$
9080 W1=0
9090 For i=1 to 9
9100   Print #a1:"SAVEA:OFF;DRECAL A:";w1
9110   Print #a1:"ERR?"
9120   Input #a1:e$
9130   E$=seg$(e$,5,2)
9140   if e$="62" then goto 9170
9150   Print w1;"= Waveform"
9160   goto 9180
9170   Print w1;"= ....."
9180   W1=w1+1
9190   Next i
9200 ! NOTE: "RECALL" may recall a RQS-ON
9210 ! state, so this must be turned off again by RQS OFF
9220 Print
9230 Print "Settings Memory"
9240 Print "----------------"
9250 S1=0
9260 For i=1 to 10
9270   Print #a1:"RECALL ";s1;";RQS OFF;WAIT"
9280   Print #a1:"ERR?"
9290   Input #a1:e$
9300   E$=seg$(e$,5,2)
9310   If e$="62" then goto 9340
9320   Print s1;"= Settings"
9330   Goto 9350
9340   Print s1;"= ....."
9350   S1=s1+1
9360   Next i
9370 Print
9380 Print #a1:s$
9390 Return
10000 End
```

THEORY OF OPERATION

This section describes the spectrum analyzer circuitry. The section begins with a functional description of the major circuit blocks. This is followed by more detailed descriptions of the circuitry within each block.

While reading these descriptions, refer to the corresponding block or schematic diagram in Volume 2 of the Service Manual. The description titles use the diagram names and numbers for easy reference.

The Functional Block diagram, located at the front of the Diagrams section in Volume 2, shows how the major sections in the instrument relate and the paths of most major signals. Block diagrams showing more detail of these main sections follow the Functional Block diagram. Circuit schematic diagrams follow the major block diagrams.

Adjacent to each schematic is a third level of block diagram, a circuit board parts location illustration, and cross-reference look-up tables. The third level block diagram shows the function of the components shown on the schematic. The parts location illustration and look-up tables aid in finding components on either the schematic or circuit board.

FUNCTIONAL AND GENERAL DESCRIPTION

What It Does

The spectrum analyzer accepts an electrical signal as its input and displays the signal's frequency components on a crt. Signals can be applied directly to the RF INPUT.

The display of the input signal appears on the crt as a graph where the horizontal axis is frequency and the vertical axis is amplitude. The display can be plotted, if desired, by connecting a chart recorder through rear-panel connectors. The display can also be transmitted digitally via a IEEE 488 General Purpose Interface Bus (GPIB) to a GPIB-compatible plotter.

The spectrum analyzer can be operated either manually with front-panel controls and switches, or remotely via the GPIB using a straightforward language format.

How It Works

The Spectrum Analyzer operates as a swept, narrow-band receiver. The crt beam moves horizontally as a range of frequencies is spanned or swept. When a frequency component of an input signal is detected, the beam is deflected vertically as a function of input power at that frequency. The center frequency of each span is set by the CENTER FREQUENCY control or FREQUENCY entry via a Data Entry keyboard. The frequency range of each span is set by the FREQ SPAN/DIV control or settings. The power level, represented by the top of the screen, is set by either the REFERENCE LEVEL control or the Data Entry keyboard.

First, Second, and Third Converters

Swept-frequency analysis is achieved by a triple-conversion, superheterodyne technique. Each of three frequency converters consist of a mixer, a local oscillator, and appropriate filters. Only one frequency is converted in each mixer to pass through band-pass filters to the detector. This frequency can be changed by changing the local oscillators frequency in any of the converters.

The first converter, usually referred to as the front end, converts the input signal frequency to an intermediate frequency (IF) of either 829 MHz or 2072 MHz, depending on which band is in use. The internal mixer converts signals from 50 kHz to 21 GHz. A preselector or low-pass filter is inserted in the signal path to reduce unwanted signals or images and spurious responses.

One of two second converters is selected automatically for each band so the input frequency range does not overlap the first IF frequency. Each second converter has its own local oscillator (LO), mixer, and filters. Both down-convert the signal to 110 MHz which is sent to the third converter.

The third converter amplifies the 110 MHz IF signal and converts it to the final intermediate frequency of 10 MHz. The third converter passes the signal to the main IF section for processing and detection.

IF Section

This section processes the signal for frequency resolution. Three functions are performed here:

1. Weak signals can be amplified, by switchable amplifiers, so the dynamic display range (vertical window) is shifted up or down. The REFERENCE LEVEL selects the gain and input RF attenuation to frame this window between the top of the display screen or reference level, in dBm or volts, and the bottom of the display.

2. The signal is processed through one of several band-pass filters that can be selected by the RESOLUTION BANDWIDTH control. In the auto mode the microcomputer will select the best combination of bandwidth and sweep time for the selected span, unless overridden by the operator.

3. The signal is amplified by a logarithmic amplifier then detected. The output from the detector is a voltage that corresponds to the signal strength in decibels. The detector output is then sent to the vertical channel of the display section to drive the vertical axis of the crt and display the signal.

Display Section

The display section drives the X,Y, and Z axis of the crt display. Vertical deflection of the beam is increased as the output of the amplitude detector increases. The horizontal position of a signal is controlled by the frequency control section and corresponds to the frequency of the detected signal. As the spectrum analyzer spans from low to high frequencies during its analysis, the beam is swept from left to right. When the spectrum analyzer tunes through a signal frequency, a vertical deflection shows the strength of the signal. This signal is therefore displayed at a position on the span that corresponds to its frequency, or, the display is one of amplitude as a function of frequency.

The video amplifier scales the output of the detector for vertical deflection in dB/div or performs a log/linear conversion, depending on the vertical display mode. The video processor filters the video if either the wide or narrow filter is selected.

The display section also drives the crt readout to show control settings. This readout is based on data from the microcomputer which is reading the settings of the front panel controls or data on the GPIB bus.

The sweep is usually fast enough so the display is flicker-free, but at times the sweep must be slowed below the flicker rate. With digital storage the display can be recorded and refreshed at a flicker-free rate. The display data stored in the spectrum analyzer's memory can be transmitted through the GPIB.

Frequency Control Section

The spectrum analyzer sweeps through a frequency range that is centered about a frequency set by the frequency control section. The CENTER FREQUENCY control sets the center frequency of either the 1st or 2nd local oscillator.

The output of a sweep generator is scaled by a span attenuator to sweep a range or span of frequencies either side of center. The output of the span attenuator drives the 1st LO for wide spans and the 2nd LO for narrow spans. The output sweep also deflects the crt beam across the horizontal axis as the local oscillators are swept so the display is a spectrum of frequency versus power.

In Option 01 instruments, the frequency control section also tunes the preselector so it tracks the signal frequency being detected over the 1.7 to 21 GHz range.

Counter and Phase Lock Section

The Counter, Harmonic Mixer, and Auxiliary Synthesizer form the nucleus of the frequency control hardware. Both the 1st LO and 2nd LO frequencies are controlled via the firmware based control loop. Data from the Counter is used as feedback to control the oscillator frequency. Accurate signal frequency measurement is also possible by counting the frequency of the 3rd IF.

The Phase Lock system stabilizes the 1st LO frequency. This minimizes display jitter and increases resolution.

Digital Control Section

Operational modes and internal functions of the spectrum analyzer are selected and controlled directly from the front panel or remotely controlled from an external controller through a GPIB connector. This connector interfaces to an instrument microcomputer through the GPIB. The modes and functions that are selected are processed and activated by the instrument master microcomputer which talks and listens to all circuits over the instrument bus.

Front panel control and selector data is processed by a front panel CPU that interfaces with the master microcomputer over the instrument bus. The master microcomputer receives and sends all of its information over the instrument bus to the internal circuits. It communicates with other instruments through the GPIB connector or through the Accessories Interface to the

Accessories connector located on the rear panel. Control language corresponds to front-panel nomenclature of the Spectrum Analyzer.

Power Supply Section

The power supply section provides regulated dc power and forced air cooling for all circuits within the instrument. The switching supply is capable of providing regulated voltages over a wide range of input line frequencies and voltages. The cooling system consists of an intake on the bottom of the case, air passages within the instrument, a fan, and a rear panel exhaust. Air is routed to all sections of the instrument in proportion to the heat generated by circuits within those sections. Internal temperature variations are minimized to provide reliable operation.

Other Sections

Interconnections between assemblies are made through a common Mother board. Most circuit board assemblies plug into the top side of the Mother board. Assemblies on the RF deck are connected to the bottom side of the Mother board through cables and connectors.

DETAILED DESCRIPTION

The following description is arranged by sections or systems; such as 1st Converter, 2nd Converter, etc., followed by circuit analysis of the circuits within that section. Each system or section is introduced with a description of the system using the section block diagram found in the Diagrams section of the Service Manual, Volume 2. This is followed by a description of each circuit board or major circuit within the system. The appropriate block or schematic diagram number is included in the text headings for each section or part.

1ST CONVERTER SECTION (Diagram 2)

The 1st Converter consists of the 0-60 dB Step Attenuator, Preselector circuits (Option 01 only), Mixer, 1st LO, Power Divider, 2.072 GHz Directional Filter, Diplexer, and two 4.5 GHz Low-Pass Filters. External circuits that control or drive the assemblies within the 1st Converter are; the Preselector Driver (Option 01 only), 1st LO Driver, Counter and Phase Lock system, and the RF Interface board.

The 1st Converter converts the incoming RF signals to the 1st IF. Incoming signals are applied through a calibrated 0-60 dB decade attenuator (AT10) to the 1st Mixer (A12), or for Option 01 instruments, to the Preselector circuits and then to the 1st Mixer.

In instruments with the Preselector circuits (Option 01), signals in band 1 (50 kHz to 1.8 GHz) route through a Limiter (A10) and 1.8 GHz Low-Pass Filter (FL10) to the mixer; and signals in bands 2 through 5 (1.7 to 21 GHz) route through a tunable Preselector (FL12) and a 3 dB Attenuator (AT11) to the mixer.

The RF signals are mixed with the output from a tunable local oscillator to generate products at one of two intermediate frequencies, depending on the band in use. The 1st Mixer output goes to Directional Filter FL16 through W125. In Option 07 instruments Transfer Switch S13 select between the 50 Ω and 75 Ω inputs.

The directional filter separates the 2072 MHz and 829 MHz intermediate frequencies for the 2072 MHz 2nd Converter (A18) or 829 MHz 2nd Converter (A23). The 2072 MHz IF is applied through a 4.5 GHz Low-Pass Filter (FL11) to the 2072 MHz 2nd Converter. The 829 MHz IF is fed through a Diplexer (A14) and another 4.5 GHz Low-Pass Filter (FL15) before it is applied to the 829 MHz IF stages.

The spectrum analyzer uses two intermediate frequencies (2072 MHz and 829 MHz) to prevent baseline rise caused by local oscillator feedthrough and crossover of intermodulation products. The 2072 MHz IF is selected for bands 1 and 5. The 829 MHz IF is selected for bands 2-4.

RF Interface Circuits (Diagram 28)

The RF interface circuits receive instruction from the microcomputer and produce control signals for the RF Attenuator, the Transfer Switch, and the IF Select. These RF control circuits are located on the Z-Axis/RF Interface board and their operation is described under the Z-Axis board part of the Display section.

1st Converter (Diagram 12)

RF Input

The RF input signal goes through a 0-60 dB Step Attenuator (AT10) consisting of relay-controlled 10 dB, 20 dB, and 30 dB sections. The relays are actuated by control signals from the RF Interface circuit. The signal flows from the step attenuator to the 1st mixer, or for instruments with a preselector (Option 01), through the preselector circuits.

Preselector Circuits (Option 01 only)

Coaxial switches S11 and S12 are relays that select either the low-pass filter (FL10) and Limiter (A10) or the Preselector and 3 dB attenuator (AT11) for the RF signal path. The relay coils are driven by circuitry on the Preselector Driver board. The low-pass filter path is used for band 1, and the Preselector path is used for bands 2 through 5.

The 2 GHz Limiter (A10) operates from 100 kHz to 2 GHz. It has a linear two-port transfer characteristic of unity (-1 dB) until the input exceeds +5 dBm. Above this point, the internal detector diodes conduct, reflecting part of the RF input energy back to the source. As the input level rises, the Limiter reflects more signal, limiting the amount that can pass through the mixer, thus protecting the mixer from being overdriven.

The 1.8 GHz Low-Pass Filter (FL10) strips the incoming signal of any frequency components above 1.8 GHz and passes all frequency components below

1.8 GHz to Filter Selector switch S12.

The Preselector (FL12) is a 1.7-18 GHz Yttrium-Iron-Garnet (YIG) filter that provides high selectivity and image frequency rejection. Tuning current, which is near 500 mA at 21 GHz, is provided by the Preselector Driver (A42) circuits. The Preselector operates on bands 2, 3, 4, and 5. Because the Preselector is sensitive to output load impedance, a 3 dB Attenuator (AT11) is inserted between the Preselector output and one port of the Filter Select switch to help isolate output loading.

1st Mixer

The 1st Mixer (A12) circuit consists of a single balanced mixer, a coupler, and a 90° phase shifter. A balanced mixer inherently has less conversion loss compared to an unbalanced mixer, and local oscillator feedthrough to the RF port is minimized. The local oscillator input is split through a broad-band multi-section coupler whose outputs are equal in power but 90 degrees out of phase. An additional 90 degree phase shift is cascaded with the appropriate signal to create a 180 degree phase difference that is applied across a pair of series-connected Schottky diodes. The result is that the diodes are alternately switched on and off as the local oscillator cycles.

The node between the two diodes is isolated from the 1st LO input by about 30 dB so the RF input is applied to this node. The blocking capacitor at the input connector permits broadband signal application from the RF port, while blocking the dc diode bias from getting to the RF port and the spectrum analyzer input. Mixer bias is supplied from the 1st LO Driver board via the 829 MHz IF circuits, 4.5 GHz Filter, Diplexer, and Directional Filter. Bias return is through assembly A11 to ground.

Excluding losses in the IF filtering circuitry, the fundamental conversion loss of the 1st Converter is about 14 dB, and the third harmonic conversion loss is about 24 dB. The Schottky diodes are mounted in a mixer sub-assembly (A12A1) so that they can be easily replaced.

1st Local Oscillator

The 1st LO (A16) is a YIG (Yttrium-Iron-Garnet) oscillator that has a tuning range of 2.072 to 6.4 GHz. The oscillator assembly includes the interface circuit board that couples operating and tuning voltages from the 1st LO Driver, Span Attenuator, and Error Amplifier circuits to the oscillator.

The +15 V_1 voltage provides operating bias for the oscillator. The supply is protected and decoupled by VR1010, C1016, and L1011. The second supply, +15 V_2, is not used in this instrument. VR1018 and VR1019 clamp transient voltages from the tune voltage coil. It also protects the driving circuits from the transients induced when degaussing.

When the FM coil is used to sweep the oscillator, relay K1015 closes and couples C1012 and C1014 across the tune coil. The capacitors lower the noise bandwidth of the main coil driving circuit while the FM coil is in operation. The heater provides temperature stability.

Power Divider

The Power Divider (A13) splits the output of the 1st LO (YIG oscillator) to isolate the 1st Mixer from the 1st LO OUTPUT front-panel connector. Basically, the Power Divider is two multi-section directional couplers that are cascaded to produce two ports having equal power. The isolation between output ports is 15 dB or more at the operating frequency. The Power Divider also provides an improved load to the local oscillator.

Directional Filter

The Directional Filter (FL16) couples the 2072 MHz signal to the 2nd Converter via low-pass and band-pass filters FL11 and FL14. As mixing products pass through FL16, they induce a selected current into a one-wavelength distributed ring, which couples the 2072 MHz IF signal out to the low-pass filter FL11. The remainder of the intermodulation products pass on through since the ring is excited only with 2072 MHz signals. The bandwidth of this Directional Filter is approximately 45 MHz. The unfiltered signals are passed on to the Diplexer.

2072 MHz IF Filters

The 2072 MHz signal, from the Directional Filter, passes through a 4.5 GHz Low-Pass Filter (FL11). The signal is then sent through a 15 MHz band-pass filter (FL14) which rejects intermodulation products either side of the 2072 MHz IF.

Diplexer and Filter

The Diplexer (A14) passes the 829 MHz IF signal from the mixer output through a low-pass filter (FL15) to the 2nd Converter. The Diplexer and Directional Filter provide a broadband impedance match to the 1st Mixer IF port. This match contributes to the overall flatness and frequency response of the analyzer.

2ND CONVERTER SECTION (Diagram 3)

Two 2nd Converter systems are used in the spectrum analyzer. One converts 2072 MHz to 110 MHz and the other converts 829 MHz to 110 MHz. The converter used is determined by the frequency band being conveted. The IF selection for each band is shown in Table 7-1 along with the band frequency range and the local oscillator frequency range. Two 2nd IFs are used by the analyzer for the following reasons:

- If the 1st IF is included in the frequency band being converted, it is possible for some input signals to pass un-converted through the 1st Converter to the 2nd Converter, appearing at the 1st IF. The resulting spurious signal would cause the baseline level on the screen to rise and obscure real signals. Using two 2nd converters avoids the problem by using a 1st IF not in the band being converted.

- With two IF'S, IF feedthrough in band 2 and higher order spurs in bands 3 and 4 can be eliminated.

- Because of the limited tuning range of the 719 MHz LO, the lower IF cannot be used above band 4.

The 2072 MHz 2nd Converter mixes the 2072 MHz from the 1st Converter with the output from a 2182 MHz phase-locked 2nd local oscillator. This local oscillator is swept and tuned over a 4 MHz range. The 2072 MHz input IF signal is passed through a four-cavity band-pass filter (FL14) to allow only the 2072MHz 1st IF signal to pass through and prevent other signals, generated within the 2nd Converter, from getting back to the 1st Converter. A diode mixer combines the 2072 MHz IF input and the local oscillator signals to generate the 110 MHz IF output which then passes through a 110 MHz low-pass filter to reject any higher order signals from the mixer.

The 829 MHz 2nd Converter uses a phase-locked voltage controlled oscillator to produce the 719 MHz signal that is mixed with the 829 MHz first IF signal. The swept 2182 MHz 2nd Local Oscillator is used as a reference for the phase locked oscillator. The 719 MHz oscillator can be disabled upon command from the microcomputer in the IF selection process. The phase lock circuit maintains a constant relationship between the two local oscillators as the 719 MHz oscillator is swept and tuned over a 1.33 MHz range. A four section coaxial band-pass filter is used before the mixer to exclude any RF signals other than the desired 829 MHz. Again, a diode mixer is used to mix the 829 MHz input and local oscillator signals to produce the 110 MHz second IF output.

Table 7-1
2ND CONVERTER IF SELECTION

Band	Range	2nd LO Range	1st IF
1	50 kHz-1.8 GHz	2182 ±2.25 MHz	2072 MHz
2	1.7-5.5 GHz	719 ±0.75 MHz	829 MHz
3	3.0-7.1 GHz	719 ±0.75 MHz	829 MHz
4	5.4-18.0 GHz	719 ±0.75 MHz	829 MHz
5	15.0-21.0 GHz	2182 ±2.25 MHz	2072 MHz

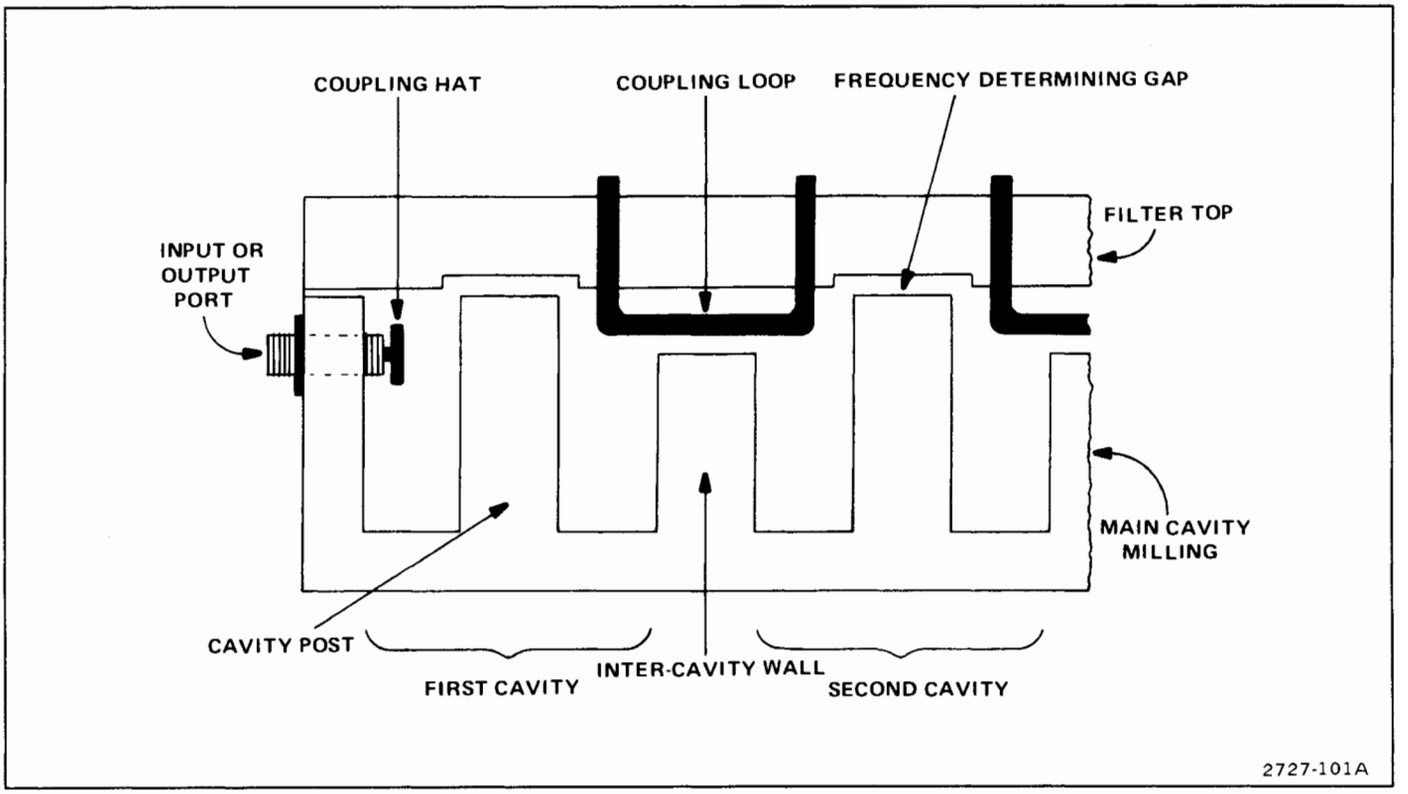


Figure 7-1. Cross section of a four-cavity filter.

Selection between the two 2nd IF signals also takes place within the 829 MHz converter system. A diode switching network connects the active 110 MHz 2nd IF signal to the output to drive the 3rd Converter.

2072 MHz 2ND CONVERTER (Diagram 12)

The 2072 MHz 2nd Converter converts the 2072 MHz signal output from the 1st Converter to 110 MHz for eventual application to the 3rd Converter. The assembly consists of a four-cavity filter connected to a narrow band mixer through an external cable, a 110 MHz low-pass filter, and a mixer-biasing circuit.

Four-Cavity Filter

The four-cavity filter (FL14) is a low-loss narrow-band filter that only passes the 2072 MHz IF signal to the mixer. Any other frequencies are reflected back to the 1st Converter and terminated. In addition, the filter prevents the converter LO and mixer products from entering the 1st Converter.

This filter has a 1 dB bandwidth of 15 MHz and an insertion loss of 1.2 dB. Each end resonator is capacity coupled to external circuits through a coupling hat plugged into a 3 millimeter connector. Intercavity coupling is provided by coupling loops that protrude from the machined filter top. The resonant frequency of each cavity is determined primarily by the depth of a gap in the underside of the filter top, and is fine tuned with a tuning screw on the side of each cavity. All of the tight machining tolerances are confined to the top. Thus, the main cavity milling need not be a high precision part. When properly tuned, using a network analyzer, the filter return loss is greater than 25 dB from either end (in a 50 ohms system). Figure 7-1 shows a cross sectional view of the filter, and Figure 7-2 shows the equivalent electrical circuit.

Mixer Circuit

The mixer circuit consists of a single-balanced, two-diode mixer, a bias circuit for the mixer, a delay line, and a 110 MHz low-pass filter.

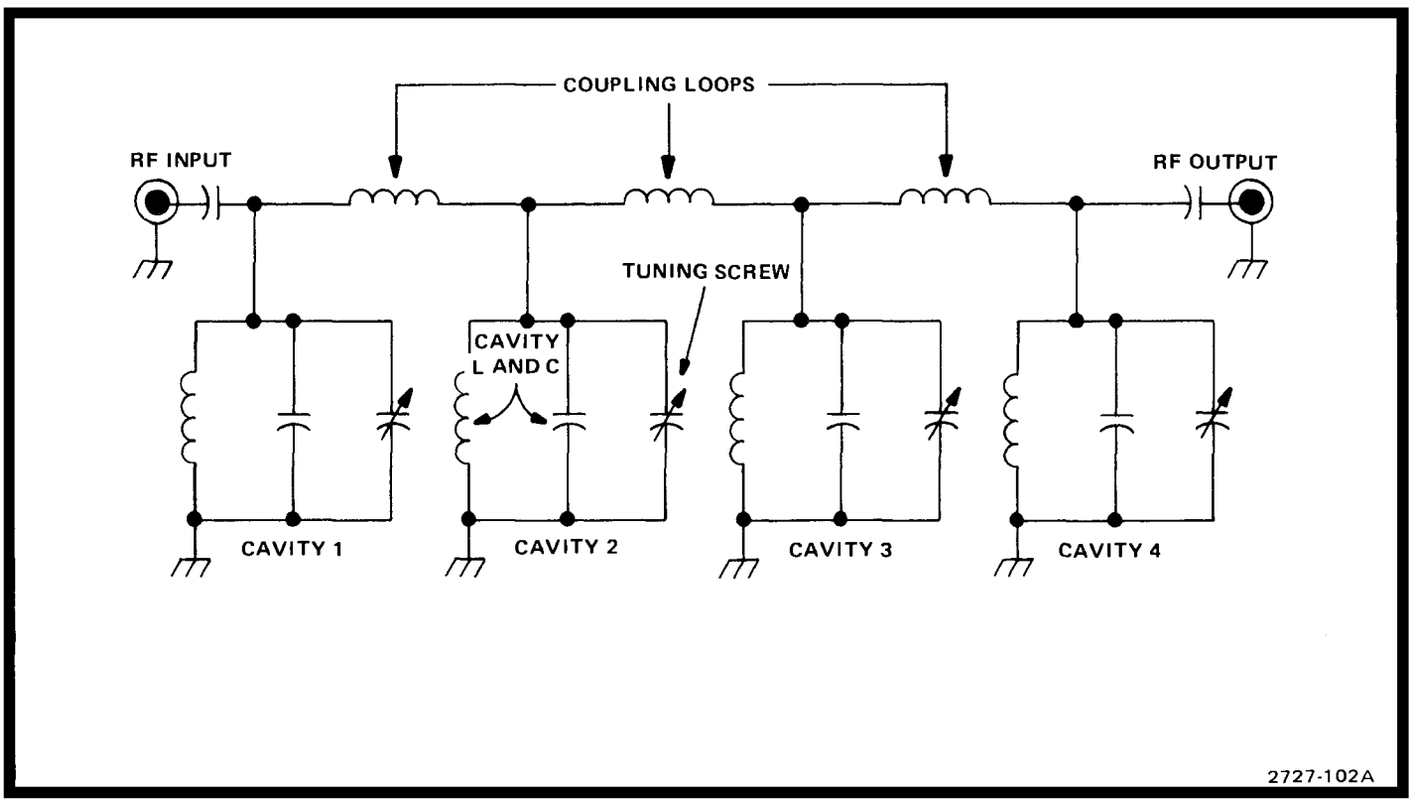


Figure 7-2. Equivalent circuit of the four-cavity filter.

2072 MHz RF from the four-cavity filter (FL14) enters the mixer, where it is switched on and off at a 2182 MHz rate by the the mixer diodes. Both mixer diodes are turned on and off by the 2182 MHz 2nd LO signal. The difference frequency of 110 MHz is separated from the other mixer products by a low-pass filter for use as the IF output. Although the diodes are connected for opposite polarity, both are turned on at the same time because of the 180 degree phase shift delay line in the input path to one of the diodes. Note that the diodes are matched and must be replaced as a pair if one fails.

At the output of the mixer, the two inductors and one capacitor form a low-pass filter that passes unattenuated 110 MHz signal to the 829 MHz 2nd Converter, via coaxial connector P182. Dc-blocking capacitors at the three inputs to the mixer, keep the diode bias from being applied to the RF and local oscillator lines.

The bias circuit, which consists of operational amplifier U1014 and the associated components, establishes the bias for the mixer diodes and also provides the means for effectively switching the mixer off (under control of the microcomputer). When the mixer is active, each diode has approximately 2 mA of forward bias. For this condition, the IF SELECT signal from the Z Axis/RF Interface circuits (applied through feedthrough capacitor C182) is low. This causes the output from U1014A to be at +14 V and the output from U1014B to be −14 V. Diodes CR1014 and CR1018 are thereby reverse-biased. Thus, the series resistances of potentiometer R1019 plus resistor R1014, and potentiometer R1010 plus resistor R1017, provide forward bias to the diodes. The potentiometers are set to balance the bias levels.

In operation where the mixer is not active, the IF SELECT signal is high. This reverses the states of the U1014 outputs and forward- biases diodes CR1014 and CR1018. With these diodes conducting, resistors R1014, R1016, R1017, and R1018 form two voltage dividers that set the reverse bias, to the mixer diodes, at 5 V. This effectively turns the mixer off and attenuates the 110 MHz signal by about 55 dB.

Precision External Cables

The external cable that connects the four-cavity filter output to the mixer RF input (W140) and the external cable that connects the 2nd LO to the mixer LO input (W222) are both critical length cables.

Filter to Mixer RF Input Cable. Several products and harmonics of the local oscillator and RF input frequencies will exit the mixer via the RF input port of the mixer. The image (RF input minus the 2nd LO) and the sum (RF input plus the 2nd LO) are two significant products. There is enough energy in these two signals to warrant efforts to recover that energy.

Only the RF signal at 2072 MHz can pass through the four-cavity filter. Thus, any other signal frequency that is applied to the filter (that is, signals exiting the mixer via the RF port) is reflected back to the mixer by the filter. If the cable between the filter and the mixer is the correct length, the most significant reflected signals (i.e., the image and the sum) can be returned to the mixer in phase and converted into additional energy at the intermediate frequency. This technique is called "image enhancement mixing" and typically improves conversion loss by approximately 3 dB at the design frequencies.

The image frequency, in this instance, is very near the RF frequency. A very sharp cut-off filter is required to pass the RF, yet reflect the image. The four-cavity filter performs this function.

2nd LO to Mixer LO Input Cable. The image and sum products are also present at the LO port of the mixer. These signals leave the mixer via the cable to the 2nd LO and are reflected back to the mixer by the LO .The oscillators resonator appears highly reflective to the image and sum signals because it is tuned to the LO frequency. Again, the length of the cable from the LO to the mixer LO port is adjusted so the image and sum signals are reflected back to the mixer, in the proper phase, for re-conversion to supply additional energy at the IF frequency.

2182 MHz PHASE LOCKED 2nd LO (Diagrams 13 and 14)

The 2182 MHz phase locked 2nd LO assembly contains a tunable microwave oscillator, frequency reference, and phase lock circuitry. A two-section housing contains the circuitry. Microwave circuitry is packaged within the machined aluminum portion of the housing. Low frequency phase lock circuitry is within the mu-metal compartment.

In the microwave or LO portion of the assembly, the 2182 MHz Microstrip Oscillator generates 2182 MHz for the 2nd converters and the 2nd LO internal reference circuitry. The 2200 MHz Reference circuit receives a 100 MHz drive signal from the 3rd converter crystal oscillator and produces 100 MHz harmonics. The 22nd harmonic or 2200 MHz is mixed with 2182 MHz from the microstrip oscillator in the 2200 MHz Reference Mixer circuit. The difference frequency of 18 MHz is then fed to the phase lock side of the module.

A phase/frequency detector, on the 16-20 MHz Phase Lock circuit board, compares the 18 MHz difference frequency with a signal from a linearized varactor tuned, 18 MHz voltage controlled oscillator. The detector output tunes the 2182 MHz Microstrip Oscillator such that the difference frequency exactly matches the frequency of the 18 MHz reference VCO.

Sweep and tune signals from the Span Attenuator and Center Frequency Control circuits tune the 18 MHz VCO. The output voltage from the phase/frequency detector forces the Microstrip Oscillator to tune the same amount.

2182 MHz Microstrip Oscillator (Diagram 14)

This oscillator consists of a printed 1/2 wavelength resonator driven by a common-emitter feedback amplifier (Q1021). The base of Q1021 is capacitively tapped into the resonator. The resonator serves as a tuned phase inverter and impedance transformer, connected between the base and collector of Q1021. Part of the base feedback capacitance is provided by a bendable tab (C1021). This allows fine adjustment of the total feedback. This feedback RF signal is detected, by the base- emitter junction of Q1021, to produce a change in bias voltage that is related to the amount of feedback. The base voltage can be monitored at TP1015 with a high impedance voltmeter without significantly disturbing the oscillator.

The dc collector voltage and current for Q1021 is regulated by an active feedback circuit containing transistor Q2021. Voltage at the junction of R2023 and L2023 is a function of Q1021 collector current. This voltage is sensed by Q2021, which alters the base current to Q1021 thereby regulating the collector current and maintaining +10 Vdc on the resonator. Decoupling and control of bias loop dynamics are provided by C2104. Resistor R2016 swamps the negative base resistance of Q1021 to provide stabilization. Resistor R2015 protects the base- emitter junction of Q1021 from excessive reverse bias in the event the +12 V supply fails.

The oscillator is tuned by varactor diode CR1028, connected to one end of the resonator. Decoupling for the varactor is provided by the low-pass elements in the tune line. Bendable tab C1022 can be used to fine tune the oscillator center frequency.

Three output taps are coupled to the resonator through printed capacitors under the resonator. One output supplies 2182 MHz through a 6 dB attenuator to the Harmonic Mixer in the 829 MHz 2nd Converter. The other two output taps couple LO power through 6 dB attenuators to buffer amplifiers Q1031 and Q1011. The

amplifiers provide approximately +10 dBm to the 2072 MHz 2nd Converter and +8 dBm to the Reference Mixer.

Since the two buffers are nearly identical, only the 2nd Converter buffer is described. Gain is provided by Q1011. Printed elements provide input and output impedance matching. Out-of-band damping is provided by R1011 in series with a 1/4 wavelength shorted stub. Dc is blocked by C1014 and C1011. A 1/4 wavelength open stub is used at the output to reflect one of the 2nd Converter's image frequencies at 4254 MHz (the other buffer does not use nor need this stub). Collector bias for Q1011 is provided through R1012, L1011, the 1/4 wavelength shorted stub, and R1011. The 1/4 wavelength shorted stub is grounded through C2011 (C2011, C1013, and L1011 are also used for decoupling). Collector voltage is determined by divider R1013 and R2013; this controls the dc feedback to the collector-base junction of Q1011. The bias network is decoupled from the RF path by L1014. Diode CR2013 protects the base of Q1011 from excessive reverse bias if the +12 V supply fails.

2200 MHz Reference Board (Diagram 14)

This circuit generates harmonics of the 100 MHz input. The 22nd harmonic or 2200 MHz is used by the Reference Mixer. The input 100 MHz signal is applied through a matching network (consisting of L1034, L1025, C1036, C1029, and C1025) to a differential amplifier (Q1024 and Q2024). The emitters of this amplifier are ac coupled through C2026, reducing low frequency gain and ensuring balanced operation. A snap-off diode (CR2014) is driven by the amplifier, via transformer T2015, to generate multiple harmonics of the 100 MHz signal including the 2200 MHz reference. The output passes through a 3 dB attenuator, for isolation, to the Reference Mixer circuit.

2200 MHz Reference Mixer (Diagram 14)

Signals from the 2200 MHz Reference circuit are filtered by a printed 2200 MHz bandpass filter. Diodes CR1011 and CR1012 are the switching elements of a single-balanced mixer. The microstrip oscillator output is applied to CR1011 and through a 1/2 wavelength delay line to CR1012. The delay line shifts the oscillator signal 180 degrees so both diodes switch together. Mixing the 2200 MHz with the oscillator 2182 MHz signal produces the difference frequency of 18 MHz. This 18 MHz signal is fed through a 37 MHz low-pass filter to the 16-20 MHz phase lock circuit. The low-pass filter prevents unwanted products, such as 82 MHz (product of 2100 MHz and 2182 MHz), from passing into the phase lock circuit.

16-20 MHz Phaselock Board (Diagram 13)

This board contains regulated power supplies, a 16-20 MHz (18 MHz nominal) voltage controlled oscillator with linearizing circuitry, and a phase/frequency detector circuit. Its main function is control of the 2182 MHz Microstrip Oscillator. The entire circuit board is housed in a magnetic shield to reduce spurious effects of external ac fields. All power supply and control inputs enter the circuit board via feedthrough capacitors in the housing wall. All connections with the microwave circuitry are through feedthrough capacitors C2200 through C2204, in the floor of the housing.

The +15 V, −15 V, and +9 V supply inputs are re-regulated down to +12 V, −12 V, and +5.2 V by regulators using operational amplifiers. IC U2025 provides a stable −6.2 V reference that is filtered by R2018 and C2015 and amplified by U2016B to produce the −12 V supply. IC U2016B uses emitter-follower Q2024 to increase the current capability of the supply. Resistor R2013 ensures sufficient base drive, while collector resistor R2025 reduces power dissipation in Q2024. Diode CR2019 protects the base-emitter junction during power supply shutdown. Feedback resistors R2016 and R2017 set the gain of U2016B and control the −12 V, +12 V, and +5.2 V supply voltages.

The −12 V supply is applied to inverting amplifier U2016A to produce the +12 V supply, and inverting amplifier U1017 to produce the +5.2 V supply. The output circuitry for the +12 V and +5.2 V supplies are similar to the −12 V supply.

Differential amplifier U2072A accepts the 2nd LO sweep voltages. One input senses the sweep voltage while the other input senses the ground potential at the Sweep board. Sweep sensitivity is adjusted by selecting resistor R2070. In wide spans, the sweep signal passes through parallel resistors R2082 and R2083. In narrow spans, R2082 may be switched out by Q2084, which reduces the weep sensitivity by a factor of ten. When the TTL signal to Q2076 is high, Q2076 is turned off, R2086 holds the gate of Q2084 to −15 V, Q2084 is turned off, and R2082 is switched out. This reduces the sweep sensitivity. When the TTL signal is low, Q2076 saturates with the collector slightly above 0 V, Q2084 turns on, and full sweep sensitivity is restored.

Amplifier U2072B accepts the 2nd LO tune voltage. the Tune board senses the ground potential of the 16-20 MHz Phase Lock board and floats the tune voltage. Tune sensitivity is adjusted by selecting resistor R2072.

The sweep and tune signals combine at the summing node input of a non-linear shaping amplifier. The non-linearity of the shaping amplifier compensates for the non-linear tuning of the reference oscillator varactor to give a linear tuning characteristic from 16 to 20 MHz. The shaping function is produced by a resistor-diode

array in the feedback loop of inverting amplifier U1073A.

All of the amplifier's feedback is through R1072 when the output swings to the negative limit. As the output voltage swings less negative, it sequentially passes the tap-point voltages of a series of voltage dividers connected between 0 V (the summing node at pin 12) and a negative reference set by Q1047. If the output becomes positive with respect to a given divider tap, a corresponding diode in U2059 forward biases and connects the output to the tap, which creates additional feedback through one leg of the divider to the summing node. This causes R2051, then R2052, then R2053 (as so on through R2056) to be connected in parallel with R1072 as the amplifier output becomes less negative. This progressively increases the feedback, which causes the gain of U1073A to decrease.

Another series of dividers connected between the amplifier's output and a negative voltage reference causes the diodes in U1059 to sequentially conduct as the output becomes more positive. Resistors R2060, then R2061, then R2062 (as so on through R2065) are sequentially added in parallel with the existing feedback. Soft diode turn-on characteristics and a large number of breakpoints result in smooth gain changes. The nonlinear amplifier's voltage-gain characteristic is controlled by the shaper reference voltage, which is set by R2049. Altering R2049 will make the breakpoints either closer together or further apart; in practice, this resistor is selected to correct the tolerance variations of the 18 MHz VCO varactor.

The forward drop of the shaper diodes gives U1073A an offset voltage. Temperature correction diodes CR1086, CR1087, and CR1088 correct this offset over a wide temperature range by summing a correction voltage through R1074. These diodes also compensate for the lack of series diode drop across R1072 and eliminate offsets at the summing input of U1073B. Selecting R1070 provides fine adjustment of the VCO's center frequency. IC U1073B is an inverting amplifier that increases the shaper output voltage swing to a level that can control the varactor of the 18 MHz VCO.

A differential amplifier with well-defined limiting characteristics is used for the 18 MHz VCO. Emitter degeneration is used to control loop gain. Transistors Q2096 and Q2087 form the differential pair of transistors, with the emitters coupled through C2091. Transformer T2092 provides ac feedback for the collector-base junction of Q2096 and also creates the majority of the resonator inductance. The total resonator inductance may be adjusted by trying different combinations of connections between taps on inductor T1091 and transformer T2092. These taps allow coarse adjustment of the VCO center frequency. The capacitor of the resonator is varactor CR1089. Capacitor C1088 completes the resonator ac path and acts as a dc block, which allows a bias voltage to be impressed on the varactor. Resistor R2092 and capacitor C2090 damp the Q2096 collector, which prevents high-frequency instability in the oscillator. Transistor Q2087 provides a buffered oscillator output.

A discrete two-stage amplifier provides an unsaturated voltage gain of approximately 43 dB for the 18 MHz signal from the 2200 MHz Reference Mixer board. Transistor Q1041 is the common-emitter first stage while Q1042 and Q1043 form the differential second stage. The differential stage limits the output swing to 0.8 V to prevent over- driving the following ECL circuitry. Dc bias is maintained by Q1041, which has dc collector-base feedback via R1046 and the R1043/R1048 voltage divider. Transistor Q1043 receives its base bias through R1042. Each transistor operates with 5 mA of quiescent current.

ECL line receivers U2041D and U2041B amplify and buffer the 18 MHz signals from the Reference Mixer and the VCO, respectively. These two signals are then applied to the phase/frequency detector for comparison.

A pair of ECL D-type flip-flops, U2031A and U2031B, comprise the phase/frequency detector. The flip-flops drive a common reset line with a wired-AND output. The clock input of U2031B is driven with the signal from the 18 MHz VCO, and the clock input of U2031A is driven with the signal from the 18 MHz signal from the Reference Mixer.

Both flip-flops are configured to reset together whenever both are set. If they are clocked with signals that exactly match in frequency and phase, then both flip-flops set simultaneously and then almost immediately reset. If the Reference Mixer signal has a slight phase lead, U2031A will remain set longer than U2031B. If the Reference Mixer signal has a slight phase lag, U2031B will set first and remain set the longest. The signal that has the phase lead will cause the associated flip-flop to be set a greater percentage of time than the lagging flip-flop. If there is a frequency difference between the two inputs, the flip-flop with the higher input frequency will be set more of the time than the other flip-flop. The ratio between the filtered output signals of the two flip-flops indicates whether the Reference Mixer signal leads, lags, or differs in frequency from the 18 MHz VCO signal.

The outputs of the flip-flops are low-pass filtered by C1031 and C1028 and applied to differential amplifier U1031. U1031 compares the outputs of the flip-flops and produces an output that controls the tuning of the 2182 MHz microstrip oscillator. The phase-lock loop bandwidth is controlled by R1026, C1029, R1027, and C1026. The gain slope breaks to −12 dB/octave for frequencies below 16 kHz. Resistors R1033 and R1034

divide and offset the output of U1031 so the tune voltage ranges between 0 and −12.5 V.

The output of divider R1033/R1034 is applied to the varactor of the 2182 MHz microstrip oscillator (2nd LO). This closes the phase-lock loop, tuning the 2nd LO so that it closely tracks the 18 MHz VCO. When the 18 MHz VCO is tuned, U1031 simultaneously tunes the microstrip oscillator an equal amount. Within the loop bandwidth, the 2nd LO performance is determined by the 18 MHz VCO instead of the microstrip oscillator, giving a significant improvement in frequency stability and reduction of phase noise.

829 MHz 2nd CONVERTER (Diagrams 15 and 16)

The 829 MHz 2nd Converter assembly (A23) down-converts the 1st Converter band 2-4 829 MHz IF signal to 110 MHz to drive the 3rd Converter. It also provides the switching to select either the 2072 MHz 2nd Converter or the 829 MHz 2nd Converter. The IF circuits in the signal path are shown on diagram 16, IF Section. The local oscillator circuits are shown on diagram 15, LO Section.

IF Section (Diagram 16)

The 829 MHz IF circuits include an input diplexer, an amplifier, a band-pass filter, a mixer, and a diode switch.

829 MHz Diplexer. The 829 MHz Diplexer (A23A4) passes signals at 829 MHz with approximately 1 dB maximum attenuation and 200 MHz pass-band. Frequencies outside the pass-band but between about 50 kHz to 2 GHz are terminated in 50Ω loads with a match of at least 10 dB. Figure 7-3 shows a simplified schematic of the diplexer.

At 829 MHz, the series resonators provide a low impedance path from input to output. The input is from the 1st Converter through low-pass filter FL15 and P231. Signal loss across the 50Ω resistors is insignificant because of the low impedance path around these resistors. The parallel resonant circuit to ground appears as an open circuit at 829 MHz.

At frequencies above or below the pass-band, the series resonators appear as large reactances, shifting the primary signal flow through the 50Ω resistors. The out-of-band impedance of the parallel resonant circuit is now small compared to 50Ω. Thus, the 50Ω resistors are essentially grounded at their junction, terminating both the input and output ports of the diplexer.

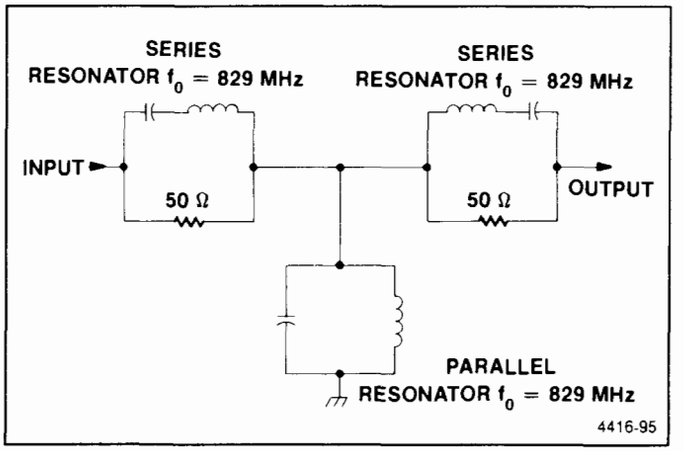


Figure 7-3. Simplified diplexer diagram.

A wide bandwidth is used to minimize loss in the resonant circuits and eliminate adjustments. Relative bandwidths of the series and parallel resonant circuits are optimized to provide reasonable match at the band edges.

As shown in the schematic diagram, the diplexer contains components not shown in Figure 7-3. The 50Ω terminations are actually two pairs of 100Ω resistors, R1014-R1015 and R1011-R1012, connected in parallel to reduce load inductance. Small capacitors, C1010 and C1013, are connected across each load to improve impedance match at frequencies above the pass-band. The inductor in the parallel resonator is a printed length of transmission line that is tapped to establish the correct bandwidth. One end of this inductor is grounded through four capacitors so that dc bias from the 1st Local Oscillator Driver can be introduced to the 1st Mixer (A12) through this diplexer. Several capacitors are used in parallel to minimize inductance and circuit Q degradation. A low-pass filter is included in the bias line to minimize any noise from the 1st LO driver.

The diplexer drives the 829 MHz Amplifier through a 1.2 GHz Low-Pass Filter that consists of three shunt capacitors and two series inductors. Cutoff frequency for this filter is 1.2 GHz.

829 MHz Amplifier. The 829 MHz Amplifier (A23A5) provides about 18 dB of signal gain at 829 MHz. The amplifier consists of two similar cascaded amplifier stages, Q1017 and Q1025, and a 3 dB pad. The overall noise figure is approximately 2.8 dB. The gain stages are stable amplifiers that are designed for use in a 50 ohm system.

Since the amplifiers are nearly identical, the following description applies to both amplifiers. The ac and dc signal paths are treated separately. Figures 7-4 and 7-5 are simplified diagrams of the ac and dc signal paths.

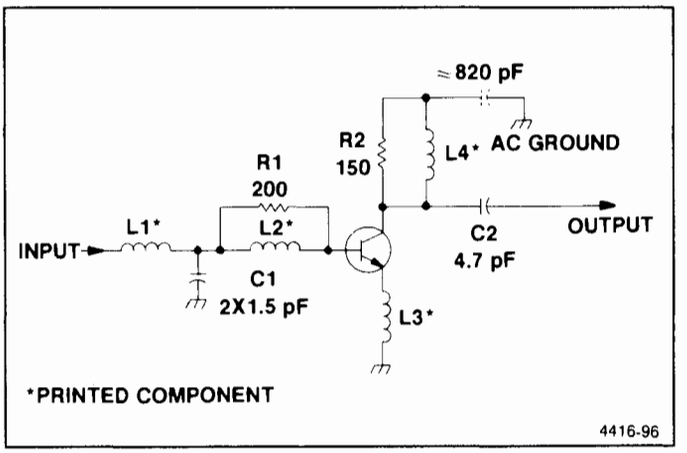


Figure 7-4. Equivalent ac circuit of an 829 MHz amplifier.

In the ac circuit (Figure 7-4), C1, L1, and L2 form the input matching network. (In the first stage, L1 is actually the series inductance of dc-blocking capacitor C1016 at the input of the amplifier.) The collector circuit is matched to 50Ω by L4 and C2. To a large extent, L3 controls the gain of the stage. High frequency stability is enhanced by R1 and R2.

In the dc circuit (Figure 7-5), negative feedback through the voltage divider, consisting of R3 and R4, sets the collector voltage as a fixed proportion of the −12 V reference supply. Collector current is determined by R5. Current requirements for the first stage are less than the requirements for the second because the first stage requires less intermodulation distortion performance. Diode clamps are provided for each amplifier (CR1013 and CR1022 at the bases of the amplifiers in the actual circuits) to protect the transistor against reverse breakdown of the base-emitter junction in case the +12 V supply fails.

In the actual amplifiers (not shown in Figures 7-4 and 7-5) L1014 and C1014 at the base of Q1017, C1013 at the collector of Q1017, L1021 and C1023 at the base of Q1025, and C1013 at the collector of Q1017 decouple the signal path from the bias network.

The 3 dB pad (R1026, R1027, R1028, and R1029) helps maintain a wide-band 50Ω interface between the second amplifier stage and the 829 MHz Bandpass Filter on the 829 MHz 2nd Converter board.

Test point J1029 at the output port of the 3 dB pad is used for checking amplifier performance and to aid in adjustment of the 829 MHz band-pass filter on the

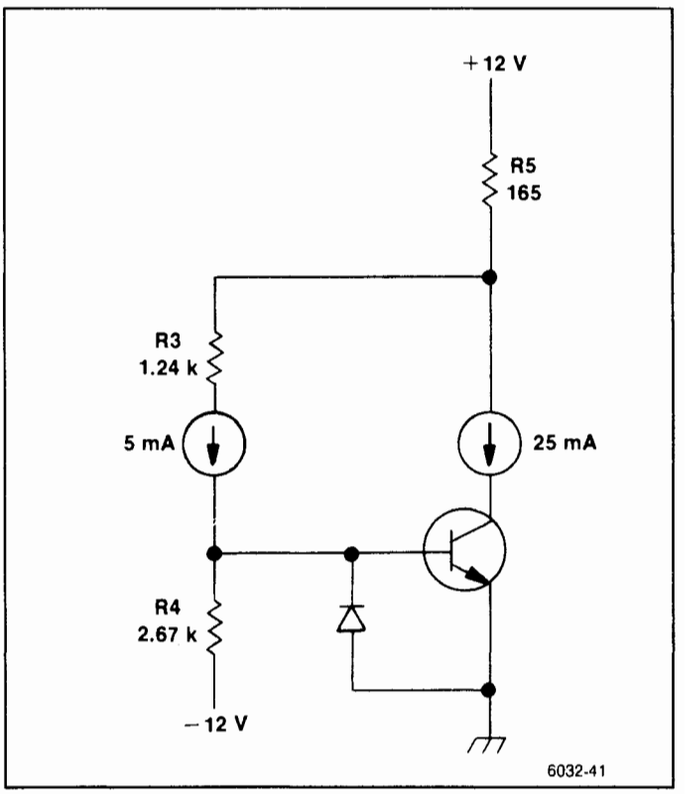


Figure 7-5. Equivalent dc circuit of an 829 MHz amplifier.

829 MHz 2nd Converter board (A23A7).

829 MHz 2nd Converter. Down-conversion from 829 MHz to 110 MHz IF occurs on the 829 MHz 2nd Converter board (A23A7). The board contains a 829 MHz Band-Pass Filter, a 1.3 GHz Low-Pass Filter, a 3 dB pad, a 450 MHz High-Pass Filter, a single-balanced mixer, and a 300 MHz Low-Pass Filter.

The 829 MHz Band-Pass Filter blocks unwanted inputs, primarily the 609 MHz image signal. It consists of four, quarter-wave, coaxial type resonators, mounted on the 829 MHz 2nd Converter board. The end resonators are tapped near their grounded end to facilitate input and output coupling of the filter. Inter-resonator coupling is provided by printed "through-the-board" capacitors that connect between the resonators at their high impedance end. A bendable tab is located at the high impedance end of each resonator for fine adjustment of resonant frequency. The bendable tab acts as a small, variable capacitor to ground, making fine adjustments of resonant frequency possible. When properly tuned, the filter presents at least 12 dB input return loss and about 2 dB insertion loss at 829 MHz.

The 1.3 GHz Low-Pass Filter blocks high frequency signals that would otherwise be admitted at the re-entrant frequencies of the band pass in excess of 2 GHz. The function of the 1.3 GHz Low-Pass Filter is shared by the 1.2 GHz Low-Pass Filter on the 829 MHz Diplexer board.

The 3 dB pad helps ensure a consistent 50Ω interface for the 829 MHz Band-Pass Filter.

The 450 MHz High-Pass Filter blocks the lower IF signals generated within the mixer.

The mixer generates several intermodulation products of the 829MHz RF and 719 MHz LO signals. The mixer diodes are transformer driven by a large amplitude (+12 dBm) 719 MHz signal from the local oscillator. This large signal drives the diodes in and out of conduction, switching the lower amplitude 829 MHz signal on and off at a 719 MHz rate, to generate the mixer products. Only the difference frequency of 110 MHz is passed through the 300 MHz Low-Pass Filter. The sum product of 1548 MHz, is reflected back to the mixer by the 829 MHz Band-Pass Filter, in-phase with LO harmonics, to increase the energy of the 110 MHz signal. A printed delay line, between the 829 MHz Band-Pass Filter and 1.3 GHz Low-Pass Filters, controls the phase delay. The net result of this "image enhancement" is low conversion loss and good inter-modulation distortion performance. The 3 dB pad reduces the image enhancement effect and permits the use of non-critical line lengths and filter characteristics. Overall conversion loss, from 829 MHz to 110 MHz, is about 8.5 dB, including 2 dB from the 829 MHz Band-Pass Filter and 3 dB from the attenuator.

The 300 MHz Low-Pass Filter blocks LO, RF, and higher frequency products.

110 MHz IF Select. The 110 MHz IF Select circuit (A23A6) selects the 110 MHz IF signal from either the 829 MHz 2nd Converter or the 2072 MHz 2nd Converter for transmission to the 110 MHz IF Amplifier.

The 110 MHz IF signal from the 829 MHz 2nd Converter board is applied directly to the select circuit. The 110 MHz IF signal from the 2072 MHz Converter board is applied to the select circuit via P233 and a controlled amplifier (Q1012/Q1011). Switching between the two signals is done by CR2011, CR2012, CR2013, and CR1015.

Diode CR2011 is turned on when the IF SELECT line to the 110 MHz IF Select is low. This steers the 110 MHz IF signal, from the 829 MHz 2nd Converter board, to the output port. At the same time CR2012, CR2013, and CR1015 turn on and Q1011 turn off to isolate the output port from any spurious signals from the 2072 MHz 2nd Converter.

When the IF SELECT line goes high, Q1011 turns on and CR2012, CR2013, and CR1015 turn off to allow the 110 MHz IF signal, from the 2072 MHz 2nd Converter, to be applied to the output port. Series diode CR2011 also turns off to prevent signal loss into the inactive 829 MHz 2nd Converter. Because the 719 MHz LO is also turned off by the state of the IF SELECT line, isolation for the 829 MHz 2nd Converter is not critical when the converter is inactive. The switch and amplifier logic is summarized in Table 7-2.

Table 7-2
SWITCH AND AMPLIFIER SELECTION

IF Select Line	Series Switch	Shunt Amplifier	110 MHz IF Source
High	On	Off	829 MHz 2nd Conv.
Low	Off	On	2072 MHz 2nd Conv.

The diodes are used as the basic switch elements. They present only a few ohms of series resistance to RF signals when forward biased, with current of several milliamps. When reverse biased, the diodes present essentially an open circuit. The control signal from Q2015 is connected in a series path through the four diodes (CR2011, CR2012, CR2013, and CR1015) and inductors L2011, L2013, and L2019. Thus, only a small current is required to forward bias all four diodes. This bias current is also used to turn off Q1011.

Diodes CR2012 and CR2013 are incorporated into a pi-type matching network, consisting of L2011, L2013, and C2012. Therefore both switches shunt the signal at moderately high impedance points. In addition, when the switch diodes are turned on, parallel resonance between L2011 and C2012 presents virtually an open circuit to signals passed by switch CR2011. Switch diode CR2013 is located at the high impedance node created by the series resonance of L2019 and C2017. Diode CR1015 directly shunts the output from Q1011.

Transistor Q1011 operates as a common-emitter amplifier for the 110 MHz IF signal from the 2072 MHz 2nd Converter. Its gain and impedance match are controlled by feedback resistors R1011 and R1012. Resistors R1013 and R1018 attenuate the output by approximately 6 dB for enhanced control of impedance match and stability characteristics.

Transistor Q1012 maintains a constant dc current through Q1011. Dc Collector current for Q1011 is set at approximately 15 mA. Collector current from Q1011 develops a voltage across R1017. Transistor Q1012 then compares this voltage with the fixed voltage of the voltage divider, R1015 and R1016. Any variation in the collector current of Q1011 is sensed by Q1012, and

offset by a resultant change in the base current of Q1011.

When the control current from Q2015 (through the switching diodes) develops a voltage across R1017 that exceeds the control limits of Q1012, it effectively removes the base-bias from Q1011 and turns Q1011 off. Negative current, supplied through R1014, ensures that Q1011 is turned off. Diode CR1011 protects the base of Q1011 from excessive reverse bias. Voltage across R1017 is approximately 3.4 V when Q1011 is turned on and approximately 4.4 V when it is off. Overall gain is approximately 12.8 dB when the amplifier is turned on.

The 110 MHz IF signal is transmitted via P232 to the 110 MHz IF Amplifier shown on diagram 17.

LO Section (Diagram 16)

The 829 MHz 2nd Converter LO generates the 719 MHz frequency that is mixed with the 829 MHz IF to produce the 110 MHz IF signal. In the following description, the circuits are referred to as the 719 MHz LO. The 719 MHz LO consists of a phase lock loop, a 719 MHz output circuit, and a 2nd LO front panel output circuit. Refer to Diagram 16 while reading the following description.

Phase Lock Circuit. The phase lock circuit receives reference frequency inputs and uses phase/frequency detection techniques to use those signals in controlling the output frequency of the 719 MHz oscillator. The circuit consists of a voltage controlled oscillator (VCO), a phase/ frequency detector, a harmonic mixer, and various amplification stages and power splitters. When the 719 MHz LO is enabled, the 2182 MHz LO output frequency is used as a swept reference to derive the 719 MHz frequency. The VCO is controlled so that the third harmonic of its output frequency is a constant difference from the 2182 MHz reference. This control is accomplished by the phase lock loop. Refer to Figure 7-6 for a simplified block diagram.

In the phase lock loop, the harmonic mixer generates a frequency that is the difference between the swept 2182 MHz input reference and the third harmonic of the VCO output frequency. Ideally, this difference is 25 MHz, which in turn, is compared with the 25 MHz that is divided down from the 100 MHz oscillator output supplied from the 3rd Converter. This comparison is done by the phase/frequency detector whose output is a correction voltage that drives the VCO and shifts the oscillator frequency in the direction to hold the nominal output frequency at 719 MHz. This completes the loop that causes the VCO to track the 2182 MHz reference.

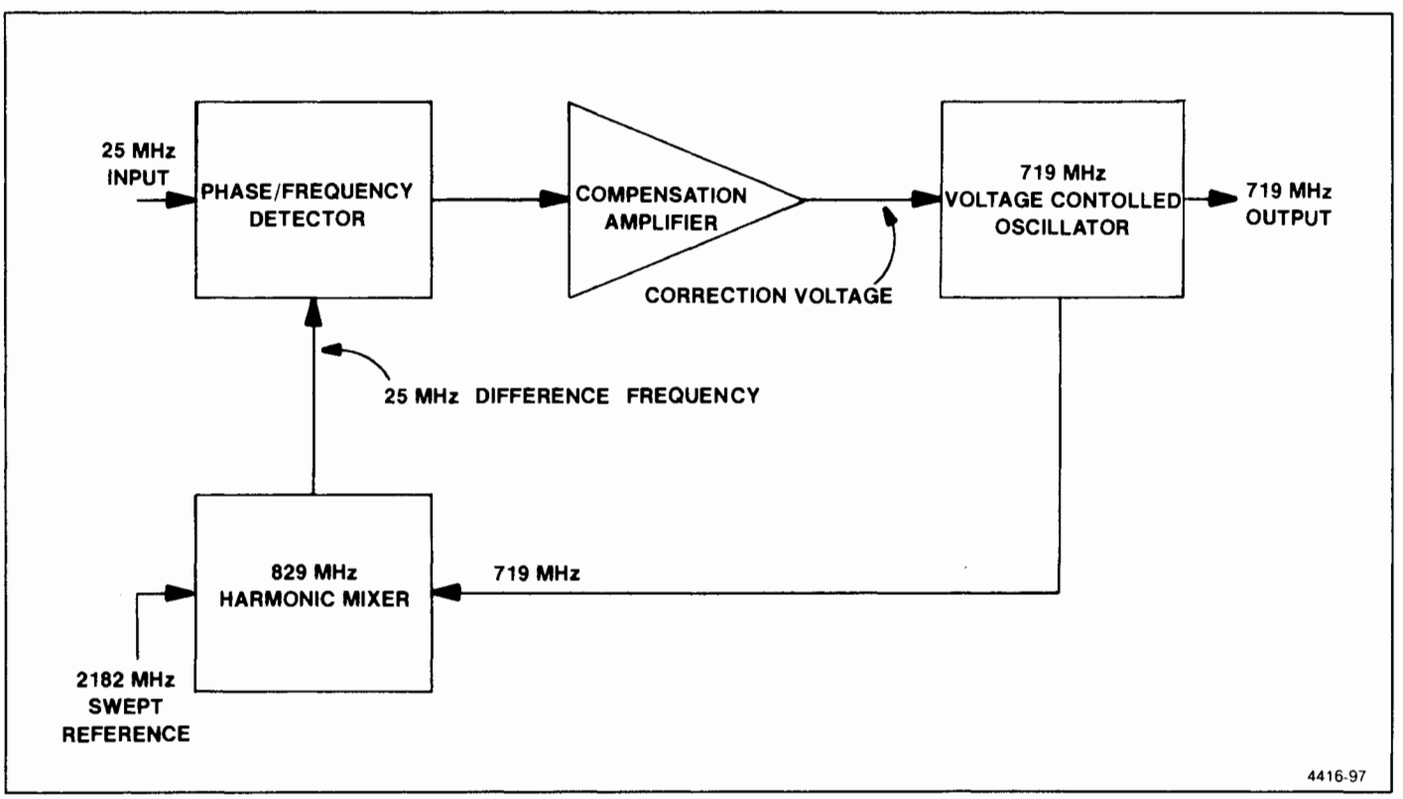


Figure 7-6. Block diagram of the phase lock loop in the 829 MHz 2nd Converter.

Because the 3rd harmonic of 719 MHz is locked to the 2182 MHz reference, the tuning range of the 719 MHz oscillator is only one third of the tuning range of the reference. Since the range is 4 MHz, the range of the 719 MHz oscillator is 719 ±1.33 MHz.

The 719 MHz VCO (Q2014) uses a Colpitts configuration, with a printed circuit quarter-wavelength transmission line resonator, to achieve high spectral purity and good thermal stability. Correction voltage is applied to varactor diode CR1011 (which is connected at the midpoint of the transmission line resonator) to vary the resonant frequency of the transmission line over a 1.5 MHz range. A tunable transmission line (also printed) adjacent to the printed resonator compensates for variations in component tolerances and resonator dimensions. This adjustable transmission line is cut, at factory calibration, to the correct length for proper VCO operation. A scale with minor divisions every 2 MHz is printed next to the adjustable line to aid in calibration. The output from the oscillator is extracted near one end of the quarter-wavelength line through two printed inductors and applied to output amplifiers through a power splitter.

The 719 MHz VCO is enabled or disabled, under microprocessor control, dependent upon the frequency band being analyzed, by the IF SELECT line. When this line is low, Q2017 is cut off, which turns Q2016 off. This, in turn, cuts off transistor Q3015 (which is the current source for oscillator transistor Q2014), thus disabling the 719 MHz oscillator.

From the oscillator, the +6 dBm 719 MHz output signal is applied, through a power divider consisting of resistors R1021, R1022, and R1020, to isolation amplifier Q1021. From the other side of this power divider, the signal is applied to an output amplifier (Q2021) for transmission to the 829 MHz 2nd Converter Mixer circuit. A second isolation amplifier (Q3021), identical in configuration, provides isolation between the 719 MHz oscillator output and any undesired Harmonic Mixer products.

The 829 MHz Harmonic Mixer produces not only the required 25MHz difference frequency, but also many higher order intermodulation products. Two of these frequencies, 744 MHz and 694 MHz, are 25 MHz from the 719 MHz oscillator frequency. The isolation amplifiers, Q1021 and Q3021, provide sufficient attenuation in the reverse direction to prevent these products from getting into the 829 MHz mixer to produce spurious signals.

To provide maximum reverse attenuation in each amplifier circuit, external RF feedback is kept to a minimum. An output matching LC network, consisting of capacitor C1025 plus a printed inductor for Q1021, and capacitor C3021 plus a printed inductor for Q3021, presents an optimum load impedance to the collector of each transistor to allow maximum power transfer to the attenuator that precedes the harmonic mixer. An input LC matching network consisting of capacitors C1023, C1022, plus a printed inductor for Q1021 and capacitors C3023, C3022, plus a printed inductor for Q3021, establishes the 50 ohm input impedance to each transistor.

A 3 dB attenuator consisting of resistors R3021, R3022, R2021, and R3023, at the output of isolation amplifier Q3021, provides a non- reflective source impedance to the mixer. Without the attenuator, mixer conversion loss could vary from unit to unit.

The 829 MHz Harmonic Mixer, consisting of diode CR2021, inductor L2014, and a half-wavelength (at 2182 MHz) transmission line, produces the difference frequency between the third harmonic of the 719 MHz oscillator frequency (nominally 2157 MHz) and the 2182 MHz reference frequency. Note that the 2182 MHz signal is supplied from the 2182 MHz 2nd Local Oscillator through coaxial connector P237 and the power divider, consisting of resistors R1021, R1023, and R1022, to a 1/2 wavelength transmission line. The VCO input to the mixer switches diode CR2021 at a 719 MHz rate. The 2182 MHz reference acts as the RF and is applied to the diode from the transmission line. The resultant 25 MHz intermediate frequency is diplexed from the mixer through the 100 MHz low-pass filter consisting of capacitor C3014 and inductor L3014. (Diode CR2021 is mounted on printed circuit board cut-outs to relieve any necessity of bending the diode leads. Lead bending may fracture the diode case.) Inductor L2014 provides a bias return path to allow the diode to switch at a 719 MHz rate.

From the 829 MHz Harmonic Mixer, the signal is applied through the above mentioned low-pass filter to cascaded amplifiers U1053 and U1044B. These amplifiers boost the -32 dBm mixer output signal to a level appropriate to drive the phase/frequency detector. IC amplifier (U1053) contains two differential amplifiers in cascade; amplifier IC U1044 contains only one differential amplifier and acts as a buffer. When the loop is first acquiring lock, such as at power-on, the nominal 25 MHz IF may be as high as 34 MHz. Two stages of amplification are necessary to ensure enough gain for the phase/frequency detector to drive the IF back to 25 MHz; the buffer is necessary to provide ECL levels to the detector.

The second input to the phase/frequency detector is the 100 MHz signal, from the reference oscillator in the 3rd Converter, via two amplifier stages, U1022A and U1022B, and a divide-by-four circuit, U1036A and U1036B. The 100 MHz signal is divided down to a 25 MHz reference for application to the phase/frequency detector. Two stages of amplification are used to isolate the 100 MHz reference bus from signals generated in the local oscillator section of the 2nd Converter. This stable 25 MHz reference signal is used

to lock the difference frequency from the Harmonic Mixer to 25 MHz.

The phase/frequency detector output is a voltage that is proportional to the phase difference between the 25 MHz reference and the IF signal from the 829 MHz Harmonic Mixer. This correction voltage is then applied to the 719 MHz VCO to lock it to the reference.

The detector circuit consists of two D-type flip-flops, U2047A and U2047B, and a differential amplifier stage used as a NAND-gate (U1044A). The 25 MHz reference signal, from the frequency divider, is applied to the clock input of flip-flop U2047A; the nominal 25 MHz signal from the 829 MHz Harmonic Mixer is applied to the clock input of flip-flop U2047B. The rising edge of the input signal to each flip-flop causes the Q(bar) outputs to return to the low level only after both flip-flops have been clocked.

If the frequency out of the 829 MHz Harmonic Mixer is below 25 MHz, or if its phase lags that of the 25 MHz reference, the Q(bar) output of flip-flop U2047A will remain high longer than the Q (bar) output of U2047B. If the frequency out of the Harmonic Mixer is above 25 MHz, or if its phase leads, the opposite will occur. When the two flip-flops are clocked at the same frequency and phase, the two outputs will be high for the same amount of time. The Q(bar) outputs are applied to a compensation or differential amplifier U3053, that determines which output is high for the longer time.

Compensation amplifier U3053 provides part of the loop gain to ensure that the 719 MHz oscillator will track the sweep of the 2182 MHz reference oscillator. The compensation amplifier also limits the loop bandwidth to 100 kHz to make certain that the loop will not oscillate. Note the differential inputs to the amplifier each include a low-pass RC filter to attenuate the undesired high frequency clock pulses from the phase/frequency detector.

The nominal swing of the U3053 output is from +12 V to -12 V. Since the compensation amplifier is capable of considerably more output than is needed to control the oscillator, a voltage divider is used to limit the output and reduce amplifier related noise. This voltage divider, consisting of resistors R2053, R2054, R3051, and R3052, reduces the possible ±12 V swing to +5 V to +12 V, as required by varactor diode CR1011. Nominal voltage swing in a locked condition is +6.75 to +7.5 V. Thus, dependent upon whether the Harmonic Mixer frequency is above or below 25 MHz, the correction voltage swing, applied to diode CR1011, is more than nominal to correct the oscillator frequency.

2nd Local Oscillator Output Circuit. A portion of each 2nd LO output signal is sent to the front panel 2nd LO OUT connector. This output provides signal for external accessory equipment, such as a tracking generator. Each local oscillator (719 MHz and 2182 MHz) output is applied through power dividers to a power combiner for application to the 2nd LO OUT connector.

The 719 MHz oscillator frequency is applied from a power splitter (R3027, R3028, R3029) through a 1 GHz low-pass filter (C3025, C2024, C1023, C1021, and three printed inductors), to the power combiner (R2024, R2025, R2026), and the front panel 2nd LO OUTPUT. The 2182 MHz oscillator signal is applied through a power splitter (R1021, R1022, R1023), a 2.2 GHz bandpass filter (consisting of coupled 1/4 wavelength printed lines) to the power divider (R2024, R2025, R2026) and the front panel 2nd LO OUTPUT.

Both 2nd local oscillator signals, 2182 MHz and 719 MHz, are present at the front panel when the 829 MHz 2nd Converter is selected.

719 MHz Output Circuit. The 719 MHz 2nd Local Oscillator signal is applied is applied through divider resistors R2021, R2023, and R2024 to isolation amplifier Q2021. Q2021 boosts the signal level from about 0 dBm to +12 dBm to drive the 829 MHz mixer. The output of the amplifier includes a 3 dB attenuator (consisting of resistors R2027, R2028, and R2029), to ensure a 50 ohms non-reflective source impedance. The signal level at test point J2026 is typically −6 dBm.

3RD CONVERTER (Diagram 4)

The 110 MHz IF Amplifier (A32)and 3rd Converter (A34) down converts the 110 MHz output signal from the 2nd Converter to 10 MHz for the Variable Resolution circuits. A 100 MHz crystal controlled local oscillator is applied to the mixer and, through output amplifiers, to many other circuits throughout the instrument as a reference signal. It is also available for external use at the front-panel CAL OUT connector.

The 110 MHz signal is amplified in a three-stage gain block and applied to a three-section band-pass filter. This filter uses helical resonators and has a nominal bandwidth of 1 MHz. From the band-pass filter, the signal is applied to the converter, which consists of a mixer, an oscillator, and various output amplifiers.

110 MHz IF AMPLIFIER (Diagram 17)

Initial gain for the analyzer is provided by the 110 MHz IF Amplifier. This gain compensates for conversion losses in the thre mixers. Typical gain for the amplifier is 21 dB. The amplifier consists of three stages of amplification and an attenuator. The first two mixers in the RF system offer no high-frequency gain; therefore, it is important that this amplifier exhibit low noise characteristics. It must also be relatively free from third-order intermodulation distortion.

Signal input is applied through an impedance matching band-pass filter (L2044 and C325) to a parallel tuned circuit. The signal is injected into the parallel-tuned circuit through a tap in the inductor and taken out at the high impedance side through variable capacitor C2047. Inductive input provides for conversion to high impedance within the tuned circuit; the extra capacitor on the output provides for conversion back to 50 ohms nominal. The primary tuning capacitor, C325, adjusts the resonant point; the output capacitor, C2047, is adjusted in combination with C325 for good impedance match at 110 MHz. This is done with a return loss bridge. The nominal return loss is 35 dB. The Q of the input filter is approximately 20.

From the input filter, the signal is applied to Q4053, which is the first stage of amplification. This is a broad-band feedback amplifier to provide good input and output impedance and controlled gain. All feedback is through reactive components (transformer T3054), not resistive components. Thus, the impedance and gain can be controlled without significant noise problems.

The second amplifier stage, Q4037, is essentially the same as the first, with only minor bias differences. Gain through each of these stages is approximately 9 dB. The output is applied through a 3 dB attenuator, to preserve the impedance figure, to the bridged "T" adjustable attenuator. The 3 dB attenuator consists of resistors R2039, R2038, and R2043.

From the 3 dB attenuator, the signal is capacitively coupled through C2037 to the adjustable attenuator. This attenuator uses two PIN diodes, CR3030 and CR1029, in the mode when the resistance to RF signal flow is controlled by the current through the diodes. Refer to Figure 7-7 to aid in understanding the following description.

If resistor R1 in Figure 7-7 were set to infinite resistance and resistor R2 were set to zero resistance, the RF signal path would be through R2 to ground, to produce infinite signal attenuation. If resistor R1 were set to zero resistance and resistor R2 were set to infinite resistance, the RF signal path would be through R1 to the load, to produce almost no attenuation. This, basically, is how the adjustable attenuator operates, except that resistors R1 and R2 are actually PIN diodes and the RF path resistance through these diodes is controlled by the current through the diodes in an inverse proportion (higher current results in less resistance to RF).

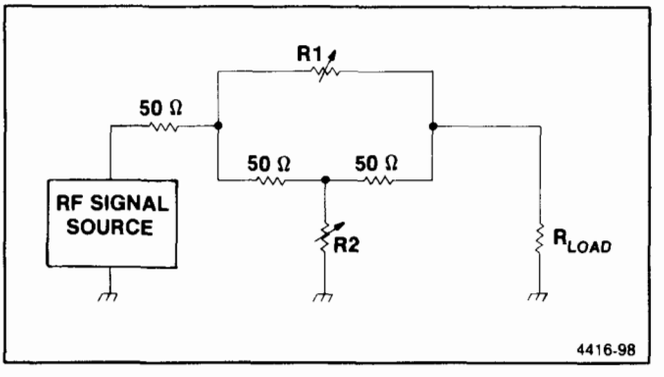


Figure 7-7. Bridged "T" attenuator equivalent circuit.

Resistors R3035 and R2030 on the detailed schematic diagram establish a constant current of approximately 2 mA from the 15 V supply to the diodes. This current is divided according to the bias on the diodes. The bias, in turn, is established by gain adjustment R1015, from the +15 V supply. If R1015 is set low (near ground), diode CR3030 is reverse biased and the 2 mA flows through diode CR1029. This routes the RF signal through resistors R2032 and R3029 and capacitor C2029, with the impedance characteristics of CR1029 added for maximum attenuation.

If R1015 is set higher (nearer +15 V), diode CR3030 is forward biased and starts to conduct. Since the 2 mA supply current is relatively constant, this subtracts from the current through CR1029. Thus, the impedance of the diodes is relatively constant, which results in a good impedance match over a broad range. The RF signal path is determined by the exact amount of current through CR3030; part of the RF signal path is through CR3030 to the output amplifier and part is through R2032 and diode CR1029 to ground. This results in reduced signal attenuation.

If R1015 is set to the positive limit, the entire 2 mA flows through CR3030. This routes the RF signal through CR3030 (which exhibits little resistance with high current) to the output amplifier with almost no attenuation. (The insertion loss is approximately 1 dB.)

From the adjustable attenuator, the signal is applied to the final amplifier Q3018. This stage is a broad-band feedback amplifier that supplies relatively substantial output current and exhibits good intermodulation distortion performance. This is provided primarily through the large current capacity, by negative feedback through resistor R3014, and emitter degeneration through resistor R4029. These resistors are sized to provide a resonably good impedance match at 110 MHz. Nominal gain of the stage is 13 dB.

With Gain potentiometer R1015 set for maximum gain (least attenuation), the gain of the 110 MHz IF Amplifier is approximately 26 dB to 27 dB. R1015 is normally adjusted for total gain of 21 dB.

The output signal from the 110 MHz IF Amplifier is applied through the 110 MHz band-pass filter, FL36, to the 3rd Converter.

110 MHz BAND-PASS FILTER (Diagrams 11 and 17)

The 110 MHz band-pass filter is a three-section filter using helical resonators, which determine the widest resolution bandwidth of the analyzer. The filter provides image rejection to prevent the mixer from producing 10 MHz outputs from input signals of 90 MHz, and it also limits the noise spectrum that appears at the 10 MHz IF circuits to those frequencies at which signals also appear.

Though the filter is a sealed unit, in the interest of system understanding, the following brief description is provided.

The filter consists of three small encapsulated helical resonators that are tuned with multi-turn trimmer capacitors. For purposes of impedance matching, the filter is symmetrical. The end resonators are connected to external circuits by 10 pF capacitors attached to taps on the coils. Coupling between resonators is accomplished through holes in the resonator cans.

Adjustment of the filter for minimum attenuation is performed by setting the three trimmer capacitors. Insertion loss is approximately 4 dB to 4.5 dB. From the filter, the 110 MHz signal is applied to the 3rd Converter board.

3rd CONVERTER (diagram 17)

The 3rd Converter consists of a crystal and phase locked 100 MHz oscillator and mixer. It outputs the 3rd IF of 10 MHz, for the VR, and a stable 100 MHz reference for other circuits within the instrument.

100 MHz Oscillator

A Colpitts oscillator is formed by Q2038, L1041, C1038, and related components. Y3038 is a 100 MHz crystal that operates in a series resonant mode in the feedback loop of the oscillator. The output of the oscillator is coupled through C2042 to differential amplifier Q2042/Q2041. The two separate outputs of approximately 2 V peak-to-peak amplitude go to three hybrids (mixer U3051, distribution amplifier U3031, and calibrator U2022) on the 3rd Convertor board.

Mixer

At mixer U3051, 100 MHz enters on pin 2 and is amplified to drive a ring diode mixer. 110 MHz enters on pin 10 and is mixed with the 100 MHz to yield mixing products at 10 MHz and 90 MHz. The 10 MHz signal passes through a low-pass filter and is sent to the Variable Resolution Input circuit, while the unwanted 90 MHz signal is terminated in a 50 ohm resistance within the mixer.

Distribution Amplifier

U3031 distributes a 100 MHz signal to other modules in the instrument. The input level on pin 2 is typically 2 V peak-to-peak, while the output level is 0 dBm into a 50 ohm load.

Calibrator

U2022 and related components regulate a 100 MHz signal to -20 dBm for the front-panel CAL OUT connector, through coaxial connector J1011. VR1051 serves as an accurate 6.2 V reference, which is attenuated to approximately 1.2 V and applied to pin 6 of U2022. The 100 MHz signal enters pin 1 and passes through a variable attenuator pin diode. The signal is then amplified

and passed through a low-pass filter to remove any harmonics. The signal then enters a peak detector and comparator where the peak amplitude of the 100 MHz signalis compared to the 1.2 V reference on pin 6. An operational amplifier then adjusts the attenuation level of the pin diode to maintain a constant signal level. The output of this operational amplifier can be measured on TP3011. A small portion of the 100 MHz signal is attenuated through R2011 to -20 dBm. R1021 and R1022 supply bias current to the peak detector circuits. The voltage on pins 7 and 8 should typically be +5 V.

C2023, C2011, and related components form a high-pass filter to allow harmonics of 100 MHz to pass through to the front panel. The final result is a calibrator signal rich in harmonics with an accurate 100 MHz amplitude.

IF SECTION (Diagram 5)

The IF section receives the 10 MHz IF signal from the 3rd Converter, establishes the system resolution, levels the gain for all bands, logarithmically amplifies the signal, and detects the signal to produce the video output to the Display section.

System bandwidth resolution is selectable from 1 MHz to 1 kHz in decade steps. This selection is performed by the Variable Resolution circuits and is controlled over the instrument bus. Two sets of filters are used to establish the bandwidth. Band-pass filters are also included at the circuits input and output.

Significant gain is also provided by several stages of amplification within the Variable Resolution circuit block. Other gain steps, under microcomputer control, are also provided by switching gain blocks in or out of the signal path. These gain blocks provide −10, +20, or +30 dB of additional gain when switched in combination.

Leveling, to compensate for front-end losses, is also included in the Variable Resolution circuit block. Because there are greater front-end losses in the higher frequency bands, band leveling amplification is required for these bands.

Logarithmic amplification of the signal is required to calibrate the graticule in dB/division. This is performed by a seven stage amplifier that produces an output proportional to the logarithm of the input. Thus, the screen displacement can be selectable for the amount of change per division, and can be proportional to the input level change. For example, in the 10 dB/div display mode, each division of displacement on the screen represents a signal level change of 10 dB regardless of whether it is at the top or bottom of the screen.

An area detector follows the logarithmic amplifier to produce a positive-going output signal that is applied to the display section as the VIDEO signal.

Variable Resolution (Diagrams 18, 19, 20, and 21)

The Variable Resolution (VR) circuits establish the resolution bandwidth and provide approximately 41 dB of system gain in band 1. The assembly (A68) consists of two sets of filters plus gain stages. Since the input to the VR circuits is nominally at −35 dBm and the Log Amplifier input requires +6 dBm for full screen, the VR circuits must provide the gain difference. The VR supplies 30 dB of additional gain and 10 dB of gain reduction for all vertical display modes as well as 30 dB of additional gain for band leveling.)

Physically, the VR assembly contains two sub-assemblies that connect together and plug onto the instrument Mother board. The input circuits are in one sub-assembly and the output circuits and digital interface are in the other. Each of the sub-assemblies consists of boards that plug onto a four-layer VR Mother board with a ground plane on both outside layers. Only power supply and control voltages travel through the VR Mother board. All signal interconnection is via coaxial cable.

VR Input (Diagram 19)

The VR Input circuit receives the −35 dBm 10 MHz signal from the 3rd Mixer through J693. This signal is applied to a two-pole, 1.2 MHz bandpass filter, which augments the 1 MHz filter that precedes the 3rd Mixer and provides initial selectivity. This 1.2 MHz filter includes C1037 and C1031 and all of the components between. Filter tuning is provided by variable capacitors C1033 and C1026, Input Align.

From the filter, the signal is applied to broadband feedback amplifier Q1023, which is biased for a large output current (approximately 50 mA) to exhibit good intermodulation distortion performance. This performance is provided primarily through the large current capacity by negative feedback through resistor R1025 and by emitter degeneration resistor R1023.

A 6 dB attenuator at the output of amplifier Q1023 provides a clean 50 ohm output to the 1st Filter Select circuit and reflects a 50 ohm termination back through the amplifier for proper termination of the 1.2 MHz band-pass filter. The output signal is transmitted via jumper B.

1st Filter Select (Diagram 19)

The 1st Filter Select circuit operates with the 2nd Filter Select circuit through banks of switched filters to set the overall system bandwidth. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder IC U4035 (it provides a low signal on the appropriate output pin to enable the selected filter). Bandwidth selections are 1 MHz to 1 kHz in decade steps. The data bits select a filter bandwidth according to Table 7-3.

Filter selection is done by PIN diode switching. At the input and output of each filter is a series and a shunt diode. When a filter is selected, the series diodes are biased on and the shunt diodes are biased off. For the filters that are not selected (only one is on at a time), the diode conditions are opposite. Since the switching operation is the same for all filters, the

Table 7-3
BANDWIDTH SELECTION

Bandwidth	DB0	DB1	DB2
1 MHz	1	0	0
100 kHz	0	1	0
10 kHz	1	1	0
1 kHz	0	0	1

description for the 100 kHz filter selection is applicable to all filters.

With a content of 010 for the three data bits, line 2 from U4035 will be low. This turns on transistors Q3019 and Q3055, which operate as dc switches. With input switch Q3019 turned on, the current path is through R4012, L3012, CR3010, L3013, R3014, and Q3019. This current is determined by decoupling resistor R3014 and resistor R4012. The voltage drop across R3014 and R4012 is enough to turn CR3010 on and reverse bias CR3012. The same case exists for the filter output switch, Q3055. Resistors R3057 and R1067 establish the current to forward bias CR3061 and reverse bias CR3060.

Thus the signal from the input circuit, via jumper B, is applied through the selected filter and transmitted to the 10 dB Gain Steps circuit via jumper K. Nominal loss through the filter circuit is approximately 13 dB, with slight variations among the filters. The output level is nominally −32 dBm.

In the non-selected filter sections, the input and output switch transistors are turned off by the high outputs from decimal decoder U4035. The collectors are pulled toward −15 V through the resistors that forward bias the shunt diodes in the input and output. Since one filter is always selected, the voltage drop across the common input and output resistors (R4012 and R1067, respectively) back biases the series diodes. The number 6 output from U4035 pin 7 is always high in this instrument.

A filter is not used in the 1 MHz section, because this circuit section is preceded by two filters that accomplish the required function; the first is the 1 MHz filter between the 2nd and 3rd Converters, the second is the 1.2 MHz filter in the input circuit. Instead of a filter, a 6 dB attenuator is contained in the 1 MHz selection circuit. This attenuator provides initial leveling to compensate for the loss when a filter is used.

The 100 kHz filter is a double-tuned LC circuit designed for a good time-domain response shape. The filter is tuned with composite variable capacitors consisting of small air variables paralleled with switched fixed capacitors. A third variable capacitor may be adjusted to establish the desired bandwidth. For Option 07 instruments, a similar 300 kHz filter replaces the 100 kHz filter.

The 10 kHz filter uses a pair of two-pole monolithic crystal filters that are interconnected by variable shunt capacitor C2037. Input and output impedances are matched with broadband transformers T3026 and T3055. A 3 dB attenuator consisting of R2027, R2026, and R2028 is included at the filter input.

The 1 kHz resolution filter consists of a single two-pole monolithic crystal filter, matched to the 50 ohm impedance with broadband transformers T2035 and T2055. A 2 dB attenuator consisting of R2024, R2023, and R2025 is also part of the filter.

10 dB Gain Steps (Diagram 20)

The 10 dB Gain Steps circuit provides 10 dB of signal gain when selected by the microcomputer. The circuit consists of three stages of amplification; one stage provides variable gain and the other two are fixed gain steps. The nominal input signal level from the 1st Filter Select circuit is −25 dBm for a resolution bandwidth of 100 kHz. (All levels listed in this description relate to the 100 kHz resolution.)

The input signal is applied through an impedance transformer, T4019, to the first amplifier stage consisting of a differential pair, Q3016 and Q2027, and an emitter follower output amplifier, Q1036. Negative feedback through R1031 and R2051 provide gain stabilization. An output resistor, R2035, increases the output impedance of the composite amplifier to approximately 50 ohm.

Gain of the input stage is fixed for all resolution bandwidths. Adjustment R2025 is not used in this instrument. It is for use with other instruments having switchable filters in the 100 Hz position. In this instrument, Q2015 stays off, never letting the potentiometer have any affect on the circuit.

The output from the 1st stage is then applied to a common emitter stage (Q2043). Gain of this stage, when transistor Q4039 is turned on, is 10 dB. When the base of Q4039 is pulled low by data bit 0 from the decoder circuit on the #2 VR Mother board (A68A2) the transistor saturates and shunts the emitter load resistor, R3048, with R3038 and 10 dB Gain adjustment R3035.

The output of Q2043 drives the input of the third amplifier stage. This stage operates the same as the first stage except for gain variation. Feedback resistor R1060 is shunted by PIN diode CR1053. As the current through the diode increases, the resistance decreases and the gain of the stage increases. Gain control of the stage is established by the setting of the front-panel AMPL CAL adjustment. Gain range is approximately

14 dB.

Output impedance of the stage is 50 ohm, set by resistor R1064. Nominal output level is −2 dBm for a full screen display. This level may be as high as +8 dBm when MIN NOISE is active. A 10 dB gain is removed from the Log Amplifier to reduce the noise level and must be supplied by the VR section.

20 dB Gain Steps Circuit (Diagram 20)

The 20 dB Gain Steps circuit provides −6 dB, +4 dB, +14 dB, and +24 dB of gain in precise 10 dB steps. The nominal −2 dBm input is supplied through pin P from the 10 dB Gain Steps circuit. This signal is applied to a chain of three common-emitter amplifiers, each using emitter degeneration. A change of the emitter resistance is used to change the amplifier gain under the direction of the microcomputer.

The nominal gain of the complete circuit is −10 dB, with Q2018, Q2042, and Q1062 biased off. This provides a nominal −12 dBm output. In this condition, control pins V and Y are high, causing switching transistors Q2018, Q2042, and Q1062 to be cut off.

Q2018 and Q2042 are turned on, when pin V is low, increasing the total gain of the first two amplifiers 20 dB. Potentiometer R2023 (20 dB Gain) adjusts the gain shift of the first stage (Q1025) while the gain shift of the second stage (Q1035) is fixed at +10 dB. This adjustment allows the gain shift to be set exactly to +20 dB.

When pin Y is low, Q1062 is saturated. This raises the gain of the third amplifier (Q1043) by 10 dB. Variable resistor R2060 allows the gain shift to be set exactly to +10 dB.

Gain of the 20 dB and 10 dB gain step circuits is controlled by data bits 0, 1, and 2. Data is latched on the output of decoder U3017, on the VR Mother board #2 and when the bits are high, turns on transistor Q4035, Q3035, and Q4037. The resultant low out, turns on the respective gain step circuit. Table 7-4 shows the state of bits 2, 1, and 0 and the gain shifts obtained in the amplifier stages.

The output signal from the 20 dB Gain Steps circuit is applied through an interconnect coaxial cable to the VR Band Leveling circuit.

Band Leveling Circuit (Diagram 20)

The two amplifiers, in the Variable Resolution Band Leveling circuit, correct gain variations through the front end. These band-to-band variations are due to the different modulation products out of the 1st Converter and losses through the Preselector.

Nominal signal input level for band 1 at 100 kHz resolution, in the Min Distortion mode, is −12 dBm. This decreases some for the higher bands. The output level is about −2 dBm. This output level is kept constant by using the microcomputer to adjust the amplification through this circuit for each band.

The two amplifier stages on this board are similar to the 10 dB gain steps circuits. A stage consists of a three-transistor circuit using a differential pair connected to an emitter-follower. The gain is controlled by altering the feedback network.

The first stage (Q2015, Q2019, and Q1025) has a gain range of 13.5 dB by controlling the bias of PIN diode CR2021 in the feedback loop. Bias for this diode depends on a voltage divider network consisting of an array of variable resistors on the VR Mother board #2, A68A2, with the divider network selected by the microcomputer.

The second stage (Q1031, Q1033, and Q1041) is similar, except the gain change is a one step change of approximately 12.5 dB. This gain step occurs in the higher bands (4 through 11). If required, gain change is activated by the microcomputer through user-selected diodes and transistor Q2046.

The spectrum analyzer is normally calibrated with the band 1 gain control resistor set for minimum gain. Gain is then added as required for the higher bands. Data bits 3 through 6 select gain for each band selection.

The output from this board is applied through connector EE to the 2nd Filter Select circuit.

Table 7-4
GAIN STEP COMBINATIONS

Gain Required	Data Bits			10 dB Steps	20 dB Steps	
	2	1	0	Pin N (10 dB)	Pin V (20 dB)	Pin Y (10 dB)
10 dB	0	0	1	0	1	1
20 dB	1	0	0	1	0	1
30 dB	1	0	1	0	0	1
40 dB	1	1	1	0	0	0

Digital Control Circuits (Diagram 18)

The digital control circuits on the VR Mother board #2 (A68A2) provide address and data decoding for resolution bandwidth, gain step selection, and band identification for the band leveling control.

Address and data valid lines from the analyzer address bus are applied to address decoder U4022. Data bit 7 is applied to the select input A, of the decoder, as a supplemental address bit. This bit is used to select either an address to latch data for the resolution bandwidth selection or an address to latch data for band identification and gain step selection.

Data from the analyzer data bus is applied to data latches U3010 and U3017. Note that only data bits 0, 1, and 2 are applied to latch U3010.

Latch U3010 stores the data that selects the filters in the 1st and 2nd Filter Select circuits. Outputs from pins 2, 19, and 16 of U3010 are applied to the decimal decoders in the filter select circuits through edge connector pins G, F, and E to control the filter selection.

Data that selects gain steps and identifies the selected frequency band for control of the band leveling function is latched on the output of U3017. Output on pins 2, 5, and 6 of U3017 (corresponding to data bits 0, 1, and 2) are applied through transistors Q4035, Q3035, and Q4037, respectively, to the gain switching circuits in the 10 dB and 20 dB Gain Step circuits.

The output on pins 15, 16, 19, and 12 of U3017 (corresponding to data bits 3, 4, 5, and 6) are applied to band decoder U3023, an open collector decoder. If band 1 is selected, pin 1 of U3023 goes low and if band 2 is selected pin 2 goes low, etc. This output in conjunction with a 7.5 V reference source (provided by operational amplifier U3038B and driver transistor Q3036) produces a voltage at the output of a operational amplifier, U3038A. This voltage is indicative of the gain that must be set for each band so the level remains constant at the output for all bands.

The output of U3038A is applied through edge connector pin BB to the gain control PIN diode in the Band Leveling circuit. For example; when band 1 is selected (U3023 pin 1 low), current through Band 1 Gain potentiometer, R2031, and the emitter of Q3036 sets the voltage through R2033 to the summing input of operational amplifier U3038A. The increased output of U3038A increases the current through band leveling PIN diode CR2021 and increases the gain of the stage according to the setting of Band 1 Gain potentiometer R2031. In similar fashion, the other potentiometers (R3034, R3030, R3019, 3022, R3024, R3026, R3032, R3029, and R3028) allow adjustment of the current for each of the other bands.

An additional diode may be added to each decoder output, for bands 4 through 10, to transmit the low, via edge connector pin DD, to the gain control transistor, in the Band Leveling circuit, and increase the gain more for these bands. These diodes are CR3022, CR3023, CR3024, CR3025, CR3031, CR3027, and CR3026. If needed these diodes are installed during instrument calibration.

+5 V Regulator Circuit (Diagram 18)

The +5 V regulator circuit, U3041, supplies a noise-free +5 V source for the VR system. This is required because of noise in the +5 V main supply.

2nd Filter Select Circuits (Diagram 21)

Circuits on the 2nd Filter Select board (A68A8) operate in conjunction with the circuits on the 1st Filter Select board (A68A4) to set the overall system bandwidth. Banks of filters are selected under the master microcomputer control. Data bits 0, 1, and 2, from the data bus, are applied to decimal decoder U3070 (which outputs a low on the appropriate output pin to enable the selected filter). Bandwidth selections are 1 MHz to 1 kHz in decade steps.

Filter bandwidth selection is shown in Table 7-3. Filter selection is accomplished as previously described for the 1st Filter Select circuit.

The input signal, from the Band Leveling circuit via jumper EE, is routed through the selected filter to the Post VR Amplifier circuit, via jumper JJ. Nominal loss through the filter circuit is approximately 13 dB, with internal adjustment compensation for variations

between the filters. The output level is nominally −14 dBm.

An important difference between the 1st and 2nd filter select circuits is the addition of a gain adjustment in all except the 100 kHz circuit. This adjusts the amount of attenuation through the other filters and matches the output level to that of the 100 kHz filter. Since the Band Leveling circuit furnishes compensation gain to obtain equal signal levels for all bands, this adjustment compensates for variations between the filters.

No filter is used in the 1 MHz path because of the 1 MHz band-pass filter (FL 36) between the 2nd and 3rd Converters and the 1.2 MHz filter in the VR Input stage. An adjustable attenuator, adjusted by R1065, is used to provide initial signal leveling to compensate or offset the gain loss associated with the other filters in the resolution circuits.

The 100 kHz filter is a double-tuned LC circuit designed for a good time-domain response shape. The filter is tuned with composite variable capacitors consisting of small air variables paralleled with switched fixed capacitors. A third variable capacitor may be adjusted to establish the desired bandwidth. For Option 07 instruments, a similar 300 kHz filter replaces the 100 kHz filter.

The 10 kHz filter uses a two-pole monolithic crystal filter. The impedances at the input and output are matched to 50 ohm by T5047 and T7050. An attenuator that contains Gain adjustment R3039 is included at the filter input for filter variation compensation.

The 1 kHz filter is also a two-pole monolithic crystal with impedance matching transformers T4044 and T7043. A Gain adjustment is also part of the attenuator.

Post VR Amplifier Circuit (Diagram 21)

The Post VR Amplifier circuit provides the final VR system gain to bring the signal to the required +6 dBm output level, and provides the final band-pass filtering. The circuit consists of two stages of gain followed by a filter.

The input signal, at a nominal −14 dBm, is applied through toroid transformer T2063 to the base of common-emitter amplifier Q2056. Gain adjustment R2038, in the emitter circuit, sets the Post VR amplifier gain. The output is transformer coupled, by T1059, to the base of feedback amplifier Q1048. This circuit includes emitter degeneration through resistor R2042 and collector-to-base feedback through resistor R1052. The collector feedback helps to provide a well-defined output impedance of 50 ohms. Input impedance is a function of transformer T1059 and resistor R1058 across the primary winding.

From the final amplifier, the signal is applied through the 1.2 MHz band-pass filter comprised of capacitors C2033 and C2018 and the components between. This filter is a double-tuned design with an insertion loss of approximately 2 dB.

As an aid to understanding the overall VR system functions, it is helpful to understand some aspects of filter design. When designing a wide bandpass filter, where the pass band is ten percent or greater than the center frequency, stop-band attenuation becomes a severe problem in two-pole filters. The result is that a given filter design will degenerate into either a high-pass or a low-pass filter. The design of the filter in the Post VR Amplifier circuit degenerates into a low-pass unit. However, since the VR system includes a band-pass filter at both the input and the output, and since the input filter in the Input circuit degenerates into a high-pass unit, the overall VR system exhibits clean stop-band performance. The output signal from the filter is applied through coaxial connector J682 to the Log Amplifier. The output level is nominally at +6 dBm.

LOG AMP and DETECTOR (Diagram 22)

The Logarithmic (Log) Amplifier and Detector accepts input signals from the VR circuits with a dynamic range to 90 dB. The signals are amplified so the output is proportional to the logarithm of the input. The output is then applied to a linear detector which outputs a video signal. By controlling the compression curve characteristics, each dB change in the input signal level results in an equal increment of change in the output. In the 10 dB/div mode, each division of displacement on the screen represents a 10 dB change of input signal level.

Table 7-5
PROGRESSION OF GAIN REDUCTION

Input Level	Point 1	Point 2	Point 3	Point 4
	Beyond Logging Range			
X−10 dB	0.00316	0.01	0.316	0.1
				0.216
X Level	0.01	0.316	0.1	0.316
				0.684
X+10 dB	0.0316	0.1	0.316	1.0
			0.684	0.684
X+20 dB	0.1	0.316	1.0	1.684
		0.684	0.684	0.684
X+30 dB	0.316	1.0	1.684	2.368
	0.684	0.684	0.684	0.684
X+40 dB	1.0	1.684	2.368	3.052
X+50 dB	3.16	Beyond Logging Range		

Log Amplifier Circuits

The Log Amplifier circuits logarithmically amplify the input signal from the VR circuits and apply the output signal to the Detector circuit. This circuit consists of seven ac-coupled amplifier stages. Each stage has two gain values that depend on signal amplitude. In addition, the first three stages have an extra automatically selected gain value. The combined circuits provide high gain for low-level signals and low gain for high-level signals. For the output signal to be proportional to the logarithm of the input, more gain is required for a change from −80 dBm to −79 dBm than a change from −1 dBm to 0 dBm. For a given stage of the circuit, the gain starts at approximately 10 dB for a low-level signal and decreases to unity as the input signal level increases. In the first three stages, the gain becomes less than unity as the signal amplitude increases.

Input signal levels nominally range between −84 dBm and +6 dBm. As the signal level increases, the gain decrease begins with the final stage and proceeds, in succession, back through the remaining six stages to the first. Each stage initially produced approximately 10 dB of gain. That gain was reduced to unity, so the total gain reduction is 70 dB. With further increases in input signal level, three more gain change steps take place. The gain of the first three stages is reduced below unity approximately 7 dB for each stage. This reduction starts with the first stage and proceeds to the third, to provide an additional gain reduction of approximately 20 dB.

As the input signal increases from −84 dBm to +6 dBm, the gain through the amplifier decreases logarithmically so that the output signal is exactly proportional to the logarithm of the input. This is accomplished through a system of series diode limiting in each stage, with a second set of diodes for extra limiting in each of the first three stages.

The following description of a simple three-stage log amplifier, with one gain step in each stage, provides an aid to understanding the concept of a logarithmic amplifier. For the example amplifier described and shown in Figures 7-8, 7-9, and 7-10, the gain of each stage is 3.16 V (10 dB) up to an output level of 1 V peak, then unity for output levels greater than 1 V peak; that is, each stage uses one breakpoint. That breakpoint voltage is used for ease of illustration; the actual breakpoint voltage is significantly lower.

The amplifier is shown in Figure 7-8. The source has a step attenuator that allows the input signal to be incremented in 10 dB steps. Table 7-5 shows the progression of gain reduction above 1 V at each amplifier output. Note that with each input level change of 10 dB, the output change at point 4 is 0.684 V. The gain curve for one stage is shown in Figure 7-9. Also note that when the level at point 1 is increased beyond 1 V, it is beyond the logging range of the amplifier. Similarly, if the input level is decreased 10 dB below the minimum input level, the output increment is different. A curve of the logging range is shown in Figure 7-10.

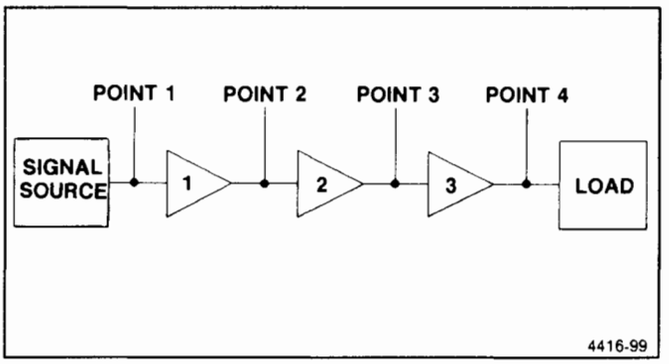


Figure 7-8. Block diagram of a three stage log amplifier.

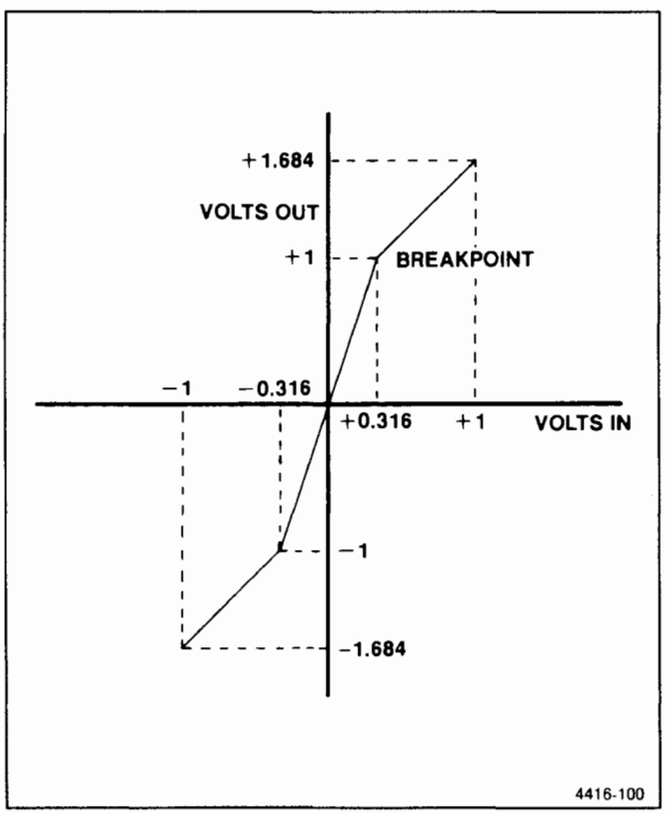


Figure 7-9. Log amplifier gain curve showing break points.

The signal is applied from the VR circuits to input preamplifier Q3105, in the Log Amplifier circuits, through coaxial connector P621. The input preamplifier provides transfer from 50Ω to the high- impedance input of the first amplifier stage. The input signal is also applied to transistor Q2105, a common-base amplifier that acts as a buffer to supply the 10 MHz IF signal to the rear panel connector.

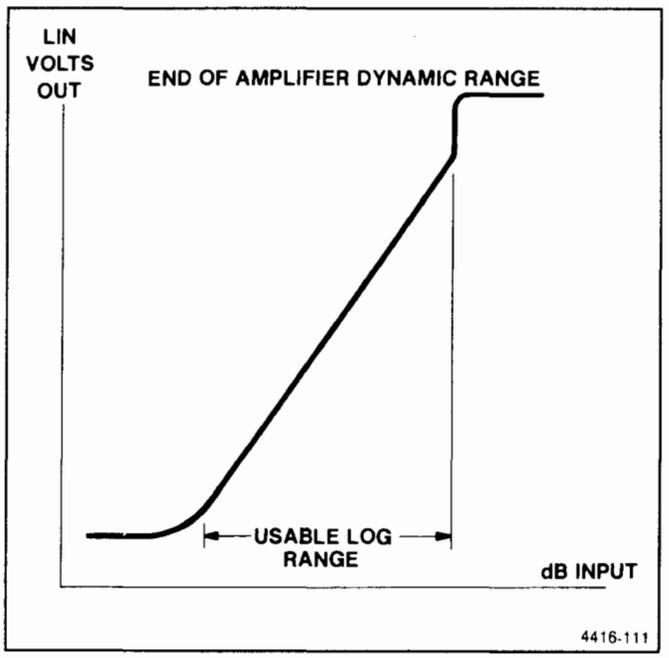


Figure 7-10. Curve showing end-of-range for a log amplifier.

From the input preamplifier, the signal is applied to the first of seven cascaded amplifiers that consist of Q3100/ Q1095, Q3090/Q1080, Q3075/Q1070, Q3055/Q1050, Q3045/Q1035, Q3030/Q1025, and Q3015/Q6010, plus the associated circuitry. These stages are similar, except that the first three stages contain an extra set of diodes for a second gain step.

Typically, when the input level to transistor Q3015 is less than approximately 60 mV peak-to-peak, the transistor conducts enough to maintain forward bias on series limiting diodes CR4015 and CR4012. The RF signal path at that level is through both diodes, capacitor C5014, and resistors R4010H, R4010B, R4015, and R4010D, to common-base amplifier Q6010. The gain of the stage, under these conditions, is approximately 10 dB. As the input signal voltage increases, more current flows through CR4015 to increase the reverse bias of CR4012. This sharply reduces the stage gain to unity. The signal current then flows only in R4010B, R4015, and R4010D. This change takes place during the positive-going portion of each cycle. The opposite occurs during the negative-going portion of the signal above the minimum input level. As the input signal increases beyond the point at which the gain of the final stage decreases to unity, the same sequence occurs in the preceding stage, Q3030/Q1025, and in succession, back to the first stage, Q3100/Q1095.

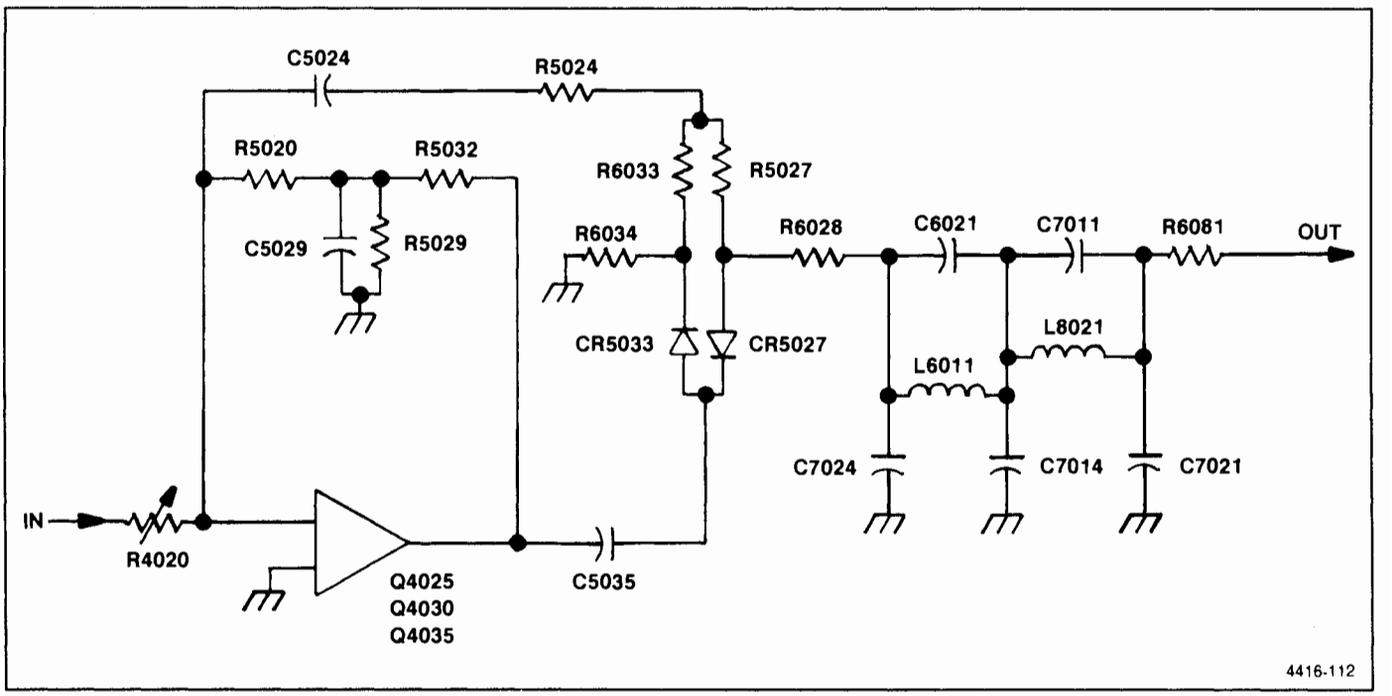


Figure 7-11. Simplified detector circuit.

Signal levels above this point activate the second tier of gain reduction in the first three stages. Each stage incorporates a second set of diodes that reduces the gain by another 7 dB. In the first tier of gain reduction, reduction started at the last stage and proceeded to the first; in the second tier, the reduction starts at the first stage and proceeds to the third.

In the first stage, diodes CR3089 and CR2087 are forward biased when the stage is in the unity gain mode. Limiting occurs in the same manner as previously described, with a further increase in input signal level, and results in less than unity gain through the stage (approximately 1/3). The one-two-three reduction sequence is established by the values of pull-down resistors R3082, R2076, and R2066.

Detector Circuit

This circuit detects and filters the output of the Log Amplifier circuit, and produces the VIDEO signal that is transmitted to the Video Amplifier circuits. The circuit consists of an operational amplifier with a diode detector in the feedback path and a low-pass filter at the output.

Although the circuit is called an operational amplifier, it is not easily recognized as such. It is made up of grounded emitter amplifier Q4025 and a differential amplifier that consists of Q4030 and Q4035. The summing node for the negative input is the base of Q4025 (the positive input is at the grounded emitter of Q4025). Also, the differential amplifier is designed for high impedance output to allow the current that is available from Q4025 to drive the operational amplifier very rapidly during the period when both detector diodes, CR5033 and CR5027, are effectively open circuited; that is, when the output is near 0 V. When neither diode is conducting, it is necessary that the output change rapidly through that zone. Note that the network consisting of resistors R5032, R5029, R5020, and capacitor C5029 is included to stabilize the point of dc operation.

Figure 7-11 shows a simplified schematic diagram of the detector circuit. As shown in this diagram, detector diodes CR5033 and CR5027 are used, but only the negative half cycle is taken as the output (from CR5027). The output from the collector of transistor Q4035 is applied to the diodes through capacitor C5035. Ac coupling is used on both sides of the detector to prevent temperature coefficient effects of the operational amplifier from affecting the detector output. This isolation occurs when the detector charges and discharges capacitors C5035 and C5024, by the current induced in each half cycle of the signal without a change to voltage level.

As shown in schematic Diagram 22, the positive-going output signal from the detector is applied to the Video Amplifier through a low-pass filter that consists of capacitors C7024, C7014, C7021, C7011, C6021, and inductors L6011, L8021.

DISPLAY SECTION (Diagram 6)

FUNCTIONAL DESCRIPTION

The display section consists of the following major blocks:

- Video Amplifier
- Video Processor
- Digital Storage
- Deflection Amplifiers
- Z-Axis
- CRT Readout

The Video Amplifier processes the detected IF signal through logarithmic amplifiers for log displays or linear amplifiers for linear displays, and provides pulse stretching if selected for narrow pulsed signals.

The Video Processor provides band leveling to correct front-end unflatness through the bands, video filtering for noise averaging, out-of-band blanking to clamp the display to the baseline when the sweep is outside the range of the selected band, and video marker capability for use with a TV sideband adapter.

The Digital Storage digitizes the video and sweep signals and stores the data in memory. Stored data is then converted to analog signals for the Deflection Amplifier and Z-Axis circuits.

The Deflection Amplifier provides the drive voltages for the CRT. This includes vertical and horizontal deflection signals as well as readout characters from the CRT Readout board.

The Z-Axis circuits receive and decode data from the microcomputer; accept control levels from the front-panel beam controls and generate unblanking signals to control the display appearance, brightness, and focus; detect power failure; monitor the instrument voltage supplies; and record the elapsed operating time.

The CRT Readout circuits generate the alphanumeric characters (letters and numbers) for the display.

VIDEO AMPLIFIER (Diagram 23)

Video signals, from the detector and log amplifier in the IF section, are received by the Video Amplifier. In the logarithmic mode, the signals are amplified linearly and applied to the Video Processor. In the linear mode, exponential amplification converts the logarithmic gain characteristic to linear function. In either mode, baseline compensation from the Video Processor is applied to the video signal to compensate for any unflatness in the front-end response. The pulse stretch circuit at the output of the Video Amplifier alters narrow pulses so data can be acquired and displayed by the Digital Storage logic. Signal amplitude offset circuits provide display offset for the "Identify" mode operation.

Log Mode Circuits

The log mode circuits process VIDEO signal from the Log Amplifier, and add offset for selecting that segment of the log amplifier gain curve to be displayed. The circuits also select screen display gain steps from 1 dB/div to 15 dB/div.

The VIDEO and the VIDEO 1 signals are summed at the input to operational amplifier U4090A. Front-end unflatness is compensated by the VIDEO I signals, which are equal and opposite in amplitude to the unflatness. The two signals are also summed with the reference level, set by R4071, and the output of the digital-to-analog converter (DAC) U5041.

The DAC converts the microcomputer commands to an offset signal that selects the location on the log amplifier curve for the display (see Figure 7-12). In dB/div or log display, a change in Vertical POSITION control produces an effect, after the log amplifier, that is the same as a signal level or gain change before the log amplifier. Instead of using a large amount of linear gain before the log amplifier, the output of the DAC (U5041) effectively moves the display up or down along the log curve. This process is called offset. Offset produces the same effect as varying the POSITION control except the display position does not change, only the signal level required to reach the reference level changes.

This process allows the linear gain to change while the top of the screen is kept constant, and it must also allow any 16 dB segment (in the 2 dB/div mode) to be displayed. Nominally, the log amplifier operates with +6 dBm at the top of the screen.

The output of U4090A is equivalent to 20 mV/dB. Full screen is 2.2 V. At 2.2 V, the output of variable log gain amplifier U4090B is 0 V. This is the only voltage at which the feedback circuit switching network resistors of preamplifier U4090B can be switched without changing the output voltage. (The switching network is described later in this discussion.) The 2.2 V output of U4090A is adjusted to full screen by Input Ref Lvl potentiometer R4071.

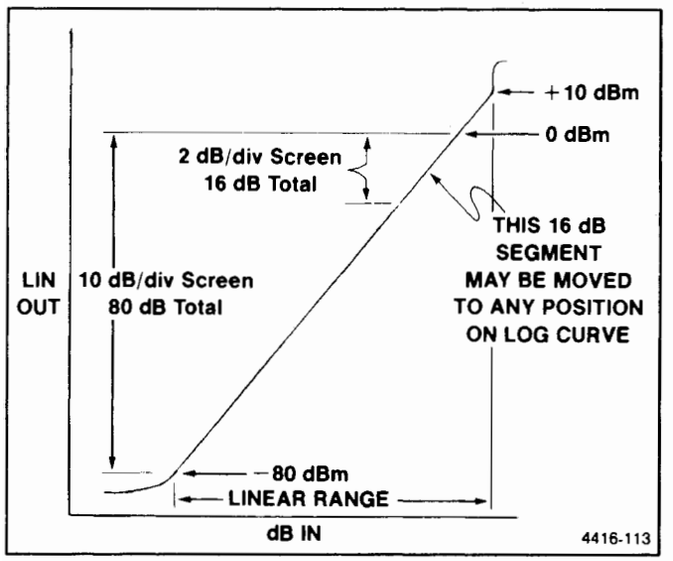


Figure 7-12. Selection of display position on the log scale.

From U4090B, the output signal is applied through FET Q5090 (if that transistor has been turned on by data bit 5 when it is high) to operational amplifier U4090C, pin 10. The signal then travels through emitter follower Q4100 to the Video Processor via the LOG CAL adjustment on the front panel. Output Ref Lvl (output reference level) potentiometer R4081, in the input circuit to U4090C, is adjusted so the output level is a full screen display after the Input Ref Lvl potentiometer R4071 is set for no change in the output of U4090B when switching between the 10 dB/div and 2 dB/div modes.

The basic adjustment sequence for the potentiometers is as follows:

1. The digital-to-analog converter output voltage is adjusted by the front-panel LOG CAL control so that the output is appropriate for 10 dB/div.

2. The Log Amplifier detector circuit Log Gain R4020, is adjusted so the Log Amplifier output agrees with the digital-to-analog converter output.

3. Input Ref Lvl potentiometer R4071 is adjusted a constant for a constant output level from U4090B, for both the 10 dB/DIV and 2 dB/DIV display modes.

4. Output Ref Lvl R4081 is then adjusted for a full screen display.

The gain switching network provides for 15 resistance values to be switched into the feedback path of variable log gain amplifier U4090B. The network consists of FET switches Q4075, Q4070, Q5070, and Q5075, and resistors R6080, R6074, R6073, and R6082. The FET switches, controlled by data bits 0, 1, 2, and 3 from the analyzer data bus, switch in feedback resistors for U4090B in 15 value combinations determined by the binary content of the four data bits.

Linear Mode Circuits

The linear mode circuits accept the log preamplifier U4090A output and rescale the signal level to linear values. Since no switching is provided by the Log Amplifier circuits (i.e., all signals are logarithmically scaled), the signal level must be re-exponentiated to operate the system in the linear mode. High gain is required at the top of the screen and low gain is required at the bottom of the screen to offset the characteristics of the Log Amplifier circuits.

In addition to the signal path described for the log mode circuits, the output from preamplifier U4090A is also applied to linear mode operational amplifier U4090D, with a successive resistor network in the feedback path. From this amplifier, the output signal is applied through FET Q5095 (if that transistor has been turned on by data bit 4 from the analyzer data bus being a 1) to the summing node at the input of output amplifier U4090C. After this point, the signal path is identical to that of the log mode description.

Starting at the signal level that represents the top of the screen (0 V) at the output of linear mode amplifier U4090D, the operation of the network is as follows.

With a +6 dBm input from the Log Amplifier to the Video Amplifier, the output of U4090D is 0 V. At that level, the feedback path is only through resistor R4097. The other feedback resistors (R4096, R5103, R5105, and R5107) are not in the path, because the switch transistors are biased off by the bias network consisting of resistors R5111, R4109, R4107, R4105, and R4103, plus diode CR4103. (The diode is included for temperature compensation purposes.) As the display moves away from full screen, the output voltage of U4090D increases and turns transistor Q6115 on. This places R4096 in parallel with R4097 to reduce the gain. As the voltage output increases, transistors Q6110, Q6090, and Q6095 start to conduct in sequence, adding resistors R5103, R5105, and R5107, respectively, across the feedback path. This effectively reduces the gain of U4090D exponentially. The reaction characteristics of the transistors smooth the step transitions, to produce a smooth exponential gain curve.

Pulse Stretch Circuit

The pulse stretch circuit consists of FET switch Q7110 and the associated components in the feedback path of output operational amplifier U4090C. When the pulse stretch mode is not selected (data bit 7 on the

instrument data bus is low), pin 13 of U6060 pulls down to −15 V, and Q7110 is biased off. This removes C8104 from the circuit and also supplies sufficient negative bias though R7105 to keep CR8107 forward biased. With CR8107 on, the feedback loop for U4090C, through Q4100 and R7094 is closed so the signal output will fall as fast as its rise.

When the pulse stretch mode is selected (data bit 7 going high), the open collector output of U6060 (pin 13) is allowed to float. This turns Q7110 on which completes the path for C8104 to ground. During signal rise time, C8104 now charges through the low impedance of CR8107. The feedback path for U4090C is still closed which provides a fast rise time. When the output of U4090C begins to fall, CR8107 turn off and the signal fall time is now a function of the RC time constant of R8106 and C8104, since the feedback loop for U4090C is now open. Diode CR7103 turns on to prevent U4090C from slewing to far negative.

The identify offset circuit shifts the display when the identify feature is in operation so true and false signals can be identified. This feature is implemented elsewhere in the analyzer, except for the offset. When the "Identify" feature is in operation, it allows the operator to distinguish between responses which result from signals at the analyzer center frequency (true signals) and those that are produced by other harmonic conversions (false signals). This is accomplished by moving the 1st and 2nd LO frequency an equal and opposite amount, related to the 1st LO harmonic used, or by moving the 1st LO twice the IF divided by the harmonic number (N), on every other sweep. The result is that false signals will shift a significant amount horizontally on the display while true signals will remain within close approximation to each other. The offset circuit shifts the alternate or "Identify" sweep vertically (down approximately 2 divisions). This offset is accomplished by the microcomputer setting DB 6 high, during "Identify" sweep, so the open collector output of U6060 (pin 14) goes from −15 V to open. This removes the current normally flowing in R7097 from the summing node of U4090C and causes a −1.2 V or 2 division shift in the VIDEO 2 output level of Q4100.

Digital Control Circuit

The digital control circuit provides the control signals that select the various Video Amplifier functions. Addresses 78 and 79 are decoded by U6070 and sent through inverter U5070 as clock or enabling signals for gain latch U6040 and mode latch U6050.

Gain latch IC U6040 is an 8-bit latch that supplies command data to the 8-bit DAC, U5041, to offset the Log Amplifier output signal. Mode latch U6050 is an 8-bit latch that supplies command data through buffer U5060 and U6060 to select the resistors in the dB/div switching circuit and to select identify, pulse stretch, and log or linear mode.

VIDEO PROCESSOR (DIAGRAM 24)

The Video Processor performs four functions. The first is compensation for flatness variations in front-end response. The second is video filtering, which provides the selection of six video bandwidths (30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz) under control of the instrument microcomputer. The third function is out-of-band blanking, which blanks the upper and lower ends of the local oscillator swept frequency range to provide a selected window for the display. This function is also controlled by the microcomputer. The fourth is the capability to generate a negative-going ditch marker on the video display for interfacing with a 1405 TV Sideband Adapter.

Interface with 1405 TV Sideband Adapter

The TEKTRONIX 1405 TV Sideband Adapter is a specialized tracking generator that is used with the Spectrum Analyzer to analyze the response of a television transmission system. The Spectrum Analyzer monitors the RF output of the transmitter while the sideband adapter drives the video input of the system. The video input may be at the transmitter site, the head end of the studio-transmitter link, or the video switcher in the studio. The sideband adapter must be connected to the 1st LO of the Spectrum Analyzer by a short length of coaxial cable.

The system in Figure 7-13 depicts a TV transmitter operating on Channel 10 with a video carrier at 193.25 MHz. The sideband adapter is tuned to Channel 10. The Spectrum Analyzer is tuned to 195.25 MHz with a span setting of 1 MHz/Div (for purposes of illustration, the sweep is assumed to be halted at the center frequency of the analyzer).

The sideband adapter applies a 2 MHz signal to the AM modulator of the video transmitter. The modulator produces a lower sideband at 191.25 MHz, a carrier at 193.25 MHz, and an upper sideband at 195.25 MHz. This signal is amplified, filtered, and combined with the FM aural signal. The composite signal is sensed by a RF pickup and applied to the RF Input of the Spectrum Analyzer.

The 1st Converter applies the composite signal to the 1st mixer. The composite signal is mixed with a 2.26725 GHz signal from the 1st LO, forming three products. The subsequent stages of the analyzer accept only the 2.072 GHz product and reject the rest. For frequencies used in this example, the accepted product is the difference between the 1st LO and the upper sideband of the TV signal.

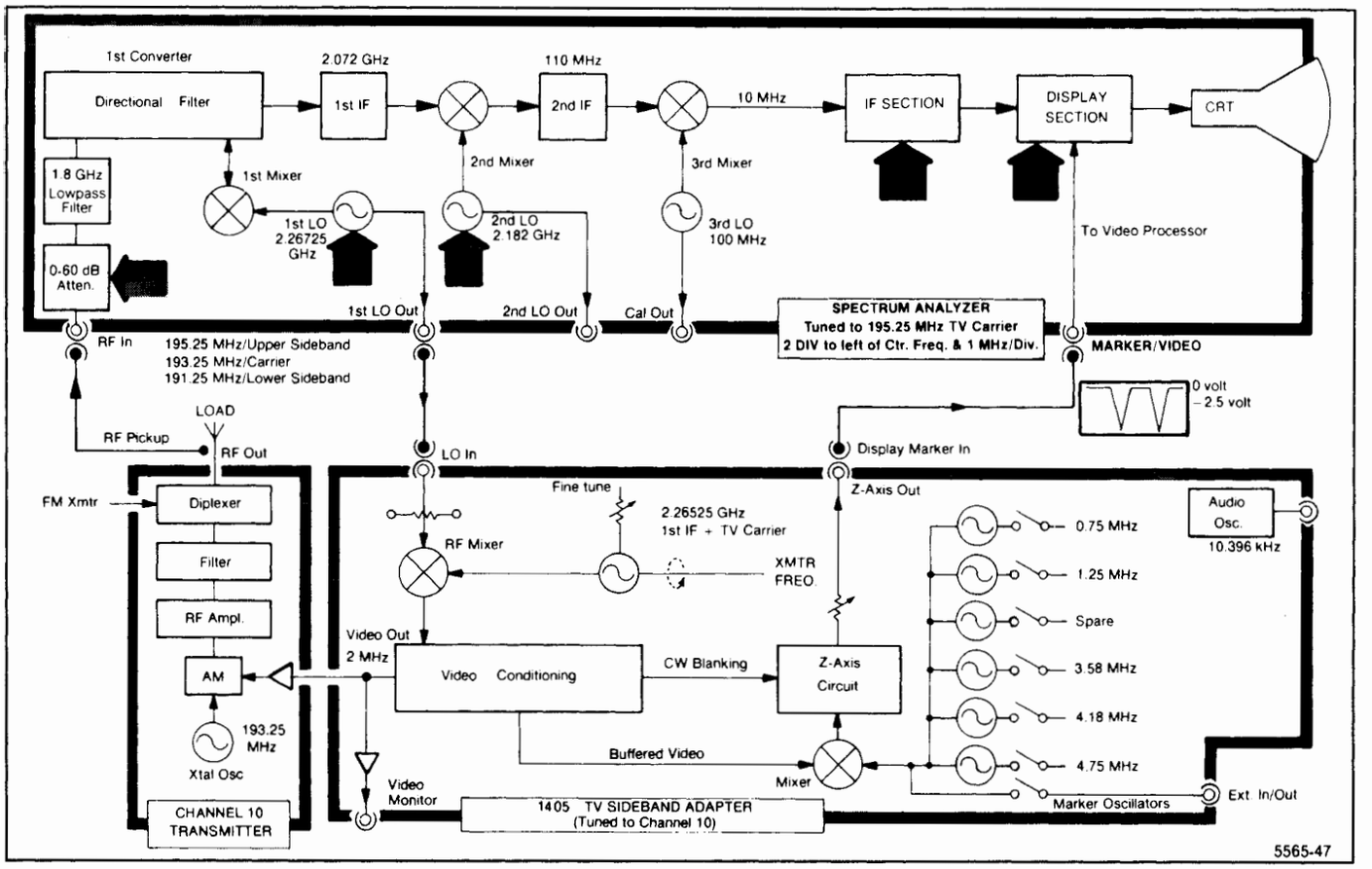


Figure 7-13. Functional diagram showing the Spectrum Analyzer and 1405 TV Sideband Adapter System.

The product is converted twice more, amplified, filtered, log amplified, and detected. This detected signal is applied either directly to the video amplifiers of the crt or to digital storage.

The Spectrum Analyzer 1st LO signal is applied to the RF mixer of the sideband adapter. The 2.26525 GHz signal from the tunable LO is subtracted from the 2.26725 GHz signal from the Spectrum Analyzer LO, yielding a 2 MHz product. This video frequency signal is conditioned with sync and blanking signals and applied to the video input of the TV transmitter.

When the Spectrum Analyzer is sweeping, the video signal starts at 3 MHz, falls to 0 Hz, and rises up to 7 MHz. During this interval, the analyzer displays the lower sideband as it moves toward the carrier, displays the carrier, and then displays the upper sideband moving away from the carrier. Since the Spectrum Analyzer and 1405 TV Sideband Adapter system is similar to a tracking generator system, it rejects noise and uncorrelated signal. This allows normal in-service use of the transmitter by adding a low level (1 to 3 IRE units) cw signal to the video or by using full levels with a VITS inserter.

The sideband adapter can insert frequency markers at preselected deviations from the carrier frequency. Six selectable crystal oscillators have their outputs mixed with video signal and applied to a Z-Axis circuit. This circuit produces two negative pulses as the video signal sweeps through the crystal oscillator frequency. These pulses are applied to the spectrum analyzer marker input, where they appear on the crt as two notches on either side of the marker frequency. The sideband adapter allows the width and depth of the notches to be adjusted with the Width and Intensity controls.

Video Marker

The Z-Axis signal from the 1405 Sideband Adapter connects to the MARKER input on the spectrum analyzer rear panel. This negative-going signal flows through the Accessories and Mother boards to the Video Processor board. Here, the signal drives the emitter of Q4060 and turns the transistor on, pulling the VIDEO OUT line down. This produces a notch in the video signal of the display to signify the location of the marker on the display.

Video Leveling

A minor slope in frequency response, caused by the 1.86 GHz low-pass filter in the front end, is corrected with band 1 Slope adjustment R1012. When operating in band 1, contacts 6 and 7 of U3025 are closed; therefore, a portion of the PRESELECTOR DRIVE signal is applied to the VIDEO 1 output signal, providing the offset necessary to correct slope difference.

Video Leveler Circuits

Video leveling compensates for analyzer front-end microwave circuit characteristics that cause unflat response in band 4 (5.4 GHz to 18 GHz). Since band 4 is a multiplied band, any unflatness is accentuated. Leveling is accomplished through programmable perturbation of the display baseline that is opposite in direction to the flatness error. As the signal power output decreases, the baseline rises an equal amount to compensate, and as power output increases, the baseline falls an equal amount. The perturbation is produced by a normalizer integrated circuit that produces 19 evenly spaced values of the input voltage, with each value corrected to compensate for unflatness.

The PRESELECTOR DRIVE signal from the 1st LO driver circuits is applied to a translation circuit that consists of two current drivers (U3045A and half of Q3038, plus U3045B and the other half of Q3038). The PRESELECTOR DRIVE signal is directly related in amplitude to displayed analyzer frequency. The nominal +10V to −10 V excursion voltage versus frequency curve, in maximum span, relates to the full bandwidth. This 20 V maximum excursion is scaled to a precise current (from 1 mA at +10 V to 0 current at −10 V) that is applied to the normalizer IC to generate the baseline perturbation. Actual signal scaling is done by current driver U3045A/Q3038. The output signal is applied to the normalizer SWP IN input, pin 5 of U2039. The second current driver, U3045B/Q3038, generates a 2 mA reference current for the normalizer. Horizontal Freq adjustment R1069, in the input translation circuits, shifts the 19 evenly spaced points up or down in frequency to compensate for unflatness.

Normalizer IC U2039 operates as a shaper and contains 19 transistors that turn on and off in sequence as the current input to pin 5 decreases from 1 mA to 0. Each collector is connected to a potentiometer that allows output trimming. Potentiometer R1061 is active with no current, and R1013 is active at 1 mA. The trimming operation is described later.

From the normalizer, the output is applied through a jumper switch to buffer amplifier U2055B, which has a gain of five, then to offset amplifier U2055A. This amplifier has a gain of two, but its primary purpose is to offset the 0 to +5 V (normal), 0 to −5 V (invert), buffer output to the levels required by the Log Amplifier circuits. The range required by the Log Amplifier is 0 to −10 V. The output voltage is a series of linear interpolations of the voltage between adjacent trimming resistors at the outputs of the normalizer. Compensation adjustment R1065 sets correct interpolation.

Jumper plug P2060 selects the input side of buffer amplifier U2055B and proper offset voltage for U2055A. This provides the means to invert the buffer output during the instrument adjustment procedure. The adjustment procedure is described in that section of this manual.

As previously noted, only band 4 requires significant compensation. Selection of band 4 is indicated by data bit 0 switching to a 1 (see the Leveling table at the top right corner of Diagram 24). When DB0 is a 1, pins 3 and 2 of switch U2015 are connected, and the output from offset amplifier U2055A is supplied out as the VIDEO 1 signal.

Minor compensation is required for Band 1, to correct a minor slope caused by the 1.8 GHz low-pass filter and 2 GHz limiter. When pins 6 and 7 of switch U3025 are connected, the PRESELECTOR DRIVE signal is offset by R4023 and R4011 and Band Slope adjustment R1012 to provide an attenuated negative-going ramp to the VIDEO 1 output line. Switch U3025 is controlled by inverter Q4025. Q4025 is activated by data bit 6 going low. As shown in the Video Blanking table on the schematic diagram, DB6 is 1 except when Band 1 is selected.

Video Filter Circuits

Video filtering provides selection of one of six bandwidths, under microcomputer control. As shown in the Video Filter table on Diagram 24, data its 1 through 4 select any of six bandwidths: 30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3Hz. Either wide or narrow-band filtering is selected at the front panel (Wide band is defined as 1/30th of the selected resolution bandwidth and narrow is defined as 1/300th of the resolution bandwidth). The microcomputer makes the selection, based on such factors as sweep rate and total dispersion. With no video filtering (all data bits are 0), the video system bandwidth is 500 kHz.

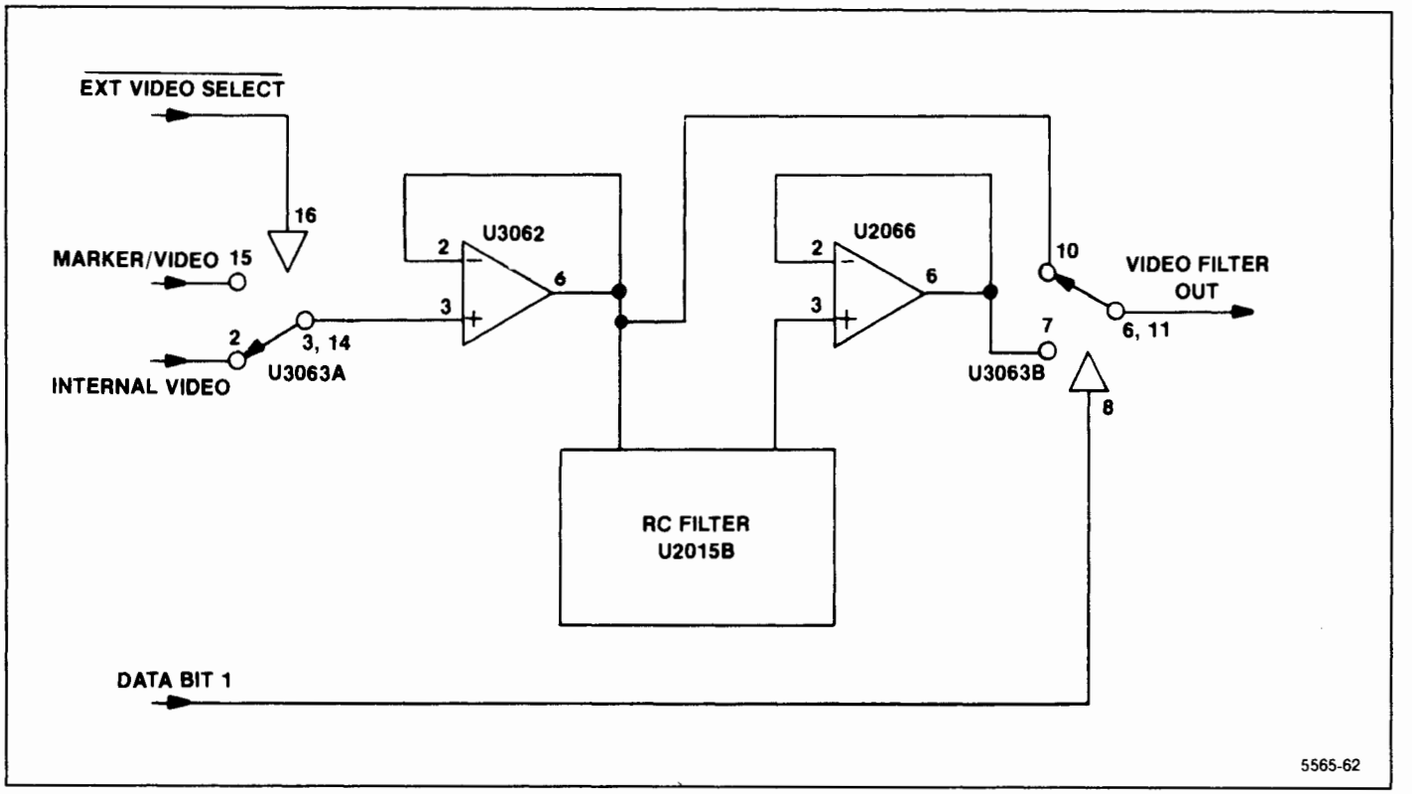


Figure 7-14. Simplified diagram of a video filter.

Table 7-6
FILTER COMPONENT COMBINATIONS

Bandwidth	DB1	R2023	C3026	R2021	R2022	C2016
30 kHz	1	X	X	X	X	
3 kHz	1,4	X	X	X		
300 Hz	1,3,4	X	X			
30 Hz	1,2	X	X	X	X	X
3 Hz	1,2,4	X	X	X	X	X
0.3 Hz	1,2,3,4	X	X	X		X

Two signal inputs (EXT MARKER/VIDEO) can be applied to the video filter circuits. The EXT VIDEO signal, from the rear-panel MARKER | VIDEO connector, is applied to pin 15 of switch U3063A through edge connector pin 53. The INTL VIDEO signal, from the Video Amplifier circuits (via the front-panel LOG CAL control), is applied to pin 2 of U3063A through edge connector pin 51. Note that the internal video sections of switch U3063A are normally held energized (pins 2 and three connected, pins 15 and 14 disconnected) by the +5 V supply through R3064. If the EXT VIDEO SELECT line (from the rear panel ACCESSORIES INTERFACE connector, through edge connector pin 55) is grounded, the external video sections of U3063A are de-energized. When this occurs, the EXT VIDEO signal is applied through, or around, the filter to become the VIDEO FILTER OUT signal at edge connector pin 57. This is shown in the simplified schematic diagram of Figure 7-14.

As shown in Figure 7-14, when no filtering is selected (all data bits are 0), either the internal or external signal is routed through U3062 and around the filter, because the two sections of U3063B are selected by DB1. When DB1 is high, the video is routed through the filter. Some filter value will be selected by bits 2, 3, and 4. These data bits control three sections of switch U2015B to add or delete filter time constants.

The filter consists of resistors R2023, R2021, R2022 and capacitors C3026 and C2016, connected between U3062 and U2066. Table 7-6 lists the filter components in the circuit for each of the six bandwidths. Data bits 2, 3, and 4 are applied to switch U2015B (pins 8, 16, and 9) which selects the components. From U2066B, the signal is routed through contacts 7 and 6 of switch U3063B to edge connector pin 57 as the VIDEO FILTER OUT signal.

Video Blanking

The video blanking circuits allow selective blanking of the lower and upper ends of the local oscillator range. Selective blanking is required because the local oscillator sweeps the full span regardless of the band limits. The video system is designed to effectively open a display window only during the time for display. Data bits 5, 6, and 7, under control of the microcomputer, select the appropriate amount of display for each end.

Video blanking and the PRESELECTOR DRIVE signal (which provides frequency information, in voltage form) are located on the Video Processor board. Switch U3063 incorporates a disable function that, when provided a low input, opens all switch sections regardless of individual section input. This feature allows the VIDEO FILTER OUT signal to be easily blanked at will.

The disable function is controlled by a combination of outputs from comparators U3015A and U3015B. Inputs to these comparators are from the PRESELECTOR DRIVE signal and a combination of voltage dividers that are switch selected under control of data bits 5, 6, and 7. The PRESELECTOR DRIVE signal is applied from edge connector pin 54 through divider resistors R4013 and R4012 to the inverting input of U3015A, and through divider resistors R4014 and R4011 to the non-inverting input of U3015B. These dividers reduce the excursion of the drive signal from (+10 V to −10 V) to (2.5 V to −2.5 V), which is the maximum input level to the comparators.

Input to the non-inverting input of U3015A is from divider resistors R3011, R3012, and selected resistor R4015. The inclusion of R4015 is controlled by DB7 through pins 2 and 3 of U3025. The junction of divider resistors R3011 and R3012 is connected to ground through R4015 for band 2.

Input to the inverting input of U3015B is from divider resistors R4018, R4017, and selected resistor R3028. The inclusion of R3028 is controlled by DB6 through pins 10 and 11 of U3025. The junction of R3011 and R3012 is connected to +5 V through R3028 when it is selected. This switching arrangement of negative and positive levels for comparison with the reduced PRESELECTOR DRIVE signal enables the top and bottom extremes of the frequency excursion to be blanked. The blanking is activated by the disable function of switch U3063, which is controlled by the microcomputer.

DIGITAL STORAGE (Diagrams 25 and 26)

The Digital Storage circuits provide the ability to store and process a signal before displaying it. This allows flicker-free displays, even at the slow sweep rates required for narrow resolution bandwidth measurements. Digitizing the signal also allows signal processing and marker generation.

The processing includes detecting peak amplitudes (Max Hold), storing a signal (Save A), subtracting one signal from another (B−Save A), signal averaging (Peak/Average), and signal comparison (View A and View B). These operations use two memory banks to independently store two complete signals that are each digitized at 500 points across the sweep. Therefore, two signals may be observed simultaneously or processed in separate ways.

The markers are used in a variety of ways. There are two waveform markers that the user sets for various measurements. In addition, an update marker shows where the actual sweep is with reference to the refreshed display.[1]

Four instrument bus addresses are associated with Digital Storage. Addresses 7A and 7B are write addresses. FA and FB are read. These addresses are shared by both the Horizontal and Vertical Digital Storage circuits. Logic on the Horizontal Digital Storage board controls which set is active. 7A on the Horizontal Digital Storage board is further subdivided into 8 subaddresses by 3 bits in address 7B on that board. Address tables in the circuit descriptions for the appropriate boards show details of the Digital Storage addresses

In the Max Hold mode, the highest amplitude at each of the 1000 points in successive sweeps is stored and displayed. In the Save A mode, a signal is stored in one memory for later examination, and is not updated. In the B−Save A mode, the A signal is stored and not updated, then arithmetically subtracted from the B signal, which is stored, but continually updated. In the averaging mode, the display area is divided by a horizontal cursor. Signals above the cursor are peak detected and displayed, and signals below the cursor are averaged. In the View A and View B modes, the contents of the selected memory or memories are displayed.

[1]There are also video markers that may be fed to the rear-panel MARKER | VIDEO input. These video markers are from an external source, and are not part of the digital storage system. See the Video Processor description for more information about the video markers.

Graphical presentation of mathematic functions or experimental data is common. One such graph has a single Y value for each X value. An alternate presentation of the data in this graph would be a table simply listing the X coordinate values along with a corresponding Y value for each X value. To further simplify the graph, if the first X value and the spacing between X values were known (all spaces assumed equal), the two-column table could be reduced to a single column with the X value implied by the position of the Y value in the column. This is the essence of digital storage — to convert a vertical analog voltage (Y coordinate value) to a binary number and insert that number in a stored table. The location of the Y value in the table is determined by the analog sweep voltage (X coordinate value) binary conversion. Once a set of binary numbers that represent values across a waveform is stored to create a table, the waveform can be recreated at any time by conversion of the table values (Y) and positions (X) back to analog voltages that represent amplitude and sweep positions.

The digital storage system uses a Table A and a Table B. Table B is updated every sweep. Table A is also changed unless the Save A mode is selected. There are 500 A values and 500 B values. The spacing between values is the same throughout both tables, but the starting point for Table B is shifted slightly so that when both tables are read, the readout values are interlaced.

When the signals are recreated, the contents of either Table A or Table B can be displayed, or both tables A and B can be displayed. If both Tables A and B are to be displayed, and the Save A mode is selected, the contents of both Table A and Table B are drawn, each display in its own trace. If the Save A mode is not selected, the contents of both Table A and Table B are displayed on one trace, with 1000 value positions across the screen. A third trace option is also available. In the B–Save A mode, the displayed values are those that result from an arithmetic operation and are the difference between the contents of Table A and Table B for each X value of analog sweep voltage.

Since a signal waveform is continuous and a table has discrete X values, an algorithm determines the Y value to be stored for a particular X value. This allows the operator to select one of two methods to determine Y values; peak or average. The Y analog voltage is continuously sampled, with the sampling rate dependent upon sweep speed. For each X value, there are always at least two samples, and there may be as many as 2^{17} samples. From this set of samples, either the largest sample value (peak value) or the mean of all the samples (average value) can be selected. Selection between peak and average is controlled by the front-panel PEAK/AVERAGE control, which sets a dc level that is compared with the analog vertical input to produce the PEAK/AVG logic signal. When the input signal is below the level selected by the front-panel control, the signal is averaged; when the input is above that level, the peak signal is displayed. The dc level appears on the display as a positionable horizontal line. This line is created when the dc level is switched to the analog output line during the cursor cycle by the CURSOR logic control signal.

Superimposed on the cursor line is an intensified spot called the update marker, which indicates the X value at which new Y values are being computed for display update. The update marker is formed when the analog sweep input is compared to the display analog X output. When the two are the same value, the sweep is forced to pause, which increases the marker intensity at that point.

Two custom integrated circuits are the heart of the digital storage circuits. The vertical control IC contains the vertical acquisition and display logic, peak detection, signal averaging, Z-Axis blanking, and special Y-value processing circuits. The horizontal control IC contains the horizontal acquisition address counter, horizontal display counter, 10-bit RAM address multiplexer, and a system control matrix. The other digital storage control circuits consist of two 8-bit digital-to-analog converters, two 10-bit digital-to-analog converters, one 10-bit latch, 8K bits of random access memory, and various auxiliary circuits. Timing is controlled by $\phi 2$ clock pulses (at 1 MHz) from the Processor board to the Horizontal Digital Storage board.

Vertical Section (Diagram 25)

The Vertical Control IC block diagram is shown in Figure 7-15. The vertical analog voltage is converted to a Y binary value by an 8-bit successive approximation register. Nine clock cycles are required for each Y conversion. After the conversion has taken place, the successive approximation register produces the negative-going SYNC signal. Most functions on both the vertical and horizontal control ICs are synchronized by this signal. On the negative-going transition of SYNC, the successive approximation register is reset to 10 00 00 00 (binary) and the next conversion cycle begins. Incoming data bits are latched into the register on the negative-going clock transition. From the register, the output data is applied to the peak and the averaging circuits.

The averaging circuit consists of three groups of circuits; those that accumulate all the Y values for a given X value into a grand total (called the numerator), those that count the number of samples that make up the numerator (this total is called the denominator), and those that subtract and shift to perform the division process.

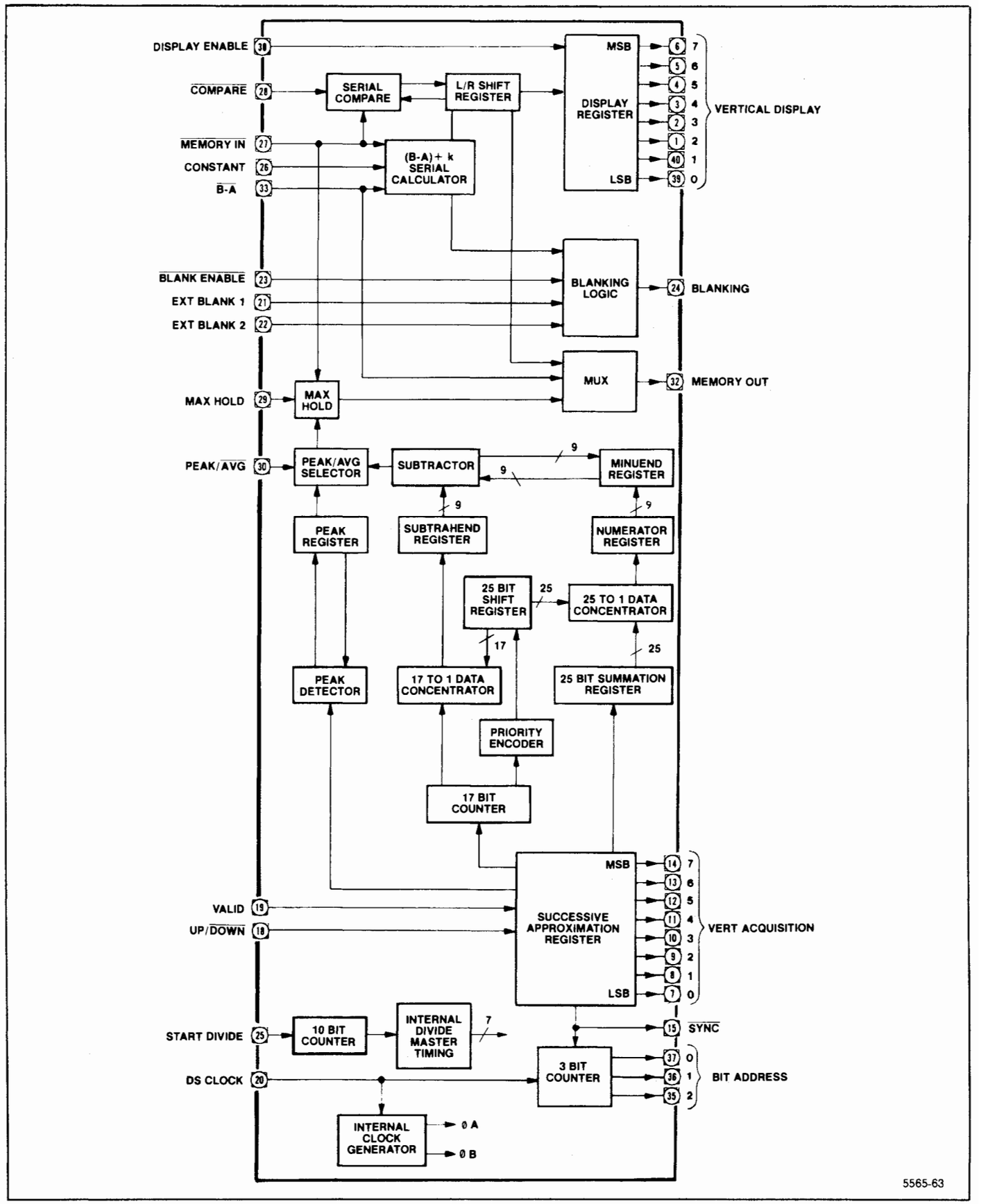


Figure 7-15. Vertical control IC block diagram.

As each new Y value is converted, it is added to the eight least significant bits of the numerator. Each carry from the most significant bit of this addition is counted by a 17-bit ripple counter. The contents of this counter and the 8-bit sum are cascaded to form a 25-bit grand total. Each time a new sample is added to the numerator, another 17-bit ripple counter is incremented to produce the denominator.

A division cycle starts when the horizontal control IC (on the Horizontal Digital Storage board) detects a change in the X value. At that time it generates the ST DIV (start divide) signal. On receiving this signal, and in synchronization with the SYNC signal, vertical control IC U2030 does five things (refer to Figure 7-16):

1. Latches the current numerator in a 25-bit latch (25-to-1 data concentrator) and latches the denominator in a 17-bit latch (17-to-1 data concentrator).

2. Clears the numerator adder circuits (25-bit summation register).

3. Performs a 17-bit priority encode on the denominator and loads a 1 in the appropriate cell of the 25-bit shift register.

4. Loads the latched numerator and denominator serially into the divide circuit (subtractor) using the contents of the 25-bit shift register as a mask.

5. Clears the denominator ripple counter (17-bit counter) to zero.

Ten clock periods are required to load the numerator and denominator into the divide circuit. The cycle starts on a SYNC pulse. The first bit of the quotient is available shortly after the first clock pulse that follows the next SYNC pulse. Division is performed by repeated subtract and shift operations. The quotient is arrived at serially with the most significant bit first. Since only 8-bit accuracy is required, with the priority encoder output used as a mask, the divider circuit is loaded with the 8 most significant bits of the denominator and the 16 most significant bits of the numerator. (Ripple borrow for a 17-bit by 25-bit subtractor would be so long that it would be impractical.)

The peak circuit consists of a peak detector and an 8-bit peak shift register. In operation, the previous peak Y value from the last set of samples is still stored in the peak shift register at the start of a conversion cycle. At that time, the peak detector, which is a serial compare circuit, is set to the state that questions whether the old or new number is larger. Each bit of the new value is then compared with the corresponding bit of the old value, most significant bit first. When one value is found to be larger, a flip-flop is set and the smaller number is gated out of the shift register. The start divide logic signal being true then forces the peak detector to select the new value and ignore the number in the shift register.

The peak/average selector, a multiplexer, selects either the peak or average value to be routed to the memories under control of the PK/AVG signal. The selector output is routed through the Max Hold circuit, which functions like the peak detector. When the MAX HOLD signal is high, the value that is routed to the output multiplexer is the larger of two values; the current memory value at the subject X coordinate or the previously-selected peak or average value.

Timing to set up the divide operation and clear the numerator, denominator, and peak circuit is controlled by a 10-stage counter. Taps are taken from appropriate stages to develop the necessary clear and latch timing pulses.

All data enters and leaves the memory serially. Data read from memory enters an 8-bit shift register and, timed by the SYNC signal, is transferred to the vertical display output latch (display register). The same shift register is used for other purposes, so the DSPL EN (display enable) signal prevents non-display information from being transferred to the output latches. An example of data moving through this shift register is seen in the B–Save A display mode. The A value is first read from memory and stored in the shift register. As the B value is read, the subtraction is done serially and the answer is applied to the shift register. Since the subtraction must be performed with the least significant bit first, a set of exclusive-OR gates change the order of extracting B from memory. The shift register direction is reversed to present the most significant bit to the proper display latch. The shift register output is also applied to the output multiplexer.

In subtraction, the operation performed by the serial calculator is not merely B minus A. The actual expression implemented is (B–A) + K, where K is a serial input external constant specified by the user. This permits zero to be placed anywhere on the screen. To avoid confusion when (B–A) + K results in an off-screen position, the subtractor blanks the display. (The subtractor examines the carry bit and borrow bit when the most significant bit is calculated. If either bit is a 1, the screen is blanked.)

When the Save A mode is not selected and both A and B are being displayed, maximum resolution is obtained (1000 points across the display). If this display includes a very narrow pulse, it is possible that the top of the pulse is only as wide as a single X coordinate. If this maximum value were in the B Table and the Save A mode was selected and B turned off, there would be an apparent drop in amplitude. So, when the Save A mode is selected, a special set of circuits in U2030 compares all A and B values that have the same X value, and stores the larger in Table A. The B value is read and

stored in the display shift register. Then, as the A value is read, it is compared with the B value and the larger of the two is loaded into the display shift register. Finally, the number in the shift register is written into memory. This operation is performed once each time that the Save A mode is selected.

Vertical control IC U2030 contains a 3-bit synchronous counter that identifies the specific bit of an 8-bit vertical value that is to be read from memory or written into memory. This is the only memory addressing that is performed by U2030. All other addressing is performed by the horizontal control IC (on the Horizontal Digital Storage board).

Digitizing Circuits. The input vertical signal, VID FLTR OUT, coupled through edge connector pin 60 is applied through buffer U3040 to sample and hold switch U2040C. U2040C is controlled by flip-flop U1010B. U1010B generates the sample pulse, and is enabled during the clock cycle after the last approximation, as indicated by the least significant bit from the successive approximation register in U2030. The switched sample is then applied through buffer U1045 to a summing junction. At this point the output current from digital-to-analog converter U3025, that is supplied from the successive approximation register in U2030, is subtracted from the sample current. The difference current is then applied through comparator U2035B and synchronizing flip-flop, U2027A, to pin 18 of U2030 as the UP/DOWN signal. The binary equivalent of the input sample is effectively produced by the combination of the successive approximation register, the digital-to-analog converter, and the sample and hold circuit.

Address Decoding. The address decode logic accepts inputs from the address bus and from the address control logic on the Horizontal Digital Storage board, producing the control signals for read and write operations:

CONT W (control write)

DATA W (data write)

DATA R (data read)

The control write signal gates the control word from the data bus into control register U2028 to generate mode control signals. This control word consists of one bit, Q4, that represents the front-panel MAX HOLD function. If output Q5 is low, a peak operation is forced; if output Q5 is high and Q6 is low, an average operation is forced. The data read and data write signals are applied to the interface logic to control memory read and write operations.

Interface Logic. The interface logic, in general, performs control and interface functions between the active data circuits in the vertical and horizontal sections and the rest of the instrument. It allows the microcomputer to control the storage system functions and to access the digital storage memory. It also contains the circuitry for serial-to-parallel and parallel-to-serial conversion. (The microcomputer uses parallel transfer; the digital storage memory uses serial transfer.) Shift register U4020 reads data from memory to the data bus. Register U2025 stores information from the data bus for transfer to memory. Multiplexer U4015 does the parallel-to-serial conversion and applies the data output to gate U3024B, which acts as a buffer to supply either the multiplexer output or the MEM OUT (memory output) signal from U2030 to the memory as the DSDI (digital storage data input) data train.

The interface circuit group on the Vertical Digital Storage board is the handshake logic that works with the horizontal control circuits to access the memory and to determine when to increment the memory address counter. In either a data read or data write operation (when the corresponding signal goes high), flip-flop U3020B is triggered. This releases the BUS REQ (bus request) line to allow that signal to go high and signals the horizontal control circuit that memory access is required. When the horizontal circuits recognize the request, those circuits pull the BUS REQ line low at the same time that SYNC is low. The interface logic detects the BUS REQ and SYNC low condition through U2015A, U2015B, U3010A, and U3015A, and produces the low BUS GRANT signal to indicate memory access. The BUS GRANT signal then enables shift register U4020 to shift data from memory or enable register U1021. BUS GRANT also enables multiplexer U4015 to shift data to memory as indicated by the DATA R and DATA W lines. At the end of a data read cycle, gates U2010B and U4030C produce the INCR ADRS (increment address) signal to increment the address register in the horizontal circuits.

Maximum Hold. As described previously, when the Max Hold mode is selected, the signal from Q4 of control register U2028 causes the circuits in U1023 to compare the binary equivalent of the input signal for a given X value with the information in memory for that same X value. This causes the larger value of the two to be stored in memory. The signal from Q4, in combination with the VALID signal from the horizontal circuits, produces the MAX HOLD command to U2030 through inverter U4030E and gate U4040A.

Constant Circuit. As described previously, in the B minus A operation, a constant is used. This constant is selected internally with switch S1015. This switch, in

combination with multiplexer U2020, supplies the CONSTANT data to U2030. Multiplexer U2020 is, in turn, controlled by address bits 0, 1, and 2 to provide the proper constant data bit to U2030.

Output Circuits. From the U2030 vertical display register, the parallel data output is applied to 8-bit digital-to-analog converter U1035. The converter output is then applied to the output storage/cursor switch, U2040B, through a vector generator that consists of an integrator (U1040 and C1035) with an associated feedback loop sample-and-hold circuit. Integrator U1040 has a time constant that provides a ramp to last between the existing sample and the new sample (that is, between sync pulses). Circuits U2040A and U2045 and capacitor C2045 make up a sample-and-hold circuit with U2045 acting as an output buffer. From U2045, the output current through resistor R1036 subtracts from the digital-to-analog converter output current to modify the slope of the output ramp. The output of the vector generator is then applied to switch U2040B. U2040B, controlled by the MKR (marker) signal from the horizontal section, selects between the recreated video signal from U1040 and a dc (Peak/Average) level from buffer U3045, to be sent out as the vertical signal. The dc level is displayed only during retrace as the PEAK/AVERAGE cursor.

Peak/Average Level Circuits. The buffered PEAK/AVG LEVEL signal, from U3045, is compared with the sampled Video Filter Out signal, from U1045, by comparator U2035A. The output of U2035A is a high (1) if the Video Filter Out signal is greater than the PEAK/AVG LEVEL, or low if it is less. This output commands U2030, via U4040C and U4040D, to send peak or average data to the output. U4040B, C, and D are used if the instrument is under GPIB control to select one of three possible modes; Peak, Average, or front panel control knob.

Horizontal Section (Diagram 26)

Figure 7-16 is a block diagram for the Horizontal Control IC U5020. The horizontal analog voltage is converted to a current table value through a 10-bit tracking analog-to-digital converter (adc), which consists of up/down interlock and 10-bit up/down counter in U5020, and external 10-bit digital-to-analog converter (dac) U4040. As the sweep moves right, the counter increments; as the sweep retraces, the counter decrements. Each time the counter increments, it generates a new X coordinate value (the dac input) and a ST DIV (start divide) signal to start the storage cycle. The increment clock is the SYNC signal, and the decrement clock is the basic digital storage clock divided by two. When the Save A mode is selected, the counter skips every other binary number, so only B coordinates appear as addresses.

A state machine provides the horizontal system intelligence. This circuit determines which trace to write on the screen, determines when to switch from read to write, generates the B–A coordination signals for vertical control IC (on the Vertical Digital Storage board), controls the 9-bit display counter incrementing, and processes requests for the memory bus.

When an external device elects to read from or write to memory, it allows the BUS REQ (bus request) signal to go high to request permission from the state machine. When the time becomes available, the state machine pulls the BUS REQ line low, which signals the start of a request cycle. For the next eight clock cycles, the internal multiplexer output lines are in the high-impedance (open) tri-state mode.

The combination of the up/down interlock, 10-bit up/down register, 9-bit display counter, and horizontal display multiplexer constitute the primary circuits that either write to or read from memory. To generate X values to be written into memory, the circuits convert the sweep voltage to binary form. These circuits also count the sync cycles to cause the external logic to read stored data from memory and produce a vertical signal (Y value) for each corresponding X value.

During acquisition cycles, the 10-bit up/down counter, controlled by the up/down interlock, operates in a loop with the external 10-bit digital-to-analog converter. This allows the counter to acquire the equivalent (X value) of a sample section of the sweep voltage. From the counter, the 10-bit output is applied to the 10-bit up/down register. During display cycles, the 9-bit display counter counts sync pulses to acquire the X value. Either the 10-bit up/down register output or the display register output is applied to the horizontal multiplexer under control of the SELECT signal from the State Machine. From the multiplexer, the output is applied to the memories as an address.

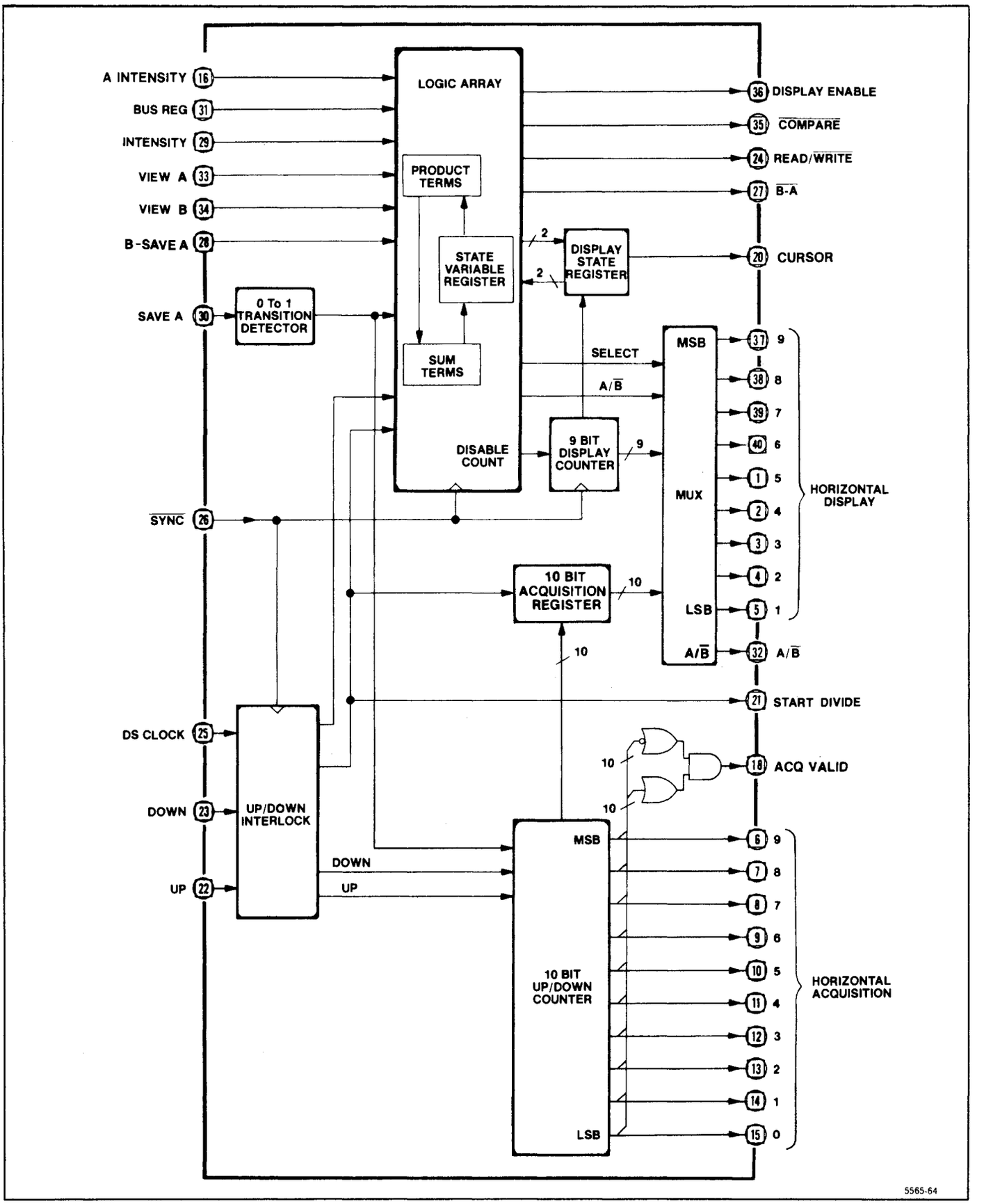


Figure 7-16. Horizontal control IC block diagram.

Marker IC. Marker IC U3020 performs several functions on the Horizontal Digital Storage board:

In conjunction with Horizontal Digital Storage IC U5020, it creates the two waveform markers and the update marker.

Controls the processor addresses assigned to digital storage — 7A, 7B, FA, and FB.

Creates the fast-retrace blanking pulse DSBLANK.

Takes control of the address lines to the display RAM when the microprocessor accesses the digital storage data.

To create the waveform marker, it monitors the horizontal display bits, HD0-9, and the CURS and B−A signals. When these lines indicate the display has reached a point that matches on of two points previously stored in the IC by the microprocessor, the IC sets A INTENSITY high, causing U5020 to repeatedly display the same point until A INTENSITY goes low again (which it does after a number of DS ENBL cycles previously stored in the IC by the microprocessor).

The update marker is initiated by a comparator detecting that the analog sweep and the display sweep have crossed as explained elsewhere. U3020 detects this event on the CSLFS line. If the VALID line is high when this occurs, U3020 sets INTENSITY high, causing U5020 to repeatedly display the same point until 15 DS ENBL cycles have passed. Then INTENSITY goes low again.

U3020 monitors HD9 to generate the DS BLANK pulse. When HD9 goes from high to low and the CURSOR line is low, U3020 sets DS BLANK high for one DS ENABLE cycle.

When the microprocessor wants to read values from or write data to the waveform memory, it first sends a starting address to U3020. Circuitry on the Vertical Digital Storage board (A61A1) controls the BUS GRANT line which indicates when U3020 can actually access the digital storage RAM without disturbing the display. When BUS GRANT goes low, U3020 (instead of U5020) drives HD0-9.

The Vertical Digital Storage board also generates an INCR ADRS (Increment Address) pulse for each BUS GRANT cycle. U3020 increments the address that it will assert on HD0-9 by one for each INCR ADRS pulse. The microprocessor loads an initial address and the address register outputs are applied to tri-state buffers. Then, the 10 bits of address from the counters are buffered. Those signals are multiplexed onto the HD (horizontal display) lines and R/W (read/write) line to the memories. These buffers are enabled only during the bus grant portion of the cycle for display of memory data.

At all other times, horizontal control circuit U5020 outputs control the HD lines to determine the memory address for update of memory data.

U3020 controls and subdivides the addresses assigned to digital storage. The Vertical Digital Storage board responds to addresses 7A, 7B, and FA. The Horizontal Digital Storage board responds to addresses 7A, 7B, FA, and FB. The DV (Data Valid) line (which clocks data to or from the microprocessor from the instrument data bus) goes to U3020, which sends a controlled version of this line, VDV, to the Vertical Digital Storage board. When the addresses on the Vertical Digital Storage board are to be addressed, this line is active and none of the addresses on the Horizontal Digital Storage board are affected. When the addresses on the Horizontal board are to be accessed, VDV is held low by U3020 regardless of DV.

Address 7A on the Horizontal board is further subdivided into 7A.0 through 7A.7 by three bits of 7B on the Horizontal Digital Storage board. Access to these addresses is passed between the two boards by U3020. Reading from address FB will give access to the Horizontal board regardless of which previously had access. Sending the bits to 7B on the Horizontal board to access 7A.6 (DB6−4= 110) will pass access to the Vertical board. Sending DB6,5=11 to 7A.5 of the Horizontal board will also pass access to the Vertical board. Sending DB6,5=10 to 7A.5 of the Horizontal board will pass access to the Vertical board, but only for one DV cycle.

Tracking Digital-to-Analog Converter. The 10-bit digital-to-analog converter operates as part of the loop that acquires a binary equivalent of the SWP (sweep) input signal from the Sweep board. Converter U4040 accepts the output from the 10-bit up/down counter of U5020 and converts that output to an analog current. The analog current is then subtracted from the SWP signal (which is applied at edge connector pin 60 through buffer U6060B). The result of this subtraction is supplied to up and down comparators in U3050. This creates the UP or DOWN signal, as appropriate, to control the count direction of the 10-bit up/down counter in U5020. The counter then counts in the appropriate direction, which changes the digital-to-analog converter output to reflect the proper value.

Update Marker Circuits. These circuits create a cursor to show the present update location while a digital storage display refreshes. The cursor is made by stopping the sweep for a short period, allowing the crt phosphors to brighten at that spot. This occurs at each of

the 500 digital storage sweep positions. The resulting display appears as a bright dot sweeping across the crt, rising and falling with the signal.

The basic circuits consist of a set of latches, a digital-to-analog converter, a comparator, a pulse generator, and control circuitry. The Horizontal Display (HD) data represents the digital equivalent of the present update position. The latches capture the data, and the digital-to-analog converter (dac) converts it, creating the analog horizontal deflection signal. When the sweep voltage reaches the dac level, the sweep stops for a longer period of time, and therefore the crt is brighter, than at other sweep positions. On the next sweep, the HD data increments to the next position, moving the cursor along the sweep.

The DSPL EN (Display Enable) signal clocks the HD (Horizontal Data) signals into latches U1020 and U2030. The latch outputs drive U2020, a 10-bit digital-to-analog converter. The converter's output current drives operational amplifier U6060A, producing a voltage called HORIZ SIG. When a digital storage signal is displayed, HORIZ SIG drives the horizontal Deflection Amplifier.

Also, U4060 compares HORIZ SIG to the sweep voltage from U6060B. The comparator output drives the "Update Intensity" input on the Marker IC, U3020. The Marker IC generates a 16-unit pulse, clocked by DSPL EN. The rising edge of U3020's output pulse produces the INTENSITY signal that temporarily prevents counting by the 9-bit display counter in U5020. This effectively stops the beam for a short time and causes a bright spot (cursor) on the trace to indicate the horizontal point being updated.

Fast Retrace Blanking. Between the display of the B memory contents and display of the A memory contents, a fast retrace occurs. This retrace, unlike the one that follows the A memory display (cursor), is not required to be seen and is blanked. This is accomplished by blanking control flip-flop U1014B, which is controlled by the most significant bit of the memory address and the DSPL EN signal during a marker cycle.

Memories. Integrated circuits U1026 and U2026 provide 8k bits of random access memory for storage of the 1000 data points used in the digital storage system. Addressing during bus transfer of memory data is controlled by address tri-state buffers U1023 and U1016 and by horizontal control IC U2035 during memory update.

DEFLECTION AMPLIFIERS (Diagram 27)

Refer to the block diagram adjacent to Diagram 27 as well as the schematic diagram. The Deflection Amplifier receives vertical signal information from the vertical section of Digital Storage or the Video Processor, and horizontal or sweep voltage from the horizontal section of Digital Storage or the Sweep board. Readout data for the display comes from the Crt Readout circuits. The output of the Deflection Amplifier drives the crt deflection plates. The amplifiers contain the switching circuits necessary to perform the selection functions and they also contain the amplifier stages needed to produce the deflection plate drive signals.

Horizontal Section

Signal lines HORIZONTAL SIGNAL (from the digital storage circuits through edge connector pin 49) and SWEEP (from the Sweep circuit through edge connector pin 51) are applied to switch IC U7055A. U7055, under control of the STORAGE OFF signal (from the digital storage circuits through edge connector pin 7), selects either the HORIZONTAL SIGNAL or SWEEP input. The SWEEP signal is selected when the STORAGE OFF line is floating or pulled high. The HORIZONTAL SIGNAL is selected when the line is pulled low. Resistive divider R7051 and R7081 reduces the selected signal from 1 V/div to 0.5 V/div. U7073 buffers the selected signal. It goes out to the HORIZ OUT rear-panel connector via edge connector pin 48. U7073 applies the signal to switch U7055B. The HORIZ R/O signal, from the Crt Readout circuits, is also applied to U7055B. The R/O OFF signal, from the Crt Readout circuits selects between these two signals. When R/O OFF is floating or pulled high, the switch transmits the signal from buffer U7073 to the shaper. When the line is pulled low, it selects the HORIZONTAL R/O signal.

U7055B applies the signal to a shaper network to compensate for non-linearity in the crt deflection characteristics. This network consists of resistors R5059, R5058, R5057, R5062, R4061, and R4059, plus diodes CR4052, CR4051, CR4058, and CR4056. The HORIZONTAL POSITION voltage, from the front panel via edge connector pin 47, through resistor R6032, is applied to the shaper circuit so the shape correction factor relates to the crt deflection.

The shaped signal is then applied through preamplifier U2060 to the deflection amplifier circuits. Horiz Gain adjustment R1055, calibrates the amount of gain compensation required for proper deflection sensitivity.

The horizontal deflection amplifier consists of two circuits similar to each other, one for each horizontal deflection plate. One circuit is an inverting amplifier, the other operates in-phase. Inputs to Q4038A of the invert-

ing side are through the parallel combination of resistors R4049 and R4048 and capacitor C4057. The series connection of resistor R4048 and variable capacitor C4057 provides high-frequency response compensation. Capacitor C2047 controls high-frequency feedback.

Input to the non-inverting side is through resistor R5029 to the base of Q4025A. R4019 and R5035 set the dc level for the feedback loop to the base of Q4025B. Variable capacitor C5021 provides adjustment to set transient gain. High-frequency feedback is controlled by capacitor C3021.

Gain of each amplifier section is approximately 20. (Horizontal deflection sensitivity of the crt is approximately 21.3 V/div per side.) Each section is single-ended and incorporates a gain- degenerated dual PNP transistor at the input side (for temperature compensation) connected as a differential amplifier. For example, Q4038B of the right deflection amplifier drives emitter follower Q4047.

Signals with a low rate of change drive the output transistor through R5037 and P3033. As the rate of rise increases, the drop across R5037 increases and when it reaches 0.6 V, either Q4035 or Q4042 are biased on. These transistors provide the high current drive for the output transistors. When the signal rate of change is low, Q1043 drives the crt deflection plate and Q1049 provides bias current for the amplifier. As the rate of rise increases, C3039 couples the signal to the base of Q1049. Q1049 provides the positive drive to the deflection plate, and Q1043 provides the negative drive. Each output transistor can provide a 200 V excursion in approximately 1 μs.

The horizontal amplifiers operate with approximately 1 mA of bias current in the output stage, as set by the current through resistor R3031, R1052, and R1049 at the base and emitter of Q1049. Current through resistor R3031 also provides the current for the input stage, Q4038A/Q4038B. Emitter follower Q4047, operates at approximately 2.5 mA. Resistors R1045 and R1034, in the emitter circuit of Q1049 and Q1043, degenerate the output stage for fast steps. Current from the −15 V source through resistor R4033, sets the output operating level. Feedback resistor R3045 sets this output level at approximately 142 V.

Operation of the right-hand (inverting) section is basically the same as the left-hand (non-inverting) section.

Vertical Section

VIDEO FILTER OUT, from the Video Processor, and VERTICAL SIGNAL, from the Digital Storage, are routed through switch IC U6055A, under control of the STORAGE OFF signal from the Digital Storage board. Note that the VIDEO FILTER OUT signal is buffered by IC U7065 to prevent a change in load transients from affecting the signal level. A high on the STORAGE OFF line selects the buffered VIDEO FILTER OUT signal, and a low selects the VERTICAL SIGNAL. U6065 inverts the selected signal and clamps it to ground. Both the VIDEO FILTER OUT and the VERTICAL SIGNAL are specified at 0.5 V/div with 0 V for the baseline and positive voltages above the baseline.

The signal is re-inverted and offset by buffer U6073 so center screen represents 0 V. Buffer U6073 supplies a sample of this centered signal to the rear-panel VERT OUT connector via edge connector pin 46. The output of U6073 is also applied through switch U6055B, when the R/O OFF line is high, to the vertical shaper circuit. When R/O OFF line is low, the VERTICAL R/O signal is applied to the shaper.

The vertical section shaper (R4062, R4065, R4067, R4069, R4064, and CR4063, CR4064, plus the preamplifier U2062) operates the same as the horizontal section. Q4078 limits positive excursions to approximately one division above the top of the screen to protect the output stages from being overdriven.

The vertical output stages are similar to the horizontal stages, with the exception of higher bias current. Current flow of approximately 1 mA, through resistors R3089 and R3098, produces approximately 5 mA in the output stages. To correct for the increased current in the dual input stage transistors, Q4083 and Q4101, resistors R5081 and R5099 are lower value than their counterparts R5041 and R5027 in the horizontal amplifier.

U6024 compares the signal level from the baseline clamp, U6065, with a reference level set by divider R7032/R7034. This produces the CLIP signal for the Z-Axis interface circuits. When the VIDEO FILTER OUT signal is more negative than the reference level (approximately 1 division above baseline), it pulls the CLIP line low. R7021 pulls the CLIP line high if the signal is more positive than the reference level.

Z-AXIS AND RF INTERFACE (DIAGRAM 28)

The Z-Axis and RF Interface board contains the RF interface circuits, crt Z-axis drive circuits, power monitor circuits, and a timer that measures operational hours. This board provides beam intensity (nominally from the front panel), baseline clipping, and unblanking logic for the signals or readout data. Unblanking logic comes from the Sweep board, the Crt Readout, the Deflection Amplifiers, and the Digital Storage. The RF Interface circuits receive data from the microcomputer that controls the RF Attenuation, and IF selection. A power fail circuit on the board detects any change in

input power frequency or power supply voltage and notifies the microcomputer. An elapsed time meter is also located on the board to give a indication of total instrument operating time.

RF Interface Circuits

The RF interface includes the digital control circuits that receive the address and instruction data from the microcomputer and decode it to control the RF Attenuator, and IF selection. The power supplies that are required to drive the attenuator and switches are also included.

Digital Control. Address decoder U2045 latches the data at the input of U3046 whenever the microcomputer selects address 4F. Table 7-7 lists the purpose of each data line from the buffer.

Table 7-7
RF INTERFACE LINES

Line	Purpose
Q1	Enables 10 dB attenuator
Q2	No connection
Q3	Enables 30 dB attenuator
Q4	Enables current drivers Q2025 and Q3028
Q5	Enables transfer switch driver
Q6	Selects 829 MHz IF (high state) or 2072 MHz IF (low state)
Q7	Enables 20 dB attenuator
Q8	Enables baseline clipping

When Q4 of U3046 goes low, Q2025 and Q3028 conduct. This raises the Vcc of attenuator drivers U3034, U3029, and U3038 to +16 V for approximately 100 ms to energize the attenuator solenoids. A diode protects each attenuator driver output line from the inductive voltage surge that occurs when the solenoids change state.

Transfer Switch. In Option 07 instruments, operation of the Transfer Switch is dependent on the output of Q3025/Q3024. The Q5 output of U3046 is applied to the input of operational amplifier U4023, which drives differential amplifier Q2025/Q3024. When Q5 goes high, Q3025 is biased on and the Transfer Switch selects the 75 Ω input. When Q5 goes low, Q3024 is biased on, and the internal mixer is selected. Diodes CR3018 and CR3017 protect the transistors from voltage spikes induced when the Transfer Switch changes state.

Z-Axis Circuits

The Z-Axis circuits provide the drive currents and bias voltage to operate the crt. They consist of the intensity control logic circuits, which control the crt beam current for normal signal display operations, and the unblanking gates, which furnish current to the Z-Axis drive amplifier to drive the crt control grid.

Z-Axis Drive Amplifier. The Z-Axis Drive Amplifier is an operational amplifier that consists of transistors Q3047, Q4058, and Q4059, and related components. R1050 is the input resistance for the amplifier, and R2066 is the feedback resistor. The output is clamped by diodes CR3059 and CR3066 to protect the amplifier from transient surges in case of crt arcing. The amplifier is driven by two sources, exclusive of each other; U2038B/Q2042 drives the amplifier during readout display periods, and U2038A/Q2044 drives the amplifier during sweep display periods. U2039 is an AND-NOR gate that provides the logic to one input of NAND gate U2038A to turn Q2044 on or off. The R/O OFF line and the output of U2039 must both be high for U2038A to furnish current to Q2044. Table 7-8 lists the conditions under which U2039 will output a high to U2038A.

Table 7-8
U2039 TRUTH TABLE

Signal	Condition
U3046 output (line Q8)	0 0 0 1 1 1 0 0 0
CLIP	0 0 0 0 0 0 1 1 1
Z-Axis Blank	1 1 1 1 1 1 1 1 1
Storage Off	0 0 1 0 0 1 0 0 1
SWP GATE	1 0 1 1 0 1 1 0 1
U2034, pin 10	0 0 0 0 0 0 0 0 0

Only the combinations shown in Table 7-8 plus a high on the R/O OFF line will gate a low out of U2038A. When the U2038A output is low, emitter current is furnished to Q2044, which in turn furnishes current through R2051 (the input resistance of the Z-Axis drive amplifier) to Q3047. U2034B is a single-shot multivibrator that produces a 3 micros pulse to blank the crt beam during trace return, between readout and signal display.

The other source of input current to the Z-Axis drive amplifier is Q2042. This transistor is turned on by U2038B when R/O UNBLANK is high and R/O OFF is low.

Q1028 is the current source for divider R1030/R1025 that establishes the operating point for Q2042 and Q2044, which sets the intensity level. Diodes CR1045 and CR1043, connected from the base of Q2042 and Q2044 to the emitter of Q2022, limit the display intensity. These diodes prevent the bases from going more positive than approximately 0.6 V above the emitter voltage of Q2022. This circuit, which includes Int Limit adjustment R1027, sets the maximum current

for both Q2042 and Q2055.

Transistors Q1017 and Q1015 provide current for the trace rotation coil. Trace Rotation adjustment R1021 sets the current so the displayed trace is aligned with the graticule.

Power-Fail Detector

This circuit detects an instrument power failure and transmits the information to the Processor and Memory boards. The LINE TRIGGER signal from the Power Supply board through edge connector pin 60 is supplied to Q2011. Q2011 buffers the signal and applies it to the input of retriggerable one-shot U2034A. U2034A performs as a missing- pulse detector to generate a power-fail signal through Q3011 to notify the Processor and Memory boards if more than two 60 Hz cycles are dropped. To avoid an undefined state, the output from U2034A is latched low by U2051. Under normal operating conditions, the POWER-FAIL signal from Q3011 is high.

Power-Supply Monitor

This circuit detects if one or more of the instrument power supplies have failed. Each voltage supply in the instrument is fed into thick film resistor network R3051, which balances the currents to provide a null output (approximately 1 Vdc). Any line change of more than ±25% drives the input to window comparator U3051 beyond its ±200 mV threshold and generates a low output. Q2059 and Q2067 drive the dual light emitting diode DS1062 to provide visual indication of power-supply status (green indicates normal operation and red indicates a fault condition). The output of U3051 is also fed to tri-state buffer U3052. After instrument power up or if a failure is detected, the microprocessor will poll address CF to determine power- supply status over the data bus.

Timer

An electromechanical timer, M1019, is calibrated for a duration of 5000 operating hours. The current through R1015 and the timer causes the copper band to progress along the scale.

HIGH-VOLTAGE SUPPLY (DIAGRAM 29)

The High-Voltage Supply furnishes the -3860 V crt bias and 6.3Vac filament voltage to the crt cathode, and provides dc restoration for the Z-AXIS DRIVE signal. The supply consists of the following four main circuits:

1. The high-voltage oscillator circuit produces the crt filament voltage and the 200 Vac that is stepped up and applied to the voltage doubler circuit.

2. The voltage doubler circuit rectifies and filters the high voltage for application to the crt cathode.

3. The high-voltage regulator circuit samples the high voltage and regulates the operation of the high-voltage oscillator.

4. The Z-Axis clipper and rectifier circuits couple the Z-AXIS DRIVE signal to the crt control grid.

High-Voltage Oscillator

This circuit consists of transistor Q1073, transformer T2065, and associated components. The approximately 200 Vac, oscillator output is coupled across T2065, where it is stepped up for application to the voltage doubler, and stepped down for application to the crt filament.

Voltage Doubler

The voltage doubler consists of CR4041, CR4035, C4027, C5021, C4024, R3038, and R1039. The output of the doubler is taken off the anode of CR4035 and applied to the crt cathode through the filter consisting of R3038, R1039, and C4024. Reference voltage for the regulator is also taken off the end of R1039. R1039 keeps the filament at the same potential as the cathode.

High-Voltage Regulator

This circuit consists of amplifier U4083 and surrounding components. The high voltage is applied through a voltage divider that consists of R1017B and R1017C. This voltage divider is connected through R1042 to +15 V. The sample of the high voltage at pin U is applied through R4075 to the input of comparator U4083. The correction signal, in the form of dc drive, is applied as bias to Q1073 to set the oscillator current.

CR4078 and CR4077 at the input to U4083, protect the input against excessive voltage excursions. The high-voltage oscillator is protected by CR4071, R3079, and R4074 in case the +100 V supply should fail. Normally, CR4071 is back biased. If the +100 V is not present, CR4071 conducts and clamps the input negative; the output of U4083 swings negative and Q1073 remains cut off. This circuit ensures that Q1073 will begin to oscillate only after the 100 V supply reaches a voltage sufficient to sustain oscillation. CR3077 (in the regulator output circuit) protects the base of Q1073 from excessive negative voltage.

Z-Axis Clipper

This circuit consists of diodes CR1056 and CR1046, plus associated components. The 225 Vac from pin 8 of T2065 is coupled through C1058 and R1048 to the junction of CR1046 and CR1056. The regulator circuit, that consists of VR1041, R2050, R2040, and Q2048 holds holds the cathode of CR1046 at approximately +100 V to 143 V, depending on the setting of R2040. CR1046 and CR1056 clip the incoming 225 Vac to a total excursion of [$V_{CR1046\ cathode}$ $-V_{Z\ AXIS\ DRIVE}$ +1.2V). R2040 is adjusted to completely cut-off the crt with Z-Axis DRIVE at minimum. The voltage that passes the clipper circuit is coupled through C1031 to the Z-Axis rectifier.

The clipped Z-AXIS DRIVE signal is rectified by CR2044 and CR2046, which are the principle components of the second section of the Z-Axis circuit. The rectified voltage is then fed to the grid of the crt. C1041 couples the fast changes of drive voltage to the crt grid to speed up the response of the grid circuit. The crt grid is protected from high-voltage arcs by neons DS2052, DS2054, and DS2057. R1043 protects CR2046 and CR2044, respectively, from high-voltage surges if the crt should arc.

CRT READOUT (DIAGRAM 30)

The Crt Readout assembly stores readout characters and generates deflection and Z-Axis signals to display those characters. It also handles the frequency dot marker display. Both characters and frequency dot displays are time-shared with the spectrum trace.

Generating Readout

Crt readout is handled by sequential logic, clocked at 3.41MHz, supplied by the Processor board. The readout circuitry (Figure 7-17) is composed of the following elements.

1. Readout On Timing — RAM for character storage.

2. Character Counter — to access the RAM and control the scan.

3. Character Generator — to unblank the crt beam.

4. D/A Converters — to deflect the crt beam.

5. Instrument Bus Interface — to store characters and control the display. A more detailed block drawing is provided adjacent to Diagram 30.

Forty characters can be displayed per line, with up to sixteen lines selected. Normally, up to three lines are displayed while simultaneously displaying the spectrum. When over three lines are to be displayed, the spectrum display is disabled to keep the readout refresh rate above 60 Hz.

Readout-On/Off Timing. Characters are written one at a time. This allows a portion of the spectrum to be drawn between each character. The character duty cycle is between 10% and 25% because it varies with the character drawn. The time sharing between character writing and spectrum display is pseudorandom to reduce the effect of gaps in the spectrum display by moving them on the trace.

The readout-off time is set to 140 μs by one-shot multivibrator U1055 (Figure 7-18). Flip-flop U1041B asserts GEN RUNNING after U1055 times out, allowing a character to be drawn. After a character is written, ROW 0 COL 0 resets the flip-flop, which clocks off time one-shot U1055. The ON control bit must have been asserted by the microcomputer to get readout (as described under Instrument Bus Interface later in this section).

If BLANK (MSB of the character data) is not set, the GEN RUNNING flip-flop unasserts R/O OFF through OR gate U2044B; this switches the readout deflection signals for the deflection amplifier inputs (Diagram 27). BLANK can be set by the microcomputer to load a space into the character RAM so the readout does not use time for the spectrum trace to scan a blank character.

Character Scan. Although the 8678 character generator IC, U2048, is often used in raster scans, in this application it is used to write complete characters, as shown in Figure 7-19. A character is drawn as a pattern of dots in an 8 x 8 matrix where the top row and first three columns are blank. These blank dots allow for beam retrace and spacing. The idle position between characters is indicated on the figure.

Character counters synchronize the horizontal and vertical scan with the Z-Axis signal from the character generator IC to draw the character. These counters, U2022, U2018, U2026, and U2014, divide by 8 for the columns within a character (columns A, B, C), divide by 8 for the rows within a character (rows A, B, C), divide by 40 for the characters within a line (characters A, B, C, D, E, F), and divide by 16 for the lines within a display. The counters are enabled only when the generator has control of the crt beam (GEN RUNNING line asserted) and INCR (increment) is high (when INCR is low, the crt beam is stopped to write a dot on the crt).

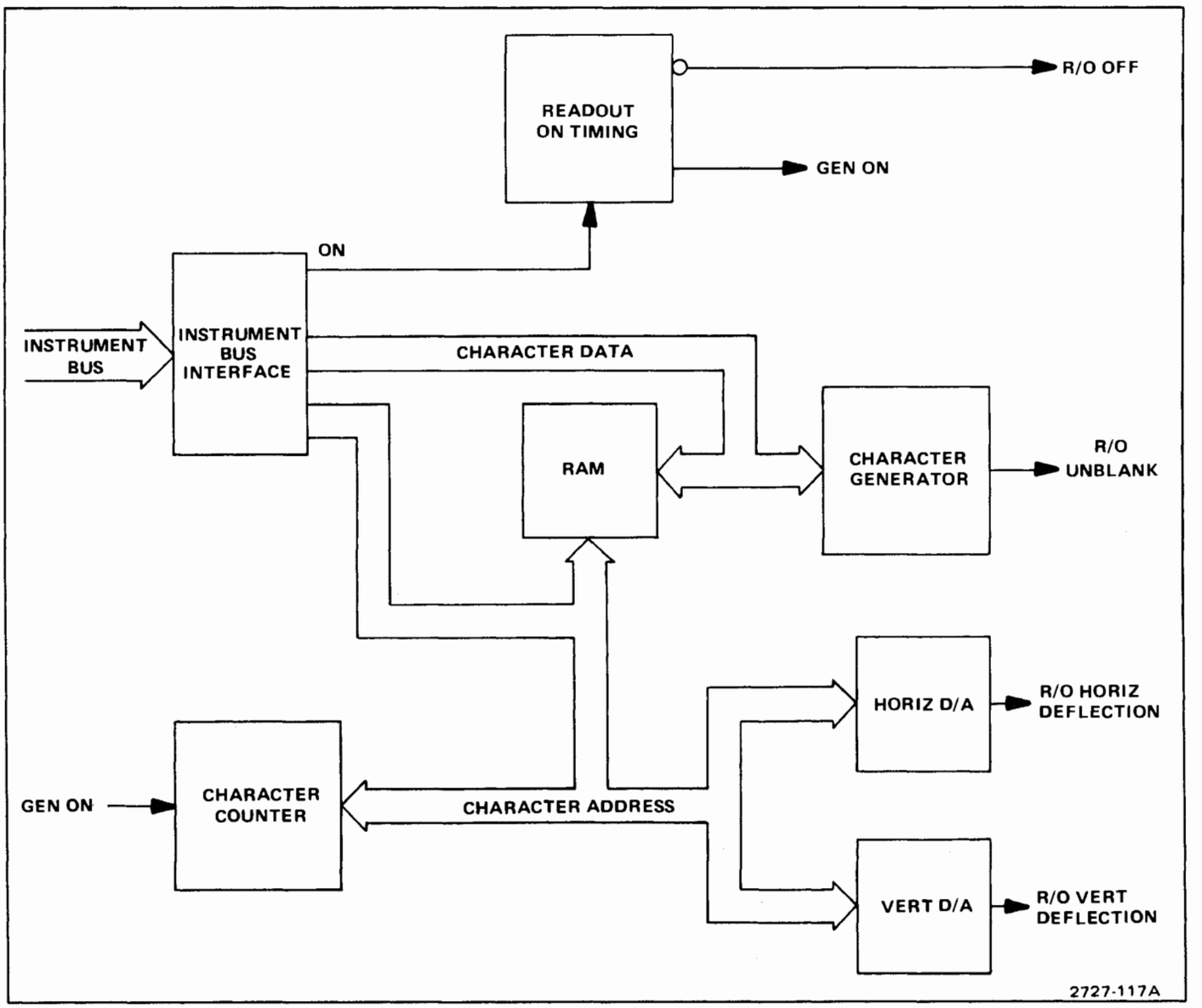


Figure 7-17. Block diagram of crt readout.

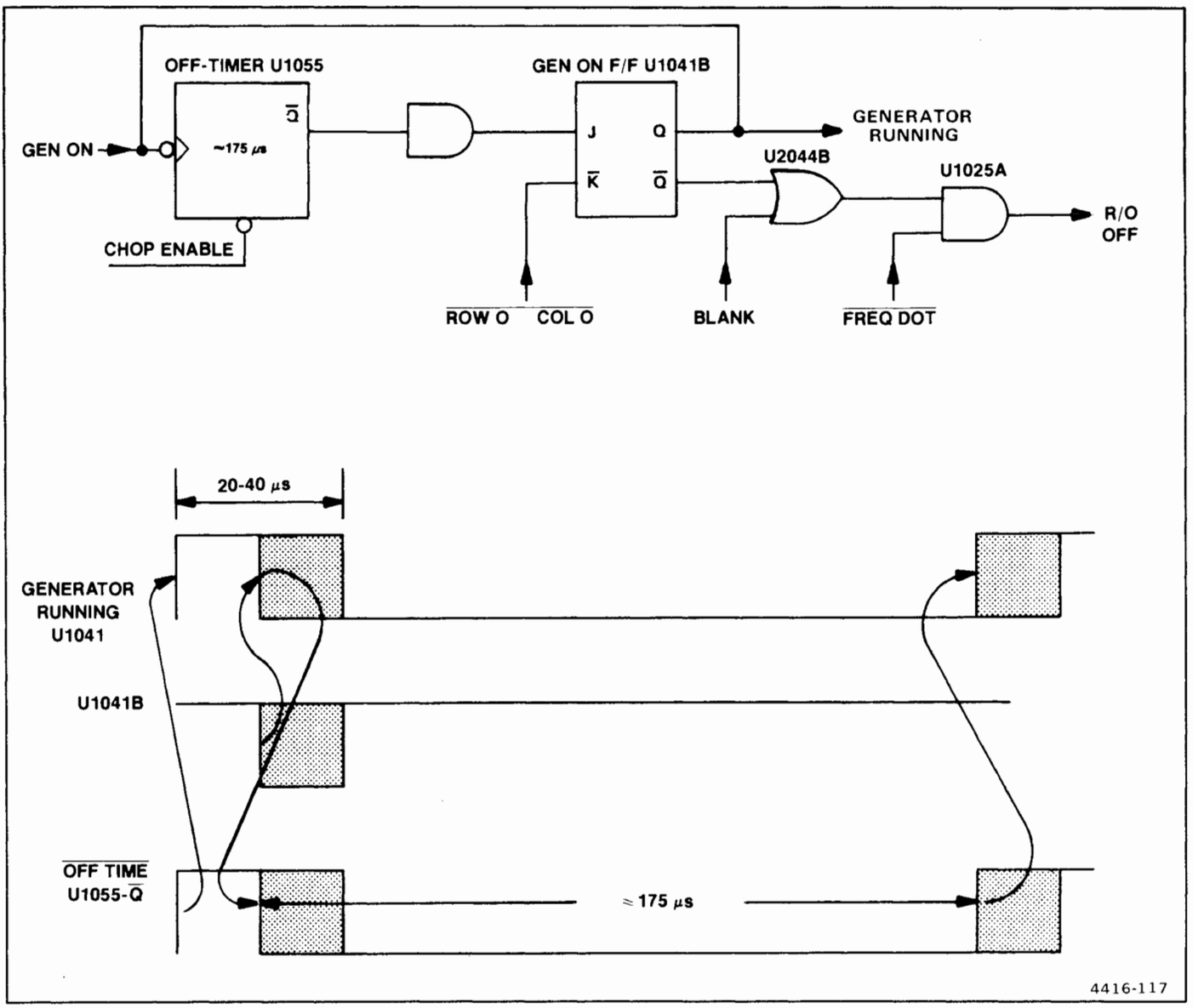


Figure 7-18. Character on/off timing.

The SKIP line from U2052 permits software control of the allowable states of line counter U2014. By placing a one in this bit of a character, the line counter is allowed to count up to the next state. This will continue until a character is encountered with the skip bit set to zero. This allows the addition of a third line to the normal two-line readout for status messages, by operating with the circuit normally in the 16-line mode (all but the bottom and top lines start with a readout character of 40 hex, which has the SKIP line set high). Thus, all but the bottom and top lines are skipped. When large messages are to be displayed, the SKIP line is set low for all characters and 16 lines are displayed.

The counters are wired to force the D/A converters to step through the character horizontally, a row at a time. At the same time, the pattern of dots is accessed under the control of the timing decoder logic, U2039B and U2031. The AND gate and decoder combine to control the character generator, U2048, which generates the correct pattern of blanking to draw the pattern of dots for the character. U2048, the 8678 character generator IC (Figure 7-20) contains a ROM with the correct pattern of 64 bits for each of the 64 characters in its repertoire. The bit patterns are accessed by a decoder that operates on the ASCII code on the character generator inputs. The pattern of bits is multiplexed, one 8-bit line at a time, into a shift register that is clocked out one bit at a time to control the crt Z-axis.

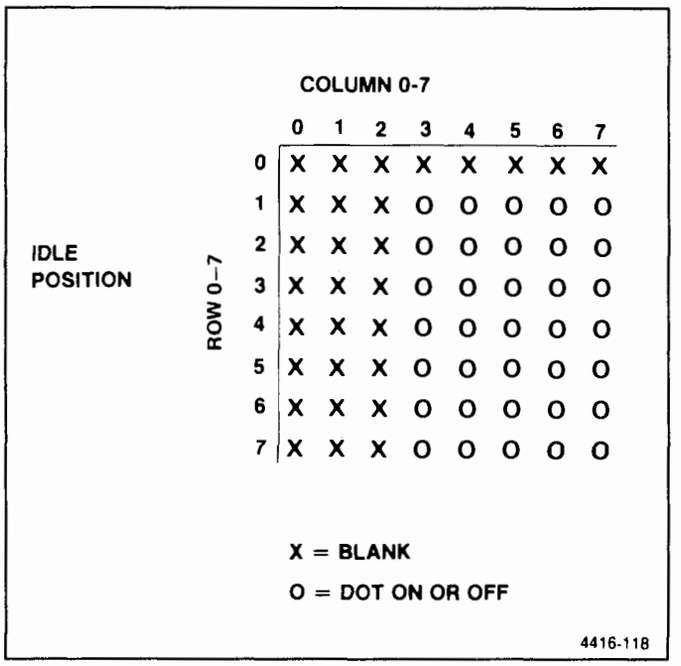


Figure 7-19. Character scan.

Character Generator Timing. The character generator timing lines are called DOT, LINE CLK, LE, and CLR. Each cycle of DOT clocks one dot (bit) out of the shift register. A positive transition on LINE CLK switches the next line (row) of dots onto the shift register inputs; the dots are latched by a negative transition on LE (load enable), setting up the shift register to display another row of dots. CLR resets the line counter to begin drawing another character.

GEN RUNNING, INCR, and CRT CLK are combined through AND gate U1037B to generate DOT to clock the character generator, U2048. Inversion by the gate restores the phase relationship of the DOT input and the inverted LINE CLK. LE is gated by U2039B when the character counter reaches column 2. This loads the shift register with the next row of dots, which is displayed starting at column 3. LINE CLK advances the line (row) counter after the scan of the current row begins to set up the next row of dots on the shift register inputs; this occurs at column count 4. Decoder U2031 outputs a ROW 1 COL 1 when the character counter reaches row 1, column 1 (the first non-blank row of dots scanned in each character). This is asserted once during the scan of each character.

The sequence of events to scan a character is illustrated in the character timing diagram (Figure 7-21). At 1, the character generator finishes a character. Then, when the counter advances, decoder U2031 asserts ROW 0 COL 0, resetting the GEN RUNNING flip-flop, U1041B, on the next clock. This stops the counter at row 0, column 1 (2 on the figure). When readout-off time one-shot U1055 completes the time-out period, it allows the GEN RUNNING flip-flop to be set. Just before the scan enters the actual character clock area (at 6), CLR resets the character generator line counter (at 5). LE (at 5a) loads one row of dots into the output shift register so that the first dot is output at 6. The break (7 on the figure) indicates that the scan continues. After the character is scanned, the scan returns to the idle state; 8 and 9 correspond to 1 and 2 on the timing figure.

Dot Delay. Each bit shifted out of the character generator is the value of a dot in the 5 x 7 character matrix; 0 for a blank and 1 for a dot that is to be written. As the scan progresses at 3.4133 MHz, a faint character display might be expected. To brighten the dots that are written, a shift register is used as a delay element so that dots are displayed and counters disabled for 3 clock cycles.

Assume that no dots have been displayed for several dot clock cycles, so the output of the character generator, pin 11 of U2048, is low. Thus, U1020B output is high, and the outputs of the delay shift register U1025C and U1020B are low. When a dot is displayed, the character generator output (pin 11 of U2048) goes high. This causes INCR to go low and disable the counters. It also causes the input to the delay shift register, pin 11 of U1020B, to go high. On the next clock pulse, U1020A output follows INCR and goes low. The shift register clocks the one in, and the unblank flip-flop, U1016B, goes high, turning the crt beam on. This is the only "1" it will clock in, because the output of U1020A is now low. The circuit is now in a lock-up state with the counters disabled. Two more clock cycles will go by until the "1" in the shift register is clocked out, allowing the output of U1033C to go high. A high on the output of U1033C starts the counters again and resets unblank flip-flop U1041A.

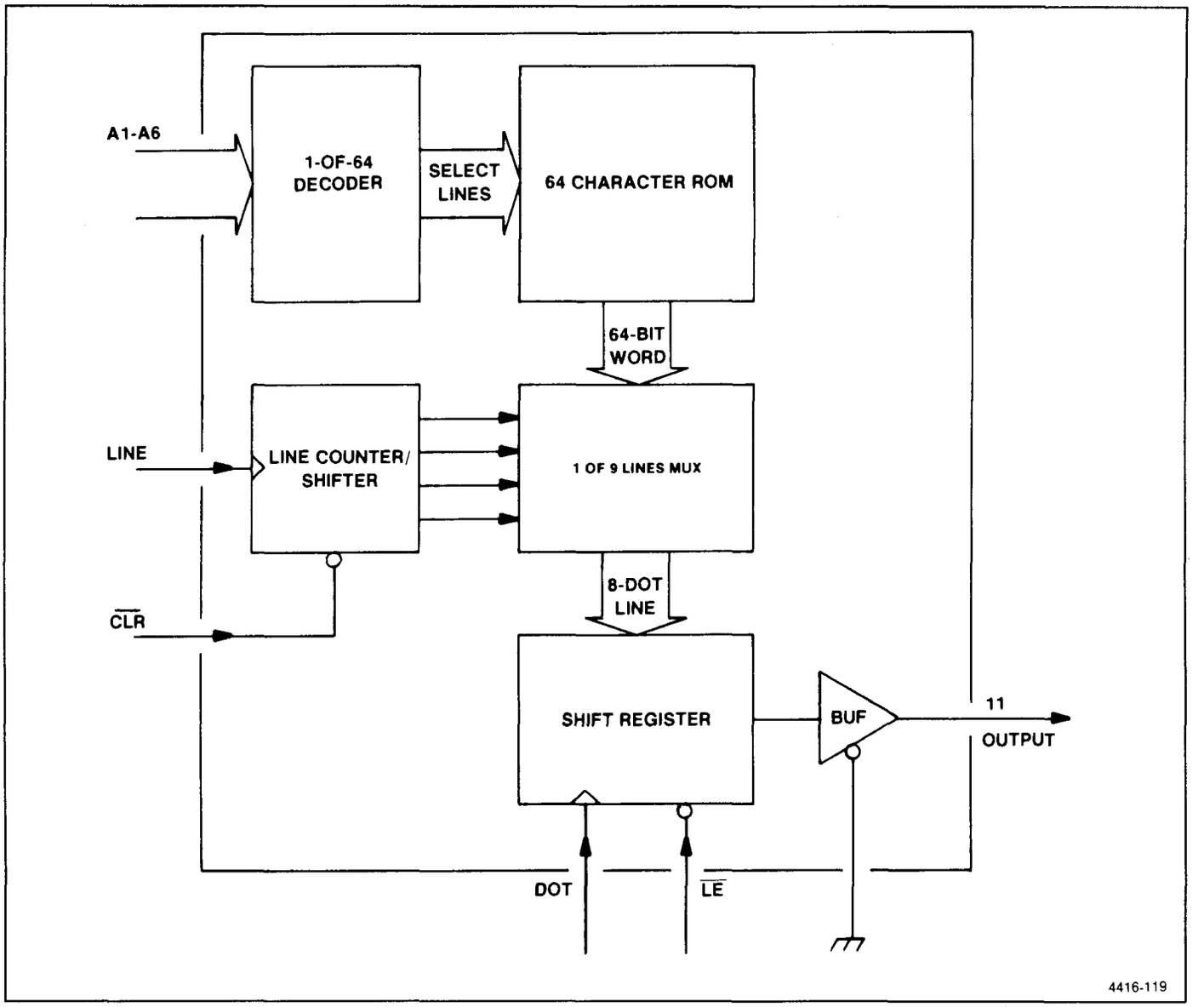


Figure 7-20. Character generator block diagram.

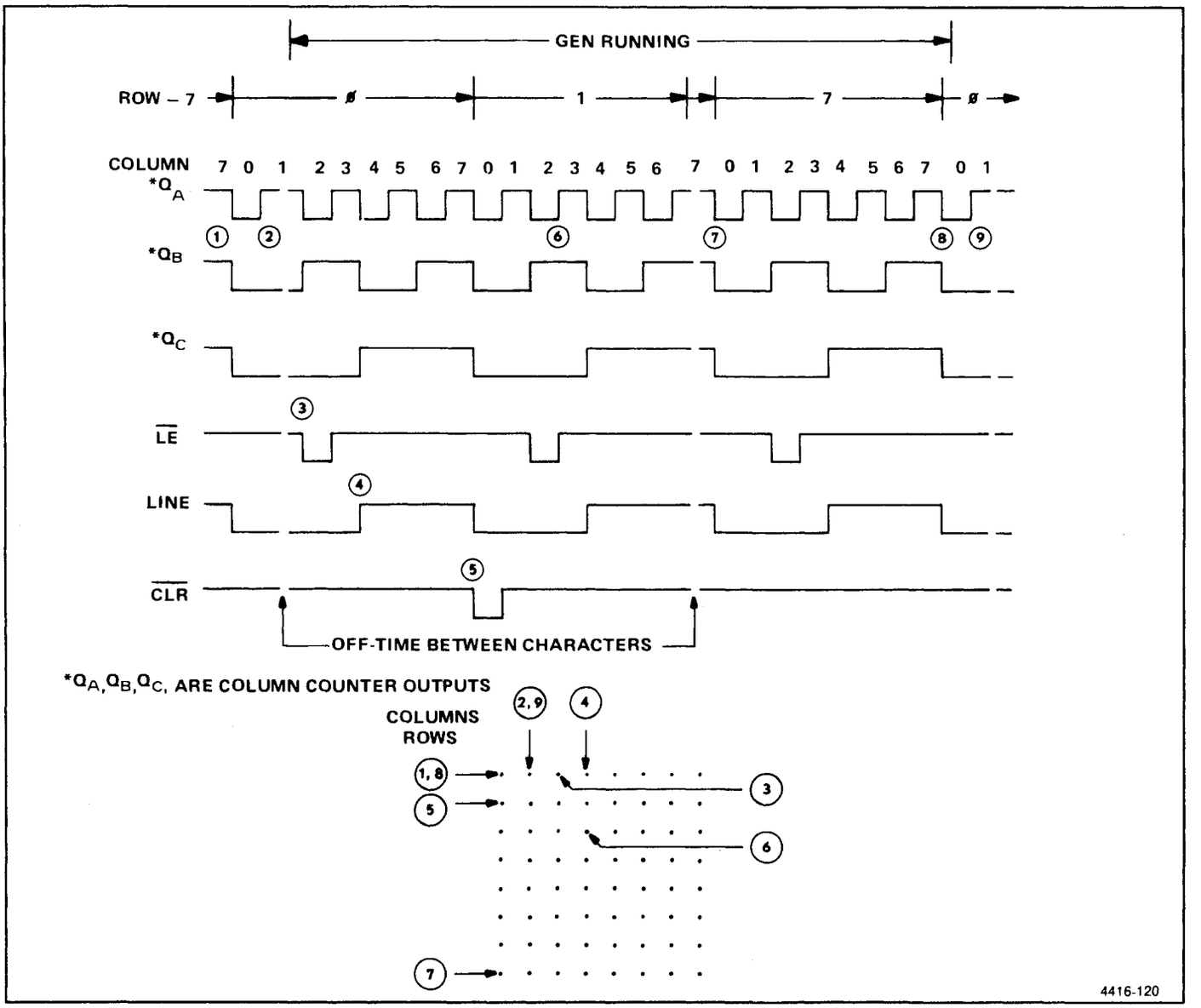


Figure 7-21. Character timing diagram.

Instrument Bus Interface

The microcomputer controls the crt readout and frequency marker dot over the instrument bus through the following ports.

Port	Hex Address
Control/Address	5F
Address/Data	2F

Decoder U3051 asserts 5F when it sees a value of 5 on the upper four bits of the instrument bus address lines, and 2F when it sees a value of 2. The decoder must be enabled by DATA VALID high on the instrument bus. The false transition of DATA VALID causes the addressed port to latch the data on the instrument bus.

Control Port. Control address port U3034 turns the readout on or off, steers data sent to the address/data port, controls the mode of the frequency marker dot, and contains two bits of the RAM address. The bits are defined in Table 7-10. Bit numbering on the instrument bus starts at zero. However, the D and Q pins of U3034 (and some other ICs) are numbered starting at one, following the manufacturers data.

Bit 0 turns the crt readout display on (1) or off (0). When set, this bit releases CLEAR from the GEN RUNNING flip-flop and allows the off timer, U1055, to set

U1041B. Also, when the ON/OFF line goes high, it enables the INCR gate, U1037C, to steer the position counter onto the character RAM address inputs through line driver U3042 and multiplexers U1050 and U1046. When cleared, this bit places an address, latched in U3038 and U3034, on the character RAM address inputs.

Bit 1 interprets data sent to the address/data port as an address (1) or data (0) for the character RAM. Setting this bit disables the character RAM for input and sets up the clock signal to latch the address.

When this bit is set, Q8 of U3034 gates a high on the output of U2044A. This high prevents input to the character RAMs, U2057 and U2052, by setting its R/W input high. This high also disconnects the instrument bus from the character RAM data inputs by disabling U3047; meanwhile, U2037A is enabled to gate the clock signal that latches the address. The positive clock transition is applied to U3038 when DATA VALID goes false at the end of a write cycle to the address/data port, releasing 2F.

When this bit is cleared and 2F is asserted, U2044A enables the character RAM for input and passes the data through U3047.

Table 7-9
CONTROL PORT

Bit	Function
0	Readout on/off
1	Address/data
2	A9 of RAM address
3	Max Span dot
4	A8 of RAM address
5	16 line mode
6	40 characters/line
7	Spectrum display available

Bit 2 is the MSB of the RAM address.

Bit 3 controls the frequency dot marker. This bit is set in the MAX SPAN mode to position the frequency dot with MAX DOT CONTROL from the Sweep board. When cleared, this bit centers the frequency dot on the spectrum display.

Bit 4 is the A8 address line for the character RAMs.

Bit 5 is the select for 16 lines mode.

Bit 6 selects the 40 character/line mode.

Bit 7 enables the clipped display with the spectrum. When high, U1055 is enabled and causes 140 micros periods to occur between characters when the spectrum is disabled. When low, U1055 is disabled, R/O OFF is forced low to disable the spectrum display, and W1028E forces the current boost addition to be disabled. Also, U1016 is disabled so that the marker dot is not displayed.

Address/Data Port. The microcomputer loads characters for crt display through the address/data port. Each character requires the following four write cycles.

1. Bit 2 in the control port is set for an address transfer, and the upper 2 bits of the RAM address (A8, A9) are sent.

2. The lower 8 bits of the address in the character RAM are sent to the address/data port.

3. Bit 2 in the control port is cleared.

4. The data is sent to the address/data port. The bits are defined in Table 7-10. Bits 0-5 are the lower six bits of the character RAM address or are the ASCII code for the character.

Table 7-10
ADDRESS/DATA PORT

Bit	Function
0-5	Address of ASCII code
6	Skip bit
7	Blank character

Bit 6 causes the line counter, U2014, to skip a line, if set.

Bit 7 is used to reduce overhead readout display. It is set when a space is transferred to the character RAM, so the readout does not steal time from the spectrum trace to scan a blank. When set, this bit prevents the GEN RUNNING flip-flop from gating R/O OFF low through U2044B.

Frequency Dot Marker

The frequency dot marker is refreshed immediately after the last character position in the lower readout is scanned. Normally, the marker is centered on the screen just below the upper readout as a pointer for the center frequency readout. When MAX SPAN is selected, however, the dot marker moves to a point on the display that corresponds to the center frequency value.

The negative transition of line D triggers the marker generator. A simplified diagram of the circuit and its timing is shown in Figure 7-22.

U1016A delays the marker dot to allow retrace while gating DOT INV low to set up the display. DOT INV affects the readout deflection outputs in the following ways.

1. The horizontal output is connected either to ground, for a center-screen dot, or MAX DOT CONTROL, for a max span pointer. MAX DOT CONTROL is proportional to the center-frequency readout offset from the center of the frequency range.

2. The U1025B output goes low during the dot interval to cause Q3018 to insert an offset current into the vertical output, to shift the dot position down on the screen.

3. R/O OFF is gated low to switch the deflection amplifier inputs from the Trace Mode to the Readout Mode, using the marker dot horizontal and vertical signals.

When the retrace one-shot times out after about 5.9 μs, it's Q line triggers the unblanking one-shot U1016B, which sets R/O UNBLANK high for 5 μs, via DISPLAY MKR DOT through U1037A. This refreshes the dot. DISPLAY MKR DOT also holds DOT INTVL low through CR1013, until the dot marker is drawn. R1015 and C1011 slow the rise of DOT INTVL to prevent a spurious signal through the "diode AND" gate.

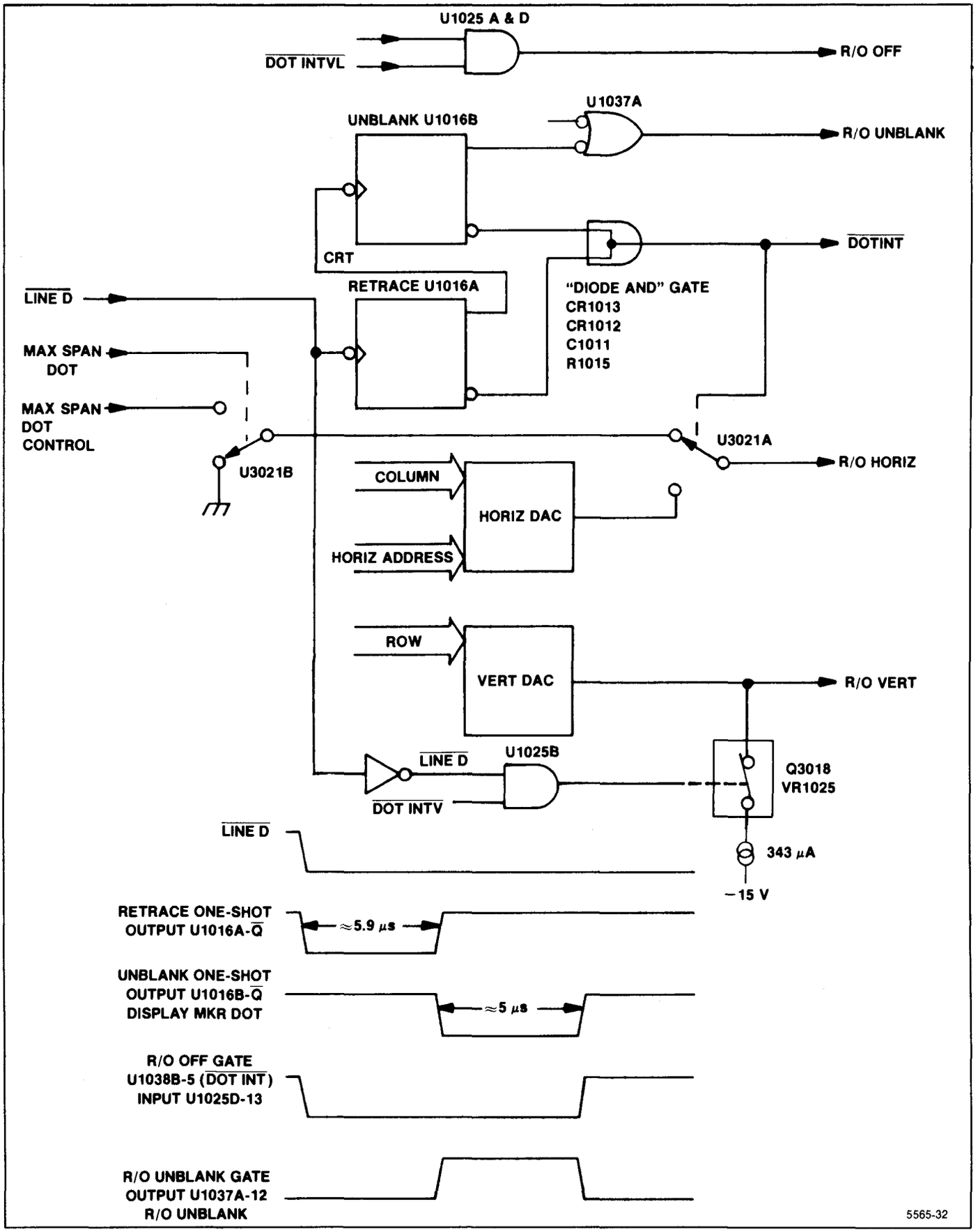


Figure 7-22. Frequency dot marker simplified diagram with timing waveforms.

FREQUENCY CONTROL SECTION (Diagram 7)

The Frequency Control section performs the tuning and scan function for the Preselector, 1st LO, and 2nd LO. It also provides the sweep voltage for the deflection amplifiers in the Display section so the crt display is coincident with the frequency scan and tuning. This section contains the following major circuits.

Sweep

Circuits on the Sweep board accept trigger inputs from line, internal and external sources, and the normal free-run mode of operation. They also receive external horizontal and manual sweep inputs. The circuits produce a PEN LIFT signal for chart recorder applications, a SWEEP GATE signal for crt display blanking, a SWEEP signal to drive the crt beam across the horizontal axis and drive the horizontal portion of the digital storage circuit, plus a ramp (OSC SWEEP) that is fed through the Span Attenuator to the Preselector Driver, the 1st LO Driver, and the 2nd LO.

Span Attenuator

This circuit attenuates the ramp signal as required, to sweep the frequency of the 1st and 2nd local oscillators, and tune the Preselector so it tracks the center frequency.

Center Frequency Control

The Center Frequency Control circuit provides a tuning voltage for the 1st and 2nd Local Oscillator circuits that results in a linear center frequency change as the front panel FREQUENCY control is changed. The circuit is directly controlled by the microcomputer, so remote control of the frequency is possible, by way of the GPIB rear-panel connector. The COARSE TUNE VOLTS signal from this circuit is applied to the 1st LO Driver circuits for summing with the SPAN signal to drive the 1st LO. The FINE TUNE VOLTS signal is applied to the Preselector Driver for summing with the IF Offset voltages, and to the 2182 MHz Phase Locked 2nd LO circuit for summing with the 2nd LO SWEEP signal.

1st LO Driver

The 1st LO Driver performs the following:

- Combines the COARSE TUNE VOLTS signal with the SPAN signal and outputs a current to drive the 1st LO.
- Produces the tuning and sweeping signal for the Preselector Driver circuits.
- Produces the mixer bias voltages.
- Produces a reference voltage that is used in both the 1st LO Driver circuit and the Preselector driver.
- Produces a supply voltage for the 1st LO.

Preselector Driver (Option 01 only)

The Preselector Driver combines the FINE TUNE VOLTS signal, from the Center Frequency Control board with the PRESELECTOR DRIVE signal and the SPAN VOLTS signal from the 1st LO Driver. This combined signal is offset, to compensate for the selected 1st IF, then shaped so the Preselector tracks with the 1st or 2nd LO as it is tuned by the output current. The Preselector Driver also drives the Filter Select switch that selects either the Preselector or the Low-pass Filter, depending on the frequency band selected. This circuit is only installed in instruments with the preselector (Option 01).

SWEEP (Diagram 31)

The circuits on the Sweep board (A72) provide the ramp voltage that drives the horizontal deflection amplifier, the 1st LO Driver and the Option 01 Preselector Driver, the 2nd LO, and a voltage used to align the frequency control system with the digital storage marker positions. The sweep board also provides signals for the Z-Axis circuitry, an external plotter pen, and digital storage.

The major circuits on the Sweep board are:

- Sweep Generator
- Trigger Circuits
- Sweep Control
- Digital Control
- Marker DAC

The sweep generator generates the voltage ramp that drives the Deflection Amplifiers, Digital Storage, Option 01 Preselector, and the swept oscillators.

The trigger circuits process and multiplex the three trigger signals.

The sweep control circuit generates the SWEEP GATE and PEN LIFT signals and determines the holdoff time for the sweep generator.

The digital control circuits receive and decode the address and instructions from the microcomputer, select the sweep rate, holdoff time, trigger source, sweep mode, control marker dac, and control interrupts to the microcomputer.

The Marker DAC provides a dc level corresponding to the marker sweep position.

The Sweep board analog section consists of the ramp or sweep generator plus its output buffers that drive the deflection amplifiers, the oscillators, digital storage, Z axis, and the trigger circuits. The sweep and trigger circuits are digitally controlled.

Digital Control

Three instrument bus addresses are associated with the sweep board. Addresses 0F and 1F are write addresses and 9F is a read address. Two bits at address 1F subdivide address 0F into four subaddresses.

Bus decoder U4030 outputs lows for addresses 0F, 1F, and 9F. U4020 buffers the instrument bus data bits. U1027 is used as a 6-bit register to hold data at address 1F. Data bits 6 and 7 go to U1030 which decodes which of U1035, U2030, U1045, and U1040 are activated at address 0F by U4030. These registers store the microcomputers latest commands (except for the trigger single sweep and the abort sweep commands, which are not stored) and they control most of the operation of the sweep board.

Commands that can be written are:

- Sweep start for single sweep mode (bit 3 of 1F high).
- Single sweep operation (bit 0 of 0F.0 high).
- Sweep rate selection (bits 0-4 of 0F.1, see Table 7-11).

TABLE 7-11
SWEEP RATE SELECTION CODES

Sweep Rate	D4	D3	D2	D1	D0
20 μs/div	1	1	0	1	1
50	1	0	1	1	1
100	1	0	0	1	1
200	0	1	0	1	1
500	0	0	1	1	1
1 ms/div	0	0	0	1	1
2	1	1	0	0	1
5	1	0	1	0	1
10	1	0	0	0	1
20	0	1	0	0	1
50	0	0	1	0	1
100	0	0	0	0	1
200	1	1	0	0	0
500	1	0	1	0	0
1 s/div	1	0	0	0	0
2	0	1	0	0	0
5	0	0	1	0	0
10	0	0	0	0	0
Manual	1	1	1	1	1
External	0	1	1	1	1

Commands written to address 1F control the triggers and sweep holdoff time. These commands are as follows:

- Abort sweep (bit 0 of 1F goes high).
- Ignore input trigger signals (bit 1 of 1F high).
- Disable sweep gate and blank non-store display (bit 2 of 1F high).
- Trigger mode (controlled by bits 3 & 4 of 0F.0, see Table 7-12).
- Sweep holdoff time (bits 5 & 6 of 0F.0, see Table 7-13).
- Interrupt at end of sweep (Data Bus bit 4 goes low when the microprocessor does a POLL after it detects the interrupt, bit 1 of 0F.0 enables the end of sweep interrupt).

Table 7-12
TRIGGER SELECTION MODES

Trigger Mode	D4	D3
Free run	0	0
Internal	0	1
External	1	0
Line	1	1

Table 7-13
SWEEP HOLDOFF SELECTION

Sweep Holdoff	D4	D3
Short	0	0
Medium	0	1
Long	1	0

The Interrupt and Service Request circuit generates the instrument bus interrupts and responds to the subsequent poll routine from the microcomputer. The Sweep board causes an interrupt when an EOS (end-of-sweep) occurrs. When an EOS occurs, and provided the EOS Interrupt Enable bit is high, flip-flop U1010A is clocked and its Q(bar) goes low. This produces a high out of U1020B which turns Q4032 on to pull the instrument bus line SER REQ (service request) low and forces an interrupt.

The microcomputer response to an interrupt is with a poll routine. It first writes FF to the instrument address bus. The Sweep board address decoders normally respond only to addresses 0F, 1F, and 9F, but the interrupt circuit detects when bit 7 of the address bus (AB7) goes high. The microcomputer raises the POLL line and reads the instrument data bus. The output of U2010A goes low. This, anded with the low out of U1010A, generates a high to turn Q3020 on and pull bit DB4 of the instrument bus low. When the microcomputer reads a low on bit DB4 it lowers the POLL line and writes 7F on the instrument bus. Again, none of the other decoders respond. However, bit 7 (AB7) of the address is pulled low. The microcomputer now writes a word to the data bus with all bits except bit DB4 high. This acknowledges the interrupt. The microcomputer now raises the POLL line again and since both inputs to U2010B are high, the output of the gate goes low. The POLL line is then pulled low and the low-to-high transition clocks the low on the D input of U1010B through to reset U1010A. Its Q output then sets U1010B. Q4032 is cut off, the interrupt is removed, and the circuit is now ready for another EOS.

Sweep Generator

The sweep generator is an integrator circuit consisting of operational amplifier U1055 with one fixed and two switchable capacitors in the feedback circuit. Fixed capacitor C1061 is used for the faster sweep rates. The other two capacitors, C1065 or C1062, are added to change the time constant when either Q2068 or Q2064 are switched on by comparators U1060A or U2050A. These comparators are driven by register U2030, which interfaces to the instrument bus. For manual sweep operation, Q2060 is turned on and the integrator becomes an amplifier.

Multiplexer U3060 connects timing resistors between a −12 volt reference, out of U3050B, and the input to integrator U2060. Data bits D2, D3, and D4 of address 0F.1 drive the select inputs of the multiplexer. The voltage reference of −10 volts out of U4055 is boosted to −12 volts by U3050B. A voltage divider sets the non-inverting input of U1055 to −8 volts. Therefore, there is about 4 volts difference across the timing resistors. The timing current through the resistors varies over two decades such that 1/I is proportional to a 2-5-10 sequence.

Switching in feedback capacitors C1065 and C2060 each changes the sweep rate by a factor of 100 times. Sweep Accuracy adjustment, R1062, compensates for differences in timing voltage or timing circuit values. The timing capacitors are matched so that one adjustment compensates for small variations in each set.

Trigger Circuits

The sweep circuit can be triggered by an externally applied signal, the internal video filter signal, or from the power line. Each trigger signal is converted to TTL level and then applied to trigger multiplexer U2026, part of the trigger control circuit. The trigger control circuit selects the desired triggering signal and triggering mode or rejects the trigger to let the sweep circuit free run, be manually controlled, or let the external sweep mode be used.

An external trigger signal applied to the external HORIZ/TRIG connector is converted to TTL level by Q2030. CR2030 limits any voltage surges that may be on the line. Line trigger signals, from the power supply, are applied through comparator U3025A to the multiplexer. Video Filter Out signals from the Video Processor board are buffered by Q4037 and converted to TTL level by Q3030. Both the external and video trigger signals are applied to multiplexer U2026 through Schmitt trigger inverters in U1015C.

Under control of the data (D2 and D3) from register U1035 (at extended address 0 of address 0F), the multiplexer selects the trigger signal and passes it to flip-flop

U1016B. After retrace and holdoff time, U1016B allows a trigger to pass through U2026 and U2020C to reset the Sweep State Control flip-flop U1025. When U1025 is reset the integrator starts a new sweep.

Sweep Output Circuits

The sweep ramp from the integrator is applied through buffer amplifiers, U3045 and U4050, and a bus on the Mother board to the Deflection Amplifiers, Span Attenuator, and Digital Storage board. The sweep out of U3045 is an 11 volt peak-to-peak ramp centered around 0 volt. The sweep out of U4050 is a 22 volt peak-to-peak ramp for the oscillators.

The sweep signal also drives pen-lift comparator U3010A and the end-of-sweep comparator U3010B. The threshold for the pen-lift comparator is +7.4 volts. The threshold for the end-of-sweep comparator is +8 volts. The sweep ramp, from the integrator, starts at −8 volts and rises towards +8 volts. When the signal reaches +7.4 volts, the pen lift comparator toggles. This output is gated through U3015B and the pen lift signal goes high. When the sweep ramp reaches +8 volt, the end-of-sweep comparator, U3010B, toggles. The resultant low output is applied through U1015A to become the EOS (end-of-sweep) signal.

Marker DAC

The Marker DAC circuit provides a dc level corresponding to the marker sweep position. This occurs during retrace, allowing oscillators to operate long enough for the counter to get an accurate reading of the marker position. The processor loads twelve bits to Marker DAC U1047. This dc level replaces the sweep ramp during the during the retrace time when the sweep is inactive. The Marker circuits on the Horizontal Digital Storage board reads the dc voltage and reconverts to digital to feed the processor. The processor compares these bits to the location of the marker in digital storage and adjusts the Marker DAC bits until the digitized voltage matches the marker position.

U1047 is a 12-bit DAC. The 12 bits come from registers U1040 and U1045, the address 0F second and third extended address registers. The DAC produces a current output, which U2040 converts to a voltage. U2045 sums an offset voltage, giving a voltage range of about ±9 volts. This voltage range is greater than the range of the sweep ramp. This fact, and the DAC having twelve bits guarantee that there will be a twelve bit number for the DAC for each of the 1000 digital storage points.

Sweep Control

U1025A is the Sweep State Control flip-flop. When reset, the high at the Q(bar) output turns off FET Q1062 and allows the integrator capacitors to charge. When the Sweep State Control flip-flop is set, by a low on pin 4, its Q(bar) goes low. This switches the output of comparator U1060B so its output turns Q1062 on and discharges the timing capacitors. The Q(bar) output of U1025A connects to pin 5 of U1017A so this low switches the output pin 6 to its high impedance state (its output is open collector). The Q output of U1025A is high. Both U1016A and U1016B where previously set when the Q output was low. This starts the holdoff cycle or retrace time which is described in detail further on.

The Sweep State Control flip-flop U1025A, is set by a low out of NOR gate U2020A when either the EOS (end-of-sweep) or the ABORT SWEEP lines go high. ABORT SWEEP is generated when a 1 is written to D0 at address 1F. The Sweep Control flip-flop is reset by either a trigger signal from multiplexer U2026 or a high on the MNL or EXT SWP line. The microcomputer writes to bits D2 and D3 at subaddress 1 of address 0F for the manual or external sweep mode.

Trigger Control

A sweep is initiated by the microcomputer, in single sweep or manual mode as noted above, or by one of three trigger signals selected by the multiplexer U2026. Data bits D2 and D3 at address 0F.0 select the input trigger signals and route them to the clock input of U1016B. During sweep time the flip-flop U1016B is set by a low on the Q output of U1025A.

The high on the Q(bar) output of U1025A is also applied through an inverter buffer in U1017A. The resultant low out discharges holdoff capacitor C3032 at the input to U3025B. The output of U3025B is low so the output of NAND gate U1020D is high. Flip-flop U1016B requires a high-to-low transition to clock any input through. Since it is high, incoming trigger signals will have no effect on the circuit.

At the end of sweep, the Q(bar) output of U1025A goes low. This switches the output of U1017A to its high impedance state and the holdoff capacitor, C3032, starts to charge towards +15 volts through R3030. When it reaches +5 volts the comparator output switches high. This, along with a high on pin 13 of NAND gate U1020D, causes the output to go low and the high-to-low transition clocks U2026 so the incoming trigger signal can now clock U1016B and produce a high at the Q(bar) output. This is gated through U2026 to the input of U2020C, so the output of the NOR gate will now reset the Sweep State Control flip-flop, U1025A, and start a new sweep.

In the free-run mode the multiplexer U2026, selects the +5 volts on pin 6. This high is clocked through to the Sweep State Control flip-flop immediately after retrace. Incoming trigger signals are ignored and the sweep runs automatically.

In single sweep mode the sweep circuit cannot be re-triggered until it is armed by the microcomputer. Bit D0 is set high at subaddress 0 of address 0F (U1035-6). This appears as a high on pin 2 of U4010A. Since U1016A has been set by the previous sweep, the two highs at the input produce a low at pin 13 of U1020D. Therefore, incoming triggers are disabled. The sweep is now in an idle state and cannot run until the microcomputer arms the trigger circuit again. This is done by setting bit D3 high at address 1F, which produces a high out of U1026 pin 3 and clocks flip-flop U1016A. The resultant low at pin 1 of U4010A forces a high at pin 11 of U1020D, and arms the trigger circuit. Thus a signal can now trigger the sweep circuit and the single sweep cycle repeats.

Sweep Holdoff

During retrace, the sweep must be held off long enough for the timing capacitors in the integrator to discharge and the circuit to stabilize. To prevent flicker, the holdoff period must vary as sweep time changes. U3025B and three timing capacitors (C3027, C3030, and C3032) plus a resistor (R3030) form the holdoff circuit.

During sweep time pin 5 of U1017A is high. This pulls pin 6 low and discharges C3032. During retrace, pin 6 is released and the timing capacitors start to charge. When they reach +5 V, comparator U3025B toggles and its output goes high. This, along with the high on pin 13 of the NAND gate U1020D, provides the clock pulse for U2026 to pass a trigger signal through to the Sweep State Control, U1025.

SPAN ATTENUATOR (Diagram 32)

The Span Attenuator, under control of the microcomputer, selects the appropriate attenuation factor for the incoming sweep signal, to establish the frequency span. Refer to the block diagram adjacent to Diagram 32 as well as the schematic diagram. The Span Attenuator consists of digital control circuits, which receive and decode the address and instructions from the microcomputer; the input amplifiers, which perform noise reduction and signal inversion on the incoming sweep signal; the digital-to-analog converter, which attenuates the sweep signal to the desired amplitude for driving the 1st LO Driver and Preselector Driver circuits; and the decade attenuator, which provides three decades of attenuation for the output signals

Digital Control

Decoder U5025 decodes the address information from the address bus and sends a low signal to either of the two latches, U1025 (address 75) or U2015 (address 76), when a latch is addressed and the DATA VALID line moves high. (The data is stored in the latches on the trailing edge of the DATA VALID signal.) Logic buffer U4015 reduces loading of the data bus. Latch U1025 stores data that controls the eight least significant digits of the span attenuation factor. Latch U2015 stores data that controls the two most significant digits of the span attenuation factor, and other functions on the board. When a span attenuation factor is selected, the microcomputer selects an address and places the first byte of the data on the bus. The DATA VALID signal causes the data to be stored in one of the two latches. Then the second address is called and the next byte is stored in the other latch. The block diagram illustrates the significance of each bit in tables near the affected circuit. A logic 1 represents the more positive of two levels or high state, and a logic 0 represents the more negative of two levels or low state.

Input Section

The sweep signal and its ground reference are applied to differential input buffer U3036. Any signals or noise induced in the two signal transmission paths are canceled by this stage.

The following stage consists of amplifier U3032, plus switching transistors Q2025, Q2028, and Q2023. Different mixing modes require the 2nd LO frequency to either increase or decrease to increase the signal frequency. Thus, this circuit is a unity gain amplifier that can be changed from inverting to non-inverting, under bus control. When line Q8 of latch U2015 is low, Q2023 conducts and its collector moves positive to about +5 V. This in turn causes both Q2025 and Q2028 to conduct. Pin 3 of U3032 is effectively grounded, the sweep signal is applied through R3028 to the summing node of the amplifier, and the gain of the stage is −1. If line Q8 is high, Q2023 does not conduct and the voltage at its collector falls to nearly −15 V. Neither Q2025 nor Q2028 are now in conduction, so the sweep signal is applied to pin 3 of U3032, and pin 2 is disconnected. Now, the gain of the stage is +1.

Digital-To-Analog Converter

The magnitude of the sweep signal is determined by the desired frequency span, band, and option installed in the instrument. The microcomputer calculates the proper magnitude for each combination, and sends the appropriate codes to the data latches, which in turn control the attenuation factor of the digital-to-analog converter. This stage consists of converter U1042,

amplifier U2042, and a complementary pair, Q2062 and Q3056, that form the output current buffer.

Figure 7-23 illustrates a simplified two-bit digital-to-analog converter. The circuit works by current division. Since the summing node of the amplifier is at ground potential, the magnitude of the current through a resistor is not affected by the position of the switch that selects that resistor. For example, when switch S1 is at position B, the current is shunted to ground. When S1 is at position A, the current through R1 becomes part of the total output current. Thus, the output current can be 0, 1/4, 1/2, or 3/4 of the total current available. Because of the resistance ratios, the ratio of the output voltage to the input voltage equals the ratio of the output to the total current ($V_{out}/V_{in} = I_{out}/I_{total}$). In this 2-bit converter, there are 2^2 or 4 output values possible. In the actual 10-bit converter, there are 2^{10} or 1024 output values.

In converter U1042, each internal resistance is switched in or out by a CMOS FET (internal to the device). The CMOS inputs are each protected by a series input resistor. Since the sweep signal is applied to the Vref input, U1042 serves as a digitally controlled attenuator for the sweep signal.

The attenuated sweep signal from U1042 is applied to U2042, an operational amplifier. It in turn drives an output current buffer, consisting of complementary pair Q2062 and Q3056. The pair is biased to produce a standing current of about 10 mA in the absence of an applied signal. This eliminates crossover distortion of the output signal. Diodes CR2051, CR2053, CR1051, and CR1049 provide temperature stabilization for the bias current in the stage. When high current is passing through the pair, diodes CR1056 and CR1061 clamp the voltage across the emitter resistors to reduce voltage drop.

Feedback for the output stage is provided by R1056, plus an internal resistor in U1042. The internal feedback resistor ensures better temperature tracking. The internal resistor provides a gain slightly less than unity; R1056 increases the stage gain and permits gain calibration, as described below.

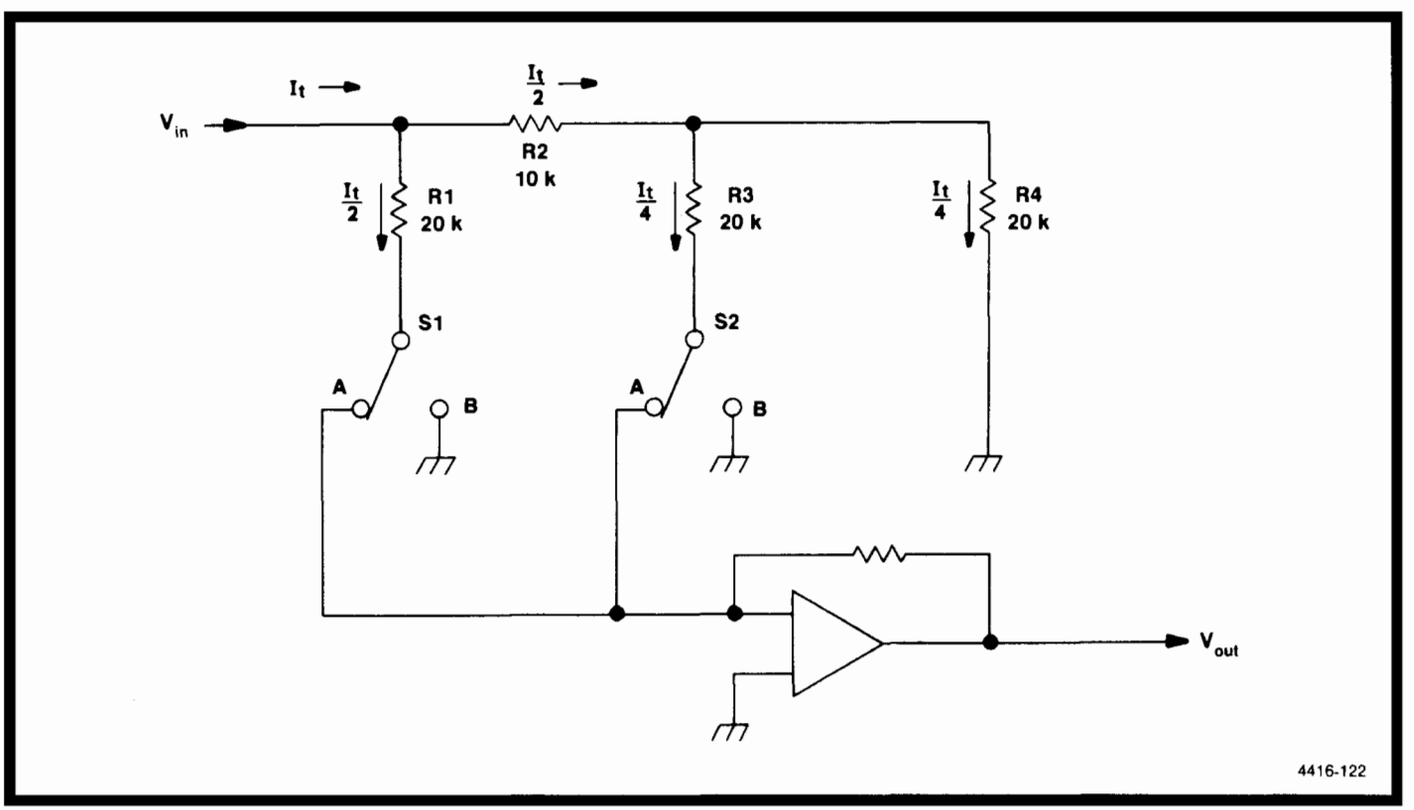


Figure 7-23. Simplified digital-to-analog converter.

One-of-four decoder, U4025, uses data bits DB3 and DB4 lines from U2015, to control three sections of a quad FET switch, U3025. (RC circuit inputs of each FET control line filter out noise from the digital circuits.) The code is exclusive; i.e., only one FET is switched on at a time. See Table 7-14 for a listing of the codes. When a FET is switched on, it connects a calibration adjustment potentiometer to the summing node of the operational amplifier. Adjustment R1065 sets the 1st LO tune coil sweep, R1071 sets the 1st LO FM coil sweep, and R1067 sets the 2nd LO span.

Table 7-14
CALIBRATION CONTROL SELECTION CODES

U4025		
DB3 (Pin 3)	DB4 (Pin 2)	Selected Adjustment
0	0	R1065 (main coil)
0	1	R1071 (FM coil)
1	0	R1067 (2nd LO)

Decade Attenuator

Since accuracy of the digital-to-analog converter is specified as a percentage of full scale, the accuracy decreases as the attenuation is increased. To maintain accuracy at 1%, it is never used at an attenuation factor of more than ten. If more attenuation is required, the decade attenuator, consisting of K4072, K3075, K3065 and the connected divider network, provides further sweep attenuation of X0.01, X0.1, and X1. See Figure 7-24 for a simplified circuit diagram.

The "2" side of U4025 is controlled by data bits, DB5 and DB6, on the Q6 and Q7 lines from U2015. The "2Y" outputs of U4025 are applied through buffers in U4042 to select the appropriate attenuation factor for the output sweep. Table 7-15 lists the states required to energize the attenuation relays. A diode across each relay coil protects the driving circuit from inductive feedback transients.

Table 7-15
ATTENUATION SELECTION CODES

U2015		
DB5 (Pin 15)	DB6 (Pin 16)	Attenuation Factor
0	0	×1 (K3065)
1	0	×0.1 (K3075)
0	1	×0.01 (K4072)

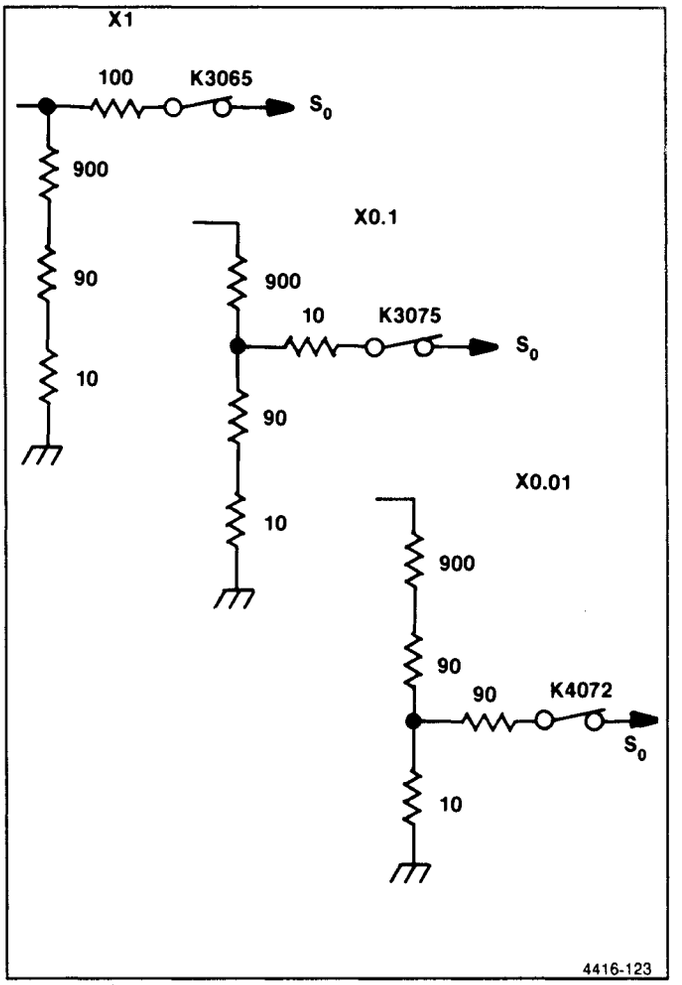


Figure 7-24. Simplified span decade attenuator.

1st LO DRIVER (Diagram 33)

The 1st LO Driver performs the following functions:

- Combines the SPAN VOLTS with the COARSE TUNE VOLTS and outputs the combination to the Preselector Driver (the combined signal is also applied to the Oscillator Driver circuits, which drive the 1st Local Oscillator coil).
- Selects and outputs the appropriate bias voltage to the internal or external 1st Mixer.
- Outputs a voltage to the Preselector Driver that peaks the Preselector.
- Controls the oscillator filter switch.

- Produces a stable and precise −10 V reference for both the 1st LO Driver and the Preselector Driver circuits.

The major circuits and their function are as follows:

- The digital control circuits buffer the incoming data from the data bus, decode the address data, select the required mixer bias, connect or disconnect the TUNE VOLTS and SPAN VOLTS signals to the summing amplifier, energize the filter switch in the 1st LO assembly, and control the drive and filtering of the oscillator driver stage.

- The oscillator filter switch driver, furnishes drive current to the capacitor switching relay in the 1st LO assembly

- The input switching circuit, connects or disconnects the SPAN VOLTS and COARSE TUNE VOLTS signals to the input of the summing amplifier.

- The summing amplifier, furnishes the drive signal to the oscillator driver. The summing amplifier sums the SPAN VOLTS ramp signal, from the Span Attenuator, with the COARSE TUNE voltage, from the Center Frequency Control circuit. In less than maximum span, a sweep voltage of ±10 V sweeps the oscillator at a rate of 333 MHz/ division. As the TUNE VOLTS signal varies from −10 V to +10 V, the oscillator's center frequency is moved over its full range.

- The oscillator driver, furnishes the current drive for the 1st LO coil.

- The −10 V reference supply, produces a precise −10 V reference for the 1st LO Driver and the Preselector Driver.

- The mixer bias circuit, produces and outputs the required bias voltages for the 1st Mixer.

- The programmable bias circuit, provides peaking voltage for the Preselector based on data supplied by the microcomputer.

Digital Control

The digital control circuit sets the oscillator span volts, the 1st Mixer bias and programmable bias. Decoder U4034 output Y1 (pin 14) goes low when the input address is 72 and output Y7 goes low for address 7E. When output Y1 goes high, data is clocked or latched into U4017, and when Y7 goes high data is latched into U4024 and U4022.

Data for U4017 consists of control codes for the oscillator drive circuits and the switches in U1016, which select 1st Mixer bias or the bias set by the front panel MANUAL PEAKING control. The codes are described where each applies to the description and in Table 7-16. Data for DAC U3022 is converted to an analog signal which provides the Programmable Bias for the instrument.

Table 7-16
U4017 OUTPUT LINES

Signal	Low	High
Q1(DB0)	Bias 1 on	Bias 1 off
Q2(DB1)	Bias 2 on	Bias 2 off
Q3(DB2)	Bias 3 on	Bias 3 off
Q4(DB3)	Manual peaking on	Peaking off
Q5(DB4)	Driver filter off	Driver filter on
Q6(DB5)	Driver input on	Driver input off
Q7(DB6)	SPAN VOLTS line off, oscillator filter on	SPAN VOLTS line on, oscillator filter off

Input Switching. If the main coil of the oscillator is not to be swept, DB6 (line Q7 of U4017) goes low. This cuts Q3028 off, de-energizes K3034 and disconnects the SPAN VOLTS signal to the summing amplifier. Diode CR3031 protects Q3028 from the inductive feedback surges that occur at turn-off.

Oscillator Filter Switch Driver. When relay K3034 is de-energized, DB6 is low, Q2029 is biased on which drives a capacitor switching relay on the 1st LO Interface board. The capacitors are switched across the main coil, when it is not being swept, to filter noise riding on the tuning current. Capacitor C2025 provides a gradual decay of current through the relay after power is turned off.

Summing Amplifier. Amplifier U2032 and the complementary pair of transistors, Q2035 and Q2039, plus related components, comprise an operational amplifier. The COURSE TUNE VOLTS and the SPAN VOLTS are summed at the input to U2032. The feedback resistor, for the operational amplifier, is R1038. The input resistance is R2027 for the COARSE TUNE VOLTS signal and R2031 for the SPAN VOLTS signals. (R2030 is switched across R2031, as mentioned previously, to increase stage gain for maximum span operation.) The output of the summing amplifier, which can swing from −10 V to +10 V, is applied to the Preselector Driver circuits and to the Video Processor board.

Oscillator Driver. The output of the summing amplifier also drives the input to the oscillator driver stage when FET Q2040 is switched on. The oscillator driver stage consists of active components Q2045, U2043, Q3047, and Q352. The input resistance consists of R2041, the 1st LO Sensitivity adjustment R1031, plus R2043. The feedback resistance is R2042. The amplifier converts a voltage input into a current drive for the 1st LO tuning coil by controlling the voltage across current sense resistor R1040, which is in series with the oscillator tune coil. Q3047 assures that Q352 base current remains within the oscillator tuning coil circuit. Q2040 is biased on except when the oscillator is degaussed. The output of the operational amplifier U2032, Q2039 and Q2035, is applied through the 1st LO Sensitivity adjustment R1031, and summed with an offset voltage set by the 1st LO Offset adjustment R1032, at the input to the preamplifier stage Q2045. Adjustments R1031 and R1032 match the oscillator driver stage to the oscillator characteristics. R1032 adds offset to the input of the preamplifier to place the oscillator at center operating frequency when the amplifier input is at 0 V.

Q2045 is a low-noise, matched, dual transistor. The feedback path through R3040 and R2042 sets the voltage across a four-terminal resistor R1040. This voltage sets the current through the resistor which is also emitter current for driver transistor Q352. The 1st LO Sensitivity adjustment R1031, sets the voltage gain of the amplifier. This in turn, changes the current drive to the oscillator coil.

Reference Supply. Preamplifier Q2052 plus amplifier U2052 and emitter follower Q2051, are the active components of the −10 V reference supply. Bias for one side of Q2052 is set by VR1055. The other side is set by the −10 V Adj R1034. Any change in the supply is amplified by Q2052 which changes the drive to the pass transistor Q2051 which compensates for the change. The diode network across the base-emitter junction limits the emitter current to about 30 mA, protecting the transistor from damage.

Mixer Bias Driver. The mixer bias driver circuit, which consists of quad FET switch U1016, amplifier U1025A, and buffer Q2025/Q1028, plus associated circuitry, furnishes the required bias current (up to 20 mA) to the 1st Mixer circuit. The bias voltage varies from +1 V to −1 V for the internal mixer.

Mixer bias is selected, by the data out of U4017 to the quad FET switch U1016, and fed to the inverting input of U1025A. The output of U1025A drives the base of a pair of complementary transistors Q1028 and Q2025 which provide the 1st Mixer Bias voltage. When any of the Q1 through Q4 (D0 to D3) lines of U4017 go low, the respective switch within U1016 closes and connects one of the Bias adjustment potentiometers or the output of U2018 (the programmable bias line) to the input of U1025A.

When the Q4 (DB3) line of U4017 goes low, U1016 selects the Programmable Bias line as the 1st Mixer Bias source. The Programmable Bias is set by the data loaded into DAC U3022, by the microcomputer, or by the front panel MANUAL PEAK control. The MANUAL PEAK control is connected to the input of U2018 when the Q5 line (DB4) of U4024 goes low and turns Q3019 on. When MANUAL PEAK is selected, the DAC output is set for 0 V.

Programmable Bias. When the microcomputer sends address 7E to decoder U4034, pin 7 (output Y7) goes low. At the end of data output cycle, data is clocked into either U4024 or U4022, depending on which latch is enabled by DB6 or DB7. This data is then converted to an analog current by U3022 which is the current source for operational amplifier U2018. The resistance between output terminals 16, 2, and 15 of U3022 is the input resistance for operational amplifier U2018. R2022 is the feedback resistance. The output of U2018 is a bias voltage that is fed, via the Programmable Bias line, to the Preselector Driver board where it is summed with the drive voltage for the Preselector.

PRESELECTOR DRIVER (Opt. 01 only) (Diagram 34)

The Preselector provides RF input selectivity between 1.7 and 21 GHz. This selectivity reduces spurious responses over this frequency range. Refer to the block diagram adjacent to Diagram 34 as well as the schematic. The Preselector Driver supplies the drive current to the Preselector coil, depicted on Diagram 12, to tune the Preselector. It also furnishes a voltage that is proportional to frequency change through the rear-panel ACCESSORIES connector for an external preselector, if used. The circuit also operates the filter select relay that selects either the Preselector or Low-pass Filter. The major circuits and their function are as follows:

1) The digital control circuit, which stores and decodes the data from the microcomputer and controls the other circuits within the Preselector Driver. The digital control circuit applies the SPAN VOLTS signal to the oscillator voltage processor when FM coil spans are selected, selects the gain of the oscillator voltage processor, turns off the drive signal to the current driver for degauss cycles or when the preselector is not in use, selects the IF offset voltages to be combined with the FINE TUNE VOLTS

signal, adds noise filtering at the driver output when the preselector is not being swept, and controls the filter select switch.

2) The oscillator voltage processor, which attenuates and offsets the input signal for application to the summing amplifier.

3) The IF offset stage, which applies an offset voltage to the summing amplifier. This offset is proportional to the 1st IF frequency in use, including the effects of fine tuning frequency changes of the 2nd Local Oscillator.

4) The summing amplifier, which combines the effective oscillator frequency voltage and the IF Offset voltage to drive the tracking adjustment circuits.

5) The tracking adjustment circuit, which compensates for different preselector sensitivities, compensates any preselector offset, and compensates for non-linear operation caused by magnetic saturation of the Preselector.

6) The final driver stage, which changes the applied signal voltage into a current drive for the Preselector coil.

7) The preselector switch driver, which drives the filter select switch, depicted on Diagram 12. The switch requires a positive pulse to select the Low-pass Filter and a negative pulse to select the Preselector.

Digital Control Circuits

The microcomputer interface circuits, which exercise digital control of the Preselector Driver circuits, consist of address decoder U5036 and latch U5031. Both the write address (77) and the read address (F7) are decoded by U5036.

Data is latched into U5031 on the trailing edge of the DATA VALID signal for address 77. This event coincides with the rising edge of the pulse on pin 3 of U5036. Table 7-17 lists output lines from U5031.

When address F7 is specified, the Y7 line of U5036 goes low. This pulls data line D4 low, informing the microcomputer that a Preselector is used.

Oscillator Voltage Processor

The oscillator voltage processor consists of U1011A, U2028, and related components. The Preselector Drive signal from the 1st LO Driver is applied to a voltage divider and scaling network consisting of R1022, R1023, R1024, and Input Offset adjustment R1031. The input voltage is ±10 V. This voltage is the summation of the sweep and tune voltages, with appropriate scaling. The output of the voltage processor is about 1 V at 2.072 GHz to about 3 V at 6.35 GHz, which corresponds to a scale factor of 2.1 GHz/V. The voltage is directly proportional to frequency; thus the offset is such that if the oscillator could operate to 0 Hz, the voltage processor output would be at 0 V.

Since the preselector drive input is not swept by the 1st LO Driver, when FM Coil spans are used, the SPAN VOLTS, from the Span Attenuator, must be summed by this stage. Line DB3 (Q4 of U5031) goes low when FM coil spans are selected, which turns Q1011 on. This

Table 7-17
U5031 OUTPUT LINES

Signal	High	Low
Q1(DB0)	Selects ×1 gain for U2028	Selects ×3 gain for U2028
Q2(DB1)	Not used	Not used
Q3(DB2)	Connects tracking adjustment output to final driver stage	Disconnects tracking adjustment output from final driver stage; (Preselector current goes to zero
Q4(DB3)	Connects SPAN VOLTS signal to U1011A input for FM coil spans	Disconnect SPAN VOLTS from U1011A
Q5(DB4)	Selects Low-pass Filter (Band 1)	Selects Preselector (Bands 2-5)
Q6(DB5)	Disconnects output filtering	Adds output filtering
Q7(DB6)	Connects 829 MHz offset	Disconnects -829 MHz offset
Q8(DB7)	Connects +829 MHz offset	Disconnects +829 MHz offset

switches the FET Q1022 on so the Span Volts signal is now applied to the inverting input of U1011A, where it is inverted and applied to the input of U2028.

Operational amplifier U2028, has a gain of 1 or 3, as directed by the microcomputer. The output signal in the X3 gain mode represents the effective oscillator frequency swing for bands 4 and 5 when the 3rd harmonic of the LO is used. When the DB0 (Q1 line of U5031) goes low, the respective output of quad comparator U5022 is also low, which holds FET Q2024 cut off. U2028 is now a unity-gain, non-inverting amplifier. When the DB0 goes high, Q2024 switches on and the gain of U2028 is a factor of three. The X3 Gain adjustment, R1052, sets the gain to precisely three in the tripler mode.

IF Offset

The −10 V reference, from the oscillator driver, furnishes the precise reference voltage for the IF offset circuit. Since the offset voltage is proportional to the IF minus 2.072 GHz, no offset is required for the +2.072 GHz IF. FET Q2034 adds the +829 MHz network into the circuit and Q2036 adds the −829 MHz network. DB6 and DB7 (Q7, Q8 of U5031) through two comparators in U5022, control the two FET switches Q2034, Q2036. One, but not both, transistors are switched on to provide the offset voltage to the inverting input of U2045. An output voltage of −9 V from the amplifier corresponds to −2901 MHz or [(−829MHz)−2072 MHz .

The signal on the FINE TUNE VOLTS line, from the Center Frequency Control board, which is used to tune the 2nd Local Oscillator, is applied to the input of U2047. Since it is applied here, it is independent of the voltage tripling action in the voltage processor circuit. The tuning voltage is also applied to the input networks of U2045 through R3044, Q2034, and R1037, Q2036. By varying the magnitude of signal in the inverting path compared to the direct path, the proper magnitude and polarity of fine tune offset for each IF is provided. Table 7-18 lists the offset voltage required for each frequency band.

Summing Amplifier

The effective oscillator frequency voltage, from U2028, and the offset IF voltage, from U2045, are applied to the inverting input of U2047. This stage drives the tracking adjustments stage and furnishes a signal for external preselector drive circuits as well. The external drive line has its own return to reduce ground loops.

Tracking and Shaper Circuits

This stage consists of gain-setting, offset, and shaping circuits. Preselector Sensitivity adjustment R1065 compensates for sensitivity variations between preselectors. Preselector Offset adjustment R1064 compensates for the offset in the preselector. This adjustment sets the preselector frequency to 2072 MHz when the output of U2047 is at 0 V.

The four other adjustments R1054, R1056, R1061, and R1063, are part of a shaper network. The network compensates for magnetic saturation in the Preselector, which would cause a deviation from linearity at frequencies above 14 GHz. Each shaper network is switched in by a resistive divider that, at a given frequency, provides forward-bias to the diode in the shaper to shape the current output.

The front panel PEAKING control applies a small offset through R5065 to the input of the current driver stage. This corrects for non-linearity or temperature drift in the 1st LO and Preselector.

Table 7-18
PRESELECTOR FREQUENCY BANDS

Band	Frequency Range	IF	Harmonic	Approximate Voltage Offset
2	1.7-5.5 GHz	−829 MHz	1st	9.0 V
3	3.0-7.1 GHz	+829 MHz	1st	3.9 V
4	5.4-18.0 GHz	−829 MHz	3rd	9.0 V
5	15.0-21.0 GHz	+2.072 GHz	3rd	0 V

Current Driver

This stage consists of the output stage Q565/Q5052; FETs Q3061, Q3077, and Q2074; amplifiers U2054 and U3054; and transistor Q4037. When the Preselector is not in use, DB2 goes low and turns Q2074 off to reduce the coil current to zero.

Preamplifier U2054 reduces the temperature drift of the output stage. Driver Offset adjustment, R2066 nulls the offset voltage (at which point the temperature drift is least). U2054 drives amplifier U3054. Q3061 isolates U3054 from the output driver Q5052/Q565.

Current amplifier Q5052 drives the main preselector driver transistor, Q565. The stage is biased so the current divides, with most of the current going through the output transistor, and a lesser portion through the bias circuits. The currents rejoin at the Preselector coil. One set of terminals for R4049 carries the coil current, the other set senses the voltage.

When DB5 line goes low, the Preselector is not swept, Q4037 and Q3077 turn on, which adds C4071 across the Preselector coil to reduce noise at the output.

Preselector Switch Driver

Operational amplifier U1011B and the complementary pair of transistors Q4025/Q3025, form the preselector switch driver. This circuit drives the filter select relay as is shown on Diagram 12. This relay requires a positive pulse to select the Low-pass Filter and a negative pulse to select the Preselector.

When DB4 line (Q5 of U5031) goes high, a positive pulse of about 100 ms in duration, generated through RC network C3021/R3021, is applied to the input of U1011B. The output of the operational amplifier drops to about −12 V and a positive pulse is passed through the transistor pair, selecting the Low-pass Filter. When the DB5 line goes low, a negative pulse of the same duration is passed to U1011B. The amplifier output rises to about +12 V and a negative pulse is passed through the transistor pair to select the Preselector.

When the circuit is quiescent neither Q3025 nor Q4025 conduct, since the sum of the zener voltages of VR3011 and VR3012 is greater than the combined supply voltages. When the output of the operational amplifier comes near one of the supply voltages, the transistor, that is connected to the other supply, becomes saturated, and supplies the drive current to actuate the relay coil. CR4012 and CR4013 protect the driver transistors from induced voltage surges and C3028 and R3028 dampen oscillation that occur in the coil.

CENTER FREQUENCY CONTROL (DIAGRAM 35)

The Center Frequency Control converts digital information, from the front panel FREQUENCY control or on the GPIB bus, via the microcomputer, to analog voltages for the 1st LO Driver and Preselector Driver. These in turn control the center frequency of the analyzer. The Center Frequency Control board contains the following major circuits:

1. The Digital Control circuit, which buffers and decodes the addresses and other data to control the other circuits.

2. The coarse and fine storage registers (latches), which store the numerical bytes that control the digital-to-analog converter (DAC) stages.

3. The coarse and fine DAC stages, which convert the digital inputs from the storage registers into analog current and voltage equivalent values.

4. The coarse and fine track/hold amplifiers, which store the analog output values during the approximation routine and compare the stored value to the approximated value for the microcomputer.

5. The write-back circuits, which inform the microcomputer when the stored value and the approximated values are equal.

Operating Modes

An explanation of circuit design principles is given before the operation of the circuit is described. Two DAC chips are used in tandem to get the required resolution. However, this method can cause errors and non-monotonic behavior in the overall converter circuit. To circumvent this problem, the outputs of the tandem DAC units are summed together so that the two units are overlapped by three bits. That is, the MSB of the low-order DAC is weighted equally with the third least significant bit, or 2×10^{-10} bit of the high order DAC. The overlap means that the lower DAC will have sufficient range to monotonically tune the output of the converter over the entire range of the analyzer, but only if the proper codes of the lower DAC device can be found. Now, suppose that the tandem DAC is loaded as follows:

Upper order 1 0 0 0 0 0 0 0 0 0 0 0
Lower order 1 1 1 1 1 1 1 1 1 1 1 1

The contents of the devices are shown overlapped to illustrate the bit weighting. Now assume that the low-order device is to be incremented one bit. The MSB of the low-order device must be moved into the high-order device before the low-order device can be

incremented. Thus, the two must appear as follows:

Upper order 1 0 0 0 0 0 0 0 0 1 0 0
Lower order 0 1 1 1 1 1 1 1 1 1 1 1

If the high-order device operated with no overall linearity inaccuracy, the operation would now be complete and the low-order incrementing could occur. However, the DAC device can vary by one LSB of the correct value. Figure 7-25 illustrates a graph of the best and worst case output. Note, that even in the worst case, the output may move only once every two or three state changes, but the output is always monotonic and within one LSB of the correct value.

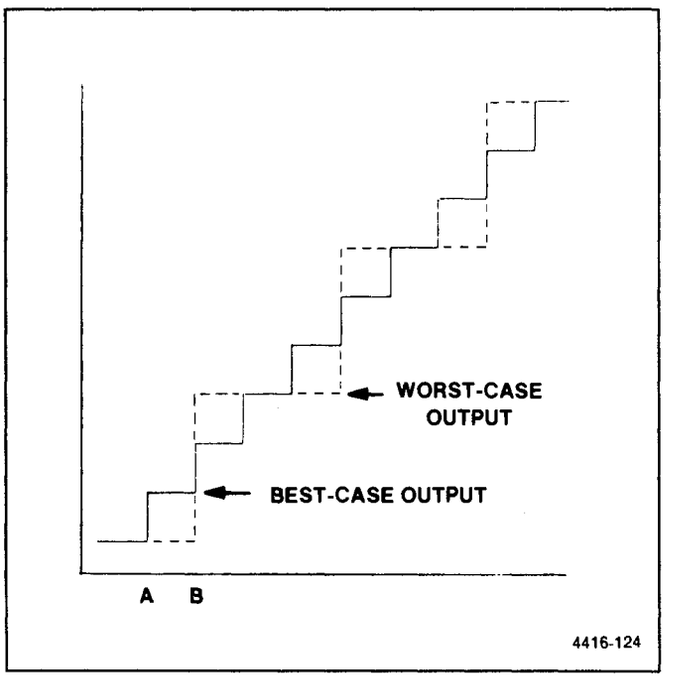


Figure 7-25. DAC Variance graph.

If, in the example shown previously, the high-order device is at point A in Figure 7-25, incrementing the device to point B has no effect on the output. If the MSB of the low-order device is set to zero, as shown in the first example, the combined output will actually decrease. Ordinarily, the Center Frequency Control circuit can increment and decrement whenever the microcomputer commands without going through a special routine. However, as just described, some microcomputer adjustment is necessary to compensate for the disparity that usually occurs between the low-order and high-order DAC units.

The first operating mode is the tracking mode, where the preamplifier and integrator are connected together by the disconnect stage, and the entire unit acts as an operational amplifier. Figure 7-26 illustrates the basic circuit. While the circuit operates in this mode, the amplifier tracks the DAC stage and sends the voltage out to the tuning circuits.

When the transfer of bits from the lower to the upper DAC is required, the microcomputer commands the circuit to shift to the hold mode. The command comes through the decoder to shut off the disconnect stage, and the preamplifier output is disconnected from the integrator. The integrator holds the voltage that was previously at the output for comparison, and the approximation cycle begins.

The microcomputer resets the low-order DAC to zero. Then, the highest order bit in the low-order DAC is set to one, and the circuit is queried to find if the DAC output and integrator output is greater or less than required. If less, the microcomputer loads the next lower bit in addition and queries the circuit once more. This process goes on until the two values are the same. Had the microcomputer found that the DAC output was greater than the integrator output at the first inquiry, it would have set the highest order bit to zero and loaded the second-order bit into the low-order DAC, then continued to load successively lower order bits, one at a time, until the circuit signaled that the comparison had reversed. By this process, which is known as the successive approximation method, the circuit finally reaches the point where the outputs are equal, and the microcomputer commands the circuit to shift back to the track mode.

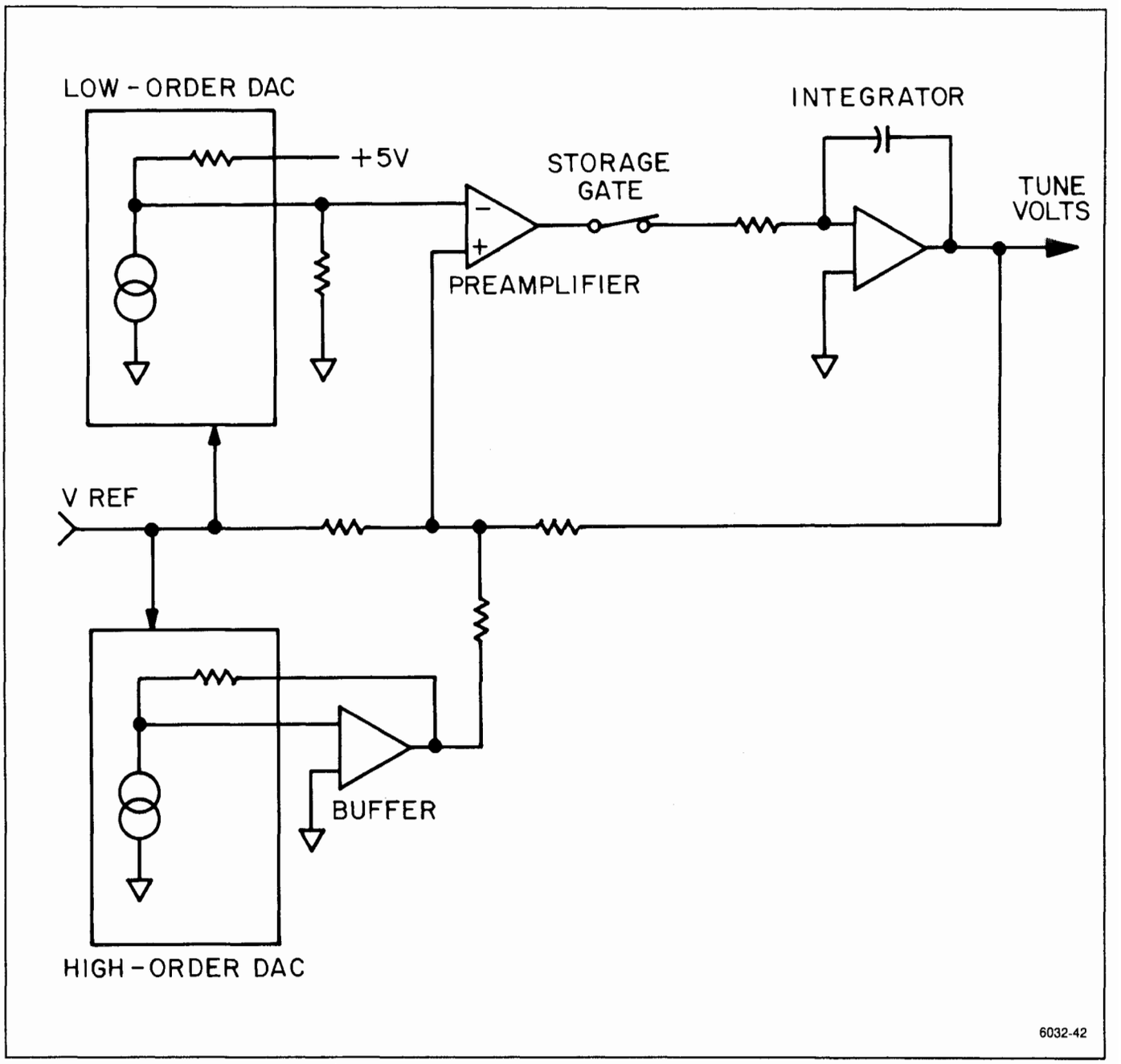


Figure 7-26. Simplified tune voltage converter.

Digital Control

The digital control circuits consist of buffer U4035, address decoder U4045, steering register U4025, and the steering gates (U4015A, U4015B, U4015D, U4060A, U4060B, and U4060D). Because of the large amount of data that must pass through these circuits, a steering register that has a separate address is used. The first byte of data, the steering byte, is clocked into U4025 by the ADDRESS 70 signal. The output levels are applied to the steering gates, and the circuit waits for the next byte. The microcomputer then furnishes the first byte of data to be sent to the low-order, fine-tune, DAC via the storage register. Latch U3015 and part of U3025 form one storage register for the low-order, fine-tune DAC. The byte is clocked into the register by the coincidence of low states at the inputs of the steering gate(U4015A or U4015B); one from the steering byte,

and the other from ADDRESS 71 signal, which is used to clock the steered data bytes into the correct register. This continues until seven bytes of data have been clocked into the register, including the steering byte. The third output from U4045, ADDRESS 80, controls transistors Q1058 and Q2017, which enable the write-back function. In addition to the six steering lines that drive the steering gates, U4025 also controls, by means of the Q3 and Q7 lines, the hold/track selector transistor for each converter side. Table 7-19 illustrates the format for ADDRESS 70. Addresses are expressed as hexadecimal numbers. Table 7-20 lists some of the significant states that are used to tune the DAC.

Storage Registers. Six storage registers are used in the circuit, U3015, U3025, U3035, U3050, U3060, and U3070. Since both sets are identical, only the coarse tune section will be described.

Data from U4035, the data buffer, is clocked into the registers each time a different tune voltage is required. U3050 feeds the lowest eight bits to the low-order DAC, U2055; U3070 feeds the highest eight bits of the high-order DAC, U2060. Register U3060 feeds the remaining bits of both units.

Table 7-19
ADDRESS 70 FORMATS

DB0	Fine Tune low byte enable
DB1	Fine Tune middle byte enable
DB2	Fine Tune high byte enable
DB3	Fine Tune hold
DB4	Coarse Tune low byte enable
DB5	Coarse Tune middle byte enable
DB6	Coarse Tune high byte enable
DB7	Coarse Tune hold

Digital-To-Analog Converters. Since both the coarse and fine tune circuits operate similarly, only the coarse tune section of the board will be discussed here. Figure 7-26 is a functional block diagram of the circuit.

Each side of the converter has two DACs summed together to produce an output of approximately ±10 V. The DACs are programmable current generators driving the preamplifier-integrator circuit. The high-order DAC provides 0 to 2 mA of current to the circuit via the buffer, while the low-order DAC provides approximately ±2.5 mV at the inverting input of the preamplifier. The preamplifier then drives the integrator via the storage gate.

An isolated ground system for each half of the circuit minimizes susceptibility to noise and extraneous signals. This is because the converters provide the dc voltages that tune the oscillators.

Track/Hold Amplifier

The amplifier consists of high-order DAC U2060, low-order DAC U2055, buffer U2050, preamplifier U1065, storage gate Q1065, and integrator U2070.

The circuit output is required to tune approximately ±10 V for the full-scale range of U2060. When U2060 is off and the output of U2050 is at 0 V, the +10 V output level is set by 1 mA of current through R1055, and the combination of R1032, R1053, and R1070. When U2060 is fully on, and output of U2050 is at +10 V, the −10 V output level is set by 2 mA of current through R1052, less the 1 mA constantly flowing in R1055. Full-scale gain is adjusted by R1032. Resistors R1052, R1053, and R1055 are matched for temperature coefficient to minimize output voltage drift as a function of temperature.

Low-order DAC U2055 tunes approximately ±2.5 mV at pin 1, and its gain is adjusted by R1028. The gain of preamplifier U1065 is set at approximately 10,000 by R1056 and the 5Ω combination of R2059 and R2060. The combination of CR1056, CR1058, R1054, and R1059 limits the gain of U1065 when the output exceeds approximately 0.7 V in either direction.

U1065 is connected to integrator U2070 via storage gate Q1065, which is on in the track mode. Transistor Q1065 is turned off any time a DAC is being tuned to allow the DAC output to settle before tuning the output of U2070. It is also turned off during the interval when a carry from the low-order DAC to the high-order DAC occurs. Transistor Q1065 is controlled by Q1061. When Q1061 is on, CR1064 is reverse-biased. The voltage at the gate of Q1065, which is developed by R1064, R1065, R1067, and R1066, is near 0 V and Q1065 conducts. When Q1061 is off, voltage to pinch off Q1065 is applied through R1062 and CR1064.

U2070 tracks the output of U1065 when the circuit is in the track mode and serves as the inverting amplifier in the feedback system shown in Figure 7-26. Normally the incoming signal is routed through R2067. To improve the slewing rate of the integrator, CR1067 and CR1069 conduct and connect R1068 across R2067 when input signals over 1 V are present.

Table 7-20
DAC TUNING CODES

Tuning Point	Data	Address	Results
Positive full range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DACs
Mid-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DACs
	33	70	Enables high byte latch, track mode
	80	71	Loads 80 into DACs. Midrange value
Negative full-range	00	70	Enables all latches, track mode
	FF	71	Loads FF into all positions of both DACs

Write-Back Circuit

This circuit consists of comparator U1055 and enabling transistor Q1058. When it is necessary to do a carry between the low- and high-order DACs, the circuit is put into the hold mode by turning off Q1065. U2060 is incremented one bit and U2055 is reset to all zeroes. The output of U1065 is now at something other than 0 V. The purpose of the following approximation routine is to get output of U1065 as close to 0 V as possible before switching the circuit back into track mode by turning on Q1065. Comparator U1055 detects whether the output of U1065 is above or below coarse tune ground. The instrument microcomputer begins to exercise the low-order DAC bits one at a time from MSB to LSB. After each bit is turned on, U1055 is enabled by turning off Q1058. If U1055 detects that the output of U1065 has crossed 0 V, that bit is turned off and the next lower bit is turned on. This continues through all 12 bits and when completed, the output of U1065 should be close to 0 V. Transistor Q1065 can now be turned back on without causing excessive jumping of the signal on the screen.

−10 V Reference Buffer

The circuit uses the voltage reference developed on the 1st LO Driver board as a reference for the DACs. Differential amplifier U2045 receives the −10 V reference and −10 V reference return, and removes any common-mode signals present. Resistor pairs R1048/R1049 and R1050/R1051 are matched for temperature coefficient to minimize reference voltage drift over temperature.

COUNTER and PHASE LOCK SECTION (Diagram 8)

FUNCTIONAL DESCRIPTION

This section consists of a Counter, Phase Lock assembly, Phase Gate, Harmonic Mixer, and Auxiliary Synthesizer. The Counter, Harmonic Mixer, and Auxiliary Synthesizer, form the nucleus of the frequency control hardware for the instrument. Both the 1st LO and 2nd LO frequencies are controlled via a firmware based control loop that uses data from the Counter as feedback to control oscillator frequency. The 10 MHz IF is also counted to accurately calculate signal frequency.

The Phase Lock assembly stabilizes the 1st LO frequency. It consists of an outer and inner loop.

The inner loop uses the subharmonic of the 100 MHz reference frequency, from the 3rd Converter, to mix with the output from a 25.032 to 25.095 VCO and compares this IF difference with a +N number (between 32 kHz and 94 kHz) set by the processor. Any deviation is detected by a phase/frequency detector whose output error voltage is used to pull the VCO frequency and phase into lock with the inner loop reference.

The outer loop consists of the inner loop, a Strobe Driver, Phase Gate Detector, Error Amplifier, and the 1st LO. The frequency of the inner loop VCO is divided down and applied as a strobe pulse to the Phase Gate Detector. This strobe pulse contains energy at frequencies equally spaced throughout the spectrum. One of these frequencies will be within 2.5 MHz of the 1st LO frequency at the other input to the Phase Gate Detector. The Phase Gate Detector outputs an error signal proportional to the difference between the nearest strobe and the 1st LO frequency. This error signal is amplified and filtered by the Error Amplifier and applied to the FM coil of the 1st LO to pull it into frequency and phase lock with the strobe.

The Harmonic Mixer mixes the 1st LO frequency and a harmonic of a synthesized 200-220 MHz signal from the Auxiliary Synthesizer. The exact frequency of the synthesizer signal is a function of the +N factor from the processor. The Harmonic Mixer output is a signal within the 10 to 80 MHz range. This signal is divided in the Auxiliary Synthesizer and sent to the Counter. The microcomputer looks at the resultant count and decides which way to move the 1st LO to bring it to the correct frequency.

Phase Lock Assembly

As previously stated, the phase lock system consists of two frequency servo loops, called the outer loop and inner loop. In the inner loop operation, the 100 MHz reference signal from the 3rd Converter, is divided down to 25 MHz, on the Synthesizer board, and applied as the reference signal to the mixer on the Offset Mixer board. The 25 MHz signal is also applied as a clock signal to +N counter circuits, on the Synthesizer board, which output a frequency (depending on the +N number from the processor) between 32 kHz and 94kHz. This signal is applied to the phase/ frequency detector on the Offset Mixer board, where it is compared to the IF output (difference between the 25 MHz reference and the output from the VCO (voltage controlled oscillator) and any difference is output as an error voltage to the Error Amplifier.

The VCO operates between 25.032 MHz and 25.094 MHz, depending on the drive from the Error Amplifier. This signal is applied to the RF input of the mixer on the Offset Mixer board, where it mixes with the 25 MHz reference frequency. The difference frequency, which is between 32 kHz and 94 kHz, is applied to the phase/frequency detector and compared to the +N frequency. If the two signals are edge and frequency coincident, phase lock occurs. If they do not coincide, an error signal is generated, passed through the Error Amplifier, and applied to the VCO to shift the oscillator frequency until it is phase locked. This evolution typically lasts for only a few milliseconds, so the inner loop phase lock is, for all practical purposes, instantaneous.

The outer loop, which includes the inner loop circuits (Offset Mixer, Error Amplifier, and VCO) consists of the Strobe Driver, Phase Gate, Error Amplifier, and 1st LO. (The Harmonic Mixer, Auxiliary Synthesizer, and Counter, are a part of the operation, but are not considered a part of the loop.)

The signal between 25.032 MHz and 25.094 MHz from the VCO is applied to the Strobe Driver where it is divided by five, filtered, and sent to the Phase Gate Detector as a strobe signal between 5.006 MHz and 5.019 MHz. This strobe generates line spectra that are equally spaced approximately 5 MHz over the spectrum. At about the 400th line, which corresponds to 2 GHz, assuming that the 1st LO is tuned to a frequency near 2 GHz, one of these lines (at about the 400th line) will be within 2.5 MHz of the 1st LO frequency. The Phase Gate Detector will then output an error signal that is proportional to the difference between the 1st LO frequency and that of the nearest strobe line, if that difference frequency is less than approximately 1MHz.

For phase-lock acquisition, the microcomputer calculates the strobe frequency required for the desired 1st LO frequency. The strobe is set to this frequency and the 1st LO is set to the required harmonic of the strobe. The outer loop is closed, and the microcom-

puter tunes the 1st LO frequency through the following sequence; up 750 kHz, down 1.5 MHz, up 1.5 MHz, and down 750 kHz. During one of these "firmware searches" the 1st LO frequency passes through the strobe harmonic frequency and the loop acquires lock.

Any frequency difference between the strobe signal and the 1st LO will generate a low frequency correction voltage. This correction voltage is filtered by the F(s) amplifier, then used to drive the oscillator FM coil to pull the oscillator frequency back to the strobe position. If the 1st LO drifts beyond the error voltage range of the F(s) amplifier, comparators on the Error Amplifier board, that monitor the error voltage, will interrupt the microcomputer and indicate the direction of drift. The microcomputer then tunes the Center Frequency Control circuits to null out any FM coil current in the phase lock loop.

Frequency Control

The 21-bit counter and its associated control circuitry, on the Counter board, plus the Harmonic Mixer and Auxiliary Synthesizer, form the frequency control hardware nucleus for the spectrum analyzer. A firmware-based control loop, that uses data from the counter as feedback on the oscillator frequency, controls both the 1st LO and the 2nd LO frequencies. The 10MHz IF is also counted by the Counter to determine the input signal frequency to the analyzer.

A mix down counting scheme is used to count the 1st LO frequency, which varies between 2 GHz and 6 GHz. The 200-220 MHz output from the Auxiliary Synthesizer is positioned so one of the signal harmonics is approximately 45 MHz above the 1st LO frequency. This output drives the LO input to the Harmonic Mixer, the 1st LO drives the RF input. One of the IF outputs from the Harmonic Mixer is within the 10 to 80 MHz range (approximately 45 MHz). This IF signal is passed through a 10-80 MHz band-pass filter, divided by 100, then counted by the Counter. Since the Processor knows the Synthesizer frequency, the 1st LO frequency can be calculated if the Processor knows which harmonic of the Synthesizer frequency was used to generate the IF frequency being counted. The harmonic of the Synthesizer frequency is calculated from the 1st LO tuning DAC (digital-to-analog converter) code, since it indicates the 1st LO frequency to within approximately +/-10 MHz.

Counting the 2nd LO frequency is much simpler. The controllable 16-20 MHz VCO in the 2nd LO assembly determines the frequency of the 2nd LO; therefore, the 2nd LO frequency is calculated by directly counting the 16-20 MHz signal. The 2nd LO frequency is then calculated from this frequency.

Controlling the Oscillator Frequency. The frequency control loop is only closed between sweeps. After the completion of each sweep, the processor switches the span/div to zero and then counts the 1st LO and the 2nd LO frequencies. If they are not at the frequency required to generate the displayed center frequency, they are set to the correct frequency by repeating the process (i.e., the DACs are changed to tune the LO, the LO is counted, etc.).

In the single sweep mode, the oscillator frequencies are corrected after each single-sweep actuation, and before the sweep starts. In the manual sweep mode, or other non-recurring sweeps, the oscillators are corrected at periodic intervals.

Counting the IF. In addition to counting the frequency of the 1st and 2nd LO, the 10 MHz IF is counted when the Counter mode is actuated; thus, the incoming signal frequency can be calculated from the frequency conversion equation for the analyzer. The 1st LO is actually phase locked before the 2nd LO and IF are counted, in order to reduce FMing in the IF signal. This allows very accurate signal counting, even in wide spans.

HARMONIC MIXER (Diagram 36)

The Harmonic Mixer combines a portion of the 2-6 GHz 1st LO signal with harmonics of the 200-220 MHz reference signal from the Auxiliary Synthesizer to provide an output signal in the 10-80 MHz range. This signal is amplified and returned to the Auxiliary Synthesizer where it is counted to get an exact computation of the oscillator frequency. The Harmonic Mixer consists of a directional coupler, an input amplifier, the mixer, and an output amplifier, all on a hybrid alumina circuit. Figure 7-27 is a functional block diagram of the Harmonic Mixer.

Input signal level, from the 1st LO to directional coupler A25A1, is a about +10 dBm. The coupling ratio is 10 dB, therefore, the coupler will deliver about 1 mW (0 dBm) to the RF input of the harmonic mixer. The through-port contributes about 0.5 dB of loss for the 2-6 GHz signal.

The 200-220 MHz reference signal, at a level of about 10 mW from the Auxiliary Synthesizer, is amplified to a level of about 100 mW (+20 dBm) by a differential amplifier Q1 and Q2. Resistor R27 couples the emitters together and the current is set by R13 and R14. Output is transformer coupled to the input of the mixer. Input signal level to the amplifier is +7 dBm minimum.

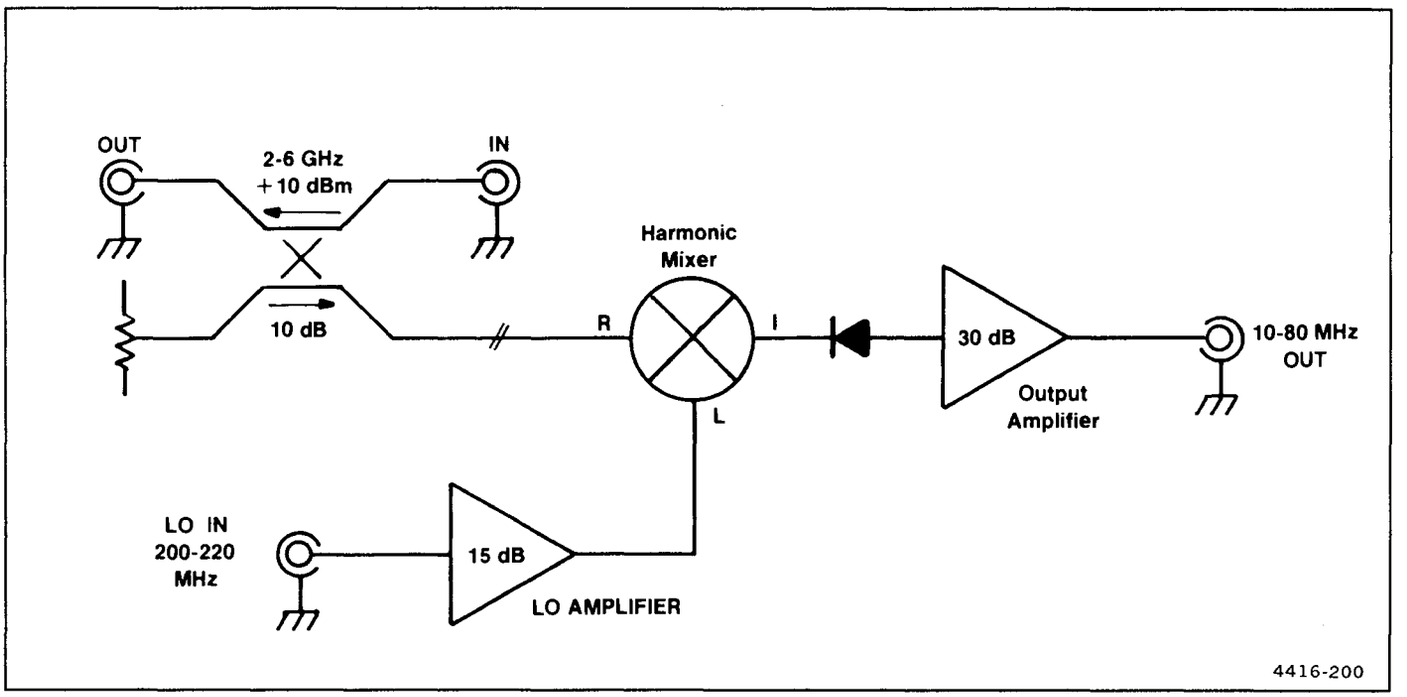


Figure 7-27. Simplified schematic of harmonic mixer.

Two additional directional couplers are used to couple the 2-6GHz signal into the mixer circuit. A power splitter (R1, R2, R3) splits the signal into two paths. Each signal (approximately –6 dBm each) is then coupled through these couplers to the mixer. The through ports are terminated in 50 ohms. Thus the 2-6 GHz signal is coupled into the mixer differentially at a power level of about –16 dBm.

The 200-220 MHz reference signal is also coupled differentially into the mixer circuit, since the output of transformer T1 is applied across the two terminating resistors R4 and R5. The level of this signal is high enough to drive the snap-off diode into its operational region. Harmonics of this 200-220 MHz signal mix with the 2-6 GHz signal to generate numerous IF products which are detected by diodes CR2 and CR3 and fed to the output amplifier.

The output amplifier is a two stage common-emitter cascade amplifier with dc coupling between stages. The standing current through the second stage (Q4) is higher than in the first stage (Q3) to provide better power and intermodulation performance. The amplifier is designed for a 10 to 80 MHz response. Signals above 80 MHz are rejected by a low-pass filter in the Auxiliary Synthesizer. Output level of signals in the 10-80 MHz range is typically -20 dBm for input signal levels as described.

AUXILIARY SYNTHESIZER (Diagram 37)

The Auxiliary Synthesizer is part of the spectrum analyzer's Direct Frequency Readout (DFR) system. This, along with a harmonic mixer, counter circuits, supporting filters and amplifiers, and appropriate firmware, make up the DFR. The DFR provides the means for measuring and determining the frequency of all oscillators and the center of the IF, so the center screen frequency is always known. Since the IF signal can be counted, this allows direct frequency measurement of any signal applied to the input port of the spectrum analyzer.

A functional block diagram of a simple or basic synthesizer is shown in Figure 7-28. The VCO frequency is divided by "N" in a programmable down-counter which outputs a pulse every Nth input pulse. This frequency along with a frequency reference is then fed to a phase/frequency detector. The difference between the two signals is filtered and fed back as a control voltage to the VCO to phase lock the oscillator to the reference. VCO frequency is related to the reference by, $F_{ref} = NF_{ref}$. As N is changed, the VCO frequency will change by F_{ref} for each step in N. This produces outputs separated by F_{ref}. To get closely spaced channels, in tuning the VCO, the reference frequency must be relatively low.

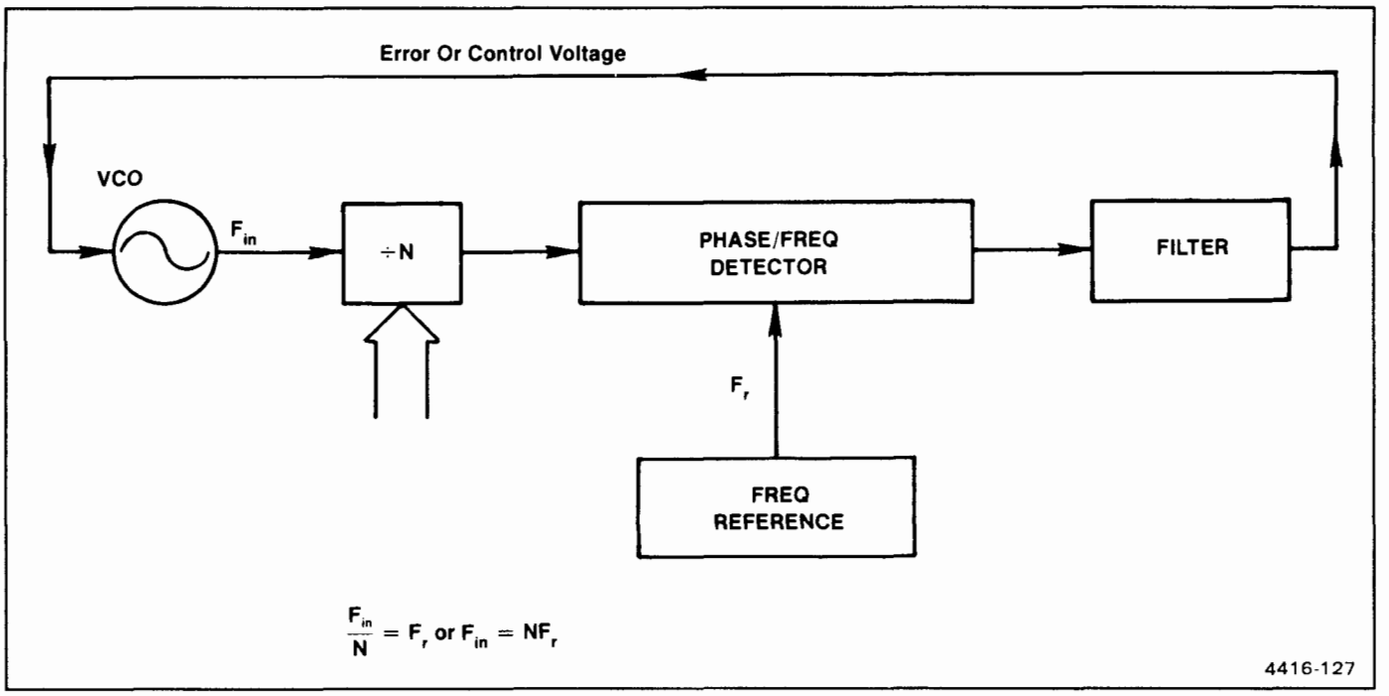


Figure 7-28. Block diagram of a basic synthesizer.

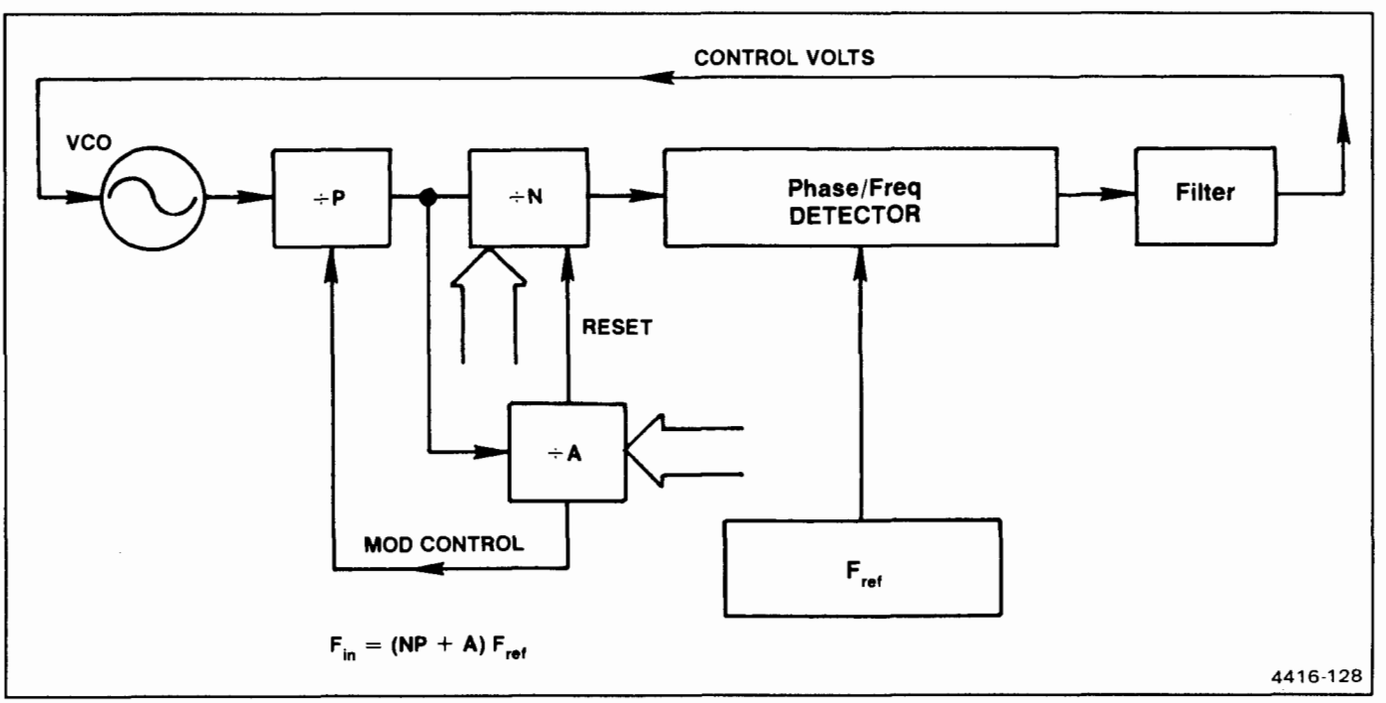


Figure 7-29. Basic block diagram of a ÷N synthesizer with a variable modulus prescaler.

This synthesizer uses a variable modulus prescaler to divide the VCO frequency before is processed by the "+N" counter, such as shown in Figure 7-29. The variable modulus prescaler is controlled by a modulus control input. When the line is high the prescaler is a divide by P+1 and when the line is low the division changes to P. A common type of prescaler is a ÷10/11. A cycle of system operation starts with all programmable counters loaded and ready to count. The variable modulus prescaler initially divides by P+1.

Two programmable dividers are used with this system, both triggered by the prescaler output. One is a +N, with N being a relatively large number, the other is a "+A", where A is a small number. One possible state includes A = 0.

The operation of this system is as follows. The lower case letters represent variables, the upper case letters represent the programmed values. At the beginning of the cycle, p=P+1, a=A, and n=N. After P+1 pulses from the VCO, one pulse is applied to the "a" and "n" counters and "a" and "n" decrease by 1 (a = A-1, n = N-1). This continues until a = 0 at which time the modulus control line changes state and p = P while n = N-A. The counting continues until n = 0. Both the "n" and "a" counters now return to the programmed condition. The total number of pulses applied from the VCO is:

$$N_{total} = (P+1)A + P(N-A) = A + PN$$

Both N and A are programmable such that $F_{vco} = (A + PN)F_{ref}$. This leads to a possible channel spacing of F_{ref}, obtained by changing A by 1.

A functional block diagram of the Auxiliary Synthesizer is shown adjacent to the schematic in the diagrams section. The VCO (Q2071) is configured in a Colpitts oscillator circuit with the inductance as a three turn air core coil with feedback provided by C2072 and C2071. Coarse tuning is accomplished with C1070, while the voltage control of the frequency comes from the varactor diode, CR2068. This diode provides a frequency shift of over 30 MHz from a voltage swing of +5 V to +11 V, which is ample overlap for the 20 MHz tuning range. The output power of the oscillator is 0 dBm into 50Ω. The oscillator is biased so it can be turned off and on rapidly.

The VCO is turned off by turning Q2076 on. In operation, the synthesizer is turned off during periods when information is presented on the CRT. Synthesis and counting is done during retrace time to prevent possible interference on the display from any radiated energy from the synthesizer.

The VCO output is split by a resistive power divider. One output drives transistor U2058, which provides +7 dBm of signal output to the Harmonic Mixer. This device is biased to a 20 mA collector current by transistor Q2055.

The other VCO output drives a low gain amplifier, Q2049, which is biased by transistor Q2051. Negative feedback, in the form of emitter degeneration and shunt current feedback, sets and stabilizes the gain to ensure stability with regards to spurious oscillations. The output of Q2049, to drive the variable modulus prescaler is 0 dBm. The variable modulus prescaler U3051, is a +32/33 IC that features an ECL input with a TTL or CMOS compatible output.

The major circuit of the synthesizer is U4041, a large-scale-integration, CMOS device for frequency synthesis applications with a variable modulus prescaler. The device contains three programmable counters; a +N, a modulus control counter +A, and a reference divider which divides an input from a crystal controlled source or other reference frequency down to a desired frequency. This device has a speed comparable to TTL. It also contains a phase-frequency detector which drives an external loop filter that uses an operational amplifier. U4041 will accept data for N, A, and R inputs from a 4-bit data bus while a 3-bit address bus selects the information to be loaded. Data contained on instrument bus lines DB4 to DB7 is loaded when the enable line goes high. Address information is contained on instrument bus lines DB0, DB1, and DB2. The appropriate 32 latches are also contained within this IC.

The output from the phase/frequency detector in U4041 is a chain of pulse signals at the reference frequency. The pulses contain both ac and dc components. The ac part of the signal causes reference sidebands to appear on the VCO output. These sidebands are suppressed by two active loop filters consisting of U2040A and U2040B. The detector outputs, ϕ_R and ϕ_V, which are similar but with reversed polarity, apply differentially to the input of U2040A. Slight differences in pulse width between the two outputs generate a dc voltage. This is further filtered by an active low-pass filter, U2040B, to suppress frequencies above 20 kHz. Then it is applied to the varactor diode CR2068 in the 200-220 MHz VCO.

U2040A is an integrator with a series resistor added to the feedback capacitor. This controls the slope of the loop gain at gain crossover. To provide additional suppression of the reference sidebands, an RC active two pole filter, U2040B, is added. Cutoff frequency is about 20 kHz. The loop filter (U2040A) and the VCO provide the dominant poles that determine the system response. A damping factor near unity provides the stability. Additional filtering in the form of passive components, with a high frequency cutoff, are added between the output of U2038B and the varactor diode

CR2068. CR1065 provides a clamp to prevent a control line voltage less than 5 V. Capacitor C1070 sets the low end of the control voltage to about 6 V. Range of the control voltage, over the 200-220 MHz VCO range, is about +6 V to +11 V.

The off/on status of the VCO is controlled by U4074 which is activated by D3 from the data bus. The value is latched in U4074 and its output turns Q2076 off or on. The output also controls the sensitivity of divider U5015. During the period when the VCO is off and there is no input signal, the divider sensitivity is lowered so stray signals will not activate the divider. This is done by turning Q5027 on and pulling input pin 6 of U5015 low.

The 100 MHz signal from the 3rd Converter is applied through a resistive power splitter to divider U2017 and to buffer amplifier Q1015. The 1 MHz output from the divider, U2017, is further divided by 5 within the synthesizer IC, to become the 200 kHz reference frequency for the synthesizer. The amplifier Q1015 has negative feedback for gain stabilization. Its output signal is applied to the counter board.

The 10-80 MHz signal from the harmonic mixer is passed through a 7-pole low-pass filter with 80 MHz cutoff. The signal is then amplified by U4021 with a broad band gain of about 24 dB.

COUNTER BOARD (Diagram 38)

The Counter board circuits and function are: 1) The address decoder which receives and decodes the talk and listen commands for the microcomputer. 2) The service request circuits that sense an impending loss of 1st LO phase lock and sends a service request to the microcomputer. It then cancels the request when directed by the microcomputer. 3) The data buffers transmit data to and from the microcomputer. 4) The input amplifiers and multiplexer amplify input signals up to TTL levels and then select which of the input signals is to be counted. 5) The $+2^n$ counter divides the selected input signal by some power of 2 as determined by the microcomputer. 6) The 21-bit counter counts at a 100 MHz rate for a given number of cycles of the selected input signal.

Address Decoder

The addresses from the microcomputer are decoded by address decoder U2040. The counter circuits have both a talk address, where the counter-buffer circuits are instructed to talk on the data bus, and a listen address, where U3024 is directed to receive data from the data bus. The talk address is F3; the listen address is 73.

Service Request Circuits

The service request circuits consist of multiplexer U3040, latch U3048B, and associated circuitry. This circuitry alerts the microcomputer in the event that the 1st LO has drifted too far. The UP and DOWN signals from the window comparator (located on the Error Amplifier board) drive NOR gate U3010C. Both signals are also sent to U3034, where their status can be read by the microcomputer. When one of these signals is high, it indicates that the Error Amplifier is approaching its operating limits and the microcomputer should adjust the 1st LO frequency so the Error Amplifier returns to the center of its range. A high at either input of U3010C produces a negative transition that is inverted by U3046C. C2050 pulls the set input of U3048B high for approximately 10 micros. The Q output of U3048B then goes high, causing Q4052 to pull the SR (service request) line low.

The Q-not output of U3048B pulls the G_1 and G_2 inputs of multiplexer U3040 low, enabling both sides. This device allows Q4034 and U3048B to respond to inquiries by the microcomputer to determine which address requested service. The microcomputer initiates the polling routine, which is to pull the POLL signal and AB7 high, then interrogate each data bus line in succession to determine which address requested service; i.e., which data line is low. To do this, the Y1 output of U3040 is set high, which causes Q4034 to pull the D2 line low. To affirm which address requested service, the microcomputer now causes the 7 address line to move low, which, via the Y2 line from U3040, clocks U3048B to the reset state as the microcomputer holds data bus line 2 low. This cancels the service request because it cuts off Q4052 permits its output to move high. In addition, the complement output of U3048B moves high, which disables the inputs to U3040. This brings the service request circuitry back to its original state.

Data Buffers

The data buffers consist of U3024, U3034, U3030, and U2026. U3024 is the listen buffer. When address decoder U2040 is addressed by the microcomputer to listen, it enables U3024, which passes on the buffered data to the other circuits in the Counter board. The function of each data bit is as follows:

D0—This line carries the serial data that selects which input signal is to be counted and what n numbers to use in the $+2^n$ counter. This data is loaded into shift register U1022. D0 also carries the data for the +N counter in the Phase Lock Synthesizer circuits.

D1—The N LATCH signal for the 1st LO phase lock is sent on this line.

D2—Reserved for future applications.

D3—This line resets the buffer sequencer at the outset of a talk cycle for the counters.

D4—This line (CONTROL LATCH) latches a control word into the output buffers of U2025 on the Error Amplifier board.

D5—This signal clears all the counter stages in the counter- buffer circuits in preparation for a count sequence.

D6—This line latches the N data in U1022.

D7—This line is used as a clock to step data into U1022 and U3048A, and for the data sent in the 1st LO phase lock. R3012 and C2010 act as a delay to provide adequate setup time for the data prior to the clock signal arriving.

Buffers U3034, U3030, and U2026 are the talk buffers that send data to the microcomputer. U3018 and U2030A make up a step-enabler that enables the talk buffers one at a time when requested by the microcomputer.

Input Amplifiers and Multiplexer

Q1018 brings the -5 dBm, 16 MHz to 20 MHz signal from the 2nd LO up to TTL levels. U2010 divides the 16-20 MHz by 32 and 256 before it sends it to multiplexer U1018. U2056 amplifies the -50 dBm, 10 MHz IF. L2056 and C2056 act as a 10 MHz bandpass filter on the input of U2056. R3056 provides current to the open collector output of U2056. C3052 couples the 10 MHz signal into U4056. U4056 acts as a divide-by-128 counter. The signal then goes to U1018.

All other input signals are at TTL levels and are connected directly to U1018. The ouput of U3010A is connected to U1018 so that the clock can be counted for diagnostic purposes. U1018 selects one of its inputs according to the data in U1022.

$\div 2^n$ Counter

The output of U1018 goes into a series of dividers made up of U1050 and U2050A. Various outputs of these dividers are connected to multiplexer U1046 to give a $+2^n$ counter where n = 1, 2, 4, 6, 8, 10, 11, or 12 (n is selected by the data stored in U1022). A strobe input to U1046 disables the multiplexer when pulled high.

21-Bit Counter

The 21-bit counter counts the 100 MHz reference frequency to give a measurement of the time required to complete a given number of cycles of the selected input signal. The counter itself consists of U1038, U2018, U1028, and U2034. U1038 is an ECL divider. Q1034 and Q1044 are ECL-to-TTL translators for the +2 and +4, respectively. The +4 goes to U2018 where it is counted with TTL dividers, and the divider chain continues through U2034. The output of each stage goes to an output buffer so the microcomputer can read the final number of counts. Therefore, measure the time period during which the counter was enabled. The counter is enabled by U2050B and U2046 for a time period equal to eight cycles of the output of the $+2^n$ counter.

At the start of a count, the microcomputer selects the input signal to be counted and selects the n number for the $+2^n$ counter. The COUNT/RESET line is then pulled high to reset all of the counters. U2046A is preset with Q in the high state, which disables the 21-bit counter. The COUNT/RESET line then goes high to start the measurement process. The output of U1046 goes to U2050B where it is further divided down. On the first rising edge at QA of U2050B, Q of U2046A goes low to start the 21-bit counter. On the eighth count of U2050B, U2046A steps back to its original state, which stops the 21-bit counter. At the same time, U2046B pulls the strobe to the $+2^n$ counter high to stop any further counts in U2050B. The microcomputer can now read the VALID COUNT line to determine when the count process is completed, and then read the data that is stored in the 21-bit counter.

PHASE LOCK SYNTHESIZER (Diagrams 39 and 40)

The Phase Lock Synthesizer provides frequency control and stability for the 1st local oscillator. The circuit consists of the Synthesizer and Phase Lock circuits. The Phase Lock assembly includes the Error Amplifier, Offset Mixer, Controlled Oscillator, and Strobe Driver. The Phase Gate Detector (shown on diagam 36) is also part of the phase lock ciruitry.

Synthesizer (Diagram 39)

The Synthesizer uses the 100 MHz reference frequency from the 3rd Converter to generate the 25 MHz reference frequency for the Offset Mixer and the +N frequency (determined by the N number from the Processor) for the phase/frequency detector in the Offset Mixer. The +N number is within the 32 kHz to 94kHz range.

The Synthesizer can be divided into three functional blocks: the 100 MHz divider, the 50 MHz divider, and the +N counter.

The 100 MHz divider consists of flip-flop U3030 and differential pair Q3040 and Q3041. The 100 MHz signal from the 3rd Converter stage is applied to the clock input of U3030. (One-half of U3030 is used to furnish a stable bias source for the clock input.) The 50 MHz signal from the Q output is applied through buffer amplifier Q3041 to P500; it is not used. The signal from the complement output of U3030 is applied through Q3040 to U1040B, the 50 MHz divider.

The 50 MHz divider consists of the flip-flop U1040B. The 50MHz from the collector of Q3040 is applied to the clock input of U1040B which divides the signal to 25 MHz. The signal from the Q output is sent to the Offset Mixer circuits. The complement signal is applied to the +N counter.

The +N counter consists of two shift register/latches U2020 and U2030; three counters, U2010, U1020, and U1030; and flip-flop U1040A. The circuit is controlled by three signals from the microcomputer via the Counter board. The output of the +N counter is a frequency within the range of 32 kHz to 94kHz which is applied to the phase/frequency detector in the Offset Mixer. When power is first applied, and before phase lock is selected, this counter typically outputs a frequency of approximately 6 kHz.

When phase lock operation is selected, the microcomputer sends data and a data clock to load a number into the latches, which accept and store serial data. The numbers that come from the microcomputer, range from about 3300 to 3830, so the count remaining, until the counters overflow, is from about 265 to 795. When the number is loaded, the N LATCH signal transfers the number from the input shift registers to the output registers of U2020 and U2030 where they are available to the counter stages. This presets the counters to a predetermined value, as just mentioned. Once loaded, the counters count at a 25 MHz rate to accumulate the remaining number of digits until they are full. The TC output of U1030 then moves high and U1040A changes state. This presets the N number in the counter stages for another count cycle. The TC output of U1030 is again simultaneously set low so the next cycle of the 25 MHz clocks U1040A back to the reset condition. The resultant output of U1040A is a series of positive pulses that range in period from 10 μs to 31 μs which is equivalent to 94 kHz to 32 kHz. This signal is sent to the phase/frequency detector in the Offset Mixer for comparison with the difference frequency generated in the mixer circuit.

Phase Lock (Diagram 40)

The Phase Lock circuits lock the 1st LO, using the Synthesizer as a reference. The circuits shown on diagram 40 include the Offset Mixer (A50A3, Error Amplifier (A50A4), Controlled Oscillator (A50A5), and Strobe Driver (A50A2). The 1st LO (A16) and the Phase Gate Detector (A24) are also major parts of the phase lock circuitry.

Offset Mixer. The Offset Mixer (A50A3) circuits mix the synthesizer and VCO outputs and compare phase and frequency with the divide-by-N frequency from the synthesizer. The resulting error signal drives the inner loop amplifier on the Error Amplifier board (A50A4).

The circuits consist of a ring diode mixer, differential amplifier, and phase/frequency detector. For this explanation, assume that the Controlled Oscillator (VCO) frequency is at 25.06 MHz and the +N signal is 50 kHz. The 25.06 MHz signal from the VCO enters the board at pin N of the Offset Mixer assembly. The signal drives the base of transistor Q2021 which drives transformer T2010. The transformer output connects across the ring diode mixer. The 25 MHz reference frequency is applied at pin K of the Offset Mixer and coupled through T1010 to the ring diode mixer. The four frequency components are picked off at the center tap of T2010. A low-pass filter passes the 60 kHz difference frequency and blocks the two fundamental frequencies and their sum.

Transformer T2030 couples the 60 kHz signal to differential pair Q1020 and Q1030. Then Q1040 amplifies the signal to TTL levels and applies it to the clock input of flip-flop U1050B, part of the phase/frequency detector.

The phase/frequency detector consists of flip-flops U1050A and U1050B, NAND gate U2050B, and inverter U2050A. Now, if the loop had been locked, the two flip-flop clock input signals would have been edge-coincident. Pin 4 and 5 inputs of U2050B would have moved high and after the signal at TP1058 goes low, the NAND gate would have reset both flip-flops. This results in a series of pulses of equal amplitude and width from each of the flip-flops which, when applied to the Error Amplifier, would not shift the frequency of the VCO.

However, in this example the +N signal is 50 kHz and the difference frequency from Q1040 is 60 kHz. Thus, Q1040's output leads the +N signal. In this case, U1050B will clock first, placing a high at the Error Amplifier's inverting input. This ramps the amplifier output low until U1050A switches a short time later. U2050B resets both flip-flops and the inner loop error amplifier will stop ramping until the next correction

cycle. At the next correction cycle, the error amplifier will have reduced the VCO frequency, therefore reducing the mixer difference frequency. This process continues until the two signals applied to the Phase/Frequency Detector are edge coincident, meaning that their frequencies and phase match.

Error Amplifier. The Error Amplifier board (A50A4) provides the inner and outer loop error amplifiers, enables the Strobe Driver (A50A2), and generates the UP/DOWN and F ERROR signals.

The inner loop amplifier integrates the error signals from the Offset Mixer and produces a correction voltage to pull the VCO to a frequency that is synchronous with the +N signal. The Output Mixer (A50A3) phase/frequency detector output drives integrating differential amplifier U3075. As the signals driving the amplifier continue toward one direction, the output continues to change the oscillator frequency in the appropriate direction. Zener diode VR2065 and CR3069 clamp the inner loop amplifier output so that it stays above +5 V. This prevents forward biasing the VCO varactor diodes.

The digital control circuits consist of shift register U2025 and quad analog switch U2037. Data from the microcomputer is fed serially, via the Counter board circuits, into the shift register, then transferred to the output lines by the CONTROL LATCH signal. Table 7-21 lists the purpose of the output lines.

Table 7-21
U2025 OUTPUT LINES

Line	High	Low
Q1	Window disabled[a]	Wide window[a]
Q2	Lock	Unlock
Q3	Wide loop	Narrow loop
Q4	Strobe enabled	Strobe disabled
Q5	Narrow window	Wide window[b]

[a]With Q5 low.
[b]With Q1 low.

The outer loop amplifier circuit consists of amplifier U2048 and surrounding components. The ERROR signal from the Phase Gate Detector and Error Amplifier is applied through LOOP GAIN adjustment R3082 to the inverting input of U2048. The signal (ERROR) is a result of the comparison of the 1st Local Oscillator frequency and the nearest multiple of the STROBE signal from the Strobe Driver circuit. The ERROR signal varies from zero to about 500 kHz, and is up to 4 V peak-to-peak in amplitude.

When phase lock is not required, data into U2025 sets output Q2 and Q4 low and Q3 high. This opens the connection between pins 11 and 10 of U2037 and the connection between pins 2 and 3. STROBE ENABLE line to the Strobe Driver goes high and disables the strobe pulse. The FM coil of the oscillator is opened by U2037 which opens the outer loop.

To establish phase lock, the microprocessor sets the 1st LO near the desired lock point and loads the proper N number into the synthesizer. The 5 MHz strobe is then turned on (Q4 and Q2 output of U2025 set high) and the microprocessor tunes the 1st LO up or down 750 kHz either side of the desired lock point at a 10 Hz rate. When the oscillator frequency crosses the desired lock point, the ERROR frequency is reduced to a dc voltage which results in U2048 pulling the 1st LO in the direction required to maintain a constant frequency. When the microprocessor measures the 1st LO frequency and finds it held constant, at the desired frequency, it then sets Q3 output of U2025 low to reduce the bandwidth of the phase lock loop.

The UP and DOWN signals alert the microcomputer that the drive current to the 1st LO FM coil is reaching its limit in holding the 1st LO in phase lock. The microcomputer then acts to bring the 1st LO frequency within the proper range. A window comparator, consisting of U1015 and the associated components, senses when U2048 has approached its operating limits. When the microcomputer causes the Q2 signal to close the path from U2048 to the FM coil, U2048 begins to furnish current to the coil which causes the 1st LO to track the stable strobe signal. That is, each time the 1st LO frequency drifts, the ERROR signal changes and U2048 shifts the FM coil current to bring the 1st LO back to its original frequency. At the same time, the microcomputer causes lines Q1 and Q5 to be low, closing the contacts that connect the output of U2048 to the input of the window comparator through a divider network. Now, as the 1st LO frequency drifts, the loop amplifier will compensate for the drift. If the drift is excessive, however, U2048 will approach its limits and will be unable to furnish any more current to the FM coil.

Window comparator U1015 is a dual comparator that senses a deviation of ±15 mV. For example, if a frequency shift forces U2048 to move positive enough (approximately 3 V), the upper half of the comparator conducts, and the UP line goes high. This triggers the service request circuits on the Counter board, which in turn alerts the microcomputer so it begins adjusting the TUNE voltage from the Center Frequency Control circuits to reduce U2048 output to zero. If the output drifts negative, the other half of U1015 conducts, causing reverse action to occur.

Normally, the input signal to the window comparator is attenuated by R2043, which reduces the voltage applied to U1015 to 0.3% of the output from U2048.

This allows U2048 to drift up and down without immediately triggering either comparator. When R2043 is in the circuit, it is called "wide window" operation. When phase lock is de-selected, the microcomputer selects narrow window (which bypasses R2043). The Center Frequency Control circuit is then instructed by the microcomputer to move the 1st LO frequency until the window comparator indicates that the FM coil current is near zero. This prevents the 1st LO frequency from shifting too far from the lock point when phase lock is canceled.

The F ERROR signal is used by the Counter board (A51) for diagnostics so that the microcomputer can determine the relationship between 1st LO frequency and the strobe line. The F ERROR signal is generated from the outer loop ERROR signal from the Phase Gate Detector (A24). The circuit consists of an active low-pass filter U2065 and Schmitt trigger U1035. This circuit filters and squares the incoming ERROR signal. The ERROR signal is applied through C2067 to an RC 500 kHz low-pass filter and amplifier U2065. After filtering, the signal is applied through Error Count Breakpoint adjustment R1061 to the input of U1035, a Schmitt trigger circuit. The squared output signal is then applied to circuits on the Counter board.

The STROBE ENABLE signal enables the strobe generator in the Strobe Driver circuit (A50A2). Shift register U2025 reads the instrument bus latch on the Counter board (A51) to determine the status of the STROBE ENABLE signal. Q2030 inverts the signal and converts it to TTL level to drive the strobe generator.

Controlled Oscillator (VCO). The Controlled Oscillator (VCO) is a voltage-controlled crystal oscillator whose frequency is controlled by the output of the Error Amplifier. The oscillator generates a reference signal that is used to stabilize the 1st LO frequency. Refer to the block diagram adjacent to Diagram 40 for a functional description of this part.

The control voltage from the Error Amplifier, which is a function of the difference between the microcomputer controlled ÷N signal and the Offset Mixer difference frequency, is applied to the VCO on the Controlled Oscillator board to regulate its frequency of operation. The circuit has two outputs: the first, which is part of the inner loop of the phase lock circuits, is fed to the Offset Mixer, where it is used to derive the difference frequency that is compared against the ÷N signal. The second output, which is part of the outer loop, is fed to the Strobe Driver circuits, where it is divided down to become the STROBE signal that is compared against the 1st LO signal in the Phase Gate.

The VCO consists of five major circuits, four of which are connected in a positive feedback loop to sustain oscillation. These circuits are the resonator stage, the differential amplifier, the bandpass filter, the isolation amplifier, and the output amplifier. The resonator stage operates at a frequency of 25.032 MHz to 25.094 MHz. The output signal from the resonator is applied to the input of a differential amplifier which drives the output amplifier and the bandpass filter. The output from the output amplifier is fed to the Offset Mixer and the Strobe Driver. The bandpass filter strips the signal of any spurii either side of center frequency and feeds the signal to the isolation amplifier. This stage furnishes the positive feedback drive to the resonator stage and isolates the bandpass filter from the resonator stage.

The resonator stage consists of crystal Y1012, varactor diodes CR1011 and CR1012, and related components. The stage operates within the frequency range of 25.032 MHz to 25.094 MHz, which is controlled by the voltage applied to varactor diodes CR1011 and CR1012. Feedback energy for sustaining oscillations comes from the isolation amplifier by way of coil L1025.

The resonator output signal is applied to a differential amplifier Q2033 and Q2041. The Q2033 side drives the output amplifier and serves to isolate the output load from the feedback loop. Gain from this side is less than one. The signal is fed from the collector of Q2041, following amplification, to the band-pass filter.

The band-pass filter consists of passive components, and is used to strip the signal of any frequency components more than about 40 kHz away from the center operating frequency, which is approximately 25.06 MHz. Capacitors C1041 and C1042 are adjusted at the factory to set the bandwidth and center the frequency of the filter.

The isolation amplifier, Q1028, is a common-base configuration, in order to match the impedance of the filter to the resonator. Output current from the stage furnishes positive feedback for the resonator.

The output amplifier, consisting of transistors Q2025 and Q2026, is connected as a differential amplifier with Q2026 driving one side of the Offset Mixer and Q2025 driving the input of the Strobe Driver circuit, for eventual application to the Phase Gate circuits.

Strobe Driver Circuit. The Strobe Driver circuit consists of counter U1022, bandpass filter FL2064, source follower Q2091, and AND gates U1091A and U1091B.

The VCO output is applied to the clock input of divide-by-5 counter U1022. The STROBE ENABLE line from the Error Amplifier permits the counter to operate

when the line is low and is the means by which the microcomputer can turn the strobe pulses on or off. The counter output couples through an impedance matching network consisting of C2030, L1031, C2033, and C1032, to the input of bandpass filter FL2064. The impedance matching circuit raises the line impedance to about 8200 ohms. The output of the filter drives another impedance matching network for the gate input of Q2091. The output of Q2091 drives two buffer amplifiers U1091A and U1091B. U1091B drives the Phase Gate circuitry, and U1091A is reserved for future applications. Capacitors C1032 and C2105 are selected to provide maximum signal amplitude at TP2087.

DIGITAL CONTROL (Diagram 9)

The Digital Control section provides operator and digital controller interfaces. It translates changes in front-panel controls and for the 2754P, also translates instructions received via the GPIB into codes that control the instrument.

The user interface to the digital control operating program is discussed in the Operators and Programmers manuals. This description focuses on the major circuits that make up the Digital Control section. Those circuits are:

Microcomputer

Addressable registers on the instrument bus

Front panel

Accessories interface

GPIB interface (2754P only)

Microcomputer

The Microcomputer system receives inputs from the front-panel controls, the instrument circuits, and the GPIB (2754P only), and sends control codes to the instrument hardware to set it for desired operation. The Microcomputer consists of a microprocessor, memory, various input/output (I/O) circuits, and associated bus structures. The circuits are located on the Processor (A58), Memory (A54), and GPIB (A56) assemblies.

The microcomputer is centered around a microprocessor. Input/output (I/O) is provided by a Timer, a Peripheral Interface Adapter (PIA), and for the 2754P a Direct Memory Access (DMA) controller and a General Purpose Interface Adapter (GPIA). System memory includes both read-only-memory (ROM) and random-access-memory (RAM). The ROM contains the instrument operating system and other firmware. Front-panel control settings, displays, and calibration information are stored in non-volatile RAM. This RAM has battery backup power to retain the data when instrument power is off. The instrument operating system uses additional RAM.

The microprocessor communicates with the memory and I/O ports via the microcomputer bus. Communication with the rest of the instrument is via the instrument bus.

Interrupts from various circuits can request processor service. The firmware contains a service routine for each of the interrupts. If necessary, the processor can mask, or ignore, all interrupts except for a power failure interrupt.

The accompanying illustrations show the address allocations for the microcomputer. These will be useful for the following descriptions. Figure 7-30 shows the entire address range of the processor. Figure 7-31 shows the I/O address range. Figure 7-32 shows PIA and Timer memory maps. Unless otherwise noted, all addresses are in hexadecimal.

Processor (Diagram 41)

The Processor board (A58) contains the microprocessor and most of its peripheral devices that compose the computer system.

Microprocessor. The microprocessor, U1025, processes data, generates addresses and control signals, and controls the operation of the instrument. The microprocessor, a 6808 (also known as 67127), has an 8-bit bi-directional data bus and a 16-bit address bus.

Output signals include the $\phi 2$ Clock (Enable), Read/Write (R/W), Bus Available (BA), and microprocessor Valid Memory Address (VMA).

The microprocessor divides the CRT Clock signal by four, producing an internal two-phase clock. This clock is available at the microprocessor's Enable output as a signal labeled $\phi 2$ Clock. The 853.3 kHz $\phi 2$ Clock drives the Timer, PIA, and DMA Controller, and it is one of the control lines available on the microcomputer bus.

The Read/Write line indicates to the peripheral and memory circuits whether the microprocessor is in the read state (high) or the write state (low). The read state is the normal standby condition and a response to a halt signal. U1030B and U2030F buffer the R/W signal to drive the various circuits.

The Bus Available signal goes high to indicate when the microprocessor releases the data bus. This occurs when the microprocessor executes a WAIT or when the HALT Input goes low.

A high VMA signal tells the memory circuits that there is a valid address on the microcomputer address bus. U3036C issues the VMA signal to the memory circuits from either the microprocessor or the DMA Controller.

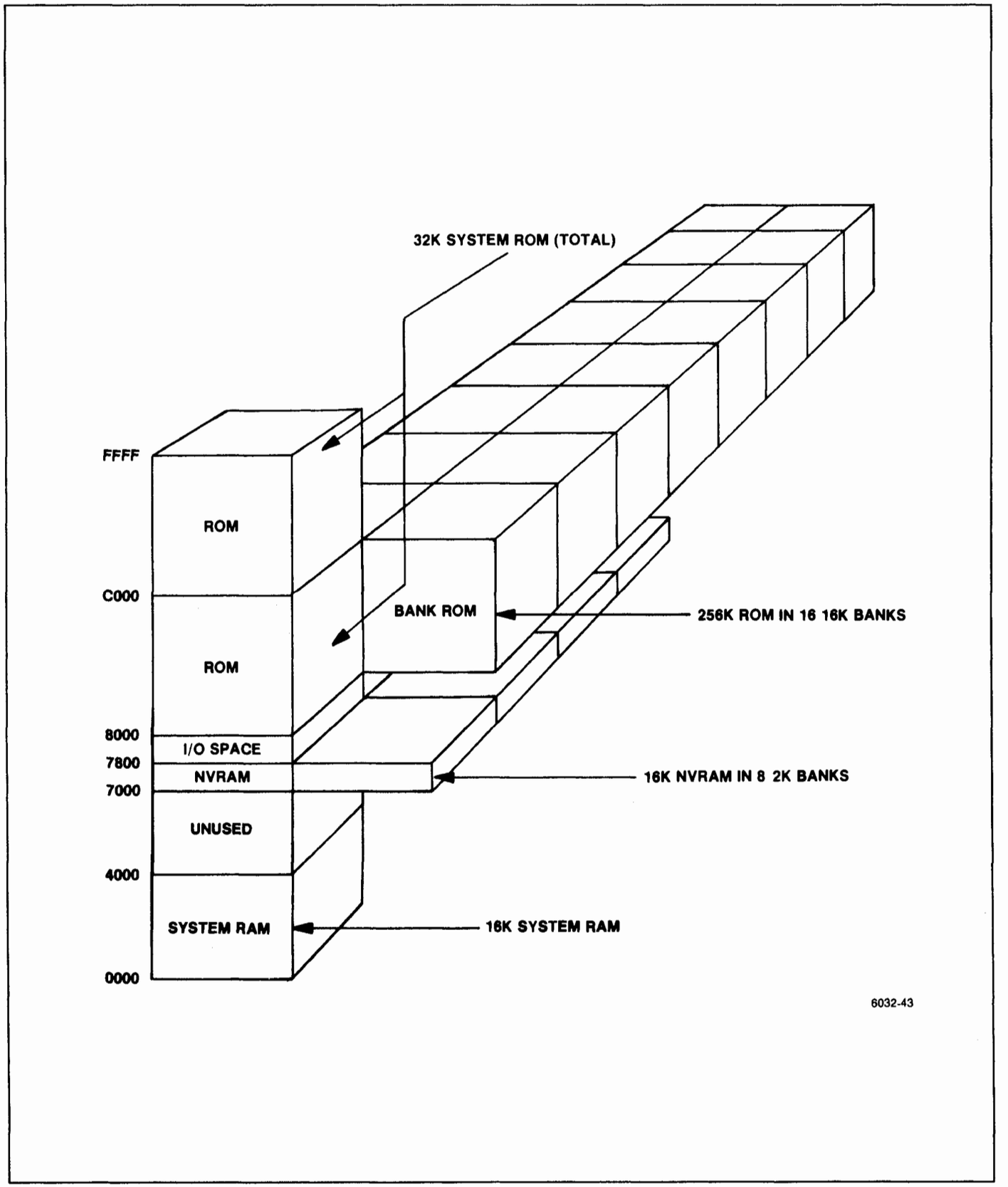


Figure 7-30. System memory map.

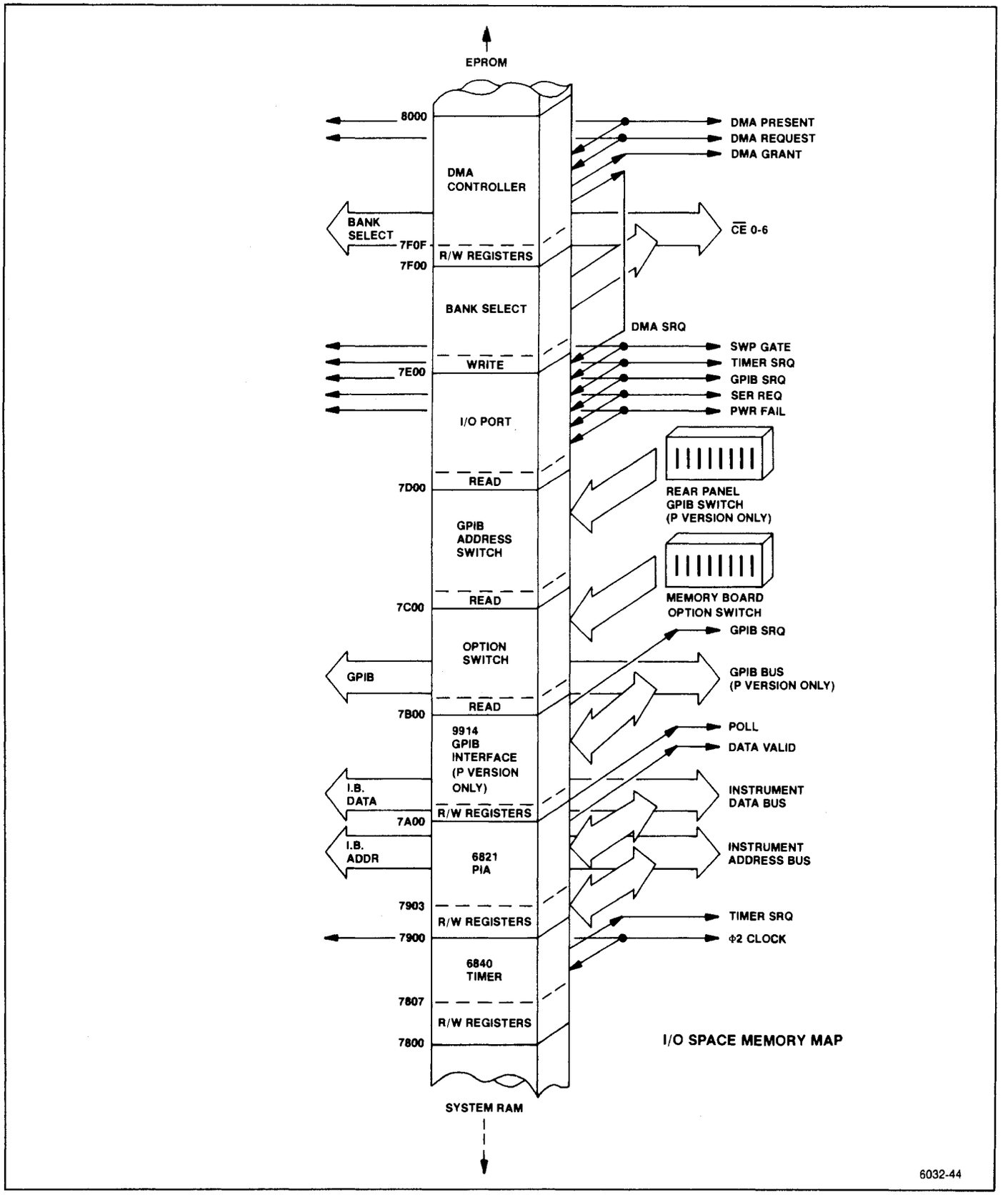


Figure 7-31. I/O address space.

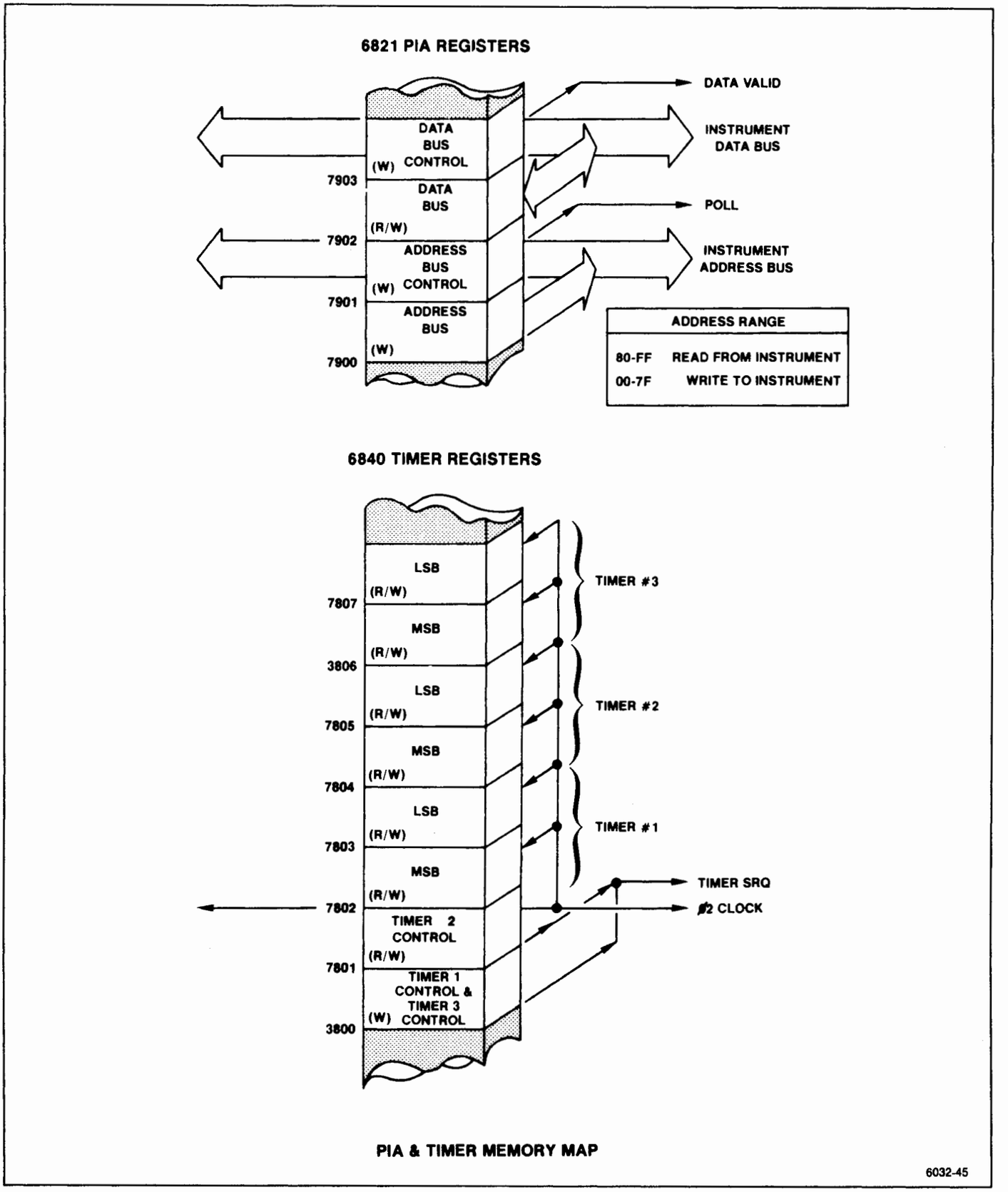


Figure 7-32. PIA and Timer address map.

Clock. This circuit generates the clock signal that drives the microprocessor, the GPIA transceiver on the GPIB board (A56), and the character generator circuitry on the CRT Readout board (A66A1).

Y1030, Q2035, and Q1030 form a clock circuit that oscillates at 3.4133 MHz. Q2035 and Y1030 form a Colpitts oscillator and Q1030 buffers the output, giving a TTL compatible clock signal. This signal is further buffered by U2030A forming the crt clock signal.

Microcomputer Bus. Microcomputer communication with memory and I/O is via the microcomputer bus. The bus consists of eight data lines (D0-D8), sixteen address lines (A0-A15), the RESET line, the VMA (Valid Memory Address) line, the Read/Write (R/W) line, and the $\phi 2$ Clock.

The data lines connect from the microprocessor through bi-directional buffer U2025. The Read/Write line controls data direction through the buffer. When the microprocessor releases the address bus, the Bus Available line (BA) disables the data bus buffers through U3036A. Jumper P3015 is a test jumper that allows disabling the data buffer and forcing a CLR B instruction to the microprocessor. Diodes CR2020 and CR2025 pull data lines MD5 and MD7 low, issuing the CLR B instruction.

The address lines connect from the microprocessor through buffers U3030 and U3025. These buffers are disabled when the DMA Controller is granted the address bus. Then the addresses come from the DMA Controller, U1020, through DMA address buffers U1015 and U1024. U1015 is a bi-directional buffer, allowing the microprocessor to address the DMA Controller.

The RESET signal is a function of the Power Failure circuit. When a power failure is sensed, the RESET signal resets the Timer, PIA, DMA Controller, and circuits on the Memory (A54) and GPIB (A56) boards. The Power Fail circuit is discussed in more detail later. The VMA, R/W, and $\phi 2$ Clock signals have already been described.

Address Decoder. AU3035 decodes the addresses for the I/O circuits on this board. When the microprocessor selects an address in the range of 7800-7FFF, the I/O line from the Memory board (A54) goes low, enabling U3035. The decoder then subdivides the address range to select each circuit. Figure 7-31 shows the I/O address map. Each circuit uses only one or a few addresses within its range.

Timer. The Timer circuit, U2015, is a 6840 programmable timer used by the microprocessor to generate variable time delays. The processor programs an interval into the timer. When the interval passes, the Timer generates an interrupt (Timer SRQ). The $\phi 2$ Clock synchronizes the Timer with the microprocessor. An address in the timer range selects the Timer. Address bits A0-A2 select internal Timer registers, counters, and latches. When the Read/Write (R/W) line is low, the Timer accepts data input from the data bus. When the line is high, the Timer puts its data on the data bus. See a 6840 data sheet for additional details. The Timer addressing is mapped in Figure 7-32.

PIA and Instrument Bus. The microcomputer communicates with the instrument through the Instrument Bus. The 6821 PIA, U1010, interfaces the Digital Control circuits to the Instrument Bus. This bus contains eight data lines (DB0-DB7), eight address lines (AB0-AB7), the DATA VALID line, the Service Request (SER REQ or SR) line, and the POLL line, all through the PIA.

The PIA receives Read/Write, $\phi 2$ Clock, and RESET control signals from the microprocessor. Figure 7-32A shows the PIA address map.

The address lines are buffered by U3015. The data lines are buffered by bi-directional buffer U3010. The buffer is gated on when data is valid. The most significant address bit selects data direction so that half of the address space is for writing to the instrument, and half is for reading from the instrument. The PIA CB2 port (U1010 pin 19) goes low when the data on the Instrument Bus is valid. Resistor-capacitor circuits delay the DATA VALID signal to the Instrument Bus, assuring the proper timing relationship with the other Instrument Bus signals.

The PIA issues the POLL and DATA VALID (or DV) signals in response to a service request from the hardware on the Instrument Bus. The requesting circuit responds to the POLL signal on the Instrument Data Bus.

The Internal Control (INTL CONT) signal comes from the Accessories Interface assembly (A30A76). This signal is normally high unless external control through the ACCESSORIES connector is desired. When low, the Bus Enable signal goes high, disabling the address and data buffers and the DATA VALID and POLL outputs. The Bus Enable jumper, P3010, may be removed to disable the Instrument Bus for test purposes.

DMA Controller. When the instrument transfers data through the GPIB interface, the DMA Controller, U1020, sets up direct transfers between system RAM and the

GPIA interface circuit on the GPIB board (A56). (This only occurs on the 2754P.)

Before each transfer, the microprocessor loads U1020 with the starting address of the RAM data and the number of data bytes to be transferred. When the GPIA interface circuit requires data, it pulls the DMA Request line, pin 4 of P1035, low. This causes U1030C to set U1020's Transfer Request input high, requesting a byte. In return, the DMA Controller sends a DMA request to the processor's HALT input, pulling it low. This also disables any maskable interrupt request to the processor. With HALT low, the microprocessor completes its currently executing instruction and then stops, signals that the bus is available (sets the BA line high), tri-states its data bus, and sets itself in the Read state (R/W line high).

The BA signal disables the microprocessor address buffers, U3030 and U3025, and enables DMA Controller access to the address bus via buffer U1024 and transceiver U1015. It also gives bus control to the DMA Controller. The least significant address lines are interfaced to U1020 through a transceiver because the processor uses addresses A0 through A4 to address the setup registers in the DMA Controller.

The DMA Controller sets the address, VMA, and Read/Write (R/W) lines to cause the RAM to place the proper byte on the data bus. Because U1030 is an open-collector gate, there is no conflict between the microprocessor and the DMA Controller over the R/W line.

The DMA Controller Transfer Strobe (TxSTB) output goes low giving the DMA GRANT signal to the GPIA circuit on the GPIB board. This informs the circuit that data is coming. After the transfer is completed, U1020 raises the HALT line, and normal processor operation resumes.

Ground from the GPIB board connects through pin 2 of P1035 as a signal that the Processor and GPIB boards are connected. If the GPIB board is not present, such as for test purposes, U1035B pin 12 goes low. This disables the DMA request.

Interrupt Processing. The microprocessor uses both maskable and non-maskable interrupts. The non-maskable interrupt is used only for sensing power-fail. The maskable interrupt is used to sense circuits requesting service. Although these interrupts may be masked by the processor, they are enabled most of the time. These interrupts can be requested by circuits on the Instrument Bus, the GPIB board, the DMA Controller, or the Timer. The instrument firmware contains service routines for each of the interrupts.

The maskable interrupts are sensed at the microprocessor's Interrupt Request (IRQ) input. Gate U2036 sets IRQ low if it senses any of the interrupt lines low. The Input Port buffer U3020 places the interrupt information and sweep information on the data bus. This allows the microprocessor to read the interrupt status.

If the interrupt is from circuits on the Instrument Bus, the microprocessor executes a poll routine to determine the exact cause of the interrupt. The Instrument Bus circuits interrupt the microprocessor by pulling the Service Request (SER REQ or SR) line low. The microprocessor responds by placing address FF on the Instrument Bus and setting the DATA VALID and POLL signals high. This causes the circuit that requested service to pull one of the data lines low.

Each circuit is assigned a different line, as shown in Table 7-22. It is possible that more than one circuit requests service at the same time. In that case, more than one data line will be low.

The microprocessor reads the data lines to determine the interrupting circuit or circuits. It then writes the corresponding bit pattern to the data bus while the address lines are set to 7F and DATA VALID and POLL are both high. When an interrupting circuit receives a low on its assigned data line with the address lines, DATA VALID, and POLL set as described, it resets its internal interrupt latch and releases the Service Request (sets SER REQ or SR high).

Table 7-22
POLL BITS

Bit 7	Not Used
Bit 6	Not Used
Bit 5	Not Used
Bit 4	End of Sweep
Bit 3	FREQUENCY knob
Bit 2	Phase Lock
Bit 1	Not Used
Bit 0	Front Panel

The non-maskable interrupt signals power loss. Circuitry on the Z-Axis assembly (A70) senses power loss and sets the PWR FAIL line low. This causes an interrupt and starts the microprocessor's power fail routine.

When PWR FAIL goes low, Q2030 turns on and C2030 begins to discharge through R1037. If the line stays low until C2030 discharges, the RESET line goes low and the microprocessor resets itself. As part of its power fail routing, the microprocessor monitors the PWR FAIL, along with other interrupts, through U3020. If the PWR FAIL line returns to a high state before the microprocessor is reset, the microprocessor does a

power-up initialization to ensure that the instrument operation will not be affected by a temporary power loss.

This power fail sequence can be disabled by removing jumper W2035. This may prevent false resets when operating the instrument on noisy power. However, power-down settings will not be stored.

Memory (Diagram 42)

The Memory board (A54) contains some of the ROM and all of the RAM used by the microprocessor. There are 64K bytes of ROM in two 32K byte EPROMs and 32K bytes of RAM in four 8K byte RAMs. Battery backup power is supplied for 16K of the RAM. The board also contains the Options switch, which sets some instrument operations and selects processor test modes. Additional ROM is located on the GPIB board (A56).

Address Decoders. The address decoding circuits monitor the microcomputer bus to enable circuits on the board. Decoder U2045 is the main address decoder on the board. U2045 decodes four 16K-byte blocks of address space:

0000-3FFF for RAM
4000-7FFF for RAM and I/O
8000-BFFF for sytem ROM and bank ROM
C000-FFFF for system ROM

The upper half of U2045 decodes the I/O and NVRAM space. The lower half decodes the remaining memory space. The $\phi 2$ Clock signal clocks the lower half of U2045 to assure proper memory timing.

The RAM address space is from 0000-3FFF and 7000-77FF. The 16K space from 0000-3FFF is for system RAM. The 2K space from 7000-77FF is switched between eight 2K banks of the 16K non-volatile RAM.

The system RAM address space is divided between two 8K RAMs, U1010 and U3020. The lower half of U2045 and the upper half of U3025 decode addresses from 0000-3FFF. This enables U1010 for addresses 0000-1FFF and U3020 for addresses 2000-3FFF.

The non-volatile RAM is bank switched into eight 2K banks addressed from 7000 to 7800. This allows more memory than the processor can directly address. At address 7E00, the bank select circuit on the GPIB board (A56) enables latch U4020. The latch holds the RAM bank number from bits D5-D7 of the microcomputer data bus.

Latched bit D7, 7000 address enable from U3040 drives the lower half of U3025 for the 7000-77FF address space. If D7 is low, U1030 is enabled; if high, U1020 is enabled. The other two bank select bits, D5 and D6, directly drive two address lines, creating four banks in each of the 8K RAMs.

The I/O space is decoded by the upper half of U2045, U3040, and U3045. The upper half of U2045 enables U3040 for addresses from 4000-7FFF. U3040 then decodes the 7800-7FFF address for Options circuit and other I/O space. This line is sent off the board as the I/O signal. The Options circuit is addressed at 7B00 by U3045.

ROM decoding is performed by U2045 and the bank select circuits on the GPIB board (A56).

RAM. The RAM is divided into system RAM and non-volatile RAM. The microcomputer uses the system RAM for interim data storage while the instrument is operating. The non-volatile RAM stores changeable data such as waveforms, readouts, and front-panel setups. The non-volatile data is backed up by battery power when the instrument is not operating.

U1010 and U3020 form the main system RAM. Each IC contains 8K bytes of RAM. The total system RAM is thus 16K bytes.

U1020 and U1030 form the battery-backed-up non-volatile RAM. When the instrument is operating, these RAMs are powered by the +5 volt supply. When the instrument is not operating, the RAMs are powered by lithium battery BT2040. See the Maintenance section for replacement information.

Each of the non-volatile memory ICs require less than 2 μA. They will hold data as long as the battery voltage is above 2.5 V. In the battery circuit, R1030 and R2037 protect the battery against accidental short circuits. The jumper on pins 1 and 2 of P1040 provides an easy way to remove power, thus clearing all data in the RAM.

The microprocessor uses flip-flop U4030 to power-up and enable the battery-backed-up RAMs. Initially, U4030 is reset by the RESET line going low. This disables the non-volatile RAMs, U1020 and U1030. As part of the initialization sequence, the microprocessor writes to instrument bus address 73 to set U4030's output high. (U4040 decodes bus address 73). This allows C2030 to charge to +5 V, turning on Q2025, Q2035, and Q2037. Q2037 connects the +5 V supply to the RAMs' power-supply inputs, back-biasing CR1030 and disconnecting the battery. Q2025 turns on Q2030, pulling the CE inputs low, allowing the microprocessor to use the RAMs. If the microprocessor "crashes" on power up

(which might happen at cold temperatures), the battery-backed-up RAM is protected from random alteration since U4030's output remains low.

On power-down the microprocessor sets the output of U4030 low. After C2030 discharges, Q2025, Q2030, Q2035, and Q2037 switch off. R2032 pulls the CE1 lines high, to the RAM supply voltage, disabling the memory. As the supply voltage falls, CR2030 switches off, and the battery begins supplying power to the RAMs. R2036 and R3034 insure that the CE2 lines are grounded, not floating, in the standby condition, as is required for lowest current drain.

Options. The Options Switch settings tell the microcomputer which instrument options are installed so that the appropriate firmware is used. It also enables diagnostic checks and allows reporting only settings over the GPIB in Talk Only mode. Figure 7-33 shows the switch settings. See the Maintenance section for more information about using the switches.

Octal switch S1050, latch U2050, and decoder U3045 form the Options Switch. The decoder enables the latch at address of 7B00. An open switch is read by the microcomputer as a 1, and a closed switch is read as a 0. When addressed, the latch places the switch data on the microcomputer data bus.

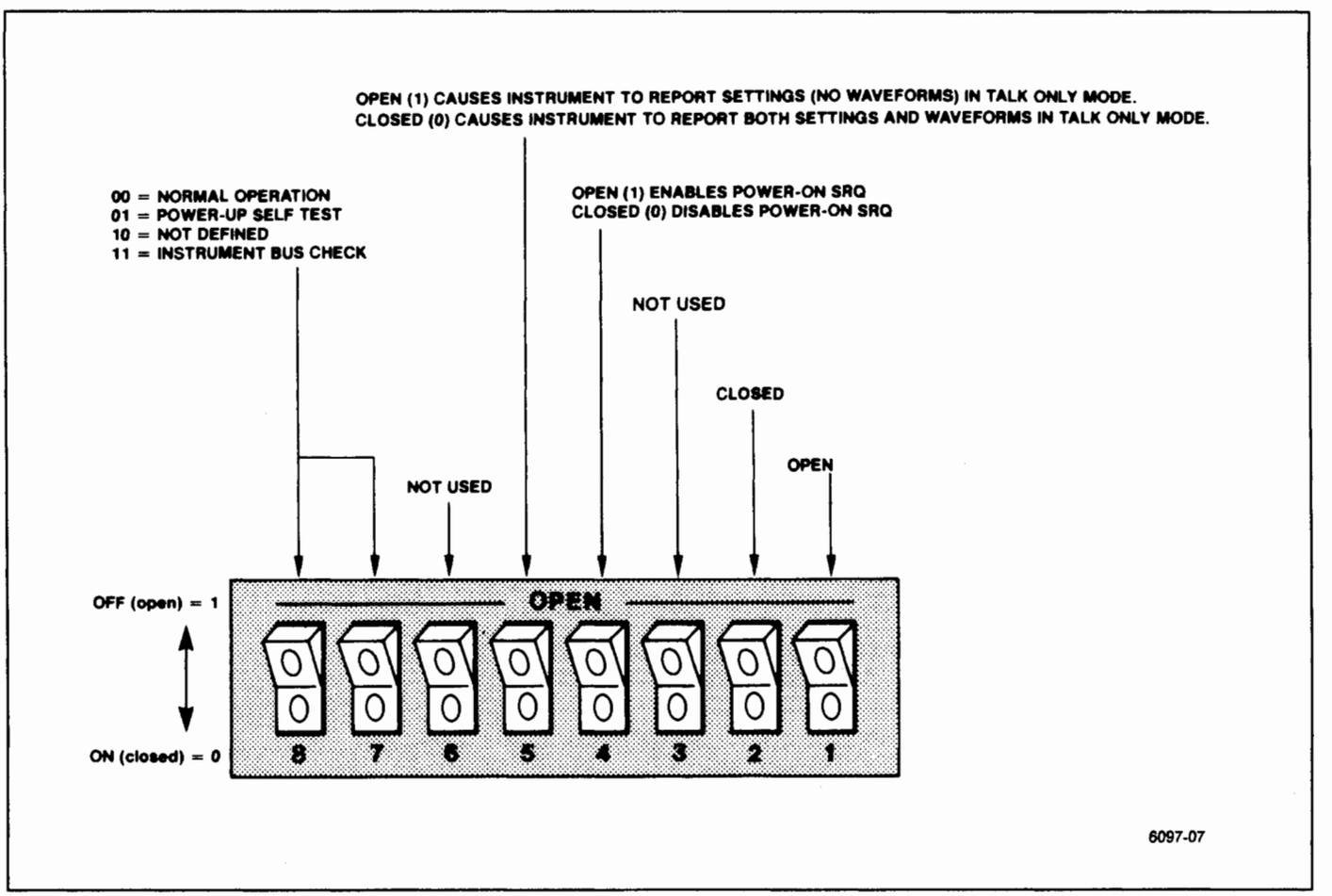


Figure 7-33. Options switch bank on the Memory board.

ROM. The ROM in this instrument is located on this board and on the GPIB board (A56). The ROM consists of system ROM containing the instrument operating system and the program ROM containing the various measurements routines and crt messages. The system ROM is always accessible, while the program ROM is bank switched as necessary. Bank switching allows expanded memory within a limited address space. The system ROM and part of the bank switched ROM are located on this board. The remaining bank switched ROM and the bank switching circuitry are located on the GPIB board (A56).

U3050 includes the "system" ROM and part of the "non-system" ROM. The ROM from C000-FFFF is the system ROM, always accessible from any of the bank ROMs. The ROM from 8000-6FFF is treated by the processor as a ROM bank. U2040C and U2040D allow both the 8000 and C000 address selection lines from U2045 to select the same physical ROM.

U3060 comprises ROM banks 0 and 1. This IC is selected when the processor addresses the range 0000-BFFF and when the CE0 signal from the GPIB board is active (low). Selection between banks 0 and 1 is done by the bank-select bit latched from DB0 by U4020. This latch is enabled when the BANK signal goes low from the GPIB board.

ROM Banks and GPIB (Diagram 43)

The GPIB board (A56) contains most of the instrument's bank-switched ROM and the General Purpose Interface Bus (GPIB) circuits. The GPIB Interface board (A30A57) connects the instrument to the GPIB (IEEE Std 488 bus). The interface board is only present on the programmable versions of the instrument.

Address Decoder. Decoder U1055, gated by the $\phi 2$ Clock, is addressed at 7800 by the I/O line from the Memory board (A54). Address lines A8-A10 produce enable signals for starting addresses 7A00, 7C00, and 7E00 as follows:

7A00 for the 9914A GPIA
7C00 for the GPIB Switch Data Buffer
7E00 for the ROM Bank Select Enable

Bank Selector. Bank switching expands the addressing capabilities of the microcomputer. The Bank Selector circuit allows addressing 256K of ROM in sixteen 16K banks. Each ROM IC holds two banks in its 32K bytes of memory. Banks 0 and 1 are located on the Memory board (A54). Banks 2 through 15 are located on this board.

Latch U2044 reads the data bus at address 7E00. Bit D0 selects even and odd banks by driving the most significant address line on each ROM IC. When D0 is low, the lower addresses in each ROM are selected. These are the even bank numbers. When D0 is high, the upper (odd bank) addresses are selected.

Bits D1 through D4 drive decoder U1040. Bit D4 enables the decoder, and bits D1 through D3 provide the chip enable signals for the ROMs. When a bank is selected, it is addressed in the 8000 through BFFF range. If another bank is selected, new data is written to the Bank Selector. Table 7-23 lists the ROM selection data.

Table 7-23

ROM Selection Data

Bank	D0	CE0-7	ROM
0	0	0	A54U3050
1	1	0	A54U3050
2	0	1	A56U1010
3	1	1	A56U1010
4	0	2	A56U1020
5	1	2	A56U1020
6	0	3	A56U1025
7	1	3	A56U1025
8	0	4	A56U1035
9	1	4	A56U1035
10	0	5	A56U3015
11	1	5	A56U3015
12	0	6	A56U3020
13	1	6	A56U3020
14	0	7	A56U3030
15	1	7	A56U3030

The light-emitting-diodes (LEDs) on U1040's chip enable outputs are diagnostic indicators. When the instrument is placed in a self-diagnostic mode, the LEDs signal results of the tests. See the Maintenance section for further information.

Bank ROMs. The bank ROMs contain most of the firmware. This includes functions such as control programs, measurement routines, and crt messages.

The memory ICs are 27256 32K-by-8 bit erasable programmable ROMs. They each have 15 address lines, 8 data lines, a chip enable line, an output enable line, and a program voltage line. Normally, the ROMs will not be erased or re-programmed.

GPIB Switches. At address 7C00, buffer U2045 writes the rear-panel GPIB switch data onto the data bus. A resistor-capacitor combination decouples each switch line to minimize noise and unwanted pulses picked up on the long circuit board lines to the rear panel.

GPIA. General Purpose Interface Adapter (GPIA) U2050 translates microprocessor commands on the microcomputer bus into appropriate codes and protocol for the GPIB bus. It also decodes data from the GPIB for the microcomputer bus. Interrupts are generated by pulling down on the GPIB SRQ line. The CRT CLK line provides the clock reference. This IC is accessed at address 7A00.

The GPIB Interface board (A30A57) connects the rear-panel IEEE 488 PORT (GPIB connector) to the GPIB board, through the GPIB Extender board (A56A1). The interface board contains two octal transceivers, U1011 and U1012, that transfer GPIB data between the rear-panel connector and the GPIA circuit.

Accessories Interface (Diagram 44)

The Accessories Interface board (A30A76) provides access to the instrument bus, the external MARKER/VIDEO input and control line, and the EXTERNAL PRESELECTOR output signal. The MARKER/VIDEO input is through a coaxial connector. The other lines are available through the ACCESSORIES connector.

To display an external signal that is applied to the MARKER/VIDEO input, pull the EXT VIDEO SELECT line (pin 1 of the ACCESSORIES connector) low. The EXT PRESEL output drive an external preselector. It is valid only in Option 01 instruments and in the preselector bands (1.7 GHz to 21 GHz). This signal tracks the instantaneous frequency at a nominal 2.1 GHz/volt with zero output corresponding to 2.072 GHz.

The instrument bus is buffered and brought out to the rear panel with the lines named to indicate their relation to the internal bus: ADV for DATA VALID, APOLL for POLL, etc.

Two lines, INT CONT and DATA BUS ENABLE, define the instrument bus/external device interface. An external controller gains control by pulling the INTERNAL CONTROL line low. This disables the internal microcomputer's instrument bus buffers and sets the data direction of buffers U2015 and U2033. In this state, the external controller sends addresses and the DATA VALID and POLL signals to the instrument. It also allows the instrument circuits to send a service request (SR) signal to the external controller. For internal control, the buffers reverse direction.

Data buffer U2038 transfers data to and from the external instrument bus. Data direction depends on whether control is internal or external and on what the address is. The buffer senses the most significant address bit, AB7, so that when in external control, the upper addresses (AB7 high) send data to the instrument and the lower half of the addresses (AB7 low) receive data from the instrument. For internal control, the data direction reverses.

The DATA BUS ENABLE line is asserted low by an external device to enable the data buffer. As long as this line is unasserted, the data buffer is set to its high impedance state and the data direction input has no effect on its output.

Front Panels (Diagram 45)

The Front Panel boards (A38A1 and A39) act as an interface between the user and the instrument. These circuits translate operator actions on front-panel controls, into data for the microcomputer to read and implement. They output data showing current operating modes to the user via LED's (light emitting diodes) and crt readout.

Output of data is provided by seven shift registers that drive LED's to light various front-panel pushbuttons and indicators to show the instrument operating mode. Operator input information, via pushbuttons or rotary switches, is read by the front-panel CPU. The CPU then outputs the data to the master microprocessor for action. The front-panel CPU scans all push buttons and rotary selectors on the keyboard matrix plus the coder for the FREQUENCY knob looking for changes in the keyboard codes or frequency coder. It then translates these changes for the master microprocessor for appropriate action. The following is a description of the hardware and a brief description of the software used by the front panel CPU.

Potentiometers. The following controls or adjustments generate analog signals used by other functions of the instrument. These controls are non-programmable.

INTENSITY is an input to the Z-Axis/RF Interface board to control trace brightness.

PEAK/AVERAGE is a digital storage input that causes signals to be either peak detected above or averaged below a displayed cursor line that tracks this control.

MANUAL SCAN sweeps the spectrum or display in manual sweep mode.

POSITION centers the horizontal and vertical deflection on the crt.

LOG/AMPL CAL varies the video signal level prior to the Video Processor board and adjusts 10 MHz IF gain to calibrate the log display.

PEAKING controls the front-end response of the analyzer by fine tuning the internal preselector.

Output Mode Shift Registers and LEDs. As previously described, LEDs mounted behind a pushbutton or below front-panel labels indicate the mode of operation. Some versions of the spectrum analyzer may not use all indicators; for example, the non-programmable versions do not have a RESET TO LOCAL button.

The LEDs are driven by shift registers (U2010, U2020, U2061, U3060, U5060, U6040, and U6070) that reside at address 74 (H) on the instrument bus. The shift registers that drive the LEDs are reloaded each time a LED changes state. The master microprocessor changes the appropriate bit in the LED code then reloads all registers. The shift register U5060 that drives the GRAT ILLUM LED also controls the voltage regulator U5080, which provides power for the graticule lights.

Processor. The CPU is an 8741 self-contained 8-bit microprocessor with on-chip EPROM and RAM. Refer to Intel UPI Users manual for a complete description of this microprocessor (Intel 8741).

The IC has a self-contained clock and a timer. The clock uses a 6 MHz crystal, Y6030, as the resonator. The timer functions either as a programmable timer or counter.

The CPU has two input/output ports. Port P10-P17 is input only and P20-P27 in an input/output port. Each port is 8-bits wide. In addition, the CPU has an 8-bit data port (D0-D7) called the output buffer, which talks to the master microprocessor. In this application all data is output only with U3030 being a buffer between the CPU and the instrument bus. Information that the CPU wishes to relay to the master microprocessor, is loaded into a latch connected to the output buffer U3030. The master microprocessor accesses the CPU by pulling address F4, out of decoder U2040, low to activate the output buffer and enable U3030 so data is passed onto the instrument bus.

The CPU is reset by the master microprocessor. When DB3 is selected for more than 10 ms (same as writing 08 at address 74) C5021 charges and U5020A output resets the CPU.

Scanning the Keyboard. The front-panel keyboard is arranged in a matrix of 6 rows of 5 columns and 6 rows of 7 columns (see Table 7-24). The RESOLUTION BANDWIDTH, SPAN/DIV, TIME/DIV, MIN RF ATTEN dB, and REFERENCE LEVEL selectors are rotary switches where each contact occupies a position in the keyboard switch matrix. Except for TIME/DIV and MIN RF ATTEN, the rotary switches are independent. The master microprocessor notes the current setting of these selectors by noting which contacts are closed. When a change is made the master microprocessor notes which direction the selector was moved by noting the relative position of the current contact closure with the previous setting. Pull up resistors, within R1030 through R1037, on each column of the row currently being read, will pull that column high if the switch is open. The basic algorithm of scanning is to pull one row at a time down and note which columns have a 1 or 0. Port one, P10-P17 (pins 27-34), read the columns. Part of port two (pins 21-24) are responsible for activating the rows. Basically the process consist of pulling one row at a time down to a logic 0 and then reading all the columns. If a switch contact is open it reads a "1" and if it is closed it reads a "0".

Since there are 16 rows to scan and only 4 pins (P20-P23) available at the number 2 port, the output is multiplexed through U2050 (U2060) and U1060 (U1061). These IC's are open collector output, TTL compatible multiplexers. They decode data out of P20, P21, P22, and P23 (pins 21-24) and their output pulls the appropriate row of keys down. Table 7-24 is a chart showing the switch matrix codes, and which keys correspond to a given address in the matrix code. Note that column 6 contains the MIN RF ATTEN settings, column 7 the SPAN/DIV and RESOLUTION BANDWIDTH settings, column 8 the REFERENCE LEVEL settings, and columns 1 & 2 are devoted entirely to the TIME/DIV selections.

Due to the characteristics of the switch matrix, if two keys, in any row or column are closed, and a third is closed so three corners of a rectangle are established in the key matrix, the CPU will see a phantom closure at the fourth corner. For example; if Y6/X3, Y6/X7 are closed, and then Y3/X7 is closed, the CPU will see a phantom closure at Y2/X3 as it scans the key matrix. To suppress these phantom key closures, diodes have been added in series with the RESOLUTION BANDWIDTH, MIN RF ATTEN, SPAN/DIV, and certain other keys in column 6 and 7 of the key matrix. In addition, an error detection algorithm is used in the CPU to eliminate additional phantom key closures that

might occur.

Scanning the FREQUENCY Control Coder. The FREQUENCY control contains a pair of phototransistors that output a gray code through U5020B and U5020C to P27 and P26 (pins 38 and 37) of the CPU. This gray code signifies the direction the control is turned. During a scan cycle, the CPU looks at the status of the FREQUENCY control code and if it detects a change, the CPU performs a shift and exclusive-OR operation which derives the correct code to output over the instrument bus to the master processor to tell it which direction to tune the center frequency.

Outputting the Correct Code. The remaining two bits out of port 2 (P24 and P25) drive the appropriate hardware and initiate an SRQ on the instrument bus. When the SER REQ line is pulled down, the master microprocessor will service either the keyboard or the frequency coder. The front panel CPU (U5030) initiates a SRQ by pulling down P24 or P25. A low out of P24 (pin 35) will initiate a keyboard SRQ. The master microprocessor will now service the request by reading the keyboard data in output buffer U3030. A low out of P25 (pin 36) initiates a FREQUENCY control SRQ and causes the master microprocessor to service the request by reading the frequency code in the output buffer.

A low out of P24 is inverted by U4010E so it clocks the flip-flop U5011B. The resultant low on the Q(bar) output pulls the SER REQ line down. (Refer to the instrument bus POLL sequence described under the master microprocessor description for the service request sequence.) The master microprocessor now raises both the POLL line and AB7. This is gated through U3010A (U6030A) as a low to DB0 on the instrument bus. The master microprocessor reads the bus and sees a low on DB0. This indicates that a keyboard interrupt has occurred and it must read the new keyboard code. The master processor first clears the interrupt by pulling AB7 and then the POLL line low. DB0 now goes high. The master microprocessor now writes a 0 to DB0, the same as it read, and raises the POLL line. This clocks U5011A and resets U5011B which removes the SRQ(bar). The instrument processor now reads the data in the output buffer, U3030, at address F4. The front panel CPU now recognizes that its output buffer has been read and it resets P24 to a 1. It is now ready for another cycle.

A similar process occurs when P25 (pin 36) of the CPU is pulled low by a FREQUENCY coder interrupt. A low on P25 is propagated through U4010E, U5010A, U5010B, and U3010C (U6030C); only this time DB3 is involved in the poll. U4010D and U3010B (U6030B) decode a low on AB7 and high on POLL line to clock U5010A and U5011A.

Software. The algorithm that the CPU follows consists of a main scan routine, which is an endless loop, and four subroutines that can be called. One subroutine runs the on-chip timer that is used to debounce the keys, another reads the frequency knob coder and derives the proper code to output to the master processor, the third subroutine reads the keyboard and stores the address of all keys that were closed, and the fourth subroutine looks at the keycode from the key addresses that were stored, and outputs the key codes and/or frequency code for the master processor. There are also a number of checks and tests that have to be done in each routine in addition to the obvious tasks.

Main Scan Routine. There are two types of scan; the first is made after a reset, the second type consists of the following scans; the keyboard, frequency coder, and the output data. During the first scan, data in the CPU is initialized. The CPU reserves part of its RAM to store and remember all key and frequency knob coder settings. During all scans, the CPU reads the frequency code and each row of keys on the keyboard. It compares what it read to that stored in RAM and if there is a difference, the CPU calls the appropriate subroutine for either the keyboard or the frequency coder knob. After a complete scan, the CPU checks to see if new information needs to be output to the instrument processor. If it does the CPU calls up the output subroutine.

Prior to the first scan, after reset, the CPU puts all 1's (highs) into its keyboard memory. This corresponds to open keys. On the first scan, the CPU will note five apparent closures due to the TIME/DIV, MIN RF ATTEN, SPAN/DIV, RESOLUTION BANDWIDTH, and REFERENCE LEVEL selectors. These closures are noted and output to the master processor. Because the master processor memory knows the position of each selector to close a key, the processor calls these the power-up settings. When a front panel knob changes position the master processor can determine which direction the knob changed and what it must do to respond to the change. A complete scan, without detecting any key closures takes about 800 us.

Keyboard Check Subroutine. This subroutine is called when the main scan routine detects a change in the keyboard matrix which occurs when a key opens or closes. A key opening usually signifies that an action has been completed, whereas a closure indicates that an operation or action is requested by the user; there-

fore, the two are treated differently by the CPU.

Because mechanical keys tend to bounce when they open or close, the subroutine must debounce each key change. To debounce, the subroutine calls up the timer subroutine. This sets a number into the internal timer and starts it running. When the timer has timed out, in about a millisecond, the keyboard subroutine again scans the row and compares this scan with the scan before the debounce check. If the scan does not compare, the routine assumes the key change was a bounce or fluke, and it returns to the main scan routine. If it does compare, the routine then recognizes that a key state has changed. It then checks to see if this is the first scan that looked for a key change after it has outputted previous information to the master processor. If it is the first pass then the routine causes the CPU to re-scan the full keyboard matrix to ensure that there is not a phantom key closure. If this is the second or subsequent pass and an actual key change has occured, the routine then notes if the key change was an opening or closure. If it was an opening the CPU memory is updated to the fact that the key is open. If a closure has occurred, the routine will then check the column that has the closure and output a new key address onto the output stack. This address consists of the key's row and column location. After outputting the address, the subroutine returns to scanning the remainder of the keyboard matrix.

Frequency Coder Subroutine Check. This subroutine is called when the main scan routine detects a change in the frequency coder switch. Like the keyboard subroutine, this routine also debounces the frequency coder switch after every change to ensure that the switch code has changed. If a real change is noted, the routine proceeds to determine the direction of the change. The frequency knob outputs a two-bit code with only one bit at a time changing as the control is rotated. The direction the knob is rotated is determined by the property of a gray code, generated by an exclusive-OR logical operation within the CPU. The previous state of one bit is compared with the current state of the other bit. Down (counterclockwise rotation) yields unequal inputs, while up (clockwise rotation) yields the opposite. The bit that indicates direction is inserted as the MSB for the frequency coder byte. This byte is then loaded into the output stack. The subroutine then returns to the main scan routine.

Output Subroutine. After each scan, the CPU checks its output register to see if any information needs to be output. If it needs to be output, the output subroutine is called up; if not, another scan is started. The output subroutine checks a number of things before it outputs any information to the output register. It first determines if the CPU is on its first or initial scan after a reset. The first scan will contain more than one closure. All of these closures must be output before it continues. On all scans that follow, the routine looks for more than one closure by checking the number of entries into the output stack. If more than one closure has been entered, the output routine aborts. This eliminates outputting phantom key closures.

The routine is now ready to output information. It pulls a key address from the output stack and looks up the code from a look-up table in ROM. This key code is loaded into the data port or output buffer. The appropriate port P24 or P25 (pins 35 & 36) is pulled low. The routine continuously reads the frequency coder and updates its memory while it is waiting for the master processor to read the data in the output buffer. Once the data has been read, P24 or P25 goes high and the subroutine starts to check the output stack for more key closures. When the output stack is empty, the first scan flag is rescinded and the CPU returns to its main scanning routine.

Table 7-24
FRONT PANEL SWITCH MATRIX CODE/FUNCTION TABLE

ROW	COL	HEX CODE	MAIN FUNCTION	<SHIFT> FUNCTION	DATA ENTRY
X1	Y1	00	20 μs TIME/DIV		
X1	Y2	01	50 μs TIME/DIV		
X1	Y3	02	0.1 ms TIME/DIV		
X1	Y4	03	0.2 ms TIME/DIV		
X1	Y5	04	0.5 ms TIME/DIV		
X1	Y6	05	1 ms TIME/DIV		
X1	Y7	06	2 ms TIME/DIV		
X1	Y8	07	5 ms TIME/DIV		
X1	Y9	08	10 ms TIME/DIV		
X1	Y10	09	20 ms TIME/DIV		
X2	Y1	0A	50 ms TIME/DIV		
X2	Y2	0B	0.1 s TIME/DIV		
X2	Y3	0C	0.2 s TIME/DIV		
X2	Y4	0D	0.5 s TIME/DIV		
X2	Y5	0E	1 s TIME/DIV		
X2	Y6	0F	2 s TIME/DIV		
X2	Y7	10	5 s TIME/DIV		
X2	Y8	11	AUTO		
X2	Y9	12	MNL		
X2	Y10	13	EXT		
X3	Y1	14	EXT TRIG		
X3	Y2	15	SINGLE SWP		
X3	Y3	20	SAVE A		
X3	Y4	17	2 dB/DIV	dB/Hz	
X3	Y5	16	B-SAVE A		
X3	Y6	19	10 dB/DIV	dB/DIV	
X3	Y7	1A	START/STOP	MKR START/STOP	Hz dB
X3	Y8	2F	MAX SPAN		
X3	Y9	1C	– STEP	STEP SIZE	
X3	Y10	1D	FINE		
X3	Y11	60	FIND PEAK↑		
X3	Y12	61	1		
X3	Y13	62	5		
X3	Y14	63	9		
X3	Y15	64	BANDWIDTH	dB BW	
X3	Y16	65	FIND PEAK MAX	FIND PK & CENT	
X4	Y1	1E	INT TRIG		
X4	Y2	1F	FREE RUN		
X4	Y3	22	NARROW		
X4	Y4	21	LIN	MKR–>REF LVL	
X4	Y5	18	VIEW B		
X4	Y6	23	WIDE		
X4	Y7	2A	ZERO SPAN		
X4	Y8	25	AUTO RES		
X4	Y9	26	+ STEP		
X4	Y10	1B	MIN NOISE/DIST		
X4	Y11	66	FIND PEAK <–	xdB<–	
X4	Y12	67	2	(Plotter type)	
X4	Y13	68	6		

Table 7-24 (Continued)
FRONT PANEL SWITCH MATRIX CODE/FUNCTION TABLE

ROW	COL	HEX CODE	MAIN FUNCTION	<SHIFT> FUNCTION	DATA ENTRY
X4	Y14	69	0	(Diagnostic menu)	
X4	Y15	6A	SIGNAL TRACK		
X4	Y16		Not used		
X5	Y1	28	Not used		
X5	Y2	29	GRAT ILLUM	RESET	
X5	Y3	2B	MAX HOLD	(Display errors)	
X5	Y4	30	SPAN/DIV	BAND▽	MHz/+dBx
X5	Y5	2C	REF LEVEL	REF LEVEL UNITS	kHz/−dBx
X5	Y6	24	VIEW A		
X5	Y7	2D	SHIFT	(Shift cancel)	
X5	Y8	27	FREQUENCY	BAND△	GHz
X5	Y9	2E	TUNE CF/MKR	MKR OFF	
X5	Y10	31	REPEAK (75Ω in Opt. 07)	PEAK MENU	
X5	Y11	6C	FIND PEAK–>	xdB–>	
X5	Y12	6D	3	(Plotter B-A offset entry)	
X5	Y13	6E	7	(Disable corrections)	
X5	Y14	6F	.	(Display errors)	
X5	Y15	70	RECALL DISPLAY	STORE DISPLAY	
			MIN RF ATTEN dB		
X6	Y1	32	0		
X6	Y2	33	10		
X6	Y3	34	20		
X6	Y4	35	30		
X6	Y5	36	40		
X6	Y6	37	50		
X6	Y7	38	60		
X6	Y8	39	RECALL SETTINGS	STORE SETTINGS	
X6	Y9	3A	ΔF	STEP ENTRY	
X6	Y10		Not Used		
X6	Y11	72	FIND PEAK↓		
X6	Y12	73	4		
X6	Y13	74	8		
X6	Y14	75	BACK SP		
X6	Y15	76	PULSE STRETCHER	IDENT	
X6	Y16	77	THRESHOLD	MENU	
X7	Y1	3C	FREQUENCY SPAN/DIV		
X7	Y2	3D	FREQUENCY SPAN/DIV		
X7	Y3	3E	FREQUENCY SPAN/DIV		
X7	Y4	3F	FREQUENCY SPAN/DIV		

Table 7-24 (Continued)
FRONT PANEL SWITCH MATRIX CODE/FUNCTION TABLE

ROW	COL	HEX CODE	MAIN FUNCTION	<SHIFT> FUNCTION	DATA ENTRY
X7	Y5	40	RESOLUTION BANDWIDTH		
X7	Y6	41	RESOLUTION BANDWIDTH		
X7	Y7	42	RESOLUTION BANDWIDTH		
X7	Y8	43	RESOLUTION BANDWIDTH		
X7	Y9	4A	RESET TO LOCAL	SRQ	
X7	Y10	45	LINE		
X7	Y11	78	READOUT	CAL	
X7	Y12	79	BASELINE CLIP		
X7	Y13	7A	ΔMKR	MKR->CF	
X7	Y14	7B	1<-MKR->2		
X7	Y16	7D	PLOT	(Select plotter)	
X8	Y1	46	REFERENCE LEVEL		
X8	Y2	47	REFERENCE LEVEL		
X8	Y3	48	REFERENCE LEVEL		
X8	Y4	49	REFERENCE LEVEL		

POWER SUPPLY

The Main Power Supply furnishes all the regulated voltages for the spectrum analyzer, except the crt high-voltage supply. The high-efficiency design of the Main Power Supply reduces total weight and conserves energy. The power supply consists of the following: the line input circuit, which rectifies and filters the incoming line voltage; the inverter, which drives the primary of the power transformer; the rectifier-filter circuit, which rectifies and filters the secondary voltages; the voltage reference circuit, which furnishes a stable and precise reference for the regulators; and the regulator circuits, which control the voltage and current for the supplies that require precise regulation.

The Fan Driver board houses the Fan Driver circuit, which furnishes the appropriate drive current for the fan motor. It also contains the Over-Voltage Protection circuit, which shuts down the +5 V supply in case of over-voltage. Refer to Diagram 46.

Line Input Circuits

Power is applied through line filter FL301, line Fuse F301, and through FL302 (for additional normal mode/common mode EMI filtering) to POWER switch S300. The power is then sent through line selector connector J1091. The line filter prevents power-line interference from entering the power supply, and it also prevents internally- generated signals from radiating out the power cord.

Line selector switch S302 allows instrument operation from either a 15 V nominal or 230 V nominal line voltage source. With S302 is in the 115 V position, pins 1 and 2 of P1091 are connected to the input power, and rectifiers CR3096 and CR4094 operate in conjunction with energy storage filter capacitors C6101 and C6111 as a full-wave doubler; thus, the voltage across the two capacitors is the peak-to-peak value of the line voltage. With S302 in the 230 V position, pins 2 and 3 of P1091 are connected to the input power and CR3096, CR4095, CR3098, and CR4094 operate as a bridge rectifier. As a result, the output voltage applied to the inverter is about the same for 115 V or 230 V operation.

Thermistors RT2093 and RT2097 limit current surge at turn on. After the instrument warms up, the current demand drops. The increase in temperature decreases the resistance value of the thermistors so they have minimum affect on the circuit.

WARNING

Because C6011 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the POWER switch is turned off. A relaxation oscillator formed by C5113, R5111, and DS5112, indicates the presence of voltages in the circuit until the potential across the filter capacitors is below 80 V.

Thermal cutout switch S2103 opens if the interior of the instrument reaches 103 degrees C to prevent overheating in case the cooling fan fails.

E1094 and E2095 are surge voltage protectors. When the line selector switch is in the 115 V position, only E1094 is connected across the line input. If a peak voltage surge in excess of 230 V occurs across the input, or if the instrument is accidentally connected to a 230 V source, E1094 will break down and demand enough current to open the line fuse. When the instrument is operated with the line selector at 230V, E1094 and E2095 operate in series to protect the input against line surges of approximately 460 V peak.

The voltage for the line trigger is taken across CR3096. This 48 Hz to 440 Hz voltage drives optical isolator U5043. The pulsating 5 V output is ac coupled, then sent both to the Sweep circuit to provide instrument triggering at the line frequencies and to the Z-Axis board for the Power-Fail Detector circuit.

Inverter Circuit

The inverter consists of a multivibrator that produces a rectangular shaped signal to drive the ramp generator and the inverter logic circuits. The ramp generator produces a low-level sawtooth ramp that is applied to the primary regulator circuit. The inverter logic circuits control the duty cycle of the inverter driver and the inverter output stage. The primary regulator circuit compares the +17 V supply output with a reference voltage, then gates the inverter logic circuits off and on to control the inverter duty cycle and the effective primary voltage. The inverter driver stage amplifies the signal from the inverter logic circuit and drives the output stage. The output stage consists of two power switching transistors that drive the primary of main power transformer T4071. The primary over-current sense and soft start circuits add protection.

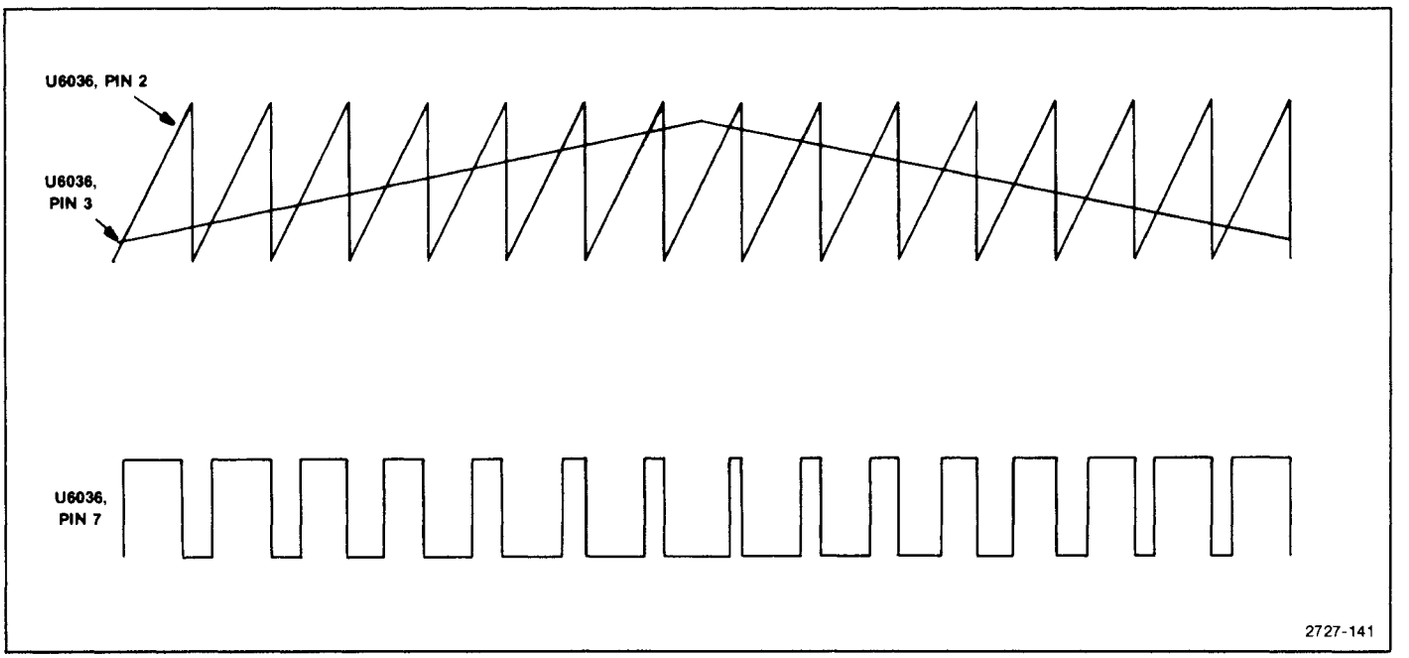


Figure 7-34. Primary regulator input and output waveforms.

Multivibrator

U6059, a low-power 555 timer, is a multivibrator that operates at approximately 66 kHz and 90% duty cycle. Oscillator frequency is adjusted by R6061. The rectangular-shaped output signal is applied through R6052 to the primary of T6044 in the ramp generator and also directly to U6053, U6063A, U6063B, and U6069.

Ramp Generator

The ramp generator circuit is a gated sawtooth generator that consists of T6044, Q5023, Q6034, Q5032, and related components. The negative excursion of the rectangular shaped signal from U6059 is coupled across T6044 to force Q6034 into conduction. This forward-biases Q5032. Its collector moves toward +17 V to charge C5038 to this value. Q6034 loses drive (since the pulse coupled across T6044 has died away) and the two transistors cut off. Q5023 acts as a constant-current drain to linearly discharge C5038. This signal is coupled across divider R5036/R6032, then applied through C6039 to the input of comparator U6036, which is part of the primary regulator.

Primary Regulator

The primary regulator circuit consists of comparator U6036 and U6046, photocoupler U6043, and related components. The circuit varies the duty cycle of the driving signal for the inverter. The +17 V is divided by R6038 and R6037 to approximately +4.8V and applied to the inverting input of U6036. The +5 V reference is applied through R6022 to the non-inverting input of U6036, where it is combined with the ramp signal from the ramp generator stage. The non-inverting input receives a sawtooth signal of approximately 500 mV peak-to-peak superimposed on a +5 V dc level. This is compared with the +4.8 V on the other input, so the comparator switches with each sawtooth cycle. Note in Figure 7-34 that as the level at pin 3 (which corresponds to the +17 V supply variations) rises and falls, the duty cycle of the output waveform varies accordingly.

The output signal of U6036 is applied to optical isolator U6043, which drives the input of U6069.

Inverter Logic

This stage consists of steering flip-flop U6063B and dual quad input NAND gate U6069. The flip-flop is connected so it toggles to enable first one gate then the other. The square-wave output from the multivibrator drives the clock input of U6063B. The signal also enables each gate to ready it for the other signals that

arrive later. The output state of U6063 determines whether the upper or lower section of U6069 will be ready for the enabling signal. Assume that the Q output of U6063B is holding pin 2 of U6069 high. This means that the complement output of the latch is holding the opposite side of the gated pair disabled. When the output of U6043 moves high, U6043 controls the duty cycle of the inverter, the upper section of U6069 produces a low state. This causes current to flow through half the primary and Q6078 only. On the opposite cycle of the multivibrator signal, the latch is reset, so the lower half of U6069 is enabled and Q6077 is now in the conduction path.

Inverter Driver

The inverter driver consists of transistors Q6077 and Q6078, transformer T6081, and related components. This is a push- pull amplifier with diode protection in the collector circuits to prevent damage from voltage transients during operation. The drive signal is induced into the two secondary windings of T6081 and coupled to the output stage.

Output Stage

This circuit consists of transistors Q2071 and Q2061, series LC tank L1081/C1063, and transformer T4071. The output transistors are connected in a half-bridge configuration. The two transistors drive the series tank, which acts as an energy storage element and an averaging circuit. Output transformer T4071 is driven by the tank circuit, and it, in turn, drives the secondary circuits.

Primary regulation, as discussed previously, occurs when the duty cycle of the inverter driver main switching transistors is varied. Maximum duty cycle occurs at low input line (90 V) and fully loaded output. At maximum duty cycle, both transistors are off for only 10% of the period, or 1.5 μs. This short interval allows any stored base charge to deplete, so there is no chance both transistors will conduct at the same time. Minimum duty cycle occurs at high input line (132 V) and minimum loaded output. At minimum duty cycle, each transistor is off for approximately 6 μs, or 40% of the total period.

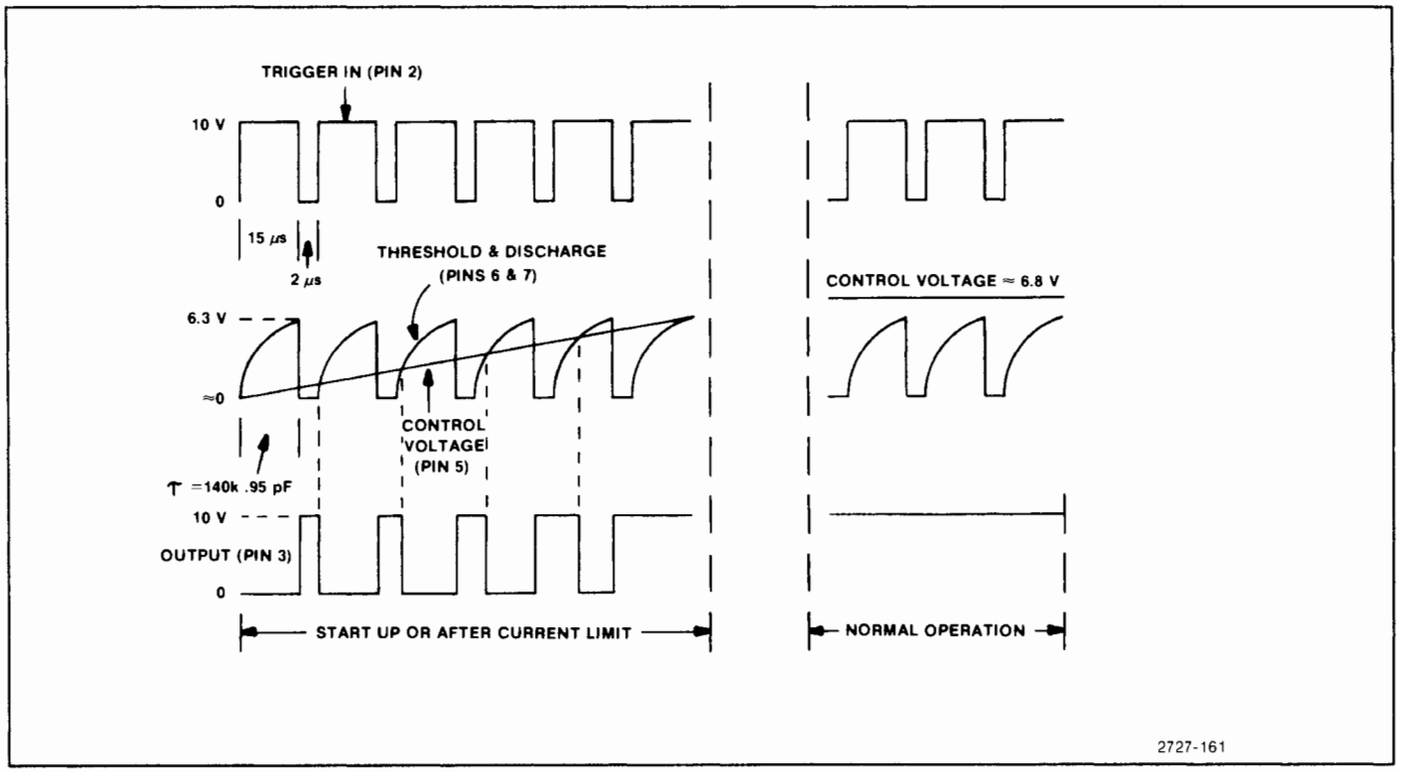


Figure 7-35. Timing waveforms for soft-start circuit.

Soft Start and Primary Over-Current Circuits

The soft start circuit consists of U6053 and associated components. Soft start gradually increases the switching transistor's duty cycle at turn-on or after over-current shutdown to prevent excessive transistor current due to charging output capacitors. Refer to Figure 7-35 for timing waveforms.

The primary over-current circuit protects against secondary shorts that could destroy the switching transistors. T2080 senses the collector current in Q2071 and creates a voltage on pin 5 of U6046B. If the bias on pin 5 surpasses the 2.5 V reference on pin 6, at approximately 6 A through Q2071, the output of U6046B sets U6063A. U6063A is a D-type flip-flop used as a timer to shut down the inverter logic for approximately 1 s and to reset the soft start circuit.

Rectifier-Filter Circuits (secondary section)

Transformer T4071 has three secondary windings. The first furnishes current to the +300 V and +100 V supplies; the second furnishes current to the −7 V, +7 V, and +9 V supplies; and the third furnishes current to the +17 V and −17 V supplies. The linear regulated supplies (+5 V reference, +5 V, −5 V, +15 V, and −15 V) derive their current from the rectifier-filter circuits.

The ac voltage from pins 7 and 8 of T4071 is applied to a bridge rectifier composed of CR3053, CR3056, CR3055, and CR3054. The output of this rectifier is filtered, then applied to the remainder of the instrument as the +100 V supply.

The +300 V supply is derived by stacking a 2X multiplier on the +100 V supply. CR3052, CR1042, CR1034, CR1022 and associated capacitors, compose this circuit.

The ac voltage from pins 9 and 10 supply current to full-wave rectifier CR4061/CR4062. The output is filtered and sent to the rest of the instrument as the +9 V supply. Two other taps off the same winding (pins 11 and 12) supply current to the bridge rectifier that consists of CR4063, CR4057, CR4053, and CR4065. The output divides across filter capacitors C3051 and C4051 to become the +7 V and −7 V supplies. The +7 V supply is only used on the Main Power Supply board; the −7 V supply is used by other circuits in the instrument.

The third winding of T4071 (pins 13, 14, and 15) furnishes current to full-wave bridge rectifier CR5052, CR5062, CR5065, and CR5055. The output is divided to become the +17 V and −17V supplies. The −17 V supply is used only on the Main Power Supply board; the +17 V supply is used both on the Main Power Supply board and elsewhere in the instrument.

+5 V Voltage Reference Supply

The +17 V is divided down by a voltage divider to Zener diode VR6026. The 6.2 V from VR6026 is divided across R6029, R6028, and R6023. CR5031 provides a regulated source of bias to VR6026 after +15 V comes up. The +5 V REF adjustment, R6028, is set by monitoring the +15 V supply and setting it for a precise +15.00 V.

Regulator Circuits

The +15 V, −15 V, +5 V, and −5 V are regulated. Since all four regulators are basically the same, only the +5 V regulator is described. Significant differences are discussed following this description.

U2037A, the voltage regulator part of the circuit, compares the +5 V[REF and +5 V SENSE voltages, amplifies the difference, and applies the change to driver transistor Q2023. The change is amplified by this stage and applied to the base of series-pass transistor Q2024 to change its conduction and correct for the original change to the +5 V. The +5 V sense samples the +5 V at a distribution point on the Mother board. This signal compensates for voltage (IR) losses to that point.

U2037B is the current limiter portion of the regulator. The amplifier detects the voltage differential across the current sensing resistor R2017, which is in series with the output load. When the overload threshold is reached, as set by R2017, R2039, R3032, and R3031. U2037B removes bias current from driver transistor Q2023 and Q2024. The negative bias on R3031 allows the limiter to remain active under short circuit conditions.

The +15 V regulator is identical to the +5 V regulator, except that the current limiter, U2037D supplies additional positive bias for Q2031 when it is not active. The −15 V regulator is virtually identical to the +5 V regulator. The −5 V regulator differs from the others in that a driver stage is not required, so the preamplifiers drive series-pass transistor Q5013 directly.

+5 V Over-Voltage Protection Circuit

Zener diode VR1015 and SCR Q1010 form the over-voltage protection circuit. If the +5 V supply exceeds +6 V, the potential on the gate of Q1010 biases it into conduction. This forces the +5 V supply to ground potential; it remains at ground potential until the mains power is turned off and turned on again.

Fan Drive Circuit

The fan drive circuit provides a temperature- controlled current drive to the fan motor. The circuit produces a three-phase drive current of approximately 240 Hz operating frequency. The actual drive circuit operates as a ring counter.

Transistors Q1038 and Q1044 form a voltage regulator controlled by thermistor RT2045. The value of RT2045 varies inversely with the internal temperature of the analyzer. The thermistor and a companion resistor, R2042, fix the turn-on voltage at the emitter of Q1044 at approximately −13 V; the voltage goes more positive as the analyzer warms up. VR 2038 is connected with jumper P2043 when the rackmount fan is used to prevent the output voltage from going below approximately 9 V.

The ring counter consists of three stages: Q1025 and Q1020, with R1031/C1032 and R1027/C1018 as the frequency-determining components; Q2025 and Q1018, with R1033/C1033 and R2019/C1019 as the frequency-determining components; and Q2030 and Q2020, with R2014/C2012 and R2016/C2018 as the frequency-determining components. When the analyzer is energized, one of the three ring counter stages begins to conduct before the others; owing to circuit imbalances. Assume that the upper stage (Q1025 and Q1020) begins to conduct first. The collector voltage of Q1025 is near −17 V, which fixes that point as the most negative in a ring consisting of R1032, R1029, R1028, R2036, R2034, and R1036. Since the emitter voltage of the three control transistors (Q1020, Q1018, and Q2020) is the same, the voltage division around the resistive ring is such that Q1018 and Q2020 remain cut off. When the capacitive charge that holds Q1020 in conduction bleeds off, the transistor cuts off and the next stage can begin to conduct. Operation of the other two stages is prevented until the RC combination discharges. The fan motor inductance works in conjunction with the RC components to regulate the switching of the stages.

This ring-counter action builds up slowly until the circuit produces a three-phase drive signal of approximately 240 Hz. The inductance of the motor coils round off the otherwise sharp corners of the drive signal, so the current waveform looks a great deal like the output of a half-wave rectifier at P2020 pins 1, 2, and 3. The phases of the fan drive signals is approximately 120 degrees apart.

OPTIONS

This section describes the options available at this time for the spectrum analyzer. Changes in specifications, if any, are described in this section. Contact your local Tektronix Field Office or representative for additional information and ordering instructions (unless otherwise indicated).

Options are usually factory installed; however, field kits are available for some options. Contact your local Tektronix Field Office or representative for information on field kits and their installation.

Options A1 — A5 (Power Cord Options)

There are five international power cord options offered for the spectrum analyzer. The physical descriptions of the cord plugs are illustrated in Figure 8-1. For ordering purposes, refer to the Replaceable Mechanical Parts list in the Service Manual, Volume 2, for the Tektronix Part Number.

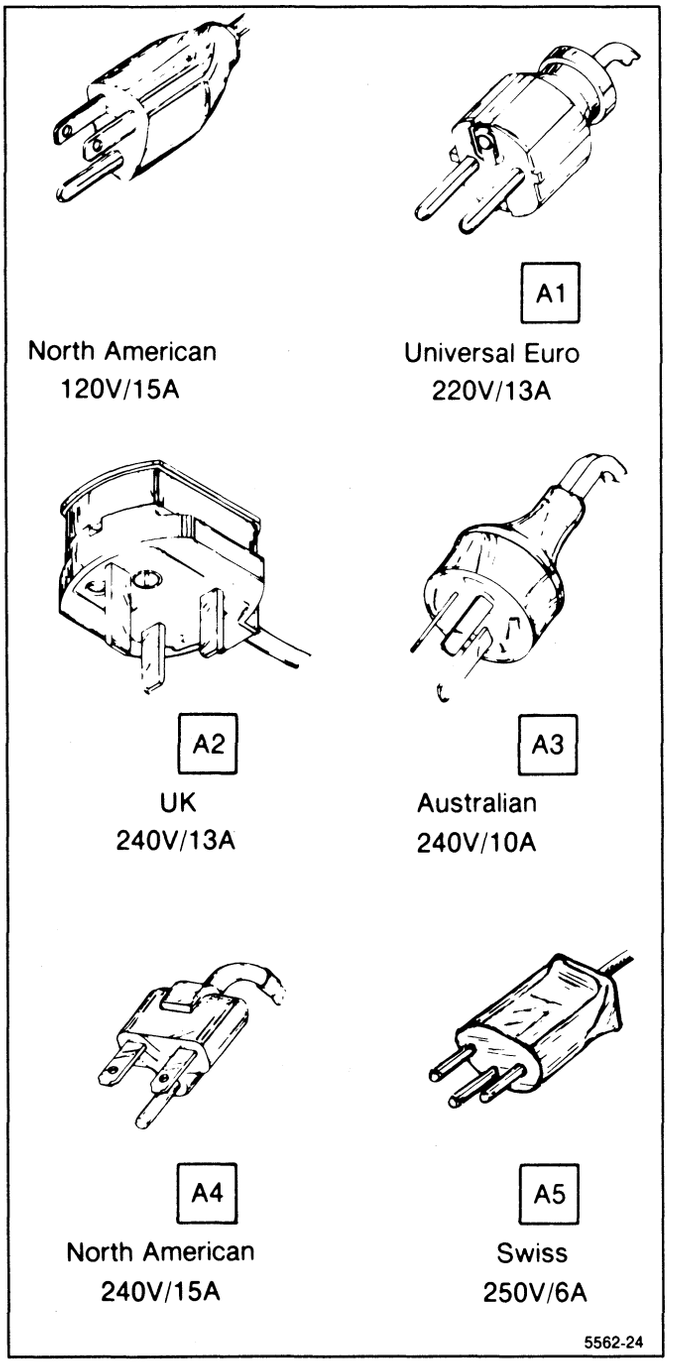


Figure 8-1. International power cord options.

Options M1—M5 (Extended Service and Warranty Options)

There are five extended service and warranty options offered for the spectrum analyzer (see Table 8-1) that go beyond the basic one-year coverage. In addition, Options M4 and M5 provide NBS certification with each calibration. Refer to the Tektronix, Inc. catalog or your local Tektronix Field Office or representative for additional information to satisfy your specific requirements.

Option 01 (Preselector)

Option 01 adds an internal preselector and limiter. Band 1 input signals are routed through a limiter and low-pass filter. The band 1 frequency range becomes 50 kHz to 1.8 GHz. Band 2–5 input signals (1.7 GHz–21 GHz) are routed through the preselector. Table 8-2 lists the specification changes and additions to the standard instrument electrical characteristics.

Table 8-1

EXTENDED SERVICE AND WARRANTY OPTIONS

Option	Description
M1	Two routine calibrations to published specifications; one each in years two and three of warranty coverage
M2	Two years remedial service coverage in years four and five of product ownership
M3	Four years of routine calibrations; one each in years two, three, four, and five of product ownership
M4	Five routine calibrations to published specifications; one in year one and two each in years two and three — all calibrations certified.
M5	Nine routine calibrations to published specifications; one in year one and two each in years two through five, and two years remedial service coverage in years four and five — all calibrations certified.

Table 8-2
OPTION 01 ALTERNATE SPECIFICATIONS

Characteristic	Performance Requirement		Supplemental Information
FREQUENCY			
Frequency Response			
Coaxial (direct) Input	**About the midpoint between two extremes**	**Referenced to 100 MHz**	
Band and Freq Range			
1 (50 kHz–1.8 GHz)	±1.5 dB		
2 (1.7–5.5 GHz)	±2.5 dB	±3.5 dB	
3 (3.0–7.1 GHz)	±2.5 dB	±3.5 dB	
4 (5.4–18.0 GHz)	±3.5 dB	±4.5 dB	
5 (15.0–21.0 GHz)	±5.0 dB	±6.5 dB	
AMPLITUDE			
Spurious Responses			
3rd Order Intermodulation Products			
50 kHz to 21 GHz (Bands 1–5)	At least −70 dBc from any two on-screen signals within any frequency span		At least −100 dBc when signals are separated 100 MHz or more in preselected bands.

Table 8-2 (Continued)
OPTION 01 ALTERNATE SPECIFICATIONS

Characteristic	Performance Requirement						Supplemental Information
AMPLITUDE (Continued)							
Harmonic Distortion							
50 kHz to 1.8 GHz (Band 1)	−60 dBc or less						Measured at −40 dBm input level in Minimum Distortion Mode.
1.7 to 21 GHz	Not discernible						Typically −100 dBc
LO Emission	Less than −70 dBm to 21 GHz						With 0 dB RF Attenuation
INPUT							
Maximum Safe Input Level (Attenuator Maximum Rating)							+30 dBm (1 W) continuous, 75 W peak, pulse width 1 μs or less with a maximum duty factor of 0.001 (attenuator limit). DO NOT APPLY DC VOLTAGE TO THE RF INPUT. (See Optional Accessories for DC Block
SENSITIVITY	**Equivalent Input Noise in dBm versus Resolution Bandwidth**						Equivalent maximum input noise with internal preselection for each resolution bandwidth for frequency bands 1–5 (50 kHz–21 GHz), the NARROW Video filter is activated for resolution bandwidths of 1 kHz or less, and the WIDE filter for resolution bandwidths above 1 kHz.
Band and Frequency Range	**100 Hz**	**1 kHz**	**10 kHz**	**100 kHz[a]**	**300 kHz[a]**	**1 MHz**	
1 (50 kHz–1.8 GHz)	−119	−110	−100	−90	−85	−80	
2 (1.7–5.5 GHz)	−120	−110	−100	−90	−85	−80	
3 (3.0–7.1 GHz)	−119	−109	−99	−89	−84	−79	
4 (lower part) (5.4–12.0 GHz)	−105	−95	−85	−75	−70	−65	
4 (upper part) (12.0–18.0 GHz)	−100	−90	−80	−70	−65	−60	
5 (15.0–21.0 GHz)	−100	−90	−80	−70	−65	−60	
PHYSICAL							
Weight with standard accessories, except manuals	55 pounds, maximum						

Option 07 (75Ω Input)

Option 07 provides an optional 75Ω input, replacing the external mixer capability. Table 8-3 lists the changes and additions to the standard instrument electrical characteristics. These characteristics apply to the 75Ω Input.

[a] Option 07 replaces the 100 kHz filter with a 300 kHz filter.

Table 8-3
OPTION 07 ALTERNATE SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
Input Impedance		75Ω
Return Loss		
5 MHz to 800 MHz		17 dB (1.35:1 VSWR)
800 MHz to 1000 MHz		13 dB (1.6:1 VSWR) with ⩾10 dB attenuation
Maximum Input Level		
With 0 dB Attenuation		+75 dBmV
With 20 dB or More Attenuation		+78 dBmV, 100 V_{dc} maximum (dc + peak)
Center Frequency Operating Range		1 MHz to 1000 MHz
Static Resolution Bandwidth	Within 20% of 300 kHz bandwidth (6 dB down)	300 kHz resolution filter replaces the standard instrument 100 kHz filter.
Frequency Response 5 MHz to 1000 MHz Coaxial Input	±2.0 dB about the midpoint between two extremes	Frequency response is measured with ⩾10 dB RF attenuation. The response figure includes the effects of: •input vswr •mixer •gain variations Variations in display flatness contribute about 1 dB to the response figure.
1 MHz to 5 MHz		Typically <3 dB down from the 5 MHz response
Reference Level Range		+78 dBmV to −75 dBmV +88 dBmV is achievable in MIN NOISE mode
Equivalent Input Noise Sensitivity 5 MHz to 1000 MHz		See the main specifications and the Option 01 specifications for 300 kHz sensitivity with the 50Ω RF INPUT.
100 Hz	−74 dBmV	Typically −83 dBmV
1 kHz	−66 dBmV	Typically −73 dBmV
10 kHz	−56 dBmV	Typically −63 dBmV
300 kHz	−41 dBmV	Typically −48 dBmV
1 MHz	−36 dBmV	Typically −43 dBmV
Calibrator Output (CAL OUT) Level	+20 dBmV ±0.5 dB at 100 MHz ±10 PPM	100 MHz comb of markers provide amplitude calibration at 100 MHz and markers for frequency and span calibration
Output Impedance		75Ω nominal

Options 30 and 31 (Rackmount)

Option 30 provides the spectrum analyzer installed in a rackmount cabinet. External vibrations, from rack cooling fans or surrounding equipment, may lower the FM-characteristic. Because of different rack frame types, this lowering cannot be specified; in a typical fan-cooled rack, lowering increases by a factor of two.

Option 31 provides the cabling necessary to access all the front-panel connectors at the cabinet rear panel. Because of the extra cabling, lowering may occur in response flatness and sensitivity at the high end of the frequency range; above 3.0 GHz this is typically about 2 dB.

Installation Requirements. Information on installation requirements and installation procedures for Options 30 and 31 is not available at this time.

Option 52 (North American 220V)

Option 52 provides a North American 220 V configuration with the standard power cord. The fuses are replaced with 2A slow blow.

Table 8-5
OPTION 42 ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
110 MHz IF Output Center Frequency	108.5 MHz-111.5 MHz	
3 dB Bandwidth	> 5 MHz	
Bandpass Ripple	⩽ 0.5 dB	
Symmetry about 110 MHz	±1.0 MHz	
Power Output Band 1	⩽ 0 dBm	With −30 dB input and signal at full screen.
Band 5	⩾ −40 dBm	In MIN DISTORTION mode only. 1 dB compression of output ⩾ 0 dBm.

GLOSSARY

The following glossary is presented as an aid to better understand the terms as they are used in this document and with reference to spectrum analyzers.

GENERAL TERMS

Center Frequency. That frequency which corresponds to the center of a frequency span, expressed in hertz.

dBc. Decibels referenced to carrier level.

Effective Frequency Range. That range of frequency over which the instrument performance is specified. The lower and upper limits are expressed in hertz.

Frequency Band. A part of effective frequency range over which the frequency can be adjusted, expressed in hertz.

Full Span (Maximum Span). A mode of operation in which the spectrum analyzer scans an entire frequency band.

Zero Span. A mode of operation in which the frequency span is reduced to zero.

Envelope Display. The display produced on a spectrum analyzer when the resolution bandwidth is greater than the spacing of the individual frequency components.

BLine Display. The display produced on a spectrum analyzer when the resolution bandwidth is less than the spacing of the signal amplitudes of the individual frequency components.

Line Spectrum. A spectrum composed of signal amplitudes of the discrete frequency components.

Markers. The instrument uses three types of markers:

Waveform Markers. — When the Marker function is enabled, it provides a movable cursor with readout of frequency and amplitude at the marker position. When the delta marker mode is enabled, a second marker allows operations and readout between the two marker positions.

Update Marker. - Marks the current sweep position in a digital storage display as the display is being updated.

Video Markers. - Marker signals applied to the external VIDEOMARKER input from a Tektronix 1405 Television Sideband Analyzer. The Video Markers mark frequencies of interest on the television signal.

Maximum Safe Input Power

WITHOUT DAMAGE. The maximum power applied at the input which will not cause degradation of the instrument characteristics.

WITH DAMAGE. The minimum power applied at the input which will damage the instrument.

Intermodulation Spurious Response (Intermodulation Distortion). An unwanted spectrum analyzer response resulting from the mixing of the nth order frequencies, due to non-linear elements of the spectrum analyzer, the resultant unwanted response being displayed.

Baseline Clipper (Intensifier). Increasing the brightness of the signal relative to the baseline portion of the display.

Pulse Stretcher. A pulse shaper that produces an output pulse, whose duration is greater than that of the input pulse, and whose amplitude is proportional to that of the peak amplitude of the input pulse.

Signal Identifier. A means to identify the spectrum of the input signal when spurious responses are possible.

Spectrum Analyzer. An apparatus which is generally used to display the power distribution of an incoming signal as a function of frequency.

NOTE

It is useful in analyzing the characteristics of repetitive electrical waveforms in general, since repetitively sweeping through the frequency range of interest will display all components of the signal.

Video Filter. A post detection low-ORpass filter.

Scanning Velocity. Frequency span divided by sweep time and expressed in hertz per second.

FREQUENCY TERMS

Display Frequency. The input frequency as indicated by the spectrum analyzer and expressed in hertz.

Frequency Span (Dispersion). The magnitude of the frequency band displayed, expressed in hertz or hertz per division.

Frequency Linearity Error. The error of the relationship between the frequency of the input signal and the frequency displayed (expressed as a ratio).

Frequency Drift. Gradual shift or change in displayed frequency over the specified time due to internal changes in the spectrum analyzer, and expressed in hertz per second, where other conditions remain constant.

Residual FM (Incidental FM). Short term displayed frequency instability or jitter due to instability in the spectrum analyzer local oscillators, given in terms of peak-to-peak frequency deviation and expressed in hertz or percent of the displayed frequency.

Impulse Bandwidth. The displayed spectral level of an applied pulse divided by its spectral voltage density level assumed to be flat within the pass-band.

Static (Amplifier) Resolution Bandwidth. The specified bandwidth of the spectrum analyzer's response to a cw signal, if sweep time is kept substantially long.

NOTE

This bandwidth is the frequency separation of two down points, usually 6 dB, on the response curve, if it is measured either by manual scan (true static method) or by using a very low speed sweep (quasi-static method).

Shape Factor (Skirt Selectivity). The ratio of the frequency separation of the two (60 dB/6 dB) down points on the response curve to the static resolution bandwidth.

Zero Pip (Response). An output indication which corresponds to zero input frequency.

AMPLITUDE TERMS

Deflection Coefficient. The ratio of the input signal magnitude to the resultant output indication.

NOTE

The ratio may be expressed in terms of volts (rms) per division, decibels per division, watts per division, or any other specified factor.

Display Reference Level. A designated vertical position representing a specified input level.

NOTE

The level may be expressed in decibels (e.g., 1 mW), volts, or any other units.

Sensitivity. Measure of a spectrum analyzer's ability to display minimum level signals, at a given IF bandwidth, display mode, and any other influencing factors, and expressed in decibels (e.g., 1 mW).

Equivalent Input Noise Sensitivity. The average level of a spectrum analyzer's internally generated noise referenced to the input.

Display Flatness. The unwanted variation of the displayed amplitude over a specified frequency span, expressed in decibels.

Relative Display Flatness. The display flatness measured relative to the display amplitude at a fixed frequency within the frequency span, expressed in decibels.

NOTE

Display flatness is closely related to frequency response. The main difference is that the spectrum display is not recentered.

Frequency Response. The unwanted variation of the displayed amplitude over a specified center frequency range, measured at the center frequency, expressORed in decibels.

Display Law. The mathematical law that defines the input-output function of the instrument.

NOTE

The following cases apply:

1) **Linear** — A display in which the scale divisions are a linear function of the input signal voltage.

2) **Square law (power)** — A display in which the scale divisions are a linear function of the input signal power.

3) **Logarithmic** — A display in which the scale divisions are a logarithmic function of the input signal voltage.

Dynamic Range. The maximum ratio of the levels of two signals simultaneously present at the input which can be measured to a specified accuracy.

Display Dynamic Range. The maximum ratio of the levels of two non-harmonically related sinusoidal signals each of which can be simultaneously measured on the screen to a specified accuracy.

Gain Compression. Maximum input level where the scale linearity error is below that specified.

Spurious Response. A response of a spectrum analyzer wherein the displayed frequency does not conform to the input frequency.

Hum Sidebands. Undesired responses created within the spectrum analyzer, appearing on the display, that are separated from the desired response by the fundamental or harmonic of the power line frequency.

Noise Sidebands. Undesired response caused by noise internal to the spectrum analyzer appearing on the display around a desired response.

Residual Response. A spurious response in the absence of an input signal. (Noise and zero pip are excluded.)

Input Impedance. The impedance at the desired input terminal.

NOTE

Usually expressed in terms of vswr, return loss, or other related terms for low impedance devices and resistance- capacitance parameters for high impedance devices.

DIGITAL STORAGE TERMS

Digitally Stored Display. A display method whereby the displayed function is held in a digital memory. The display is generated by reading the data out of memory.

Digitally Averaged Display. A display of the average value of digitized data computed by combining serial samples in a defined manner.

Multiple Display Memory. A digitally stored display having multiple memory sections which can be displayed separately or simultaneously.

Clear (Erase). Presets memory to a prescribed state, usually that denoting zero.

Save. A function which inhibits storage update, saving existing data in a section of a multiple memory (e.g., Save A).

View (Display). Enables viewing of contents of the chosen memory section (e.g., "View A" displays the contents of memory A; "View B" displays the contents of memory B).

Max Hold (Peak Mode). Digitally stored display mode which, at each frequency address, compares the incoming signal level to the stored level and retains the greater. In this mode, the display indicates the peak level at each frequency after several successive sweeps.

Scan Address. A number representing each horizontal data position increment on a directed beam type display. An address in a memory is associated with each scan address.

Volatile/Non-volatile Storage. A volatile storage system is one where any total loss of power to the system will result in a loss of stored information. Non-volatile memory is not subject to the instrument power supply for its storage.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

Tektronix®
Committed to Excellence

MANUAL CHANGE INFORMATION

Date: 2-11-87 Change Reference: C2/287
Product: see below Manual Part No.: see below Product Group: 26

2754/2754P Service 1	070-6097-00
2755/2755P Service 1	070-6032-00

TEXT CHANGES

Page 6-41, Step 4, paragraph c, CHANGE TO READ:

c. Press <SHIFT> 0 and select item 6 from the menu; then press <SHIFT> 0, and select item 0 from the menu. Now select frequency display of 2nd LO (2). Readout will now indicate the 2nd LO frequency.

Tektronix®
Committed to Excellence

MANUAL CHANGE INFORMATION

Date: 12/14/87
Change Reference: C1/188
Product: 2754/2754P Service 1
Manual Part No: 070-6097-00
Product Group: 26

This modification adds the preselector to all instruments. In all manuals eliminate any reference to "Option 01".

Section 1 – GENERAL INFORMATION

*Add the following to the **"Product Description"***

The analyzer features:

•preselector and input limiter

Section 2 – SPECIFICATIONS

Replace the present Specifications Tables with the following:

Table 2-1
FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Center/Marker Frequency		
Operating Range		50 kHz to 21 GHz Tuned by the CENTER/MARKER FREQUENCY control or the DATA ENTRY keypad.
Accuracy (After front-panel CAL has been performed)		Center/Marker Freqeuncy Accuracy is specified by two characteristics: • initial accuracy (Firmware corrected) • center frequency drift during the sweep
Initial (start of sweep) Bands 1 & 5 with SPAN/DIV>200 kHz, and Bands 2—4 with SPAN/DIV >100 kHz (1st LO unlocked)	±[20%D + (CF x 10^{-5}) + 15N kHz] Where: D = SPAN/DIV or RESOLUTION BANDWIDTH , whichever is greater CF = Center/Marker Frequency N = Harmonic Number	Refer to 'IF, LO Range and Harmonic Number' specification for the N value. Allow a settling time of one second for each GHz change in CF within a band. In band 4, divide the CF change by N. Over operating temperature range (CF x 1.5 x 10^{-5})
Bands 1 & 5 with SPAN/DIV ≤200 kHz and Bands 2—4 with SPAN/DIV ≤100 kHz (1st LO locked)	±[20%D + (CF x 10^{-5}) Hz] Where: D = SPAN/DIV or RESOLUTION BANDWIDTH, whichever is greater CF = Center/Marker Frequency	

56-103

SERVICE MANAGER

247 MANUAL CHANGE

Table 2-1 (Continued)
FREQUENCY RELATED CHARACTERSTICS

Characteristic	Performance Requirement	Supplemental Information
Center Frequency Drift		With constant ambient temperature and fixed center frequency. Any error is observed during sweep time. Correction will occur at the end of sweep or as often as necessary to maintain specifications.
After 30 minute warmup Bands1&5 with SPAN/DIV >200 kHz and Bands 2—4 with SPAN/DIV >100 kHz (1st LO unlocked)		Typically ≤(25 kHz)N per minute.
Bands 1&5 with SPAN/DIV ≤200 kHz and Bands 2—4 with SPAN/DIV≤100 kHz (1st LO locked)		Typically ≤150 Hz per minute.
After 1 hour warmup Bands 1&5 with SPAN/DIV >200 kHz and Bands 2—4 with SPAN/DIV >100 kHz (1st LO unlocked)		Typically ≤(5 kHz)N per minute
Bands 1&5 with SPAN/DIV ≤200 kHz and Bands 2—4 with SPAN/DIV ≤100 kHz (1st LO locked)		≤50 Hz per minute of sweep time
Readout resolution		≤10% of SPAN/DIV to minimum of 1 kHz. 100 Hz in delta mode.

Table 2-1 (Continued)
FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Residual FM		Short term, after 1 hour warmup.
Bands 1 & 5 with SPAN/DIV >200 kHz and Bands 2—4 withSPAN/DIV >100 kHz (1st LO unlocked)	≤(7 kHz)N total excursion in 20 ms.	Refer to 'IF, LO Range, and Harmonic Number' specification for the N value.
Bands 1 & 5 with SPAN/DIV ≤200 kHz and Bands 2—4 with SPAN/DIV ≤100 kHz (1st LO locked)	≤(10+2N)Hz total excursion in 20 ms.	
Resolution Bandwidth (6 dB down)	Within 20% of selected bandwidth.	1 kHz to 1 MHz in decade steps.
Shape Factor (60 dB/6 dB)	7.5:1 or less	
Noise Sidebands	At least –73 dBc at an offset of 30 x resolution bandwidth	
Video Filter Narrow		Reduces video bandwidth to approximately 1/300th of the selected resolution bandwidth.
Wide		Reduces video bandwidth to approximately 1/30th of the selected resoultion bandwidth.
Pulse Stretcher Fall-Time		30 µs/division (±50%)

Table 2-1 (Continued)
FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Frequency Span/Div		
Overall Range		
With SPAN/DIV control		200 Hz to 1 GHz (in a 1-2-5 sequence)
With the DATA ENTRY Keypad.		200 Hz to 1.2 GHz (to two significant digits)
Minimum Span/Div		200 Hz in all bands.
Maximum Span/Div		With SPAN/DIV Control / With DATA ENTRY Keypad
Band 1 (0—1.8 GHz)		100 MHz / 170 MHz
Band 2 (1.7—5.5 GHz)		200 MHz / 370 MHz
Band 3 (3—7.1 GHz)		200 MHz / 400 MHz
Band 4 (5.4—18 GHz)		1 GHz / 1.2 GHz
Band 5 (15—21 GHz)		500 MHz / 590 MHz
		In addition, MAX SPAN sweeps across an entire band and ZERO SPAN provides a 0 Hz display. With ZERO SPAN the horizontal axis is calibrated in time/div instead of frequency/div.
Accuracy/Linearity	Within 5% of the selected Span/Div	Measured over center 8 divisions.
IF Frequency, LO Range, and Harmonic Number (N)		1st IF (MHz) / LO Range (MHz) / (N)
Band and Freq. Range		
1 (0—1.8 GHz)		2072 / 2072—3872 / 1-
2 (1.7—5.5 GHz)		829 / 2529—6329 / 1 -
3 (3.0—7.1 GHz)		829 / 2171—6271 / 1 +
4 (5.4—18 GHz)		829 / 2072—6276 / 3 -
5 (15—21 GHz)		2072 / 4309—6309 / 3 +
Marker Accuracy	Identical to Center Frequency Accuracy	For the live trace
ΔMKR Accuracy	1% of total span	

Table 2—2
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Vertical Display Modes		10 dB/Div, 2 dB/Div, and Linear. Any integer between 1—15 dB/Div can also be selected via the DATA ENTRY keypad.
Display Dynamic Range		80 dB maximum for Log Mode 8 divisions for Linear Mode.
Display Amplitude Accuracy 10 dB/DIV Mode	±1.0 dB/10 dB to a maximum cumulative error of ±2.0 dB over 80 dB range	
2 dB/DIV Mode	±0.4 dB/2.0 dB to a maximum cumulative error of ±1.0 dB over 16 dB range	
LIN Mode	±5% of full scale	
Reference Level		Top of the graticule
Range Log Mode (With 0 Reference Level offset)		From –117 dBm to +40 dBm; +40 dBm includes 10 dB of IF gain reduction (+30 dBm is the maximum safe input). Alternate reference levels are: •dBV (–130 dBV to +27 dBV) •dBmV (–70 dBmV to +87 dBmV) •dBμmV (–10 dBμV to +147 dBμV)
LIN Mode		39.6 nV/Div to 2.8 V/Div (1W maximum safe input)
Steps 10 dB/DIV Mode		10 dB for the coarse mode. 1 dB for the FINE mode.
2 dB/DIV Mode		1 dB for the coarse mode. 0.25 dB for the FINE mode.
LIN Mode		1-2-5 sequence for coarse mode. 1 dB equivalent steps for FINE mode.
Set via DATA ENTRY Keypad		Steps correspond to the display mode in coarse, but 2 dB/DIV where steps are 1 dB. In FINE mode: 1 dB when the mode is 5 dB/Div or more 0.25 dB for display modes of 4 dB/Div or less (referred to as ΔA mode)

Table 2-2 (Continued)
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Reference Level (continued)		Dependent on the following characteristics:
Accuracy		•RF Attenuation Accuracy •IF Gain Accuracy •Resolution Bandwidth •Frequency Response •Display Mode •Calibrator Accuracy •Frequency Band •<SHIFT> CAL routine reduces error between resolution bandwidths at –20 dBm REF LEVEL. Other REF LEVELs may have larger errors. •Temperature variation (±0.15 dB/°C maximum)
Marker/s Accuracy (Normal or Δ mode)		Identical to REF LEVEL accuracy plus cumulative error of display scale (Dependent on vertical position)
RF Attenuator Range		0—60 dB in 10 dB steps
Accuracy Dc to 1.8 GHz	Within 0.5 dB/10 dB to a maximum of 1 dB over the 60 dB range	
1.8 GHz to 18 GHz	Within 1.5 dB/10 dB to a maximum of 3 dB over the 60 dB range	
18 GHz to 21 GHz	Within 3.0 dB/10 dB to a maximum of 6 dB over the 60 dB range	
IF Gain Range		87 dB of gain increase, 10 dB of gain decrease (MIN NOISE mode), in 10 dB and 1 dB steps.
Accuracy 1 dB Step	≤ 0.2 dB/dB step to 0.5 dB/9 dB steps except at the decade transitions.	
Decade Transitions –29 to –30 dBm –39 to –40 dBm –49 to –50 dBm –59 to –60 dBm	0.75 dB or less	Maximum 1 dB cumulative error over 10 dB. Measured in MIN NOISE mode.
Maximum Deviation over the 97 dB Range	±2 dB	

Table 2-2 (Continued)
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement		Supplemental Information
Gain Variation Between Resolution Bandwidths			Measurement conditions: •Measured at –20 dBm •MIN DISTORTION mode •After CAL routine @ ambient temp.
With respect to the 1 MHz Filter	±0.4 dB		
Between Any Two Filters	≤0.8 dB		
Frequency Response			Measured with 10 dB RF Attenuation and Peaking optimized for each center frequency setting (when applicable). Response is affected by: •input VSWR •harmonic number (N) •gain variation •mixer •preselector Digital Storage typically increases errors by ±0.5% Display flatness is typically 1 dB greater than frequency response. Refer to the Options portion of this EIS for variations in this specification.
Band and Frequency Range	About the mid-point between two extremes	Referenced to 100 MHz	
1 (50 kHz—1.8 GHz)	±2.0 dB	±3.0 dB	
2 (1.7—5.5 GHz)	±3.0 dB	±4.0 dB	
3 (3.0—7.1 GHz)	±3.0 dB	±4.0 dB	
4 (5.4—18 GHz)	±4.0 dB	±5.0 dB	
5 (15—21 GHz)	±5.5 dB	±7.0 dB	

Table 2-2 (Continued)
AMPLITUDE RELATED CHARACTERISTIC

Characteristic	Performance Requirement	Supplemental Information
Differential Amplitude Measurement		ΔA mode provides differential measurements in 0.25 dB increments. (This is not related to the ΔMKR mode.)
Range		Maximum range of 48 dB dependent on Reference Level when ΔA mode is activated. DO NOT USE ΔA mode outside the –117 dBm to +30 dBm Reference Level
Accuracy		Difference / Steps / Error 0.25 dB / 1 / 0.15 dB 2 dB / 8 / 0.4 dB 10 dB / 40 / 1.0 dB 48 dB / 192 / 2.0 dB
Spurious Responses Residual	–95 dBm or less	No input signal, 0 dB RF Attenuation and fundamental mixing Bands 1—3. Input teminated in 50Ω.
3rd Order Intermodulation Products	–70 dBc or less	From any two on–screen signals within any frequency span. In MIN DISTORTION mode.
Harmonic Distortion 50 kHz to 21 GHz	–60 dBc or less	Measured at –40 dBm input level in MIN DISTORTION mode.
LO Emissions	Less than –70 dBm to 21 GHz	With 0 dB RF Attenuation.

Characteristic	Performance Requirement					Supplemental Information
Sensitivity	Equivalent Input Noise in dBm vs. Resolution Bandwidth					Equivalent maximum input noise for each resolution bandwidth. Measured at 25° C with: • 0 dB attenuation (Min Atten 0 dB) • Narrow Video Filter on • Vertical Display 2dB/Div • Digital Storage on • Max Hold off • Peak/Average in Average • 1 sec Time/Div • Zero Span • Input terminated in 50Ω
Frequency Range	1 kHz	10 kHz	100 kHz	300 kHz[a]	1 MHz	
Band 1 50 kHz—1.8 GHz	–110	–100	–90	–85	–80	
Band 2&3 1.7 GHz—5.5 GHz & 3.0 GHz —7.2 GHz	–108	–98	–88	–83	–78	
Band 4 5.4 GHz—12 GHz	–94	–84	–74	–69	–64	
Band 4 12 GHz—18 GHz	–89	–79	–69	–64	–59	
Band 5 15 GHz—21 GHz	–88	–78	–68	–63	–58	

[a]Option 07 replaces the 100 kHz filter with a 300 kHz filter.

Table 2-3
INPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
RF INPUT		Type N female connector, specified to 21 GHz. (See Option 07 for supplemental specifications concerning an additional 75Ω input.)
Impedance		50 Ω
VSWR With RF Attenuation ≥10 dB 50 kHz—2.5 GHz		1.3:1 (typically 1.2:1)
2.5—6 GHz		1.7:1 (typically 1.5:1)
6—18 GHz		2.3:1 (typically 1.9:1)
18—21 GHz		3.5:1 (typically 2.7:1)
VSWR With 0 dB RF Attenuation		Measured within 3 MHz of the center of the preselector on Bands 2, 3, 4, and 5.
50 kHz—6 GHz		Typically 1.9:1
6—18 GHz		Typically 2.3:1
18—21 GHz		Typically 3.0:1
Maximum Safe Input (Attenuatior Maximum Rating)		+30 dBm (1 W) continuous, 75 W peak • Pulse Width = 1μs or less • Maximum duty factor of 0.001(attenuator limit) DO NOT APPLY DC VOLTAGE TO THE RF INPUT.
1 dB Compression Point (Minimum)		0 RF Attenuation.
MIN DISTortion mode	–23 dBm	
MIN NOISE mode	–13 dBm	
Optimum RF Input Level for Linear Operation		–30 dBm, referenced to the input mixer. This is achieved in MIN DISTORTION mode when not exceeding full screen display.

Table 2-3 (Continued)
INPUT SIGNAL CHARACISTISIC

Characteristic	Performance Requirement	Supplemental Information
HORIZ|TRIG		Dc coupled input for external horizontal drive (selected by the EXT position of the TIME/DIV control) and ac coupled input for external trigger signals (selected at other positions of the TIME/DIV control).
Sweep Input Voltage Range		0 to +10V (dc + peak ac) for full screen deflection
Trigger Input Voltage Range		
Minimum	At least 1.0 V peak from 15 Hz to 500 kHz	Typically 1.0 MHz at 1.5 V peak.
Maximum		
dc + peak ac		50V
ac		30V $_{rms}$ to 10 kHz, then derate linearly to 3.5V $_{rms}$ at 100 kHz and above.
Pulse Width		0.1 µs minimum
MARKER|VIDEO		External Video input or External Video Marker input, switched by pin 1 of the ACCESSORIES connector.
MARKER Input Level		0 to –10V Interfaces with TEKTRONIX 1405 Sideband Adapter.
VIDEO Input Level		0 to + 4 V for full screen display with pin 1 of the ACCESSORIES connector low

Table 2-3 (Continued)
INPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
ACCESSORY Connector (J104)		25–pin connector (Not RS–232 compatible) Provides bi–directional access to the instrument bus. Also provides external Video select. All lines are TTL compatible, except 2 and 3. Maximum voltage on all lines is ±15V.
Pin 1		External Video Select Low selects External VIDEO Input. High (default) selects Video MARKER Input.
Pin 2		External Preselector Drive — Drive signal for an external preselector. Output voltage is proportional to center frequency.
Pin 3		External Preselector Return — Ground return for the External Preselector signal.
Pin 4		Internal Control. High (default) selects internal control. Instrument bus lines are output at the ACCESSORIES connector. Low selects External control. Instrument bus lines at the ACCESSORIES connector accept input from an external controller.
Pin 5		Chassis Ground
Pins 6–13 [a]		Instrument Bus Address lines 7– 0[a]
Pin 14 [a]		Instrument Bus Data Valid signal[a]
Pin 15 [a]		Instrument Bus Service Request signal[a]
Pin 16 [a]		Instrument Bus Poll signal[a]
Pin 17		Data Bus Enable input signal for external controller. High (unasserted) disables external data bus. Low enables external data bus.
Pins 18–25		Instrument Bus Data lines 0–7 Active when External Data Bus Enable (pin 17) is low.

[a] Output when internally controlled (pin 4 high) and input when externally controlled (pin 4 low).

Table 2-4
OUTPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Calibrator (CAL OUT)	–20 dBm ±0.3 dB at 100 MHz ±10 PPM*	100 MHz comb of markers provide amplitude calibration at 100 MHz and markers for frequency and span calibration to 1.0 GHz
1st LO and 2nd LO OUTPUTs		Provide access to the output of the respective local oscillators. THESE PORTS MUST BE TERMINATED IN 50 Ω AT ALL TIMES.
1st LO OUTPUT Power		≥+6.0 dBm
2nd LO OUTPUT Power		–22 dBm to 0 dBm.
VERT Output		Provides 0.5V ±5% (open circuit) of signal per division of video that is above and below the centerline. Full range –2.0V to +2.0V. Source impedance is approximately 1kΩ.
HORIZ Output		Provides 0.5V/Div (open circuit) either side of center. Full range –2.5V to +2.5V. Source Impedance is approximately 1kΩ.
PEN LIFT		TTL compatible, nominal +5V to lift plotter pen.
10 MHz IF Output		Provides access to the 10 MHz IF signal. Output level is approximately –5 dBm for a full screen signal at –30 dBm reference level. Normal impedance is approximately 50Ω
IEEE STD 488 PORT		In accordance with IEEE 488–78 standard and Tektronix Codes and Formats standard (version 81.1).
P Version		Implemented as SH1, AH1, T5, L3, SR1, RL1, PP1, DC1, DT1, and C0.
Non-P Version (Plotter Output)		Implemented as SH1, AH0, T3, L0, SR0, RL0, PP0, DC0, DT0, and C0.
PROBE POWER		Provides operating voltages for active probes.
Outputs		
Pin 1		+5V at 100 mA maximum
Pin 2		Ground
Pin 3		–15V at 100 mA maximum
Pin 4		+15V at 100 mA maximum
ACCESSORIES (J104)		All inputs and outputs are listed in Table 2-3 Input Signal Characteristics.

* Over the operating temperature range this is +15 PPM

Table 2-5
DISPLAY CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Sweep		Triggered, auto, manual, and external
Sweep Time	20 µs/Div to 5 s/Div in 1-2-5 sequence (10 s/Div available in AUTO)	
Accuracy	±5% over center 8 divisions	
Triggering		INTERNAL, EXTERNAL, FREE RUN, and LINE.
Internal Trigger Level	2 divisions or more of signal	
EXTERNAL Trigger Input Level	1.0V peak, minimum	EXTERNAL is ac-coupled (15 Hz—500 kHz). Maximum external trigger input is 50V (dc + peak ac).

Table 2-6
GENERAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information		
Video Bandwidth		Resolution Bandwidth	WIDE	NARROW
		1 MHz	30 kHz	3 kHz
		100 kHz	3 kHz	300 Hz
		10 kHz	300 Hz	30 Hz
		1 kHz	30 Hz	3 Hz
Crt Readout		Displays all parameters listed on the crt bezel, plus operating messages.		

Table 2-6 (Continued)
GENERAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Battery-Powered Memory		Instrument settings, displays, calibration offsets, and preselector peaking codes for each band are stored in battery powered non-volatile RAM.
Battery Life		
At +55°C Ambient Temperature		1—2 years
At +25°C Ambient Temperature		
Lithium (Standard)		At least 5 years
Temperature Range for Retaining Data		
Operating		0°C to +50°C
Non-Operating		–30°C to +75°C

Table 2-7
POWER REQUIREMENTS

Characteristics	Performance Requirement	Supplemental Information
Line Frequency Range	47—63 Hz	47 Hz to 440 Hz. Operation over 63 Hz exceeds protective grounding conductor leakage current of 3.5 mA. A redundant protective grounding means is essential to prevent against electric shock
Line Voltage Range	90 V_{ac} to 132 V_{ac}	115 V nominal
	180 V_{ac} to 250 V_{ac}	230 V nominal
Line Fuse		
115V Nominal		4A
230V Nominal		2A Medium-Blow
Input Power	210 W maximum (3.2A)	At 115V and 60 Hz
Leakage Current		5 mA maximum

Table 2-7
ENVIRONMENTAL CHARACTERISTICS

Meets MIL T-28800C, type III class 5, style E specifications.

Characteristic	Description	
Temperature		
Operating	0°C to +50°C	
Non–operating[a]	–40°C to +75°C	
Humidity		
Operating	95% ±5% below +30°C. 75% ±5% above +30°C. 45% ±5% above +40°C.	
Altitude		
Operating	10,000 feet (3050 meters)	
Non–operating	40,000 feet (120000 meters)	
Vibration, Operating (instrument secured to a vibration platform during test)	MIL–Std–810D, METHOD 514 Procedure I (modified). Resonant searches in all three axes at 0.013 inch displacement for 15 minutes. Dwell for an additonal 10 minutes in each axis at the frequency of the major resonances or at 33 Hz if none was found. Resonance is defined as twice the input displacement. Total vibration time is 75 minutes.	
Shock (Operating and Non–operating)	Three guillotine–type shocks of 30g, one–half sine, 11 ms duration each direction along each major axis; total of 18 shocks.	
Electromagnetic Interference (EMI)	Meets requirements described in MIL–Std–461B Part 4, except as noted.	
	Test Method	Remarks
Conducted Emissions	CE01–60 Hz to 15 kHz	1 kHz to 15 kHz only
	CE03–15 kHz to 50 MHz power leads	15 kHz to 50 kHz, relaxed by 15 dB
Conducted Susceptibility	CS01–30 Hz to 50 kHz power leads	Full limits
	CS02–50 kHz to 400 MHz power leads	Full limits
	CS06–spike power leads	Full limits

[a] After storage at temperatures below –15°C, the instrument may not reset when power is first turned on. If this happens, allow the instrument to warm up for at least 15 minutes, then turn POWER OFF for 5 seconds and back ON.

Table 2-7 (Continued)
ENVIRONMENTAL CHARACTERISTICS

Characteristic	Description	
Electromagnetic Interference (EMI) (Continued)	Test Method	Remarks
Radiated Emissions	RE01–30 Hz to 50 kHz magnetic field (measured at 30 cm).	Exceptioned, 30 kHz to 36 kHz
	RS02–14 kHz to 10 GHz	Full limit
Radiated Susceptibility	RS01–30 Hz to 50 kHz	Full limit
	RS02–Magnetic Induction	To 5 A only, 60 Hz
	RS03–14 kHz to 10 GHz	Up to 1 GHz, 1 V/m

Table 2-8
PHYSICAL CHARACTERISTICS

Characteristic	Description
Weight	60 lbs. (27 kg) Including cover and standard accessories, except manuals.
Dimensions	7.0 X 17.0 X 25.0 inches (17.8 X 43.2 X 63.5 cm)

Section 4 – PERFORMANCE CHECK PROCEDURE

Change the following sections as indicated.

Initial Power–Up

c. The operating functions and modes should initialize to the following "power up" state:

FREQ RANGE 0—1.8

8. Check Noise Sidebands

Change the specification statement (after the above title) to read:

(–73 dBc or more at 30 times the resolution bandwidth)

Change the following steps to read:

b. Check that the amplitude of the noise sidebands is 53 dBc or more down from the reference level at 30 times the resolution bandwidth (3 divisions away from the center frequency position). See Figure 4–9.

d. Check that the amplitude of the noise sidebands 30 kHz away from the center frequency position is at least 73 dB below the signal level or 55 dB below the top of the screen.

9. Check Frequency Response

Replace this step with the following:

Response, about the midpoint of the two extremes, is:

±2.0 dB from 50 kHz to 1.8 GHz; ±3.0 from 1.7 to 7.1 GHz; ±4.0 dB from 5.4 to 18 GH; and ±5.5 dB from 15 to 21 GHz. Response with respect to 100 M Hz is: ±3.0 dB from 50 kHz to 1.8 GHz; ±4.0 dB from 1.7 to 7.1 GHz; ±5.0 dB from 5.4 to 18 GHz; and ±7.0 dB from 15 to 21 GHz.

Frequency response is the peak–to–peak variation of the display amplitude over a specified center frequency range, measured at the center frequency. It is measured with 10 dB of RF attenuation, with Peaking optimized, for those bands that are applicable, for each center frequency setting. Response includes the effect of input vswr, mixing mode (N), gain variation, and preselector or mixer. Digital storage may increase errors by 0.5%.

Accurate measurement requires many small incremental checks across the frequency range. The response at each check point, above band 1 should be peaked with MANUAL PEAK or by activating the AUTO PEAK mode.

NOTE

Loss of signal through interconnecting cables becomes significant above 1 GHz; therefore, short (25 inch or less) semi–rigid cable with precision fittings to interconnect the test equipment should be used. Precise matching terminations and power dividers are also used to minimize reflections.

To expedite the measurement, this procedure uses a leveled output sweep oscillator rather than incremental checks. Digital storage is also used to provide a complete display of the sweep frequency. VIEW A, VIEW B and MAX HOLD are reactivated for each sweep.

a. Test equipment setup is shown in Figure A. Set the FRQUENCY to 5 MHz, FREQ SPAN/DIV to 1 MHz, TIME/DIV to 20 ms, REF LEVEL to 0 dBm, and MIN RF ATTEN to 30 dB. Activate 1 dB/div and AUTO RESOLN.

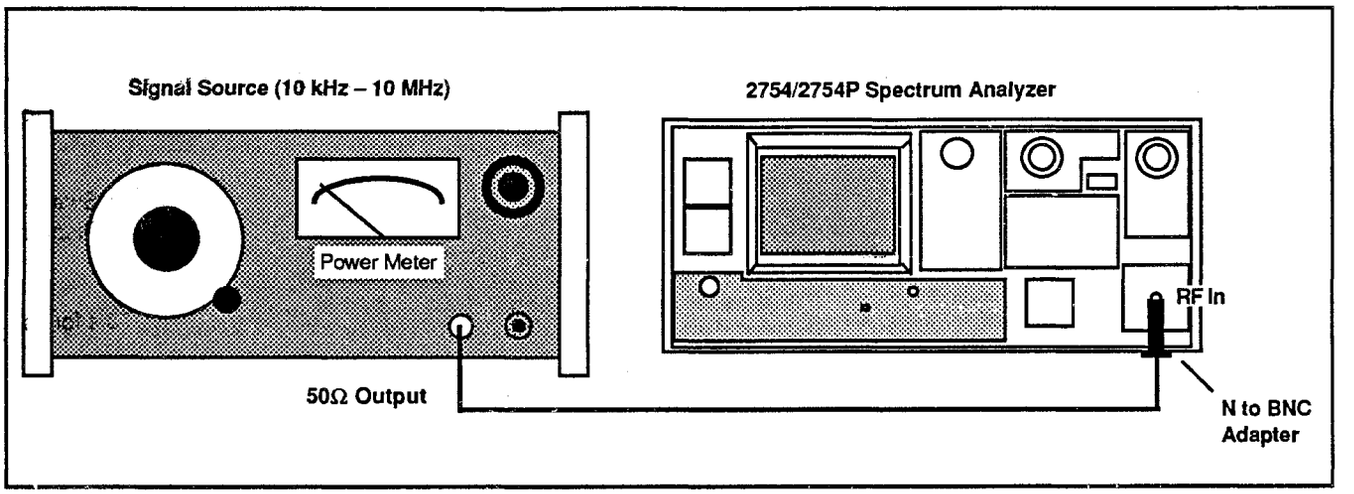


Figure A. Test equipment setup for measuring 10 kHz to 10 MHz frequency response

b. Apply the output of a constant level and calibrated 50 kHz to 10 MHz Signal Generator to the RF INPUT of the instrument. Set the generator frequency to 100 kHz and its output for about –10 dBm.

c. Adjust the REF LEVEL so the amplitude of the 100 kHz signal is about half screen, in the 2 dB/DIV mode. Activate VIEW A. SAVE A, and MAX HOLD.

d. Slowly tune the Signal Generator frequency from 50 kHz to 10 MHz, monitoring the output to ensure it remains constant. Note the frequency response (amplitude deviation above and below the average). Frequency response or amplitude deviation must not exceed ±2.0 dB from 50 kHz to 10 MHz (See Figure B for a typical display).

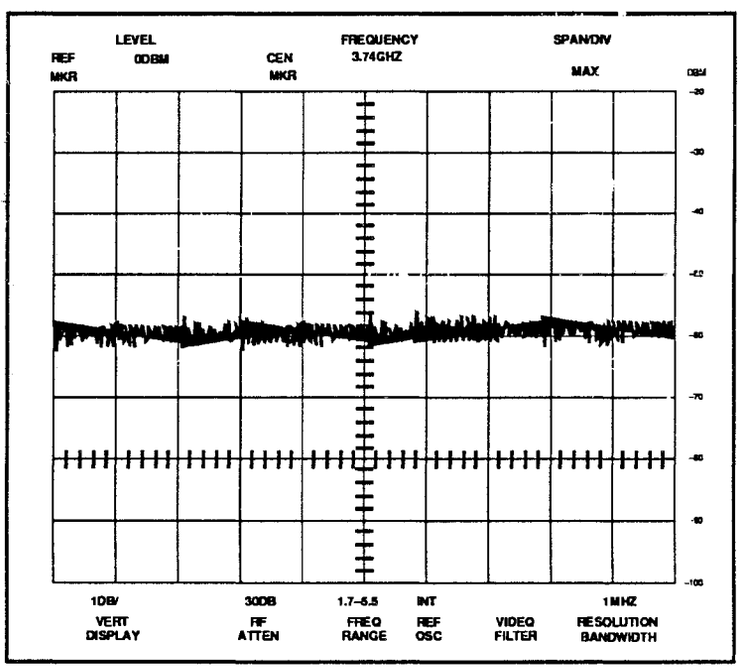


Figure B. Display showing frequency response pattern from a sweeping source

e. Replace the 50 kHz to 10 MHz signal source with a 0.01 to 2.4 GHz sweep oscillator and connect the test equipment as shown in Figure C. The output of the Sweep Generator is applied through a 3 dB attenuator and high performance coaxial cable to a power divider. Connect one output of the power divider to the RF INPUT of the instrument and the other output to the sensor for the power meter or to the ALC input of the sweep oscillator.

f. Change the FREQ SPAN/DIV to 200 MHz and the FREQUENCY to approximately 1.0 GHz. On the Sweep Generator, select a 1 GHz cw marker and adjust the output for a –6 dBm reading on the power meter. With the Vertical Display in the 2 dB/DIV mode, adjust the REF LEVEL so the signal amplitude is about half screen.

g. Change the Sweep Generator sweep mode to Automatic Internal Sweep and set the Sweep Time to 100 s for its slowest sweep time.

h. Check the frequency response over the 10 MHz to 1.8 GHz span. Deviation must not exceed ±2.0 dBm (refer to Figure B).

i. Change the FREQUENCY to 2.0 GHz and the FREQ SPAN/DIV to 100 MHz. Switch the Sweep Generator CW Marker on, and set it to 2.0 GHz. Peak the signal response of the instrument with the MANUAL PEAK control or activate AUTO PEAK.

j. Return the Sweep Generator to its Sweep mode and set the Start/Stop markers for 1.5 and 2.5 GHz. Sweep the 1.7 to 2.5 GHz span for Band 2 and note the frequency response. Frequency response or deviation must not exceed 3.0 dB

NOTE

If any segment or portion of the span fails to meet the specification, set the FREQUENCY to the center of this position; apply a cw marker at this frequency and re–peak with the MANUAL PEAK or AUTO PEAK mode. Decrease the FREQ SPAN/DIV to display that portion and then recheck the frequency response for this position.

k. Replace the sweep source with a sweep oscillator that covers the frequency range to 21 GHz. Connect the test equipment as shown in Figure C. On the RF plug–in, switch the ALC to Mtr position and connect a coaxial cable between the Recorder Output of the power meter and the Ext ALC input of the plug–in unit. Decrease the Power Level to approximately –6 dBm then adjust the Gain for a stable operation (output stops oscillating).

l. Set the FREQ SPAN/DIV to 200 MHz and the FREQUENCY to 4.0 GHz. Re–peak the response with the peaking controls, then sweep the upper portion of band 2 and check frequency response. If necessary, recheck those portions that do not meet specification after peaking the response at the center of those portion of the frequency spectrum.

m. Increase the FREQUENCY RANGE to the 3.0 to 7.2 GHz band. Tune the CENTER FREQUENCY to approximately 5.0 GHz. Apply a 5.0 GHz cw marker and peak the response. Activate MAX SPAN and check the frequency response by sweeping the 3.0 to 7.2 GHz frequency range. It may be necessary, if the response does not meet the 3.0 dB performance, to again peak the response at the center of those portions that do not meet specifications and recheck frequency response in smaller segments.

n. Repeat the foregoing procedure to check the response of the remaining bands to 21 GHz. Frequency response for band 4 (5.4–18 GHz) is ±4.0 dB and ±5.5 dB for band 5 (15.0–21.0 GHz).

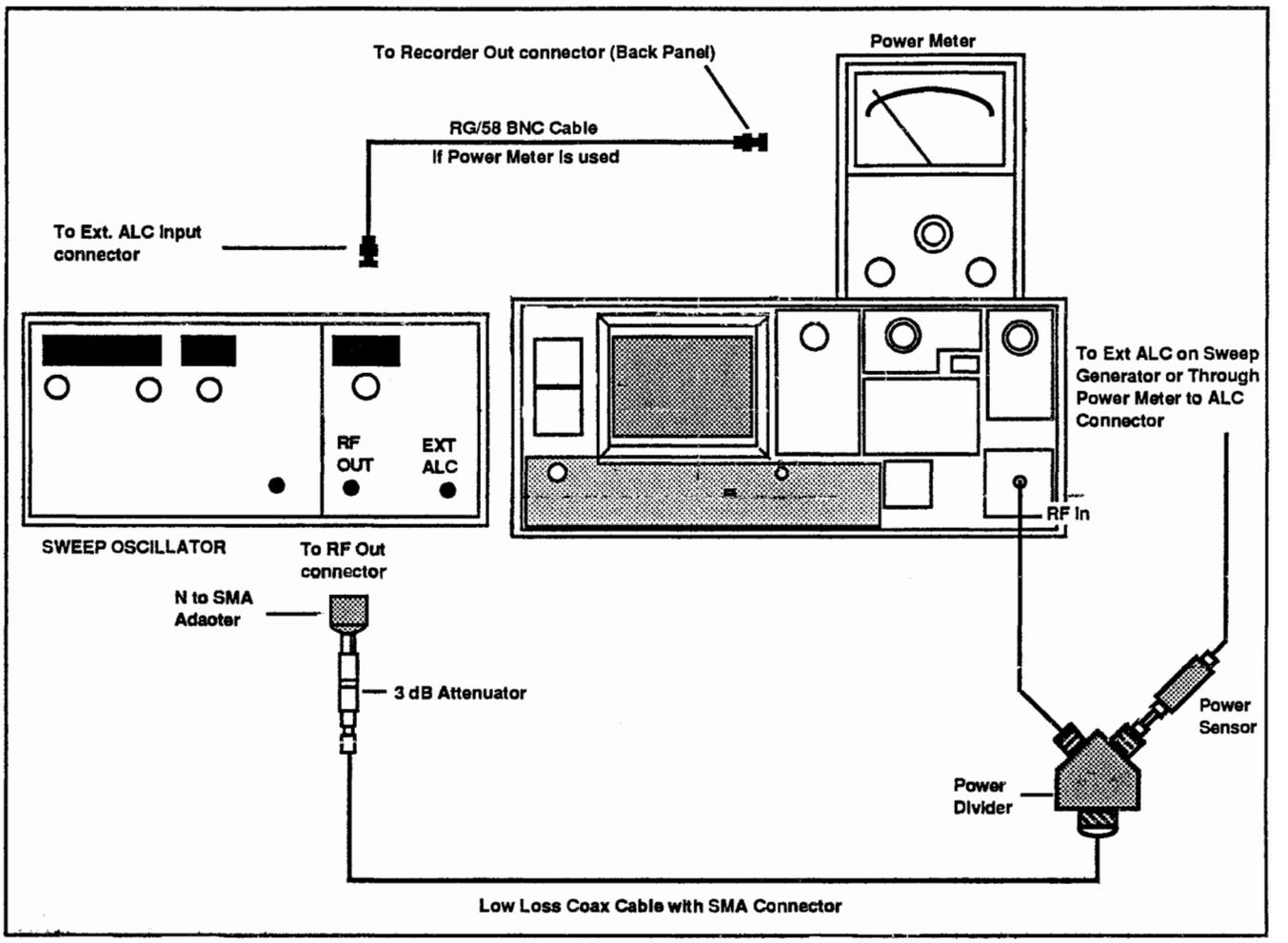


Figure C. Test equipment setup for measuring .01 to 21 GHz frequency response

11. Check Preseleetor Ultimate Rejection

Change the first paragraph to read:

This is a check of preselector operation, not a performance requirement specification.

13. Check IF Gain Accuracy

Change the specification statement to read:

(±0.2 dB/dB to a maximum of ±0.5 dB/9 dB except at the decade transitions of –29 dBm to –30 dBm, –39 dBm to –40 dBm, –49 dBm to –50 dBm, and –59 dBm to –60 dBm where an additional 0.75 dB can occur for a total of 1.25 dB/ decade. Maximum deviation over the full 97 dB range is within ±2 dB, measured in Min Noise mode)

e. Switch the REF LEVEL from –10 dBm to –20 dBm in 1 dB steps, adding 2 dB of external attenuation at each step. Note incremental accuracy and the 10 dB gain accuracy. Incremental accuracy must be within 0.2 dB/dB (0.5 minor division). Maximum cumulative error must not exceed 0.5 dB (1.5 minor division) except when stepping from the 9 dB to 10 dB increment, where the error could be an additional 0.75 dB. This exception does not apply when stepping from –69 to –70 dBm, –79 to –80 dBm, etc.

15. Check Sensitivity

Substitute the following for Table 4–9

Table 4–9
SENSITIVITY
EQUIVALENT INPUT NOISE (dBm) VERSUS RESOLUTION BANDWIDTH

Band/Frequency	1 MHz	300 kHz[b]	100 kHz	10 kHz	1 kHz
Band 1 50 kHz—1.8 GHz	–80	–85	–90	–100	–110
Band 2&3 1.7 GHz—7.2 GHz	–78	–83	–88	–98	–108
Band 4 5.4 GHz—12 GHz	–64	–69	–74	–84	–94
Band 4 12 GHz—18 GHz	–59	–64	–69	–79	–89
Band 5 15 GHz—21 GHz	–58	–63	–68	–78	–88

[a] Equivalent maximum input nosie (average noise for each resolution bandwidth with internal mixer).

[b] Option 07 replaces the 100 kHz filter with a 300 kHz filter.

Change the body as follows.

a. Remove the CAL OUT signal from the RF INPUT, and terminate the RF INPUT with its characteristic impedance (50Ω). Set the Spectrum Analyzer controls as follows:

FREQ RANGE 0—1.8 GHZ

b. Check that the noise floor (level) is down 80 dB or more as per Table 4–9 (30 dB down or more from the –50 dBm REF LEVEL).

d. Check that the noise floor (level) is down 90 dB or more as per Table 4–9 (40 dB down or more from the –50 dBm REF LEVEL).

f. Check that the noise floor (level) is down 100 dB or more as per Table 4–9 (50 dB down or more from the –50 dBm REF LEVEL).

h. Check that the noise floor (level) is down 110 dB or more as per Table 4–9 (60 dB down or more from the –50 dBm REF LEVEL).

16. Check Residual Spurious Response

Change the specification statement as follows:

(With no input signal, –95 dBm or less, with reference to the mixer input and fundamental mixing for Bands 1–3)

Change step b. as follows:

b. Scan the frequency range of bands 1, 2 or 3 in 100 MHz increments Note the amplitude of any spurious response. Spurii amplitude must not exceed –95 dBm (Push <SHIFT> STEP SIZE. This allows changing center frequency in 50 MHz increments by use of the +STEP function.)

19. Check LO Emission

Change the specification statement as

(–70 dBm or less to 21 GHz)

Change step c. as follows:

c. Check for any indication of LO emission. LO emission must be less than –70 dBm.

20. Check 1 dB Compression Point

Change the specification statement as follows:

[–23 dBm (MIN DIST mode). Bands 1 through 5]

Change step e. and k. as follows:

e. Set the test spectrum analyzer controls as follows:

Ref Level –23 dBm

k. Check that the 1 dB compression point occurs at –23 dBm or less (23 dB or less attenuation between the generator and the RF INPUT).

SECTION 7 – THEORY OF OPERATION

Change the following sections as indicated.

Frequency Control Section

Change the third paragraph to read:

The frequency control section also tunes the preselector so it tracks the signal frequency being detected over the 1.7 to 21 GHz range.

DETAILED DESCRIPTION

1ST CONVERTER SECTION (Diagram 2)

*Change the **Preselector Circuit** section to read:*

Preselector Circuits

FREQUENCY CONTROL SECTION (Diagram 7)

*Change the **Preselector Driver** section to read:*

Preselector Driver

The Preselector Driver combines the FINE TUNE VOLTS signal, from the Center Frequency Control board with the PRESELECTOR DIRVE signal and the SPAN VOLTS signal from the 1st LO Driver. This combined signal is offset, to compensate for the selected 1st IF, then shaped so the Preselector tracks with the 1st or 2nd LO as it is tuned by the output current. The Preselector Driver also drives the Filter Select switch that selects either the Preselector or the Low–pass Filter, depending on the frequency band selected.

SECTION 8 — OPTIONS

*Delete the section that refers to **Option 01 (Preselector)** and **Table 8–2 OPTION 01 ALTERNATE SPECIFICATIONS.***