



PLEASE CHECK FOR CHANGE INFORMATION
AT THE REAR OF THIS MANUAL.

TG 501 TIME MARK GENERATOR

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-1576-02

Serial Number _____

First Printing OCT 1978

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols As Marked on Equipment



DANGER — High voltage.



Protective ground (earth) terminal.



ATTENTION — refer to manual.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the

power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Plug-In Unit Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.



SPECIFICATION

INTRODUCTION

Description

The TG 501 is a general purpose Time Mark Generator plug-in designed to operate in a TM 500 Series Power Module. A Variable Timing Readout provides a simple but accurate means of measuring timing errors over $\pm 7.5\%$ minimum range. Since many specifications are given in percentages, the error readout eliminates the need for computations and, additionally, lessens parallax discrepancies.

Marker selection from 5 s through 1 ns in a 1, 2, 5, sequence is available. 5 s through 10 ns markers are selected by a rotary switch. 5, 2, and 1 ns modified sine waves are

selected by self-canceling push-buttons when the rotary switch is in the 521n position.

All outputs are available at the front-panel connectors, or by modification at the interface connector, located at the back of the plug-in, and the TM 500 Series Power Module.

Power supplies are current limited. The 5 V supply is over-voltage protected to avoid damage to the integrated circuits.

Table 1-1

ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements		Supplemental Information
Markers	5 s through 1 ns in a 1, 2, 5 sequence.		5 s through 10 ns are selected by a rotary switch. 5 ns, 2 ns, and 1 ns are push button selected modified sine waves.
Marker Amplitude	≥ 1 V peak on 5 s through 10 ns markers. ≥ 750 mV peak-to-peak into 50 Ω on 5 ns and 2 ns markers. ≥ 200 mV peak-to-peak into 50 Ω on 1 ns markers.		
Trigger Output Signal	Slaved to marker output from 5 s through 100 ns. Remains at 100 ns for all faster markers.		Amplitude same as marker amplitude.
Internal Reference	Standard	Option 01	
Crystal Frequency	1 MHz	5 MHz	
Stability (0°C to +50°C) after 1/2 hour warm-up	Within 1 part in 10^5	Within 5 parts in 10^7	
Long-Term Drift	1 part or less in 10^5 per month	1 part or less in 10^7 per month	
Setability	Adjustable to within 1 part in 10^7	Adjustable to within 5 parts in 10^9	

Table 1-1 (cont)

Characteristics	Performance Requirement	Supplemental Information
External Reference Input (Available Only if U50 and jumpers are installed and U100 is removed)		Lift pin 3 of U350 from socket; IC and jumpers for 5 or 10 MHz. 1 MHz external reference requires jumpers.
Acceptable Frequencies	1 MHz, 5 MHz, or 10 MHz.	Internally hard wired so output frequencies counted down to 1 MHz.
Input Amplitude	Must be TTL, compatible.	
Error Readout Range	To $\pm 7.5\%$.	
Timing Error Measurement Accuracy	Device under test error is indicated to within one least significant digit (i.e., to within one displayed count).	Example: If DUT Timing error reads 3.0% slow, the absolute accuracy will be between 2.9% and 3.1% slow.

Table 1-2

ENVIRONMENTAL CHARACTERISTICS

Characteristics	Description	
Temperature	Meets MIL-T-28800B, class 5.	
Operating	0°C to +50°C	
Non-operating	-55°C to +75°C	
Humidity	95% RH, 0°C to 30°C 75% RH, 30°C to 40°C 45% RH, 40°C to 50°C	Exceeds MIL-T-28800B, class 5.
Altitude	Exceeds MIL-T-28800B, class 5.	
Operating	4.6 Km (15,000 ft)	
Non-operating	15 Km (50,000 ft)	
Vibration	0.38 mm (0.015 inch peak-to-peak, 5 Hz to 55 Hz, 75 minutes.	Exceeds MIL-T-28800B, class 5, when installed in qualified power modules.
Shock	30 g's (1/2 sine) 11 ms duration, 3 shocks in each direction along 3 major axes, 18 total shocks.	Meets MIL-T-28800B, class 5, when installed in qualified power modules.
Bench Handling	12 drops from 45°, 4 inch or equilibrium, whichever occurs first.	Meets MIL-T-28800B, class 5.
Transportation	Qualified under National Safe Transit Association Preshipment Test Procedures 1A-B-1 and 1A-B-2.	
EMC	Within limits of MIL-461A, and F.C.C. Regulations, Part 15, Subpart J, Class A.	
Electrical Discharge	20 kV maximum charge applied to instrument case.	

Table 1-3
PHYSICAL CHARACTERISTICS

Characteristics	Description
Finish	Anodized aluminum panel and chassis
Net Weight	2 lbs., 4 oz. (1 kg.)
Dimensions	2.633 in. (66.8 mm) w x 11.240 in. (285.3 mm) d x 4.961 in. (125.9 mm) h

OPERATING INSTRUCTIONS

Installation

The TG 501 is calibrated and ready for use when received. Referring to Fig. 2-1, install the Generator and turn on the Power Module. Check the front-panel of the Generator to see that the knob skirt is lighted. The TG 501 is designed to operate in any compartment of a TM 500 Series Power Module. Refer to the Power Module Instruction Manual for line voltage requirements and Power Module operation.

Refer to the Controls and Adjustments page for front-panel controls, connectors and indicator descriptions.

CAUTION

Turn the Power Module off before inserting the plug-in; otherwise, damage may occur to the plug-in circuitry.

CONTROLS AND CONNECTORS

MARKER Control

- Rotary switch selects individual marker intervals from 5 s to 10 ns. Set to 521n position when using push buttons for 5 ns, 2 ns and 1 ns. Readout Display is turned off in 521n position.

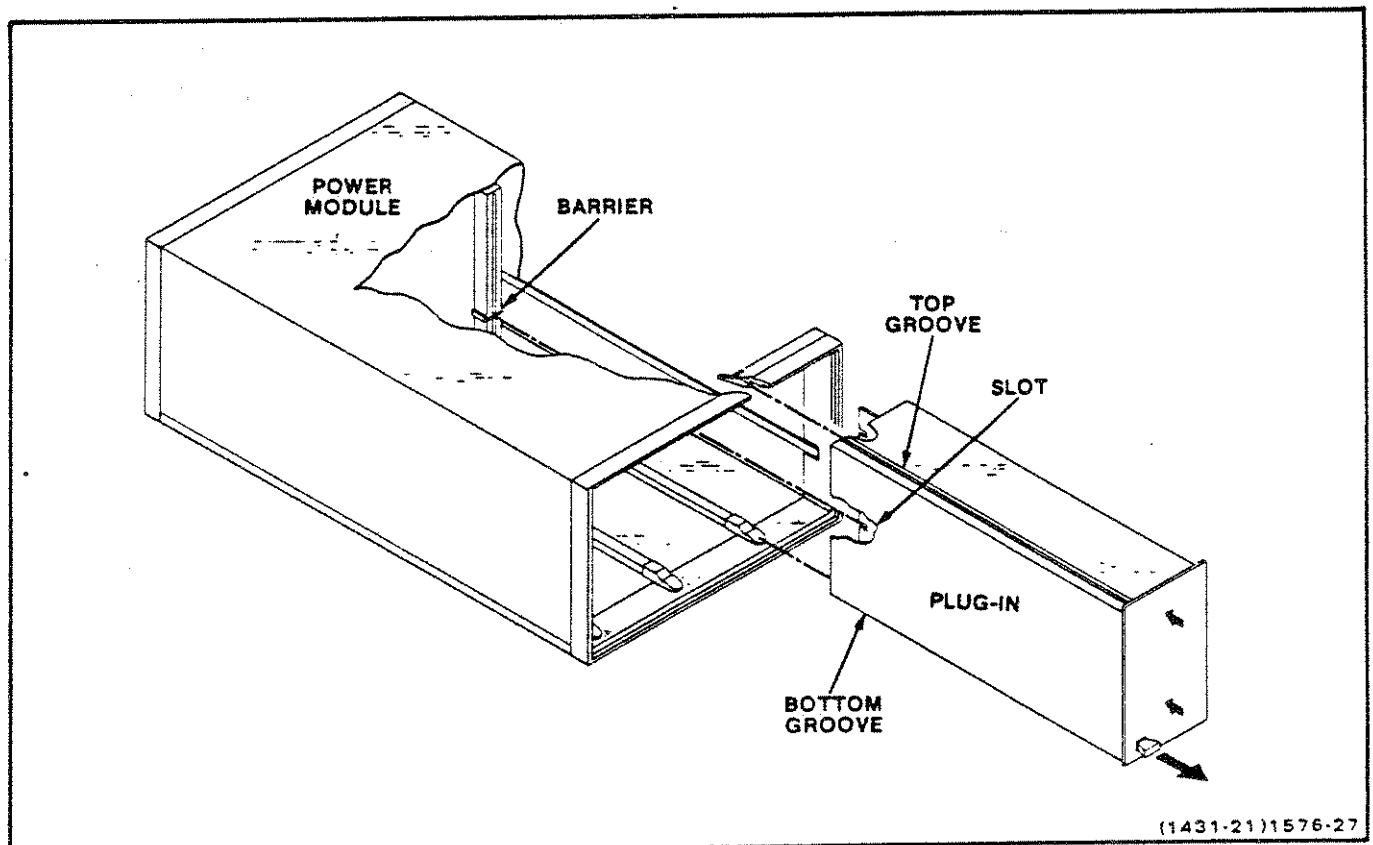


Fig. 2-1. Plug-in installation and removal.

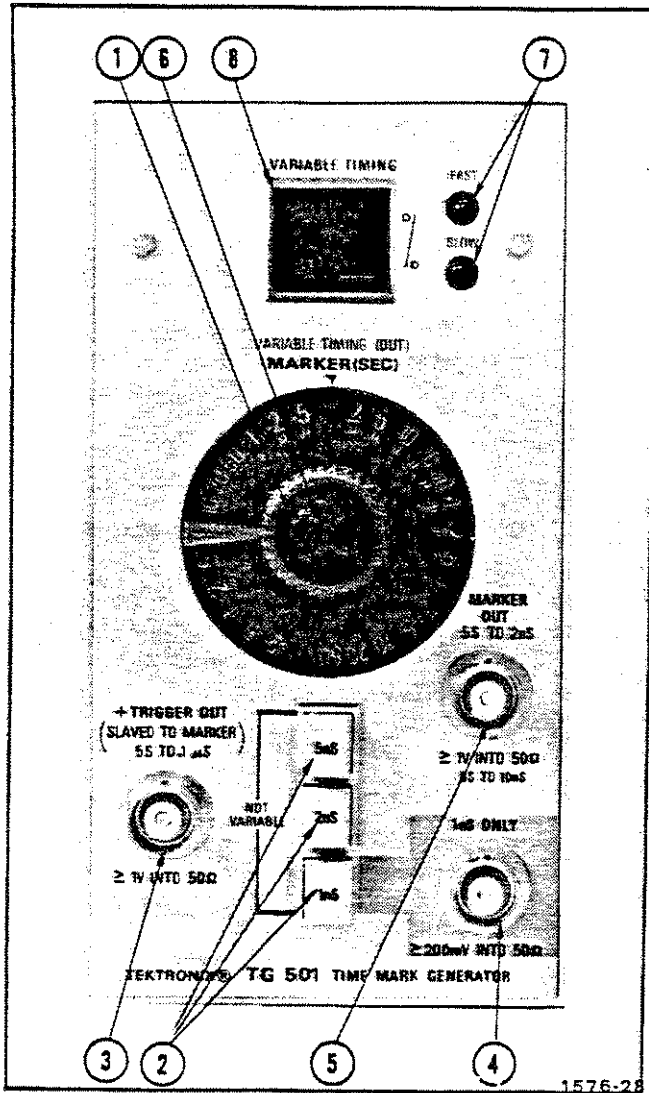


Fig. 2-2. Controls and Connectors.

**5 ns, 2 ns AND
1 ns PUSHBUTTON**

- ② Self-canceling pushbuttons select modified sine waves for 5, 2, and 1 ns when MARKER control is in 521n position. 1 ns marker has a separate output connector. These are not variable.

TRIGGER OUT Connector

- ③ Provides trigger pulses slaved to Marker Output from 5 s through 100 ns. Remains at 100 ns for all faster markers. Pulse amplitude is ≥ 1 V into 50 Ω .

1 ns ONLY Connector

- ④ Provides ≥ 0.5 V peak-to-peak amplitude into 50 Ω of 1 ns modified sine wave selected by the 1 ns push button when MARKER Control is in 521n position.

MARKER OUT Connector

- ⑤ Provides positive markers of ≥ 1 V peak amplitude into 50 Ω for 5 s through 10 ns selected by MARKER Control rotary switch. Provides markers of ≥ 1 V peak-to-peak amplitude into 50 Ω for 5 ns and 2 ns modified sine waves, selected by self-canceling push buttons when MARKER Control is in 521n position.

VARIABLE TIMING Control

- ⑥ Concentric with MARKER Control switch. Markers are calibrated when center button is pushed in allowing selection as indicated by the lighted knob skirt. When center button is out, output timing is fast or slow by the percentage indicated on the Readout Display.

FAST-SLOW Indicators

- ⑦ Light when variable timing control is used. 'Fast' lights when timing is faster than the standard indicated by lighted knob skirt. 'Slow' lights when timing is slower. Percentage faster or slower is read from VARIABLE TIMING Readout.

VARIABLE TIMING Readout

- ⑧ Indicates timing variation from standard timing. First digit is in percent units, second indicates one-tenth percent units.

OPERATING MODES

Calibrated Mode

When the center-button of the VARIABLE TIMING Control is pushed in, the MARKER Control selects calibrated marker intervals from 5 s to 10 ns, indicated by the lighted knob skirt. To select 5, 2, or 1 ns modified sine wave markers, set the MARKER Control to 521n position and press the desired pushbutton.

Variable Timing Mode

When the center button of the VARIABLE TIMING Control is out, output timing is faster or slower than the calibrated marker to the percentage indicated by the VARIABLE TIMING READOUT Display and the FAST-SLOW Indicator lights. 5, 2, and 1 ns push-button controlled modified sine waves are not variable and the Readout Display is turned off when the MARKER Control is in the 521n position.

Readout Display Test

To check the operation of the display LED's (Light-Emitting Diodes), press the center button of the VARIABLE TIMING Control (push in firmly). All LED segments should light, displaying 8.8 in the Readout.

TYPICAL APPLICATIONS

The TG 501 can be used for many applications not described in the manual. Use the following examples to become familiar with the TG 501's VARIABLE TIMING READOUT. Contact your Tektronix Field Office or representative for making specific measurements with this instrument.

Time Base Measurements

To accurately determine the timing error of a time base:

1. Connect the MARKER OUT of the TG 501 to the Vertical Input of the oscilloscope. Use a 50 Ω coaxial cable terminated into 50 Ω .

2. Connect the TRIGGER OUT of the TG 501 to the External Trigger Input of the time base. Use a 50 Ω coaxial cable terminated into 50 Ω .

3. Select external trigger source on the time base.

4. Select, for example, the 1 μ s sweep rate of the time base.

5. Set the MARKER Control rotary switch of TG 501 to 1 μ s.

6. Make sure the center button of VARIABLE TIMING Control, concentric with the MARKER Control, is out (Variable Timing Mode).

7. Use the Horizontal Position control of the time base to make the first time mark coincide with the first graticule line on the oscilloscope. See Fig. 2-3.

8. Rotate the VARIABLE TIMING knob until all time markers coincide with graticule lines on the oscilloscope, as shown in Fig. 2-4.

9. Either the FAST or SLOW Indicator will light showing whether the time base is faster or slower than the calibrated markers of the TG 501. Read the percentage of error from the VARIABLE TIMING READOUT Display.

Pulse Generator Measurements

To accurately determine pulse duration or period of a Pulse Generator:

1. A dual-trace oscilloscope is required. Select alternate mode.

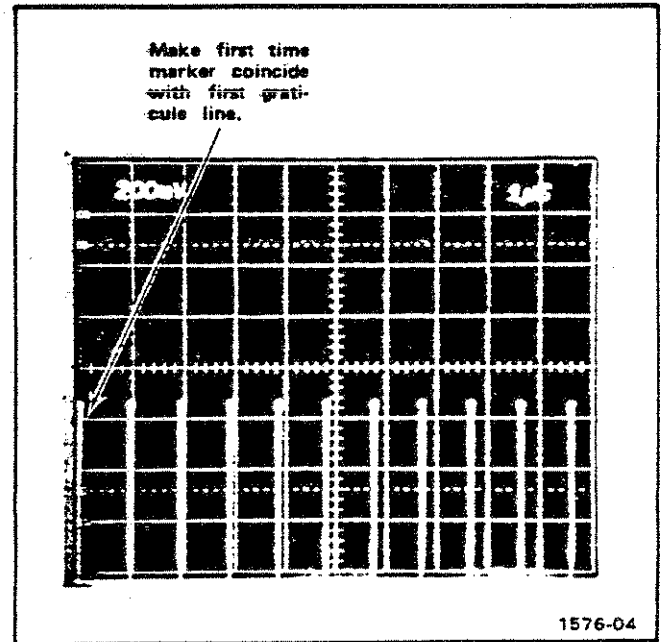


Fig. 2-3. Timing error of time base.

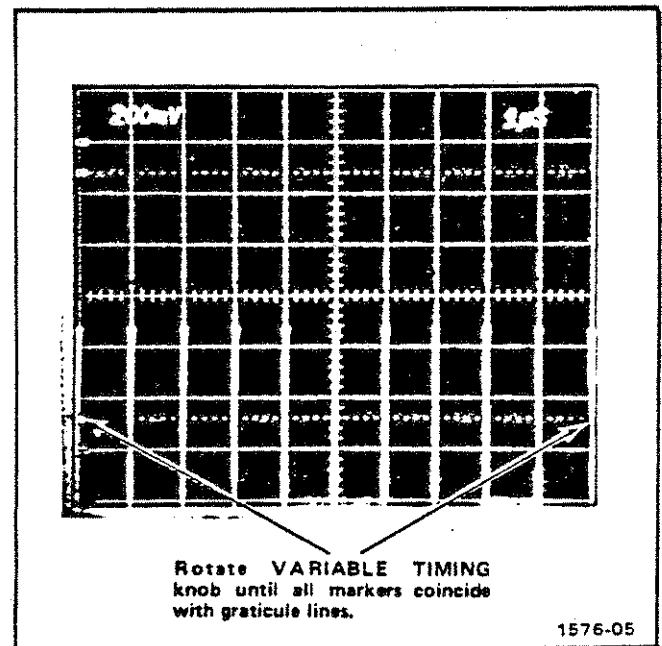


Fig. 2-4. Measuring timing error of time base.

2. Connect the MARKER OUT of the TG 501 to one channel of the dual-trace oscilloscope. Use a 50 Ω coaxial cable terminated in 50 Ω .

3. Connect the Output of the pulse generator to the other channel of the dual-trace, using a 50 Ω coaxial cable terminated in 50 Ω .

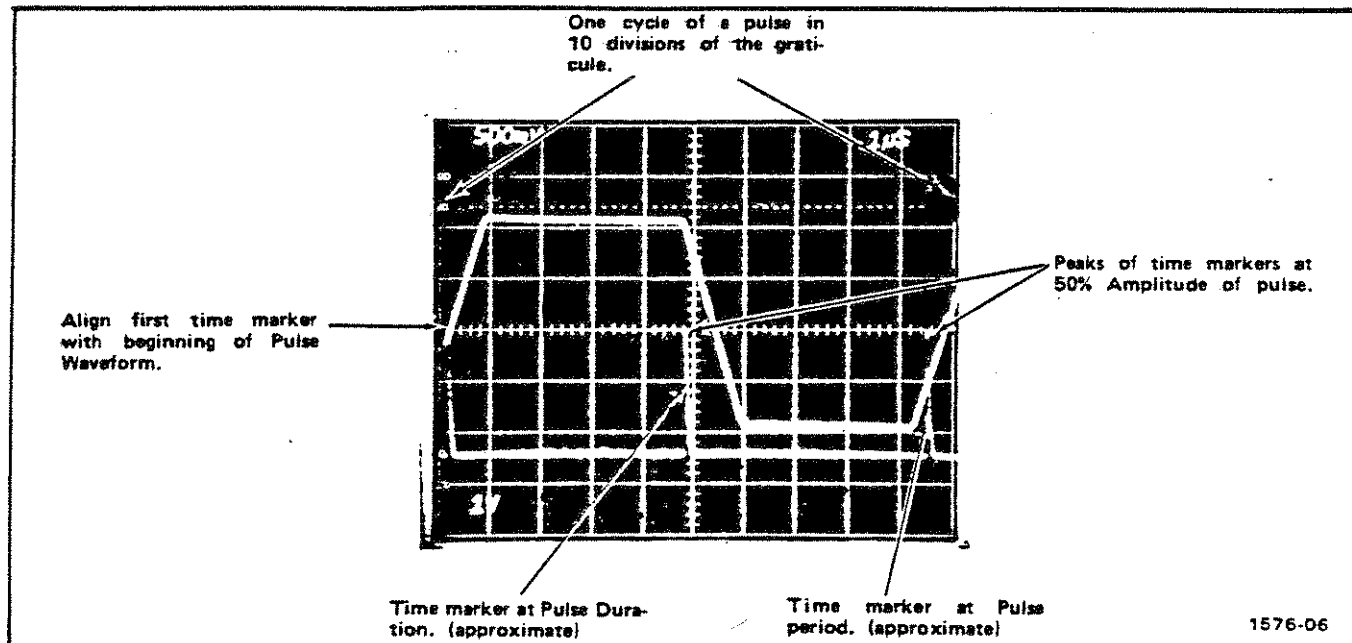


Fig. 2-5. Markers approximately at pulse duration and period.

4. Set the time/div switch to display 1 cycle of a pulse in 10 divisions of the graticule on the oscilloscope, as indicated in Fig. 2-5.

11. Read the VARIABLE TIMING READOUT Display and check the FAST-SLOW Indicators as described in step 9 to find the percentage of error from standard timing.

5. Use the MARKER Control switch of the TG 501 to display one time marker approximately at pulse duration and one at pulse period. Align the first time marker with the beginning of pulse wave-form. See Fig. 2-5.

6. Select Variable Timing Mode on the TG 501 (VARIABLE TIMING Control center button out).

7. Use the Vertical Position control of the oscilloscope to set the peaks of the time markers at 50% amplitude of the pulse shown in Fig. 2-5.

8. To check pulse duration, rotate the VARIABLE TIMING knob until time marks coincide with pulse duration, as shown in Fig. 2-6.

9. Either the FAST or SLOW Indicator will light, showing whether the pulse duration of the pulse generator is faster or slower than the calibrated time mark of the TG 501. Read the percentage of error from the VARIABLE TIMING READOUT Display.

10. To check pulse period, rotate the VARIABLE TIMING knob until time marks coincide with pulse period. See Fig. 2-7.

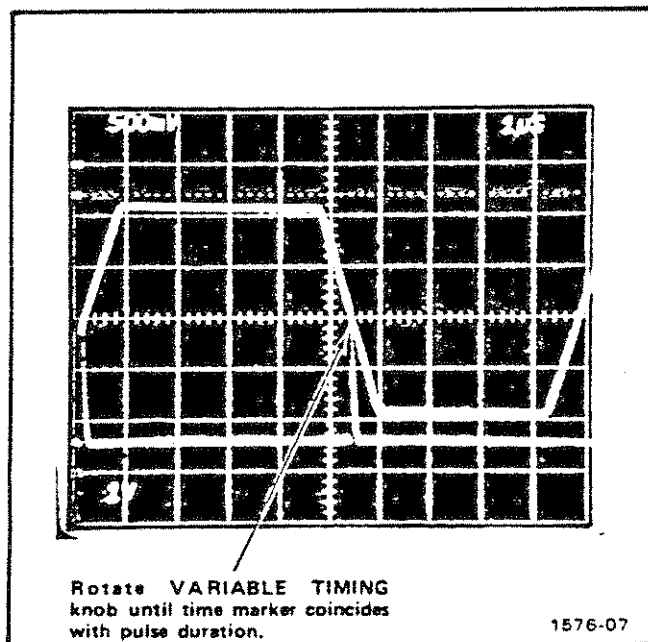


Fig. 2-6. Measuring pulse duration.

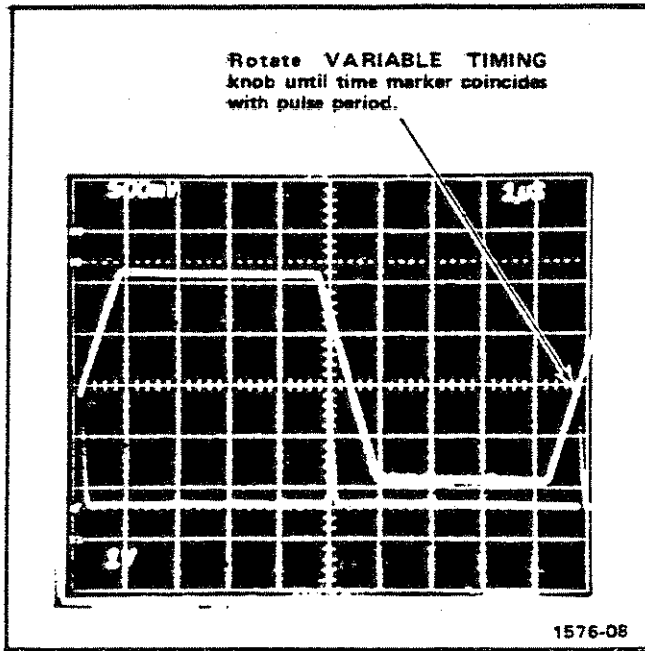


Fig. 2-7. Measuring pulse period.

REPACKAGING FOR SHIPMENT

If the Tektronix instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner (with address) and the name of an individual at your firm that can be contacted, complete instrument serial number and a description of the service required.

Save and re-use the package in which your instrument was shipped. If the original package is unfit for use or not available, repackage the instrument as follows:

1. Obtain a carton of corrugated cardboard having inside dimensions of no less than six inches more than the instrument dimensions; this will allow for cushioning. Refer to the following table for carton test strength requirements.
2. Surround the instrument with polyethylene sheeting to protect the finish of the instrument.
3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between carton and instrument, allowing three inches on all sides.
4. Seal carton with shipping tape or industrial stapler.

SHIPPING CARTON TEST STRENGTH

Gross Weight (lb)	Carton Test Strength (lb)
1-10	200
10-30	275
30-120	375
120-140	500
140-160	600



THEORY OF OPERATION

DIAGRAMS 1 & 2

PHASE LOCK LOOP

1 MHz Crystal Reference and Enable Gate

The reference frequency is supplied by the 1 MHz crystal reference circuitry of Y100, U100 and U350A. The output of the crystal reference circuit is supplied to pin 12 of U110D, which is part of the enable gate circuit. The enable gate circuit, which determines whether the 1 MHz crystal reference or the 1 MHz variable clock is connected to the phase lock loop, is composed of U110A, U110B, U110D, and U115D. When the VARIABLE TIMING (OUT) knob is pushed in and locked, a low is on pin 11 of U110D, allowing the crystal reference oscillator to be available at pin 13 of U110D. A low is also created at pins 12 and 13 of U115D, resulting in a high at pin 11 of U115D and at pin 3 of U110A. The high at pin 3 of U110A causes a low at pin 5 of U110B, which allows U110B to pass the crystal reference oscillator signal to pin 1 of U230A.

100 MHz Voltage Controlled Oscillator, Divide-By-Five Counter ECL-To-T²L Translator, and Divide-By-Two Counter

The voltage controlled oscillator is composed of an astable multivibrator Q280-Q285-Q290, etched capacitor, and Q272, which supplies the charge current for the etched circuit board capacitor. U290D acts as a buffer for the voltage controlled oscillator. The NOR output of U290D is connected to the Divide-By-Five Counter. The ÷5 counter contains U310A, U310B, and U315A. The output of the ÷5 counter is translated from ECL into T²L logic levels by Q330, then supplied to ÷2 counter U320.

Divide-By-Five Counter, Divide-By-Two Counter, Phase Comparator, and Loop Amplifier/Filter

The output of ÷2 counter U320 is supplied to the input of U325. The output, pin 11 of U325 is applied to ÷2 counter U225 pin 12. The Q output of U225 is supplied to pin 5 of U230B.

U230A pin 1 receives 1 MHz from either the crystal reference or the variable clock. U230B pin 5 receives the counted down (÷100) 100 MHz signal from the VCO (Voltage-Controlled-Oscillator). Pins 9 and 12 of U230 go high if the negative edges of the input signals coincide; this occurs when the 100 MHz VCO is operating on frequency. The high inputs to U235A produce a low output that clears U230A and U230B. The transition to a low that occurs at pin 12 of U230A is integrated by R231 and C231; the transition to a high level that occurs at pin 8 of U230B is integrated by R239 and C239. The two integrated output levels are summed by R234 and R239. This summation is then fed to the negative input of the loop amplifier/filter.

The input signal to the loop amplifier/filter is amplified and inverted by operational amplifier U250. The output of U250 is kept from changing rapidly by C250 and C251. The slow change in the output of U250 causes it to be an apparent DC level. VR250 level-shifts the output of U250 to a level that can be used to control the current flow through Q272.

Frequency Regulation of the 100 MHz Voltage Controlled Oscillator

Assume that the frequency has been correct up to this cycle, and that pins 9 and 12 of U230 are low. When the 100 MHz VCO frequency is slower than 100 MHz the negative edge to the phase comparator will toggle U230A first. This results in a high at pins 8 and 12 of U230 and a more negative voltage at the output of U250. This more negative voltage causes Q272 to conduct harder, which allows the etched circuit board capacitor to charge more quickly, to increase the oscillator frequency.

Again assume that the frequency has been correct up to this cycle, but this time the voltage controlled oscillator is faster than 100 MHz. The negative edge of the next cycle will toggle U230B first, resulting in a low at pins 8 and 12 of U230. This in turn causes a more positive voltage at the output of U250 which reduces the conduction of Q272. The etched circuit board capacitor now requires longer to charge since its available charging current has been reduced by Q272.

Out-of-Lock Detector

Ground via the cam switch for all the marker output enable logic gates is via Q270. If the 100 MHz voltage controlled oscillator is running quite slowly (out of specifications), the voltage at the output of the loop amplifier/filter operational amplifier U250 will be quite low. This low voltage will turn on Q255 and Q260, which will turn off Q270, stopping the marker output.

On the other hand, if the 100 MHz VCO is running very fast (out of specifications), the voltage at the output of U250 will be very high. This high voltage will turn off normally conducting Q65, which in turn will turn off Q270, breaking the ground on the enable logic gates. Without ground there is no marker output.

20 ns AND .2 μ s DIVIDE-BY-TWO COUNTERS,

10 ns, 20 ns, or 50 ns AND .1 μ s, OR .5 μ s ENABLE GATES

Theory of Operation—TG501

The 20 ns $\div 2$ counter contains U315B, U290B and U290A. The input to the counter is the output of the 100 MHz VCO. The 20 ns markers from the $\div 2$ counter are coupled to enable gate U300B.

The .2 μ s $\div 2$ counter is part of U325. The $\div 2$ counter output is pin 12 of the integrated circuit, which is supplied to enable gate U330A.

Enable gates for the 10 ns, 20 ns, and 50 ns markers are U300C, U300B, and U300A respectively, while the enable gates for the .1 μ s, .2 μ s, and 15 μ s markers are U330C, U330A, and U335A-U335B respectively. U335C is an OR gate that couples the selected .1 μ s, .2 μ s, or .5 μ s markers to the decade dividers.

1 MHz VARIABLE CLOCK

The 1 MHz variable clock circuit is an emitter-coupled astable multivibrator. Temperature compensation transistor Q120, which is the same type of transistor as Q130 and Q135, establishes the power supply voltage for the multivibrator. Q130, Q135 and Q140 are the multivibrator transistors, with Q130 controlling the charge current available to timing capacitor C127. VR140 provides level shifting for the Q130 base voltage. R135 controls the frequency of the multivibrator by controlling the conduction of Q130. The lower end of R135 is the higher frequency end while the top end reduces the frequency. R145, Variable Timing Center, is used to set the frequency of the multivibrator to 1 MHz when R135 is set to its mechanical midrange position.

PHASE COMPARATOR AND FAST-SLOW LED'S

Description

1 MHz is fed to pin 1 of U150A by either the crystal reference or the variable clock. The 1 MHz crystal reference is fed to pin 5 of U150B. Pins 12 and 9 of U150 will go high if the negative edges of the two 1 MHz input signals coincide. This occurs when the 1 MHz variable clock is on frequency. With these inputs high, U115A produces a low that clears U150A and U150B. The low now at pin 9 of U150B and the high now at pin 13 of U150A are summed by R152 and R153. The output of the summing resistors is then fed to the negative input of amplifier U160.

The input signal to U160 is amplified and inverted by the operational amplifier. The output of U160 is kept from changing rapidly by C160. The slow change in the output of U160 causes it to be an apparent DC level. If U115B has been enabled by releasing the VARIABLE TIMING (OUT) control, the output voltage level of U160 is applied to the junction of DS170 and DS172.

Fast-Slow Indication with VARIABLE TIMING (OUT) Control released

Assume that the frequency has been correct up to this cycle, pins 9 and 12 of U150 are low. When the 1 MHz variable clock frequency is slower than 1 MHz, the negative edge to the phase comparator will toggle U150B first. This results in a high at pins 9 and 13 of U150 and a more positive voltage at the output of U115B. This more positive voltage causes DS172 to conduct and become illuminated.

Again assume that the frequency has been correct up to this cycle, but this time the 1 MHz variable clock frequency is faster than 1 MHz. The negative edge of the next cycle will toggle U150A first, resulting in a low at pins 9 and 13 of U150. This in turn causes a more negative voltage at the output of U115B, which results in the conduction and illumination of DS170.

DIGITAL MIXER AND COUNTER

The 1 MHz Crystal reference is counted down by a factor of 20,000 (2 times 10^4) using gate chain interval decade counters U220, U218, U212, and U210 and flip-flop U215A. The resultant 50 Hz gate frequency (20 ms gate period) available at the outputs of U210 is used to control the display time of the VARIABLE TIMING % LED. Pin 11 of U210 is the $\div 5$ output; pin 12 is the $\div 2$ output. The two outputs of U210 are ANDed by U180D to produce a 2 ms pulse, which is used to clear BCD counters U185 (0.01% digit, which is not displayed), U195 (0.1% digit) and U200 (units % digit).

The 1 MHz Crystal Reference and the 1 MHz variable clock output frequencies are compared by digital mixer U215B, with only the frequency difference of the two input frequencies appearing at the output. The output of U215B is ANDed in U180C with the inverted $\div 2$ output (10 ms wide gate) of U210. The output of U180C goes to the first of the three BCD counters. Inverter U190B, located between U185 and U195, provides averaging so that U195 (0.1% digit) changes on the count of five instead of nine.

The 2 ms output pulse of U180D and the 10 ms output pulse of U115C go to NOR gate U110C. The output of U110C (which is an 8 ms pulse that determines LED display time) is one input to AND gate U180B. The other input to U180B must be a high from U235B to enable U180B and cause the LED display to be unblanked. A high out of U235B is caused by either depressing the VARIABLE TIMING % control fully in to check the LEDs, or by releasing the VARIABLE TIMING % control to its out position. The low to pin 5 of U235B in the out position of the VARIABLE TIMING % control is from pull-up resistor R450 via CR115 and inverter U115D. In the 521N position of the MARKER Control, the cathode of CR115 is connected to ground via S350 to disable the variable timing circuit, since the 1 ns, 2 ns, or 5 ns markers are not variable.

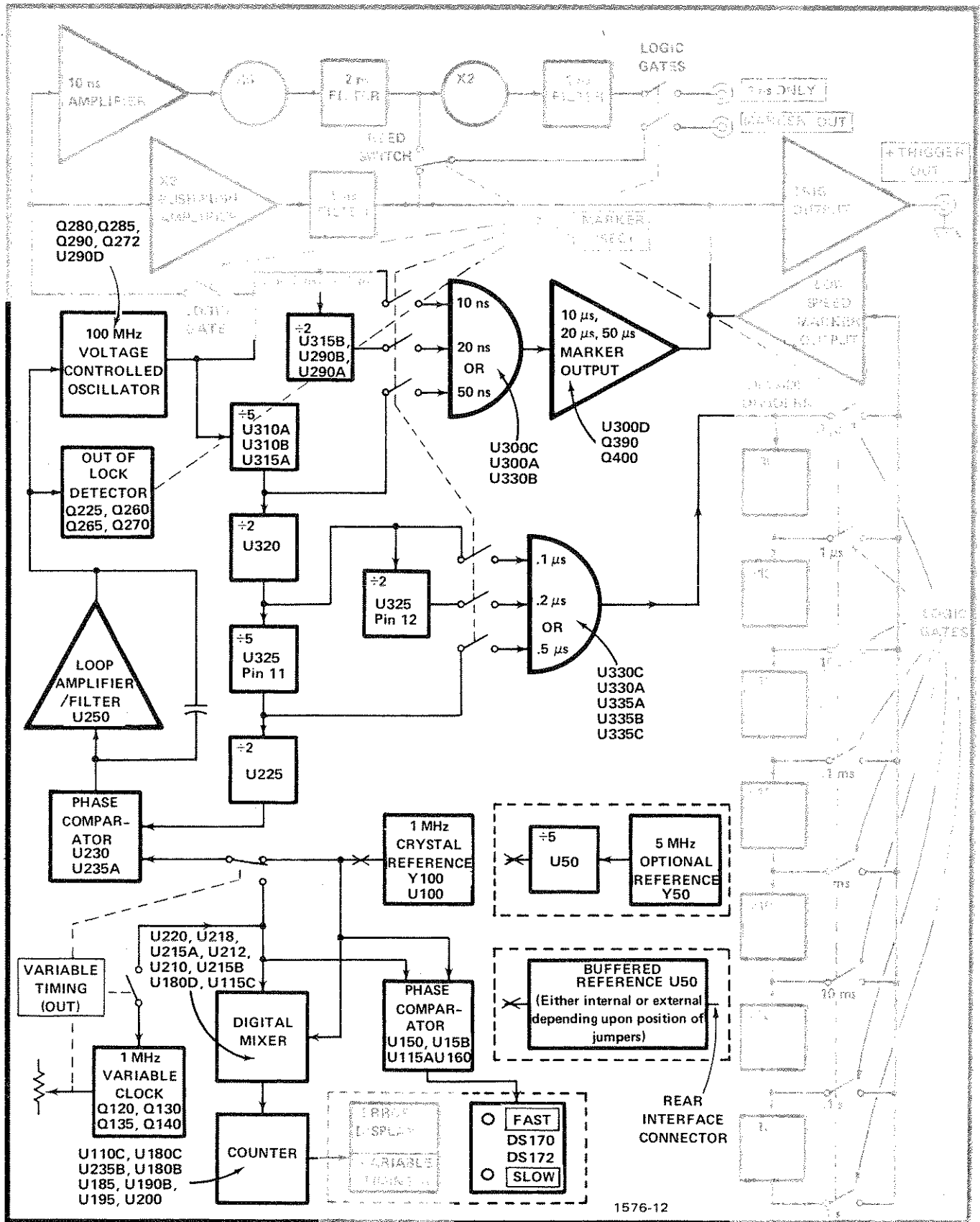


Fig. 2-1. Functional block diagram of schematic diagrams 1 & 2 circuitry.

DIAGRAM 3

DECADE DIVIDERS

The decade dividers operate continuously; however, the output is selected by enabling the appropriate enable logic gate with a low, via the cam switch S350. The $\div 10$ dividers are U355, U360, U362, U364, U368, and U372. The NAND enable logic gates are U330B, U350C, U190A-C-D and U366A-B-C-D. The square-wave pulse from the logic gates is differentiated by an RC circuit using capacitors C358, C360, C362, C366, C368, C370 and C372. The resistance for the RC circuit is selected by cam switch S350 via the 5-2-1 sequence logic gates, depending upon the timing position in the 5-2-1 sequence.

The selection of the resistance for the RC circuit determines the slope of the falling edge of the marker and hence controls the marker brightness. R385, the largest resistance, is selected in all positions of the 5-2-1 sequence. In the 2 position, a low from the 5-2-1 sequence logic gate turns on Q384 and connects R384 in parallel with R385, reducing the resistance and the marker brightness. In the 1 position, Q380 turns on and R381 parallels R385 to reduce the resistance and brightness from that obtained in the 2 position.

Q405 provides a stage of isolation between the decade dividers and the low speed marker output amplitude. The isolation stage increases the impedance seen by the input to the low speed marker output operational amplifier.

LOW SPEED MARKER OUTPUT AMPLIFIER

The low speed marker output amplifier is an operational amplifier having a gain of 1.5. The amplifier consists of Q408 and Q415 with R406 and R410 being the input resistor and feedback resistor respectively.

10 ns, 20 ns, 50 ns MARKER OUTPUT AMPLIFIER

Q390 and Q400 form an emitter coupled switch which is controlled by U300D, an ECL enable logic gate. U300D requires a low from the 10 ns, 20 ns, or 50 ns logic gate to pass the square-wave. The square-wave at output pins 15 and 9 of U300D is differentiated by RC networks C390-R394 and C400-R400. The differentiated signal is coupled through Q400 as long as pin 13 of U300D remains low. The output from Q400 is summed with the output from the low speed marker output amplifier and supplied to the MARKER OUT connector J470.

TRIGGER OUTPUT

At MARKER Control settings of 5 s through $.1 \mu\text{s}$ the marker available at the MARKER OUT connector is used as a slave trigger. The slave trigger from the low speed marker output amplifier is coupled through emitter followers Q430 and Q435 and made available at + TRIGGER OUT connector J435.

At Marker Control settings of 50 ns and faster, the trigger signal rate available at the + TRIGGER OUT connector remains $.1 \mu\text{s}$. The $.1 \mu\text{s}$ output is obtained by enabling logic gates U235C and U330D. Enabling U330D allows the output square-wave from U320 to be differentiated by RC network R400-R445-C440, then amplified by Q440 before being coupled to the + TRIGGER OUT connector via emitter follower Q435. The RC network determines the width and amplitude of the trigger signal, while R439-C439 network in the emitter of Q440 controls the signal gain. R445 High Speed trigger amplitude provides a means of adjusting the high speed trigger amplitude to match the low speed trigger amplitude.

DIAGRAM 4

X2 PUSH-PUSH AMPLIFIER AND 5 ns FILTER

Placing the MARKER (SEC) switch at its 521N position enables ECL logic gate U290C, which allows the 100 MHz signal to pass to J450. Pushing the 5 ns pushbutton enables ECL logic gate U450B, applying the 100 MHz (10 ns) signal to the primary of T450.

T450 is a toroidal transformer having a center-tapped primary and secondary winding. C450 tunes the resonance frequency of the T450 primary to 100 MHz. The secondary of T450 connects to a push-push amplifier U455, which acts as a frequency doubler. The output of U455 connects to the 5 ns filter, which contains a parallel resonant (as seen at the output) tank circuit consisting of L462, part of the etched circuit board, and C465. C465 is used to tune the tank circuit to 5 ns (200 MHz). C467 is as an amplitude adjustment for the 5 ns markers. From the output of the 5 ns filter, the 5 ns markers connect to the MARKER OUT connector, J470, via K450-S1 contacts.

10 ns AMPLIFIER, X5 2 ns FILTER, X2 and 1 ns FILTER

Placing the MARKER (SEC) switch at its 521N position enables ECL logic gate U290C, which allows the 100 MHz signal to pass to J450. Pushing the 2 ns or 1 ns pushbutton enables ECL logic gate U450C, applying the 100 MHz (10 ns) signal to the base of Q484.

Q484 and Q486 compose a Class C amplifier. R482, CR482, and U450C make up a temperature compensation network for the amplifier. R482, Amp Bias, is used to peak the amplifier gain.

The output of the amplifier connects to a parallel resonant tank circuit consisting of L490 and C498. C498 is used to tune the tank circuit to 10 ns (100 MHz). L500, part of the etched circuit board, and C500 make up a matching network for the input to varactor CR500.

CR500 is a snap type varactor, i.e. a varactor that snaps off. The varactor is triggered at a 100 MHz rate. The sudden current change that occurs when CR500 snaps off at its 100 MHz rate causes L502, part of the etched circuit board, and C504 to ring at a 2 ns (500 MHz) rate. C504 tunes the ring circuit to resonance at a 2 ns rate.

The 2 ns filter is a tuned stub comb filter with each stub tuned successively to resonance. The input to the filter is a damped sine-wave, which is then electromagnetically coupled between the sections of the filter.

The 2 ns output sine-wave is applied to CR515 and connected to J470 the MARKER OUT connector only if K450 has been enabled by depressing the 2 ns pushbutton thus closing K450-S1 contacts to C515.

When the 1 ns or 2 ns buttons are pressed in (and the 5 ns button is released), Q460 is biased on. In this state, Q460 functions as a 5 ns suppression gate by presenting a low impedance path from L465 and R463 to the +5 volt supply at the emitter of Q460. Undesirable 5 ns signals that would otherwise appear in the output circuitry are effectively bypassed to signal ground via the +5 volt supply.

The 2 ns sine-wave input to CR515 is distorted by the non-linear device (diode) to achieve a 1 ns sinewave. The 1 ns sinewave is then filtered by the 1 ns filter which is similar in operation to the 2 ns filter discussed previously. The output from the filter is available through the 1 ns ONLY connector. The 1 ns markers are available from the 1 ns ONLY connector whenever the MARKER Control is set to 521N and either the 2 ns or 1 ns pushbutton has been depressed.

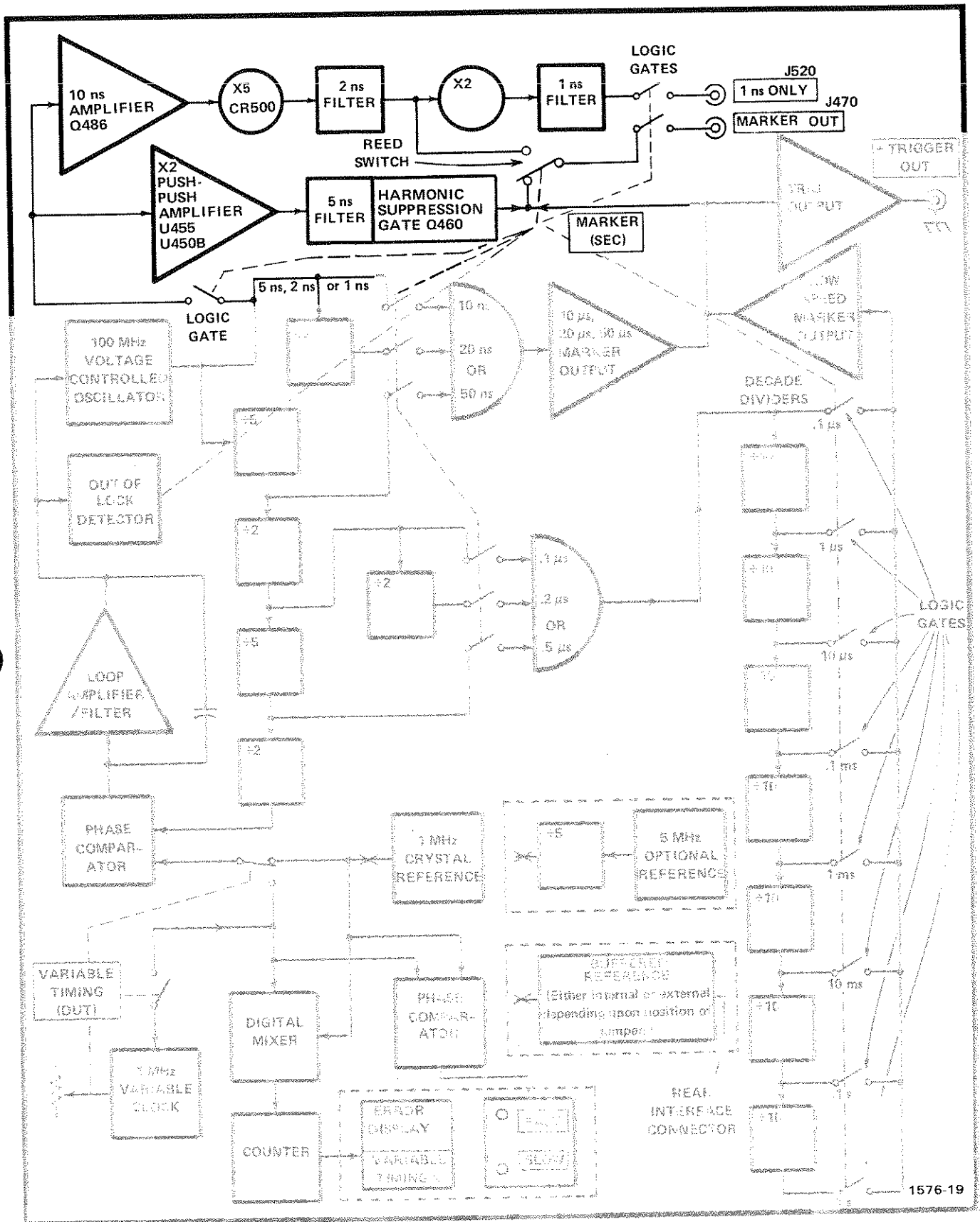


Fig. 2-3. Functional block diagram of schematic diagram 4 circuitry.

DIAGRAM 5

ERROR DISPLAY

The decoder drivers U550 and U570 are driven by the output signals of the counter circuitry. U550 output drives the .1% LED display device DS550 while U570 output drives the 1% LED display device DS570.

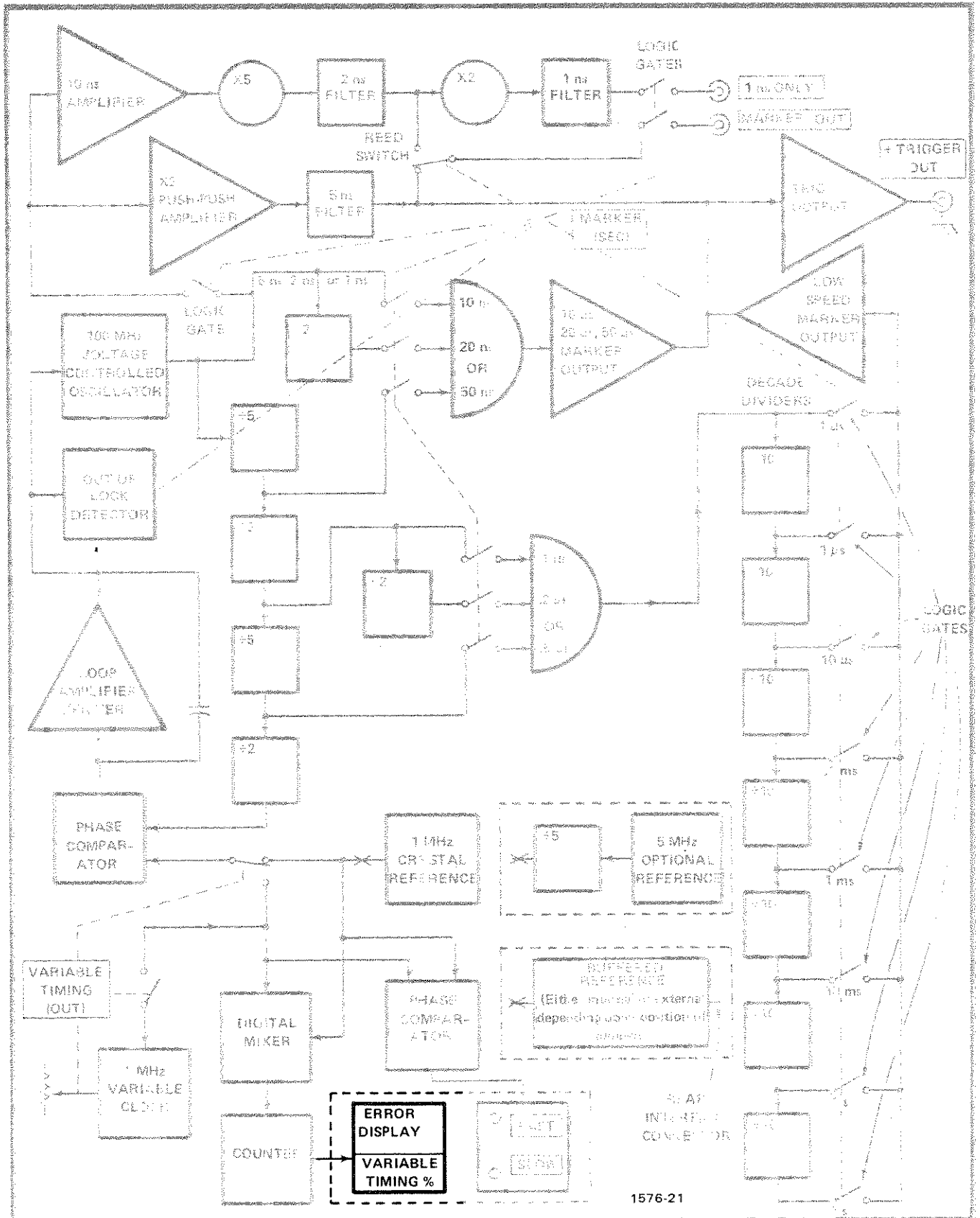


Fig. 2-4. Functional block diagram of schematic diagram 5 circuitry.

DIAGRAM 6

POWER SUPPLY

+15-Volt Supply

The regulator for the +15 volt supply consists of short circuit protection and error sensing amplifier transistor Q605, Error amplifier transistor Q600, Reference Zener diode VR605, and a Darlington transistor pair (Q610 and a series-pass transistor located in the power module mainframe). The supply voltage is established by comparing the supply voltage sample (which is established by the R616-R606-R605 divider at the base of Q605) with the reference voltage established by VR605 at the emitter of Q605. Potentiometer R606 is adjusted for a +15 V supply output of +15.2 volts. Any difference between the Q605 base and emitter is amplified by Q605 and Q600, and used to change the conduction of the series-pass transistor to correct the output voltage. VR605 is temperature compensated by the base-emitter junction of Q605. R614 provides current limiting for the series pass transistor. R603 and Zener diode VR600 establish the operating voltage range for Q600.

If the +15 V output is shorted (i.e., output goes low), Q605 starts to turn off which pulls the base of Q600 high through R600. Consequently, transistor Q600 saturates against the voltage established by 3 V Zener VR600 and R603. Thus, the voltage at the collector of Q600 is nearly 3 V below the unregulated line. The 3 V is reduced by the voltage drops at the base-emitter of Q610 and the base-emitter of the series-pass transistor in the power module mainframe to a maximum of approximately 1.6 V across R614. The 1.6 V across R614 establishes the maximum current that can be drawn from the +15 V supply.

+5-Volt Supply

The regulator for the +5 volt supply consists of error sensing amplifier integrated circuit U625, short circuit protection transistor Q620, over-voltage protection circuit VR640-Q640 and a Darlington transistor pair (Q635 and a series-pass transistor in the power module mainframe). The supply voltage is established by comparing the supply voltage sample at the negative input to U625 with the reference at the positive input to U625. Any difference between the inputs to U625 causes an amplified correction voltage to be sent to the base of Q635, which in turn will cause a change in the conduction of the series pass transistor to correct the output voltage. R621 provides current limiting for the series pass transistor.

If the +5 V output is shorted (i.e., output goes low), the increased voltage drop across R621 causes Q620 to turn on. This pulls the negative input of U625 positive, which turns off Q635 and the series pass transistor. Fuse F620 protects Q620 if the short causes excessive current to be drawn from the supply.

In case the regulator causes the voltage to become more positive (i.e., +7 V or more), silicon controlled rectifier (SCR) will fire and short the +5 V output to ground.

