INSTRUCTION MANUAL

MODEL 802
50 MHz PULSE GENERATOR

WAVETEK
SAN DIEGO

9045 BALBOA AVENUE, SAN DIEGO, CALIFORNIA

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MODEL 802
50 MHz PULSE GENERATOR

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All Wavetek instruments are warranteed against defects in material and workmanship for a period of one year after date of manufacture. Wavetek agrees to repair or replace any assembly or component (except batteries) found to be defective, under normal use, during this period. Wavetek's obligation under this warranty is limited solely to repairing any such instrument which in Wavetek's sole opinion proves to be defective within the scope of the warranty when returned to the factory or to an authorized service center. Transportation to the factory or service center is to be prepaid by purchaser. Shipment should not be made without prior authorization by Wavetek.

This warranty does not apply to any products repaired or altered by persons not authorized by Wavetek, or not in accordance with instructions furnished by Wavetek. If the instrument is defective as a result of misuse, improper repair, or abnormal conditions or operations, repairs will be billed at cost.

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.

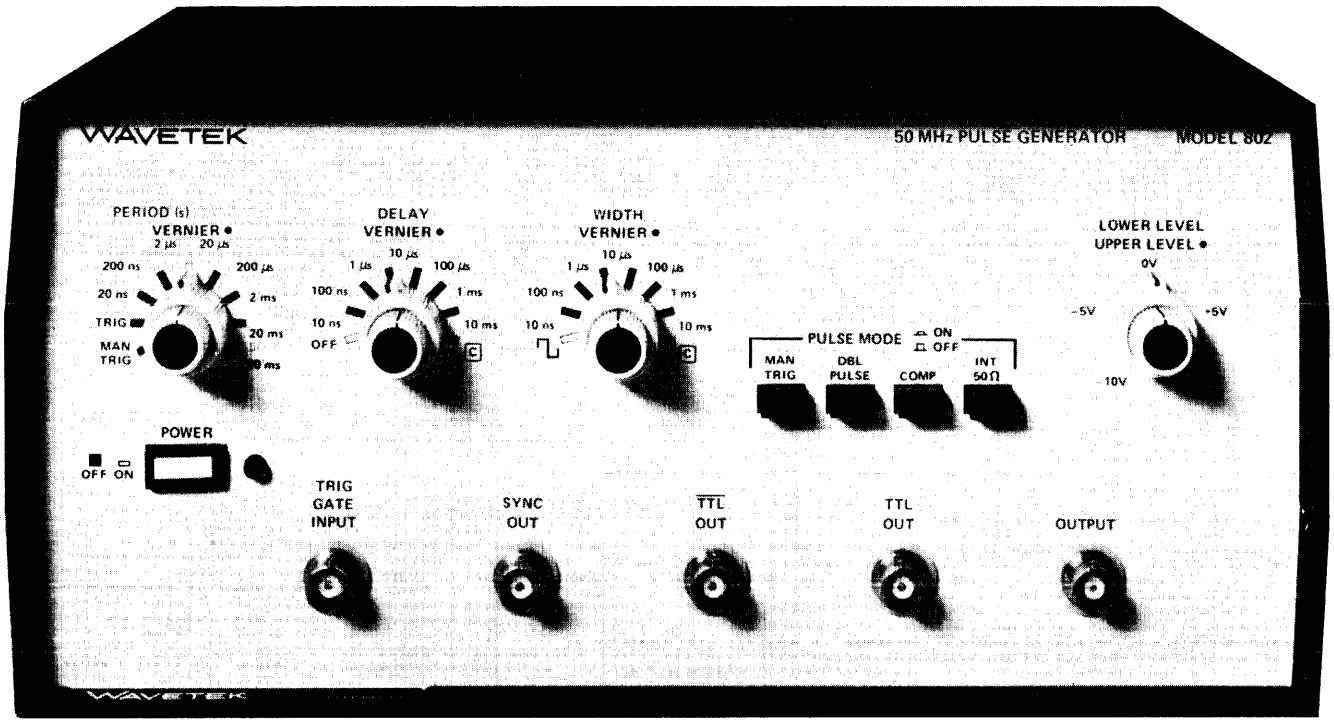


Figure i. Model 802 50 MHz Pulse Generator

SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 802

The Model 802 is a 50 MHz general purpose laboratory pulse generator. The instrument gives you full control in primary pulse triggering and shaping plus simultaneous TTL, $\overline{\text{TTL}}$ and sync pulses. The primary pulse output has controllability in rate, width, delay, upper level, lower level and a choice of positive, negative or complementary outputs. The TTL and $\overline{\text{TTL}}$ are of fixed levels and rise times that are standard for use with compatible devices. The primary pulse has rise and fall times of 5 ns or less.

The output is ±10 volts with a 50Ω termination. Upper and lower pulse levels are fully adjustable through ±10 volts, a 20 volt window. Termination may be internal, at the load or both.

Single pulses or pulse pairs may be triggered; pulse width may be trigger controlled; continuous pulses may be gated for a 'burst' output.

1.2 SPECIFICATIONS

1.2.1 Versatility

Four Simultaneous Pulse Outputs
Fixed TTL level sync, TTL and $\overline{\text{TTL}}$ outputs, and variable amplitude output pulses are available over a 5 Hz (200 ms) to 50 MHz (20 ns) frequency range.

For optimum pulse characteristics from the variable amplitude pulse output, an internal 50Ω load can be selected via a front panel control.

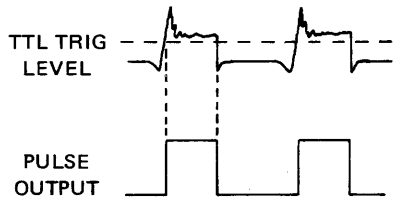
Operational Modes
Continuous: Generator oscillates continuously at selected frequency.

Triggered: Generator quiescent until triggered by external TTL pulse or front panel control, then generates one pulse.

Gated: Generator oscillates at the period rate selected by the front panel control when gate input is high. Generator quiescent when input is low. First cycle is synchronous with rising edge of gating signal.

Double Pulse: Same as continuous, triggered and gated, except two pulses for each period. Time to second pulse is controlled by delay control. Double pulse at all outputs except sync.

External Width: External signal at trigger input determines output pulse width and period as shown.



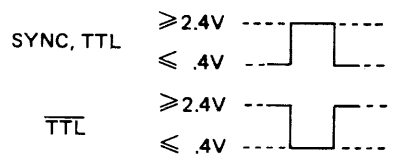
1.2.2 Pulse Outputs

Variable Amplitude Pulse

SOURCE	LOAD	DYNAMIC RANGE	AMPLITUDE MAXIMUM	AMPLITUDE MINIMUM
50Ω	50Ω	+5V −5V	5V	.5V
1 kΩ	50Ω	+10V	10V	1V
OR				
50Ω	⩾1 kΩ	−10V		

Upper and lower pulse levels are independently adjustable. Pulse dynamic range is ±10V when load is 50Ω terminated and source is not (internal 50Ω off) or vice versa. Maximum pulse amplitude is 10V; minimum is 1V. Dynamic range and pulse amplitude are decreased by a factor of 2 when source and load are 50Ω terminated. Overshoot and ringing are less than ±(5% of amplitude setting +100 mV) when terminated into 50Ω at both load and source. Transition times are less than 5 ns.

Sync, TTL and $\overline{\text{TTL}}$ Pulses
Sync pulse levels from 50Ω; TTL and $\overline{\text{TTL}}$ pulse levels into 50Ω termination.



Transition times less than 7 ns into 50Ω termination.

Normal/Complement Control
Normal pulse or its complement is selected. The normally quiescent and active levels are reversed in complement format. This control affects all outputs except sync pulse.

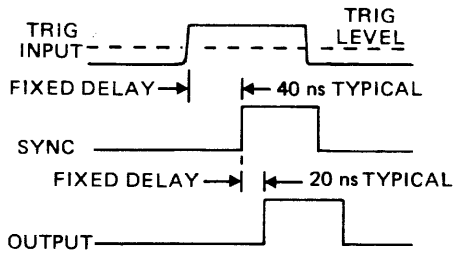
1.2.3 Time Domain

Period
Period range is from less than 20 ns to greater than 200 ms in 7 overlapping ranges. Period jitter is less than ±0.1% plus 50 picoseconds.

Width
Width range is from less than 10 ns to 10 ms in 6 overlapping ranges. Maximum duty cycle is 70% for periods to 200 ns, decreasing to 50% for 20 ns periods. Width selector switch also has a square wave detent and a customer-specified detent.* ⊓⊔ duty cycle is 50 ±4% to 2 μs period, changing to 50 ±15% at 20 ns period. Width jitter is less than ±0.1% plus 50 picoseconds. Sync pulse duty cycle is 50 ±4% of pulse period to 2 μs period, changing to 50 ±15% at 20 ns period except in trigger and external width modes, in which case it is determined by the trigger signal.

Delay
Pulse occurence can be delayed from less than 10 ns to 10 ms with respect to the sync pulse (not including fixed delay). Delay selector switch also has a customer-specified detent.* Maximum delay duty cycle is 70% for periods to 200 ns, decreasing to 30% for 20 ns periods.

Delay jitter is less than ±0.1% plus 50 picoseconds. Fixed delay is as shown.



1.2.4 Input Characteristics

External Trigger
The circuit receiving the external trigger is TTL compatible. Triggering level is fixed at approximately 1.4V. Input impedance is greater than 500Ω shunted by approximately 33 pF. Triggering and gating occurs on the rising edge of the input signal.

1.2.5 General

Environmental
Specifications apply at 25°C ±5°C after 30 minutes warm-up. Instrument will operate from 0°C to 50°C.

Dimensions
28.8 cm (11.4 in.) wide; 10.2 cm (4 in.) high; 29 cm (11.4 in.) deep.

Weight
4.0 kg (8.9 lb) net; 5.4 kg (12 lb) shipping.

Power
108 to 132V or 216 to 250V; 50 to 400 Hz; 40 watts nominal.

*Customer-installed capacitor determines detent range.

SECTION 2
INSTALLATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground path can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 108 to 126 Vac line supply and with a 0.5 amp fuse.

Conversion to other input voltages requires a change in rear panel fuse-holder voltage card position and fuse according to the following table and procedure.

Card Position	Input Vac	Fuse (Slow Blow, 3 AG)
100	90 to 105	0.5 amp
120	108 to 126	0.5 amp
220	198 to 231	0.25 amp
240	216 to 250	0.25 amp

1. Open fuse holder cover door and rotate FUSE PULL to left to remove the fuse.
2. Select operating voltage by orienting the printed circuit board to position the desired voltage on the top left side. Push the board firmly into its module slot.
3. Rotate the FUSE PULL back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.
4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

2.2.2 Signal Connections

Use 3 foot RG58U 50Ω shielded cables equipped with female BNC connectors to distribute input and output signals when connecting this instrument to associated equipment.

2.3 ELECTRICAL ACCEPTANCE CHECK

This checkout procedure verifies the generator operation. If a malfunction is found, refer to the Warranty in the front of this manual. A 2 channel oscilloscope and 50Ω coax cable are needed for this procedure (see figure 2-1).

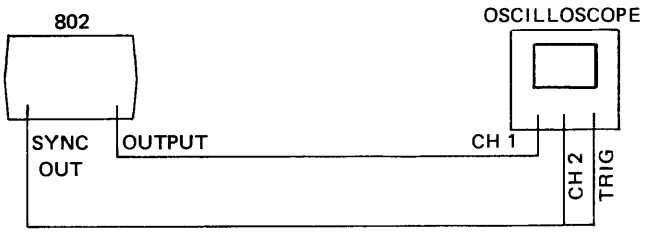


Figure 2-1. Initial Setup

Preset the pulse generator controls by setting the following switches to their white mark:

PERIOD/RATE
DELAY
WIDTH

Set the PULSE MODE switches OFF except set INT 50Ω ON.

Set the following controls to 12 o'clock:

PERIOD/RATE VERNIER
DELAY VERNIER
WIDTH VERNIER
LOWER LEVEL
UPPER LEVEL

Perform the steps in table 2-1. Only approximate values are required to verify operation.

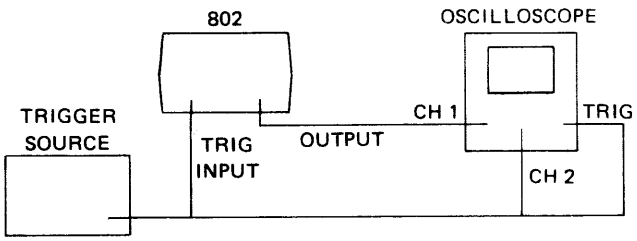


Figure 2-2. Second Setup

Table 2-1. Performance Checkout

Step	Control	Position/Operation	Observation
1	POWER	ON	CH 1: A near 0 volt dc level. (LEVEL control is not calibrated.) CH 2: Approximately 2.5 volt pulses.
2	LOWER LEVEL	Rotate ccw	Pulse base drops 10V.
3	UPPER LEVEL	Rotate ccw	Pulse upper level drops 10V.
4	UPPER LEVEL	Rotate cw. Make observation; then reposition for good display	Pulse rises 10V, then rises 10V more while pulling the base up 10V. Base rises to 0V.
5	COMP	ON then OFF	Set scope for one or two cycles. Observe the switching of duty time from first half cycle to second half cycle.
6	WIDTH	Rotate ccw, then to 10 μs ▮ 100 μs	Pulse width changes. (Use scope X 10 magnification to see narrow widths.)
7	WIDTH VERNIER	Rotate ccw, then to 12 o'clock	Pulse width decreases, then increases.
8	DELAY	Rotate cw to 10 μs ▮ 100 μs	Pulse delay changes within cycle time.
9	DELAY VERNIER	Rotate ccw, then cw	Pulse delay moves to left, then right.
10	PERIOD/RATE VERNIER	Rotate cw, then to 12 o'clock	Period increases, then decreases.
11	DBL PULSE	ON	Two pulses instead of one.
12	DELAY VERNIER	Rotate ccw, then cw, but maintain double pulse	Pulse pairs move closer, then further apart.
13	WIDTH VERNIER	Rotate ccw, then to 12 o'clock, but maintain double pulse	Pulse width of each pulse of pulse pair decreases, then increases.
14	OUTPUT	Remove cable; place on TTL connector	TTL double pulse output.
15	TTL OUT	Remove cable; place on $\overline{\text{TTL}}$ connector	$\overline{\text{TTL}}$ double pulse output complement of previous output.

Table 2-1. Performance Checkout (Continued)

Step	Control	Position/Operation	Observation
16		Change to setup in figure 2-2; trigger with a 10 kHz signal; adjust scope for best display	One pulse on CH 2; set of pulses on CH 1.
17	WIDTH	Rotate to ⊓⊔	One pulse on CH 1; one pulse on CH 2.
18	MAN TRIG	ON	Repeated operation makes pulse pair observable.

SECTION 3
OPERATION

3.1 CONTROLS AND CONNECTORS

The generator controls and connections are shown in figure 3-1 and keyed to the following descriptions.

① **PERIOD/RATE Switch** – Selects one of seven ranges of pulse period calibrated in seconds and hertz. The TRIG detent holds the output at the inactive level until a TTL level trigger signal is applied at the TRIG GATE INPUT BNC. On the input rising edge, one pulse, or one double pulse, is output. The MAN TRIG detent is as the TRIG detent, except pressing the MAN TRIG switch generates the output.

NOTE

For continuous mode operation, low input or 50Ω termination to the TRIG GATE INPUT BNC must be removed.

VERNIER Control – Varies the pulse period within the range selected by the outer knob. Clockwise increases the pulse period and decreases frequency.

② **DELAY Switch** – Selects one of seven ranges of pulse delay or time-to-second-pulse of double pulses, depending on DBL PULSE switch setting. OFF position of DELAY switch ensures minimum delay. The detent marked "C" is for customer selected range.

VERNIER Control – Varies the delay time within the range selected by the outer knob. Clockwise increases the delay.

③ **WIDTH Switch** – Selects one of seven ranges of pulse width or an approximate 50% duty cycle. The detent marked "C" is for customer selected range.

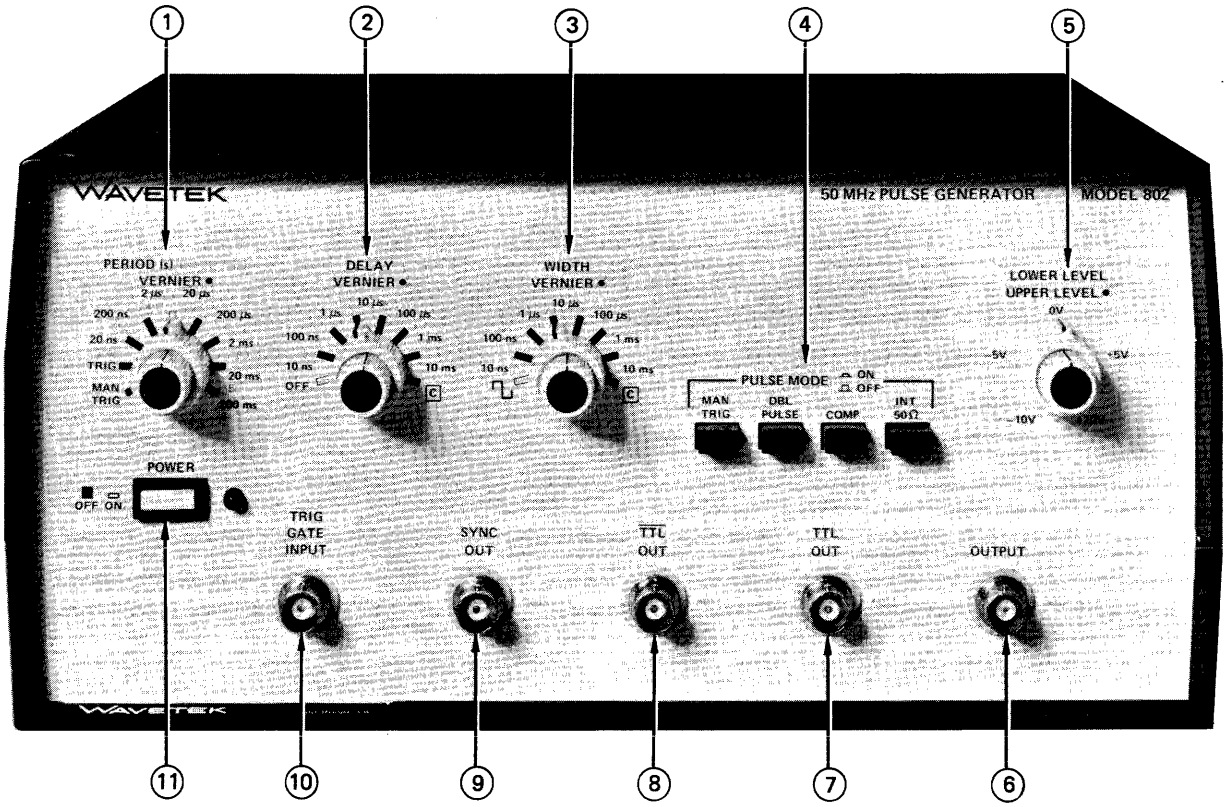


Figure 3-1. Controls and Connections

VERNIER Control – Varies the pulse width within the range selected by the outer knob except in ⊓⊔ .

④ **MAN TRIG Switch** – Triggers the generator one time when pressed. Output depends on the mode selected.

DBL PULSE Switch – When ON, a double pulse occurs in each period. Time to leading edge of second pulse is controlled by the DELAY setting. When OFF, one pulse occurs in each period.

COMP Switch – Selects a normal pulse when OFF or its complement when ON, which swaps the active and quiescent levels. Affects all outputs, except SYNC.

INT 50Ω Switch – When ON, the output current source is 50Ω terminated internally. When OFF, the current source has greater than 1 kΩ impedance.

⑤ **LOWER LEVEL Control** – Outer knob sets the lower level of the OUTPUT pulse, which may be varied from –10 to +10 volts into a single 50Ω termination or –5 to +5 volts into a double 50Ω termination. Maximum pulse heights are 10 and 5 volts, respectively.

UPPER LEVEL Control – Inner knob sets the upper level of the OUTPUT pulse. Upper level range is identical to that stated for the lower level.

⑥ **OUTPUT Connector** – The main output of the generator. Pulses from this output may be controlled in level as well as frequency and width.

⑦ **TTL OUT Connector** – An output with a transistor-transistor-logic level pulse whose occurrence and duration are controllable. Normal pulse level is <0.4V quiescent, $>$ 2.4V active into a 50Ω termination. Levels are reversed for the complement pulse.

⑧ **$\overline{\text{TTL}}$ OUT Connector** – An output like the TTL output ⑦ except active and quiescent levels are reversed.

⑨ **SYNC OUT Connector** – A TTL level output from a 50Ω source. Square wave in all modes except external width and external trigger modes, in which pulse width is determined by trigger pulse width.

⑩ **TRIG GATE INPUT Connector** – Accepts an external TTL level signal to trigger or gate the generator. Triggers on rising edge of input. Gates off when level is at a TTL low level.

⑪ **POWER Switch** – Pulse generator on/off switch features red power-on indicator light and black/white changing switch surface for off/on indication.

3.2 NOTES ON OPERATION

3.2.1 Modes

The following modes of operation are available and selectable as described herein.

Continuous – For a continuous stream of pulses, the PERIOD switch must be in any position except TRIG or MAN TRIG and the TRIG GATE INPUT BNC must be free of input signals and 50Ω terminations.

Triggered – For a pulse, or pulse pair, triggered by an external signal, the PERIOD switch must be set to TRIG and a TTL level square pulse must be present at the TRIG GATE INPUT. Triggering occurs on the trigger pulse rising edge.

Manually Triggered – For a pulse, or pulse pair, triggered by the MAN TRIG switch, the PERIOD switch must be set to MAN TRIG.

Gated – For continuous pulses for the duration of a gate signal, the PERIOD switch must be in any position except TRIG or MAN TRIG and a TTL level square pulse must be input to the TRIG GATE INPUT BNC. For manual gating, place a 50Ω termination on the TRIG GATE INPUT BNC to disable the generator output. Push the MAN TRIG switch to gate an output.

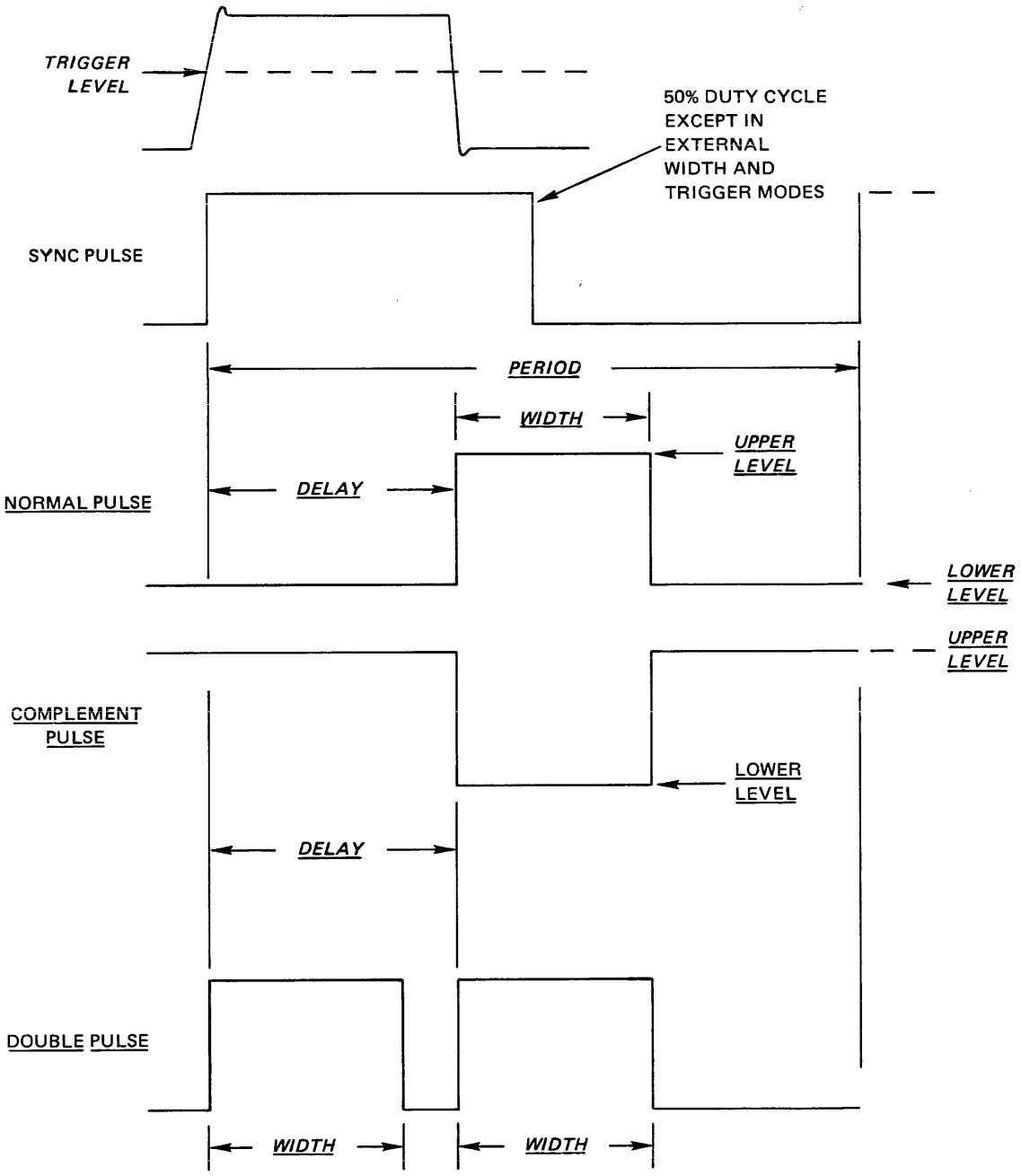
External Width – For pulses whose widths are determined by an external signal, the PERIOD switch must be set to TRIG and the WIDTH switch must be set to ⊓⊔ .

3.2.2 White Marks

When first becoming familiar with the 802, the white mark settings are handy. The white mark settings for the front panel switches will always give a 50 to 500 kHz sync signal when power is on. The same settings will give 50% duty cycle TTL, $\overline{\text{TTL}}$ and output pulses; the LOWER LEVEL/ UPPER LEVEL control may need adjusting to observe the output on an oscilloscope. Once the output is observed, each control can be adjusted and observed until the desired result is obtained.

3.2.3 Pulse Width and Delay

Narrow duty cycle pulses require a normal output (COMP OFF) while greater than 70% duty cycle pulses require the COMP ON setting to allow the width circuitry sufficient recovery time. When using DELAY time, ensure that delay $\leqslant$ 70% of PERIOD and width $\leqslant$ 70% of PERIOD.



NOTE: Underline indicates a front panel controlled parameter.

Figure 3-2. Pulse Parameters

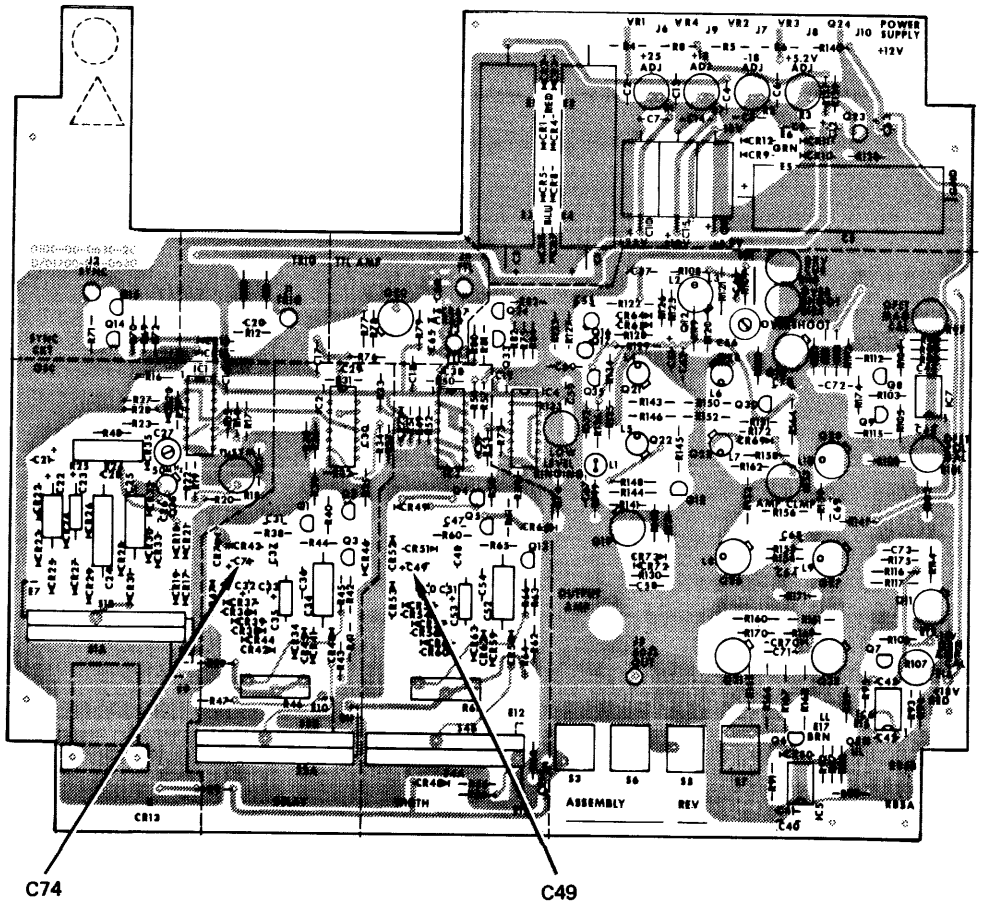


Figure 3-3. Placement of Customer Option Capacitors

The ⊓⊔ width setting gives a 50% duty cycle in continuous mode, when TRIG or MAN TRIG is selected on the PERIOD switch, the pulse width is determined by the trigger signal width. This is external width mode of operation.

Table 3-1. Capacitance and Range

Delay or Width Range	Capacitance
10 ns - 100 ns	None
100 ns - 1 μs	2000 pF
1 μs - 10 μs	0.02 μF
10 μs - 100 μs	0.2 μF
0.1 ms - 1 ms	2.0 μF
1 ms - 10 ms	20 μF
10 ms - 100 ms	200 μF
0.1s - 1s	2000 μF

The unmarked detent on the DELAY switch and WIDTH switch can be any desired range by placing appropriate capacitors on the circuit board, as shown in figure 3-3. Refer to table 3-1 for typical capacitance and range.

3.2.4 Output Terminations

Only 50Ω RG58U cables should be used to connect the 802 to the circuit under test. Either the INT 50Ω should be ON or a 50Ω 2W load should be used at the circuit end of the cable. For best pulse fidelity, a 50Ω load at both the source and the load is required.

As shown in figure 3-4, the combinations of load and source impedances determine the output pulse amplitude range

SOURCE	LOAD	DYNAMIC RANGE	AMPLITUDE	
			MAXIMUM	MINIMUM
50Ω	50Ω	+5V	5V	.5V
		−5V		
* 1 kΩ	50Ω	+10V	10V	1V
OR				
50Ω	⩾1 kΩ	−10V		

*1 kΩ is the unterminated source impedance of the OUTPUT.

Figure 3-4. Load and Source Terminations

and the dynamic range. As shown, when a greater than 5V pulse is desired, only one 50Ω termination can be used, and the placement of the termination can optimize the pulse purity. In this case, the capacitance of the circuit being driven must be considered. For capacitive loads greater than 20 pF, reflections on the line are most effectively absorbed by the 50Ω termination at the 802 (INT 50Ω switch ON). For capacitive loads less than 20 pF, the 50Ω termination should be placed at the load side of the line. When a less than 5V pulse is required, a 50Ω termination at each end of the line is recommended for optimum pulse purity.

The 50Ω terminations should always be used on the SYNC, TTL and $\overline{\text{TTL}}$ outputs.

3.2.5 Duty Cycle

Always use the lowest range possible for both delay and width functions. This will reduce the recovery time of the circuit one-shots and extend the maximum duty cycle of the 802 to its fullest capability.

3.2.6 Output Mixing

By triggering a second 802 from the sync output of the first 802 and then mixing their outputs in a common load, three level signals can be created, as shown in figure 3-5.

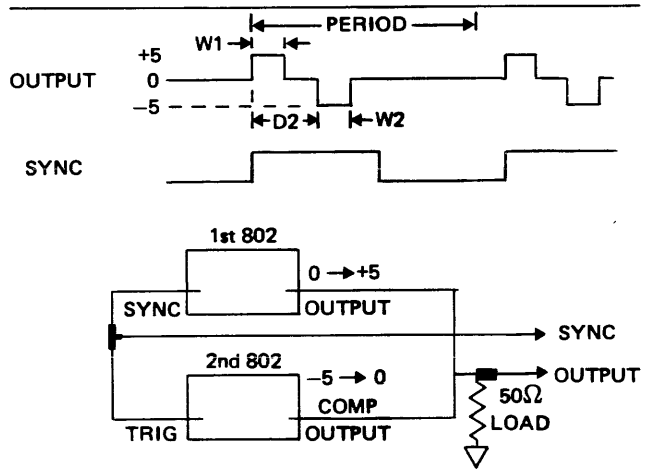


Figure 3-5. Output Mixing

3.2.7 Precise Output Levels

Many times when testing a circuit, it is desirable to lock the output of the generator at either the high or low level. A precise measurement of this level may then be obtained using a DVM.

To lock the output at high or low level, select EXT TRIG and ⊓⊔ with no TRIG GATE INPUT. Use the COMP ON/OFF switch to select high and low level outputs.

3.2.8 Fixed Delay

A fixed delay of 20 ns has been incorporated within the 802 to ensure that the leading edge is visible on the scope. If this delay is not desired, simply increase the length of the sync cable coax at the rate of 1.5 ns/ft to obtain the desired result.

3.2.9 Two Phase Clocking

If a secondary 802 is triggered by the sync out from the primary 802, a two phase nonoverlapped clock source can be obtained as shown in figure 3-6.

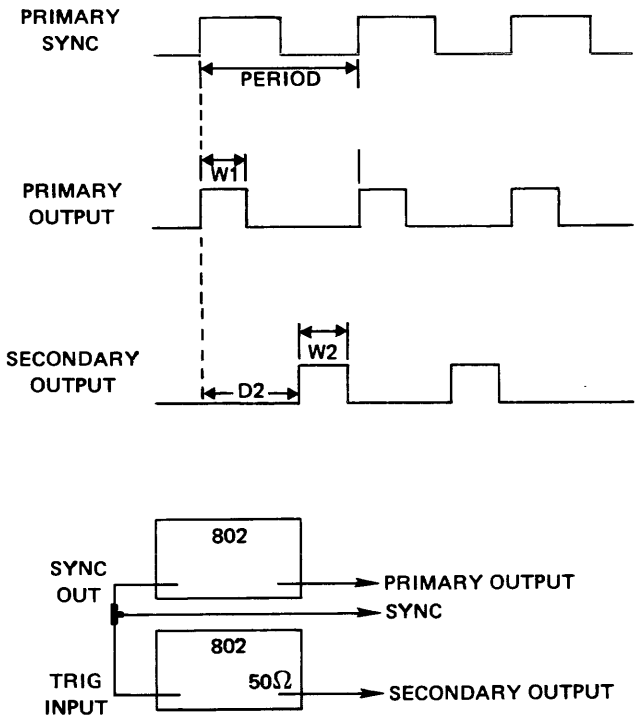


Figure 3-6. Two Phase Clock Generation

3.2.10 Rise Time Measurements

When measuring rise time in a linear device under test, the error induced by the rise time of the testing system must be considered. For example, when observing the 802 rise time on an oscilloscope, 802 rise time is

$$t^2_{observed} = t^2_{scope} + t^2_{802}$$

or

$$t_{802} = \sqrt{t^2_{observed} - t^2_{scope}}$$

That is, the observed rise time must be corrected for by the inherent oscilloscope rise time to determine the actual 802 rise time. Extending the method to include a circuit under test will determine circuit under test rise time:

$$t^2_{observed} = t^2_{802} + t^2_{scope} + t^2_{c.u.t.}$$

or

$$t_{c.u.t.} = \sqrt{t^2_{observed} - t^2_{802} - t^2_{scope}}$$

3.3 OPERATION

In the following descriptions of operation, observe the pulse on an oscilloscope. In continuous mode, trigger oscilloscope on SYNC OUT. In all other modes, trigger on the trigger signal. (See figure 3-2 for pulse parameters.)

Observe the following constraints:

Delay $\leqslant$ 70% of period.
Width $\leqslant$ 70% of period.

3.3.1 Continuous Pulses

Set the controls (and connectors) as follows:

Control	Operation
TRIG GATE INPUT Connector	No signal present
INT 50Ω Switch	ON
PERIOD Switch	Desired range setting
Other Controls	Set as desired

3.3.2 Wide Duty Cycle Pulses

For wider pulses than those that can be normally obtained, set up for a pulse with the complemented width, then press the COMP pulse switch ON. For example, if a 95 ns pulse with a 125 ns repetition rate is desired:

$$125 \text{ ns} - 95 \text{ ns} = 30 \text{ ns}$$

Set up for a 30 ns pulse, then press the COMP switch ON. (See figure 3-7.)

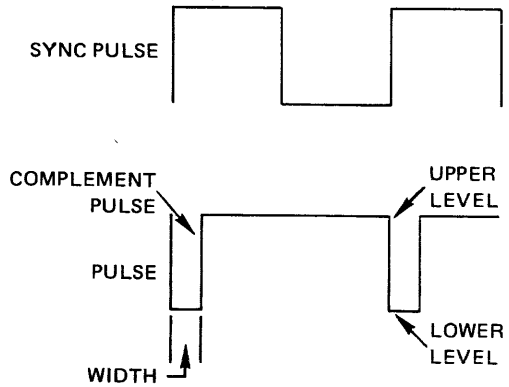


Figure 3-7. Greater Than 70% Duty Cycle Pulse

3.3.3 Externally Triggered Pulses

Set controls (and connectors) as follows:

Control	Operation
PERIOD Switch	TRIG
TRIG/GATE INPUT Connector	Apply TTL rectangular pulse
INT 50Ω Switch	ON
WIDTH Switch	Set to range desired (but not ⌜⌞)
Other Controls	Set as desired.

3.3.4 Manually Triggered Pulses

Set controls (and connectors) as follows:

Control	Operation
PERIOD Switch	MAN TRIG
INT 50Ω Switch	ON

Control	Operation
WIDTH Switch	Set to range desired (but not ⊓⊔)
MAN TRIG	Push to trigger
Other Controls	Set as desired

3.3.5 Gated Pulses

Set up as in paragraph 3.3.1, except set the width of the TRIG GATE INPUT pulse to allow the desired number of output pulses.

3.3.6 Pulses With Width Controlled Externally

Set up as in paragraph 3.3.3, except set WIDTH switch to ⊓⊔ .

3.3.7 Double Pulses

For double pulses in any mode, additionally set controls as follows:

Control	Operation
DBL PULSE	ON
DELAY	Set for desired time between start of first pulse and second pulse of pulse pairs. (Since the same one-shot forms both pulses, a minimum recovery time is necessary.)

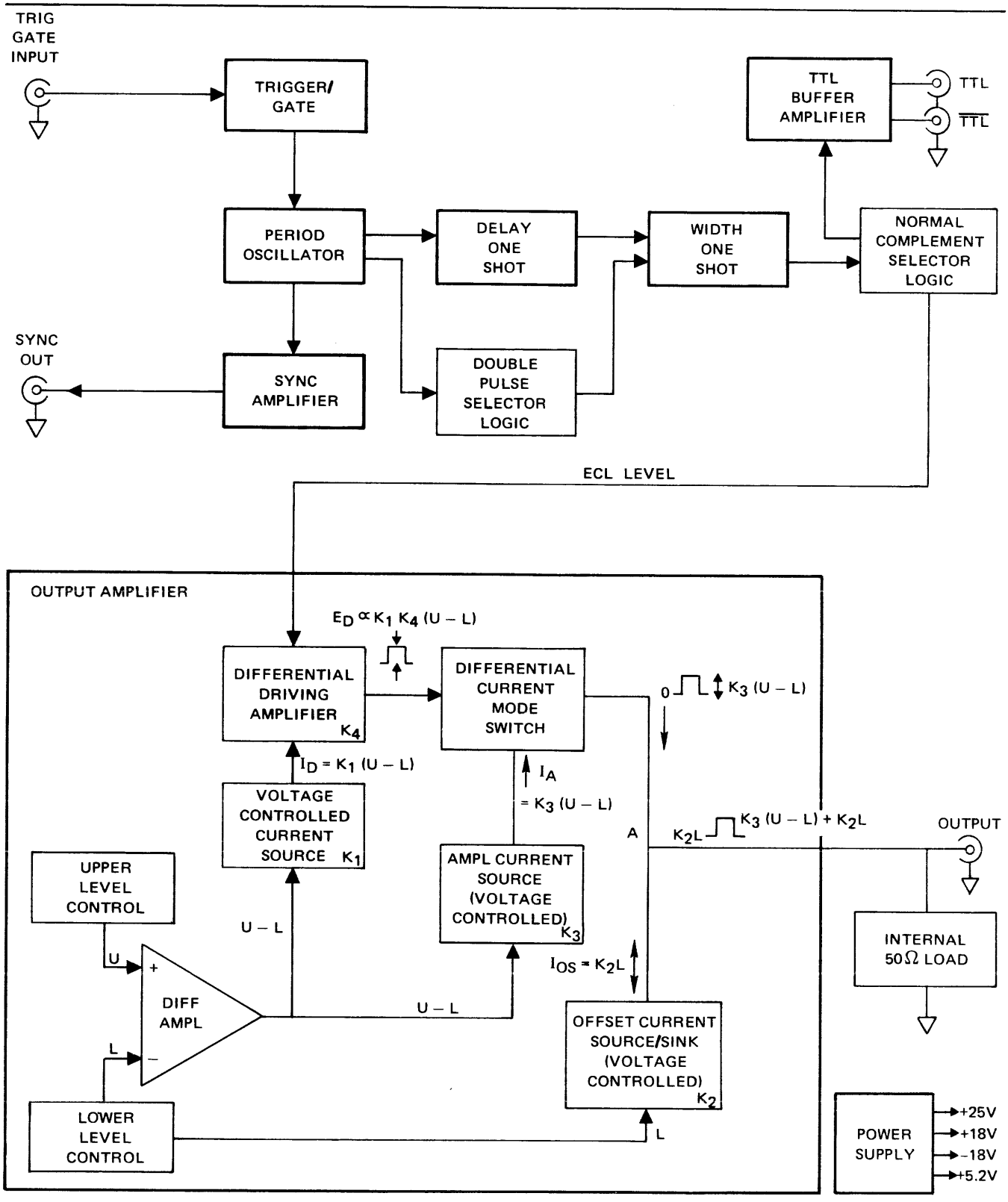


Figure 4-1. Overall Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 OVERALL BLOCK DIAGRAM

The Model 802 is made up of eight major circuit blocks: trigger/gate circuit, period oscillator, sync amplifier, delay one shot, width one shot, TTL buffer amplifier, output amplifier, and a power supply. (See figure 4-1.)

All the circuitry is on one PC board with a combination of ECL logic gates and discrete semiconductor devices. The ECL logic, in addition to making up individual circuit blocks, serves as a signal coupling medium between the blocks. The signal path changes depending on the mode selected.

4.2 PERIOD OSCILLATOR

A simplified diagram of the period oscillator, an ECL multivibrator, appears in figure 4-2.

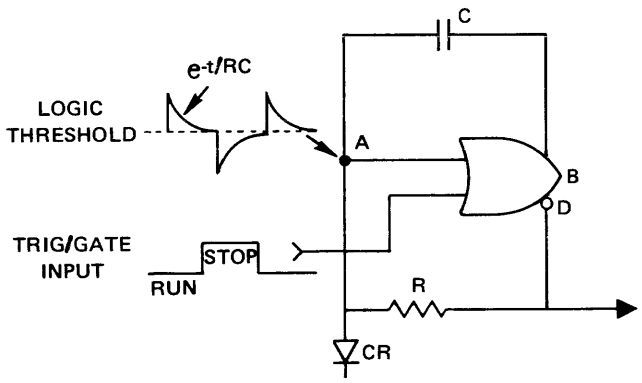


Figure 4-2. Simplified Diagram of the Period Oscillator

The RC time constant determines the charge and discharge rates for capacitor C and, therefore, the frequency of operation.

Positive feedback via the path through C results in a stable oscillator. Varying resistor R changes the frequency over a 10:1 range. Note that since the charging and discharging current are equal but opposite, the resulting waveform has a 50% duty cycle.

The oscillator may be gated via the trig/gate input. Whenever this input is high, it forces output D low and stops the oscillator. The oscillator starts synchronously when the input goes low.

4.3 TRIGGER/GATE CIRCUIT

The trigger circuit consists of an ECL gate connected to provide positive feedback which forms a Schmitt trigger. An input divider adjusts the trigger level to approximately +1.4V. This makes the input compatible with TTL logic. Triggering always occurs on the positive edge and the source can be either external or internal via the manual trigger switch.

The output of the trigger circuit is always connected to the oscillator. Gating occurs automatically. Whenever the input to the trigger circuit is 1.4V, it forces the trig/gate input of the oscillator high (figure 4-2) and stops the oscillator.

When the trigger mode is selected, node A of the oscillator is pulled low via diode CR. The IC now acts as an inverter to the trig/gate input and passes the signal on to the delay one shot.

4.4 SYNC CIRCUIT

The sync circuit acts as a buffer amplifier between the oscillator and the external equipment. It provides a TTL output level from a 50Ω source. The output from the sync circuit is an approximate square wave at the oscillator frequency.

When gating the generator, the sync signal should be taken from the gating source rather than the 802.

4.5 DELAY CIRCUIT

The delay one shot allows an adjustable time between the sync output and the leading edge of the final output pulse. The delay circuit consists of an ECL gate and discrete circuit one shot multivibrator. When the delay circuit is triggered by the oscillator, a timing capacitor is discharged by a constant current source until a threshold point is reached. The circuit then resets by rapidly recharging the timing capacitor. The output pulse from the ECL gate has a width proportional to the timing capacitor value and the magnitude of the current source. The pulse width is independent of the triggering rate as long as it is less than 70% of the trigger period.

4.6 WIDTH CIRCUIT

The width one shot determines the width of the output pulse. The width circuit, triggered by the trailing edge of the delay one shot, is identical in operation to the delay circuit. In the double pulse mode it is triggered on the leading and trailing edges of the delay one shot pulse. When the mode is selected, the delay and width one shots are disabled and the oscillator square wave passes through them to the output amplifier. An exclusive OR gate allows either phase of the width one shot output to be selected as the signal to drive the output amplifier.

4.7 TTL BUFFER AMPLIFIER

The output of the width one shot drives a current mode switch, the TTL buffer amplifier, in addition to the output amplifier. This switch is designed to drive TTL level signals into 50Ω loads. Both signal phases, TTL and $\overline{\text{TTL}}$, are available simultaneously.

4.8 OUTPUT AMPLIFIER

The output amplifier (figure 4-1) establishes the pulse lower level by passing a constant current through the 50Ω load. The current is provided by a voltage controlled current source programmed by the lower level control potentiometer. A current pulse of the proper amplitude is now added at node A to this base line for the duration of the width one shot time. The amplitude of the current pulse is equal to the difference between the upper and lower level controls (U – L). The upper level will be (U – L) + L = U at the output.

In order to generate a current pulse, the width one shot drives a current mode switch via a driving amplifier. The current mode switch connects a current source to the load whenever the output of the width one shot is high. The current source is voltage controlled and its output is equal to the difference between the upper and lower level controls (U – L).

The output of the driving amplifier varies in amplitude directly with the output level programmed by the level controls. This prevents overdriving the current mode switch and distorting the output at low levels.

Note that changing the lower level control will change both the base line and the current pulse amplitude which will cause the upper level to remain fixed. That is (U – L) + L = U, regardless of the value of L.

The internal 50Ω load may be switched in or out depending on the application.

4.9 POWER SUPPLY

The power supply converts the line voltage to four regulated dc voltages which power all the other circuit blocks.

4.10 MODES OF OPERATION

The major circuit block connections depend on the mode of operation selected. Block diagrams of the major modes and key waveforms are shown in figures 4-3 through 4-8.

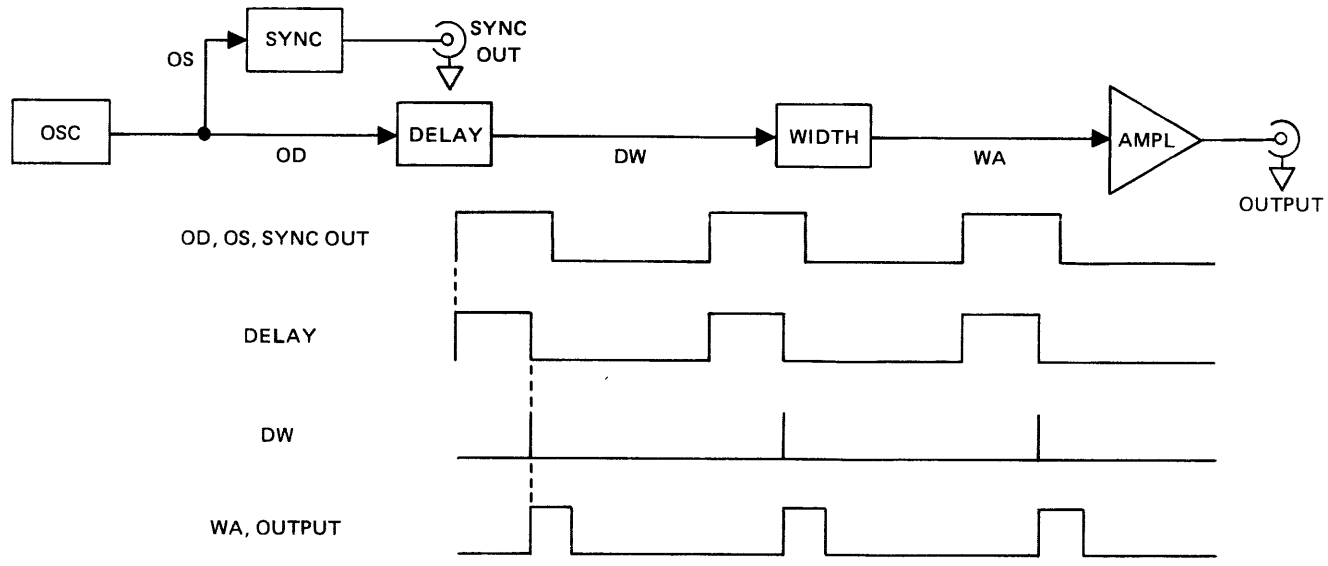


Figure 4-3. Continuous Mode

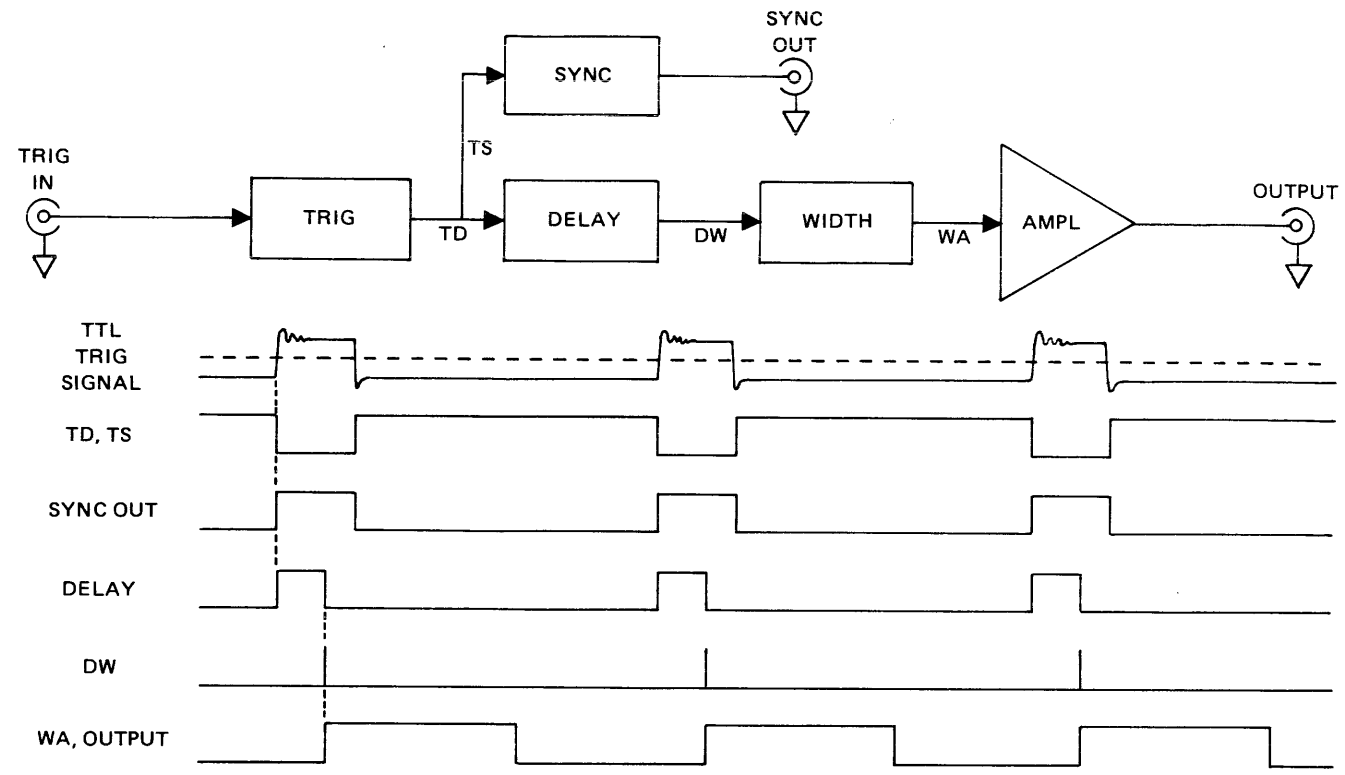


Figure 4-4. Trigger Mode

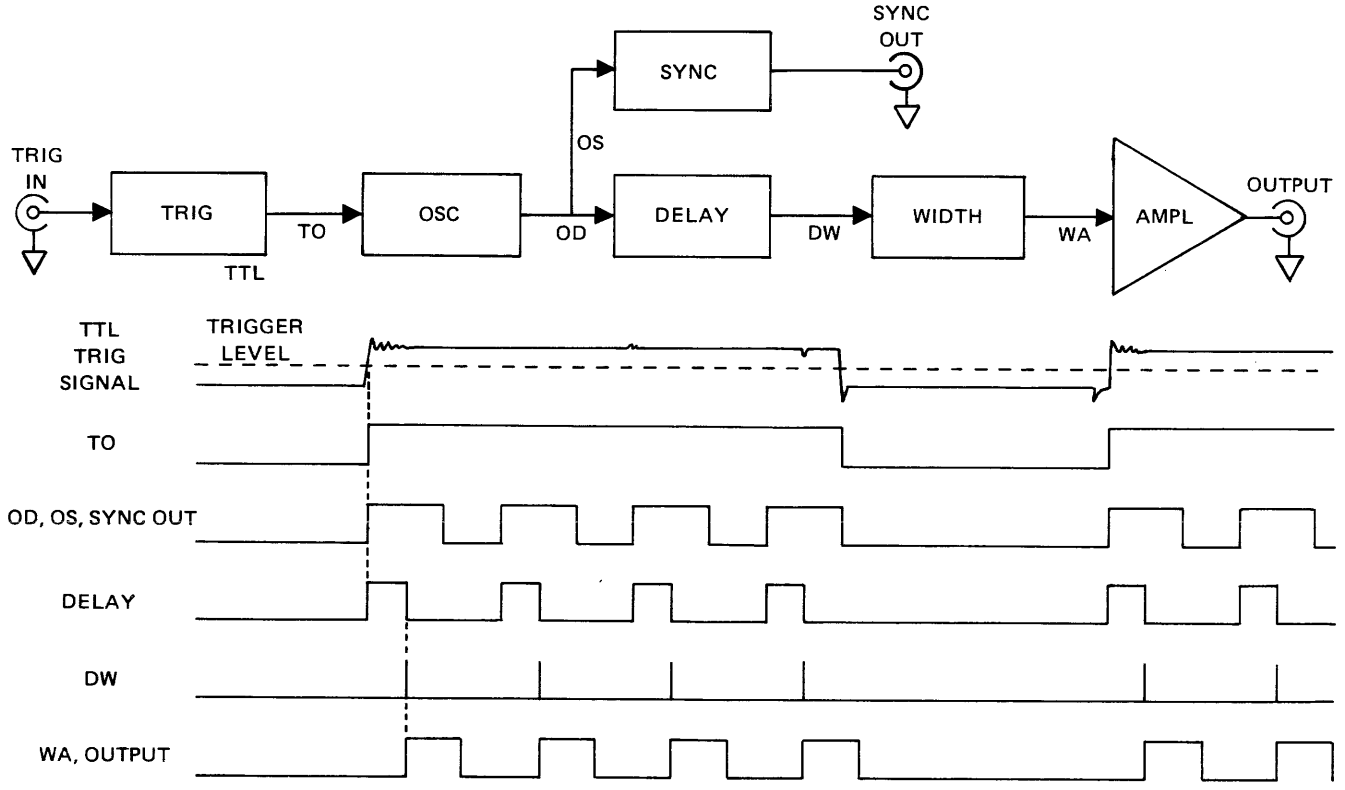


Figure 4-5. Gate Mode

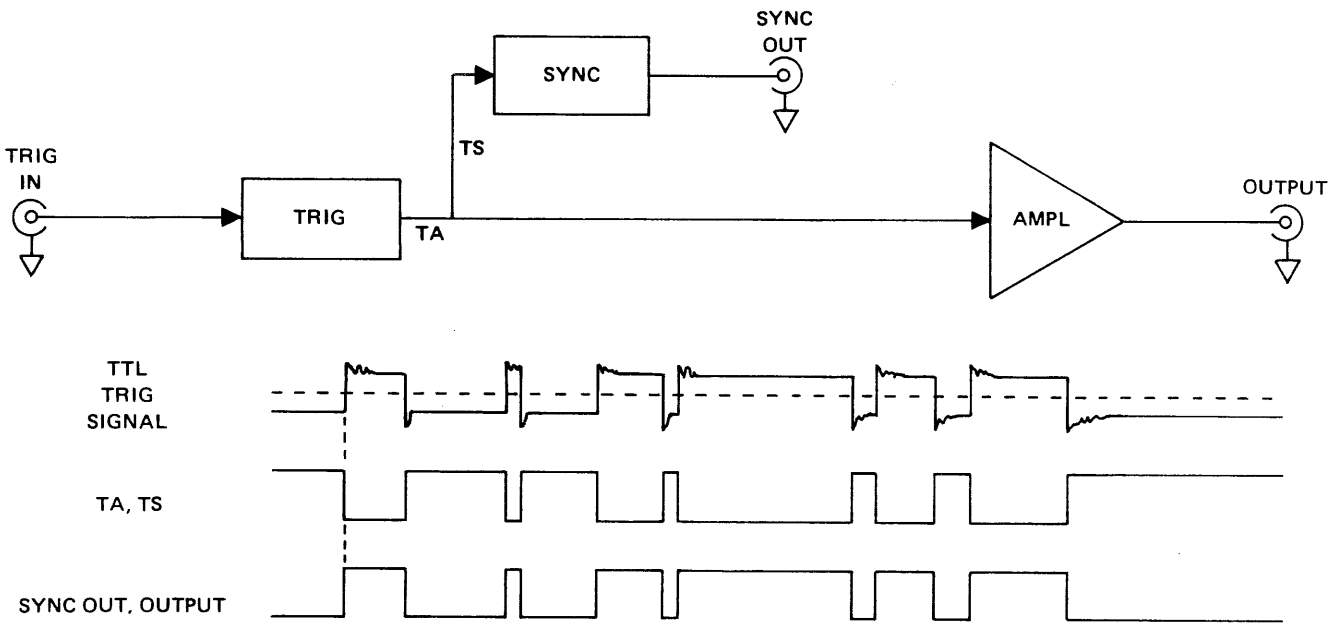


Figure 4-6. External Width Mode

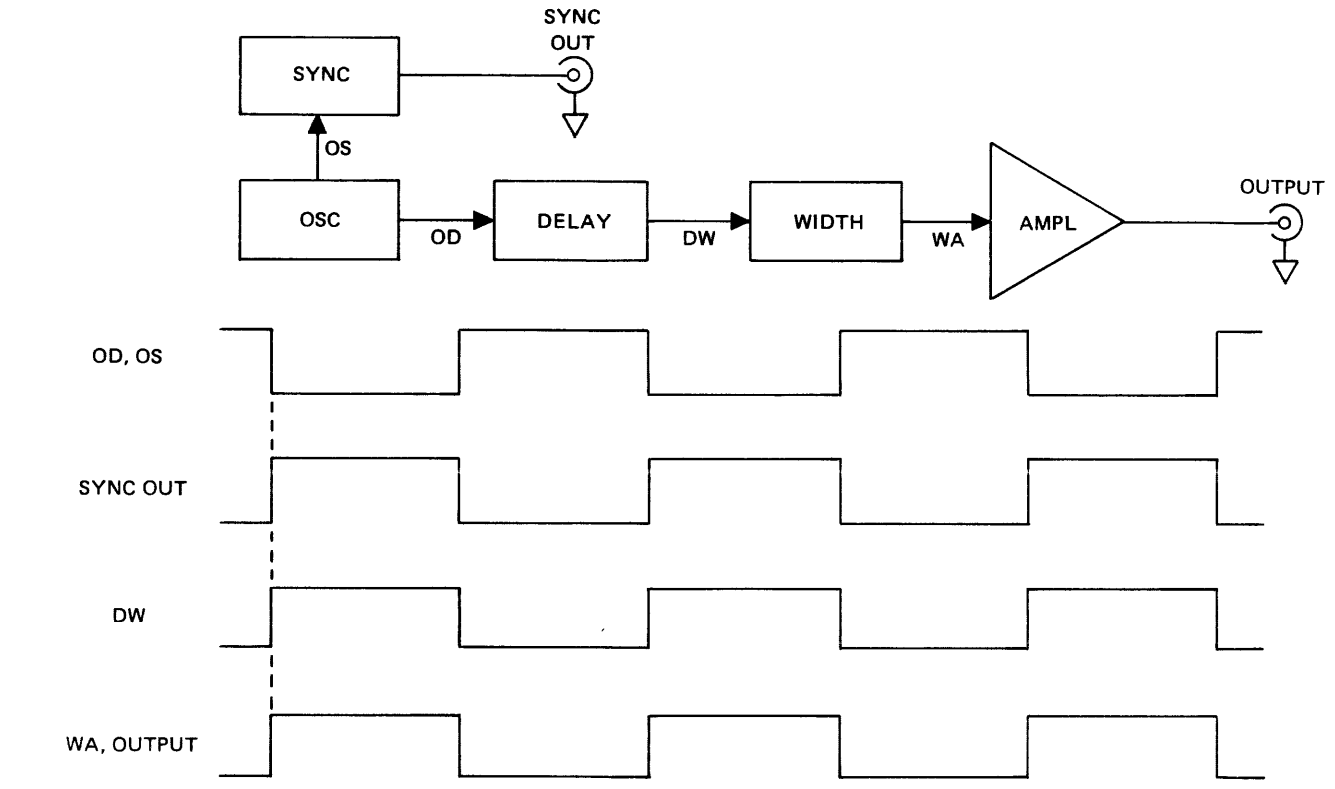


Figure 4-7. Continuous Square Wave Mode

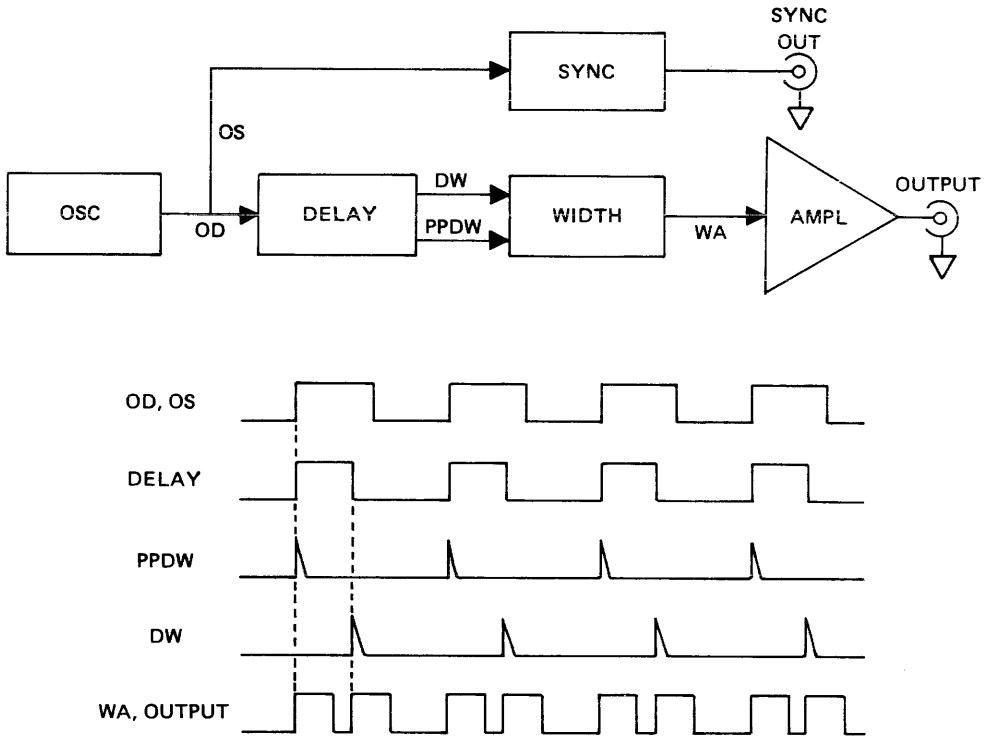
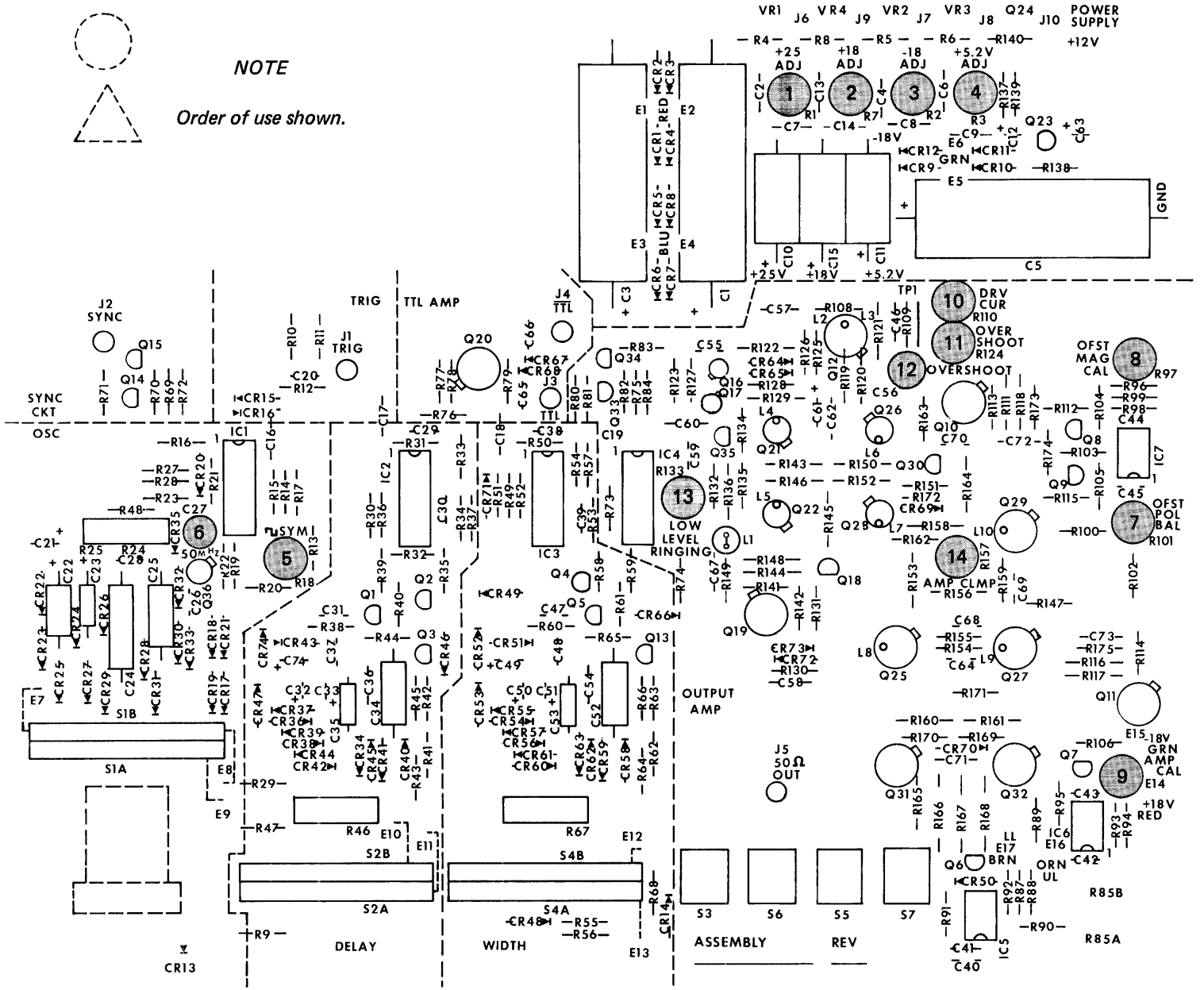


Figure 4-8. Continuous Double Pulse Mode



MOD 802
0100-00-0630-3C

Figure 5-1. Calibration Points

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those custormers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter . . . . Millivolt dc measurement (0.1% accuracy)
Oscilloscope, Dual Channel . . . . . 500 MHz bandwidth
Oscilloscope, Sampling . . . . . 1 GHz bandwidth
Counter . . . . . 55.0 MHz (0.01% accuracy)
50Ω Feedthru . . . . . ±0.1% accuracy, 2W (3 ea)
10X 50Ω Feedthru Attenuator . . . . . ±0.1% accuracy, 2W
Function Generator . . . . . 5 kHz ∿ , 4V p-p
RG58U Coax Cable . . . . . 3 ft length BNC male contacts
BNC Tee . . . . . 1 male, 2 female connectors

5.3 REMOVING GENERATOR COVERS

1. Invert the instrument and remove the four screws in the cover.

2. Turn the instrument upright, remove the top cover, and remove the four screws securing the bottom cover.

3. Replace the cover and turn the instrument upside down.

NOTE

Remove the cover only when it is necessary to make adjustments or measurements.

5.4 CALIBRATION

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1. If performing partial calibration, check previous settings and adjustments for applicability. See figure 5-1 for calibration point location. location.

1. Unless otherwise noted, all measurements made at the TTL, $\overline{\text{TTL}}$ or OUTPUT connectors must be terminated into a 50Ω (±0.1%) load.

2. Start the calibration by connecting the unit to an ac source and setting the front panel switches as follows:

PERIOD . . . . . 200 ns ▮ 2 μs
PERIOD VERNIER . . . . . Full cw
PULSE MODE . . . . . OFF
DELAY . . . . . OFF
WIDTH . . . . . ⊓
LOWER LEVEL . . . . . −10V
UPPER LEVEL . . . . . +10V

3. Allow the unit to warm up at least 30 minutes for final calibration. Keep the instrument covers on to maintain heat. Remove covers only to make adjustments or measurements.

Table 5-1. Calibration Chart

Step	Check	Tester	Cal Points	Control Settings	Adjust	Desired Results	Remarks
1	Power Supply	DVM	–	–	R1	+25V ±0.10V	
2			–	–	R7	+18V ±0.05V	
3			–	–	R2	−18V ±0.05V	
4			–	–	R3	+5.2V ±0.05V	

Table 5-1. Calibration Chart (Continued)

Step	Check	Tester	Cal Points	Control Settings	Adjust	Desired Results	Remarks
5	Duty Cycle	Scope	TTL	R157: Full cw	R18	50% duty cycle ±0.5%	
6				PERIOD: 20 ns ▮ 200 ms PERIOD VERNIER: Full ccw	C27	51 MHz (19.6 ns)	
7	Output Amplifier	DVM	OUTPUT	PERIOD: TRIG COMP: ON LOWER LEVEL: Full cw, then full ccw	R101	Equal cw & ccw voltage	
8				LOWER LEVEL: Full cw	R97	+10.5V ±0.05V	Repeat steps 7 and once.
9				LOWER LEVEL: 0V on DVM			Loosen and realign LOWER LEVEL knob at 0V, if necessary.
10				UPPER LEVEL: Full cw COMP: OFF	R107	+10.5V ±0.05V	
11				UPPER LEVEL: 0V on DVM			Loosen and realign UPPER LEVEL knob at 0V, if necessary. Make sure mechanical interlock on knob is engaged.
12			TP1	UPPER LEVEL: Full cw	R110	−0.6V ±0.05V	
13	Overshoot & Ringing	Scope	OUTPUT	INT 50Ω: ON LOWER LEVEL: 0V	R124 C56	Minimum overshoot & ringing	
14				UPPER LEVEL: +0.5V	R133	Minimum ringing	Repeat steps 13 and 14 once.
15	Overshoot & Rise Time			UPPER LEVEL: Full cw LOWER LEVEL: Make a +5V pulse	R157	Minimum overshoot	Maintain ≥ 5.1V pulse and ≤ 5 ns rise time. A slight readjustment of R110 may be necessary.

SECTION 6
TROUBLESHOOTING

6.1 INTRODUCTION

This section is organized as follows:

Safety
Circuit Board Access
Basic Techniques
Troubleshooting Individual Components
Flow Charts

Refer to paragraph 5.2 for required test equipment.

NOTE

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 SAFETY

6.2.1 Precautions

Refer all servicing and calibration to a qualified electronic technician.

Always disconnect the power cord when working on this instrument, unless electrical measurements are being taken. Never attempt to isolate the safety ground lug of the power cord.

Be sure that the fuse rating is correct and that the line voltage selector card is set to the proper range (refer to section 2).

Line voltage is present on the circuit board of the ac power connector, *even when the power switch is off*. This voltage is only accessible if the shield is removed from the ac power connector.

6.2.2 Safety Check

Disconnect the power cord from facility power and check that the resistance from the cord earth ground terminal to the instrument front panel metal is less than one ohm. Press the power switch on an measure the resistance between the instrument front panel metal and each of the power cord's two matching terminals. Resistance to each terminal should be greater than two megohms. Check the fuse for proper type and value. Remove the instrument covers and inspect the power supply and circuit boards for evidence of overheating or arcing. Check lines and cables for good physical connections. Correct any discrepancies detected.

6.3 CIRCUIT BOARD ACCESS

Remove the top cover (paragraph 5.3) for access to the circuit board. Remove the four screws securing the board to the bottom cover for access to the bottom of the board.

6.4 BASIC TECHNIQUES

Troubleshooting requires no special technique. Listed below are a few reminders of basic electronic fault isolation.

1. Check control settings carefully. Many times a seemingly malfunction is an incorrect control setting, or a knob that has loosened on its shaft.

2. Check associated equipment connections. Make sure that all connections are securely connected to the correct connector.

3. Perform the calibration procedure. Many out-of-specification indications can be corrected by performing specific calibration procedures.

4. Visually check the interior of the instrument. Look for such indications as broken wires, charred components and loose leads.

5. Try to isolate the problem to a specific circuit by checking generator operation in all modes and referring to the block diagrams for each mode (see figures 4-3 thru 4-8). After the problem has been isolated to a specific stage, check the dc operating voltages at the pins of all solid state devices within that stage.

6. Check the associated passive elements with a high impedance ohmmeter (instrument unplugged) before replacing a suspected semiconductor device.

6.5 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.5.1 Transistor

A transistor is defective if more than one volt is measured across its base emitter junction in the forward direction.

A transistor when used as a switch may have a few volts reverse bias voltage base to emitter.

If the collector and emitter voltages are the same, but the base emitter voltage is less than 500 mV forward voltage (or reversed bias), the transistor is defective.

A transistor is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).

6.5.2 Diode

A diode is defective if there is greater than 1 volt (typically 0.7 volts) forward voltage across it (except Zener and LED).

6.5.3 Operational Amplifier

The "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.

If the output voltage stays at maximum positive, "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.5.4 FET Transistor

No gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective.

The gate-to-source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485, and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.

6.5.5 MOSFET Transistor

For MOSFET's such as the SD214 or SD215, a positive gate source voltage causes the device to conduct drain current. Zero volts or a negative voltage cause the device to pinch off. A MOSFET transistor can be damaged by a static charge buildup when out of the circuit. Keep MOSFET leads shorted together until soldered in the circuit board.

6.5.6 Capacitor

Shorted capacitors have zero volts across their terminals.

An unopened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

6.5.7 ECL Gate

The emitter coupled logic using NOR logic is:

Inputs		NOR Output	Exclusive OR Output
A	B	$C = A + B$	$C = \overline{A \oplus B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	1

The levels are:

"0" = +3.4V ±0.1V
"1" = +4.3V ±0.1V

Never short the output of an ECL gate to ground; this will damage the output transistor in the gate. Any input may be pulled high, even when driven by an output of another gate, by connecting a diode between the input and the +5.2V supply (anode to supply).

6.6 FLOW CHARTS

The flow charts (see figures 6-1 thru 6-6) help isolate any malfunction to a specific stage. If you already know the specific circuit block at fault, go directly to that block in the flow chart. If a problem cannot be isolated to a portion of a flow chart, then follow the flow chart from the beginning.

If the problem cannot be located, return the instrument to the factory for servicing, with a description of the failure.

Before performing flow chart troubleshooting, set the front panel controls as follows:

PERIOD . . . . . 2 μs ▮ 20 μs
PERIOD VERNIER . . . . . 12 o'clock
DELAY . . . . . 10 ns ▮ 100 ns
DELAY VERNIER . . . . . 12 o'clock
WIDTH . . . . . 100 ns ▮ 1 μs
WIDTH VERNIER 12:00
LOWER LEVEL . . . . . −10V
UPPER LEVEL . . . . . +10V
DBL PULSE . . . . . OFF
COMP . . . . . OFF
INT 50Ω . . . . . ON

Connect both the sync and the output BNC's to an oscilloscope with 3 foot 50Ω cables terminated with 50Ω feedthroughs.

When troubleshooting the output amplifier, the flow chart in figure 6-6 should be followed. In addition, tables 6-1 and 6-2 provide additional guidance as to what voltages exist at the semiconductor devices and how they should vary with the output level controls.

Table 6-1. Level Control Dependent Voltages

Level Control Knob Setting	Output Waveform Into 50Ω	E17 Voltage Upper Level	E16 Voltage Lower Level	TP1	IC7-6	Emitter of Q6	Emitter of Q19
	+10 ———	−18	−18	−18	−3.6	+8.1	+22
	+10 0	−18	0	−0.6	0	+8.1	+22
	+ 5 − 5	−9	+9	−0.6	+1.8	+8.1	+22
	0 ———	0	0	−18	0	0	+25
	0 −10	0	+18	−0.6	+3.6	+8.1	+22
	−10 ———	+18	+18	0	+3.6	0	+25

Table 6-2. Transistor Voltages

NOTE

These voltages apply with the controls set as follows.

PERIOD . . . . . *TRIG*
DELAY . . . . . *OFF*
WIDTH . . . . . ⊓
COMP . . . . . *OFF*
DBL PULSE . . . . . *OFF*
INT 50Ω . . . . . *ON*
UPPER LEVEL . . . . . *Max cw*
LOWER LEVEL . . . . . *OV*

Transistor	B	C	E	Transistor	B	C	E
Q6	+8.7	+20.8	+8.1	Q22	+18.6	+12	+20.5
Q7	−0.6	−0.6	0	Q23	+10.8	0	+11.4
Q8	0	+18	≈0	Q24	+11.4	0	+12.0
Q9	0	−18	≈0	Q25	+12.0	+10.0	+12.6
Q10	+18	+13	+18	Q26	+15.2	+13.0	+15.8
Q11	−18	−13	−18	Q27	+12.0	+10.0	+12.6
Q12	−0.6	+0.3	−1.2	Q28	+15.2	+13.0	+15.8
Q16	+4.3	+6.4	+3.7	Q29	+12.0	+10.0	+12.6
Q17	+3.4	+9.8	+3.7	Q30	+14.6	+12.0	+15.2
Q18	+20.8	21.4	+21.4	Q31	−12.0	+10.0	−12.6
Q19	+21.4	21.4	+22.0	Q32	−12.0	+10.0	−12.6
Q21	+18.6	+12	+20.5	Q35	+18.0	+12.0	+18.6

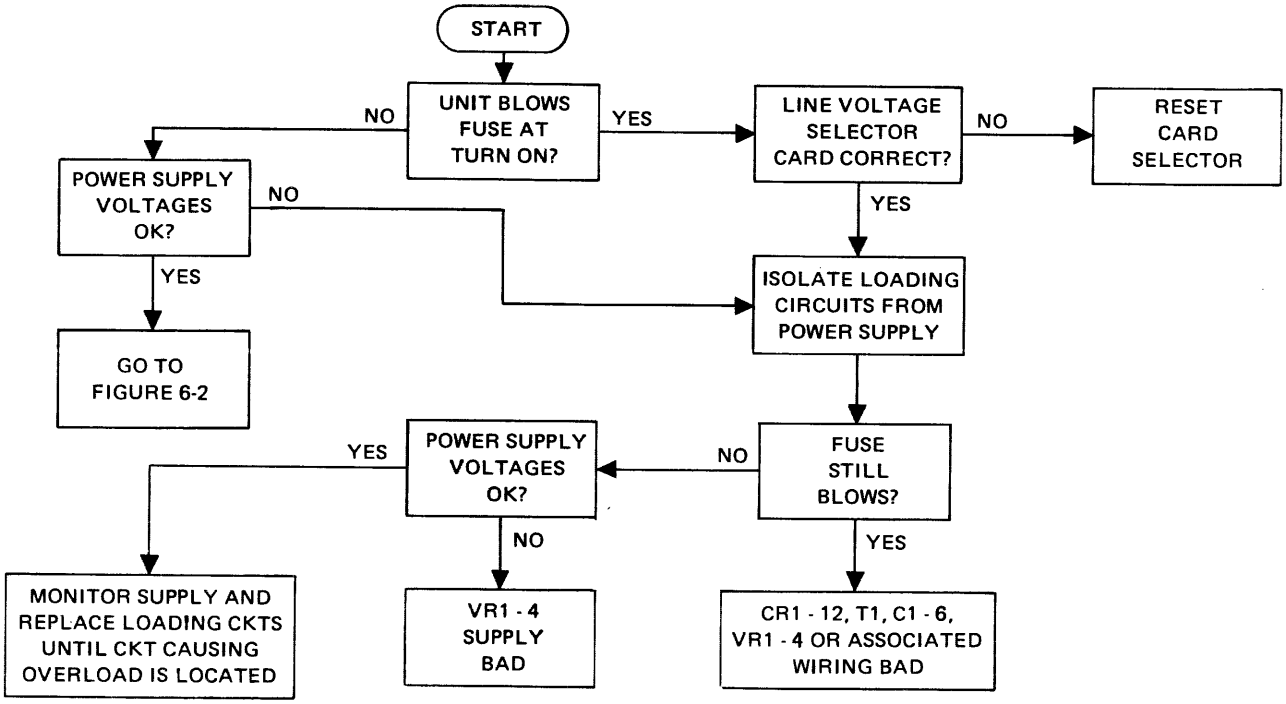


Figure 6-1. Power Supply Troubleshooting

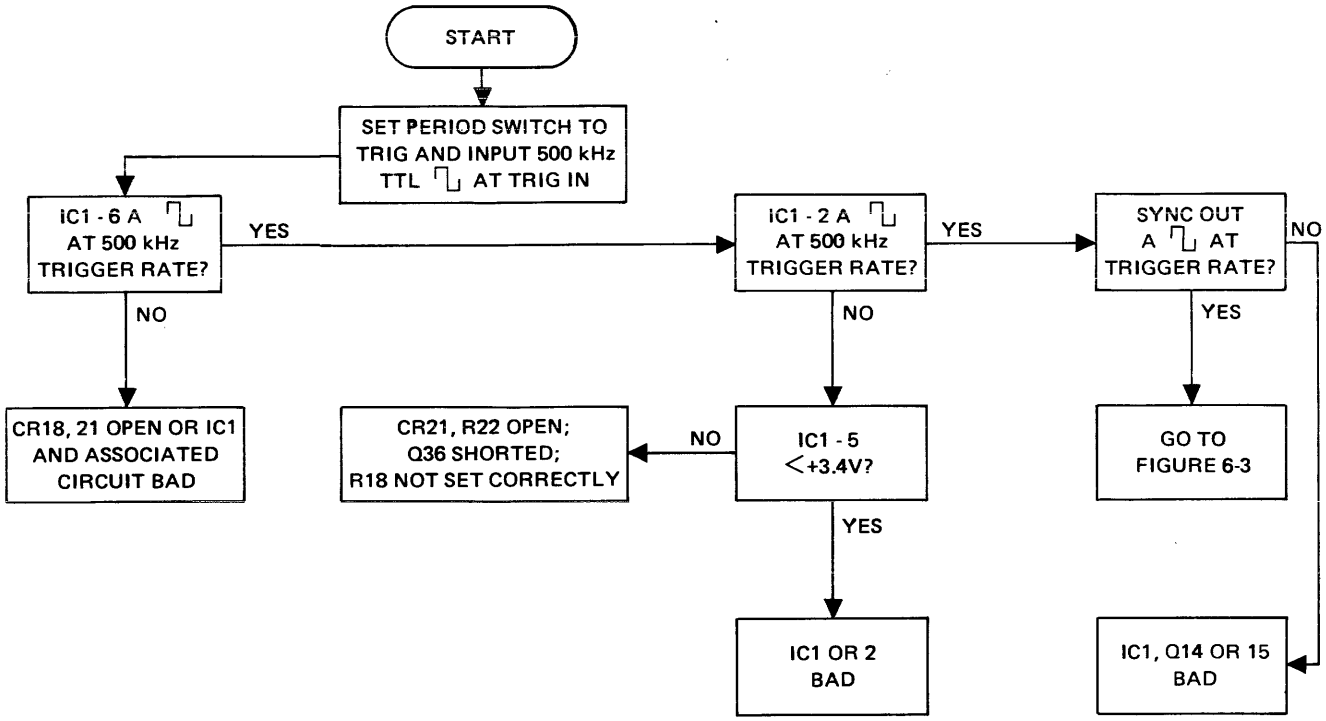


Figure 6-2. Trigger Circuit Troubleshooting

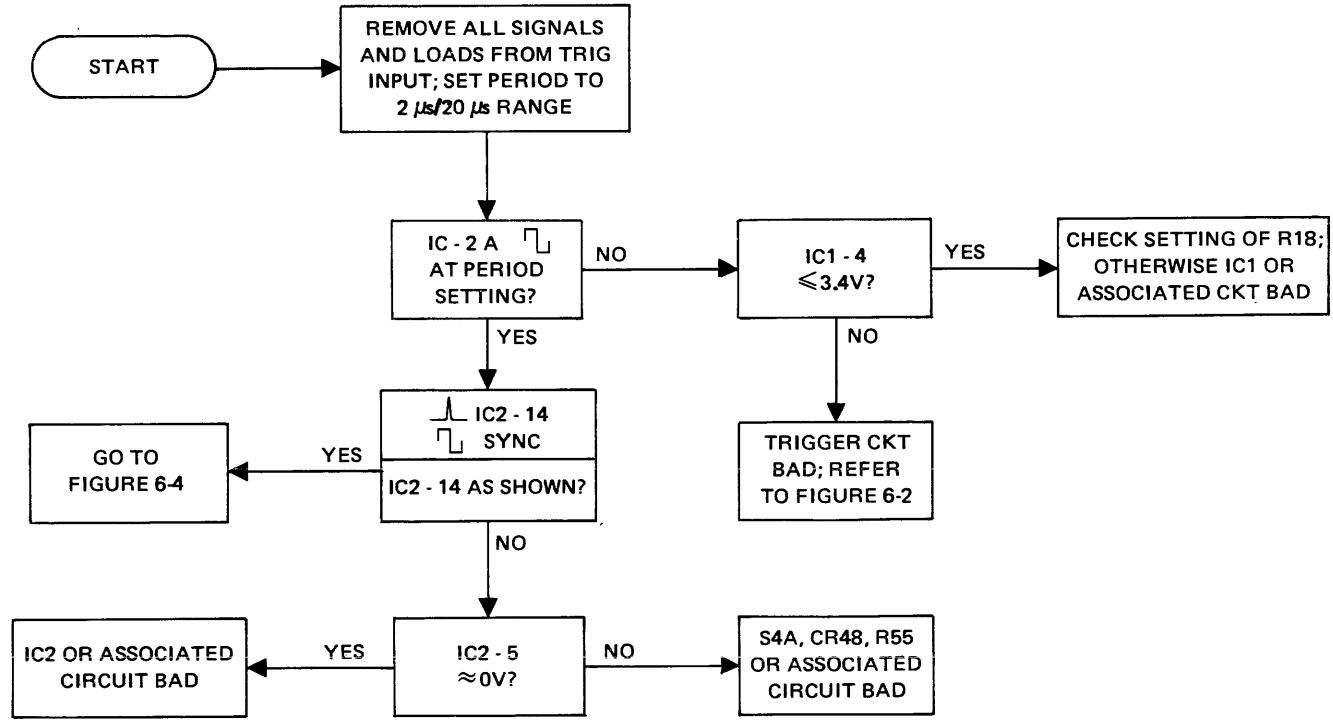


Figure 6-3. Oscillator Troubleshooting

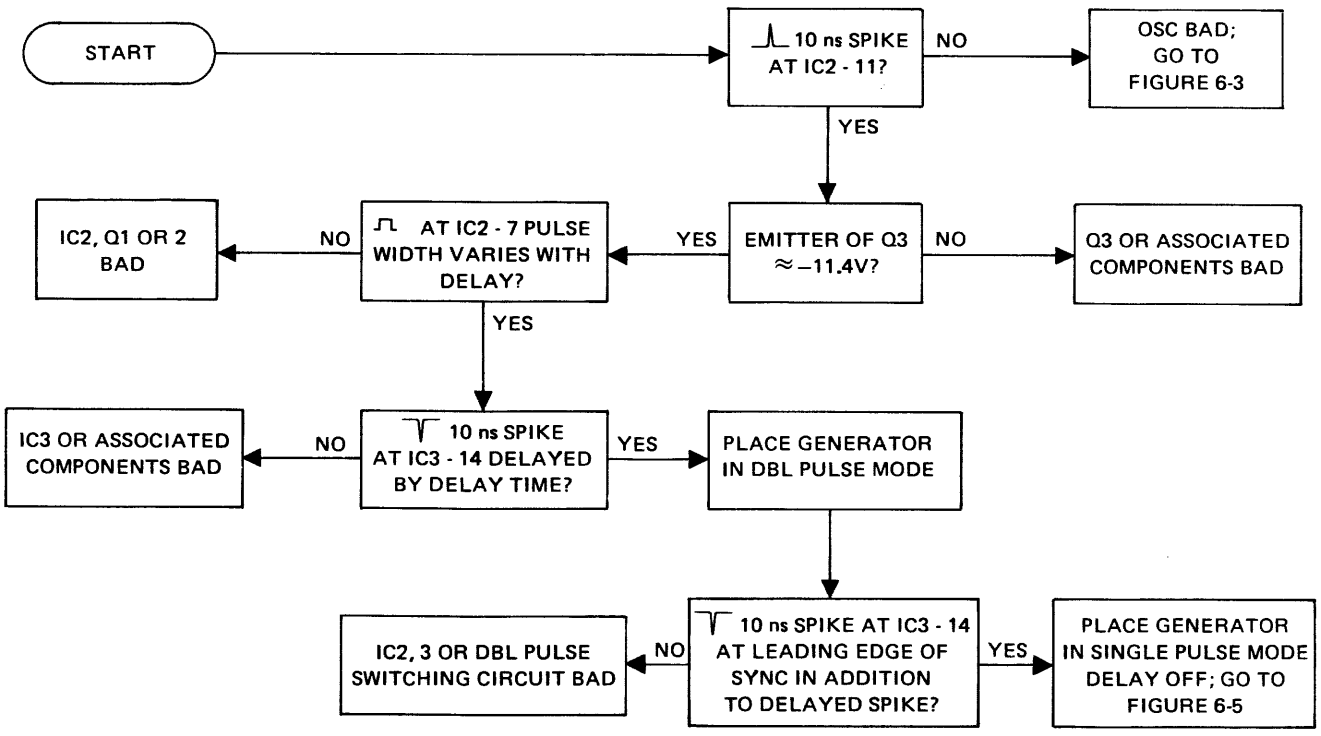


Figure 6-4. Delay Circuit Troubleshooting

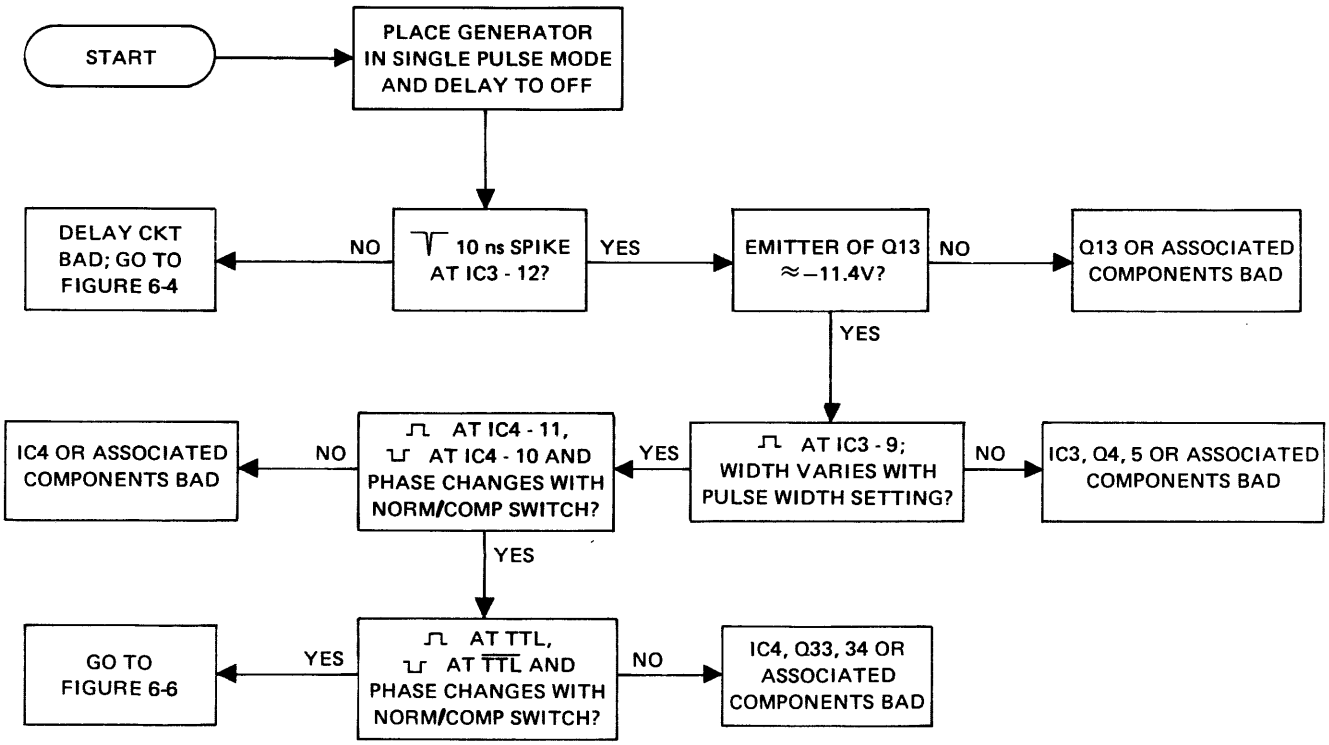


Figure 6-5. Width Circuit Troubleshooting

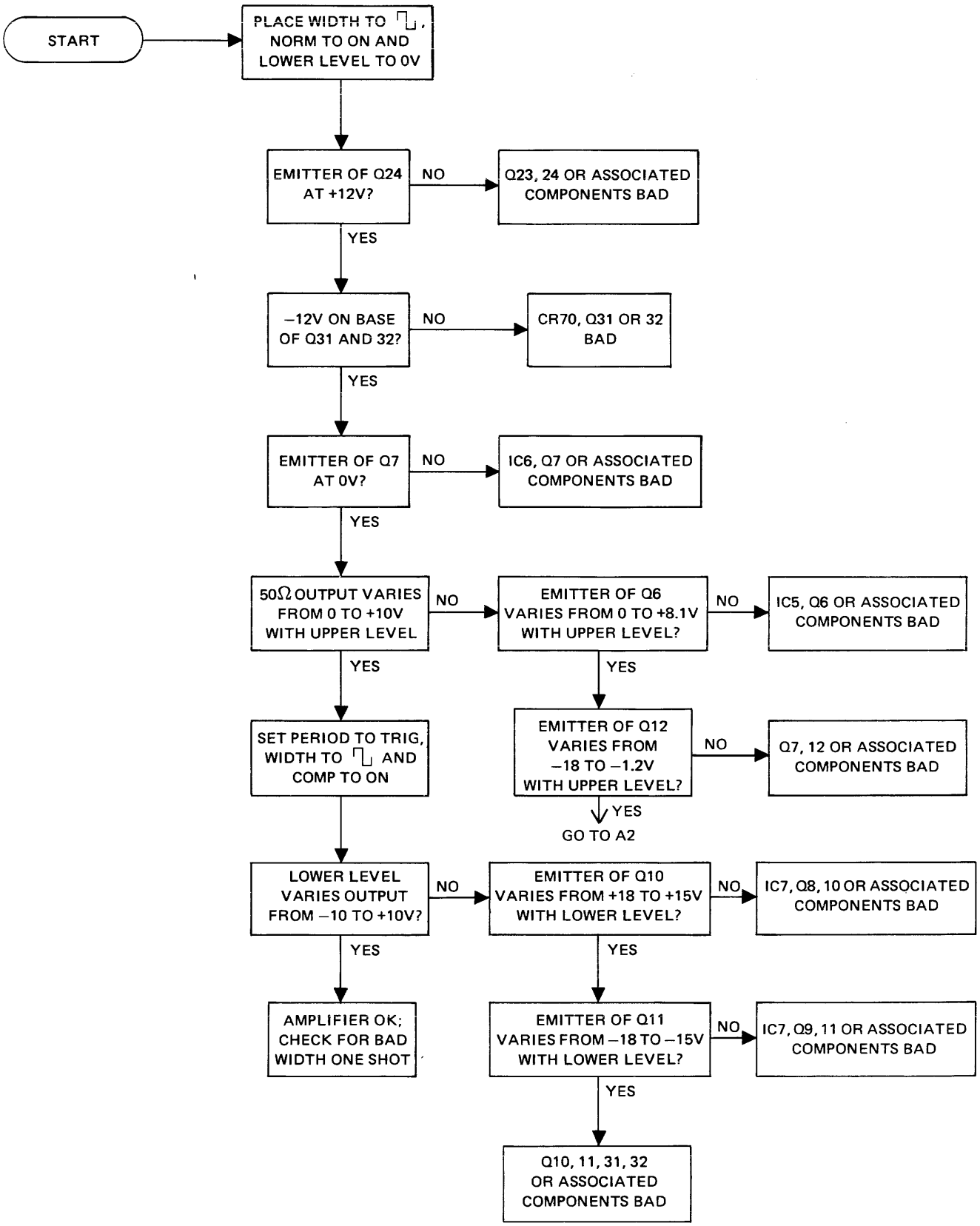


Figure 6-6. Output Amplifier Troubleshooting

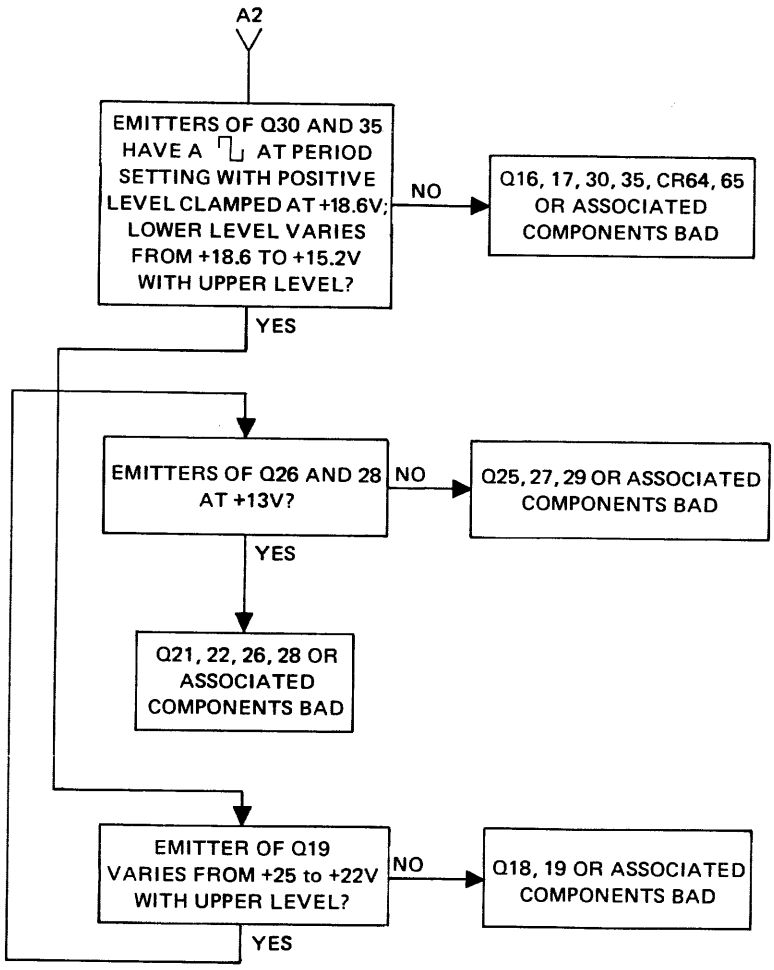


Figure 6-6. Output Amplifier Troubleshooting (Continued)

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, parts lists and schematics are in the arrangement shown below.

7.2 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and the function performed.

7.3 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the cover.

Drawing	Drawing No.	Drawing	Drawing No.
Instrument Schematic	0004-00-0119	Main Board Assembly	0101-00-0630
Chassis Assembly	0102-00-0631	Main Board Schematic	0103-00-0630
Chassis Parts List	1101-00-0631	Main Board Parts List	1100-00-0630

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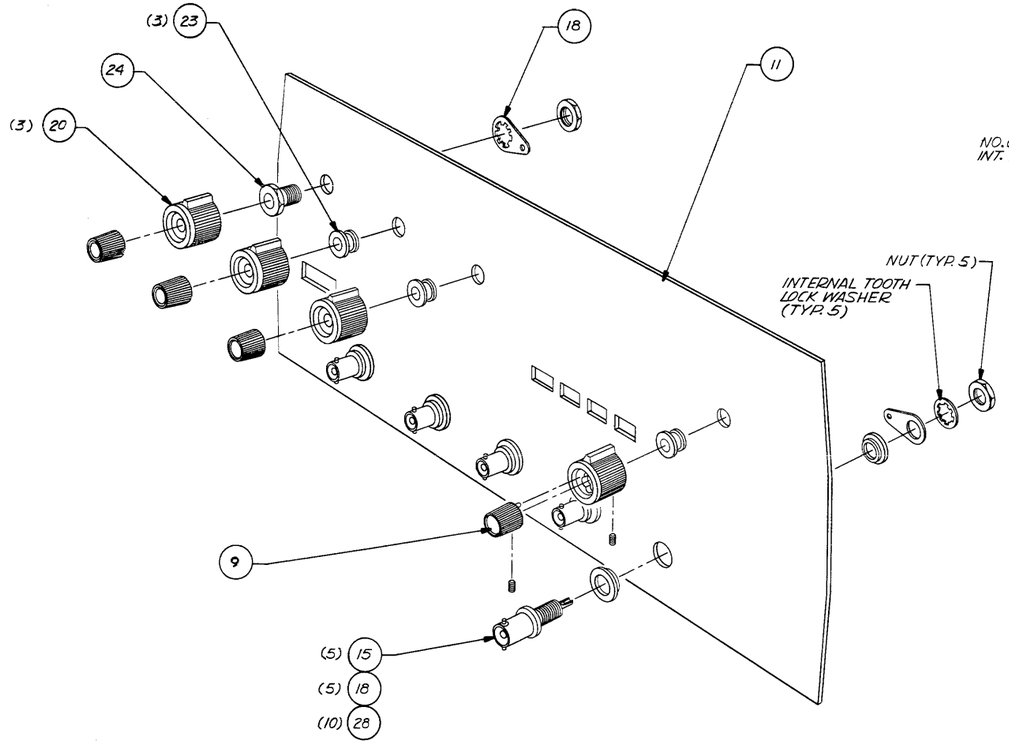
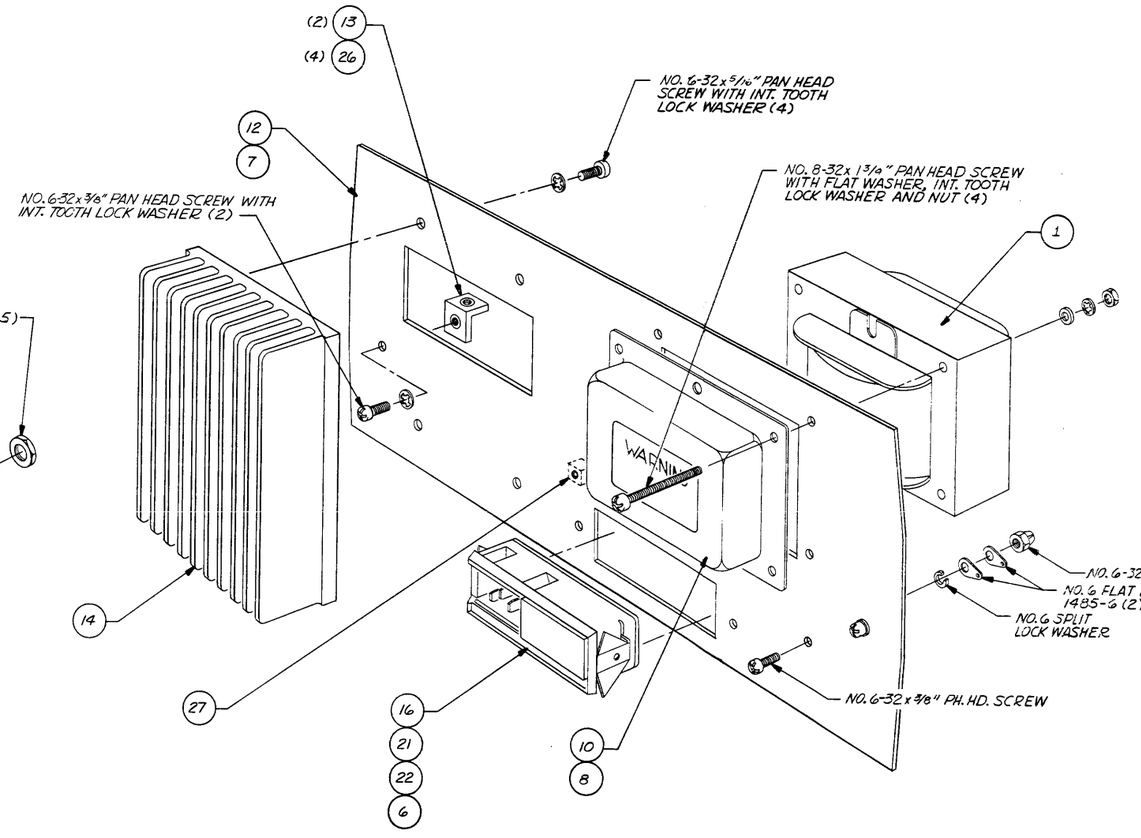
REV	ECN	BY	DATE	APP
A	ECN 1713	RO	4-20-79	





NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 9/1977	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RON CONERO	11/1/77	TITLE ASSEMBLY CHASSIS
FINISH WAVETEK PROCESS	RELEASE APPROV RON CONERO	11/22/77	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO. 802 / DWG NO. 0102-00-0631 / REV. A
	SCALE		CODE IDENT 23338 / SHEET 1 OF 2

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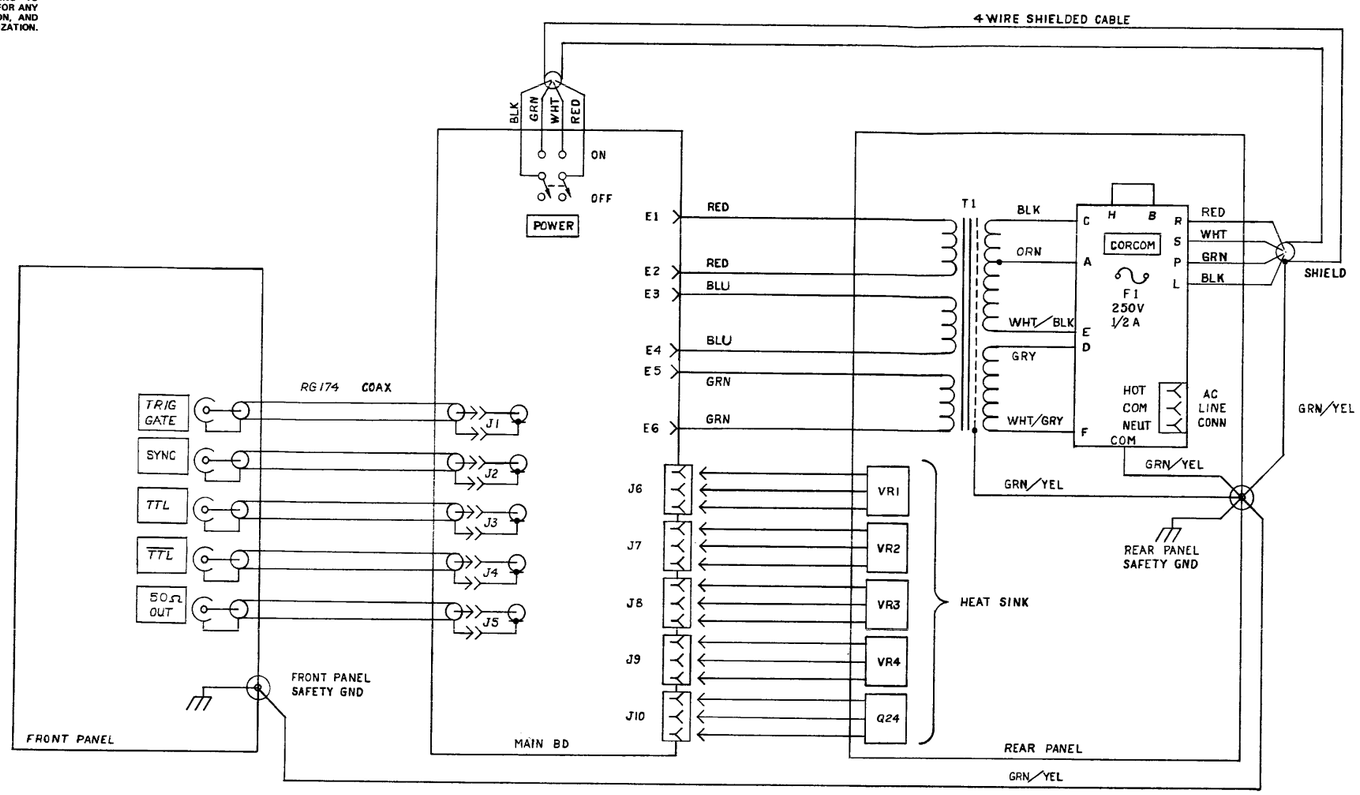
REV	ECN	BY	DATE	APP



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RON CONERO	11/11/77	TITLE: INSTRUMENT SCHEMATIC
	RELEASE APPROV RON CONERO	11/22/77	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 802 / DWG NO. 0004-00-0119 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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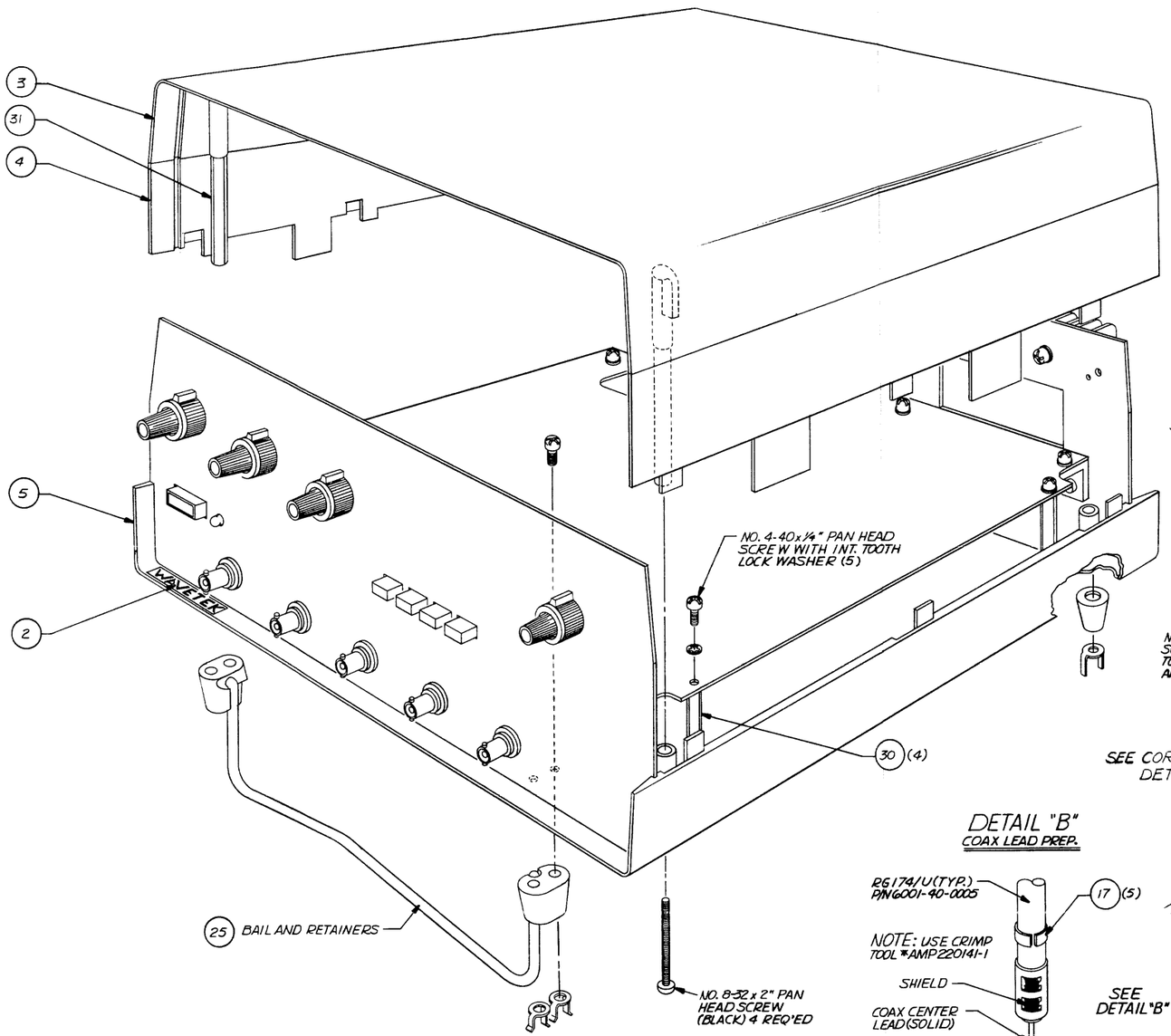
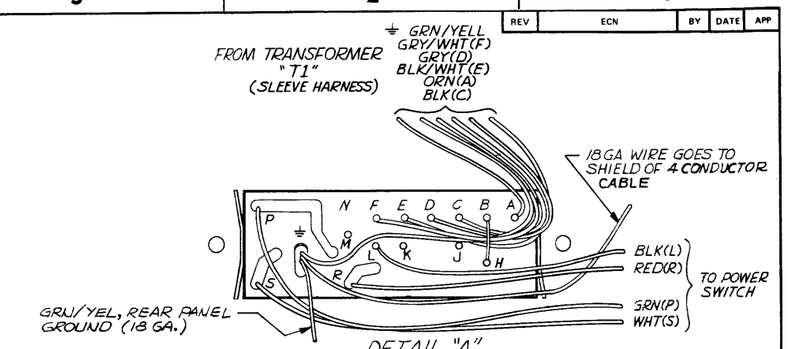
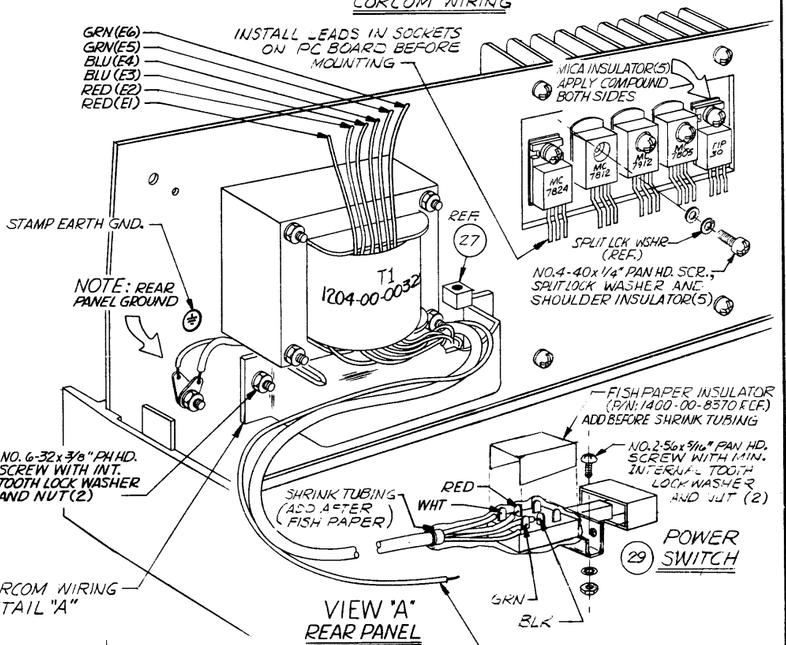
REV	ECN	BY	DATE	APP



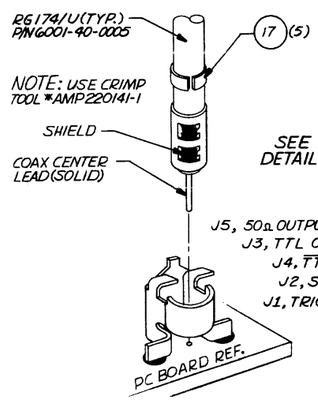


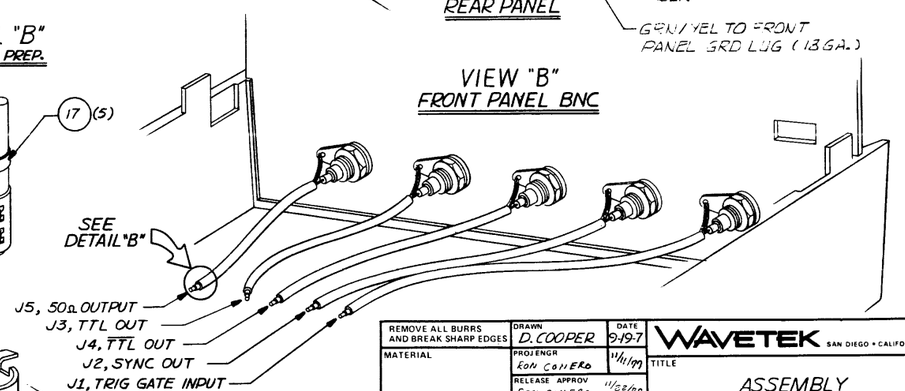
DETAIL "A"
CORCOM WIRING



VIEW "A"
REAR PANEL

DETAIL "B"
COAX LEAD PREP.





VIEW "B"
FRONT PANEL BNC

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 9-19-7	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RON CONERO	11/11/97	TITLE ASSEMBLY CHASSIS
	RELEASE APPROV RON CONERO	11/12/97	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 802	DWG NO. 0102-00-0631 REV A
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG CHASSIS	0102-00-0631	WVTK	0102-00-0631	1
1	TRANSFORMER	802-0632	WVTK	1204-00-0632	1
2	PLATE,NAME	139-305	WVTK	1400-00-2180	1
3	COVER,TOP	180-300-1	WVTK	1400-00-5000	1
4	EXPANDER	180-301	WVTK	1400-00-5010	2
5	COVER,BOTTOM	180-300-2	WVTK	1400-00-5030	1
6	SHIELD,PWR	1400-00-6210	WVTK	1400-00-6210	1
7	LABEL,I.D.	1400-00-6930	WVTK	1400-00-6930	1
8	LABEL,WARNING	1400-00-6940	WVTK	1400-00-6940	1
9	COAX KNOB SET (MOD) QTY:11:2400-01-0009	1400-00-6979	WVTK	1400-00-6979	1
10	END BELL	1400-00-6982	WVTK	1400-00-6982	1
11	PANEL,FRONT	1400-00-7840	WVTK	1400-00-7840	1
12	PANEL,REAR	1400-00-7853	WVTK	1400-00-7853	1
13	BRKT,SUPT	1400-00-7883	WVTK	1400-00-7883	2
14	HEAT SINK REF:3200-06-0002	1400-00-7899	WVTK	1400-00-7899	1
NONE	INSULATOR,PWR SWITCH REF:1600-99-0001	1400-00-8370	WVTK	1400-00-8370	1

WAVETEK PARTS LIST | TITLE CHASSIS | ASSEMBLY NO. 1101-00-0631 PAGE: 1 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	WIRE,COAX	BIX019-10050	BRKTC	6001-40-0005	6
NONE	CABLE,4 COND,20GA	8722	BELDN	6001-70-0007	2

WAVETEK PARTS LIST | TITLE CHASSIS | ASSEMBLY NO. 1101-00-0631 PAGE: 3 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
15	BNC CONN	KC-7946	KING	2100-01-0002	5
16	RECEPTACLE	6J1	CDMCM	2100-03-0026	1
17	CABLE CONTACT	22h2M6-2	AMP	2100-03-0040	5
18	SOLDER LUG	1447	SMITH	2100-04-0012	6
19	SOLDER LUG	1485-6	SMITH	2100-04-0025	2
20	COAX KNOB SET	KB-67-1-SB+0-M-9	HOGAN	2400-01-0009	3
21	LABEL,RECEPT	85-1501	CDMCM	2400-04-0002	1
22	FUSE,250V,1/2A,SB	313.500	LITFU	2400-05-0010	1
23	BUSHING NYLINER	4L2FF	THOMN	2800-01-0002	3
24	BEARING,PANEL	119	SMITH	2800-01-0004	1
31	STANDOFF	1475-M03-F05-832	UNICP	2800-02-0010	4
30	STANDOFF	1479-M03-F05-440	UNICP	2800-02-0023	4
25	RAIL ASSY W/FT	180-500	WVTK	2800-08-0010	1
26	INSERT # 6	74-11-106-13	SOTCO	2800-09-0017	4
27	FAST,CHASSIS	1591-C11	USECO	2800-09-0022	1
28	WASHER,SHOULDER	2668	SMITH	2800-27-0004	10
29	SWITCH ASSY PB	5102-00-0008	WVTK	5102-00-0008	1

WAVETEK PARTS LIST | TITLE CHASSIS | ASSEMBLY NO. 1101-00-0631 PAGE: 2 | REV E

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 802 / DWG NO. 1101-00-0631 / REV. E
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-2624

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REV	ECN	BY	DATE	APP
A	ECN 1713	RO	4-20-77	

LAST REF. DES. USED

R175
CR74
IC7
Q36
VR4
S7
C74
L10
J10

R26 & R86 NOT USED

RED E1 — CR1 IN4002 — +28V — VR1 7824 — J6 (3) — +25V .3A
CR2 IN4002, CR3 IN4002, CR4 IN4002
C1 500/50, C2 .47/50, R1 200 (+25V ADJ.), R4 4.99K, C7 .1/50, C10 50/50
VR4 7812 — J9 (3) — +18V .35A
R8 2.00K, C13 .1/50, R7 1K (+18V ADJ.), C14 .1, C15 50/50
RED E2
BLU E3 — CR5 IN4002, CR6 IN4002
C4 .1/50, C3 1000/35, R2 1K (-18V ADJ.), C8 .1, C11 50/50, R5 2.00K
CR7 IN4002, CR8 IN4002
BLU E4 — -21V — VR2 7912 — J7 (3) — -18V .3A

GRN F5 — CR9 IN4002 — +8V — VR3 7805 — J8 (3) — +5.2V .375A
CR10 IN4002, CR11 IN4002, CR12 IN4002
C5 1900/15, C6 .1, R3 100 (+5.2V ADJ.), R6 4.99K, C9 .1, C12 22/15, R9 392, CR13 TIL-220 PWR, C16 .1, C17 .1, C18 .1, C19 .1
GRN E6

R33 316, R37 316

PPDW
DW
CR47
CR74, C74 TRIM, E10, E11 -18V
CR36, C32 22/15V, R47 332, DELAY
CR37, CR38
CR39, C33 2.2/25V, +18V
CR40
CR41, C34 .2/100V
CR42
CR44, C35 .02/100V, OFF S2B, OFF S2A
CR45
CR34, C36 2000PF 50V SM

C21 47/20V, CR22, CR23
C22 +47/15V, CR24, CR25
C23 +47/50V, CR26, CR27
C24 .047/100V, CR28, CR29
C25 .0047/100V, CR30, CR31
C26 330PF 500V SM, CR32, CR33
E7, E8, R29 1.21K, -18V, PERIOD S1B
MAN TRIG

+5.2V — CR14 — S3 MAN TRIG
R10 1.96K, +18V
R14 1K, R15 1K, K13 1K, R17 499, R18 100K, R19 63.4K SYM, R20 49.9K
Q36 SD215
CR15, +5.2V, CR16, C20 33PF, R12 392
C27 50 MHz ADJ, 7-35PF 250V
CR35 FD777, OSC
IC1, IC2, SQR
R28 316, R48 38.3K, R25 10K CW PERIOD, R24 392, C28 47PF, R27 392
R31 100, R32 499, C29 15PF, R30 499, +5.2V
R34 78.7, C30 15PF, R35 10, R36 316
- 18V, K11 3.16K, TRIG GATE, J1
R16 499, R21 100, CR20, R23 200, R22 316
CR17, CR18, CR19, CR21
PERIOD, E9, S1A, MAN TRIG

C31 22PF, +5.2V, CR43 FD777, R38 51.1, Q1 2N3646
R39 100, R40 33.2, R44 10, CR46, SQR, Q2 2N3640
R42 33.2, Q3 2N3646, R41 4.99K, R43 3.32K, R45 499, R46 10K CW, DELAY, -18V

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D COOPER	DATE 9/2/77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RON CONERO	11/1 100	TITLE: SCHEMATIC MAIN BOARD
	RELEASE APPROV RON CONERO	11/22/77	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 802	DWG NO 0103-00-0630 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 2

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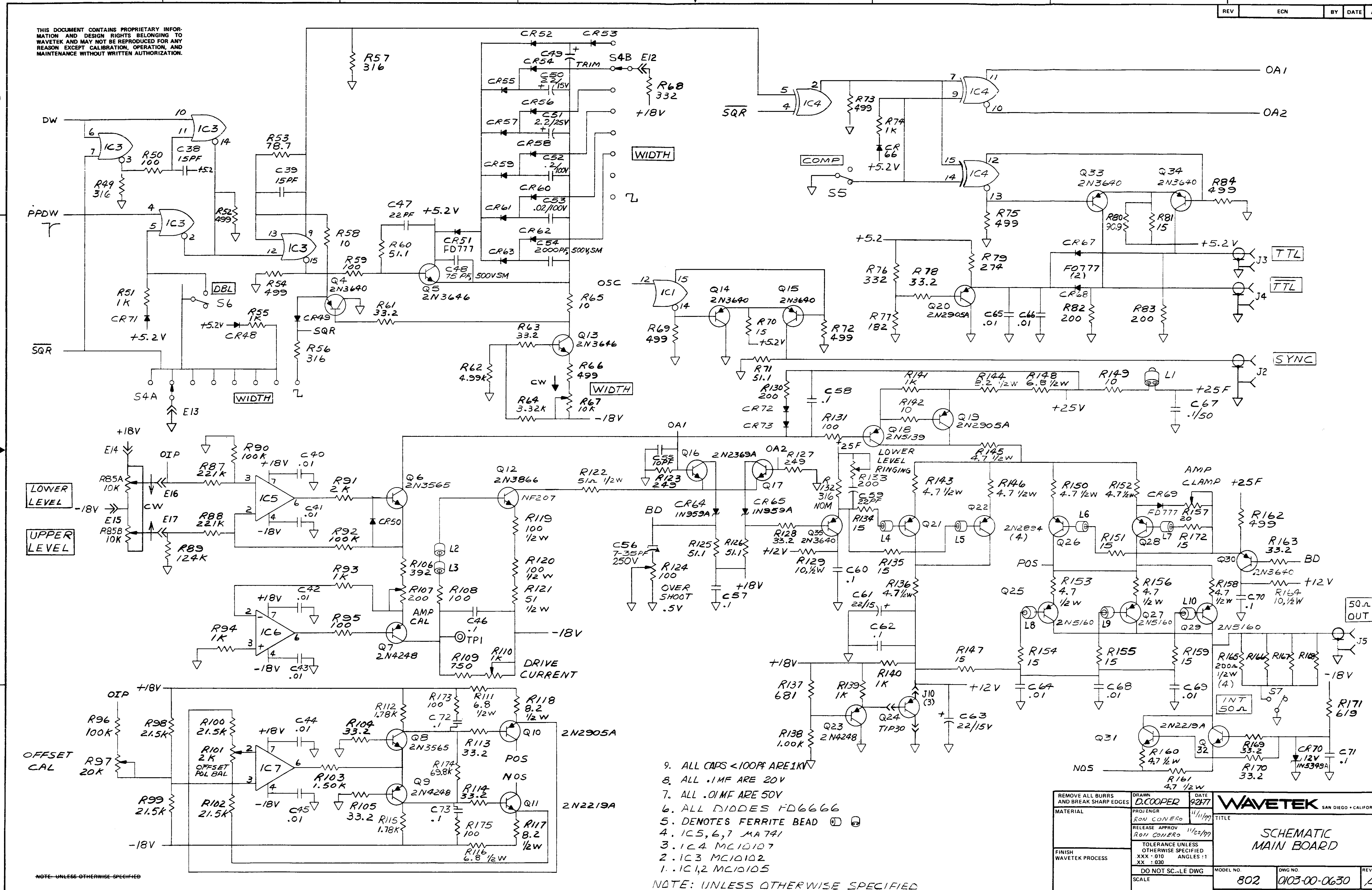


9. ALL CAPS <100PF ARE 1KV
8. ALL .1MF ARE 20V
7. ALL .01MF ARE 50V
6. ALL DIODES FD6666
5. DENOTES FERRITE BEAD
4. IC5,6,7 MA741
3. IC4 MC10107
2. IC3 MC10102
1. IC1,2 MC10105

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D.COOPER DATE 9/21/77
MATERIAL	PROJ ENGR RON CONERO 11/11/77
	RELEASE APPROV RON CONERO 11/22/77
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
	DO NOT SCALE DWG
	SCALE

WAVETEK SAN DIEGO • CALIFORNIA

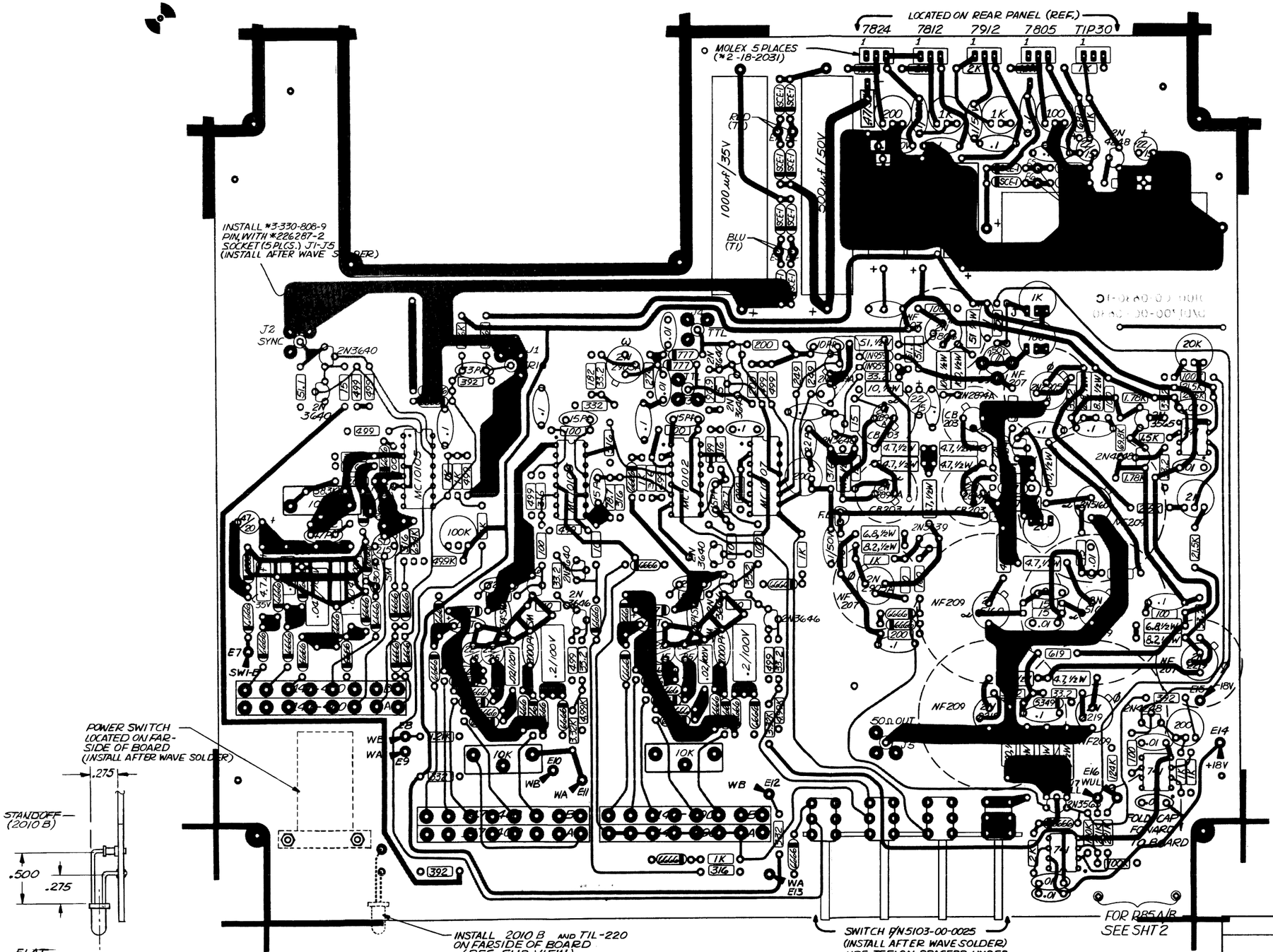
TITLE: SCHEMATIC MAIN BOARD

MODEL NO. 802 — DWG NO. 0103-00-0630 — REV A

CODE IDENT 23338 — SHEET 2 OF 2

~~NOTE: UNLESS OTHERWISE SPECIFIED~~

B	ECN 1713	R0	4-20-78



NOTE:

- ⊓ = INSTALL 2 EA. FERRITE BEAD ON BASE
- ∽ = INSTALL FERRITE BEAD ON BASE

} DO NOT INSTALL TRANSIPADS ON THESE DEVICES

- ω INSTALL SHORT TRANSIPAD (10123N)
- ϕ INSTALL TALL TRANSIPAD (10160)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL .1 CAPS ARE 20V
2. ALL .01 CAPS ARE 50V
3. ALL CERAMIC DISC. CAPS ARE 1KV

D. COOPER	9-22-7	WAVETEK
RON CONERO	11/11/77	ASSEMBLY MAIN BOARD
RON CONERO	11/22/77	802 | 0101-00-0630 | B
		SHEET 1 OF 2

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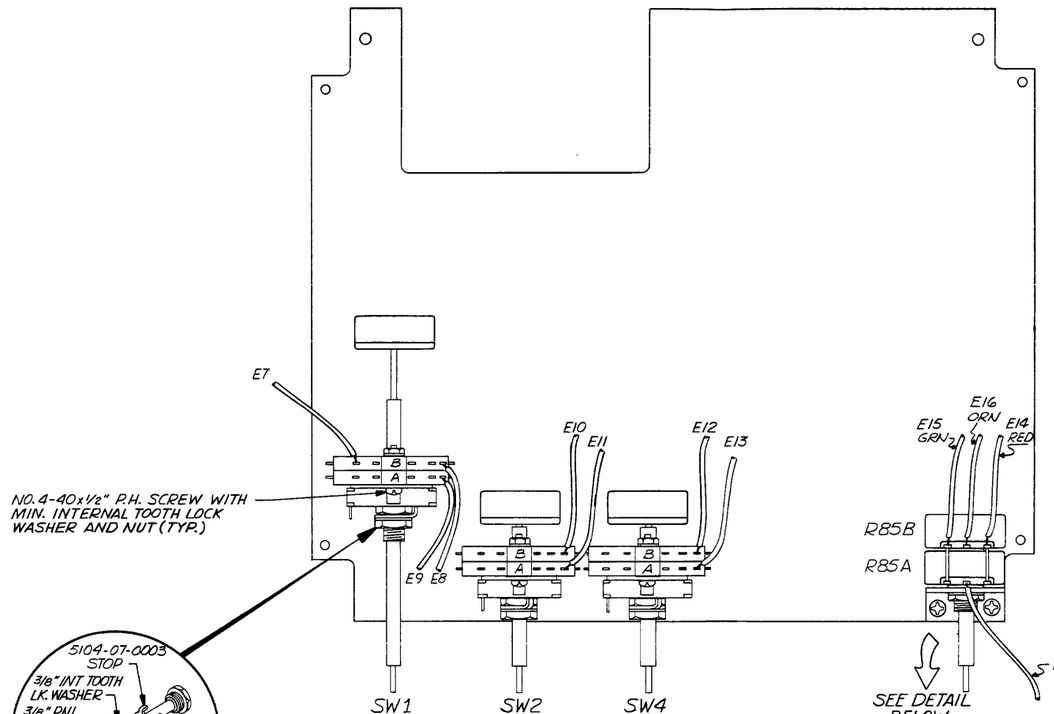
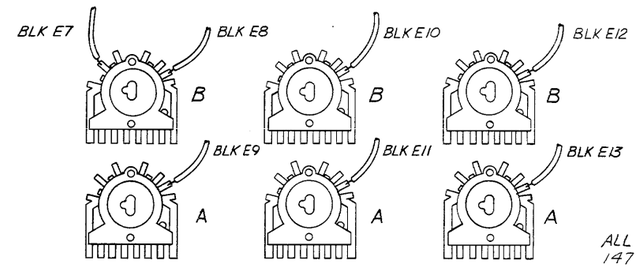
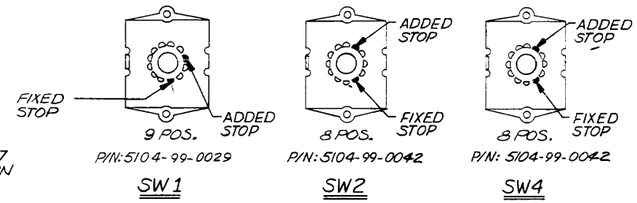
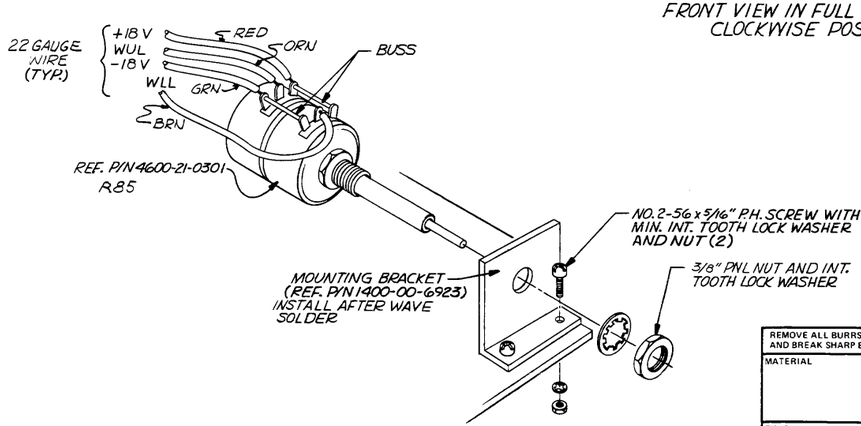
REV	ECN	BY	DATE	APP







DETENTS SHOWN FROM FRONT VIEW IN FULL COUNTER CLOCKWISE POSITION



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 9-21-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RON CONERO	11/11/77	TITLE: ASSEMBLY MAIN BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV RON CONERO	11/22/77	
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 802 / DWG NO. 0101-00-0630 / REV B
	SCALE		CODE IDENT. 23338 / SHEET 2 OF 2

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG MAINBOARD	0101-00-0630	WVTK	0101-00-0630	1
NONE	SCHEMATIC MAINBOARD	0103-00-0630	WVTK	0103-00-0630	1
NONE	BRACKET	1400-00-6923	WVTK	1400-00-6923	1
C55	CAP,CER,10PF,1KV	DD-100	CRL	1500-01-0011	1
C40 C41 C42 C43 C44 C45 C64 C65 C66 C68 C69	CAP,CER,.01MF,50V	CK-103	CRL	1500-01-0310	11
C13 C4 C67 C7	CAP,CER,.1MF,50V	CK-104	CRL	1500-01-0410	4
C14 C16 C17 C18 C19 C46 C57 C58 C6 C60 C62 C70 C71 C72 C73 C8 C9	CAP,CER,.1MF,20V	UK20-104	ARCO	1500-01-0413	17
C29 C30 C38 C39	CAP,CER,15PF,1KV	DD-150	CRL	1500-01-5011	4
C31 C47 C59	CAP,CER,22PF,1KV	DD-220	CRL	1500-02-2011	3
C20	CAP,CER,33PF,1KV	DD-330	CRL	1500-03-3011	1
C28	CAP,CER,47PF,1KV	DD-470	CRL	1500-04-7011	1
C36 C54	CAP,MICA,2000PF,500V	DM19-202J	ARCO	1500-12-0200	2
C26	CAP,MICA,330PF,500V	DM15-331J	ARCO	1500-13-3100	1
C37 C48	CAP,MICA,75PF,500V	DM15-750J	ARCO	1500-17-5000	2
C3	CAP,ELECT,1000MF,35V	39D108G035GL6	SPRAG	1500-31-0212	1

WAVETEK PARTS LIST | TITLE: PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 1 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	TERM	2010R1	USECO	2100-05-0011	1
NONE	HEAT SINK	NF-207	WAKE	2800-11-0001	4
NONE	TRANSIPAD	10123A	METRS	2800-11-0003	1
NONE	TRANSIPAD	10160	METRS	2800-11-0004	4
NONE	HEATSINK	NF-209	WAKE	2800-11-0008	5
NONE	HEATSINK	203 CB	WAKE	2800-11-0009	4
NONE	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	9
NONE	BALUN CORE	287300D902	FARIT	3100-00-0002	1
R124 R3	POT,TRIM,100	91AR100	BECK	4600-01-0103	2
R110 R2 R7	POT,TRIM,1K	91AR1K	BECK	4600-01-0209	3
R18	POT,TRIM,100K	91AR100K	BECK	4600-01-0402	1
R157	POT,TRIM,20	91AR20	BECK	4600-02-0000	1
R1 R107 R133	POT,TRIM,200	91AR200	BECK	4600-02-0101	3
R101	POT,TRIM,2K	91AR2K	BECK	4600-02-0201	1
R97	POT,TRIM,20K	91AR20K	BECK	4600-02-0301	1
R85	POT,DUAL,10K	4P-1997	CTS	4600-21-0301	1
R25	POT,CONT,10K	4609-71-0309	WVTK	4609-71-0309	1

WAVETEK PARTS LIST | TITLE: PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 3 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R103	RES,MF,1/8W,1%,1.5K	RN55D-1501F	TRW	4701-03-1501	1
R134 R135 R147 R151 R154 R155 R159 R172 R70 R81	RES,MF,1/8W,1%,15	RN55D-15R0F	TRW	4701-03-1509	10
R112 R115	RES,MF,1/8W,1%,1.78K	RN55D-1781F	TRW	4701-03-1781	2
R77	RES,MF,1/8W,1%,182	RN55D-1820F	TRW	4701-03-1820	1
R10	RES,MF,1/8W,1%,1.96K	RN55D-1961F	TRW	4701-03-1961	1
R130 R23 R42 R83	RES,MF,1/8W,1%,200	RN55D-2000F	TRW	4701-03-2000	4
R5 R8 R91	RES,MF,1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	3
R100 R102 R98 R99	RES,MF,1/8W,1%,21.5K	RN55D-2152F	TRW	4701-03-2152	4
R87 R88	RES,MF,1/8W,1%,221K	RN55D-2213F	TRW	4701-03-2213	2
R123 R127	RES,MF,1/8W,1%,249	RN55D-2490F	TRW	4701-03-2490	2
R79	RES,MF,1/8W,1%,274	RN55D-2740F	TRW	4701-03-2740	1
R132T R22 R28 R33 R36 R37 R49 R56 R57	RES,MF,1/8W,1%,316	RN55D-3160F	TRW	4701-03-3160	9
R11	RES,MF,1/8W,1%,3.16K	RN55D-3161F	TRW	4701-03-3161	1
R47 R68 R76	RES,MF,1/8W,1%,332	RN55D-3320F	TRW	4701-03-3320	3
R43 R64	RES,MF,1/8W,1%,3.32K	RN55D-3321F	TRW	4701-03-3321	2
R104 R105 R113 R114	RES,MF,1/8W,1%,33.2	RN55D-33R2F	TRW	4701-03-3329	13

WAVETEK PARTS LIST | TITLE: PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 5 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C5	CAP,ELECT,1900MF,15V	39D198G015GL4	SPRAG	1500-31-9201	1
C10 C11 C15	CAP,ELECT,50MF,50V	500D506G050DD7	SPRAG	1500-35-0003	3
C1	CAP,ELECT,500MF,50V	39D507G050GL4	SPRAG	1500-35-0103	1
C35 C53	CAP,MYLR,.02MF,100V	BA1B203F	IMH	1500-42-0304	2
C34 C52	CAP,MYLR,.2MF,100V	BA1B204F	IMH	1500-42-0404	2
C25	CAP,MYLR,.0047MF100V	WMF-1D47	CDF	1500-44-7214	1
C24	CAP,MYLR,.047MF,100V	WMF-1S47	CDF	1500-44-7304	1
C27 C56	VARI,7-35PF,250V	7S-TRIM0-02 7/35 PF	TRIKO	1500-53-5000	2
C33 C51	CAP,TANT,2.2MF,25V	196D225X9025HA1	SPRAG	1500-72-2502	2
C12 C32 C50 C61 C63	CAP,TANT,22MF,15V	196D226X9015KA1	SPRAG	1500-72-2601	5
C2 C23	CAP,TANT,.47MF,50V	150D474X9050B2	SPRAG	1500-74-7403	2
C22	CAP,TANT,4.7MF,35V	150D475X903582	SPRAG	1500-74-7502	1
C21	CAP,TANT,47MF,20V	196D476X9020PE4	SPRAG	1500-74-7601	1
NONE	MAINBOARD	1700-00-0630	WVTK	1700-00-0630	1
NONE	SPRING SOCKET	3-330-808-9	AMP	2100-03-0037	5
NONE	COAX SOCKET	2262A7-2	AMP	2100-03-0038	5
NONE	SOCKET	10-18-2031	MOLEX	2100-03-0047	5

WAVETEK PARTS LIST | TITLE: PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 2 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R46 R67	FROM:4600-01-0312 POT,CONT,10K FROM:4600-01-0312	4609-71-0310	WVTK	4609-71-0310	2
R129 R164	RES,C,1/2W,5%,10	RC20GF-100	STKPL	4700-25-0100	2
R136 R143 R145 R146 R150 R152 R153 R156 R158 R160 R161	RES,C,1/2W,5%,4.7	RC20GF-4R7	STKPL	4700-25-0479	11
R121 R122	RES,C,1/2W,5%,51	RC20GF510J	STKPL	4700-25-0510	2
R111 R116 R148	RES,C,1/2W,5%,6.8	RC20GF-6R8	STKPL	4700-25-06A9	3
R117 R118 R144	RES,C,1/2W,5%,8.2	RC20GF-8R2	STKPL	4700-25-0829	3
R119 R120	RES,C,1/2W,5%,100	RC20GF101J	STKPL	4700-25-1000	2
R108 R131 R173 R175 R21 R31 R39 R50 R59 R95	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	10
R13 R138 R139 R14 R140 R141 R15 R51 R55 R74 R93 R94	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	12
R90 R92 R96	RES,MF,1/8W,1%,100K	RN55D-1003F	TRW	4701-03-1003	3
R142 R149 R35 R40 R58 R65	RES,MF,1/8W,1%,10	RN55D-10R0F	TRW	4701-03-1009	6
R29	RES,MF,1/8W,1%,1.21K	RN55D-1211F	TRW	4701-03-1211	1
R89	RES,MF,1/8W,1%,124K	RN55D-1243F	TRW	4701-03-1243	1

WAVETEK PARTS LIST | TITLE: PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 4 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R128 R163 R169 R170 R40 R42 R61 R63 R78					
R48	RES,MF,1/8W,1%,3K.3K	RN55D-3832F	TRW	4701-03-3832	1
R106 R12 R24 R27 R9	RES,MF,1/8W,1%,392	RN55D-3920F	TRW	4701-03-3920	5
R16 R162 R17 R30 R32 R45 R52 R54 R66 R69 R72 R73 R75 R84	RES,MF,1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	14
R4 R41 R6 R62	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	4
R20	RES,MF,1/8W,1%,49.9K	RN55D-4992F	TRW	4701-03-4992	1
R125 R126 R38 R60 R71	RES,MF,1/8W,1%,51.1	RN55D-51R1F	TRW	4701-03-5119	5
R171	RES,MF,1/8W,1%,619	RN55D-6190F	TRW	4701-03-6190	1
R19	RES,MF,1/8W,1%,63.4K	RN55D-6342F	TRW	4701-03-6342	1
R137	RES,MF,1/8W,1%,6B1	RN55D-6810F	TRW	4701-03-6810	1
R174	RES,MF,1/8W,1%,69.8K	RN55D-6982F	TRW	4701-03-6982	1
R109	RES,MF,1/8W,1%,750	RN55D-7500F	TRW	4701-03-7500	1
R34 R53	RES,MF,1/8W,1%,78.7	RN55D-78R7F	TRW	4701-03-7879	2
R80	RES,MF,1/8W,1%,90.9	RN55D-90R9F	TRW	4701-03-9099	1
R165 R166 R167 R168	RES,MF,1/2W,1%,200	RN65D2000F	TRW	4701-23-2000	4
CR64 CR65	DIODE	1N959	MOT	4801-01-0959	2

WAVETEK PARTS LIST | TITLE: PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 6 | REV E

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: MAIN
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		MODEL NO. 802 / DWG NO. 1100-00-0630 / REV E
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 2
	SCALE		

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3804

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR70	DIODE	1N5349A	MOT	4801-01-5349	1
CR1 CR10 CR11 CR12 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9	DIODE	SCE-1	SEMTC	4801-02-0001	12
CR35 CR43 CR51 CR67 CR68 CR69	DIODE	FD-777	FAIR	4807-02-0777	6
CR14 CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR30 CR31 CR32 CR33 CR34 CR36 CR37 CR38 CR39 CR40 CR41 CR42 CR44 CR45 CR46 CR47 CR48 CR49 CR50 CR52 CR53 CR54 CR55 CR56 CR57 CR58 CR59 CR60 CR61 CR62 CR63 CR66 CR71 CR72 CR73 CR74	DIODE	FD-6666	FAIR	4807-02-6666	52
CR13	LED	TIL-220	TI	4899-00-0006	1
Q11 Q31 Q32	TRANS	2N2219A	FAIR	4901-02-2191	3
Q16 Q17	TRANS	2N2369A	FAIR	4901-02-3691	2
Q21 Q22 Q26 Q28	TRANS	2N2894A	NSC	4901-02-8941	4
Q10 Q19 Q20	TRANS	2N2905A	FAIR	4901-02-9051	3
Q6 Q8	TRANS	2N3565	FAIR	4901-03-5650	2

WAVETEK PARTS LIST | TITLE PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 7 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
VR1	IC	7824	FAIR	7000-78-2400	1
VR2	IC	7912	MOT	7000-79-1200	1
VR3	VOLTAGE REGULATOR	7805393	FAIR	8000-78-0500	1
IC3	IC	MC10102	MOT	8001-01-0200	1
IC1 IC2	IC	MC10105	MOT	8001-01-0500	2
IC4	IC	MC10107	MOT	8001-01-0700	1

WAVETEK PARTS LIST | TITLE PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 9 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q14 Q15 Q2 Q30 Q33 Q34 Q35 Q4	TRANS	2N3640	FAIR	4901-03-6400	8
Q1 Q13 Q3 Q5	TRANS	2N3646	FAIR	4901-03-6460	4
Q12	TRANS	2N3866	MOT	4901-03-8660	1
Q23 Q7 Q9	TRANS	2N4248	FAIR	4901-04-2480	3
Q18	TRANS	2N5139	FAIR	4901-05-1390	1
Q25 Q27 Q29	TRANS	2N5160	MOT	4901-05-1600	3
Q24	TRANS	TIP-30	TI	4902-00-0300	1
Q36	TRANS	SD215DF	SIG	4902-00-2140	1
NONE	SWITCH ASSY	5103-00-0025	WVTK	5103-00-0025	1
NONE	BUTTON	J-52305-BLACK	CHL	5103-04-0003	4
NONE	WAFER	147-400	WVTK	5104-02-0015	6
NONE	SWITCH STOP	215-33-001-01-22	CTS	5104-07-0003	3
SW1	DETENT MOD FROM:5104-01-0010	5104-99-0029	WVTK	5104-99-0029	1
SW2 SW4	DETENT,MOD FROM:5104-01-0003	5104-99-0042	WVTK	5104-99-0042	2
IC5 IC6 IC7	IC	MA-741	FAIR	7000-07-4100	3
VR4	IC	MC7812CP	MOT	7000-78-1200	1

WAVETEK PARTS LIST | TITLE PCA MAINBOARD | ASSEMBLY NO. 1100-00-0630 | PAGE: 8 | REV E

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE MAIN
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 802	DWG NO. 1100-00-0630 REV E
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

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