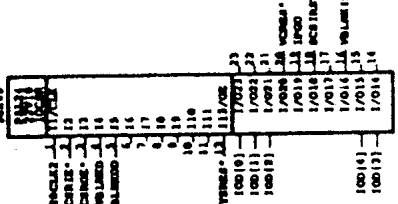
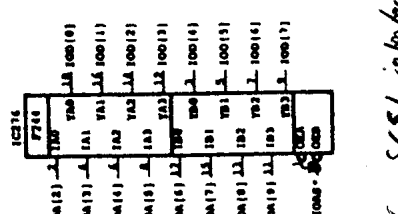


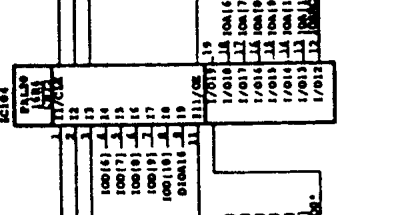
WRITE ENABLE/PAUSE BUS



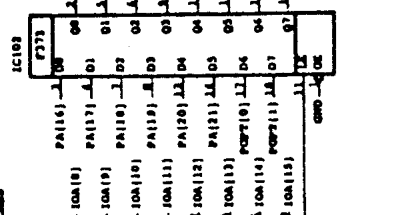
ADDRESS OF DATA BUS BUFFER



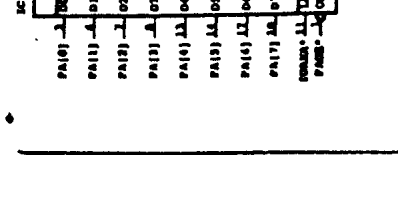
DATA BUS ADDRESS COMBINER



DATA BUS ADDRESS COMBINER

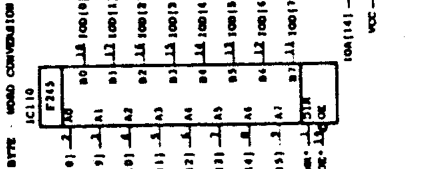


DATA BUS ADDRESS COMBINER

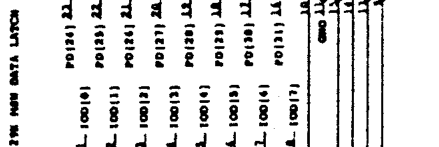


Buffer for SCSI in memory

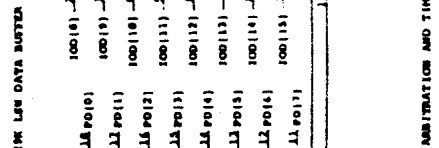
BYTE WORD CONVERSION



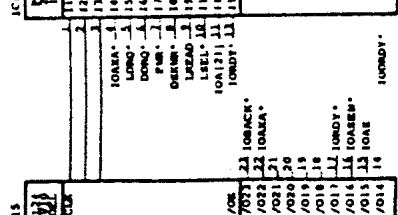
DATA BUS DATA LATCH



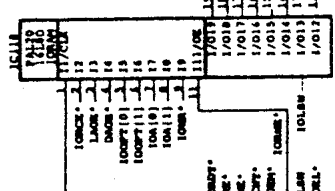
DATA BUS DATA BUFFER



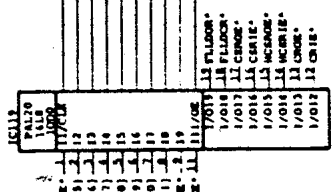
I/O INITIALIZATION AND TIMING



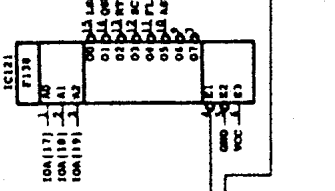
I/O ENABLES



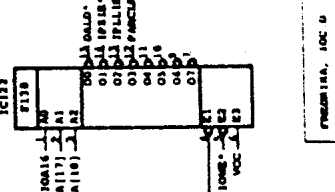
REGISTER ADDRESS SIGNALS



CHIP SELECT DECODER



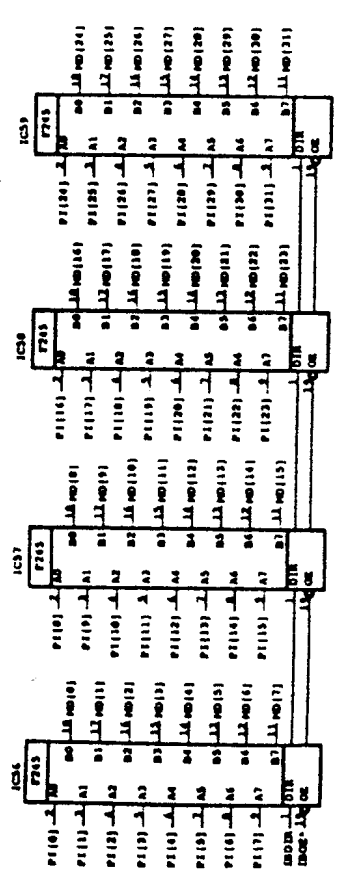
WRITE ENABLE DECODER



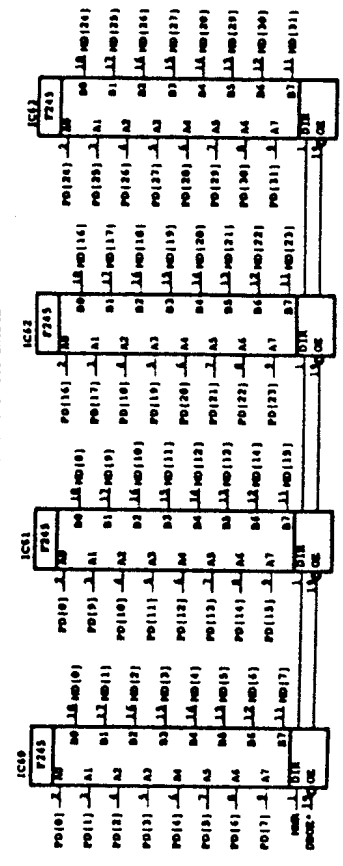
IC133

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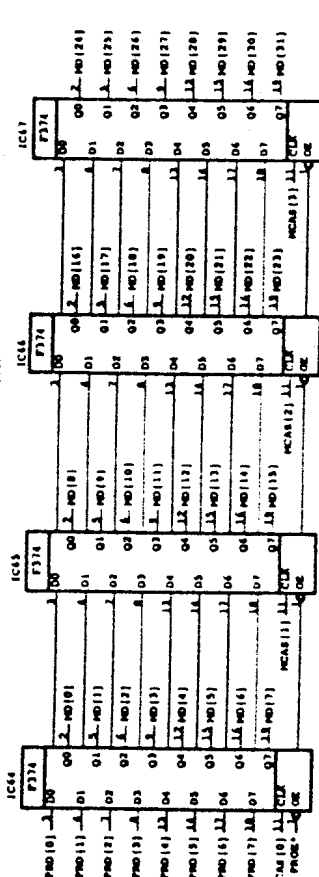
MEMORY - INSTRUCTION BUS INTERFACE



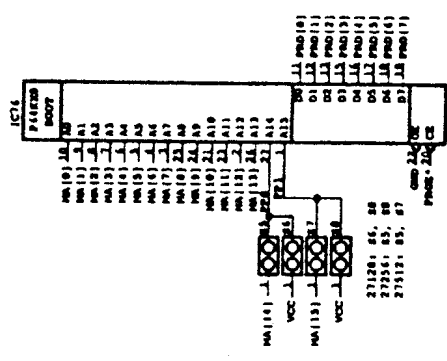
MEMORY - PROCESSOR DATA BUS INTERFACE



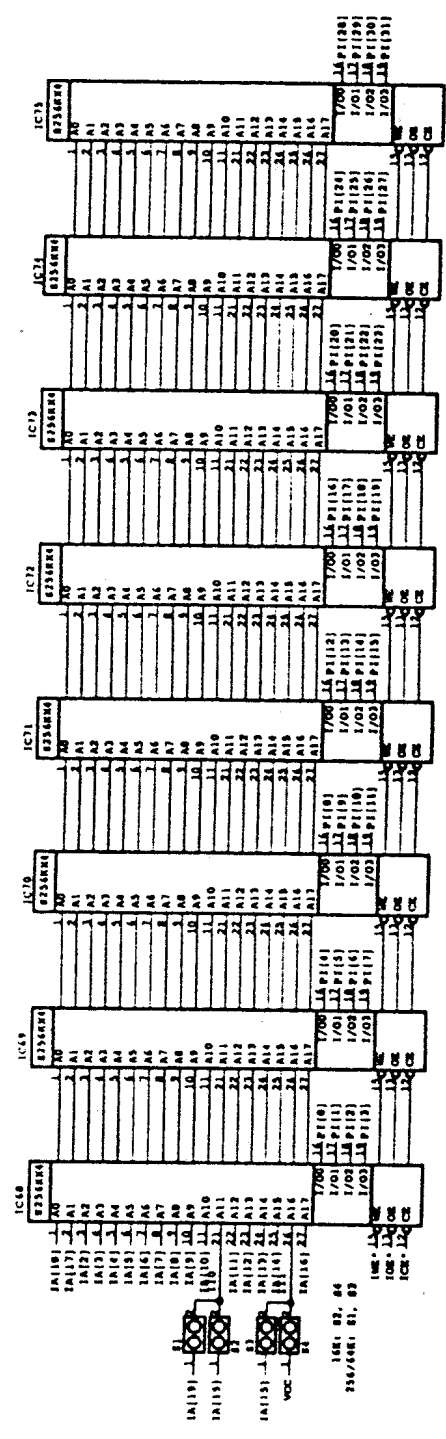
FROM BYTE TO WORD CONVERSION



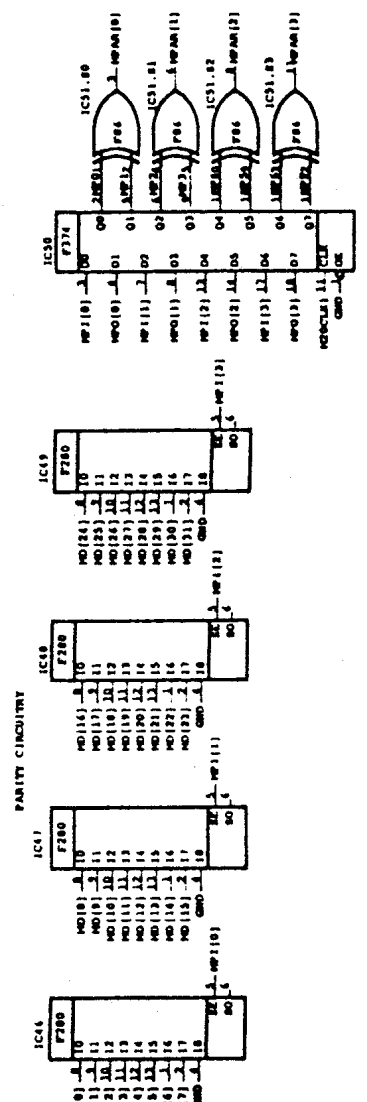
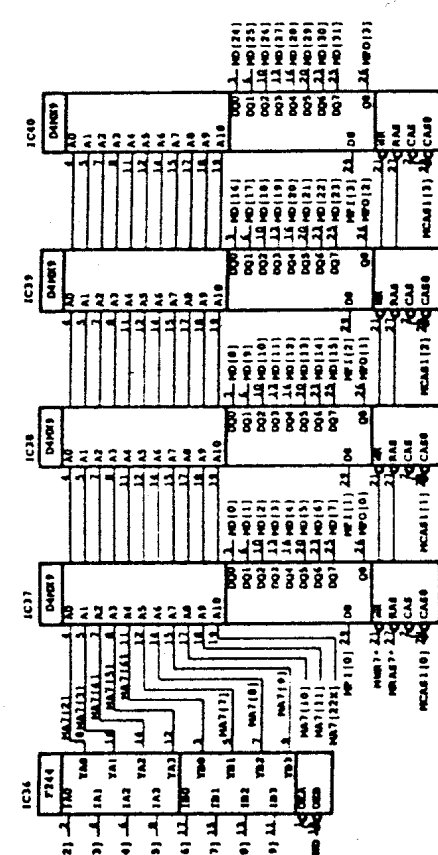
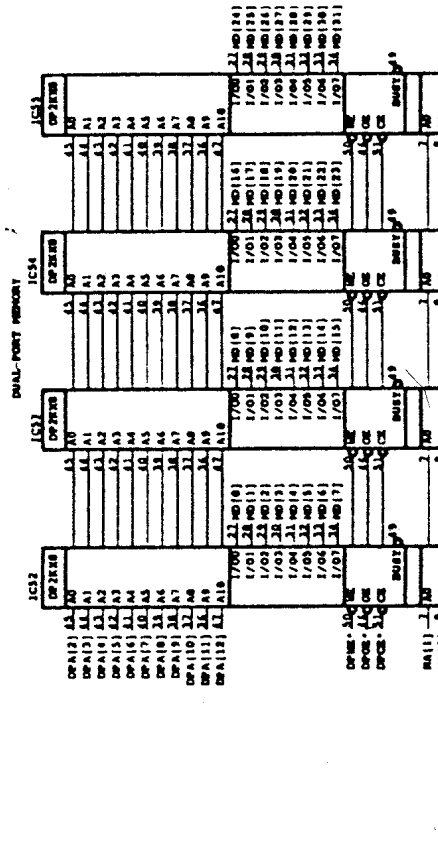
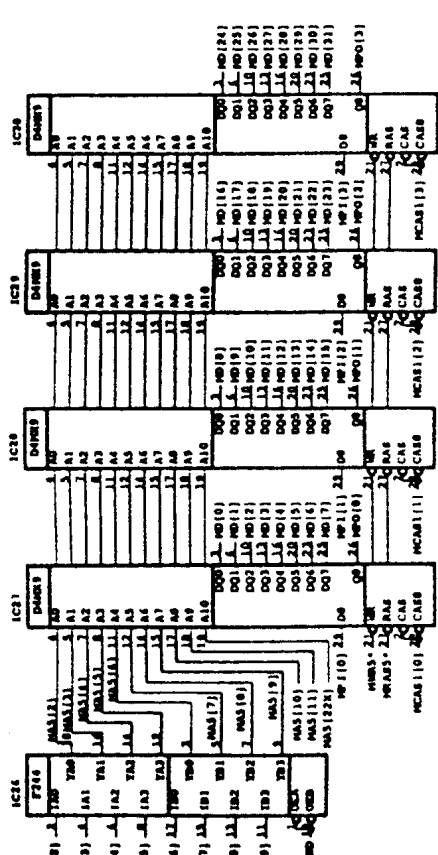
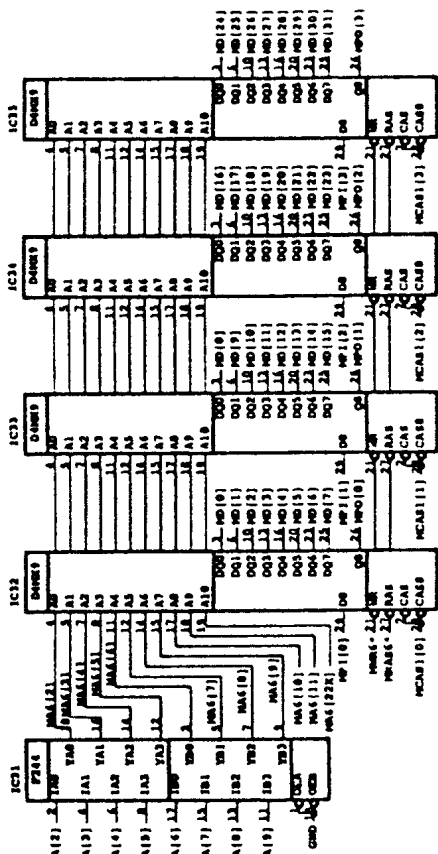
SCATTERPACK FROM



FAST INSTRUCTION MEMORY



PRIENTEA, MEM-3
MEMORY DATA AND INSTRUCTION PATHS
REV. 10-1981-04-13 DL



DUAL-PORT MEMORY

PARITY CIRCUITRY

VIDEO CONTROLLER, CLUT, AND DACS

IMAGE MEMORY BANK 9 (LEFT/RIGHT TWO FIELDS)

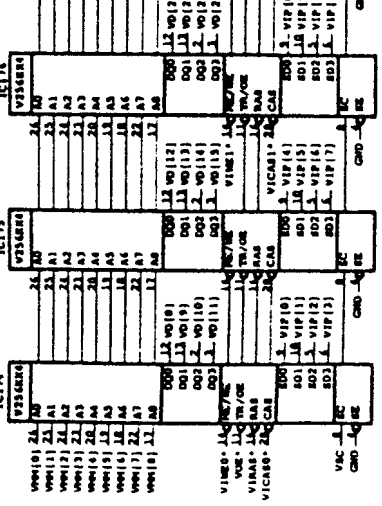


IMAGE MEMORY BANK 1 (LEFT/RIGHT TWO FIELDS)

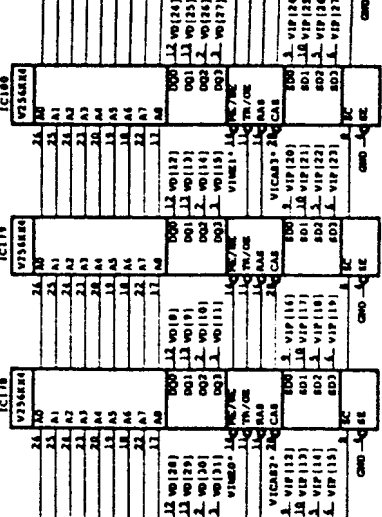
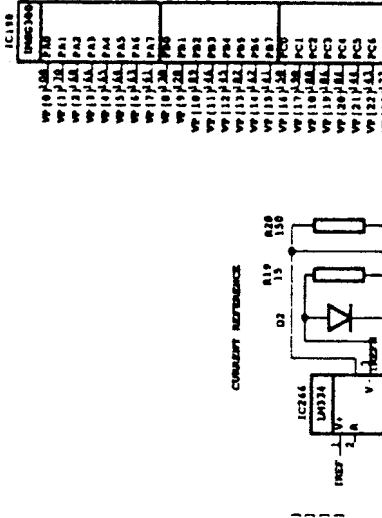
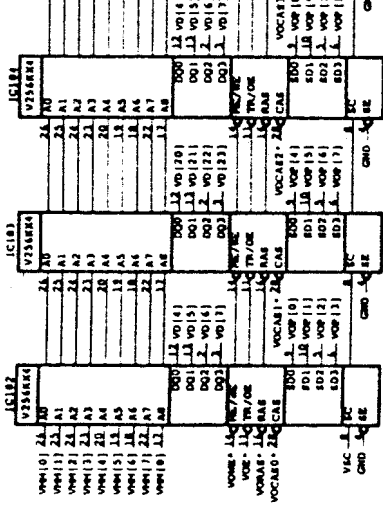


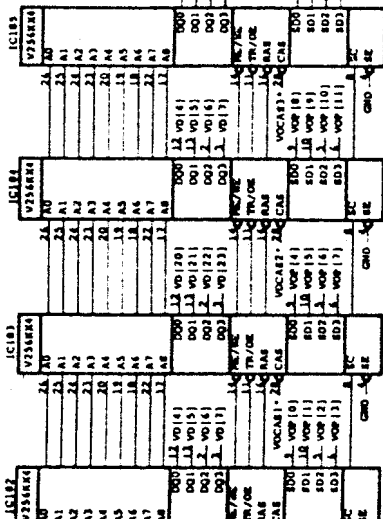
IMAGE MEMORY BANK 2 (LEFT/RIGHT TWO FIELDS)



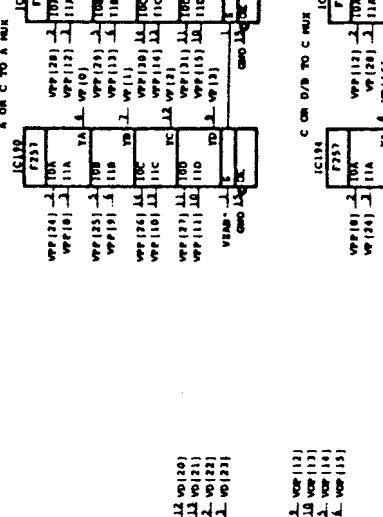
OVERLAY MEMORY BANK 0



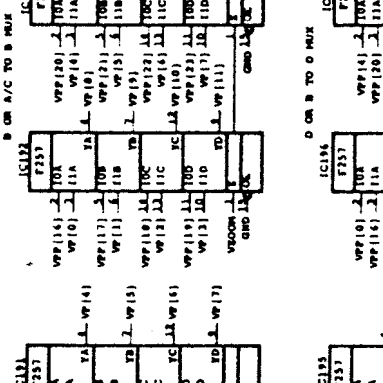
OVERLAY MEMORY BANK 1



A OR C TO A MUX



B OR A/C TO B MUX



C OR B TO C MUX

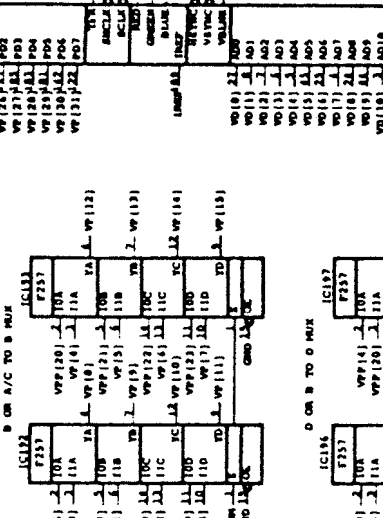
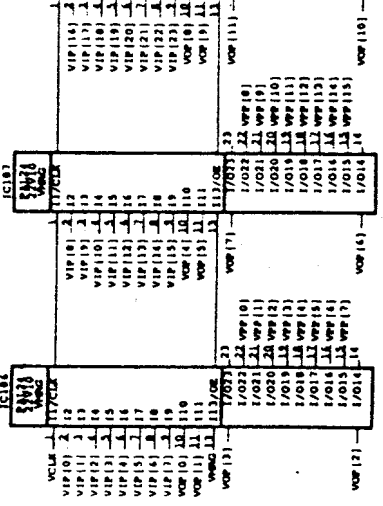
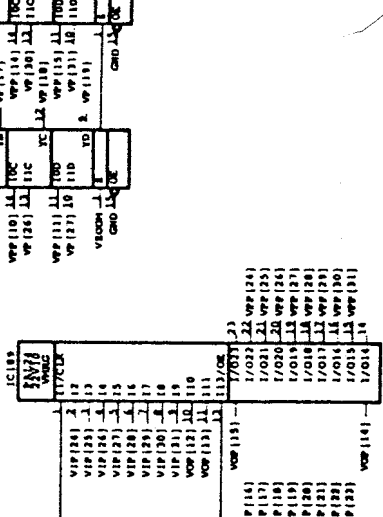


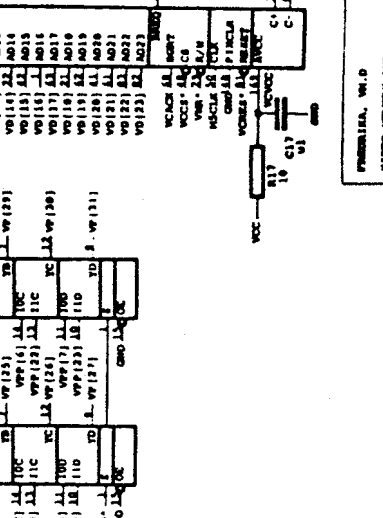
IMAGE - OVERLAY COMBINERS



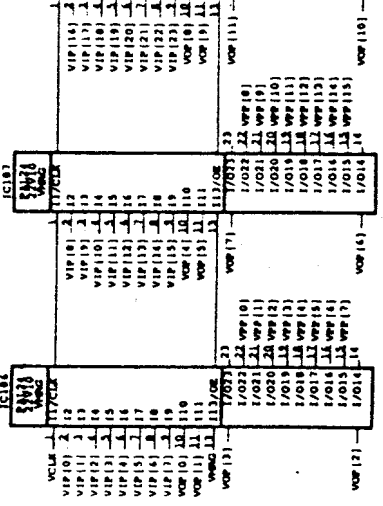
VIDEO CONTROLLER



CLUT AND DACS

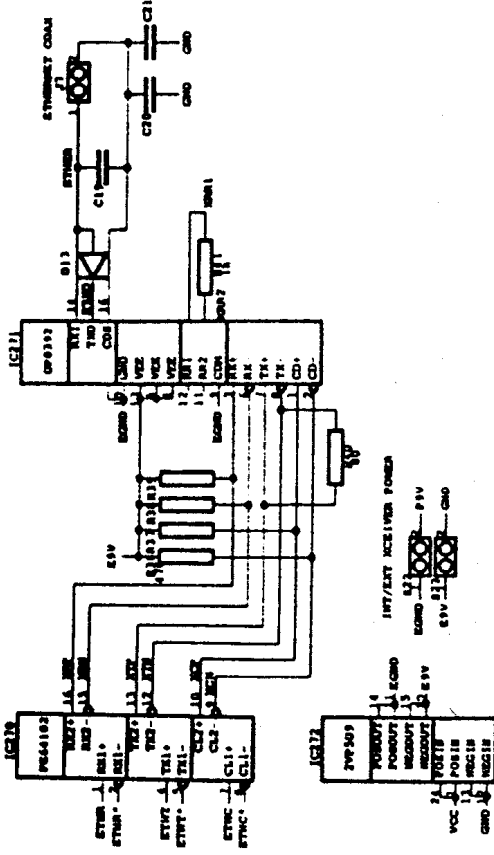


VIDEO MEMORY AND OUTPUT

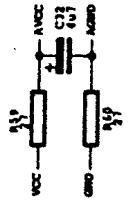
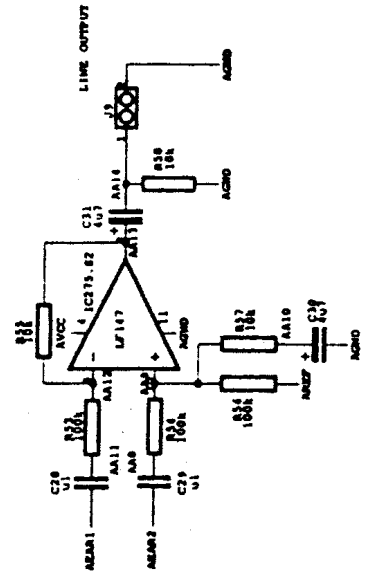
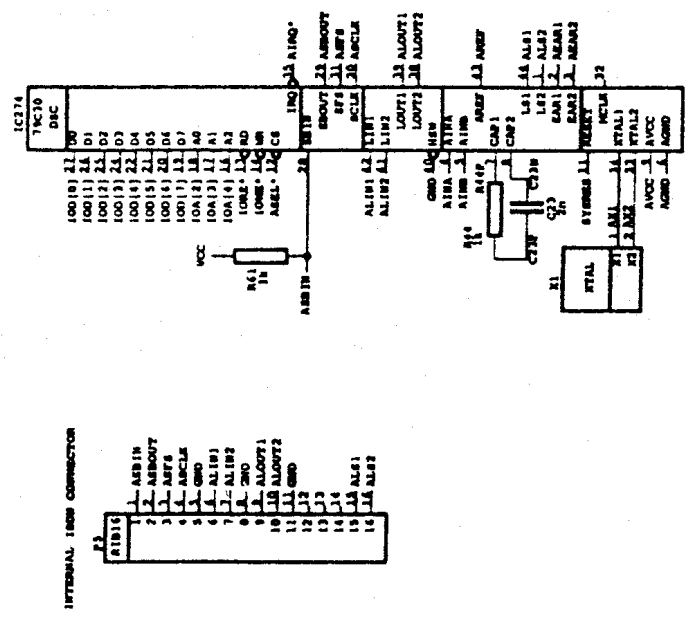
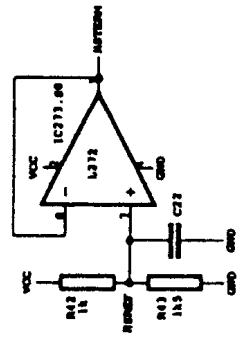


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VIDEO MEMORY AND OUTPUT
REV. 80 1989-05-19 BL

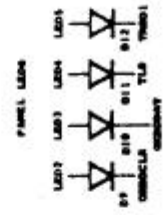
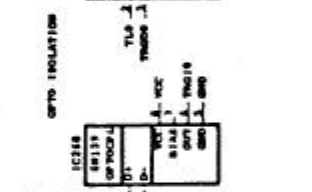
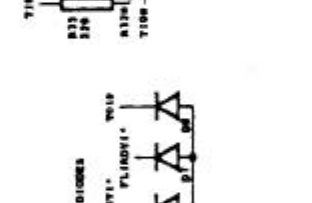
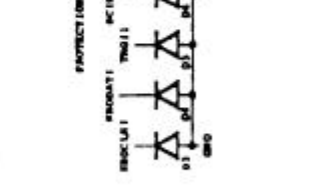
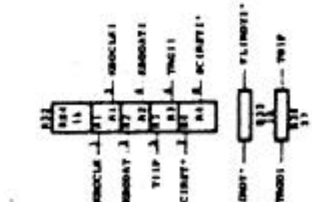
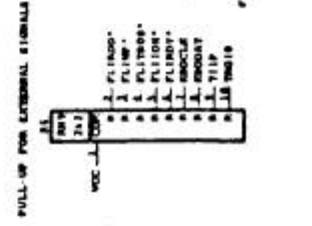
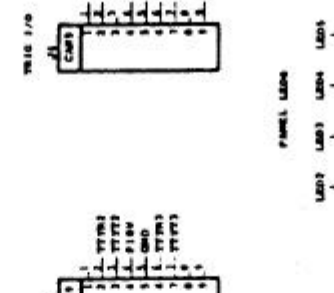
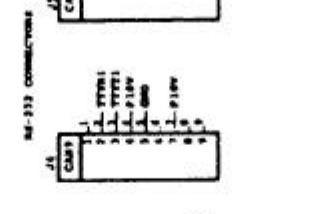
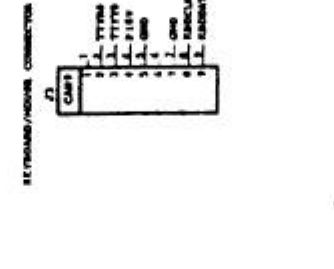
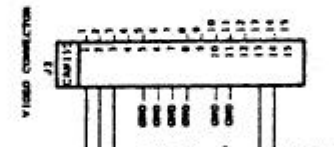
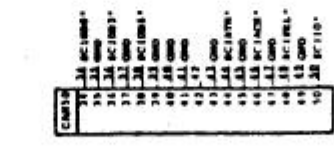
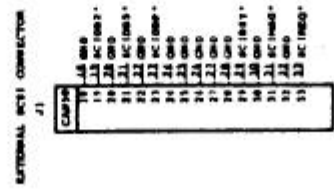
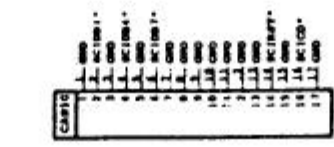
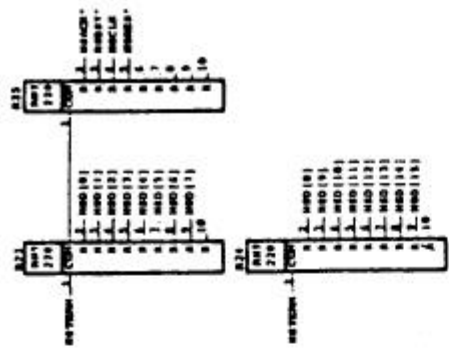
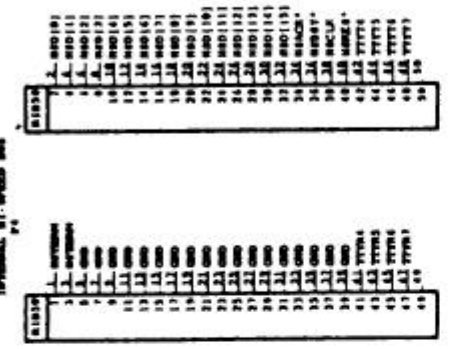
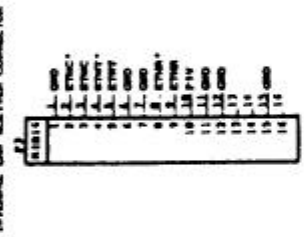
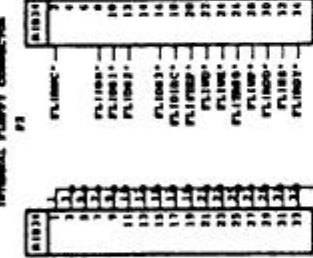
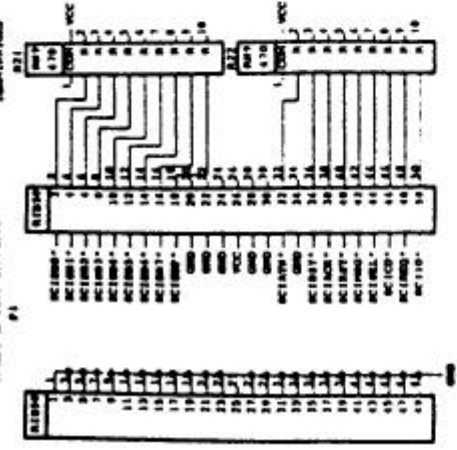
STEREOPHONIC TRANSMITTER



HI-SPEED BIAS TERMINATION SUPPLY



INTERNAL RESET CONNECTOR TERMINATIONS INTERNAL FLIGHT CONNECTOR INTERNAL LAP RECEIVED CONNECTOR INTERNAL 51-6000 800 50% TERMINATION



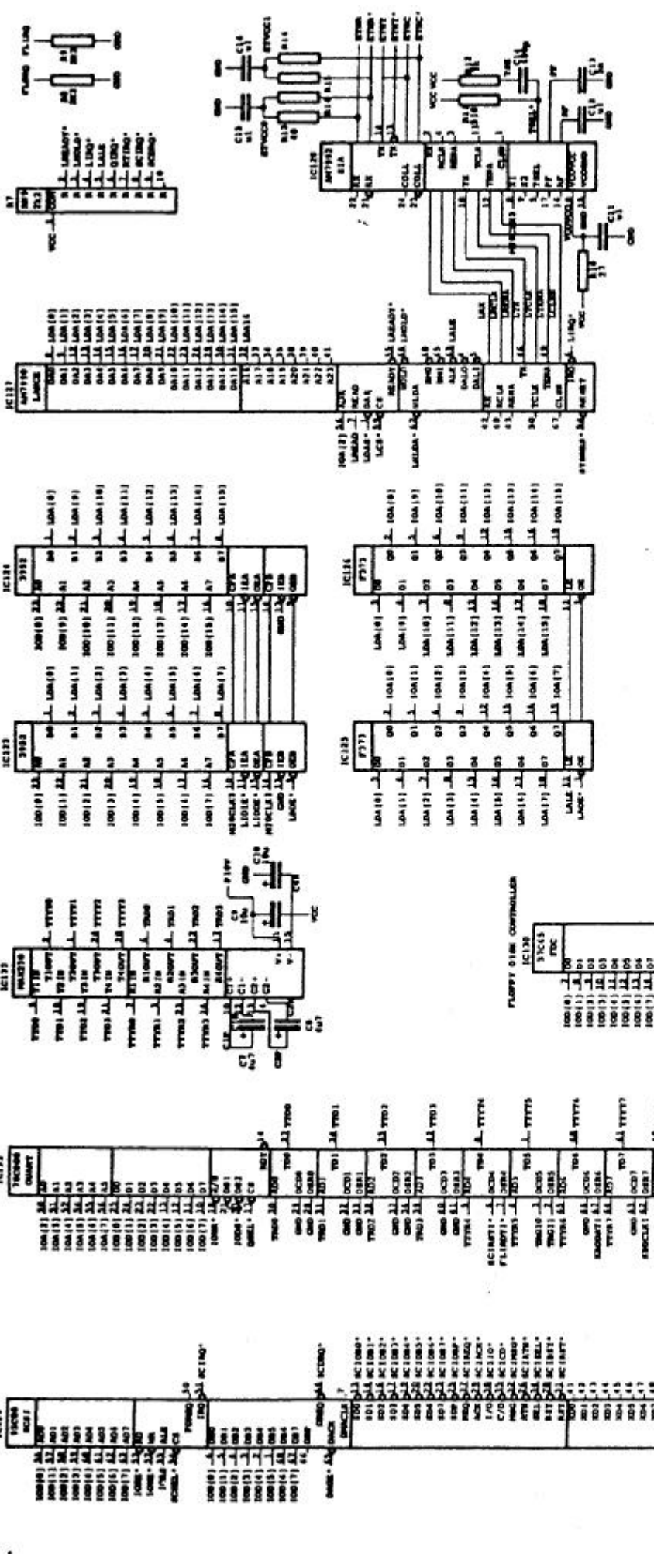
MSB CONVERTER

VTV INTERRUPT

MS-232 CONVERTER

LANCIS DATA AND ADDRESS BUFFERS

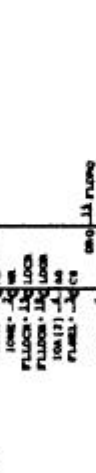
PERIPHERAL I/F INTERFACE



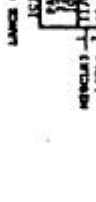
GLOBAL CONTROL REGISTER



FLOPPY DRIVE CONTROLLER



LANCIS CONTROL



PERIPHERAL SIGNALS



I/O DECODEMENTS

