bc824/827VXI
Rubidium Frequency Standard
8500-0094

User's Guide
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bc824/827VXI
RUBIDIUM FREQUENCY STANDARD

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CHAPTER ONE
GENERAL INFORMATION

1.0 INTRODUCTION

This User's Guide provides information on the installation and operation of the bc824/827VXI Rubidium Frequency Standard (VRFS).

1.1 USER'S GUIDE SUMMARY

This User's Guide is divided into the following chapters:

Chapter One - General Information
This chapter includes a general description of the VRFS including key features and specifications.

Chapter Two – Installation and Setup
Describes initial configuration, set up, and installation.

Chapter Three – Functional Description
Provides a detailed Theory of Operation of the unit.

Chapter Four – Software Interface
Provides information on the available low level and high level VXIbus commands.

Chapter Five - Parts Lists
Provides a list of parts (by Datum Part Number) of the items/materials in this unit. Customer specified options are not included in this Parts List.

Chapter Six - Drawings
Includes the Top Assembly drawing of the VRFS and associated Assembly drawings. Customer specified options are not included in this Drawing List.

1.2 PRODUCT DESCRIPTION – bc824VXI

The Datum Model bc824VXI is a VXIbus Rubidium Frequency Standard (VRFS). The bc824/827VXI product line consists of the existing design that is feature backward compatible to the Datum Efratom VRFS unit. In addition, it has the standard time and frequency processing capabilities of the Datum board level product line. It can also be provided with an additional option bay card.

This VRFS is an ultra-stable miniature atomic (Rubidium) oscillator for use as a VXIbus system clock. It is housed in a C-size VXIbus module as defined by the VXIbus specification. The VRFS is a message-based device that offers timing accuracy of ± 1 ppb over its specified operating temperature at the VXIbus system clock frequency of 10 MHz. The VRFS provides eight 10 MHz coaxial outputs in both sinusoidal and TTL (square) waveforms. The VRFS accommodates external calibration inputs for disciplining the on-board atomic (Rubidium) oscillator.

An internal, low phase noise 10MHz Voltage Controlled Crystal Oscillator (VCXO) is disciplined to the internal Rubidium oscillator. This provides a low phase noise 10MHz sine wave with the long-term stability of a Rubidium oscillator. All timing outputs/functions on this card come from or are derived from this VCXO.

1.2.1 KEY FEATURES

Rubidium Oscillator Modes of operation are supplemented by flywheel operation. If the synchronization source is lost the bc824/827VXI will continue to function at the last known reference rate. The following operational modes are supported: (Modes are distinguished by the reference source).

Free Running – Internal 10MHz Synchronization
External 10 MHz Synchronization
External GPS Syncronization
External 1 PPS Synchronization
External IRIG B AC or DCLS (DC Level Shift) Synchronization

Mode	Source of Synchronization
IRIG	Time Code – IRIG B (AM or DCLS)
FRUN	Free Running – Internal 10 MHz Selected Reference
PPS	1 PPS – External One Pulse Per Second Input
CAL	Calibration - External 10 MHz Selected Reference
	Reserved
GPS	GPS (bc827VXI) - GPS Antenna/Receiver

The VRFS generates IRIG B time code synchronized to the reference source. Modulated and DC level shift formats are produced simultaneously.

A Programmable Periodic (Heartbeat) output is provided. The output frequency is programmable from 10MHz to 3Hz in 1Hz steps and can be synchronized to the VRFS 1PPS output signal.

A Time Coincidence Strobe output is provided. It is programmable from hours through microseconds. This strobe also has an each second mode programmable to microseconds.

Three maskable interrupt sources are supported including voltage events, frequency events, and disciplining events. All interrupt sources can be polled. VXI IRQ levels one through seven are programmable.

The internal clock has a resolution of 50 nanosecond.
A Message Based Device interface based on the Datum Efratom VRFS VXI Rubidium Frequency Standard is used to access information. Time can also be accessed by a Register based interface.

There is an independent set of time registers. These 16x16 bit registers latch and hold the current time on request. Time is provided in either a binary format (UNIX seconds through 100 nanoseconds), or decimal format (days through 100 seconds). Minor time is always binary with a resolution of 100 nanoseconds.

It is a two-Slot Wide, C-Size VXIbus Module.

1.3 PRODUCT DESCRIPTION – bc827VXI

With the addition of a GPS Receiver Module, the bc824VXI becomes the Model bc827VXI VXIbus Rubidium Frequency Standard (VRFS). The bc827 contains all the features and attributes of the bc824. The additional GPS capability provides the ability to set the time of the VRFS to UTC (Universal Time Coordinated) i.e. the time standard maintained by the U.S. Naval Observatory, and provide a precise 1PPS pulse to which the VRFS will lock.

The GPS Receiver Module operates on the civilian L-band (1575.42MHz) utilizing C/A (Coarse Acquisition) code transmissions to monitor time and frequency data from the Navstar satellite constellation. Time and frequency is determined from satellite transmissions and calculations referenced to USNO (United States Naval Observatory) through the GPS Master Clock system. This link provides traceability to USNO and all international time scales through the use of publications from NIST (National Institute of Standards Technology), USNO, and BIPM (Bureau of International Des Poids et Measurements) in Servres, France.

The GPS Receiver Module automatically acquires and tracks satellites based on health status and elevation angle. In the AUTO mode, four satellites are required for the GPS Module to do three dimensional (latitude, longitude, and altitude) position fixes (i.e. to acquire accurate position data).

1.3.1 NAVSTAR/GPS DESCRIPTION

The Navstar/GPS satellite-based timing and navigation system consists of a constellation of high altitude satellites orbiting the earth every twelve sidereal hours, a group of ground-based control/monitoring stations and the user equipment which may be located on land, sea and/or air.

The GPS System was completed in the early 1990's and provides three dimensional positioning, velocity, and time, on a continuous world-wide basis. The constellation is comprised of twenty-one satellites and three spares. The satellites are located in six different orbital planes inclined approximately sixty degrees to the equator at altitudes of 10,400 miles above the earth.

The GPS Receiver Module determines time and frequency by measuring the time of arrival of the precise timing mark and measuring the Doppler effect from one satellite. A previously entered or determined position allows computation of the receivers time offset. An accurate timing mark (1pps) can be set with respect to UTC. The satellite positions are known within a few meters and the satellite clocks are calibrated within a few nanoseconds so position can be computed within an absolute accuracy of better than 120 meters (with current selective availability).

The GPS signal transmitted from a satellite consists of two carrier frequencies. L1 at a frequency of 1575.42 MHz and L2 at a frequency of 1227.6 MHz. The L1 signal is modulated with both a precision (P) code and a coarse acquisition (C/A) code. The precision (P) code is available to authorized users only. The GPS Timing Unit operates on the C/A code.

Each satellite transmits a unique C/A code that reflects the satellite identity for acquisition and tracking. The C/A PRN code is a gold code of 1023 bits repeating at a one-millisecond rate.

The L1 and L2 frequency is also modulated with a fifty-bit-per-second data stream providing satellite ephemerides, system time, satellite clock behavior, and status information on all satellites. The data message is contained in a data frame that is 1,500 bits long.

Ground based control/monitoring stations track the satellites and provide an upload several times each day to provide a prediction of each satellites ephemeris and clock behavior for the next day's operation.

1.4 PERFORMANCE SPECIFICATIONS

1.4.1 ELECTRICAL

A. OUTPUTS: (See Front Panel Drawing, Figure 1-1)

SIGNAL	QUANTITY	SIGNAL LEVEL	CONNECTOR
10 MHz SINE	0 to 8*	2 Vpp Sine into 50 Ω	BNC
10 MHz TTL	0 to 8*	TTL into 50 Ω	BNC

*Each of the 8 BNC outputs are internally jumper selectable for 10MHz sine wave or TTL square wave.

10 MHz FREQUENCY STABILITY:

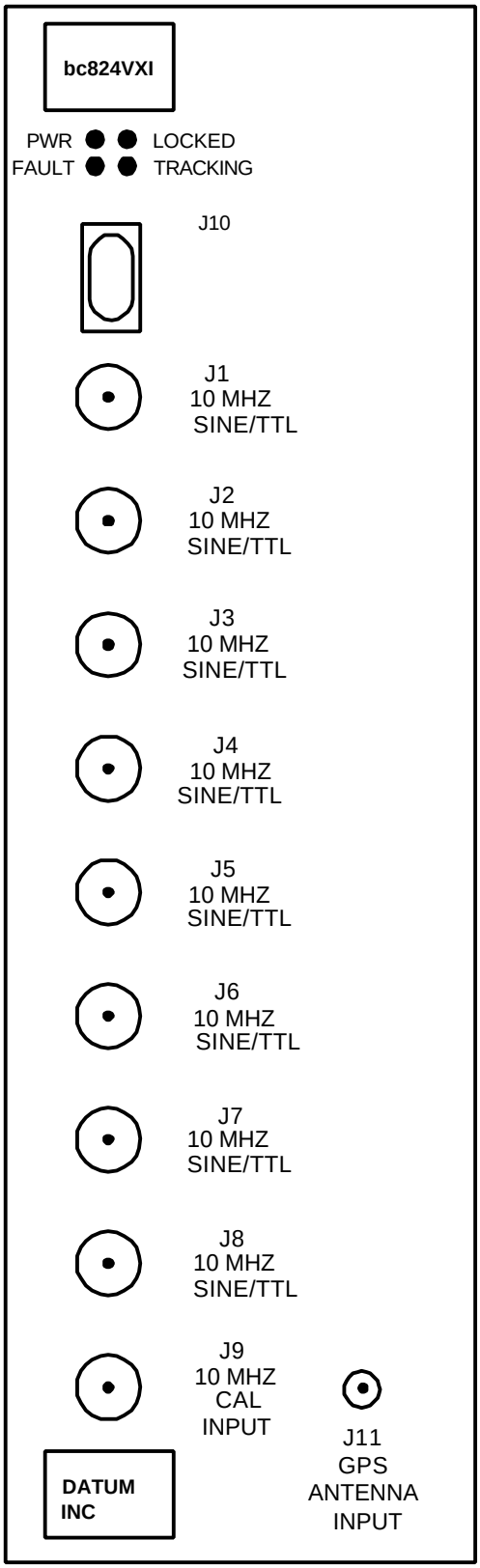
SHORT-TERM STABILITY

1 Second (Allan Variance)	$1e^{-10}$
10 Second (Allan Variance)	$3e^{-11}$
100 Second (Allan Variance)	$1e^{-11}$
1-Day Stability @ 25C ± 3C	$1e^{-10}$
Drift per Month	$5e^{-11}$
(after 1 month continuous operation)	
Accuracy at Shipment @ 25C	$5e^{-11}$
Frequency Retrace	$5e^{-11}$
(after 1 hour power ON @ 25C and less than 25 hours power OFF)	

PHASE NOISE	
1 Hz Offset	< -75 dBc/Hz
10 Hz Offset	< -110 dBc/Hz
100 Hz Offset	< -140 dBc/Hz
1 kHz Offset	< -150 dBc/Hz
10 kHz Offset	< -150 dBc/Hz

SPECTRAL PURITY	
Harmonics	< -50 dBc
Non-Harmonic Spurious	< -80 dBc
Noise Floor	< -150 dBc

Figure 1-1


bc824VXI
PWR
FAULT
LOCKED
TRACKING
J10
J1
10 MHZ
SINE/TTL
J2
10 MHZ
SINE/TTL
J3
10 MHZ
SINE/TTL
J4
10 MHZ
SINE/TTL
J5
10 MHZ
SINE/TTL
J6
10 MHZ
SINE/TTL
J7
10 MHZ
SINE/TTL
J8
10 MHZ
SINE/TTL
J9
10 MHZ
CAL
INPUT
J11
GPS
ANTENNA
INPUT
DATUM
INC

OUTPUT CHARACTERISTICS:

Isolation Between Outputs	> -80 dB
Fault Protection	Short Circuit

WARM-UP TIMES:

Time To Lock @ 25C	< 5 minutes
Minutes/Frequency @ 25C	10 minutes/$1e^{-9}$

B. ADDITIONAL OUTPUTS:

TIME CODE (Amplitude Modulated)

The VRFS generates an amplitude modulated IRIG B time code signal synchronized to the input timing source. This signal is on front panel 15 pin high density D connector J10 pin 15. Time code shall track the selected timing source to within +/- 5 microseconds.

The characteristics are as follows:

Format:	IRIG B122.
Amplitude:	4V programmable peak-peak (nominal).
Ratio:	3:1/6:1 (software selectable).
Output Impedance:	50 Ohms.

TIME CODE (DC Level Shift)

The VRFS generates a DCLS IRIG B time code signal synchronized to the input timing source with the following characteristics. This signal is on front panel 15 pin high density D connector J10 pin 14. Time code shall track the selected timing source to within +/- 5 microseconds.

Format:	IRIG B002
Signal Specification:	Single ended, TTL compatible (using the + sense of the differential signal) into 50Ω.

1PPS OUTPUT

The VRFS generates a 1 PPS signal derived from the input timing signal (or from the on-board 10MHz oscillator in flywheel mode). This signal is on front panel 15 pin high density D connector J10 pin 11.

The output characteristics are:

Signal Levels:	TTL when driving ≥ 50 Ohms.
Timing:	Rising edge on-time.
Pulse-width:	1 millisecond.

PERIODIC OUTPUT

The VRFS generates a programmable periodic digital output signal, with a programmable pulse width, that is generated by dividing down a 20MHz clock. The 20 MHz clock is derived from the 10 MHz VCXO, thus the Periodic Output is synchronous with the timing source. The periodic output frequency is software programmable from 10 MHz to 3 Hz. The Periodic Output is synchronized to the VRFS 1PPS signal if the frequency is an integer sub-harmonic of the 20 MHz clock. At output frequencies greater than 100 kHz, the synchronization to the 1PPS signal is less effective.

This signal is on front panel 15 pin high density D connector J10 pin 13, and will output TTL levels into a 50 ohm load.

STROBE OUTPUT

The VRFS provides a programmable Time Coincidence Strobe Output signal. The Strobe resolution is from hours through microseconds. The duration of the Strobe pulse is 5 to 10µsec. The rising edge of the Strobe occurs at the programmed time. Two modes of operation are supported. In one mode, both the major and minor time are used to generate the Strobe output once each day. In the other mode, only the minor time is used to generate the Strobe output once each second. This signal is on a front panel 15 pin high density D connector J15 pin 12, and will output TTL levels into a 50 ohm load.

C. INPUTS:

10 MHz CAL

The VRFS supports an external 10 MHz calibration input on a front panel BNC.

The input characteristics are:

Amplitude:	1 to 2 volts peak-to-peak sine wave into 50Ω.
Input Impedance:	50Ω.
Loading:	AC coupled.

TIME CODE (Amplitude Modulated)

The VRFS supports IRIG B single-ended amplitude modulated time code format and signal characteristics for use as time setting only. This signal is on front panel 15 pin high density D connector J10 pin 5.

Formats:	IRIG B120, IRIG B121, IRIG B122, and/or IRIG B123 per IEEE 1344.*
Amplitude:	500mV to 5V peak-peak.
Modulation Ratio:	3:1 to 6:1.
Impedance:	>10kOhms, AC coupled.

* The VRFS will accept IRIG B123 per IEEE 1344. However, IRIG bits P50 through P79 are not translated.

TIME CODE (DC Level Shift)

The VRFS supports IRIG B DCLS time code formats and signal characteristics for use as time setting and synchronization. This signal is on front panel 15 pin high density D connector J10 pin 4.

Formats:	IRIG B000, IRIG B001, IRIG B002, IRIG B003 per IEEE 1344
Signal Specifications:	Single-ended, TTL and CMOS compatible.
Loading:	10kOhms DC Coupled; 50 Ohms AC Coupled.

EXTERNAL 1PPS

The VRFS supports an external 1PPS signal for use as a timing source. This signal is on front panel 15 pin high density D connector J10 pin 1.

Format:	Positive Edge On Time.
Signal Specifications:	Single-ended, TTL and CMOS compatible.
Timing:	100ns minimum width.
Loading:	10kOhms DC Coupled; 50 Ohms AC Coupled.

EVENT CAPTURE

The VRFS supports two software programmable external event capture signals (Event 1 and Event 2). These signals are programmable/selectable and are input on front panel 15 pin high density D connector J10 pin 2 (Event 1) and J10 pin 3 (Event 2). Two FIFOs can capture up to 256 events each consisting of minor and major time. If either input is programmed for rising or falling edge, worse case accuracy is 50 ns. However, if Event 1 is dedicated to a rising edge, and Event 2 is dedicated to a falling edge, the accuracy is 5 ns with a resolution of 1 ns.

Format:	Rising or Falling Edge Triggered.
Signal Specifications:	Single-ended: TTL and CMOS compatible.
Timing:	100 nanoseconds minimum width, 10 microseconds minimum period.
Loading:	10kOhms DC and 50 Ohms AC.

GPS RECEIVER (Optional bc827VXI)

The VRFS mechanically supports both the Trimble ACE II and Motorola Encore GPS Receiver modules. This allows the VRFS to be synchronized to the GPS system 1PPS.

A Bias-T Circuit is provided to allow a separate +5 volts (external to the GPS Receiver module) to power the GPS antenna.

D. J10 I/O CONNECTOR:

The following table defines additional input and outputs available to/from the VRFS on the front panel 15 pin D connector J10:

PIN NO.	FUNCTION
1	1PPS Input
2	Event 1 Input
3	Event 2 Input
4	IRIG B DCLS (DC Level Shift) Input
5	IRIG B AC Input
6	Ground
7	Ground
8	Ground
9	Ground
10	Ground
11	1PPS Output
12	Strobe Output
13	Periodic Output
14	IRIG B DCLS (DC Level Shift) Output
15	IRIG B AC Output

For signal specifications, refer to Section 4.1.1 B and C.

1.4.2 MECHANICAL

Size: Two-Slot Wide, C-Size VXIbus Module
Front Panel: See figure 2-1 for front panel drawing.
Power Consumption: 16 Watts/Slot
Cooling Requirements:
Airflow: 6 liter/sec @ 0.05 mm H_2O for 5 °C Rise
Weight: 5 lbs.

1.4.3 ENVIRONMENTAL

Temperature Range:
Operating: 0 °C to +50 °C Ambient
Storage: -40 °C to +75 °C

Relative Humidity:
Operating or Storage: 0 to 80% (non condensing)

Frequency Sensitivity:
Over full temperature range: $3e^{-10}$
Magnetic field: $< 3e^{-11}$/Gauss

LED INDICATORS	"ON" FUNCTION	COLOR
PWR	Power On	Green
FAULT	Output Fault	Red
LOCKED	Rb/OCXO Locked	Green
TRACKING	Tracking Selected Input Reference	Green

POWER:	DC PEAK CURRENT	DYNAMIC CURRENT	WARM-UP CURRENT
+5 V	2 A	1 A	2 A
+12 V	1 A	0.5 A	2 A
-12 V	0.5 A	0.5 A	0.5 A
+24 V	2 A	1 A	3 A
-24 V	0.5 A	0.5 A	0.5 A

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CHAPTER TWO

INSTALLATION AND SETUP

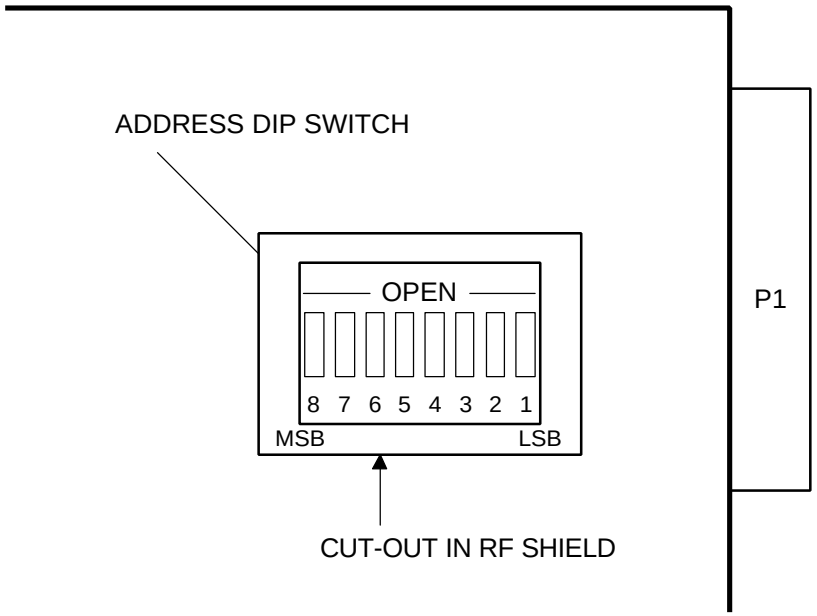
2.0 CONFIGURATION AND INSTALLATION

The VRFS is designed to be installed into any C-size VXIbus mainframe, using any slot except slot 0 (zero), which is reserved. Before installing the VRFS into the mainframe, the logical address for the VRFS must be assigned by setting the 8-position DIP switch accessible through a cut-out on the right side cover of the module (refer to Section 2.1). After setting the logical address, slide the VRFS into the VXIbus mainframe until the backplane P1 and P2 connectors are mated properly. Once the module is seated in the mainframe, tighten the two captive screws above and below the ejector handles to secure the VRFS into the mainframe.

2.1 LOGICAL ADDRESS SWITCH

The logical address of the VRFS is statically configured to any address from 1 to 254. Logical address 0 is reserved for the VXIbus resource manager, and logical address 255 is reserved for VXIbus modules supporting dynamic configuration. The logical address for the VRFS must be assigned by setting the 8-position DIP switch accessible through the cut-out on the right side cover of the module. Figure 2-1 shows a view of the location of the DIP switch on the VRFS. Position 8 of the DIP switch corresponds to the most significant bit of the logical address and position 1 corresponds to the least significant bit of the logical address. A switch in the OPEN position corresponds to a logic 1, and a switch in the CLOSED position corresponds to a logic 0.

Figure 2-1



2.2 BACKPLANE IACK* AND BGn* JUMPERS

The VRFS is an interrupting device and uses the IACKIN* and IACKOUT* signals. The mainframe must be configured to OPEN the connection between these two signals for the slot in which the VRFS is plugged into the P1 connector. Ensure that the IACK* jumper is in the OPEN position according to the manufacturer's guidelines. The VRFS is a slave and does not use the BGnIN* or BGnOUT* signals. The VRFS is internally jumpered to transparently pass the BGn* signals through to the next slot. Consequently, the BGn* jumpers can be configured in either position and will not affect the proper operation of the VXIbus system.

2.3 ADVANCED CONFIGURATION OPTIONS

The VRFS has some internal jumpers that are configured at the factory and should not be changed without proper guidance from the manufacturer. The function of these jumpers is included here for completeness. Figure 1-4 shows a view of the circuit board of the VRFS identifying all jumpers and header connectors. Table 2-1 lists the functions of the jumpers. Table 2-2 lists the functions of the header connectors.

Table 2-1
Factory Jumper Configuration Options

JUMPER	CONFIGURATION OPTIONS	
JP1	Jumper 1-2: Sine Output at J8	Jumper 2-3: TTL Output at J8
JP2	Jumper 1-2: Sine Output at J7	Jumper 2-3: TTL Output at J7
JP3	Jumper 1-2: Sine Output at J6	Jumper 2-3: TTL Output at J6
JP4	Jumper 1-2: Sine Output at J5	Jumper 2-3: TTL Output at J5
JP5	Jumper 1-2: Sine Output at J4	Jumper 2-3: TTL Output at J4
JP6	Jumper 1-2: Sine Output at J3	Jumper 2-3: TTL Output at J3
JP8	Jumper 1-2: Sine Output at J2	Jumper 2-3: TTL Output at J2
JP10	Jumper 1-2: Sine Output at J1	Jumper 2-3: TTL Output at J1
JP11	Removed: Sine Output at J1	Installed: TTL Output at J1
JP12	Removed: Sine Output at J2	Installed: TTL Output at J2
JP13	Removed: Sine Output at J3	Installed: TTL Output at J3
JP14	Removed: Sine Output at J4	Installed: TTL Output at J4
JP15	Removed: Sine Output at J5	Installed: TTL Output at J5
JP16	Removed: Sine Output at J6	Installed: TTL Output at J6
JP17	Removed: Sine Output at J7	Installed: TTL Output at J7
JP18	Removed: Sine Output at J8	Installed: TTL Output at J8
JP7	Jumper 1-2: DSP MP mode	Jumper 2-3: DSP MC mode
JP9	Jumper 1-2: configuration mode	Jumper 2-3: operation mode

EXAMPLES OF JP1 (i.e. J8) JUMPERED
FOR SINE AND TTL OUTPUT

SINE:

TTL:

Table 2-2
Header Connector Functions

CONNECTOR	FUNCTION
P3	JTAG connector for in-circuit programming of CPLDs (U3, U40)
P6	Serial connector for interface to DSP (for use with serial cable)
P8	Serial connector for in-circuit programming of FPGA (U53)
P7	JTAG connector for in-circuit emulation and downloading of DSP

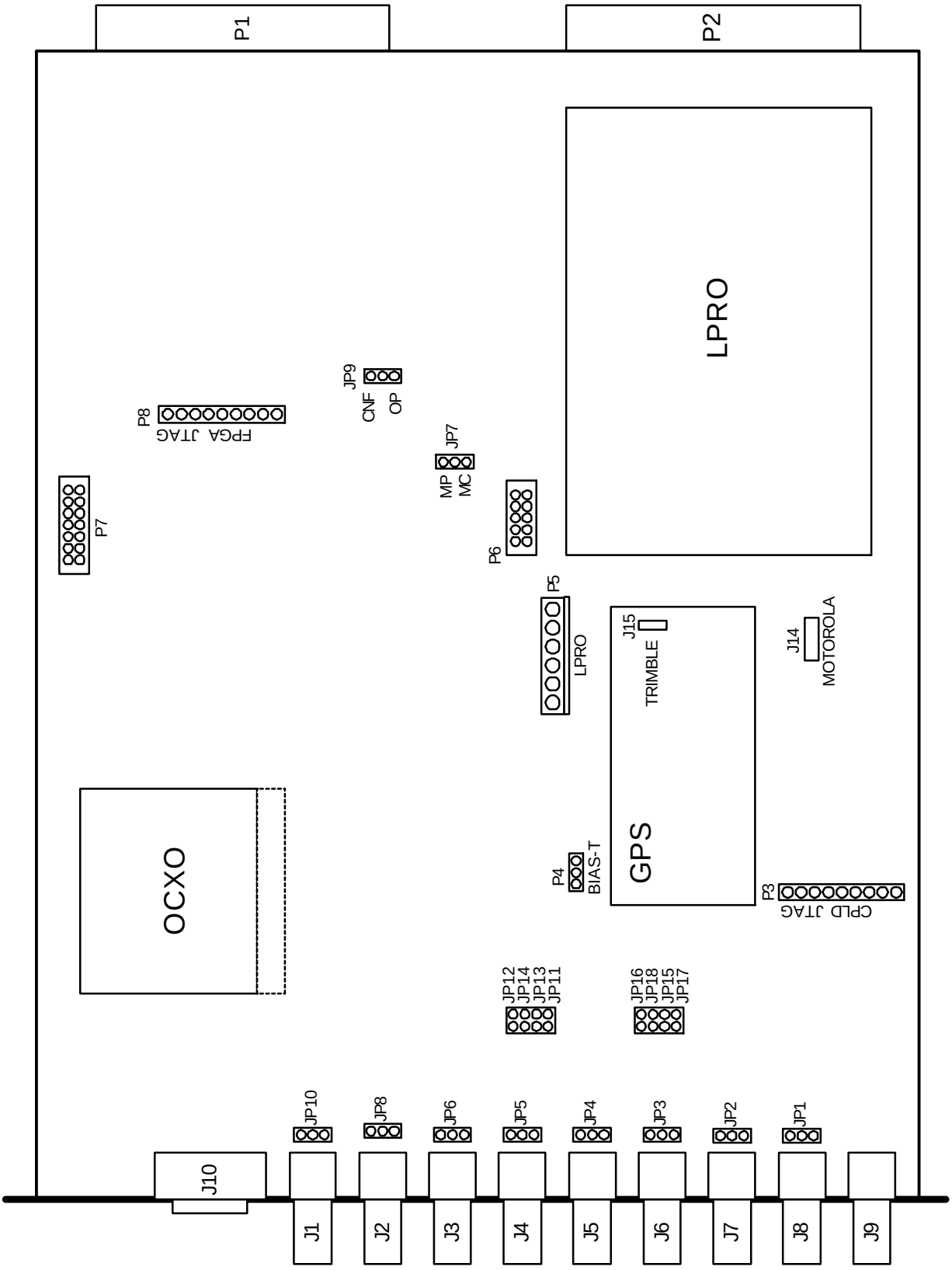


Figure 2-2. Jumper and Header Locations of Model bc824/827VXI VRFS

CHAPTER THREE
FUNCTIONAL DESCRIPTION

3.0 GENERAL

The VRFS is an ultra-stable miniature atomic oscillator for use as a VXIbus system clock housed in a C-size VXIbus module as defined by the VXIbus specification. The VRFS is a message-based device that offers timing accuracy of ± 1 ppb over its specified operating temperature at the VXIbus system clock frequency of 10 MHz. The VRFS provides eight 10 MHz coaxial outputs in both sinusoidal and square waveforms. The VRFS accommodates external calibration inputs for disciplining the on-board atomic oscillator. These external calibration inputs include a 10 MHz sinusoid, a 1PPS input, IRIG time coding, and a GPS receiver.

3.1 THEORY OF OPERATION

A functional block diagram of the VRFS is shown in Figure 3-1. The VRFS operation is centered around an on-board Texas Instruments TMS320F240 digital signal processor (DSP). The DSP provides the intelligence for controlling all functions of the VRFS, including the VXIbus interface, the output control loop, the rubidium calibration control loop, the fault monitoring, and the timing signal capture and generation functions. The VXIbus interface functions includes interpreting and responding to message-based commands and accessing the A16 timing registers. The output control loop function enables the DSP to discipline the VRFS outputs with respect to the rubidium oscillator. The VRFS outputs are generated by an oven-controlled crystal oscillator (OCXO) that is phase-locked to the rubidium oscillator. In this manner, the VRFS outputs have the long-term (low-frequency) drift and stability characteristics of the rubidium oscillator and the short-term (high-frequency) phase noise characteristics of the OCXO. The rubidium calibration control loop enables the DSP to discipline the rubidium oscillator (LPRO model) to an external calibration source. These external calibration inputs include a 10 MHz sinusoid, a 1PPS input, IRIG time coding, and a GPS receiver. The calibration loop is active only when an external calibration source is present. In this manner, the VRFS can be calibrated with an external reference and hold that state when the calibration source is removed. The fault monitoring function includes monitoring the outputs for short-circuit conditions, monitoring the LPRO rubidium oscillator for lock, monitoring the DSP control loops for lock, monitoring the backplane voltages, and monitoring the option fault condition. The timing signal capture and generation functions involve the DSP time tagging external events, generating pulsed waveforms with specified timing properties, and the generation and decoding of IRIG time coded signals.

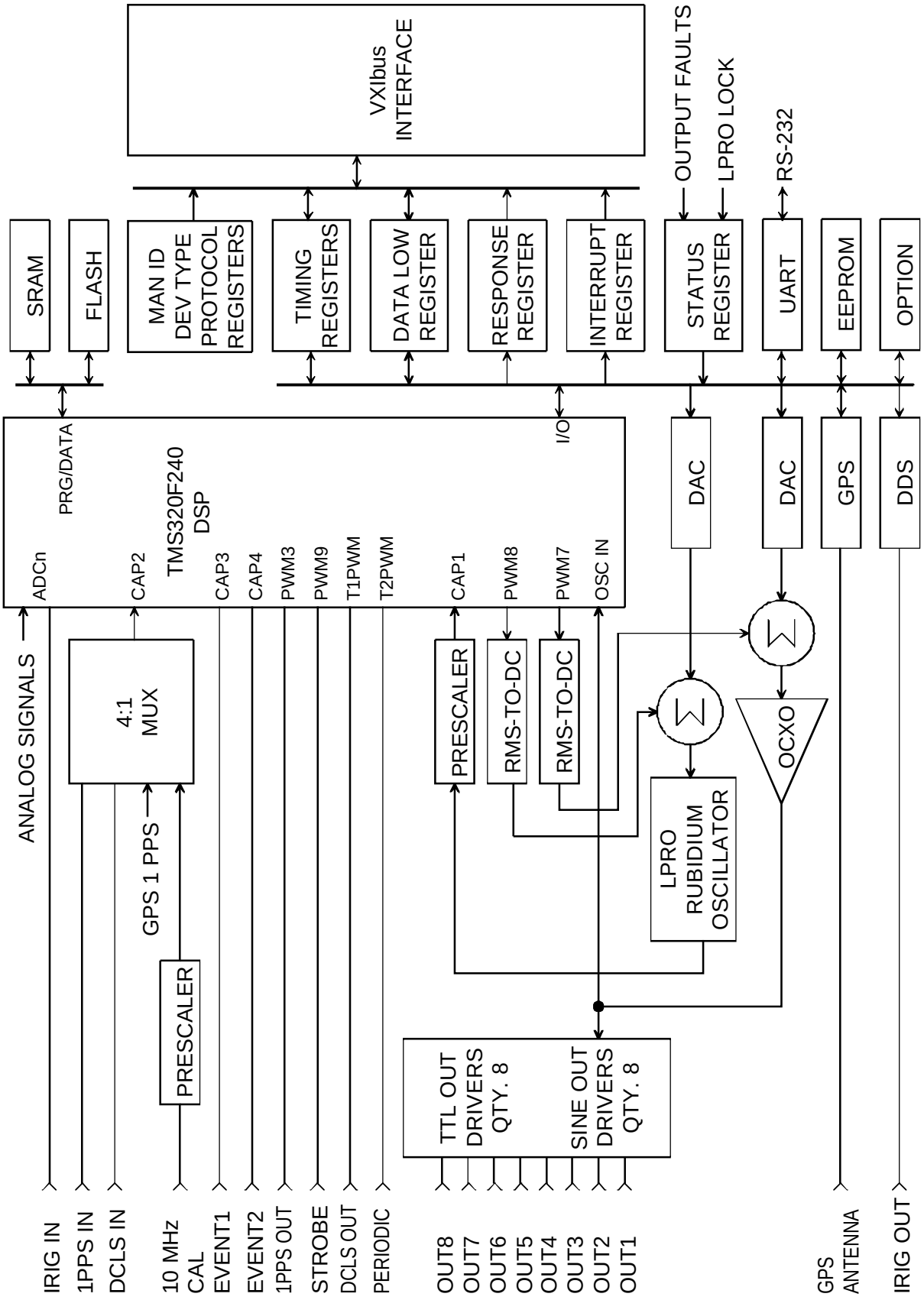


Figure 3-1. Block Diagram of Model bc824VXI VRFS

3.1.1 DSP RESOURCES

The Texas Instruments TMS320F240 DSP uses both on-chip and external peripherals to perform the VRFS functions. The internal peripherals include FLASH memory, random-access memory (RAM), time capture (CAP) inputs, pulse-width modulation (PWM) and compare (CMP) outputs, and analog-to-digital converters (ADC). The DSP program firmware is stored within the on-chip FLASH memory. The on-chip SRAM is used by the to run the program firmware. The time-capture inputs are used to time-tag external events including the 1 pps inputs for the control loops. Pulse-width modulation and compare outputs are used to generate pulsed waveforms for outputs and for the control loops. The ADC inputs are used to monitor the VXIbus backplane voltages, the control voltages produced by the oscillator loops, and the time-capture charge-pump voltages. Also, ADCs are used to demodulate the IRIG time-coded carrier to detect the encoded timing information.

External memory peripherals for the DSP include static random-access memory (SRAM), FLASH memory, and EEPROM. The external SRAM provides additional memory to the DSP to run the program firmware. The FLASH memory is used to store the bit file to download an on-board FPGA upon power-up. The EEPROM is used for storing calibration and configuration data in non-volatile memory. Other external peripherals include the VXIbus interface registers, a Status Register, a universal asynchronous receiver/transmitter (UART), digital-to-analog converters (DAC), a direct digital synthesizer (DDS), an optional global positioning system (GPS) daughter card, and an optional expansion card. The DSP interfaces to the VXIbus host processor via the message-based protocol using the Data-low Register and the Response Register. In addition to the message-based interface, timing registers in A16 register-based memory provide minimum latency access to time-keeping data. Also, the DSP can interrupt the VXIbus host processor using one of the backplane IREQn* lines. The interrupt level and interrupt vector are assigned by the DSP writing to an Interrupt Register. A Status Register provides the DSP with all fault and alarm indications. A UART provides a serial RS-232 interface for interfacing the DSP. DACs provide the coarse adjustment for the control voltages in the two oscillator control loops. A DDS provides a time-coded IRIG carrier output. An optional GPS unit provides a mechanism to discipline the LPRO rubidium oscillator. Lastly, an option expansion slot provides an upgrade path for additional features.

3.1.2 OSCILLATOR CONTROL LOOPS

The VRFS outputs are generated in an oscillator control loop that phase-locks the oven-controlled crystal oscillator (OCXO) to the rubidium oscillator. In this manner, the VRFS outputs have the long-term (low-frequency) drift and stability characteristics of the rubidium oscillator and the short-term (high-frequency) phase noise characteristics of the OCXO. The rubidium calibration oscillator control loop allows the rubidium oscillator (LPRO model) to be disciplined to an external calibration source. These two oscillator control loops are accomplished within DSP in the following manner.

Within the OCXO control loop, the 10 MHz output of the rubidium oscillator is digitally divided down to 1 pps using the Prescalar CPLD. This 1 pps output drives a time-capture input of the DSP for coarse (50 ns) resolution and a charge pump circuit for fine (1 ns) resolution. The repetitive occurrence of the edge of the 1 pps is measured in both coarse and fine increments. Because the OCXO provides the master clock for the DSP and related circuitry, the time-capture measurements are relative to the OCXO. When the loop is locked, this timing of the 1 pps pulse from one pulse to the next is exactly 1 second. Any deviations from the exact 1 second interval causes a change in the control voltage to affect the OCXO frequency. The OCXO control voltage is generated by the combination of the DAC output and the RMS-to-DC converter output. The DAC provides coarse adjustments and the RMS-to-DC converter provides fine adjustments in the control voltage. The RMS-to-DC converter removes the AC component of a PWM output that has a variable pulse-width that is defined by the DSP. The combined control voltage drives the control input of the OCXO to adjust its frequency to maintain the exact 1 second interval. When this loop is locked to within the frequency stability characteristics specified in this manual, the LOCKED LED is lit on the front panel.

The LPRO rubidium oscillator control loop operates in much the same fashion, except that its disciplining reference input can be either an external 10 MHz calibration signal, a GPS 1 pps signal, a DCLS time-coded waveform, or an IRIG time-coded carrier. Each of these external sources is available to the DSP time-capture circuity though use of a multiplexer (MUX). The external 10 MHz calibration signal is digitally divided down to 1 pps using the Prescalar CPLD. The 1 pps reference drives a time-capture input of the DSP for coarse (50 ns) resolution and a charge pump circuit for fine (1 ns) resolution. The repetitive occurrence of the edge of the 1 pps is measured in both coarse and fine increments. When the loop is locked, this timing of the 1 pps pulse from one pulse to the next is exactly 1 second. Any deviations from the exact 1 second interval causes a change in the control voltage to affect the LPRO frequency. The LPRO control voltage is generated by the combination of the DAC output and the RMS-to-DC converter output. The DAC provides coarse adjustments and the RMS-to-DC converter provides fine adjustments in the control voltage. The RMS-to-DC converter removes the AC component of a PWM output that has a variable pulse-width that is defined by the DSP. The combined control voltage drives the control input of the LPRO to adjust its frequency to maintain the exact 1 second interval. When this loop is locked to within the frequency stability characteristics specified in this manual, the TRACKING LED is lit on the front panel.

3.2 VXIbus INTERFACE

The VXIbus interface of the VRFS combines an A16 message-based command interface and an A16 register-based memory interface for the timing registers. The interface to the VXIbus host processor is accomplished via the message-based protocol using the Data-low Register and the Response Register. Programming of this message-based interface is discussed in detail in Section 4. In addition to the message-based interface, six timing registers are located at locations $20_{16} - 2A_{16}$ in A16 address space. These registers are discussed in detail in Section 3. Also, the VRFS can interrupt the VXIbus host processor using one of the backplane IRQn* lines. The interrupt level is assigned by the host processor using the low-level VXIbus commands. Section 3.2.1 lists the VXIbus address map for the VRFS, showing the location of all registers that are available to the VXIbus host processor. Sections 3.2.2 through 3.2.14 break the VRFS registers down to the bit level and lists the functions of each bit.

In general, all control on the module is accomplished though the VXIbus host processor via the VXIbus backplane. The host processor sends commands and queries to the VRFS to enable its functions and read its status. The command set includes the low-level VXIbus configuration commands, IEEE 488.2 common commands, commands to enable event latching, and a command to enable interrupts. The query set includes low-level VXIbus configuration queries, IEEE 488.2 common queries, queries of current frequency and voltage conditions, querries of latched frequency and voltage events. Events correspond to changes in the state of the VRFS including the locking or unlocking of the oscillator control loops, short-circuiting one of the outputs, or a fault transition in the option card. Latched events are cleared by reading the corresponding event register or with the clear command.

3.2.1 VRFS DEVICE REGISTER SUMMARY

VRFS VXIbus A16 ADDRESS SPACE		
OFFSET	**REGISTER NAME**	**TYPE**
00_{16}	DATUM MANUFACTURER'S ID	R
02_{16}	DEVICE TYPE	R
04_{16}	STATUS/CONTROL	R/W
06_{16}	OFFSET REGISTER	R/W
08_{16}	PROTOCOL	R
$0A_{16}$	RESPONSE	R
$0C_{16}$		
$0E_{16}$	DATA LOW	R/W
10_{16}		
12_{16}		
14_{16}		
16_{16}		
18_{16}		
$1A_{16}$		
$1C_{16}$		
$1E_{16}$		
20_{16}	LATCH TIME CONTROL REGISTER	R/W
22_{16}	TIME STATUS/MAJOR TIME FIELD 0	R
24_{16}	MAJOR TIME FIELD 1	R
26_{16}	MAJOR TIME FIELD 2	R
28_{16}	MINOR TIME FIELD 1	R
$2A_{16}$	MINOR TIME FIELD 2	R
$2C_{16}$		
$2E_{16}$		
30_{16}		
32_{16}		
34_{16}		
36_{16}		
38_{16}		
$3A_{16}$		
$3C_{16}$		
$3E_{16}$		

3.2.2 MANUFACTURER'S ID REGISTER BITS (READ-ONLY):

Bit #	FUNCTION	TYPE
15 – 14	10_2 – MESSAGE-BASED DEVICE CLASS	R
13 – 12	11_2 – A16 ONLY ADDRESS SPACE	R
11 – 0	$EF4_{16}$ – DATUM MANUFACTURER'S ID	R

3.2.3 DEVICE TYPE REGISTER BITS (READ-ONLY):

Bit #	FUNCTION	TYPE
15 – 0	0824_{16} – bc824VXI VRFS MODEL CODE	R

3.2.4 STATUS/ CONTROL REGISTER BITS (READ/WRITE):

Bit #	FUNCTION	TYPE
15	A24 ENABLE/ACTIVE UNUSED (0)	R/W
14	MODID DRIVEN* (0 = MODID DRIVEN)	R
13 – 4	0 (UNUSED)	
3	READY (0 = CONFIG, 1= NORMAL OPERATION)	R
2	PASSED (0 = MODULE FAILED, 1= PASSED)	R
1	SYSFAIL INHIBIT (1 = INHIBIT SYSFAIL* DRIVER)	R/W
0	SOFT RESET (1 = SOFT RESET)	R/W

3.2.5 OFFSET REGISTER BITS (READ/WRITE):

Bit #	FUNCTION	TYPE
15 – 0	A24 ADDRESS UNUSED (0)	R

3.2.6 PROTOCOL REGISTER BITS (READ-ONLY):

Bit #	FUNCTION	TYPE
15	1 – CMDR* (SERVANT ONLY CAPABILITY)	R
14	1 – SIGNAL* (SIGNAL REGISTER NOT SUPPORTED)	R
13	1 – MASTER* (NO VXIbus MASTER CAPABILITY)	R
12	1 – INTERRUPTER (INTERRUPTER CAPABILITY)	R
11	1 – FHS* (FAST HANDSHAKE NOT SUPPORTED)	R
10	1 – SHRDMEM* (SHARED MEMORY NOT SUPPORTED)	R
9 – 4	1 (RESERVED)	
3 – 0	1 (UNUSED)	

3.2.7 RESPONSE REGISTER BITS (READ-ONLY):

Bit #	FUNCTION	TYPE
15	0 (UNUSED)	
14	1 (RESERVED)	
13	DOR (1 = DATA OUT READY FOR BYTE REQ. COMMAND)	R
12	DIR (1 = DATA IN READY FOR BYTE AVAIL. COMMAND)	R
11	ERR* (0 = ERROR IN WORD SERIAL PROTOCOL)	R
10	READ READY (1 = READY FOR VXI READ)	R
9	WRITE READY (1 = READY FOR VXI WRITE)	R
8	1 (FHS ACTIVE* NOT USED)	
7	1 (LOCKED* NOT USED)	
6 – 0	1 (UNUSED)	

3.2.8 DATA LOW REGISTER BITS (READ/WRITE):

Bit #	FUNCTION	TYPE
15 – 0	WORD-SERIAL MESSAGE TO/FROM DSP	R/W

3.2.9 LATCH TIME CONTROL REGISTER (READ/WRITE):

BIT #	FUNCTION	TYPE
15-0	0 (UNUSED)	A

Note: All read or writes of this register shall cause the time registers to latch current states.

3.2.10 TIME STATUS/MAJOR TIME FIELD 0 (READ-ONLY):

BIT #	FUNCTION	TYPE
BINARY MODE:		
15-7	0 (UNUSED)	
6	FREQUENCY OFFSET ERROR (1 = FREQ. OUT OF RANGE)	R
5	TIME OFFSET ERROR (1 = TIME OUT OF RANGE)	R
4	LOCKED* (0 = LOCKED TO REFERENCE)	R
3-0	0 (UNUSED)	
or DECIMAL MODE:		
15-7	0 (UNUSED)	
6	FREQUENCY OFFSET ERROR (1 = FREQ. OUT OF RANGE)	R
5	TIME OFFSET ERROR (1 = TIME OUT OF RANGE)	R
4	LOCKED* (0 = LOCKED TO REFERENCE)	R
3-0	DAYS (HUNDREDS)	R

3.2.11 MAJOR TIME FIELD 1 (READ-ONLY):

Bit #	FUNCTION	TYPE
BINARY MODE:		
15-0	MAJOR TIME (BINARY UNIX SECONDS) BITS 31-16	R
or DECIMAL MODE:		
15-12	DAYS (TENS)	R
11-8	DAYS (ONES)	R
7-4	HOURS (TENS)	R
3-0	HOURS (ONES)	R

3.2.12 MAJOR TIME FIELD 2 (READ-ONLY):

BIT #	FUNCTION	TYPE
BINARY MODE:		
15-0	MAJOR TIME (BINARY UNIX SECONDS) BITS 15-0	R
or DECIMAL MODE:		
15-12	MINUTES (TENS)	R
11-8	MINUTES (ONES)	R
7-4	SECONDS (TENS)	R
3-0	SECONDS (ONES)	R

3.2.13 MINOR TIME FIELD 1 (READ-ONLY):

Bit #	FUNCTION	TYPE
15-8	0 (UNUSED)	R
7-4	BINARY NANOSECONDS (100 ns RESOLUTION)	R
3-0	BINARY MICROSECONDS BITS 19-16	R

3.2.14 MINOR TIME FIELD 2 (READ-ONLY):

BIT #	FUNCTION	TYPE
15-0	BINARY MICROSECONDS BITS 15-0	R

3.3 TIME FORMATS

The VRFS major time registers (TIME0, EVENT0, MAJSTRB) support two time formats. One format is binary, as referenced in Table 3-2; the other, decimal, Table 3-3. The 32-bit binary format represents time as the number of seconds since midnight, January 1, 1970 UTC (Universal Time Coordinated, aka GMT), this is the standard time format found on most UNIX systems. The decimal time format is derived from the “struct tm” format also common on UNIX systems. Table 3-4 illustrates the differences between the standard “struct tm” fields and the VRFS implementation.

The binary time is represented with a 20 bit microsecond value plus a separate 4 bit, 100 nanosecond value. The binary microsecond counter counts up to 999999 (0xF423F) before it rolls or resets to 0.

Table 3-2 VRFS Binary Time Format

Bit #	15-12	11-8	7-4	3-0
TIME0 Field	Not Defined	Not Defined	Status (*Note 1*)	Unused
TIME1 Field	Major Time (Binary Seconds) Bits 31 – 16			
TIME2 Field	Major Time (Binary Seconds) Bits 15 – 0			
TIME3 Field	Not Defined	Not Defined	10E-7 Seconds (100 nsecs)	Binary µsecs Bits 19 – 16
TIME4 Field	Binary µsecs Bits 15 – 0			

Table 3-3 VRFS Decimal Time Format

Bit #	15-12	11-8	7-4	3-0
TIME0 Field	Not Defined	Not Defined	Status (*Note 1*)	Days Bits 11-8
TIME1 Field	Days Bits 7-0		Hours Bits 7-0	
TIME2 Field	Minutes Bits 7 - 0		Seconds Bits 7 - 0	
TIME3 Field	Not Defined	Not Defined	10E-7 Seconds (100 nsecs)	Binary µsecs Bits 19 – 16
TIME4 Field	Binary µsecs Bits 15 – 0			

***Note 1*:**
Bit 6 (the frequency offset) and Bit 5 (the time offset) are dependent on the input reference. As shown in the table below, if the bit is a 0, the frequency or time is less than the stated value, and if the bit is a 1, the frequency or time is greater than the stated value.

INPUT REFERENCE	FREQUENCY OFFSET	TIME OFFSET
10MHz Cal	$1E^{-10}$	50ns
1PPS	$1E^{-10}$	100ns
GPS	$5E^{-10}$	1us
IRIG AC	$5E^{-10}$	1us
IRIG DCLS	$5E^{-10}$	500ns

bit 4 1 = flywheeling (not tracking) 0 = tracking selected reference

Table 3-4 'struct tm' Field Comparison

struct tm Field	UNIX	VRFS
Tm_sec	Seconds (0 – 59)	Same
Tm_min	Minutes (0 - 59)	Same
Tm_hour	Hours (0 – 23)	Same
Tm_mday	Days of Month (1 - 31)	Not Implemented
Tm_mon	Month (0 – 11)	Not Implemented
Tm_year	Year – 1900	Implemented, 4 digits
Tm_wday	Day of Week (Sunday = 0)	Not Implemented
Tm_yday	Day of Year (0 - 365)	(1 to 366)
Tm_isdst	1 if DST in Effect	Not Implemented
Others	Time Zone Name, GMT Offset, Etc.	Implemented

3.4 FAULTS AND INDICATORS

The conditions and events of the VRFS include voltage faults and frequency events. Either faults or events can be enabled for reporting via queries and interrupts. Voltage faults include a short-circuit condition in any one of the eight coaxial outputs. The status of all eight outputs is reported in the voltage condition register. If any output is shorted, a voltage event can be latched and an interrupt generated if the appropriate voltage event enable registers are set. Also, if any output is shorted, the FAULT LED on the front panel is lit. Frequency events include the LPRO rubidium oscillator locking or unlocking, the OCXO locking or unlocking, the LPRO rubidium oscillator beginning or ending its tracking mode, or the option card alarm transitioning on or off. The status of these four events is reported in the frequency condition register. If any event transition occurs, a frequency event can be latched and an interrupt generated if the appropriate frequency event enable registers are set.

The VRFS has four front panel LED indicators. The LOCKED and TRACKING LEDs are discussed in detail in section 3.1.2. The FAULT LED is discussed in the previous paragraph. The final PWR LED provides an indication of the general state of the VRFS. All VXIbus mainframe voltages must be correct and the DSP firmware must be loaded and operating in order for the PWR LED to be lit. The LED functions are listed here again for completeness.

PWR: All VXIbus mainframe voltages are correct and DSP is functional.
FAULT: One or more of the coaxial outputs is short-circuited.
LOCKED: The OCXO loop that provides the VRFS 10 MHz outputs is locked.
TRACKING: The LPRO loop that disciplines the rubidium is tracking an external reference.

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CHAPTER FOUR
SOFTWARE INTERFACE

4.0 GENERAL

The Datum Inc model bc824VXI is a message-based VXIbus module that supports the protocols of a VXIbus Instrument and a VXIbus 488.2 Instrument. This indicates that the VRFS is compliant with the instrument specifications outlined in the VXI-1 Rev. 1.4 and IEEE Std 488.2-1992 specifications. In accordance with these specifications, the VRFS supports a number of levels of communication protocols including the low-level VXIbus commands, the IEEE 488.2 common commands, and the high-level VRFS-specific commands. This section describes all commands for the VRFS in detail. Following the command descriptions, the status and event data structures and reporting mechanisms are described. Figures 4-8a and 48b show the data structures for the status registers on the VRFS.

4.1 bc824VXI and bc827VXI LOW-LEVEL VXIbus COMMANDS

The VRFS is a message-based VXIbus instrument supporting the following low-level VXIbus commands. These commands are sent to the VRFS by reads and writes to its Data Low register using the VXIbus word-serial protocol. Each command is defined with a unique 16-bit value that is written to the Data Low register. These low-level commands are used by the VXIbus processor at its lowest level of data transfer protocol (transparent to most users). Most users need not concern themselves with these commands, which are listed here in bold type. More information on the low-level VXIbus commands and the word-serial protocol can be found in the VXI-1 Rev. 1.4 VXIbus specification.

BYTE AVAILABLE

Sends a byte of data to the VRFS.

BYTE REQUEST

Requests a byte of data from the VRFS.

ABORT NORMAL OPERATION

Causes VRFS to cease all operations immediately and enter its configuration state.

BEGIN NORMAL OPERATION

Notifies VRFS that it can begin normal operations and enter its normal-operation state.

END NORMAL OPERATION

Causes VRFS to cease all operations in an orderly fashion and enter its configuration state.

CLEAR

Clears the VXIbus interface and any pending operations on the VRFS.

ASYNCHRONOUS MODE CONTROL

Directs the path of events and responses on the VRFS.

CONTROL EVENT

Selectively enables the generation of events by the VRFS.

READ STB

Requests the reporting of the Status Byte from the VRFS.

READ PROTOCOL

Requests the reporting of protocols supported by the VRFS (EG, I, I4).

READ PROTOCOL ERROR

Requests the reporting of the current error state of the VRFS and resets all asserted errors.

ASSIGN INTERRUPTER LINE

Assigns a particular backplane IRQn* line to the VRFS for asserting interrupts.

READ INTERRUPTER LINE

Requests the reporting of the current IRQn* line assigned to the VRFS.

READ INTERRUPTERS

Requests the reporting of the number of interrupters within the VRFS (1).

4.2 bc824VXI and bc827VXI IEEE 488.2 COMMON COMMANDS

The VRFS is an IEEE 488.2 compliant VXIbus instrument. This indicates that the VRFS supports the data transfer and recognition of ASCII strings using the Byte Available and Byte Request low-level VXIbus commands. These ASCII strings correspond to commands and inquiries directed at the VRFS. In accordance with the IEEE 488.2 specification, the VRFS supports some common commands that are listed here. The listed commands are sent to the VRFS as the ASCII strings shown in bold type. More information on the IEEE 488.2 common commands can be found in the IEEE 488.2 specification.

***RST** Reset Command

Upon receiving the Reset Command, the VRFS clears the delay value to zero.

***IDN?** Identification Query

The Identification Query is used to identify unique devices over the system interface. The response contains four fields separated by commas in the form:
"Manufacturer, model number, serial number, firmware revision level."
For the VRFS, the response will be:
"Datum, Model 2084, Serial No. *nnn*, Version 2.00"

***OPC** Operation Complete Command

The Operation Complete Command causes the VRFS to generate an operation complete message in the Standard Event Status Register when all pending selected device operations have been finished.

***OPC?** Operation Complete Query

The Operation Complete Query causes the VRFS to place an ASCII character "1" into the device's Output Queue when all pending selected device operations have been finished.

***TST?** Self-Test Query

The Self-Test Query causes the VRFS to perform an internal self-test of its EEPROM, FLASH, and Static RAM. The response "Self Test Passed" will be returned if successful.

***CLS** Clear Status Command

The Clear Status Command clears all event registers on the VRFS and its Status Byte. This includes the Voltage Event Register, the Frequency Event Register, the Questionable Status Register, the Standard Event Status Register, and the Status Byte.

***WAI** Wait-to-Continue Command

The VRFS accepts the Wait-to-Continue Command but this command has no effect on the VRFS.

***STB?** Read Status Byte Query

The Read Status Byte Query returns the value of the Status Byte. Figure 4-1 shows the structure of the Status Byte. It includes the Questionable Summary bit to indicate frequency and voltage events, the Message Available bit to indicate messages available in the output queue, the Event Status bit to indicate command and execution errors, and the Master Summary bit that summarizes the other bits in the Status Byte.

***SRE** Service Request Enable Command

The Service Request Enable Command selects which bits in the Status Byte may cause service requests. This command is used to enable three events on the VRFS: the Questionable Summary bit, the Message Available bit, and the Event Status bit. Figure 4-1 shows the structure of the Status Byte.

***SRE?** Service Request Enable Query

The Service Request Enable Query returns the value of the Service Request Enable Register to indicate which service request events are enabled. Figure 4-1 shows the structure of the Status Byte.

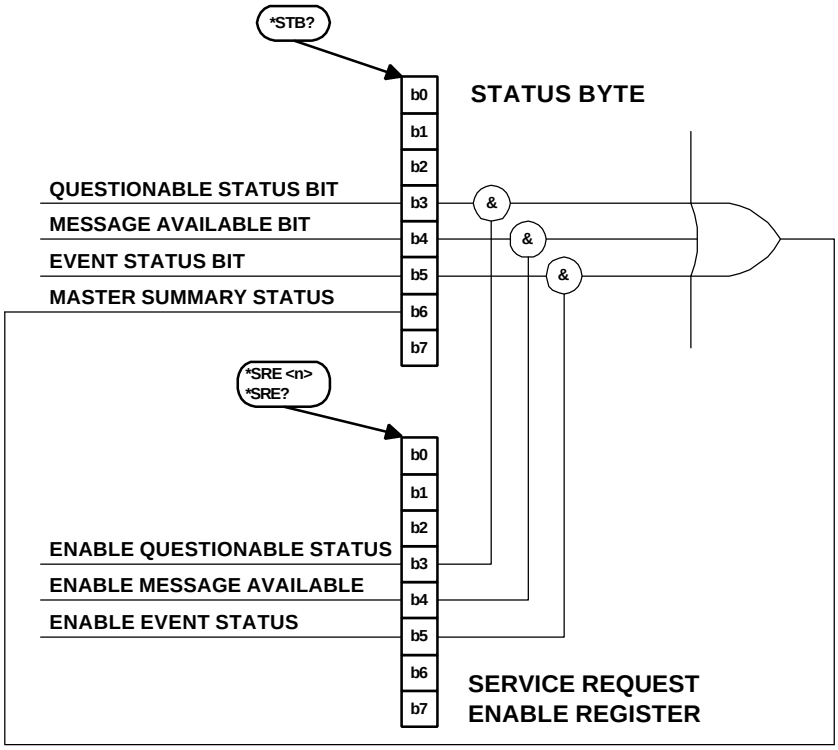

Figure 4-1. Status Byte and Service Request Enable Register

***ESR?** Standard Event Status Register Query

The Standard Event Status Register Query returns the current value of the Standard Event Status Register. This register is defined in IEEE Std 488.2-1992 and contains the following bits: the Operation Complete bit, the Request Control bit, the Query Error bit, the Device Dependent Error bit, the Execution Error bit, the Command Error bit, the User Request bit, and the Power On bit. Figure 4-2 shows the structure of the Standard Event Status Register.

***ESE** Standard Event Status Enable Command

The Standard Event Status Enable Command sets and clears bits in the Standard Event Status Enable Register to determine which standard events will be summarized in the Event Status bit. This command can be used to enable only two events on the VRFS: The Execution Error bit and the Command Error bit. Figure 4-2 shows the structure of the Standard Event Enable Register.

***ESE?** Standard Event Status Enable Query

The Standard Event Status Enable Query returns the value of the Standard Event Status Enable Register to indicate which standard events are enabled. Figure 4-2 shows the structure of the Standard Event Enable Register.

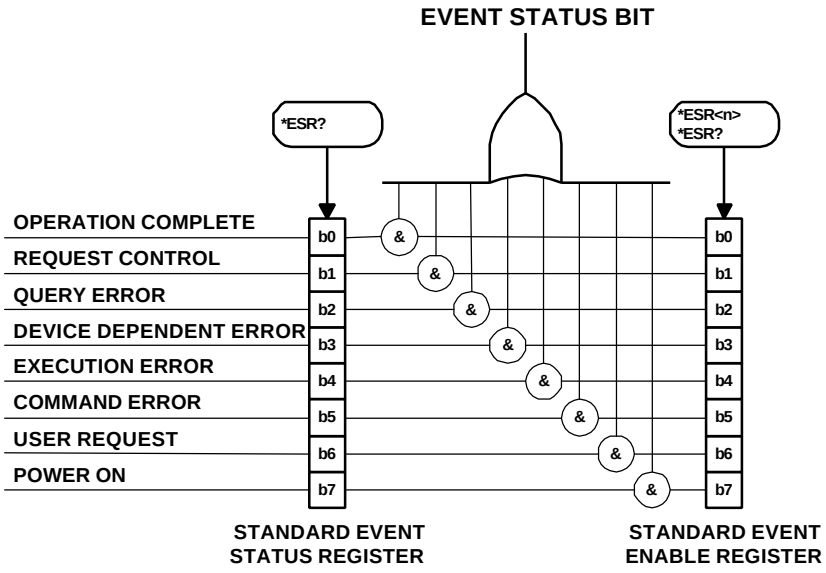

Figure 4-2. Standard Event Status and Standard Event Enable Registers

These IEEE 488 ASCII common commands are described in more detail in the IEEE Std 488.2-1992.

4.3 VRFS-SPECIFIC HIGH-LEVEL COMMANDS

The VRFS supports various high-level commands that are specific to its operation. These commands and inquiries are sent to the VRFS as ASCII strings in SCPI syntax using the Byte Available and Byte Request low-level VXIbus commands.

4.3.1 SCPI (Standard Commands for Programmable Instruments) CONFORMANCE INFORMATION

The VRFS complies to SCPI Version 1997.0.

4.3.2 bc824VXI STANDARD HIGH-LEVEL COMMANDS

The following SCPI commands are sent to the VRFS as the ASCII strings shown in bold type.

:STAT:PRES Preset Event Enable Command

This command clears the Standard Event Enable Register. It also sets all the bits in the following registers: Frequency Event Enable Register, Frequency Transition Filter Register, Questionable Event Enable Register, Service Request Enable Register, Voltage Event Enable Register, and VXI Event Enable Register. The preset values are:

Standard Event Enable Register	0_{16}
Frequency Event Enable Register	7_{16}
Frequency Transition Filter Register	3_{16}
Questionable Event Enable Register	221_{16}
Service Request Enable Register	0_{16}
Voltage Event Enable Register	FF_{16}
VXI Event Enable Register	F_{16}
Disciplining Event Enable Register	$3F_{16}$

:STAT:VERB? Verbose Status Query

The VRFS responds to this query with a long string having the form:

Datum, Model VRFS, Software Rev. 2.00,
Hardware Rev. C, Part No. bc824VXI
Rb Osc. [Locked | Unlocked],
Xtal. Adj. [Okay | Failed],
[All Outputs Okay | One or More Output Failed],
Output #1 [Pass | Fail],
Output #2 [Pass | Fail],
N
Output #8 [Pass | Fail]

:STAT:OPER? Operation Status Register Query
:STAT:OPER:EVEN?

Returns the contents of the Operation Status Register - an ASCII string representing a decimal number between 0 to 255 indicating bits set in the Operation Status Register.

:STAT:OPER:ENAB <bits to enable> Operation Event Enable Command

Enables the Operation Event Register.

:STAT:OPER:ENAB? Operation Event Enable Query

Returns the contents of the Operation Event Enable Register - an ASCII string representing a decimal number between 0 to 255 indicating bits set in the Operation Event Enable Register.

:STAT:OPER:COND? Operation Condition Query

Returns the contents of the Operation Condition Register - an ASCII string representing a decimal number between 0 to 255 indicating bits set in the Operation Condition Register.

:STAT:OPER:MAP <bit location, event number>
Remap Operational Status Register

Maps an error from the list of possible events the VFRS can generate into a specified bit in the Questionable Register.
An ASCII string containing the specified bit location (0 to 15) in the Questionable Register to map the event followed by the event number to remap, separated by a comma. The following are the valid event numbers with their corresponding events and bit numbers:

EVENT NUMBER	EVENT	EVENT BIT LOCATION
200	calibrating	bit0
201	settling	bit1
202	ranging	bit2
203	sweeping	bit3
204	measuring	bit4
205	waiting for trigger summary	bit5
206	waiting for arm summary	bit6
207	correcting	bit7
213	instrument summary	bit13
214	program running	bit14
208:	not defined	
209:	not defined	
210:	not defined	
211:	not defined	
212:	not defined	
215:	not defined	

:STAT:QUES? or
:STAT:QUES:EVEN? Questionable Status Register Query

The VRFS responds to this query with the value of the Questionable Status Register. Figure 4-3 shows the structure of the Questionable Status Register, which contains the Frequency Summary bit (bit 4) to indicate a frequency event, and the Voltage Summary bit (bit 0) to indicate a voltage event. All bits in the Questionable Status Register are cleared by this query.

:STAT:QUES:ENAB <bits to enable> Questionable Event Enable Command

This command sets and clears bits in the Questionable Event Enable Register. Figure 4-3 shows the structure of the Questionable Event Enable Register, which contains the mask bits that enable Questionable Status events to propagate further in the Questionable Summary Bit.

:STAT:QUES:ENAB? Questionable Event Enable Query

The VRFS responds to this query with the value of the Questionable Event Enable Register. The response indicates which Questionable Status events are enabled to propagate further in the Questionable Summary Bit. Figure 4-3 shows the structure of the Questionable Event Enable Register.

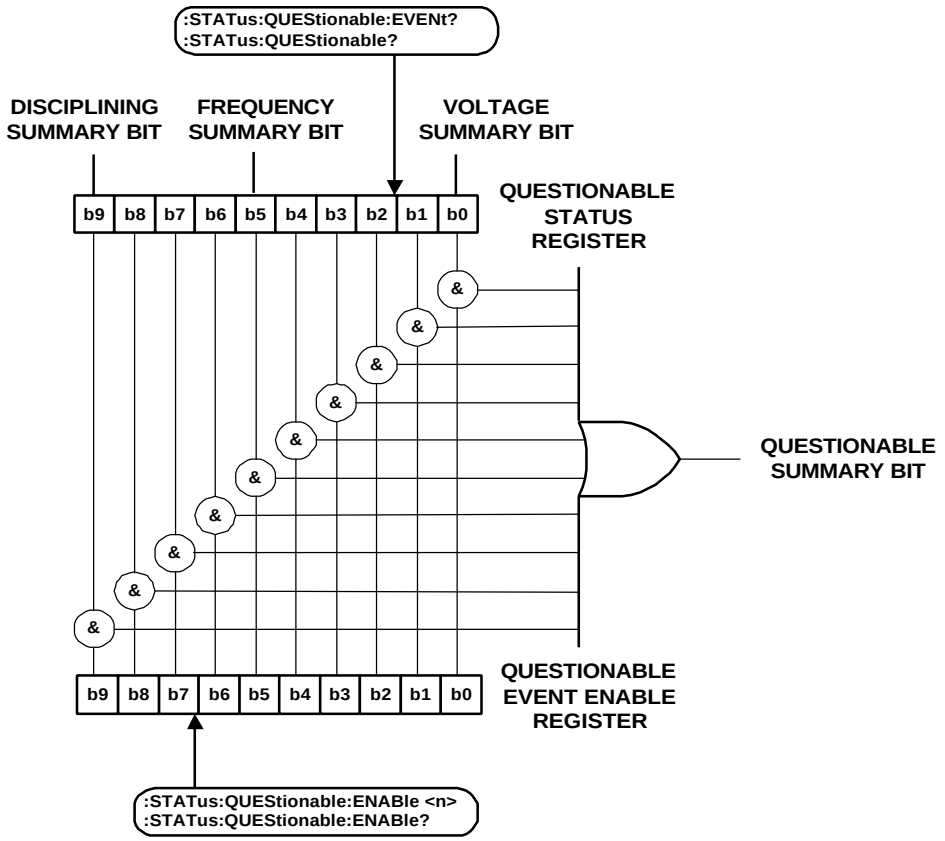

Figure 4-3. Questionable Status and Questionable Event Enable Registers

:STAT:QUES:COND? Questionable Condition Query

Returns the contents of the Questionable Condition Register - an ASCII string representing a decimal number between 0 to 255 indicating bits set in the Questionable Condition Register.

:STAT:QUES:MAP <bit location, event number>

Remap Questionable Status Register

Maps an error from the list of possible events the VFRS can generate into a specified bit in the Operation Register.
An ASCII string containing the specified bit location (0 to 15) in the Operation register to map the event followed by the event number to remap, separated by a comma.
The following are the valid event numbers with their corresponding events and bit numbers:

EVENT NUMBER	EVENT	EVENT BIT LOCATION
100	voltage	bit0
101	current	bit1
102	time	bit2
103	power	bit3
104	temperature	bit4
105	frequency	bit5
106	phase	bit6
107	modulation	bit7
108	calibration	bit8
109	disciplining	bit9
113	instrument summary	bit13
114	command warning	bit14
115	not used	
110	not defined	
111	not defined	
112	not defined	

:STAT:QUES:VOLT:COND? Voltage Condition Register Query

The VRFS responds to this query with the value of the Voltage Condition Register. Figure 4-4 shows the structure of the Voltage Condition Register, which contains eight bits to indicate the current conditions of the eight front-panel outputs. Short-circuit faults appear as set bits.

:STAT:QUES:VOLT? or Voltage Event Register Query
:STAT:QUES:VOLT:EVEN?

The VRFS responds to this query with the value of the Voltage Event Register. Figure 4-4 shows the structure of the Voltage Event Register, which contains eight bits to indicate latched voltage events. Voltage events correspond to short-circuit faults on one or more of the eight front-panel outputs. All bits in the Voltage Event Register are cleared by this query.

:STAT:QUES:VOLT:ENAB <bits to enable> Voltage Event Enable Command

This command sets and clears bits in Voltage Event Enable Register. Figure 4-4 shows the structure of the Voltage Event Enable Register, which contains the mask bits that enable Voltage events to propagate further in the Voltage Summary Bit.

:STAT:QUES:VOLT:ENAB? Voltage Event Enable Query

The VRFS responds to this query with the value of the Voltage Event Enable Register. The response indicates which Voltage events are enabled to propagate further in the Voltage Summary Bit. Figure 4-4 shows the structure of the Voltage Event Enable Register.

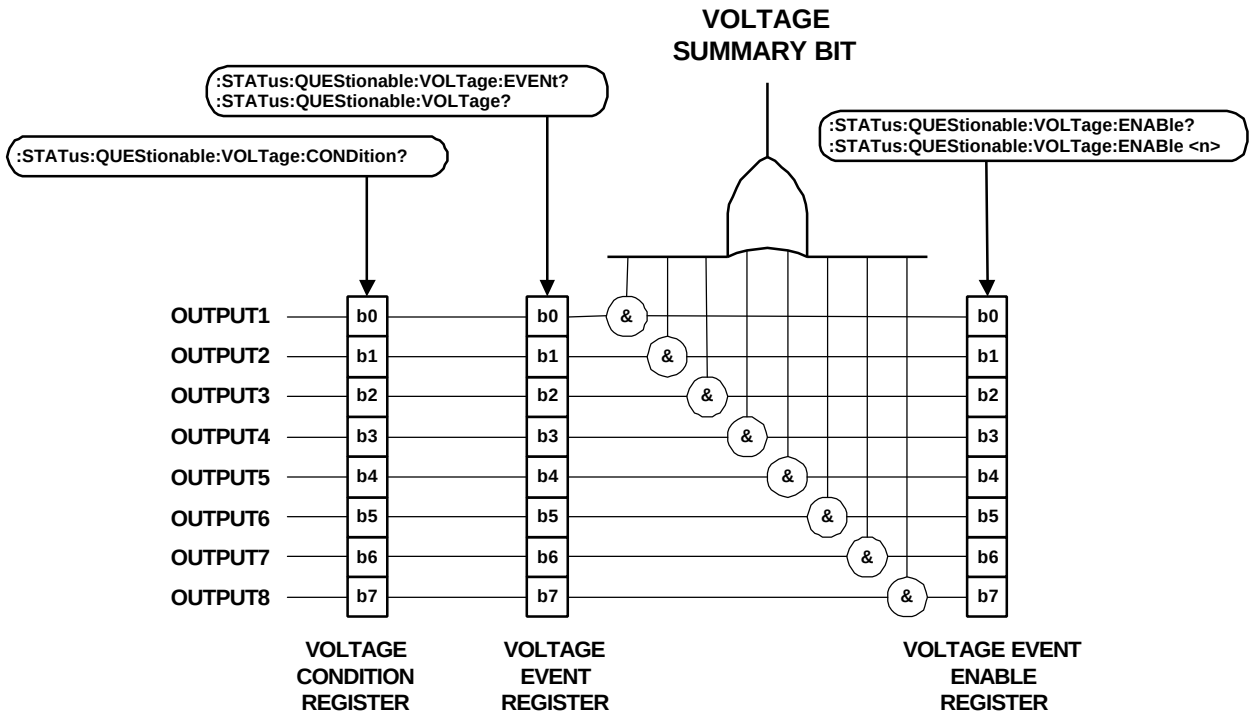

Figure 4-4. Voltage Condition, Voltage Event, and Voltage Event Enable Registers

:STAT:QUES:FREQ:COND? Frequency Condition Register Query

The VRFS responds to this query with the value of the Frequency Condition Register. Figure 4-5 shows the structure of the Frequency Condition Register, which contains two bits to indicate the current status conditions of the crystal adjust and rubidium lock. A crystal requiring adjustment or an unlocked rubidium appear as set bits.

:STAT:QUES:FREQ:PTR <bits to enable> Freq. Positive Transition Filter Command

This command sets and clears the positive transition bit in the Frequency Transition Filter that enables a rubidium lock event. Figure 4-5 shows the structure of the Frequency Transition Filter, which contains the two mask bits to enable positive and negative transition events for the rubidium lock status. Enabled transitions propagate further into the Frequency Event Register.

:STAT:QUES:FREQ:PTR? Freq. Positive Transition Filter Query

The VRFS responds to this query with the value of the positive transition bit in the Frequency Transition Filter. The response indicates whether a rubidium lock event is enabled to propagate further into the Frequency Event Register. Figure 4-5 shows the structure of the Frequency Transition Filter.

:STAT:QUES:FREQ:NTR <bits to enable> Freq. Negative Transition Filter Command

This command sets and clears the negative transition bit in the Frequency Transition Filter that enables a rubidium unlock event. Figure 4-5 shows the structure of the Frequency Transition Filter, which contains the two mask bits to enable positive and negative transition events for the rubidium lock status. Enabled transitions propagate further into the Frequency Event Register.

:STAT:QUES:FREQ:NTR? Freq. Negative Transition Filter Query

The VRFS responds to this query with the value of the negative transition bit in the Frequency Transition Filter. The response indicates whether a rubidium unlock event is enabled to propagate further into the Frequency Event Register. Figure 4-5 shows the structure of the Frequency Transition Filter.

:STAT:QUES:FREQ? or
:STAT:QUES:FREQ:EVEN? Frequency Event Register Query

The VRFS responds to this query with the value of Frequency Event Register. Figure 4-5 shows the structure of the Frequency Event Register, which contains three bits to indicate crystal adjust, rubidium lock, and rubidium unlock events. All bits in the Frequency Event Register are cleared by this query.

:STAT:QUES:FREQ:ENAB <bits to enable> Frequency Event Enable Command

This command sets and clears bits in Frequency Event Enable Register. Figure 4-5 shows the structure of the Frequency Event Enable Register, which contains the mask bits that enable Frequency events to propagate further in the Frequency Summary Bit.

:STAT:QUES:FREQ:ENAB? Frequency Event Enable Query

The VRFS responds to this query with the value of the Frequency Event Enable Register. The response indicates which Frequency events are enabled to propagate further in the Frequency Summary Bit. Figure 4-5 shows the structure of the Frequency Event Enable Register.

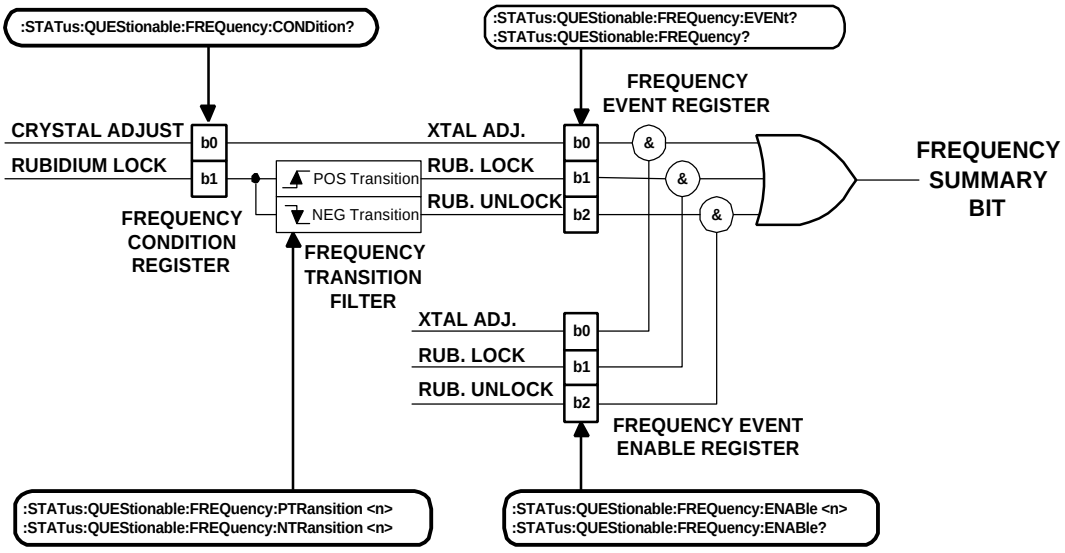

Figure 4-5. Frequency Condition, Frequency Transition Filter, Frequency Event, and Frequency Event Enable Registers

:STAT:QUES:DISC? or Disciplining Cond. Event Reg. Query
:STAT:QUES:DISC:EVEN?

Returns the contents of the Disciplining Event Register - an ASCII string representing a decimal number between 0 to 255 indicating bits set in the Disciplining Event Register. See Figure 4-6.

:STAT:QUES:DISC:COND? Disciplining Condition Register Query

Returns the contents of the Disciplining Condition Register - an ASCII string representing a decimal number between 0 to 255 indicating bits set in the Disciplining Condition Register. See Figure 4-6.

:STAT:QUES:DISC:ENAB <bits to enable> Set Disciplining Condition Enable Register

Sets the Disciplining Event Enable Register.

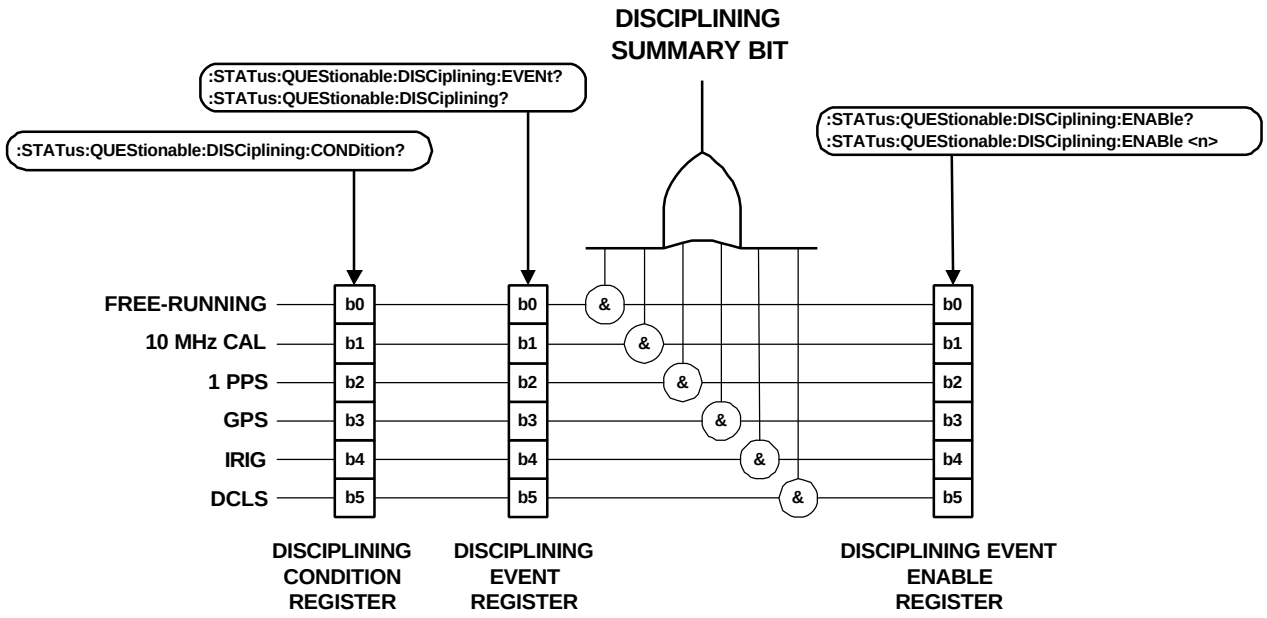

Figure 4-6. Disciplining Condition,
Disciplining Event, and Disciplining Event Enable Registers

:STAT:QUES:DISC:ENAB? Disciplining Event Enable Register Query

Returns the contents of the Disciplining Event Enable Register - an ASCII string representing a decimal number between 0 to 255 indicating bits set in the Disciplining Event Enable Register. See Figure 4-6.

:SYST:EXP:SNUM <serial number> Set Serial Number Command

Sets the VRFS module serial number – an ASCII string representing a decimal number between 0 and 65535.

:SYST:EXP:SNUM? Set Serial Number Query

Returns the VRFS module serial number – an ASCII string representing a decimal number between 0 and 65535.

:SYST:EXP:EEPR:UNPR Unprotect EEPROM

Unprotect the protected locations in the EEPROM.

:SYST:EXP:BOOT <code> Enter Bootloader mode

Places the VRFS into the bootloader mode. When the decimal number 5 is entered, the parameter will be loaded into the bootloader code register to be checked by the bootloader code to ensure the module is in the bootloader mode.

:SYST:VERS? Query System SCPI Version

Returns the SCPI version number for which the instrument complies. The response shall have the form YYYY.V where the Ys represent the year-version (i.e. 1999) and the V represents an approved version number for that year.

:SOUR:TIME:MODE <IRIG/FRUN/PPS/GPS/CAL>
Select VRFS Timing Mode

Sets the VRFS timing mode. An ASCII string representing the timing mode.
IRIG – IRIG A or IRIG B (AM or DCLS)
FRUN – Free Running (Internal 10 MHz selected)
PPS – 1 PPS – External 1PPS input
GPS – GPS
EXT – External 10 MHz

:SOUR:TIME:MODE? Query VRFS Timing Mode

Returns the current VRFS timing mode. An ASCII string representing the current timing mode.
IRIG – IRIG A or IRIG B (AM or DCLS)
FRUN – Free Running (Internal 10 MHz selected)
PPS – 1 PPS – External 1PPS input
GPS – GPS
EXT – External 10 MHz

:SOUR:TIME:FORM <BIN/DEC> Set Time Register Format

Sets the time register format for the A16 timing registers. An ASCII string representing the time mode.
BIN – Binary format
DEC –Decimal format

:SOUR:TIME:FORM? Query Time Register Format

Returns the current time register format for the A16 timing registers. An ASCII string representing the time mode.

BIN – Binary format
DEC –Decimal format

:SOUR:TIME:BIN <seconds> Set Major Time – Binary

Sets the major time on the VRFS in binary format. An ASCII string containing the major time in seconds.

:SOUR:TIME:BIN? Query Time – Binary

Returns the major and minor time in binary format. An ASCII string containing major time followed by minor time separated by a comma.

:SOUR:TIME:DEC <days, hours, minutes, seconds>
Set Major Time – Decimal

Sets the days, hours, minutes, and seconds into the VRFS in decimal format. An ASCII string containing the days, hours, minutes, and seconds respectively, separated by commas.

:SOUR:TIME:DEC? Query Time – Decimal

Returns the days, hours, minutes, seconds, and milliseconds of the VRFS in decimal format. An ASCII string containing the days, hours, minutes, seconds, and milliseconds respectively, separated by commas.

:SOUR:TIME:YEAR <year> Set Year

Sets the year into the VRFS. An ASCII string containing the current year.

:SOUR:TIME:YEAR? Query Year

Returns the year from the VRFS. An ASCII string containing the current year.

:SOUR:TIME:MAJ:BIN? Query Major Time – Binary

Returns the current seconds from the VRFS in binary format. An ASCII string containing the total binary seconds.

:SOUR:TIME:MAJ:DEC? Query Major Time – Binary

Returns the days, hours, minutes, and seconds of the VRFS in decimal format. An ASCII string containing the days, hours, minutes, and seconds, respectively, separated by commas.

:SOUR:TIME:MIN? Query Minor Time

Returns the milliseconds and nanoseconds of the VRFS in binary format. An ASCII string containing the milliseconds and nanoseconds, respectively, separated by commas.

:SOUR:TIME:PER:FREQ <frequency> Set Periodic Output Frequency

Sets the Periodic Output frequency of the VRFS – An ASCII string containing the output frequency (in Hz).

:SOUR:TIME:PER:FREQ? Query Periodic Output Frequency

Returns the current Periodic Output frequency of the VRFS – An ASCII string containing the output frequency (in Hz).

:SOUR:TIME:PER:PWID <pulse width> Set Periodic Output Pulse Width

Sets the Periodic Output pulse width of the VRFS – An ASCII string containing the pulse width (in nanoseconds).

:SOUR:TIME:PER:PWID? Query Periodic Output Pulse Width

Returns the current Periodic Output pulse width of the VRFS – An ASCII string containing the pulse width (in nanoseconds).

:SOUR:TIME:PER <ON/OFF> Periodic Output – Enable/Disable

Enables/disables the periodic output. An ASCII string ‘on’ to enable or ‘off’ to disable the periodic output.

:SOUR:TIME:PER? Query Periodic Output Condition

Returns the state (condition) of the periodic output. An ASCII string ‘on’ to indicate the periodic output is enabled or ‘off’ indicating it is disabled.

:SOUR:TIME:STR:FORM <BIN/DEC> Set Strobe Format

Sets the strobe output format. The ASCII string 'BIN' to put the strobe output in binary major and minor time mode or 'DEC' indicating it will output both the major and minor decimal time.

:SOUR:TIME:STR:FORM? Query Strobe Format

Returns the format of the strobe output. The ASCII string 'BIN' indicating the strobe output is in binary minor time mode or 'DEC' indicating it is in decimal major and minor time mode.

:SOUR:TIME:STR:MODE <MIN/MAJ> Set Strobe Mode

Sets the strobe output mode. The ASCII string 'min' to indicate the strobe output is in minor time mode or 'maj' indicating it will use both the major and minor time.

:SOUR:TIME:STR:MODE? Query Strobe Mode

Returns the mode of the strobe output. The ASCII string 'min' indicating the strobe output is in minor time mode or 'maj' indicating it is in major time mode.

:SOUR:TIME:STR:PAR <hr, min, sec, usec> *(decimal format)* or
:SOUR:TIME:STR:PAR < sec, usec> *(binary format)* Set Strobe Parameters

Sets the strobe output parameters. ASCII strings containing the hour, minute, second, and microsecond, respectively, separated by commas. If the strobe output is in minor format, the hour, minute, and second parameters are dropped.

:SOUR:TIME:STR:PAR? Query Strobe Parameters

Returns the strobe output parameters. ASCII strings containing the hour, minute, second, and microsecond, respectively, separated by commas. If the strobe output is in minor format, the hour and minute parameters are dropped.

:SOUR:TIME:STR <ON/OFF> Strobe – Enable/Disable

Enables/disables the strobe output. The ASCII string 'on' to enable or 'off' to disable the strobe output.

:SOUR:TIME:STR? Query Strobe Output Condition

Returns the state of the strobe output. The ASCII string ‘on’ to indicate the strobe output is enabled or ‘off’ indicating it is disabled.

:SOUR:TIME:IRIG:IN:MOD <SINE/DCLS> Select IRIG Input Time Code Modulation Type

Selects the time code modulation type. The ASCII string ‘SINE’ to indicate sinusoidal modulation or ‘DCLS’ indicating dc level shift modulation.

:SOUR:TIME:IRIG:IN:MOD? Query IRIG Input Time Code Modulation Type

Returns the time code modulation type. The ASCII string ‘SINE’ to indicate sinusoidal modulation or ‘DCLS’ indicating dc level shift modulation.

:SOUR:TIME:IRIG:OUT <ON/OFF> Turn IRIG Output – On/Off

Enables/disables the IRIG output encoding functionality. The ASCII string ‘on’ to indicate the IRIG output encoding functionality is enabled or ‘off’ indicating it is disabled.

:SOUR:TIME:IRIG:OUT? Query IRIG Output

Returns the state of the IRIG output encoding. The ASCII string ‘on’ to indicate the IRIG output encoding functionality is enabled or ‘off’ indicating it is disabled.

:SOUR:TIME:IRIG:OUT:GAIN <0-100> Set IRIG Out Gain

Sets the IRIG output waveform gain (amplitude). An ASCII string representing a decimal number between 0 and 100 (in percent).

:SOUR:TIME:IRIG:OUT:GAIN? Query IRIG Out Gain

Returns the gain (amplitude) of the IRIG output. An ASCII string representing a decimal number between 0 and 100 (in percent).

:SOUR:TIME:IRIG:OUT:RAT <3/6> Set IRIG Out Ratio

Sets the IRIG output waveform ratio (the ratio of the “mark” amplitude to the “space” amplitude). The ASCII string ‘6’ to indicate a 6:1 ratio or ‘3’ to indicate a 3:1 ratio.

:SOUR:TIME:IRIG:OUT:RAT? Query IRIG Out Ratio

Returns the IRIG output waveform ratio. The ASCII string ‘6’ to indicate a 6:1 ratio or ‘3’ to indicate a 3:1 ratio.

:SOUR:TIME:CAL <EVEN1/EVEN2/OCXO/TREF>
Calibrate Capture Inputs

Calibrates the specified input. An ASCII string representing the calibration input.
EVEN1 – event 1 capture input
EVEN2 – event 2 capture input
OXCO – ocxo capture input
TREF – time reference capture input

:SOUR:TIME:EVEN1 <SING/CONT/OFF>
Event 1 Capture – Single/Continuous/Off

Enables or disables the event 1 capture input and sets the event capture mode. The ASCII string ‘SING’ to enable the capture in single shot mode or ‘CONT’ to enable the capture in continuous mode. The ASCII string ‘OFF’ to disable the capture.

:SOUR:TIME:EVEN1? Query Event 1

Returns the event 1 capture input mode. The ASCII string ‘SING’ if the capture is enabled in single shot mode or ‘CONT’ if the capture is enabled in continuous mode. The ASCII string ‘OFF’ if the capture is disabled.

:SOUR:TIME:EVEN1:EDGE <RISE/FALL> Event 1 Capture Edge

Sets the capture event edge. The ASCII string ‘RISE’ to indicate rising edge capture or ‘FALL’ indicating falling edge capture.

:SOUR:TIME:EVEN1:EDGE? Query Event 1 Capture Edge

Returns the edge the capture event is set to. The ASCII string ‘RISE’ to indicate rising edge capture or ‘FALL’ indicating falling edge capture.

:SOUR:TIME:EVEN1:FIFO? Read Event 1 Capture FIFO

Returns an element of the event 1 capture fifo. An ASCII string representing a decimal number, which is the time the event was captured followed by a ‘1’ for rising edge or a ‘0’ for falling edge.

:SOUR:TIME:EVEN1:FIFO:STAT? Query Event 1 Capture FIFO Status

Returns the number of elements in the event 1 capture fifo. An ASCII string representing a decimal number, which is the number of elements in the event capture fifo. If the fifo has an overflow condition, the response will be "OVERFLOW".

:SOUR:TIME:EVEN2 <SING/CONT/OFF>
Event 2 Capture – Single/Continuous/Off

Enables or disables the event 2 capture input and sets the event capture mode. The ASCII string 'SING' to enable the capture in single shot mode or 'CONT' to enable the capture in continuous mode. The ASCII string 'OFF' to disable the capture.

:SOUR:TIME:EVEN2? Query Event 2

Returns the event 2 capture input mode. The ASCII string 'SING' if the capture is enabled in single shot mode or 'CONT' if the capture is enabled in continuous mode. The ASCII string 'OFF' if the capture is disabled.

:SOUR:TIME:EVEN2:EDGE <RISE/FALL> Event 2 Capture Edge

Sets the capture event edge. The ASCII string 'RISE' to indicate rising edge capture or 'FALL' indicating falling edge capture.

:SOUR:TIME:EVEN2:EDGE? Query Event 2 Capture Edge

Returns the edge the capture event is set to. The ASCII string 'RISE' to indicate rising edge capture or 'FALL' indicating falling edge capture.

:SOUR:TIME:EVEN2:FIFO? Read Event 2 Capture FIFO

Returns an element of the event 2 capture fifo. An ASCII string representing a decimal number, which is the time the event was captured followed by a '1' for rising edge or a '0' for falling edge.

:SOUR:TIME:EVEN2:FIFO:STAT? Query Event 2 Capture FIFO Status

Returns the number of elements in the event 2 capture fifo. An ASCII string representing a decimal number, which is the number of elements in the event capture fifo. If the fifo has an overflow condition, the response will be "OVERFLOW".

:SOUR:TIME:PDC <DELAY> Set the Propagation Delay Constant

Sets the propagation delay constant. An ASCII string representing a decimal number corresponding to the propagation delay in nanoseconds. The range is from 1 nanosecond to 1 millisecond.

:SOUR:TIME:PDC? Query the Propagation Delay Constant

Queries the propagation delay constant. An ASCII string representing a decimal number corresponding to the propagation delay in nanoseconds.

:SOUR:TIME:LTOF <hour,min> Set the Local Time Offset

Sets the local time offset. ASCII strings representing decimal numbers corresponding to the local time offset. The hours will be followed by the minutes separated by a comma. The hour parameter can range from –12 to 12 and the minute parameter must be either 0 or 30.

:SOUR:TIME:LTOF? Query the Local Time Offset

Queries the local time offset. ASCII strings representing decimal numbers corresponding to the local time offset. The hours will be followed by the minutes separated by a comma.

:SOUR:OSC:DISC:GAIN <gain> Set LPRO Oscillator Disciplining Gain

Sets the VRFS clock disciplining control loop gain. An ASCII string representing a decimal number between 0 and 65535.

:SOUR:OSC:DISC:GAIN? Query LPRO Oscillator Disciplining Gain

Returns the VRFS clock disciplining control loop gain. An ASCII string representing a decimal number between 0 and 65535.

:SOUR:OSC:DISC:DAC <gain value> Set LPRO Oscillator Control DAC

Sets the VRFS LPRO clock DAC (Digital to Analog Converter) value. An ASCII string representing a decimal number between 0 and 65535.

:SOUR:OSC:DISC:DAC? Query LPRO Oscillator Control DAC

Returns the VRFS LPRO clock DAC (Digital to Analog Converter) value. An ASCII string representing a decimal number between 0 and 65535.

:SOUR:OSC:DISC:PWM <pwm value> Set LPRO Oscillator Control PWM

Sets the VRFS LPRO clock PWM (Pulse Width Modulation) value. An ASCII string representing a decimal number between 0 and 19999.

:SOUR:OSC:DISC:PWM? Query LPRO Oscillator Control PWM

Returns the VRFS LPRO clock PWM (Pulse Width Modulation) value. An ASCII string representing a decimal number between 0 and 19999.

:SOUR:OSC:DISC:CAL? Query LPRO Oscillator Calibration Status

Returns the VRFS LPRO calibration status indicating whether the VRFS has achieved and stored a valid calibration state by tracking an external calibration source. The ASCII string YES or NO is returned.

4.3.3 bc827VXI GPS STANDARD HIGH-LEVEL COMMANDS

The following commands are applicable to a VRFS furnished with a internal GPS Receiver Module:

:SOUR:GPS:LAT <latitude> Set Position - Latitude

Allows the user to manually enter the position (in degrees of latitude) of the antenna/preamp.
Parameters: [none|-]aa,bb,cc,d
Notes: aa: in degrees, bb: in minutes, cc: in seconds, d: in tenth seconds
none = no input, North, - = negative, South

The new position will be written into the EEPROM, but it won't be used until the unit's power is recycled.

:SOUR:GPS:LON <longitude> Set Position - Longitude

Allows the user to manually enter the position (in degrees of longitude) of the antenna/preamp.
Parameters: [none|-]aaa,bb,cc,d
Notes: aaa: in degrees, bb: in minutes, cc: in seconds, d: in tenth seconds
none = no input, East, - = negative, West

The new position will be written into the EEPROM, but it won't be used until the unit's power is recycled.

:SOUR:GPS:ALT <altitude> Set Position - Altitude

Allows the user to manually enter the position (in meters of altitude) of the antenna/preamp.
Parameters: [none|-]eeeeeee
Notes: eeeeeee: in centimeters (-100,000 to +1,800,000 meters)
none = no input, positive, - = negative

The new position will be written into the EEPROM, but it won't be used until the unit's power is recycled.

:SOUR:GPS:LAT? Request Position – Latitude

Allows the user to request the position (in degrees of latitude) of the antenna/preamp.
Response: aa bb cc.d[N|S]
Notes: aa: in degrees, bb: in minutes, cc: in seconds, d: in tenth seconds
N = North, S = South

:SOUR:GPS:LON? Request Position – Longitude

Allows the user to request the position (in degrees of longitude) of the antenna/preamp.
Response: aa bb cc.d[E|W]
Notes: aa: in degrees, bb: in minutes, cc: in seconds, d: in tenth seconds
E = East, W = West

:SOUR:GPS:POS? Request Position – Altitude

Allows the user to request the position (in meters of altitude) of the antenna/preamp.
Response: [none|-]eeeeeee
Notes: eeeeeee: in meters (-100,000 to +1,800,000 meters)
none = no input, positive, - = negative

:SOUR:GPS:CDEL <feet> Set GPS Cable Delay

This command allows the user to enter a cable delay that compensates for the propagation delay between the antenna/preamp and the VRFS caused by the cable. The delay is approximately 1.5 nanoseconds per foot of antenna cable. The user simply enters the total length of antenna cable as a four digit number expressed in feet.
Parameter: xxxx (in feet)

:SOUR:GPS:CDEL? Request GPS Cable Delay

This command allows the user to interrogate the GPS Receiver Module and find out what cable delay the unit is currently using.
Response: xxxx

:SOUR:GPS:PHM <0/1/2> Set Auto/Stationary/Dynamic Mode

This command allows the user to select either the Auto mode, the Stationary mode, or the Dynamic mode.

Auto Mode: In the Auto mode, the GPS Receiver Module will automatically find its position (i.e. that of the antenna). It will take the average of 200 position fixes, and then switch to the Stationary Mode.

Stationary Mode: In the Stationary mode, the position won't change. This single satellite mode is the most frequently used mode of operation for timing applications. This mode of operation assumes that the current position (longitude, latitude, and altitude) is accurate. It uses either a single, specific satellite to derive the timing information or an averaged solution of the time information from as many satellites as the receiver is tracking.

Dynamic Mode: This mode is used if the unit's position is changing. It will continuously reacquire its position.

The mode is stored in memory so that when power is removed and then turned back on again, the unit returns to the last operating mode. The mode change will take place after the unit's power is recycled.
Parameter: 0 (AUTO mode)
1 (STATIONARY mode)
2 (DYNAMIC mode)

:SOUR:GPS:PHM? Request Auto/Stationary/Dynamic Mode

This command allows the user to request the operating mode of the GPS Receiver Module.
Response: [0/1/2] i.e. 0 = Auto mode, 1 = Stationary mode, and 2=Dynamic mode.

:SOUR:GPS:SMAN <degrees> Set Satellite Angle Mask

The GPS Receiver Module will attempt to track satellites for which the elevation angle is greater than the satellite mask angle. This parameter allows the user to control the elevation angle that was used for this decision.
Parameter: xx (0 to 89 degrees)

:SOUR:GPS:SMAN? Request Satellite Angle Mask

This command allows the user to request the current satellite angle mask that the GPS Receiver Module is using.

:SOUR:GPS:POFF <ns> Set GPS 1PPS Offset

The GPS Receiver outputs a one pulse-per-second (1PPS) signal with the rising edge placed on top of the GPS/UTC one second tic mark. The 1PPS Offset command allows the user to offset the 1PPS time mark in one nanosecond increments. This offset can be used to place the 1PPS output from the VRFS anywhere within the one second epoch.
Parameter: xxxxxxxxx (in nanoseconds)

:SOUR:GPS:POFF? Request GPS 1PPS Offset

This command allows the user to request the current 1PPS offset used by the GPS Receiver Module.
Response: xxxxxxxxx (in nanoseconds)

:SOUR:GPS:LSEC? Request Pending Leap Seconds

Leap seconds are occasionally inserted in the UTC (Universal Time Coordinated) and generally occur on midnight UTC June 30 or midnight UTC December 31. This command causes the receiver to send a message to the user indicating the status of any pending leap second correction to UTC due at the end of the current month. If a leap second is pending, its direction is also indicated.
When a Leap Second is inserted, the Time of Day (TOD) will show a value of 60 in the seconds field. When a Leap Second is removed, the date will roll over at 58 seconds.
Response: xx, pending [NO|+1|-1]

:SOUR:GPS:RST? Request GPS Receiver Status

This request allows the user to receive the GPS Receiver Module status.
Response: antenna: [OK|UC|OC], receiver: xxx
Description:

Antenna:	OK	Normal operation.
	UC	Under current (possibly an open connection).
	OC	Over current (possibly a shorted antenna or cable).
Receiver:	xxx	This is a decimal number that represents the GPS receiver status code. It first needs to be converted into 8 binary bits, and then each binary bit has a specific definition as shown below:

BIT #	DEFINITION
Bit 7	GPS Receiver Failure
Bit 6	Poor Geometry
Bit 5	3D Fix
Bit 4	2D Fix
Bit 3	Acq. Satellites/Position Hold
Bit 2	GPS Time Acquired
Bit 1	Insufficient Satellites
Bit 0	Bad Almanac

Example:

The GPS Receiver Status Code (decimal number) is 12. The following is the 8 bit binary number:

Binary Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Weight	128	64	32	16	8	4	2	1
Value	0	0	0	0	1	1	0	0

In the above example, Bits 2 and 3 are true which means that the GPS Receiver Status is: Acq. Satellites/Position Hold and GPS Time Acquired

:SOUR:GPS:SST? Request Satellite Status

This request allows the user to receive the status of the current visible satellites including:
Number of visible satellites.
Each satellite's PRN number. (The unique number of the NAVSTAR satellite).
The carrier to noise density ratio of each satellite.

Response: tracked xx, #aa, bbb, #aa, bbb, #aa, bbb, #aa, bbb, #aa, bbb, #aa, bbb, #aa, bbb, #aa, bbb

Notes: xx: no. of satellites, #aa : satellite PRN number, bbb: carrier to noise density ratio in dB-Hz.

4.4 INTERRUPT EVENTS

The VRFS can generate interrupts that are sent to the VXIbus commander in response to voltage events, frequency events, and disciplining events. A voltage event corresponds to a short-circuit fault in one or more of the eight front panel outputs. A frequency event corresponds to the crystal requiring adjustment, the rubidium oscillator locking, or rubidium oscillator unlocking. A disciplining event corresponds to the VRFS achieving or losing track of its external disciplining reference source. When an event occurs, the VRFS interrupts the VXIbus commander if it has been enabled to do so. Figure 4-7 shows the structure of the VXI Event Enable Register. The Master Summary bit provides the combined event status for the VRFS. If any enabled event occurs on the VRFS, the Master Summary bit is set. The Global Enable bit is set by the VXI low-level Asynchronous Mode Control command. The Request True bit is set upon power-up. Consequently, the VRFS responds to the VXIbus commander's interrupt acknowledge cycle with a Request True event. This indicates that during an interrupt acknowledge cycle, the VRFS places its logical address in the lower 8 bits (ID) and the request true event (FD_{16}) in the upper 8 bits (status) of the 16-bit status/ID word.

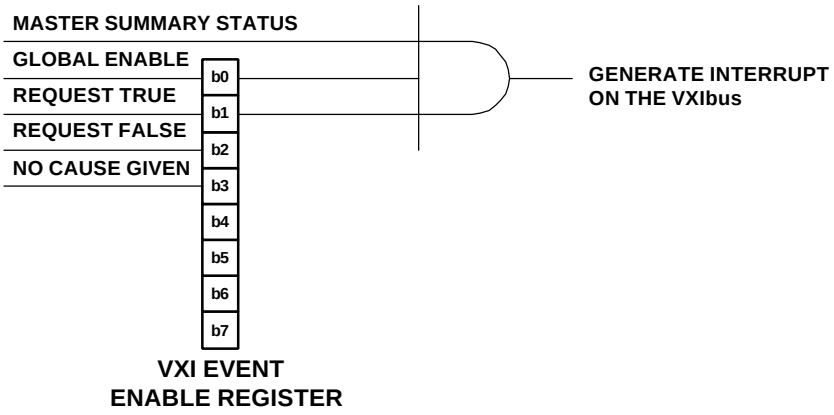

Figure 4-7. Frequency Condition, Frequency Transition Filter, Frequency Event, and Frequency Event Enable Registers

4.5 STATUS DATA STRUCTURE

Figure 4-8 shows the data structures for the status registers on the VRFS. This figure shows condition registers, event registers, and event enable registers. Condition registers reflect the current status of the VRFS. Condition registers change state whenever their corresponding signals change state. Event registers reflect past events that have occurred on the VRFS. Event registers are set high and latched when an event occurs and are reset only when the VXIbus commander reads that event register or issues a *CLS command. Event enable registers provide a means to enable and disable events from propagating onto the next level in the data structure tree. Event enable registers are set and cleared by the VXIbus commander. Figure 4-8 shows the manner in which an event propagates through the event and condition registers on the VRFS. When an event occurs on the VRFS, a cascade of events can propagate through the module and culminate in an interrupt of the VXIbus commander, if the appropriate event enable registers are set.

4.5.1 OUTPUT VOLTAGE EVENTS

If a voltage fault is detected on any of the eight outputs, that fault condition will be reflected in the Voltage Condition Register and latched in the Voltage Event Register. If the bit corresponding to the faulted output is set in the Voltage Event Enable Register, the Voltage Summary Bit will be set in the Questionable Event Register. If the bit corresponding to the Voltage Summary Bit is set in Questionable Event Enable Register, the Questionable Status Bit will be set in the Status Byte. If the bit corresponding to the the Questionable Status Bit is set in Service Request Enable Register, the Master Summary Status Bit will be set in the Status Byte. If the Global Enable and Request True bits are set in the VXI Event Enable Register, a VXIbus interrupt will be generated. This cascade of events is depicted graphically in the tree structure of figure 4-8.

4.5.2 FREQUENCY EVENTS

If a crystal adjustment is required or the rubidium oscillator is unlocked, a fault condition will be reflected in the Frequency Condition Register. A crystal adjust fault will be latched in the Frequency Event Register, but changes in the rubidium oscillator are filtered by the Frequency Transition Filter. If the rubidium oscillator becomes locked and the bit corresponding to the positive transition is set in the Frequency Transition Filter, the Rubidium Lock Bit will be set in the Frequency Event Register. If the rubidium oscillator becomes unlocked and the bit corresponding to the negative transition is set in the Frequency Transition Filter, the Rubidium Unlock Bit will be set in the Frequency Event Register. If the bit corresponding to the frequency event is set in the Frequency Event Enable Register, the Frequency Summary Bit will be set in the Questionable Event Register. If the bit corresponding to the Frequency Summary Bit is set in Questionable Event Enable Register, the Questionable Status Bit will be set in the Status Byte. If the bit corresponding to the the Questionable Status Bit is set in Service Request Enable Register, the Master Summary Status Bit will be set in the Status Byte. If the Global Enable and Request True bits are set in the VXI Event Enable Register, a VXIbus interrupt will be generated. This cascade of events is depicted graphically in the tree structure of figure 4-8

4.5.3 DISCIPLINING EVENTS

A disciplining event corresponds to the VRFS achieving or losing track of its external disciplining reference source. These disciplining sources include the external 10 MHz calibration input, the IRIG B AC modulated input, the IRIG B DC modulated input, the 1 PPS input, and the GPS 1 PPS signal. The current disciplining state is reflected in the Disciplining Condition Register. Changes to the disciplining state are latched in the Disciplining Event Register. If the bit corresponding to the event is set in the Disciplining Event Enable Register, the Disciplining Summary Bit will be set in the Questionable Event Register. If the bit corresponding to the Disciplining Summary Bit is set in Questionable Event Enable Register, the Questionable Status Bit will be set in the Status Byte. If the bit corresponding to the the Questionable Status Bit is set in Service Request Enable Register, the Master Summary Status Bit will be set in the Status Byte. If the Global Enable and Request True bits are set in the VXI Event Enable Register, a VXIbus interrupt will be generated. This cascade of events is depicted graphically in the tree structure of figure 4-8.

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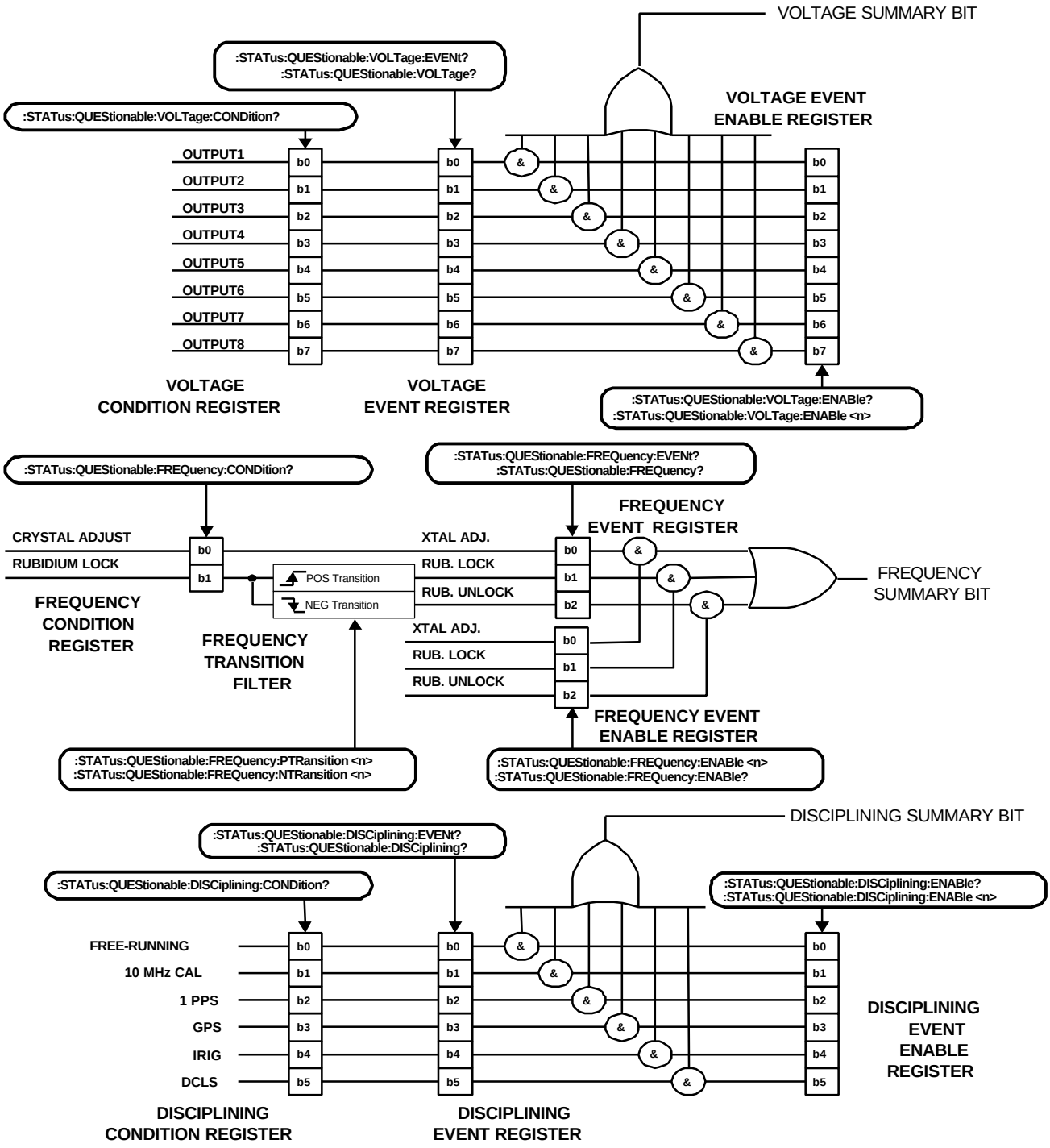

Figure 4-8A VRFS Status Data Structure

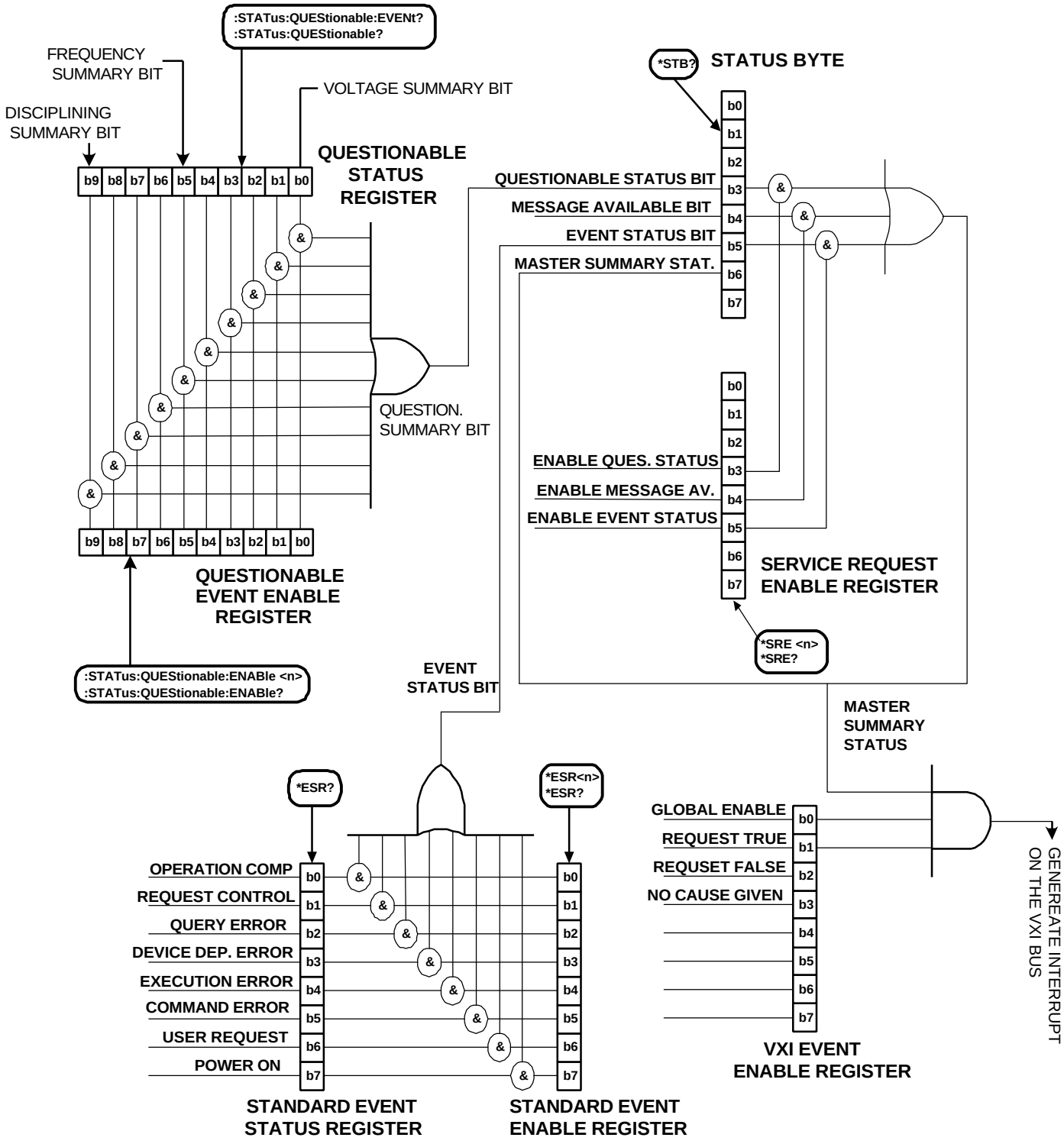

Figure 4-8B VRFS Status Data Structure

4.5.4 VRFS REGISTERS

FRS CONDITION REGISTER (R)

BIT #	FUNCTION
0	XTAL ADJ (0 = OK)
1	OCXO LOCKED (0 = OK)
2	
3	
4	
5	
6	
7	

FRS TRANSITION FILTER REGISTER (R/W)

BIT #	FUNCTION
0	RUB LOCK POSITIVE TRANSISITON
1	RUB LOCK NEGATIVE TRANSISITON
2	
3	
4	
5	
6	
7	

FRS EVENT REGISTER (R/W)

BIT #	FUNCTION
0	XTAL ADJ EVENT
1	OCXO LOCK EVENT
2	OCXO UNLOCK EVENT
3	
4	
5	
6	
7	

FRS EVENT ENABLE REGISTER (R/W)

BIT #	FUNCTION
8	XTAL ADJ EVENT ENABLE
9	OCXO LOCK EVENT ENABLE
10	OCXO UNLOCK EVENT ENABLE
11	
12	
13	
14	
15	

STATUS BYTE (R)

BIT #	FUNCTION
0	
1	
2	
3	QUES STATUS BIT
4	MAV
5	EVENT STATUS BIT
6	MASTER SUMMARY BIT
7	OPER

SERVICE REQUEST ENABLE REGISTER (R/W)

BIT #	FUNCTION
0	
1	
2	
3	ENABLE QUES
4	ENABLE MAV
5	ENABLE ESS
6	
7	ENABLE OPER

VOLTAGE CONDITION REGISTER (R)

BIT #	FUNCTION
0	OUTPUT 1
1	OUTPUT 2
2	OUTPUT 3
3	OUTPUT 4
4	OUTPUT 5
5	OUTPUT 6
6	OUTPUT 7
7	OUTPUT 8

VOLTAGE EVENT REGISTER (R/W)

BIT #	FUNCTION
0	OUTPUT 1 EVENT
1	OUTPUT 2 EVENT
2	OUTPUT 3 EVENT
3	OUTPUT 4 EVENT
4	OUTPUT 5 EVENT
5	OUTPUT 6 EVENT
6	OUTPUT 7 EVENT
7	OUTPUT 8 EVENT

VOLTAGE EVENT ENABLE REGISTER (R/W)

BIT #	FUNCTION
0	OUTPUT 1 EVENT ENABLE
1	OUTPUT 2 EVENT ENABLE
2	OUTPUT 3 EVENT ENABLE
3	OUTPUT 4 EVENT ENABLE
4	OUTPUT 5 EVENT ENABLE
5	OUTPUT 6 EVENT ENABLE
6	OUTPUT 7 EVENT ENABLE
7	OUTPUT 8 EVENT ENABLE

VXI EVENT REGISTER (R/W)

BIT #	FUNCTION
0	GLOBAL ENABLE
1	REQUEST TRUE
2	REQUEST FLASE
3	NO CAUSE GIVEN
4	
5	
6	
7	

DISCIPLINING CONDITION REGISTER (R)

BIT #	FUNCTION
0	NOT DISCIPLINING (FREERUNNING)
1	CAL10 PRESENT
2	PPS PRESENT
3	GPS PRESENT
4	IRIG PRESENT
5	DCLS PRESENT
6	
7	

DISCIPLINING EVENT REGISTER (R/W)

BIT #	FUNCTION
0	NOT DISCIPLINING (FREERUNNING) EVENT
1	CAL10 EVENT
2	PPS EVENT
3	GPS EVENT
4	IRIG EVENT
5	DCLS EVENT
6	
7	

DISCIPLINING EVENT ENABLE REGISTER (R/W)

BIT #	FUNCTION
0	NOT DISCIPLINING (FREERUNNING) EVENT ENABLE
1	CAL10 EVENT ENABLE
2	PPS EVENT ENABLE
3	GPS EVENT ENABLE
4	IRIG EVENT ENABLE
5	DCLS EVENT ENABLE
6	
7	

OPERATION CONDITION REGISTER (R)

BIT #	FUNCTION
0	CALIBRATING
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	

OPERATION EVENT REGISTER (R/W)

BIT #	FUNCTION
0	CALIBRATING EVENT
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	

OPERATION EVENT ENABLE REGISTER (R/W)

BIT #	FUNCTION
0	CALIBRATING EVENT ENABLE
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	

STANDARD EVENT STATUS REGISTER (R)

BIT #	FUNCTION
0	OPERATION COMPLETE
1	REQUEST CONTROL
2	QUERY ERROR
3	DEVICE DEPENDENT ERROR
4	EXECUTION ERROR
5	COMMAND ERROR
6	USER REQUEST
7	POWER ON

STANDARD EVENT ENABLE STATUS REGISTER (R/W)

BIT #	FUNCTION
0	OPERATION COMPLETE ENABLE
1	REQUEST CONTROL ENABLE
2	QUERY ERROR ENABLE
3	DEVICE DEPENDENT ERROR ENABLE
4	EXECUTION ERROR ENABLE
5	COMMAND ERROR ENABLE
6	USER REQUEST ENABLE
7	POWER ON ENABLE

QUESTIONABLE STATUS REGISTER (R)

BIT #	FUNCTION
0	VOLTAGE SUMMARY BIT
1	
2	
3	
4	
5	FREQUENCY SUMMARY BIT
6	
7	
8	
9	DISCIPLINING SUMMARY BIT
10	
11	
12	
13	
14	
15	NOT USED

QUESTIONABLE EVENT REGISTER (R/W)

BIT #	FUNCTION
0	VOLTAGE EVENT
1	
2	
3	
4	
5	FREQUENCY EVENT
6	
7	
8	
9	DISCIPLINING EVENT
10	
11	
12	
13	
14	
15	NOT USED

QUESTIONABLE EVENT ENABLE REGISTER (R/W)

BIT #	FUNCTION
0	VOLTAGE EVENT ENABLE
1	
2	
3	
4	
5	FREQUENCY EVENT ENABLE
6	
7	
8	
9	DISCIPLINING EVENT ENABLE
10	
11	
12	
13	
14	
15	NOT USED

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5.0 PARTS LIST

The parts lists listed below can be found on the pages following page 5-2.

Title	Number	Revision
VXI Rubidium Frequency Standard	bc824VXI	D
VXI Rubidium Frequency Standard	35029	C

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Item: BC824VXI Description: BC824VXI VXI-RUBIDIUM FRQUENCY STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell
10	225	INHOUSE KITTING-OP10	0.00	0.00	0.00	0.000	0.000	?	?	1.00	No	

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	711671 BRACKET		2.00000	EA	U	I			?
M	711666 FRONT PANEL ASSY		1.00000	EA	U	I			?
M	2330-1450 HANDLE KIT: VME		1.00000	EA	U	I			?
M	711667 SHIELD PANEL - COMP		1.00000	EA	U	I			?
M	711669 SHIELD DOOR		1.00000	EA	U	I			?
M	2310-6980-5 STANDOFF: MF, 4-40X1-15/16, 1/4HEX, BR		6.00000	EA	U	I			?
M	35029 VXI RUBIDIUM FREQ. STANDARD	D	1.00000	EA	U	I			?
M	711668 SHIELD PANEL - SOLDER		1.00000	EA	U	I			?

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell
20	327	OPER.-ELEC/MECH ASSY	0.00	0.00	0.00	2.000	0.000	?	?	1.00	No	

Notes:

REQUIRES THE FOLLOWING HARDWARE:

*4004 4-40 X 3/16 F.H. SCREW U.C.
5 EACH
*4006 4-40 X 1/4 P.H. SCREW 2 EACH
*4007 4-40 X 1/4 F.H. SCREW U.C.
6 EACH
*4048 #4 SPLIT LOCK WASHER 9 EACH
*4049 #4 FLAT WASHER SM. 8 EACH
*4053 4-40 HEX NUT 3 EACH

FLOOR STOCK NOTE.
SEE ASSEMBLY DWG# A925119NC FOR
REFERENCE.
*9101 STANDARD DATUM LOGO PLATE
*9109 LOGO PLATE FOR BC824VXI

Item: BC824VXI Description: BC824VXI VXI-RUBIDIUM FRQUENCY STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell
		SEE ASSEMBLY AID A-BC824VXI										
30	452	PROD. TEST INSP	0.00	0.00	0.00	0.000	0.000	?	?	1.00	No	
40	400	TEST	0.00	0.00	0.00	2.000	0.000	?	?	1.00	No	

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell
10	225	INHOUSE KITTING-OP10	0.00	0.00	0.00	0.000	0.000	?	?	1.00	No	

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0103-1000		5.00000	ea	U	I			?
	RES: 100 OHM, 1/10W, 1%, SM0805								
	R119 R264 R279 R293 R298								
M	0103-1001		61.00000	EA	U	I			?
	RES: 1K, 1/10W, 1%, SM0805								
	R14 R22 R27 R31 R43 R57 R70 R72								
	R77 R92 R99 R100 R102 R123 R125 R128								
	R130 R132 R134 R137 R139 R141 R143 R150								
	R153 R155 R157 R159 R160 R162 R163 R165								
	R166 R169 R170 R171 R174 R185 R188 R189								
	R191 R194 R202 R205 R206 R213 R226 R232								
	R238 R246 R247 R254 R258 R259 R266 R268								
	R270 R271 R275 R276 R280								
M	0103-1002		46.00000	EA	U	I			?
	RES: 10K, 1/10W, 1%, SM0805								
	R4 R55 R62 R80 R87 R88 R96 R112								
	R113 R114 R120 R148 R173 R181 R182 R183								
	R186 R187 R211 R215 R216 R217 R229 R234								
	R235 R237 R239 R242 R243 R249 R252 R256								
	R260 R261 R262 R263 R265 R267 R272 R273								
	R274 R277 R281 R294 R295 R304								
M	0103-1003		24.00000	EA	U	I			?
	RES: 100K, 1/10W, 1%, SM0805								
	R11 R12 R19 R20 R28 R29 R38 R39								
	R53 R54 R64 R65 R71 R81 R85 R89								
	R101 R104 R115 R118 R179 R240 R300 R301								
M	0103-10R0		4.00000	EA	U	I			?
	RES: 10.0 OHM, 1/10W, 1%, SM0805								
	R241 R269 R284 R297								
M	0103-2000		21.00000	EA	U	I			?
	RES: 200 OHM, 1/10W, 1%, SM0805								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
	R15 R18 R23 R26 R32 R33 R44 R45 R50 R51 R58 R59 R73 R74 R76 R93 R95 R103 R106 R196 R197								
M	0103-2002 RES: 20K, 1/10W, 1%, SM0805		17.00000	EA	U	I			?
	R1 R3 R5 R6 R8 R9 R10 R82 R86 R90 R94 R145 R149 R154 R203 R248 R255								
M	0103-2210 RES: 221 OHM, 1/10W, 1%, SM0805		3.00000	EA	U	I			?
	R2 R7 R83								
M	0103-2261 RES: 2.26K, 1/10W, 1%, SM0805		4.00000	EA	U	P			?
	R52 R172 R212 R220								
M	0103-2490 RES: 249 OHM, 1/10W, 1%, SM0805		1.00000	EA	U	I			?
	R199								
M	0103-2741 RES: 2.74K, 1/10W, 5%, SM0805		1.00000	EA	U	I			?
	R138								
M	0103-3011 RES: 3.01K, 1/10W, 1%, SM0805		1.00000	EA	U	I			?
	R75								
M	0103-3322 RES: 33.2K, 1/10W, 1%, SM0805		1.00000	EA	U	I			?
	R180								
M	0103-3741 RES: 3.74K, 1/10W, 1%, SM0805		1.00000	EA	U	I			?
	R200								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0103-4021		4.00000	EA	U	I			?
	RES: 4.02K, 1/10W, 1%, SM0805								
	R46 R168 R192 R193								
M	0103-4751		37.00000	EA	U	I			?
	RES: 4.75K, 1/10W, 1%, SM0805								
	R36 R37 R40 R41 R49 R63 R66 R67								
	R117 R126 R135 R144 R146 R147 R152 R177								
	R184 R198 R208 R214 R218 R221 R224 R225								
	R227 R231 R253 R278 R283 R285 R286 R287								
	R288 R289 R290 R291 R292								
M	0103-47R5		8.00000	EA	U	I			?
	RES: 47.5 OHM, 1/10W, 1%, SM0805								
	R17 R25 R34 R47 R60 R78 R97 R107								
M	0103-4990		10.00000	EA	U	I			?
	RES: 499 OHM, 1/10W, 1%, SM0805								
	R68 R124 R129 R133 R136 R142 R175 R209								
	R210 R282								
M	0103-4991		24.00000	EA	U	I			?
	RES: 4.99K, 1/10W, 1%, SM0805								
	R13 R16 R21 R24 R30 R35 R42 R48								
	R56 R61 R69 R79 R91 R98 R105 R108								
	R116 R151 R156 R201 R230 R233 R244 R296								
M	0103-4992		5.00000	EA	U	I			?
	RES: 49.9K, 1/10W, 1%, SM0805								
	R178 R190 R245 R299 R305								
M	0103-49R9		7.00000	EA	U	I			?
	RES: 49.9 OHM, 1/10W, 1%, SM0805								
	R121 R122 R127 R131 R140 R302 R303								
M	0103-5901		1.00000	EA	U	I			?
	RES: 5.9K, 1/10W, 1%, SM0805								
	R236								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0103-6040 RES: 604 OHM, 1/10W, 1%, SM0805 R158 R161 R164 R167 R176 R195 R219 R228		8.00000	EA	U	I			?
M	0103-6042 RES: 60.4K, 1/10W, 1%, SM0805 R110		1.00000	EA	U	P			?
M	0103-6191 RES: 6.19K, 1/10W, 1%, SM0805 R111 R250		2.00000	EA	U	I			?
M	0103-6490 RES: 649 OHM, 1/10W, 1%, SM0805 R204 R207 R251 R257		4.00000	EA	U	I			?
M	0103-6981 RES: 6.98K, 1/10W, 1%, SM0805 R222		1.00000	EA	U	I			?
M	0103-8250 RES: 825 OHM, 1/10W, 1%, SM0805 R84		1.00000	EA	U	I			?
M	0128-0103 RES: NET 10K, 9R, SIP10 RP1 RP2 RP3 RP4 RP5		5.00000	EA	U	I			?
M	0203-0047 CAP: 47PF, 50V, 5%, COG, SM0805 C36		1.00000	EA	U	I			?
M	0203-0101 CAP: 100PF, 50V, 5%, COG, SM0805 C20 C92 C133 C135 C218		5.00000	EA	U	I			?

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0203-0102		12.00000	EA	U	I			?
	CAP: 1000PF, 50V, 5%, COG, SM0805								
	C1 C5 C31 C49 C52 C104 C175 C176 C181 C185 C216 C217								
M	0203-0221		1.00000	EA	U	I			?
	CAP: 220PF, 50V, 5%, COG, SM0805								
	C48								
M	0203-0331		1.00000	EA	U	I			?
	CAP: 330PF, 50V, 5%, COG, SM0805								
	C39								
M	0203-0471		2.00000	EA	U	I			?
	CAP: 470PF, 50V, 5%, COG, SM0805								
	C38 C47								
M	0203-08R2		1.00000	EA	U	I			?
	CAP: 8.2PF, 50V, 5%, COG, SM0805								
	C40								
M	0213-0103		44.00000	EA	U	I			?
	CAP: 0.01UF, 50V, 20%, X7R, SM0805								
	C4 C33 C53 C56 C57 C58 C59 C61 C64 C65 C66 C67 C70 C78 C79 C80 C81 C82 C83 C84 C85 C87 C88 C89 C91 C93 C97 C100 C102 C108 C117 C118 C119 C121 C122 C126 C130 C139 C144 C150 C151 C154 C155 C206								
M	0213-0103-1		16.00000	EA	U	I			?
	CAP: 0.01UF, 200V, 10%, X7R, SM1206								
	C9 C10 C12 C13 C15 C16 C18 C19 C23 C24 C28 C30 C35 C37 C46 C51								
M	0213-0104-2		113.00000	EA	U	I			?
	CAP: 0.1UF, 25V, 10%, X7R, SM0805								
	C8 C11 C14 C17 C21 C22 C27 C29								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
	C34 C41 C60 C62 C63 C69 C71 C72 C73 C74 C75 C76 C77 C86 C90 C94 C95 C96 C98 C99 C101 C103 C105 C106 C107 C109 C110 C111 C112 C113 C114 C115 C116 C120 C123 C124 C125 C127 C128 C129 C131 C132 C134 C136 C137 C138 C140 C141 C142 C143 C145 C146 C147 C148 C149 C152 C153 C156 C157 C158 C159 C160 C161 C162 C164 C165 C166 C167 C170 C171 C172 C173 C174 C177 C178 C179 C180 C182 C183 C184 C186 C187 C188 C190 C191 C192 C193 C194 C195 C196 C197 C198 C199 C201 C202 C203 C204 C205 C207 C208 C210 C212 C213 C214 C215								
M	0213-0105		6.00000	EA	U	I			?
	CAP: 1UF, 50V, 20%, X7R, SM2220 C154 C163 C168 C169 C189 C200								
M	0223-0106		6.00000	EA	U	I			?
	CAP: 10UF, 20V, 20%, SM2412 C42 C43 C44 C45 C55 C219								
M	0223-0225		2.00000	EA	U	I			?
	CAP: 2.2UF, 25V, 10%, SM3528 C3 C7								
M	0223-0685		8.00000	EA	U	I			?
	CAP: 6.8UF, 50V, 10%, SM7343 C2 C6 C25 C26 C32 C50 C68 C209								
M	0301-0811		10.00000	EA	U	I			?
	IC: AD811A DIP8 U4 U5 U6 U8 U12 U21 U25 U30 U41 U49								
M	0301-7915		1.00000	EA	U	I			?
	IC: 7915 TO-220 A1 SEE NOTES								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0303-0002		1.00000	EA	U	I			?
	IC: REF02 S08								
	U45								
M	0303-0208		1.00000	EA	U	I			?
	IC: CDC208 SOL20								
	U22								
M	0303-0211		1.00000	EA	U	I			?
	IC: DG211BDY S016								
	U24								
M	0303-0213		5.00000	EA	U	I			?
	IC: OP213ES S08								
	U15 U33 U44 U51 U58								
M	0303-0277		2.00000	EA	U	I			?
	IC: TLC277 S08								
	U11 U34								
M	0303-0320		1.00000	EA	U	I			?
	IC: TMS320F240PQ QFP132								
	U55								
M	0303-0339		2.00000	EA	U	I			?
	IC: LM339A SO14								
	U9 U17								
M	0303-0394		2.00000	EA	U	I			?
	IC: MAX394 SOL20								
	U36 U37								
M	0303-0515		1.00000	EA	U	P			?
	IC: MAX515 SO8								
	U19								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0303-0611		1.00000	EA	U	I			?
	IC: DG611DY S016								
	U20								
M	0303-0736		2.00000	EA	U	I			?
	IC: AD736KR S08								
	U42 U43								
M	0303-0780-15		1.00000	EA	U	I			?
	IC: TL780-15 TO-220								
	A2								
	SEE NOTES								
M	0303-0820		1.00000	EA	U	P			?
	IC: AD820 S08								
	U16								
M	0303-0822		2.00000	EA	U	I			?
	IC: AD822A S08								
	U46 U47								
M	0303-0826		1.00000	EA	U	I			?
	IC: AD826A S08								
	U48								
M	0303-0961		3.00000	EA	U	I			?
	IC: MAX961 S08								
	U1 U2 U27								
M	0303-1466		2.00000	EA	U	I			?
	IC: LT1466LC S08								
	U10 U23								
M	0303-1655-0		1.00000	EA	U	I			?
	IC: 16550 PLCC44								
	U39								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0303-25C0-20		1.00000	EA	U	I			?
	IC: 25C020 S08								
	U60								
M	0303-3186		1.00000	EA	U	I			?
	IC: MAX3186 S020								
	U26								
M	0303-5206-5		1.00000	EA	U	I			?
	IC: XC5206-5 QFP208								
	U53								
M	0303-6164		1.00000	EA	U	I			?
	IC: SRAM 256KX16 10NS SOJ44								
	U50								
M	0303-8190		1.00000	EA	U	I			?
	IC: MAX819M SO8								
	U61								
M	0303-8228		1.00000	EA	U	I			?
	IC: DAC8228 SOL20								
	U54								
M	0303-9831		1.00000	EA	U	I			?
	IC: AD9831AST QFP48								
	U32								
M	0303-9F74		2.00000	EA	U	I			?
	IC: 74F74 S014								
	U14 U28								
M	0303-ACT0-8		1.00000	EA	U	I			?
	IC: 74ACT08 SO14								
	U18								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0303-ACT1-4		1.00000	EA	U	I			?
	IC: 74ACT14 SO14								
	U31								
M	0303-ACT2-73		2.00000	EA	U	I			?
	IC: 74ACT273 SOL20								
	U29 U38								
M	0303-ALS7-60		2.00000	EA	U	I			?
	IC: 74ALS760 SOL20								
	U35 U56								
M	0303-AS10-34		4.00000	EA	U	I			?
	IC: 74AS1034 SO14								
	U7 U13 U52 U57								
M	0503-0141		8.00000	EA	U	I			?
	DIODE: M1MA141KT1 SOT-323								
	CR9 CR32 CR33 CR35 CR36 CR39 CR40 CR41								
M	0503-0914		31.00000	EA	U	I			?
	DIODE: 1N914 SOT-23								
	CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR10 CR11 CR12 CR25 CR27 CR37 CR44 CR45 CR46 CR47 CR48 CR49 CR50 CR51 CR52 CR53 CR54 CR55 CR56 CR57 CR58 CR59 CR60								
M	0523-2805		19.00000	EA	U	I			?
	DIODE: HSMS-2805 SOT-143								
	CR13 CR14 CR15 CR16 CR17 CR19 CR20 CR22 CR23 CR24 CR26 CR28 CR29 CR30 CR31 CR34 CR38 CR42 CR43								
M	0553-3906		4.00000	EA	U	I			?
	XSTR: 2N3906 SOT-23								
	Q1 Q2 Q3 Q4								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	0603-0474		1.00000	EA	U	I			?
	IND: 0.47UH 10%								
	L2								
M	0603-0822		1.00000	EA	U	I			?
	IND: 8.2UH 10%								
	L1								
M	0610-0310		9.00000	EA	U	I			?
	FILTER: EMI 50V 7A								
	FL1 FL2 FL3 FL4 FL5 FL6 FL7 FL8 FL9								
M	1205-0008-1		1.00000	EA	U	I			?
	SW: DIP 8PST								
	SW1								
M	1301-LPRO		1.00000	EA	U	I	11/01/99		?
	(OBS.) RUB. OSC - See 102500-001								
	Y1								
M	1302-2900		1.00000	EA	U	I			?
	OSCILLATOR: 10 MHZ (LOW PHASE NOISE)								
	Y2								
M	1702-0001-1		3.00000	EA	U	I			?
	CONN: 1P 1X1 HEADER ST								
	TP1 TP3 TP9								
M	1702-0002-2		8.00000	EA	U	I			?
	CONN: 2P 1X2 HEADER ST								
	JP11 JP12 JP13 JP14 JP15 JP16 JP17 JP18								
M	1702-0003		11.00000	EA	U	I			?
	CONN: 3P 1X3 HEADER ST								
	JP1 JP2 JP3 JP4 JP5 JP6 JP7 JP8 JP9 JP10 P4								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	1702-0006-4 CONN: 6P 1X6 HEADER ST P5		1.00000	EA	U	I			?
M	1702-0009 CONN: 9P 1X9 HEADER ST P3 P8		2.00000	EA	U	I			?
M	1702-0010-7 CONN: 10P 2X5 HEADER ST J14		1.00000	EA	U	I			?
M	1702-0012 CONN: 12P 2X6 SOC STRIP J12		1.00000	EA	U	I			?
M	1702-2514 CONN: 14P 2X7 HEADER ST P7		1.00000	EA	U	I			?
M	1702-6002-10 CONN: 10P 2X5 HEADER ST P6		1.00000	EA	U	I			?
M	1703-0096 CONN: 96P DIN MALE R/A P1 P2		2.00000	EA	U	I			?
M	1704-1005 CONN: BNC JACK R/A PC J1 J2 J3 J4 J5 J6 J7 J8 J9		9.00000	EA	U	I			?
M	1704-5862 CONN: OSX COAX JACK ST J11 J13 J16		3.00000	EA	U	I			?

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell

Type	Item	Revision	Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
M	1704-DF11		1.00000	EA	U	I			?
	CONN: 8P 2X4 SOC STRIP ST 2MM								
	J15								
M	1704-HD15-S1		1.00000	EA	U	I			?
	CONN: 15P D-SUB RECP R/A PC								
	J10								
M	172494	D	1.00000	EA	U	I			?
	P.C. BOARD								
M	1790-9453		2.00000	EA	U	I			?
	SCREW LOCK KIT: D-SUB CONN FEMALE								
	J10 (35013) TO LPRO								
M	2204-0017		1.00000	EA	U	I			?
	LED: DUAL GREEN/RED T-1 R/A								
	CR18								
M	2204-0018		1.00000	EA	U	I			?
	LED: DUAL GREEN/GREEN T-1 R/A								
	CR21								
M	2310-1248-12		6.00000	EA	U	I			?
	SPACER: SWAGE, #4X3/8, 1/4RND, BR								
M	35013		1.00000	EA	U	I			?
	LPRO CONNECTOR (FOR 35029)								
M	711590	A	1.00000	EA	U	I			?
	HEATSINK:LPRO								
M	711670	A	2.00000	EA	U	I			?
	WASHER, GANG, LPRO								
	INSTALLED ON NEX ASSEMBLY.								
M	DP2000		1.00000	EA	U	I			?
	PLD2000								
	U3								
M	DP2100		1.00000	EA	U	I			?
	PLD2100								

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell
	Type	Item	Revision			Quantity	U/M	Per	Ref	Eff Date	Obs Date	BOM Seq
		U40										
	M	DT5000				1.00000	EA	U	I			?
		PROM										
		U59										
	M	102500-001				1.00000	EA	U	T	11/05/99		?
		FINAL ASSY, LPRO										
	M	0103-0000				1.00000	EA	U	I			?
		RES: JUMPER, 0 OHM, 0W, SM0805										
		R109										
	M	0103-1651				1.00000	EA	U	P			?
		RES: 1.65K, 1/10W, 1%, SM0805										
		R223										
20	327	OPER.-ELEC/MECH ASSY	0.00	0.00	0.00	5.000		0.000		?	?	1.00 No

Notes:

INSTALL HARDWARE LISTED BELOW ON A1 AND
A2.
SCREW 4-40 X 5/16" *4011 QTY. 2
#4 FLAT WASHER *4049 QTY.2
#4 SPLIT WASHER *4048 QTY.2
#4 NUT *4053 QTY.2

INSTALL THERMAL BASEPLATE PAD BETWEEN
LPRO RUBIDIUM OSC P/N 1301-LPRO AND
HEATSINK P/N 711590

INSTALL HEATSINK P/N 711590 AND GANG
WASHER P/N 711670 TO LPRO RUDIDIUM OSC
P/N 1301-LPRO USING FOLLOWING HARDWARE:
SCREW 4-40 X 3/4" *4026 QTY. 6
#4 SPLIT WASHER *4048 QTY. 6
TO SECURE LPRO AND HEATSINK TO P.C.
BOARD USE THREADLOCKER 222 OR EQUIV. ON
4-40 X 3/4" SCREWS.

SEE ASSEMBLY AID # A-35029

Item: 35029 Description: VXI RUBIDIUM FREQ. STANDARD Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Size	Ctl Pnt	Cell
30	452	PROD. TEST INSP	0.00	0.00	0.00	0.000	0.000	?	?	1.00	No	
40	400	TEST	0.00	0.00	0.00	0.000	0.000	?	?	1.00	No	

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CHAPTER SIX

DRAWINGS LIST

6.0 DRAWINGS

The drawings listed below can be found on the pages following page 6-2.

TITLE	NUMBER	REVISION
VXI Rubidium Frequency Standard	A-bc824VXI	D
VXI Rubidium Frequency Standard	35029	C

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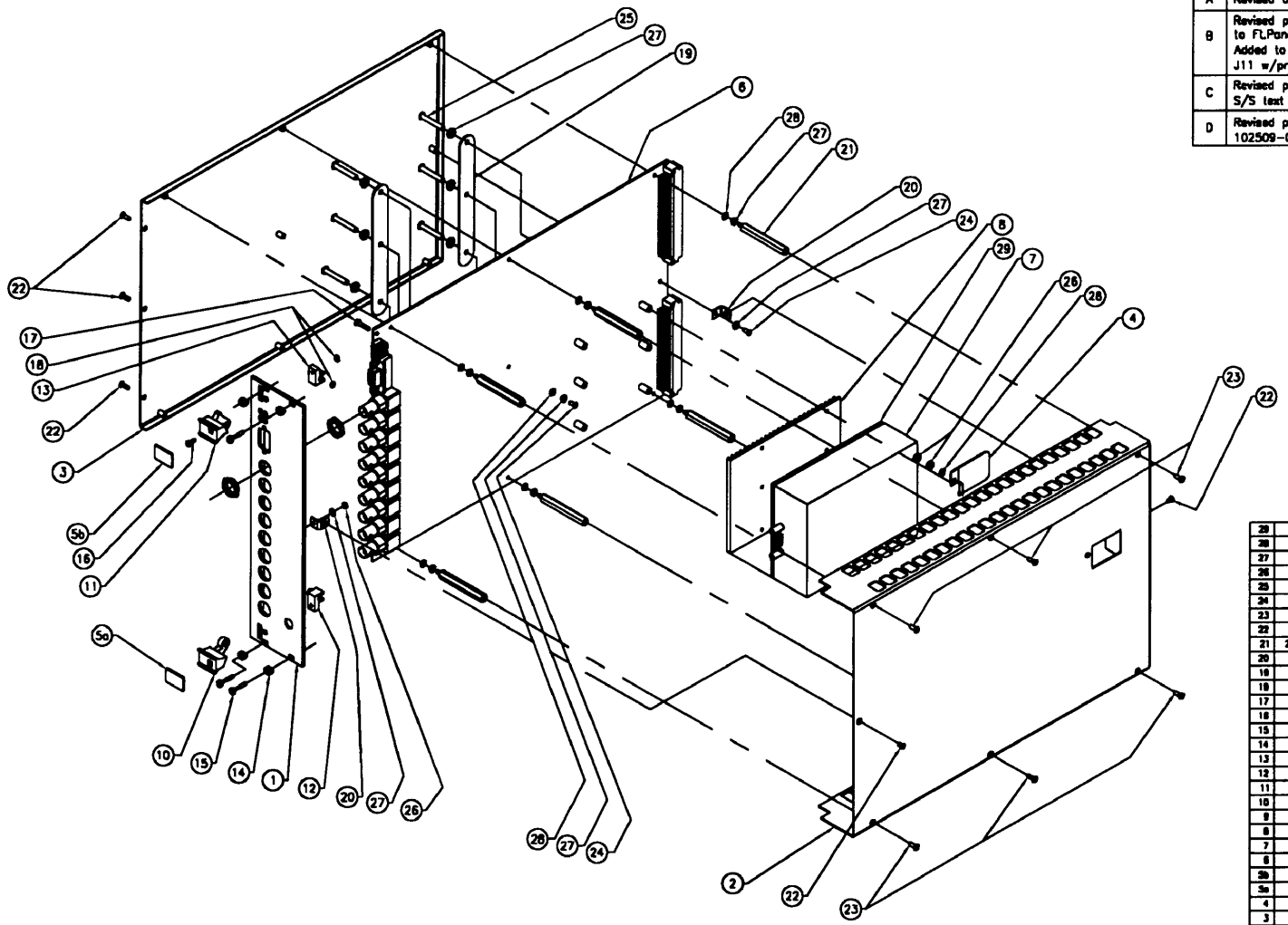

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Revised and released per ECO T7750.	06/98	CFC
B	Revised per ECO T7965: Added GPS hole to Ft.Panel. Sht2: Deleted J10a printing. Added to J5 printing (SINE/TTL), Added J11 w/printing.	04/23/99	G.H.
C	Revised per ECO T7965-1: Chg J1 to J8 S/S text to read SINE/TTL.	04/30/99	G.H.
D	Revised per ECO T7965-4: Added (29) 102509-001 Thermal Pad	06/14/99	G.H.

ITEM	PART NUMBER	DESCRIPTION	QTY.
29	102509-001	Thermal Pad	1
28	*4048	Washer, #4 Flat	8
27	*4048	Washer, #4 Lock, Split	15
26	*4053	Nut, #4-40, Hex	3
25	*4036	Screw, #4-40 x 3/4, FH	6
24	*4006	Screw, #4-40 x 1/4, FH	2
23	*4007	Screw, #4-40 x 1/4, FH U.C.	8
22	*4004	Screw, #4-40 x 3/16, FH U.C.	5
21	2310-0880-5	Standoff, #4-40 x 1.038, male/female, hex	6
20	711871	Bracket, .25 w/4-40 thd x .25 w/.139 hole	2
19	711870	Washer, Comp, bc824VXI	2
18	(2)	Nut, M 2.5 x 45 P, Hex	4
17	(2)	Screw, M 2.5 x 14, FH	2
16	(2)	Screw, M 2.5 x 8, FH	2
15	(2)	Screw, Captive, Phillips p/n VMCS 4000	4
14	(2)	Screw, Retainer, Phillips p/n VMCR 3000	4
13	(2)	Bracket, Ejector Handle, VXI, Left, Phillips p/n VMEB 3000 L	1
12	(2)	Bracket, Ejector Handle, VXI, Right, Phillips p/n VMEB 3000 R	1
11	(2)	Ejector Handle, VXI, Left, Phillips p/n VMEX 1000 L	1
10	(2)	Ejector Handle, VXI, Right, Phillips p/n VMEX 1000 R	1
9	(2)	Plate, Phillips p/n VMCP 5000 (Replaced by (5a) & (5b))	2
8	711580	Heatsink, LPRO	1
7	1301-LPRO	LPRO Rubidium	1
6	35029	PCB Assembly, bc824VXI	1
5b	*9108	Label, bc824VXI, ID	1
5a	*9101	Label, Datum, Logo	1
4	711648	Shield Door, bc824VXI	1
3	711888	Shield Panel, Solder, bc824VXI	1
2	711887	Shield Panel, Component, bc824VXI	1
1	711886	Front Panel Assembly, bc824VXI	1

PARTS LIST

(2) Part number: 2330-1450 VME Hardware Kit, Phillips #VME 6U1450.

1 Dimensions shown are in inches. Dimensions in () are for reference only, not to be applied to critical features.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL. ON 2 PLACE DECIMALS ± 0.03 ANGLES ± 1°

TITLE: Assembly, bc824VXI

datum inc

DRN	Rdd/Omnics	1/98/98	DES	JE/Omnics	12/97
CHK	CFC	3/98/98	ENGR	CH	3/98/98
SCALE	NONE		FILE	OJPN2	

C | A-bc824VXI | D

SIZE | SHT 1 OF 3 | REV

CAD FILE NAME: bc824-10.dwg DRW NO. 890

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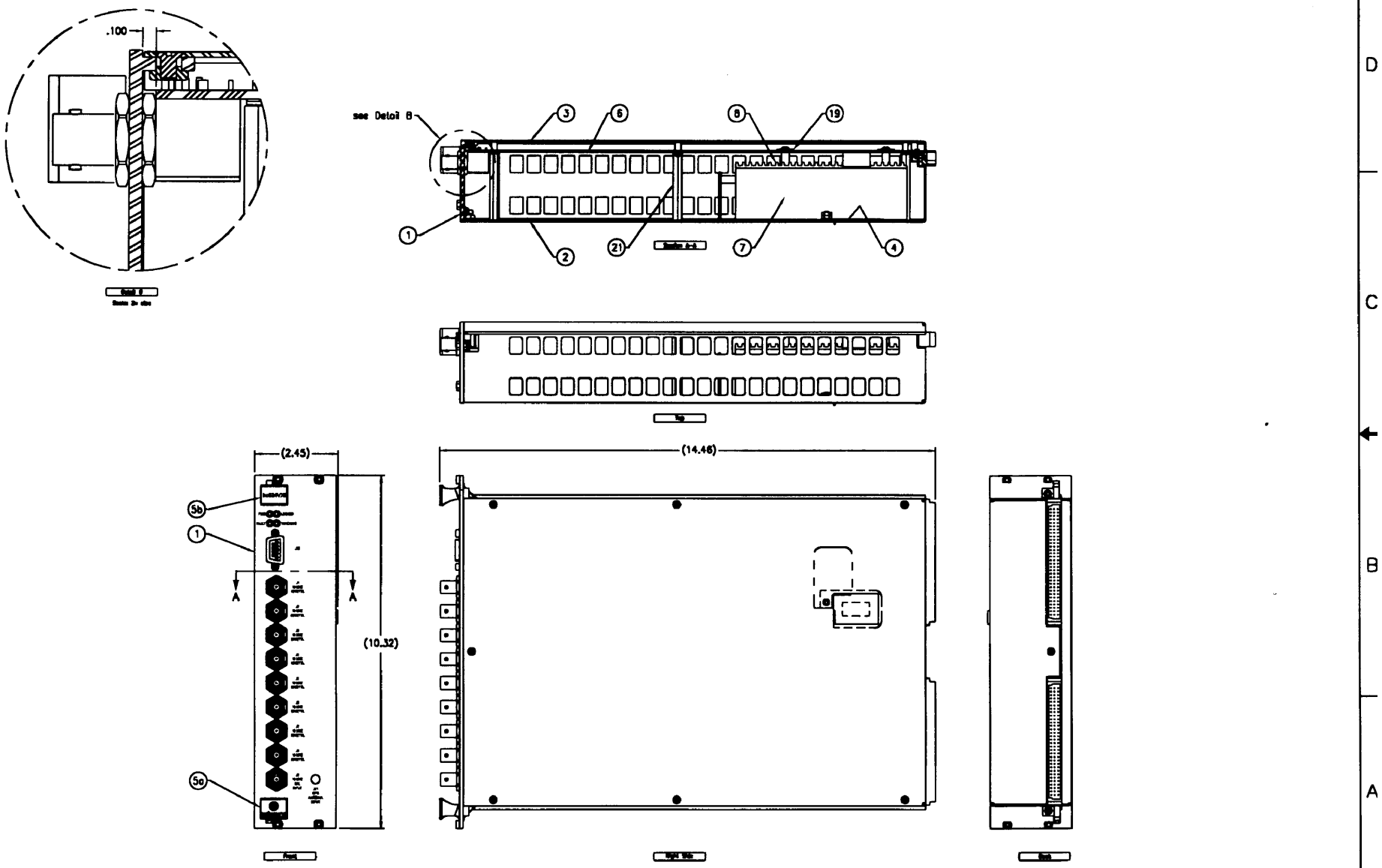

NOTES: UNLESS OTHERWISE SPECIFIED

C	A-bc824VXI	D
SIZE	SHT 2 OF 3	REV

CAD FILE NAME: bc824-2c.dwg BBK NO. 890

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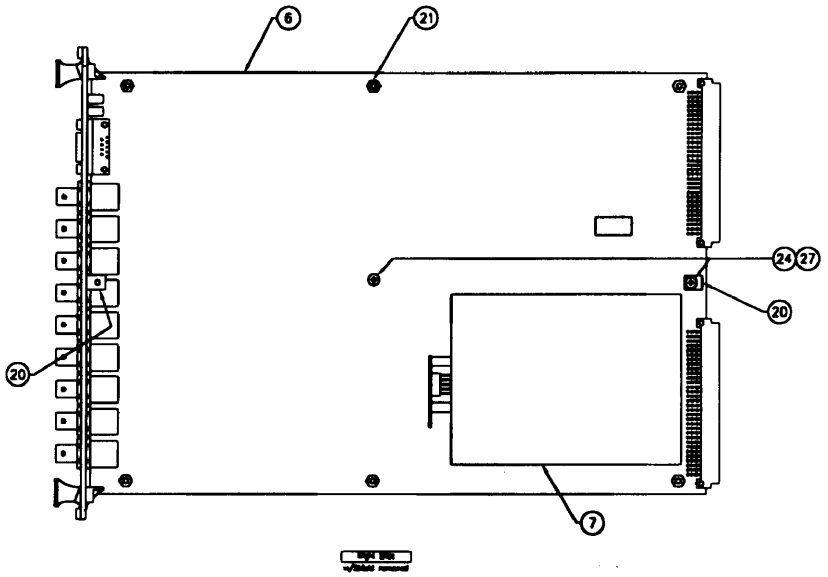

NOTES: UNLESS OTHERWISE SPECIFIED

C	A-bc824VXI	D
SIZE	SHT 3 OF 3	REV

CAD FILE NAME: bc824-30.dwg DISC NO. 890

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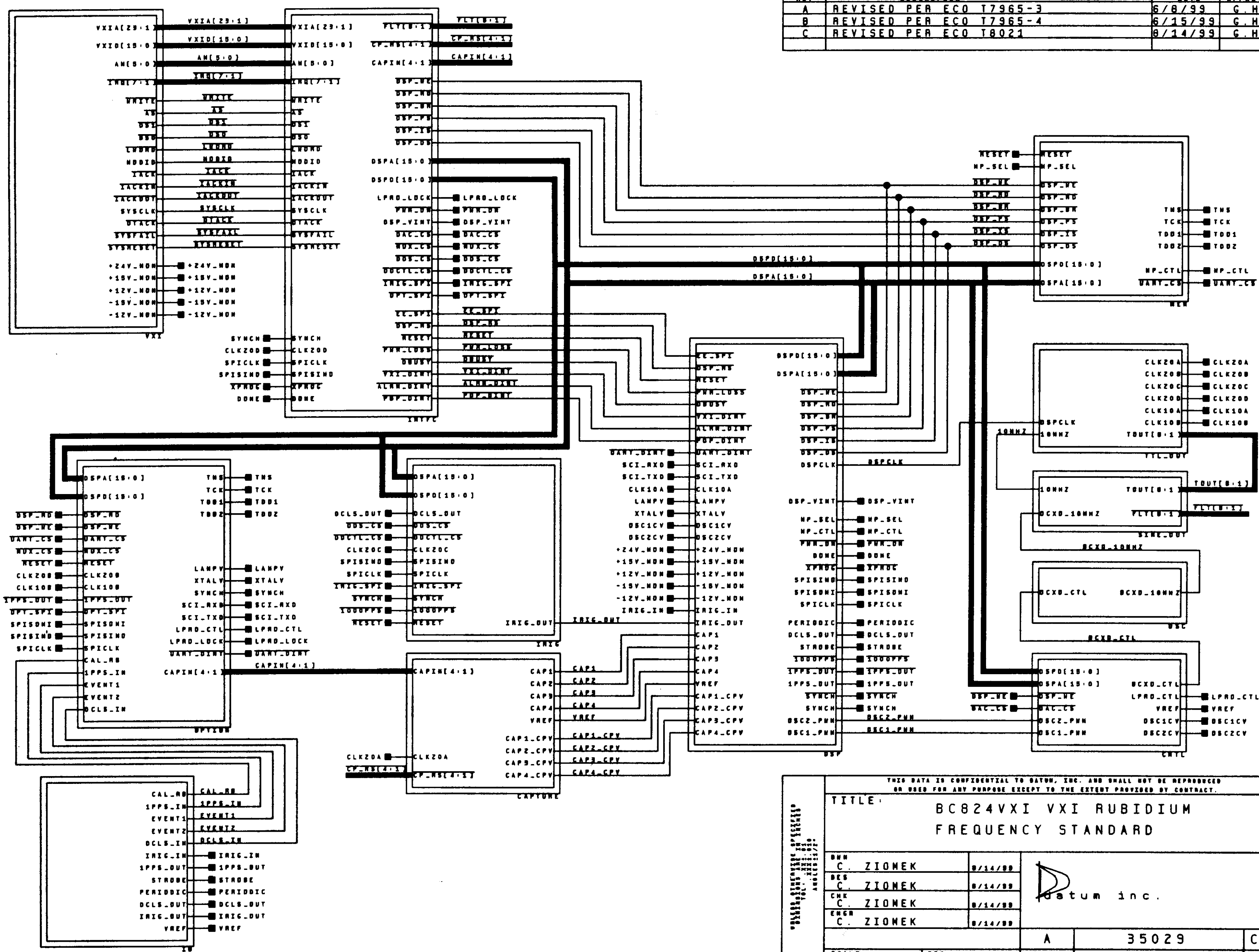
REV	DESCRIPTION	DATE	APPROVED
A	REVISED PER ECO T7965-3	6/8/99	G.H.
B	REVISED PER ECO T7965-4	6/15/99	G.H.
C	REVISED PER ECO T8021	8/14/99	G.H.



TITLE: BC824VXI VXI RUBIDIUM FREQUENCY STANDARD

DWN	C. ZIOMEK	8/14/99
DES	C. ZIOMEK	8/14/99
CHK	C. ZIOMEK	8/14/99
ENGR	C. ZIOMEK	8/14/99

Datum inc.

SCALE	NONE	FSC	31160	SIZE A	35029	SHT 1 OF 13	REV C

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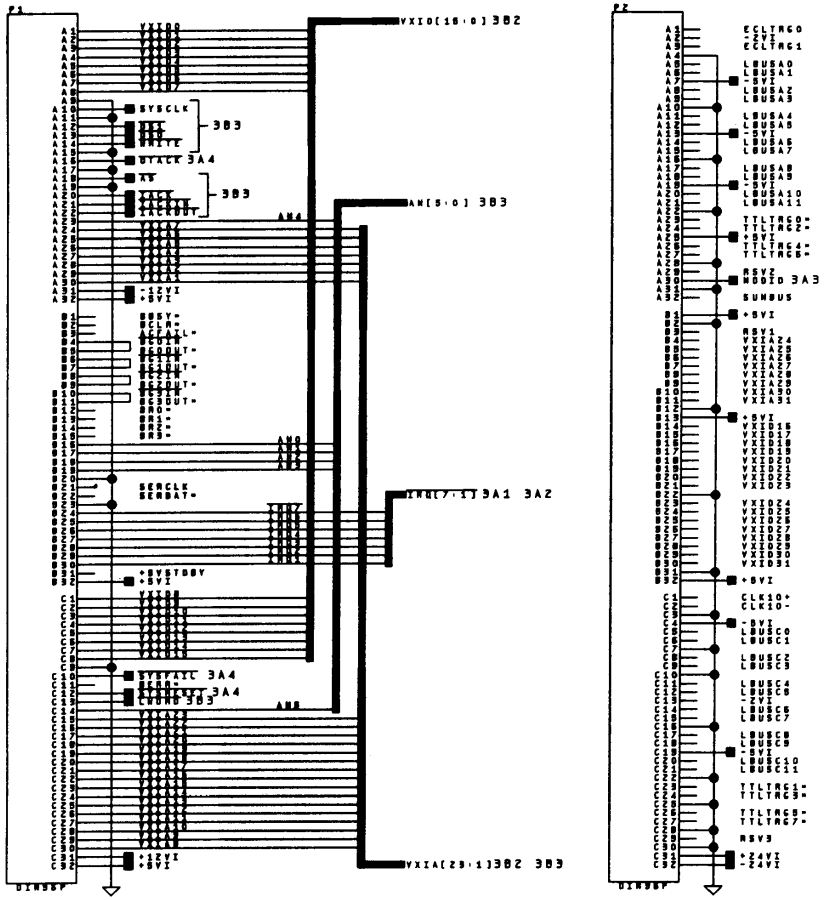

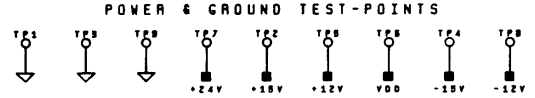

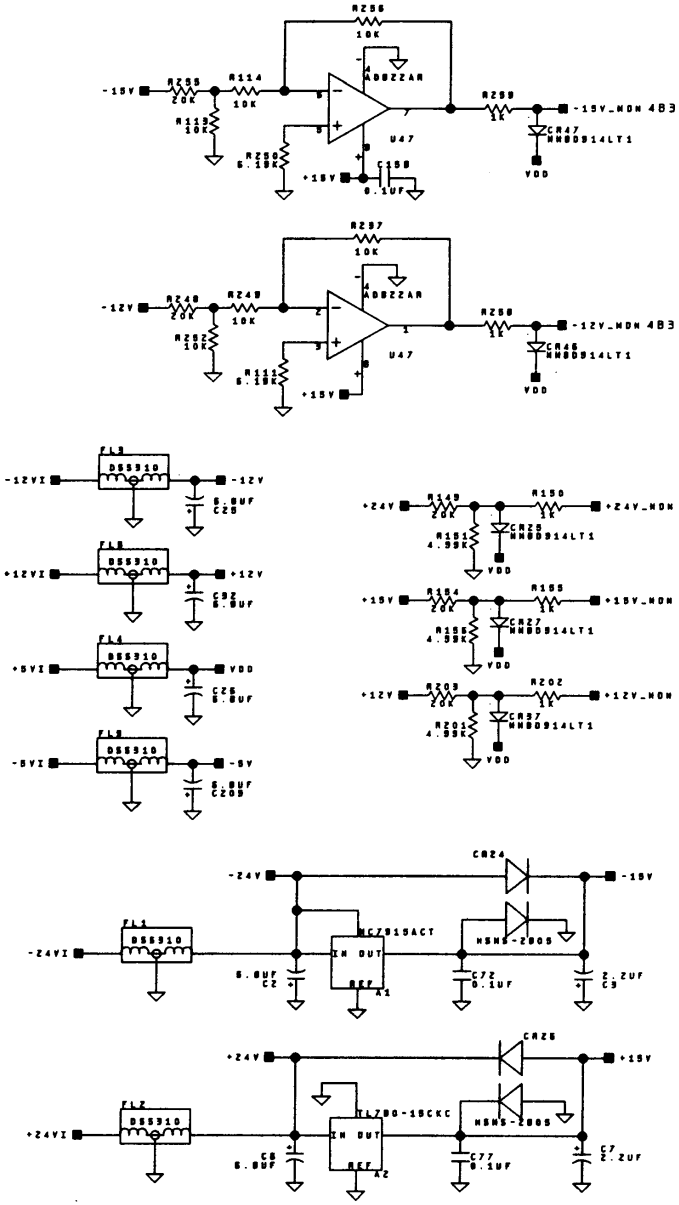

VXI BACKPLANE

VXI RUBIDIUM FREQUENCY STANDARD	A	35029	C
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.	SIZE	SHT 2 OF 13	REV

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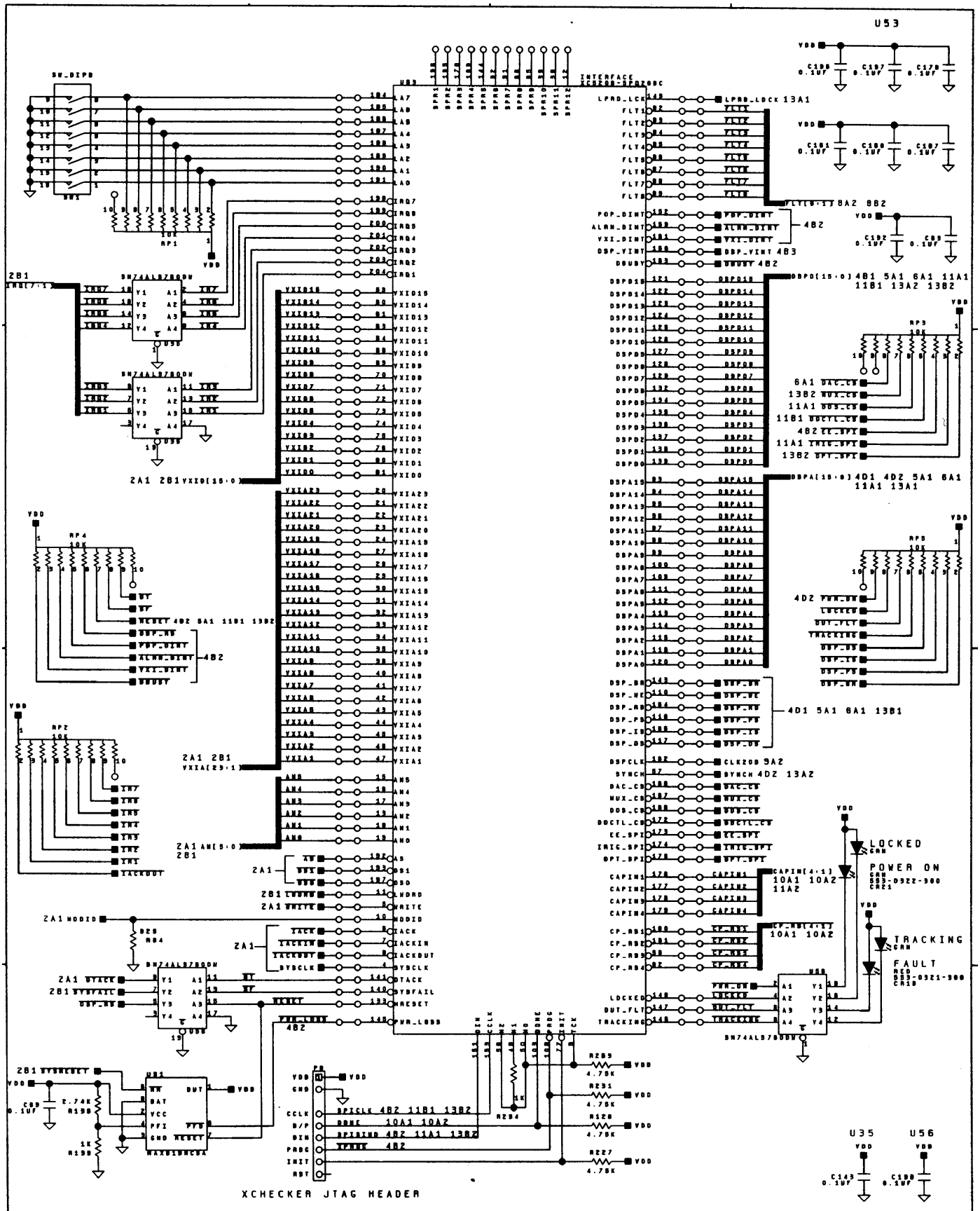
U53
SW_DIPB
INTERFACE XC9536-5PC44
LPRB_LDCK 13A1
4B2
4B3
4B2
4B1 5A1 6A1 11A1 11B1 13A2 13B2
4D1 4D2 5A1 6A1 11A1 13A1
4D1 5A1 6A1 13B1
CLK20B 9A2
SYNCH 4D2 13A2
CAPIN[4:1] 10A1 10A2 11A2
10A1 10A2
LOCKED
GRN
POWER ON
GRN
595-0922-300
CR21
TRACKING
GRN
FAULT
RED
595-0321-300
CR19
XCHECKER JTAG HEADER
U35
U56
INTERFACE FPGA
VXI RUBIDIUM FREQUENCY STANDARD
A
35029
C
SHT 3 OF 13
REV
SIZE

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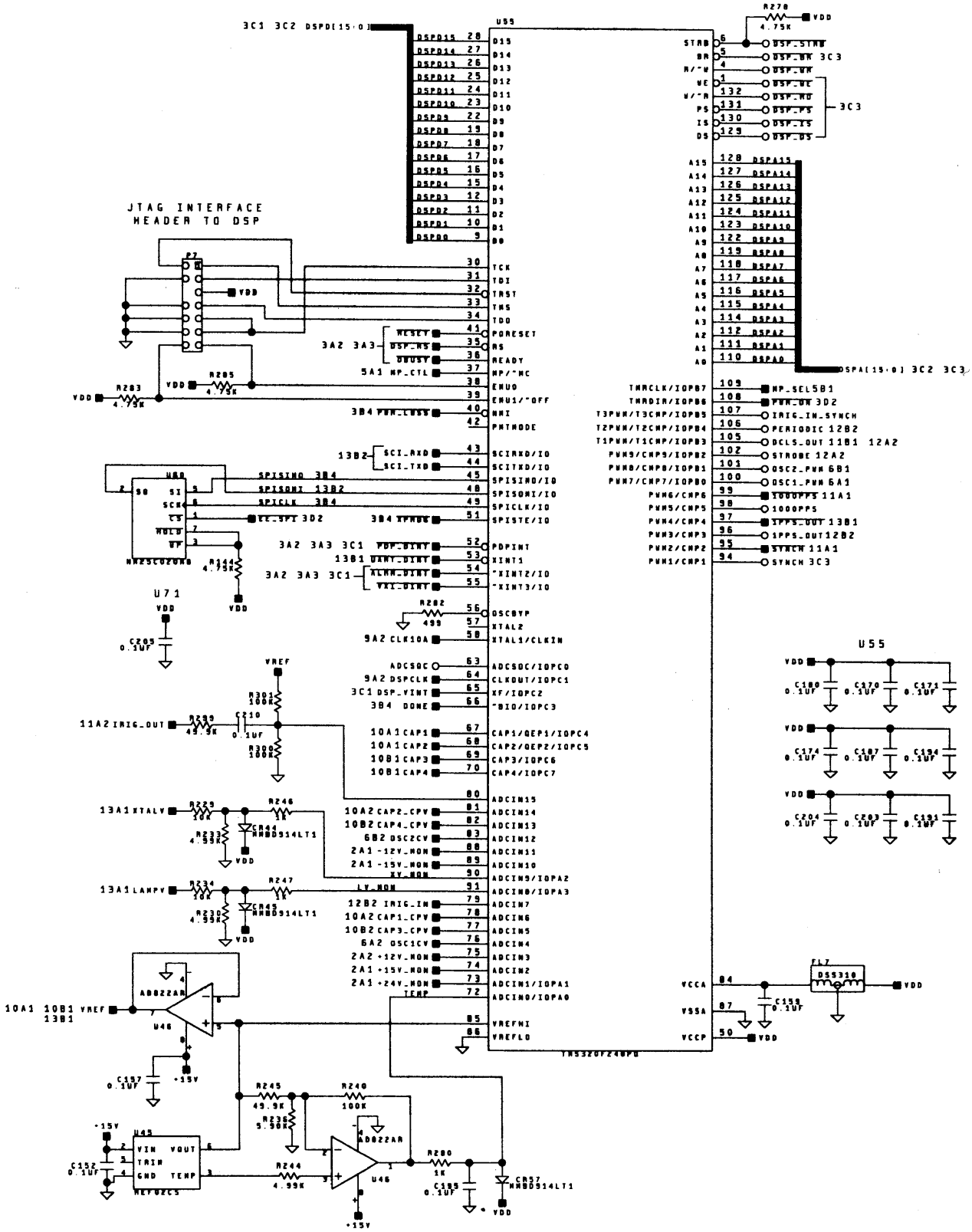
JTAG INTERFACE
HEADER TO DSP
U55
U71
U55
DSP PROCESSOR
VXI RUBIDIUM FREQUENCY STANDARD
A
35029
C
SIZE
SHT 4 OF 13
REV

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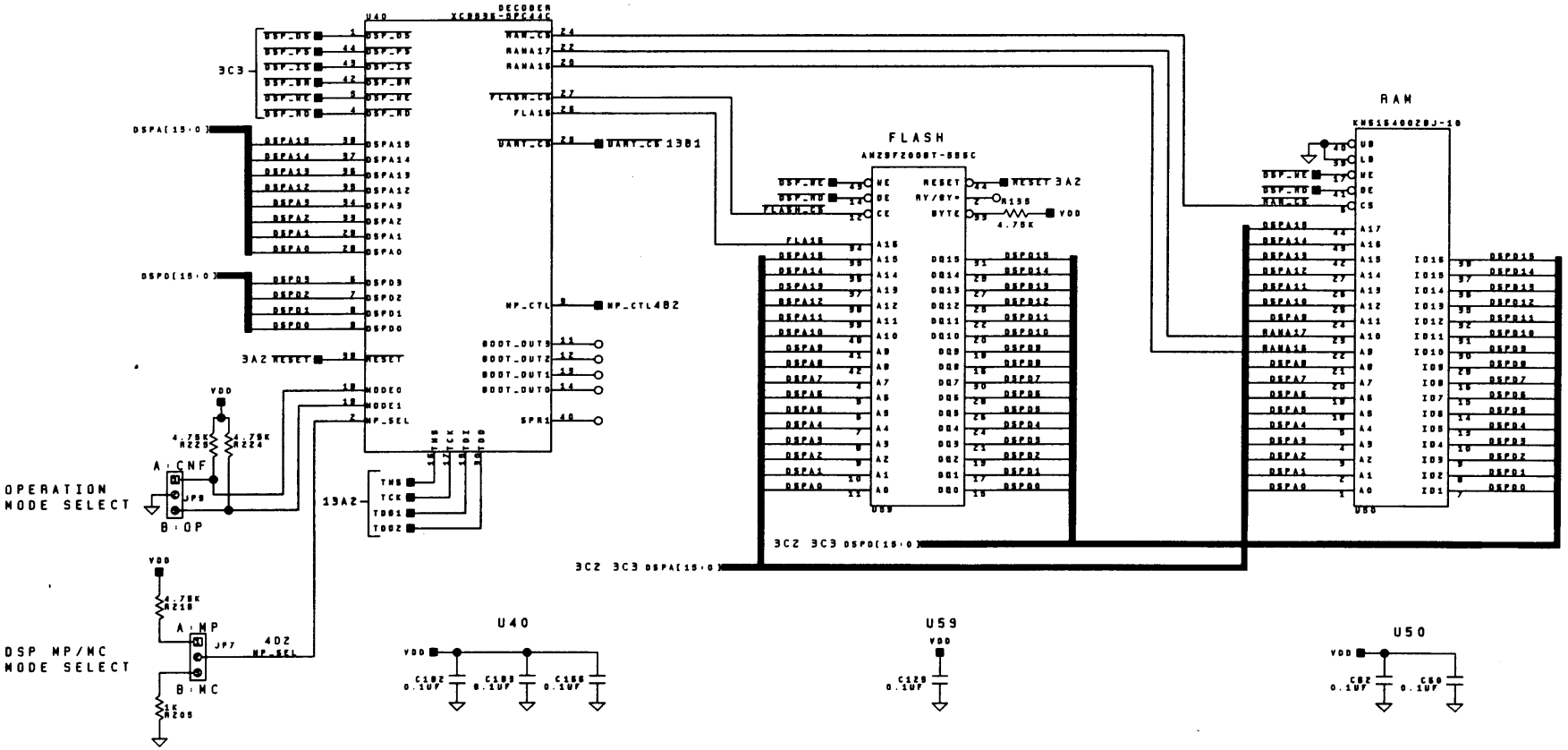

MEMORY

VXI RUBIDIUM FREQUENCY STANDARD	A	35029	C
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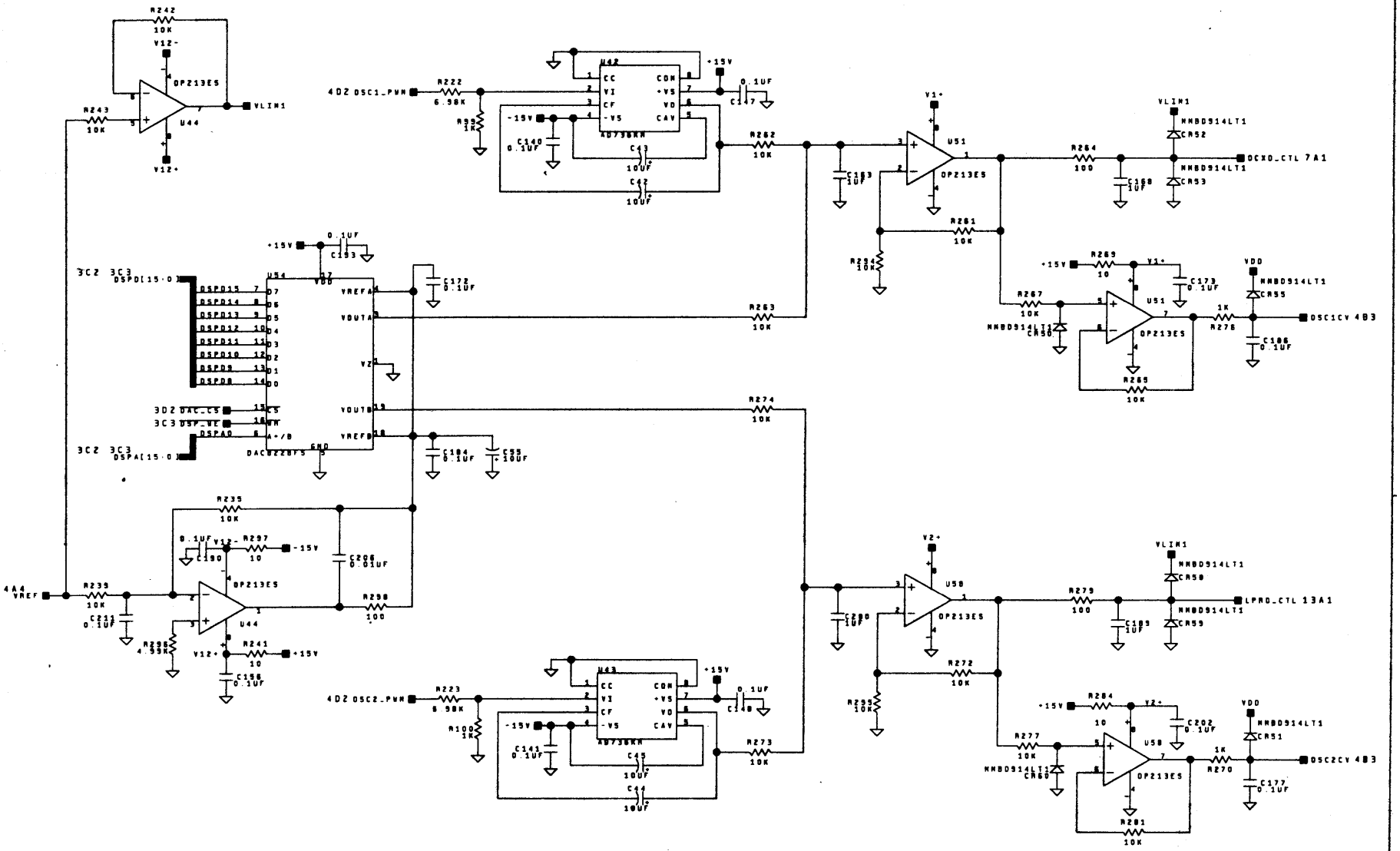

OSCILLATOR CONTROL

VXI RUBIDIUM FREQUENCY STANDARD	A	35029	C
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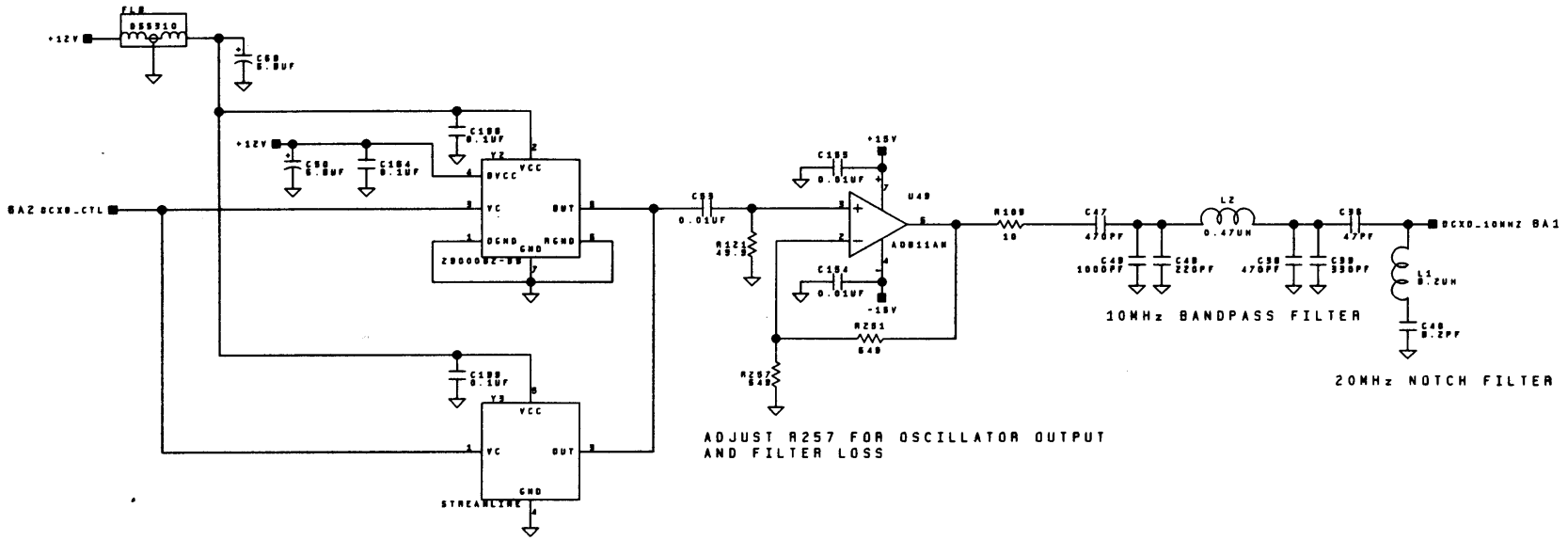
+12V
FL8
C58
0.1UF
+12V
C188
0.1UF
C50
0.1UF
C164
0.1UF
VCC
8VCC
VC
OUT
DGND
RGND
GND
Z9000-99
BAZ OCXO_CTL
C199
0.1UF
Y3
VCC
VC
OUT
GND
STREAMLINE
C53
0.01UF
R121
49.9
+15V
C185
0.01UF
U49
AD811AH
C184
0.01UF
-15V
RZ61
649
RZ57
649
R169
10
C47
470PF
C49
1000PF
C48
220PF
LZ
0.47UH
C39
470PF
C38
330PF
C36
47PF
L1
0.12UH
C40
8.2PF
OCXO_10MHZ BA1
10MHz BANDPASS FILTER
20MHz NOTCH FILTER
ADJUST R257 FOR OSCILLATOR OUTPUT
AND FILTER LOSS
INSTALL EITHER:
Y3, C199
OR
Y2, C50, C164, C188

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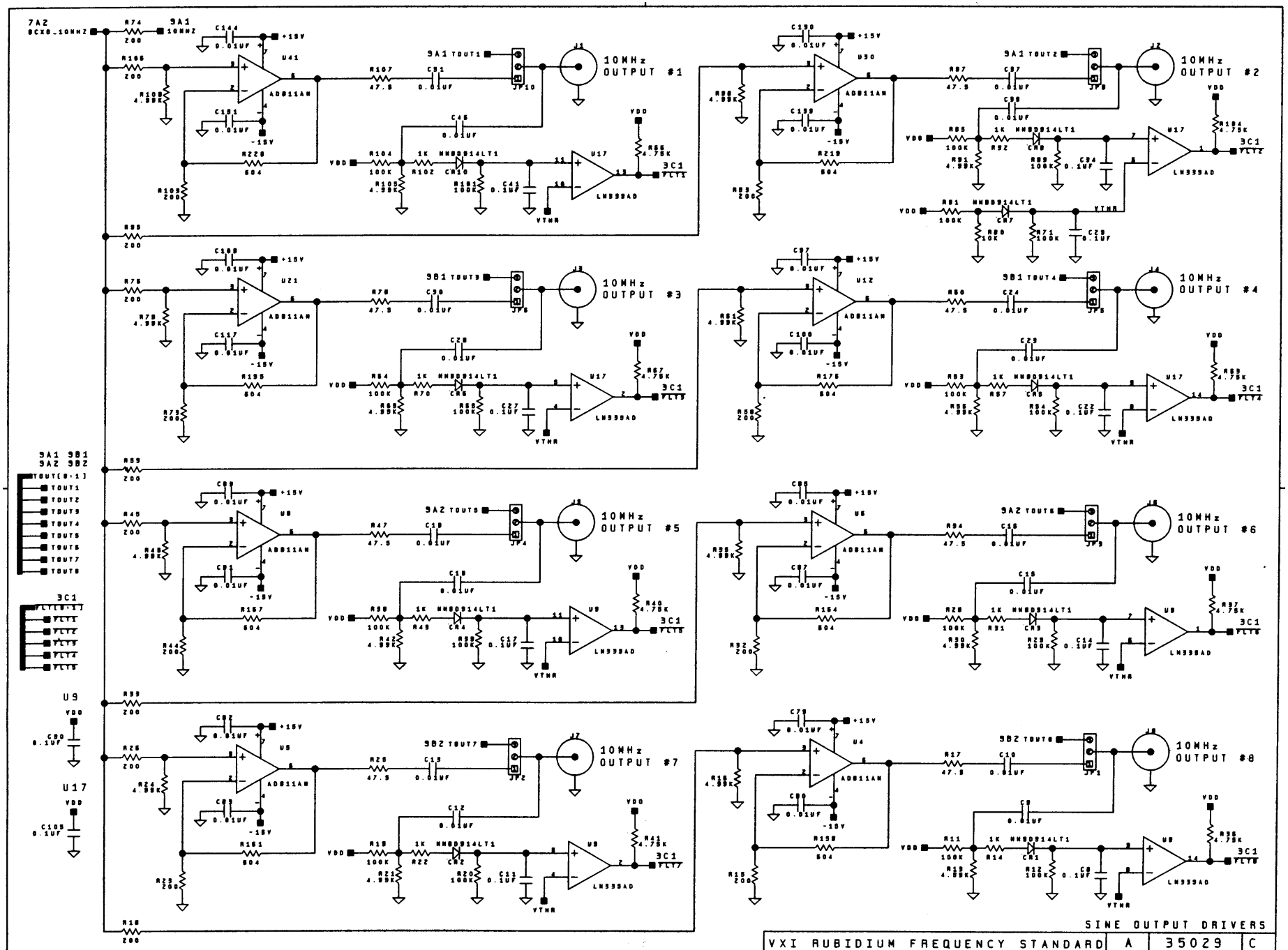
10MHz OUTPUT #1
10MHz OUTPUT #2
10MHz OUTPUT #3
10MHz OUTPUT #4
10MHz OUTPUT #5
10MHz OUTPUT #6
10MHz OUTPUT #7
10MHz OUTPUT #8
AD811AN
LM339AD
MMBD914LT1
SINE OUTPUT DRIVERS
VXI RUBIDIUM FREQUENCY STANDARD
A
35029
C
SIZE
SHT 8 OF 13
REV

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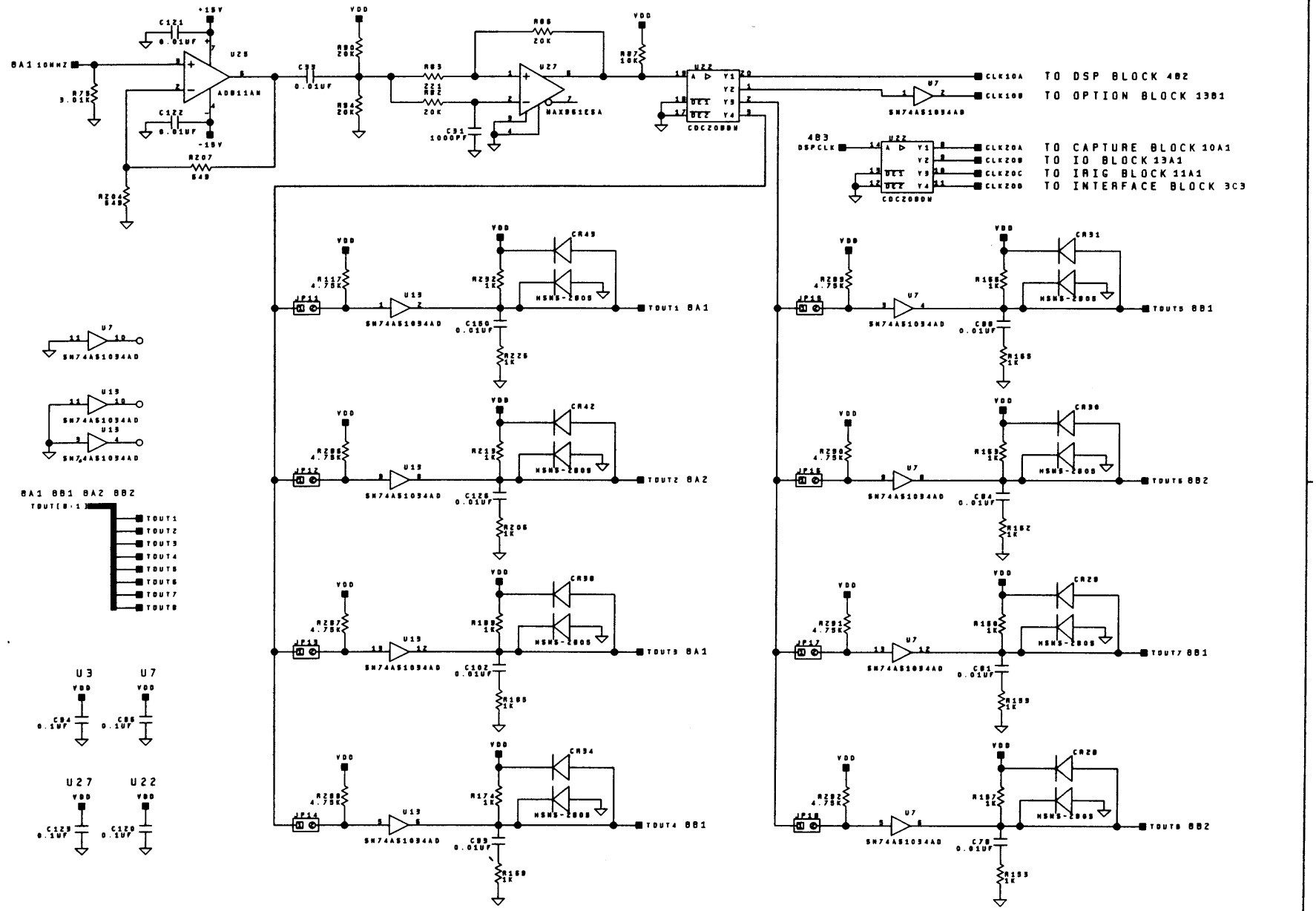
8A1 10MHZ
+15V
-15V
VDD
U26
AD811AN
U27
MAX961ESA
U22
CDC2088W
R85
20K
R87
10K
C91
1000PF
CLK10A TO DSP BLOCK 4B2
CLK10B TO OPTION BLOCK 13B1
SN74AS1034AD
4B3
DSPCLK
CLK20A TO CAPTURE BLOCK 10A1
CLK20B TO IO BLOCK 13A1
CLK20C TO IRIG BLOCK 11A1
CLK20D TO INTERFACE BLOCK 3C3
8A1 8B1 8A2 8B2
TOUT(8:1)
TOUT1
TOUT2
TOUT3
TOUT4
TOUT5
TOUT6
TOUT7
TOUT8
U3
U7
U27
U22
HSMS-2805
TOUT1 8A1
TOUT2 8A2
TOUT3 8A1
TOUT4 8B1
TOUT5 8B1
TOUT6 8B2
TOUT7 8B1
TOUT8 8B2
TTL OUTPUT DRIVERS
VXI RUBIDIUM FREQUENCY STANDARD
A
35029
C
SIZE
SHT 9 OF 13
REV

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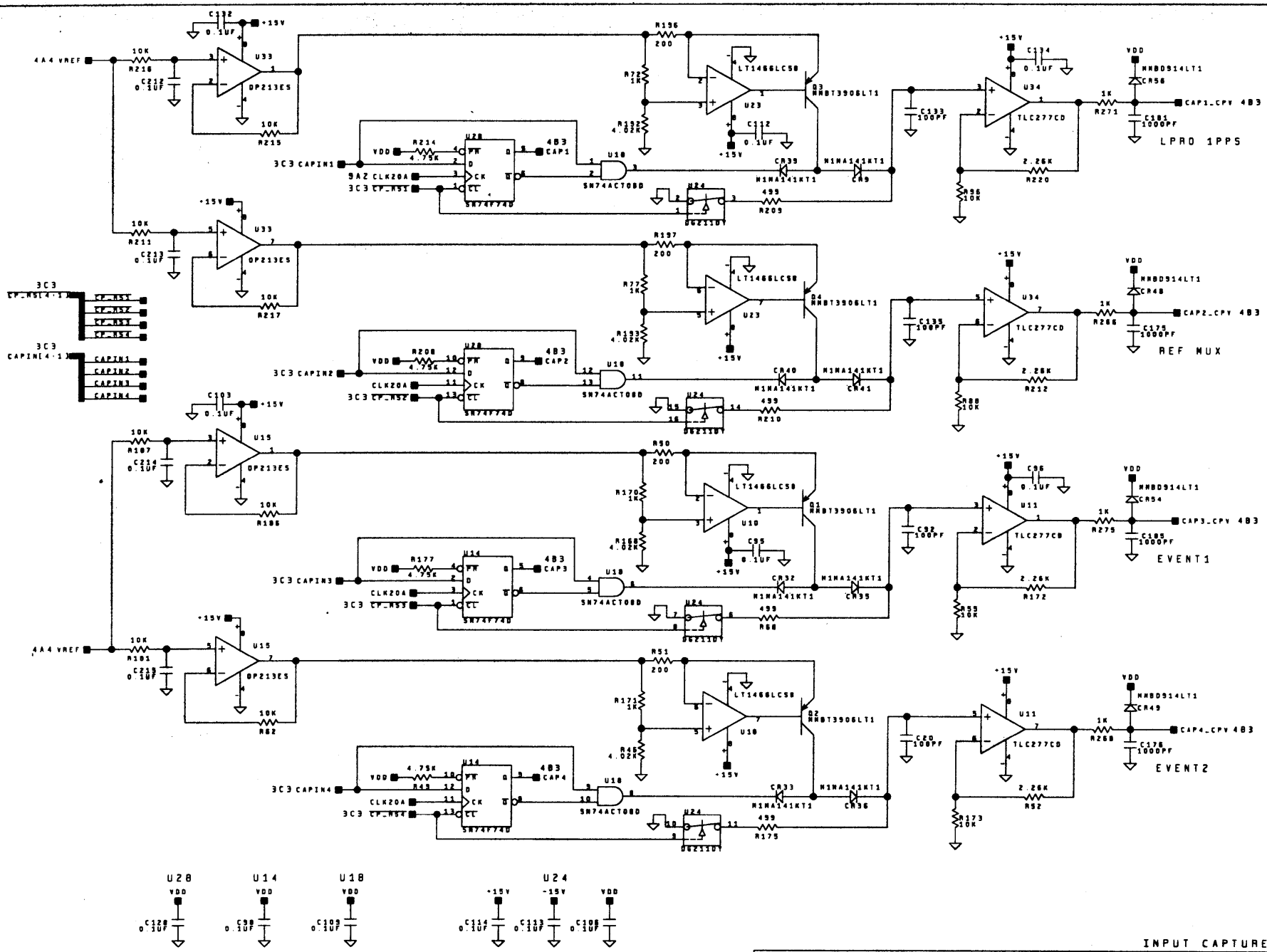
LPRO 1PPS
REF MUX
EVENT1
EVENT2
INPUT CAPTURE
VXI RUBIDIUM FREQUENCY STANDARD
A
35029
C
SIZE
SHT 10 OF 13
REV

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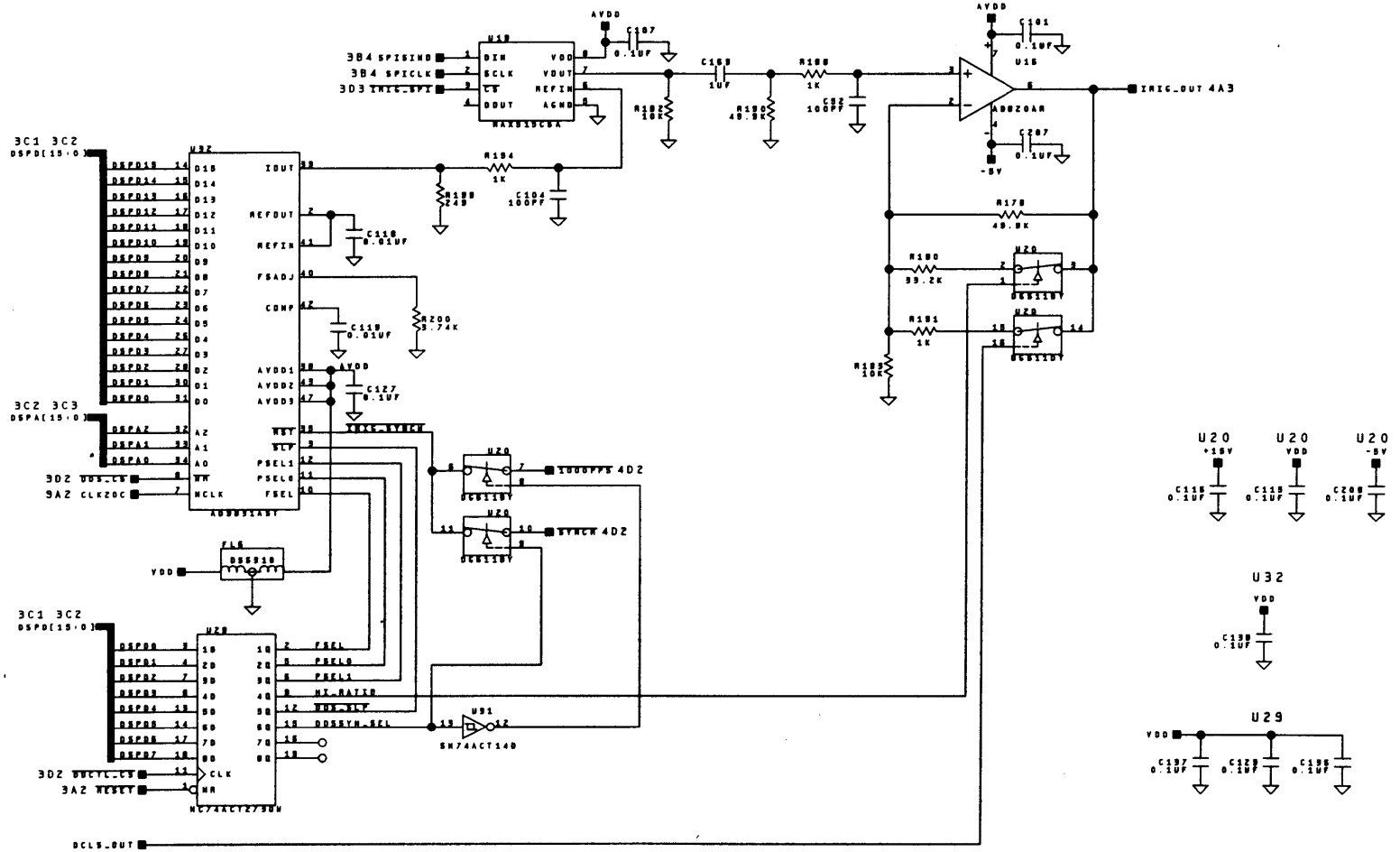

IRIG OUT GENERATOR

VXI RUBIDIUM FREQUENCY STANDARD	A	35029	C
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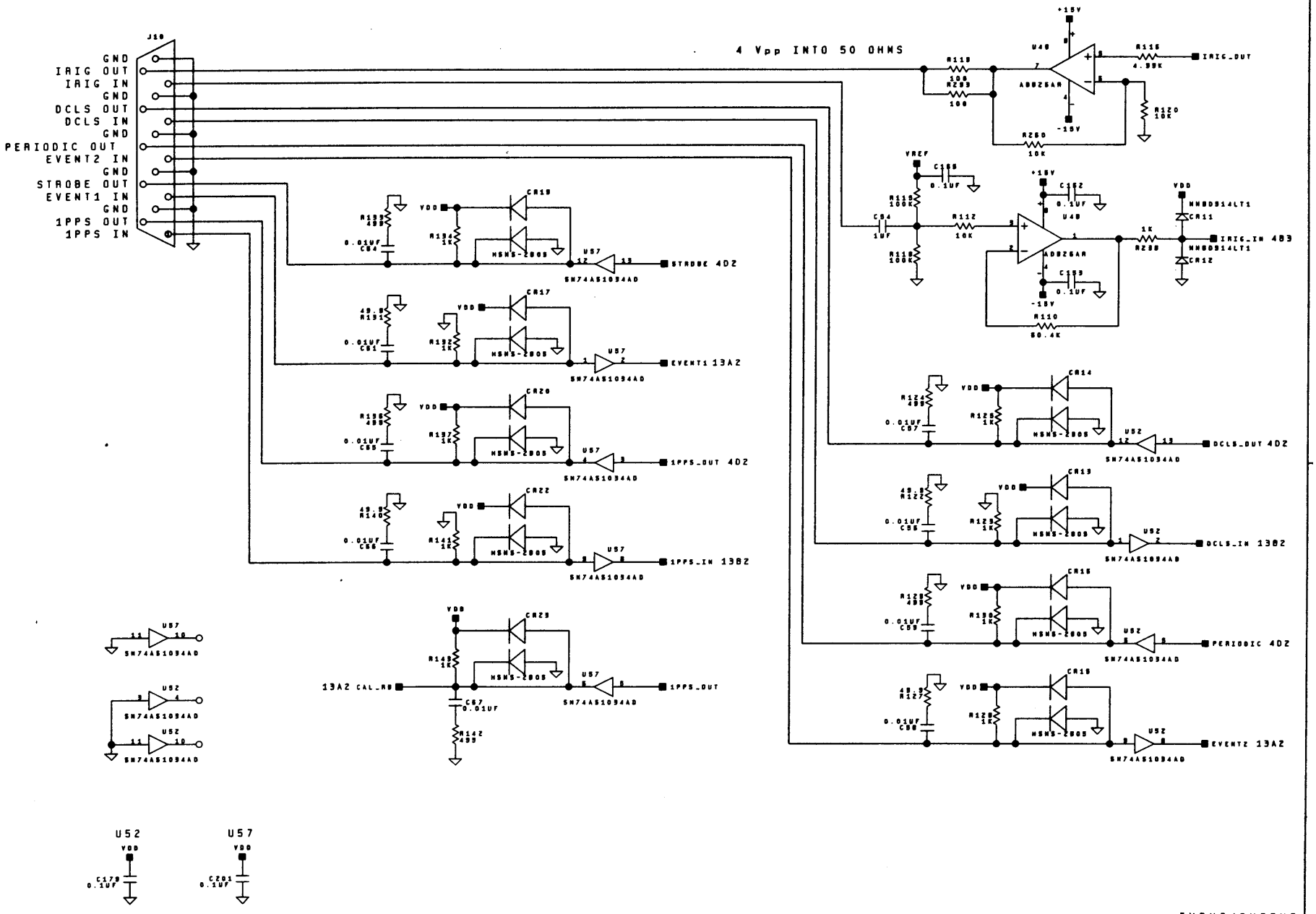

INPUT/OUTPUT

VXI RUBIDIUM FREQUENCY STANDARD	A	35029	C
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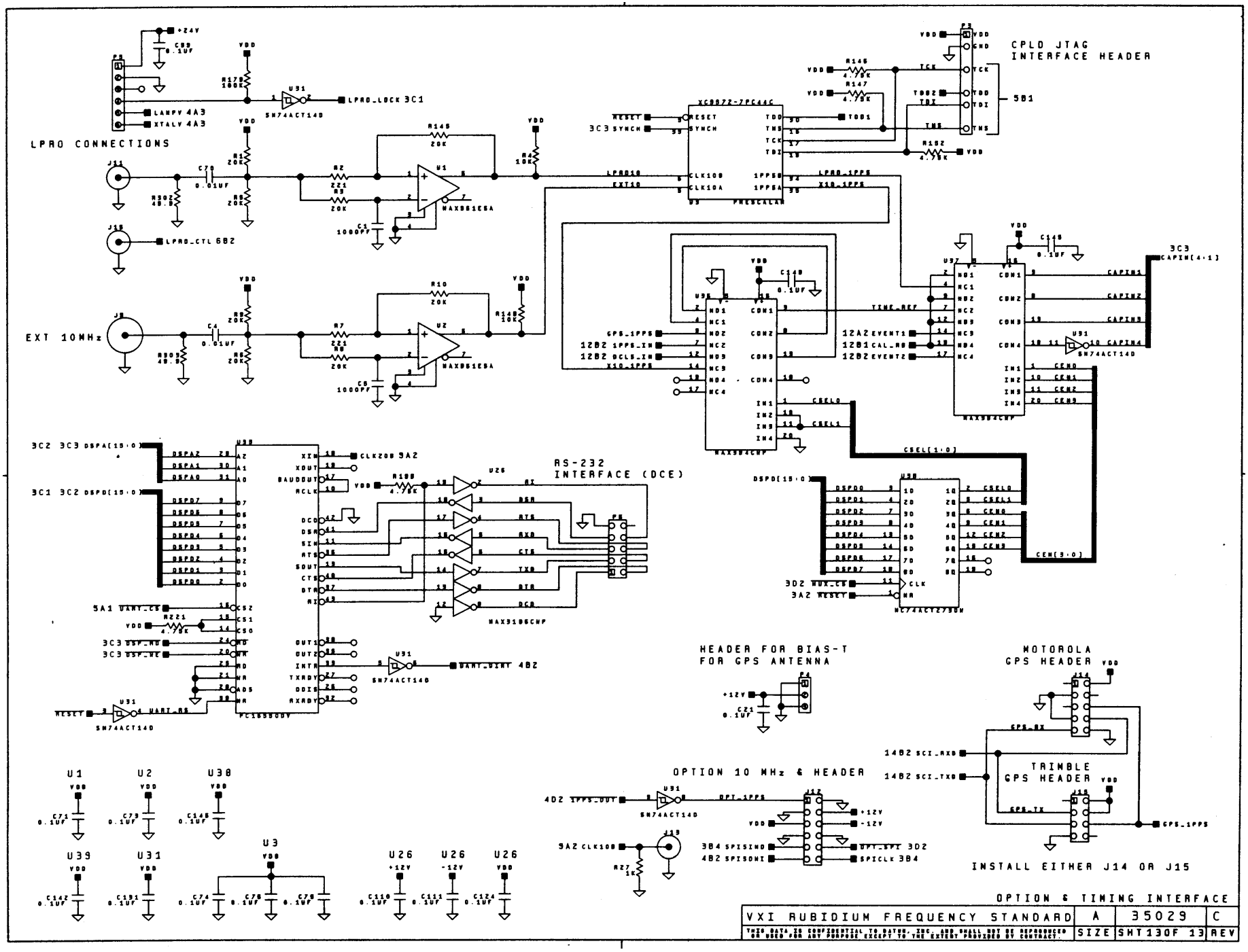

OPTION & TIMING INTERFACE

VXI RUBIDIUM FREQUENCY STANDARD	A	35029	C
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