thandar

# TF200 FREQUENCY METER

## SERVICE MANUAL

**CONTENTS**

## GENERAL

### Service Handling Precautions

Service work or recalibration should only be carried out by skilled engineers. Please note the following points before commencing work.

The tracks on the printed circuit board are very fine and may lift if subjected to excessive heat. Use only a miniature temperature controlled soldering iron and remove all solder (on both sides of the joint) with solder wick or suction before attempting to remove a component.

The integrated circuits IC1 to IC12 are CMOS devices and care should be taken when handling to avoid damage by static discharge.

### Dismantling the instrument

1. Invert the instrument and remove the 4 rubber feet.

2. Remove the 4 recessed and one surface screw.

3. Holding the case upper and lower together, turn the instrument the right way up and lift off the top, ensuring that the jack socket stays with the lower half of the instrument.

4. If further dismantling is required to replace components, proceed as follows.

   Remove the batteries and remove the two screws in the battery compartment; lift out the battery carrier.

   Remove the two countersunk screws that hold the battery carrier restraint and pcb to the case lower and remove the constraint. Remove the two other pcb retaining screws at the sides of the board.

   The complete pcb assembly can then be lifted out with the rear panel and front panel still attached, though these can be removed if necessary by de-soldering the appropriate connections and in the case of the front panel by unscrewing the nut holding the earthing strip to the pcb stud.

5. Reassemble in the reverse order.

Note: It is essential that if testing is carried out with the instrument sitting on a ground plane (which will minimise any noise pick-up) then the earthing spring must make contact to that ground plane (as it does in the cased instrument) otherwise sensitivity will be worsened.

### Calibration

It is not necessary to dismantle the instrument for recalibration only, see Calibration section.

## TECHNICAL SPECIFICATION

### FUNCTIONS

#### Lo Frequency

| | |
|---|---|
| Input | Socket A |
| Frequency Range | 10Hz to at least 20MHz |
| Gate Times | 0.01 to 100 secs in 5 decade steps. |
| Readout | kHz |
| Resolution | 100Hz to 0.01Hz in step with gate times of 0.01 to 100 secs. |
| Accuracy | ± (1 count + timebase accuracy). |

#### Hi Frequency

| | |
|---|---|
| Input | Socket B |
| Frequency Range | 15MHz-200MHz |
| Gate Times | 0.01 to 100 secs in 5 decade steps |
| Readout | kHz |
| Resolution | 1kHz to 0.1Hz in step with gate times of 0.01 to 100 secs. |
| Accuracy | ± (1 count + timebase accuracy). |

#### Time Average Period

| | |
|---|---|
| Input | Socket A |
| Frequency Range | 10Hz-1.5MHz |
| Minimum Pulse Width | 200ns |
| Number of periods averaged | 10-100K in decade steps |
| Readout | µs |
| Resolution | $\frac{1}{\text{(No. of periods averaged)}}$ µs |
| Accuracy | $\pm \left[1 \text{ count} + \text{timebase accuracy} + \frac{\text{trigger error}}{\text{No. of periods averaged}}\right]$ |

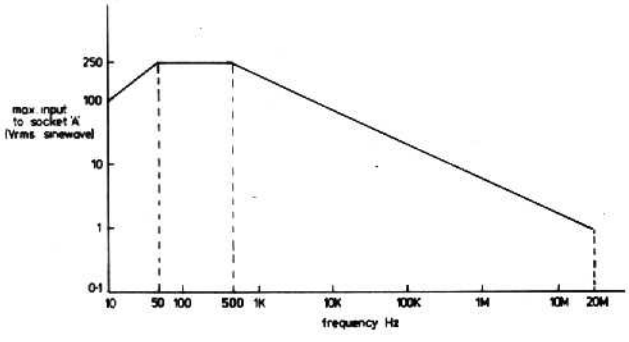
#### Totalise

| | |
|---|---|
| Input | Socket A |
| Counter Range | $10^8$ + overflow |
| Frequency Range | 10Hz-20MHz |

### INPUTS

#### Socket A

| | |
|---|---|
| Input impedance | 1M // < 25pF |
| Frequency Range | 10Hz to at least 20MHz |
| Sensitivity | 10mV rms sinewave 20Hz-20MHz, 20mv rms sinewave 10Hz-20Hz. |
| Attenuation | AGC from 10mV rms to approx. 350mV rms. then diode clipping. |
| Maximum permissible input voltage | 100VDC, 250V rms 50Hz; for other frequencies see graph. |




Trigger error (relevant to time-average period measurements only) $< \left[\frac{2.8}{\text{Signal slope (V/µs)}}\right]$ ns for 20dB S/N ratio

#### Socket B

| | |
|---|---|
| Input impedance | 50Ω nominal |
| Frequency range | 15MHz to at least 200MHz |
| Sensitivity from 50Ω source | 10mV rms sinewave 15-100MHz; 30mV rms sinewave 100-200MHz. |
| Dynamic Range | 40dB (10mVrms-1Vrms) |
| Maximum permissible input voltage | 100V DC, 250Vrms 50Hz, 1Vrms 15MHz- 200MHz |

### TIMEBASE

| | |
|---|---|
| Crystal Oscillator frequency | 4MHz |
| Initial oscillator adjustment error | < ± .3ppm at temperature specified on QA label. |
| Oscillator temperature coefficient | Typical oscillator stability better than ± 3ppm 18°C to 28°C, ± 10ppm–20°C to 70°C. |
| Oscillator ageing rate | <±10ppm per year |
| Internal clock | 1MHz (divided down from 4MHz) |
| Timebase | 0.01s to 100s in decade steps |

Time between measurements

| | |
|---|---|
| i) Frequency | 400ms |
| ii) Time average period | 400ms + <1 input period |

### GENERAL

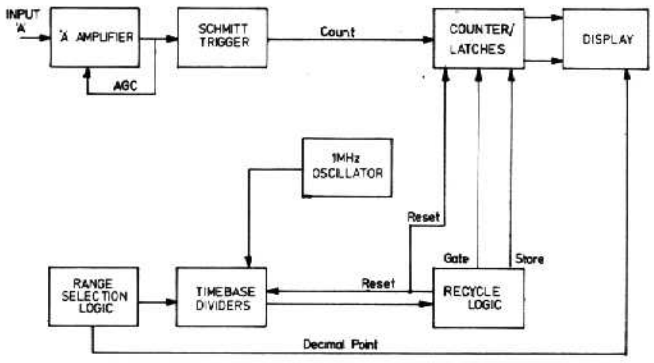
| | |
|---|---|
| **External Clock** | Rear panel socket and switch for internal 1MHz out, or external 1MHz reference in. |
| Input voltage range | 2V to 5V peak to peak sinewave or squarewave. |
| Maximum permissible input voltage | 50VDC, 30Vrms |
| **Current Drain** | 20–42mA depending on range selected and input frequency. Maximum of 42mA applies to A range with 20MHz input,or B range with no input. |
| **Battery Life** | Typically 150-200 hours (6 alkaline 'C' cells)depending on rangeselected. |
| **Minimum working voltage** | 6.0V. Typical life remaining after low battery indicator lights:8 hours. |
| **Overflow indication** | ◀ shown in display when the measurement in progress or the displayed information exceeds $10^8$. |
| **Gate Open Indication** | 'Gate' shown in display. |
| **Reset Button** | Resets display to zero and counter logic to start of new gate period in all modes. Reset cycle time < 800ms |
| **Environmental Operating Range** | 5°C to 40°C, 20% to 80% RH |
| **Environmental Storage Range** | –40°C to +60°C (with alkaline batteries), < 75% RH |

### MECHANICAL

| | |
|---|---|
| **Case size** | 255 x 150 x 50mm |
| **Weight** | Excluding batteries, 800gms. Including alkaline batteries,1200gms |

## FUNCTIONAL DESCRIPTION

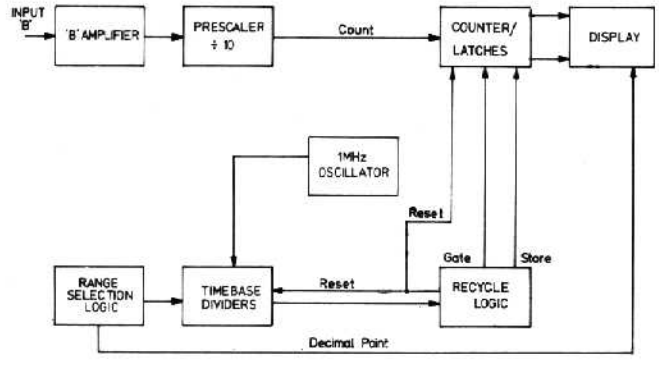
### Low Frequency Mode




The signal at input A is amplified, then squared by the Schmitt trigger and passed to the counter. The counter is enabled by the Gate signal for an accurate time determined by the timebase dividers and the range selection logic. At the end of this time the counter is disabled and Store and Reset signals are generated by the recycle logic to store the accumulated count in the latches and to reset the counter and timebase dividers. The display will show the updated count held by the latches.

If the counter is enabled for t seconds and the input to A is f Hz, the display will read t x f. By positioning the decimal point with the range selection logic the readout is automatically given in kHz. Hence if a 10 second gate time is selected, a 2MHz signal applied to input A will result in a display reading of $2 \times 10^6 \times 10$ or 20000000. The decimal point will be positioned by the range selection logic to read 2000.0000 kHz.

### High Frequency Mode

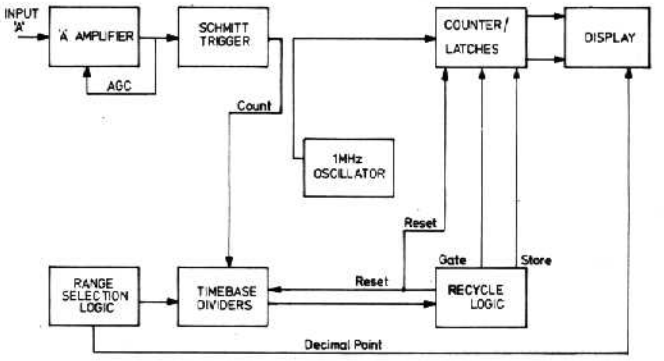



The signal at input B is amplified then divided by 10 before being passed to the counter. The rest of the operation is the same as for the low frequency mode already described.

If the counter is enabled for t seconds and the input to B is f Hz the display will read $\frac{t \times f}{10}$. The decimal point must therefore be positioned one place further to the right to compensate for the extra divide by 10 of the prescaler; this is accomplished by the range selection logic.

### Time Average Period Mode

The signal from input A is amplified, then squared by the Schmitt trigger to give the Count signal as before. It is then passed to the timebase divider, the 1MHz clock signal being

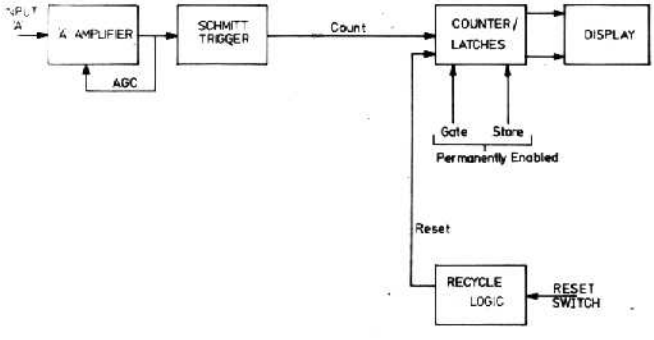



passed to the counter. The counter is enabled by the Gate signal from the recycle logic for a multiple of 10 input periods, the actual multiple being selected by the range selection logic. At the end of this time, the counter is disabled, the display latches updated and the counter and timebase dividers reset as before.

As the counter has been incremented once every 1µS by the 1MHz oscillator the display will read the time in µS that the selected multiple of 10 input periods has spanned.

If the input at A is f Hz and the multiple selected is $10^n$ the display will read $\frac{10^n}{f} \times 10^6$ µS. To allow the display to read the time for one period at the A input, the decimal point must be positioned to divide this readout by $10^n$; this is achieved by the range selection logic. Hence a 200Hz signal applied to input A and a multiple of $10^3$ periods averaged will result in a display reading of $\frac{10^3}{200} \times 10^6$ or 5000000. With the decimal point positioned to divide by $10^3$ the result will be 5000.000µS i.e. the time for one period of the 200Hz input signal.

### Totalise Mode




In this mode the signal at input A is amplified and squared as before and passed to the counter. The Gate and Store signals are held active to permanently enable the counter and allow the count to pass directly to the latches and display. The result is that the display reads the total number of counts seen at input A. The reset switch can be used to generate the Reset signal to clear the counter and display.

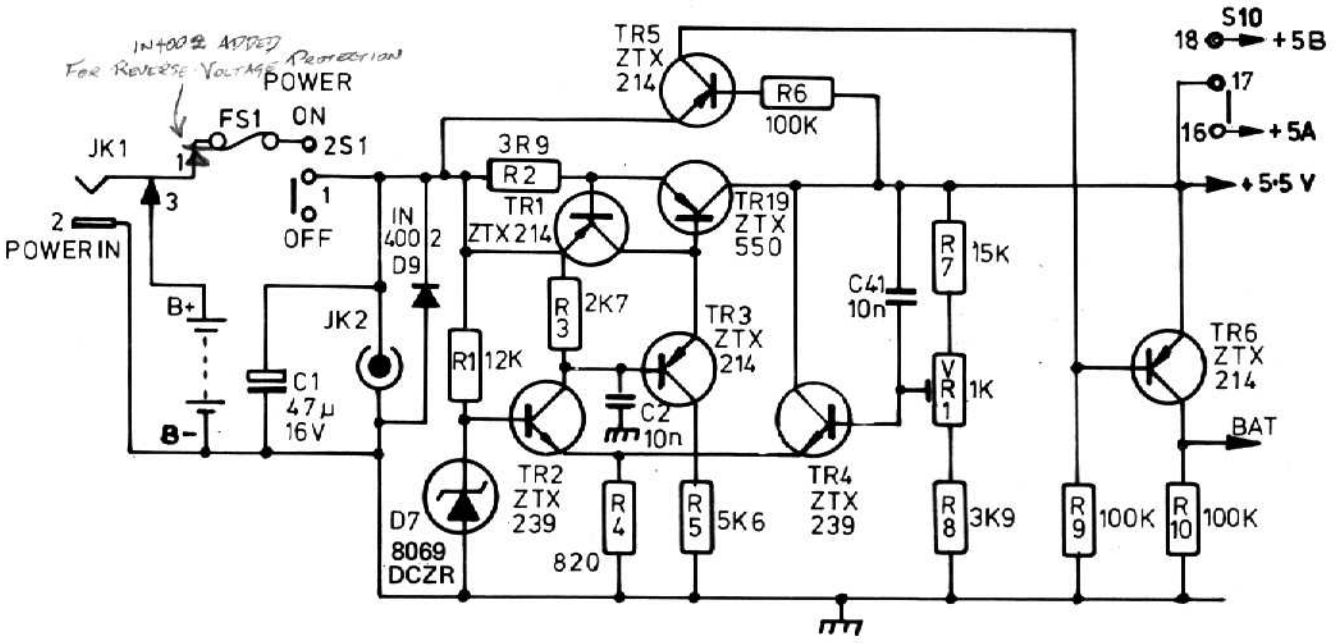
## CIRCUIT DESCRIPTIONS

Note that in the following descriptions:

LOW = LOGIC '0' = 0V
HIGH = LOGIC '1' = 5V

The convention adopted in naming logic signals is to call the Q output of a bistable 'NAME', and the $\overline{Q}$ output 'NAME' and elsewhere to use 'NAME' for the inverse of a signal called 'NAME'. This convention does not imply that inputs of I.C.s receiving NAME signals are active when LOW; the text describes whether the input is active in the HIGH or the LOW state.

### Power Supply




Power is supplied either from the batteries or external AC adaptor via JK1. C1 decouples out low frequencies e.g. mains ripple. The protection diode D9 prevents damage to the components by limiting the reverse voltage across them, should the instrument be switched on with batteries or external power source reversed. However, the high current that can flow in this condition, particularly with alkaline cells, may cause the printed circuit board fuseable link, FS1, to blow. If this happened the link should be repaired with a single strand of 0.1mm (40swg) tinned copper wire.

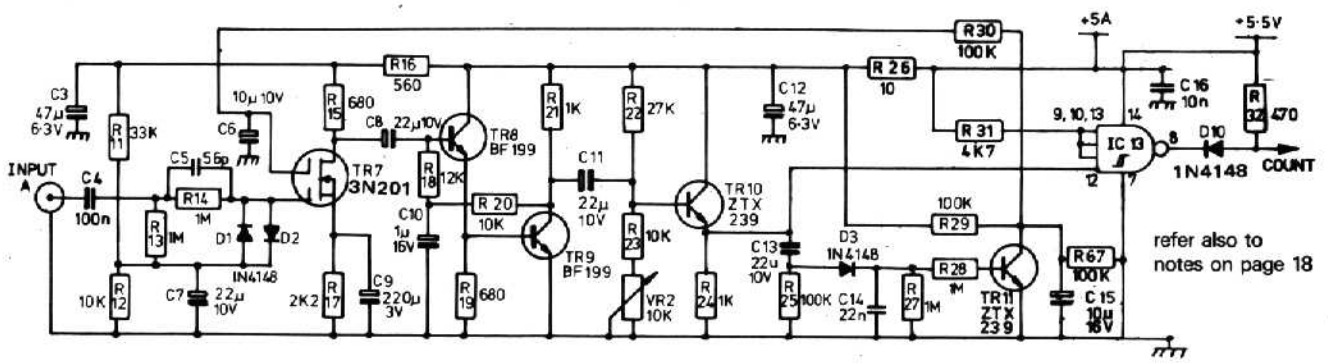
The regulator consists of a precision reference diode D7 (1.225V nominal) connected to one input of the long tail pair amplifier TR2, TR4. The other input is fed with a proportion of the regulated output via R7, R8 and VR1. VR1 is used to set the regulated output to 5.55V ± 0.01V. The collector of TR2 drives the base of emitter follower TR3 which drives the output transistor TR19. It is unconventional in that TR3 collector is not connected to TR19 collector. This is to reduce the voltage drop across the regulator and allow correct operation down to very low unregulated voltages (approximately 5.8V for Vcc = 5.55V).

TR1 and R2 form a current limiting circuit which operates at 200mA nominal to protect against accidental short circuits.

TR5 monitors the voltage across the regulator transistor and R2. When this voltage drops below 0.7V nominal TR5 turns off, allowing TR6 to draw base current through R9, thus turning TR6 on, causing the BAT signal to go high and turn on the low battery indicator on the display.

To minimise current drain, power is only supplied to the B amplifier when required, i.e. in the High Frequency mode and only to the A amplifier in all other modes i.e. Low Frequency, Time Average Period, and Totalise. Switching is accomplished by S10 (the High Frequency function switch), and the two switched supply rails are referred to as +5A and +5B for the A and B amplifiers respectively. All other parts of the circuit are supplied direct from the +5.55V rail at all times.

## Low Frequency Amplifier




The purpose of this amplifier is to take input signals of any wave shape and convert them to logic levels (OV and +5V) so that they may be counted accurately by the logic circuits. The amplifier handles signals in the range 10Hz to 20MHz.

The input signal is passed from the BNC socket, through isolating capacitor C4, and the parallel combination of R14, C5, to the signal gate of TR7. Resistors R11, R12 set the bias level on the control gate to +2V nominal. R13 defines the input impedance. R14, D1 and D2 provide protection against large signals, the maximum peak to peak swing on the control gate being limited to 1.2V nominal. C5 is necessary to compensate for the high frequency roll-off caused by R14 and the input capacitance of TR7.

In the absence of an input signal large enough to cause AGC the control gate of TR7 is held at approximately mid-rail, this being the condition for maximum gain. Pulling the control gate down towards the OV rail will reduce the gain of TR7 and hence the overall gain of the amplifier. This voltage is controlled by TR11 via R30, the AGC line being decoupled by C6 and C15.

R17 sets the channel current of TR7 to 1mA nominal and is by-passed by C9. The inversion of the input signal - either larger or smaller - is then seen at the drain of TR7, and passed via C8 to the next stage TR8, TR9. These two transistors form a high gain - typically in excess of 80 times - inverting amplifier. The collector current of TR9 will be between 2 and 3.5mA depending on the HFE of the two devices. The emitter current of TR8 is fixed at 1mA nominal by R19.

Once in AGC the signal level on TR9 collector will be 2V peak to peak nominal. This signal is passed via C11 to the buffer stage TR10.

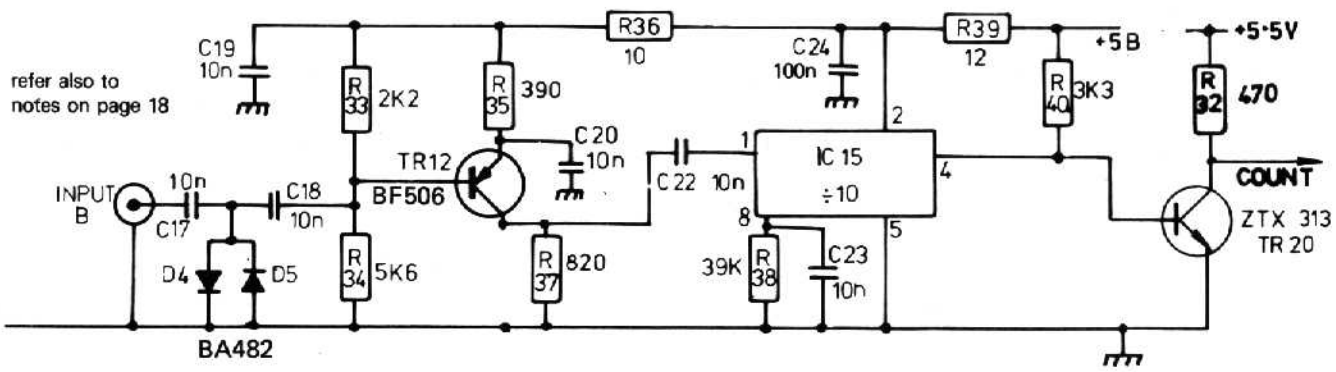
The purpose of TR10, and associated components, is to set the DC component of the amplified signal such that the hysteresis band of the Schmitt trigger IC13 is completely traversed by the peak to peak signal swing. This DC component is set by VR2 and should be adjusted with an input signal of approximately 20MHz at 9mV rms.

The output of IC13 is pulled up by R32 via D10 to give a 5V peak to peak square wave, the COUNT signal. When the B range is selected the A amplifier is turned off and IC13 output is permanently high because its input is pulled low by R24; D10 isolates the output of IC13 from TR20, the output of the B amplifier, so that IC13 output is not pulled low when TR20 goes low.

The output from TR10 is also passed to D3 via C13. D3 peak rectifies the signal and the DC level generated on C14 is passed via R28 to TR11 - the AGC amplifier. Hence as the output from TR10 increases so TR11 is turned on more pulling down the voltage applied to the control gate of TR7 and reducing the overall gain.

The +5A supply comes from the 5.55V rail via S10, and is decoupled by C16, R26, C12, R16 and C3 and fed to the various stages of the amplifier.

## High Frequency Amplifier and Prescaler



The purpose of this stage is the same as the low frequency amplifier, but the frequencies involved are higher i.e. 15MHz to 200MHz. Input signals are amplified and then divided by 10 to produce a frequency range of 1.5MHz to 20MHz to drive the same logic circuits as before.

The input signal is passed via C17 and C18 to the base of the amplifier transistor TR12. TR12 with R33, R34, R35, R37, C20 and L1 form a high frequency amplifier having a voltage gain of approximately 15dB at 200MHz and an input impedance close to 50 ohms. D4 and D5 protect the input against high voltages. The output from TR12 collector is passed via C22 to the input of the ECL prescaler IC15. The IC divides this input frequency by 10 and the divided signal—a square wave of 0.7V peak to peak—is passed to the buffer, TR20.

The +5B supply comes from the 5.5V rail via S10. The supply is decoupled by R39, C24, R36 and C19.

The collector of the buffer transistor TR20 is fed to the COUNT signal and shares the same load resistor R32, as the LF Schmitt trigger.

**Counter and Display**

IC1 and IC2 are LS1 devices each containing the following:

1. 4 decade counter
2. 4 x 4 bit latches
3. 4 BCD to 7 segment decoders
4. 28 liquid crystal display segment drivers
5. Oscillator used to generate the 128 Hz back plane signal
6. ½ digit/carry logic

The two devices are cascaded to provide 8 decades of count/display with overflow indication. To enable the counters in each device to count an input applied to pin 32, pin 31 must be held HIGH. Hence IC2 with COUNT applied to pin 32 will count only if $\overline{GATE}$ on pin 31 is HIGH. IC1 has pin 31 connected to Vcc (i.e. is permanently HIGH) and will always count the carry output of IC2, pin 28. This carry signal will be HIGH during the time that the most significant decade of IC2 is at '9'. The carry signal will go LOW when the most significant decade is counted from 9 to 0 and at this point IC1 is incremented by 1.

In both devices the 4 bit latches will be updated (i.e. loaded with the accumulated count) during the time that $\overline{STO}$ (Store signal) is LOW. All the counters, but not the latches, are cleared during the time that the $\overline{RST}$ (reset signal) is LOW. Hence by generating $\overline{STO}$ followed by $\overline{RST}$ the display will be updated from the decade counters and the counters reset ready for a new series of counts on pin 32 of IC2. See fig. a.

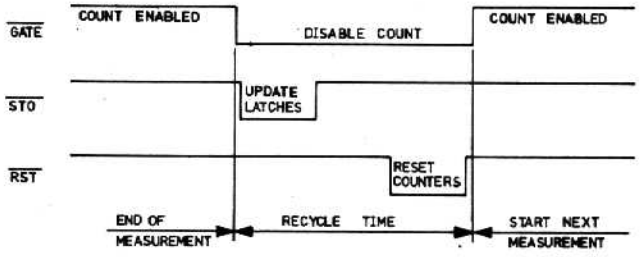



fig a.

Liquid crystal displays require that no DC component is present in the drive waveforms, hence they are driven by a common or Backplane signal (BP) which is a square wave of 5 V peak to peak at 128Hz nominal. To drive a segment a signal either in phase or in anti-phase with the BP is used. When BP and the drive are in phase the segment is inactive or off. When BP and the drive are in anti-phase the segment is active or on. See fig b.

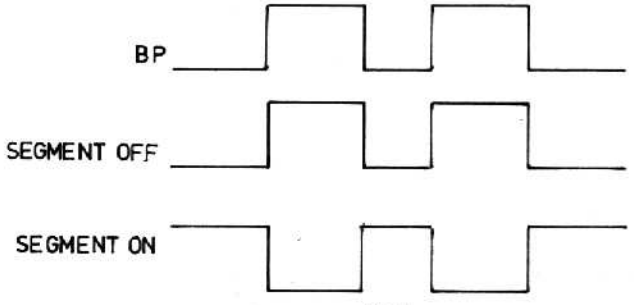
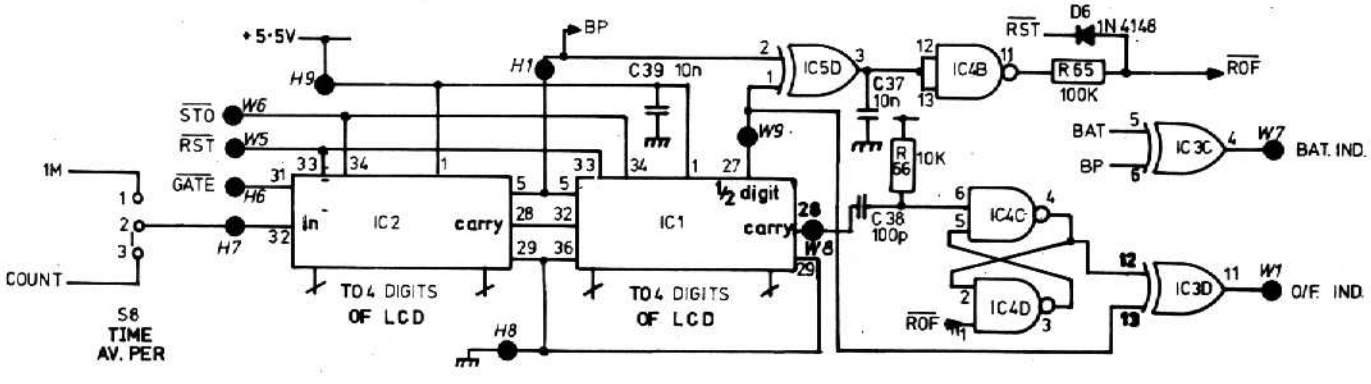



fig b.

The segments of all eight digits are driven in this way by IC1 and IC2; the decimal points and indicators, however, must be driven separately. To drive these "extra" segments, use is made of a logic function known as the Exclusive OR or XOR. The logic symbol and truth table are shown in fig c.


| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

fig c.



If the BP signal is applied to one input, it is possible to make the output either in phase or in anti-phase with BP by driving the other input either LOW or HIGH respectively. See fig d.

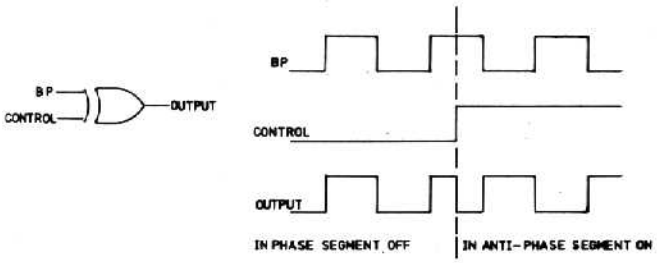



fig d.

All decimal points and indicators in the TF200 are driven in this way. Take for example the BAT IND (low battery indicator) from IC3C; when the BAT signal on pin 5 is LOW the indicator is off, and when the BAT signal goes HIGH the indicator is on. The BP signal is generated by IC1 and IC2 and comes from Pin 5.

The O/F IND (overflow indicator) from IC3D is a little more complicated but is essentially the same as above. The control input of IC3D is the set output from the overflow latch consisting of IC4C and IC4D. Pin 13 (the other input to IC3D) is not however, the BP signal. Pin 13 is fed from IC1 pin 27 - the ½ digit output. This output is really a display driver signal which will be in phase with BP at all times except when the display information (i.e. the contents of the latches in IC1) is in an overflow condition, when it will be in anti-phase with BP, i.e. $\overline{BP}$. The O/F IND can therefore be on either when IC4C output is HIGH and IC1 pin 27 is in phase with BP, or when IC4C output is LOW and IC1 pin 27 is in antiphase with BP, i.e. $\overline{BP}$; under all other combinations of conditions the O/F IND will be off. This apparent complication is to ensure that the O/F IND shows not only when the displayed count (held in the latches) has overflowed but also when the measurement in progress (i.e. the counters themselves) overflow, or both. The following further explanation should clarify the operation.

When the measurement in progress overflows, the HIGH to LOW transition of the carry output pulls IC4C pin 6 LOW momentarily via C38 and sets the output of the overflow latch, IC4C pin 4, HIGH. Since the ½ digit signal from IC1 pin 27 is in phase with BP because the displayed count held by the latches has not yet overflowed, the O/F IND is turned on. At the end of measurement the ½ digit display signal goes anti-phase with BP at the HIGH to LOW transition of $\overline{STO}$. At the same time, the overflow latch is reset by $\overline{ROF}$ (the reset overflow signal) going LOW as follows: Input pin 1 of IC5D, the ½ digit signal is now anti-phase with BP on the other input of IC5D; IC5D output therefore goes HIGH, forcing IC4B output LOW and pulling $\overline{ROF}$ LOW via R65. Thus IC3D pin 12 is now LOW, but ½-digit on pin 13 is now $\overline{BP}$, so IC3D pin 11 is still $\overline{BP}$ and the O/F IND remains on. This is shown in phase (i) of fig e.

When the measurement in progress again overflows during the next measurement cycle, the carry HIGH to LOW transition again tries to set the overflow latch via C38 but does not do so because $\overline{ROF}$ is still LOW and "clamps" the overflow latch in reset. This is shown in phase (ii) of fig e.

When a measurement cycle occurs which does not overflow the counters there is no carry signal and at the $\overline{STO}$ HIGH to LOW transition the ½ digit signal reverts to being in-phase with BP. The output of IC3D therefore becomes BP since the output of IC4C is still LOW and the O/F IND turns off. At the same time IC5D output goes LOW forcing IC4B output HIGH and $\overline{ROF}$ HIGH, removing the reset from the overflow latch. This is shown in phase (iii) of fig e.

The $\overline{ROF}$ line can also be pulled LOW by $\overline{RST}$ via D6. This at first appears unnecessary, but consider the possibility of the carry signal being high at the $\overline{STO}$ HIGH to LOW transition (at which point counting has been disabled), fig f. It can be seen that if $\overline{ROF}$ is not forced LOW during $\overline{RST}$ it is possible to set the overflow latch erroneously when carry goes from HIGH to LOW as the counters are reset by $\overline{RST}$. See fig f.

fig f.

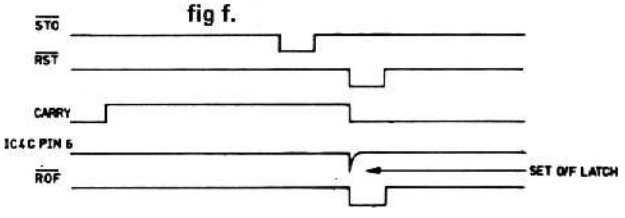
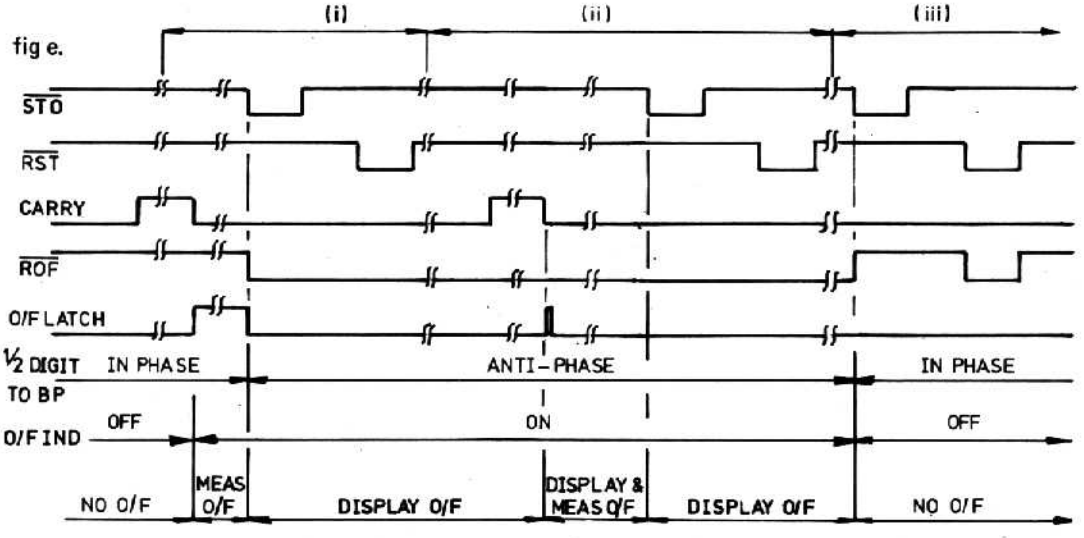
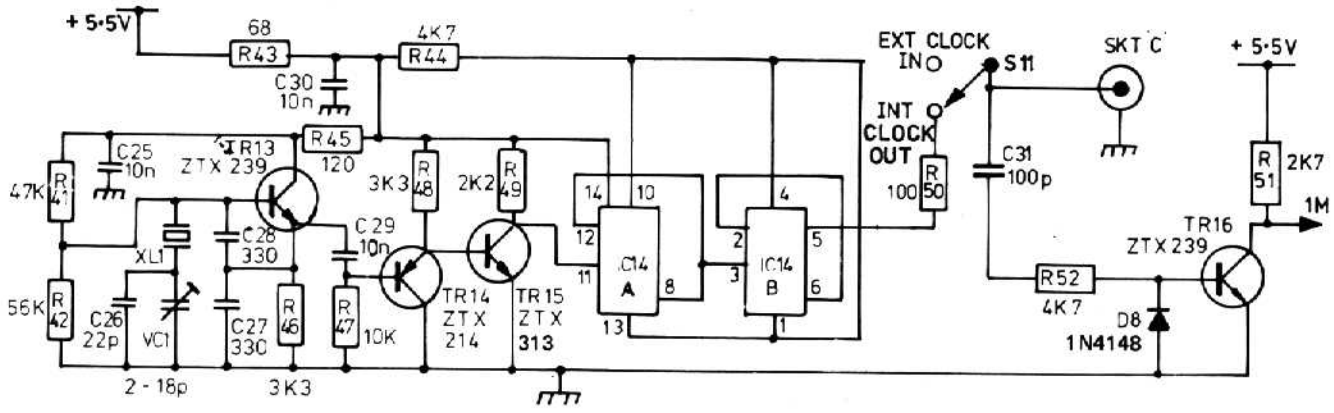



fig e.



**Timebase**




TR13, XL1 and associated components form a high stability 4MHz crystal oscillator trimmed by VC1. The oscillator output is buffered to LSTTL levels by TR14 and TR15 and fed to IC14 which is a dual D-type bistable connected as a divide-by-4. The output from IC14B pin 5 is therefore a 1MHz square wave which is fed via R50 and S11 to a buffer consisting of TR16 and associated components, and to Socket C on the rear panel to permit monitoring. When S11 is switched to the other position, the internal 1MHz is disconnected and an external 1MHz frequency standard can be connected directly to the TR16 buffer input via socket C.

The output of TR16 goes to the timebase decade dividers, or to IC2 count input via S8 in Time Average Period mode.

**Timebase Dividers**

The Timebase Dividers successively divide the stable 1MHz signal by 10 to provide accurate time slots which are then used by the Recycle Logic to generate gate times for the counter.

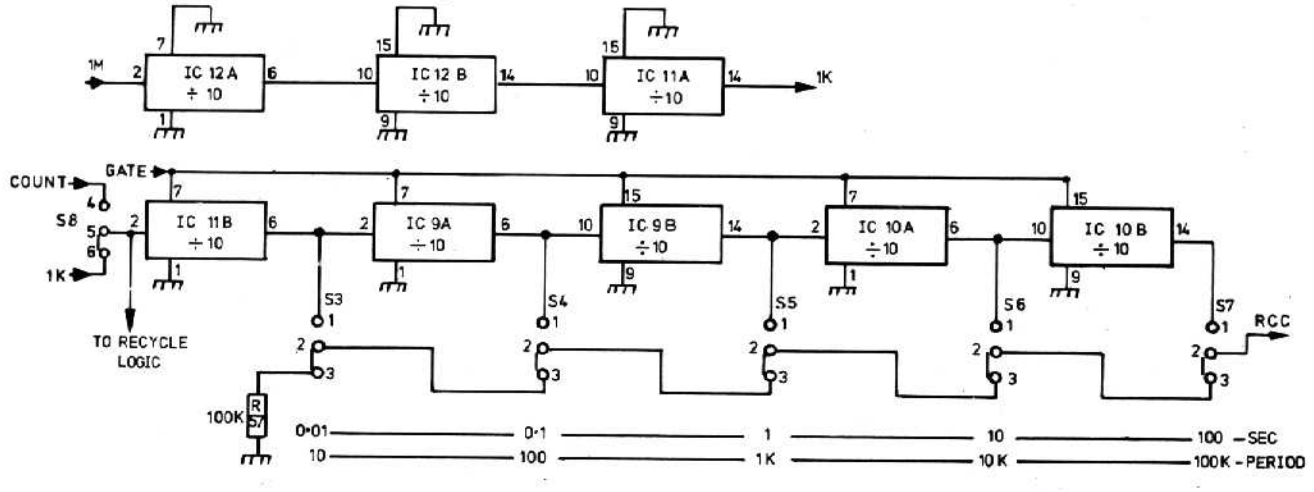
IC12, IC11, IC10, and IC9 are dual decade up-counters clocked on the negative edge. IC12A, IC12B and IC11A divide the 1MHz output from the timebase by $10^3$ to give a 1kHz signal at IC11A pin 14.

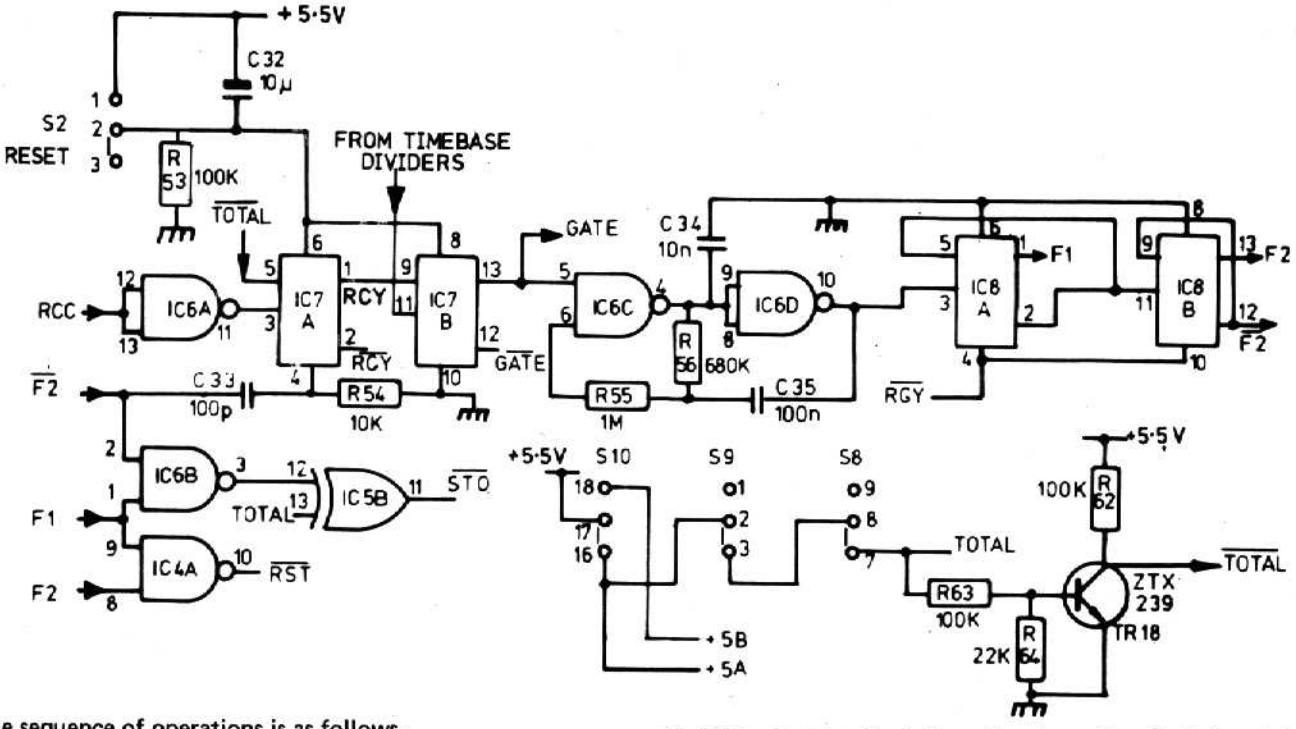
In Frequency mode the 1kHz signal from IC11A (1K) is fed to the further chain of decade counters IC11B, IC9A and B, IC10A and B, and the clock input of IC7B in the Recycle Logic. The 5 outputs of the decade divider chain are IC11B: 100Hz (period = 10mS), IC9A: 10Hz (period = 100mS), IC9B: 1Hz (period = 1s), IC10A: 0.1Hz (period = 10s), and IC10B: 0.01Hz (period = 100s). One of the outputs is selected by the range selection switching S3, S4, S5, S6, and S7, as the Recycle Clock signal (RCC) for the Recycle Logic; the period of the selected output is used by the Recycle Logic to determine the gate time of counter IC2.

In Time Average Period mode the COUNT signal from the A amplifier output, which is at the frequency of the signal being measured, is fed via S8 to the input of IC11B and to IC7B in the Recycle Logic. In this mode the decade divider chain outputs have the following periods - IC11B: 10 input periods, IC9A: 100 input periods, IC9B: $10^3$ input periods and IC10B: $10^5$ input periods. One of the outputs is again selected by the range selection switching S3, S4, S5, S6, and S7 as the Recycle Clock signal (RCC) for the Recycle Logic; the gate time for IC2 generated by the Recycle Logic will be of a duration equal to the number of input periods selected.

**Recycle Logic**

The Recycle Logic generates the main control signals to a) enable counting in IC1 ($\overline{\text{GATE}}$), b) to reset the Timebase Dividers to zero (GATE), c) to transfer information from the counters to the latches in IC1, IC2 ($\overline{\text{STO}}$) and hence to the display, and d) to reset the counters in IC1, IC2 ($\overline{\text{RST}}$).






The sequence of operations is as follows.

A recycle is initiated by RCC going from HIGH to LOW setting the Recycle bistable IC7A. The next LOW to HIGH transition of IC7B pin 11 (1k or COUNT, in Frequency or Time Average Period mode respectively) then sets the Gate bistable IC7B. With GATE set HIGH the timebase dividers IC11B, IC9A, IC9B, IC10A, IC10B are reset to zero, and counting in IC2 (and therefore IC1) is inhibited by $\overline{\text{GATE}}$ going LOW. GATE going HIGH also enables the Recycle oscillator consisting of IC6C, IC6D, R55, R56, C34 and C35 which runs at 7.5Hz nominal. The output from IC6D goes HIGH approximately 50ns after GATE goes HIGH and this sets bistable F1 (IC8A). Bistables F1 and F2 (IC8B) form a binary counter with four states; the truth table is shown below.

| RECYCLE OSC | F1 | F2 | REMARKS |
|---|---|---|---|
| 0 | 0 | 0 | Gate open, IC2, IC1 counting |
| 1 | 1 | 0 | Gate closed, $\overline{\text{STO}}$ LOW |
| 2 | 0 | 1 | Gate closed, idle |
| 3 | 1 | 1 | Gate closed, $\overline{\text{RST}}$ LOW |
| 4 | 0 | 0 | Gate opens on next 1K LOW to HIGH transition. |

Successive LOW to HIGH transitions of IC6D output clock this counter through its states until F2 resets (state 4 of the truth table); IC6B, IC4A, IC5B decode the counter outputs to generate the $\overline{\text{STO}}$ and $\overline{\text{RST}}$ signals for IC1, IC2. When F2 resets, F2 goes from HIGH to LOW and this is passed via C33 to the clear input of the Recycle bistable IC7A, resetting it. With the Recycle bistable reset, the next LOW to HIGH transition of the 1K/COUNT signal resets the Gate bistable IC7B. GATE goes LOW, removing the clear from the Timebase Dividers and inhibiting the Recycle Oscillator; $\overline{\text{GATE}}$ goes HIGH and enables IC2 (and hence IC1) to count again. F1 and F2 are clamped in reset by the $\overline{\text{RCY}}$ output of the Recycle bistable IC7A when it resets to avoid further counting of F1 and F2 should the Gate bistable IC7B still be set at the next positive edge of the Recycle Oscillator which could happen in Time Average Period mode when the clock input to IC7B is in fact the COUNT signal. Fig g shows the complete recycle timing diagram.

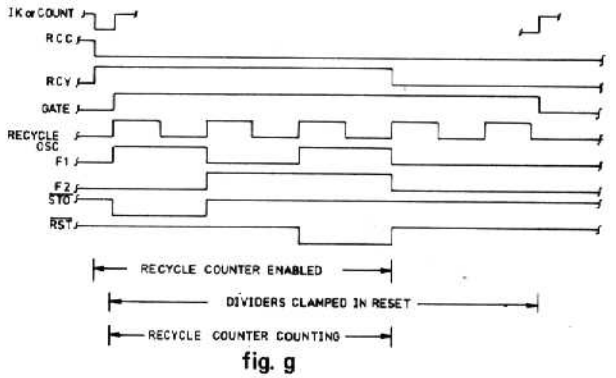


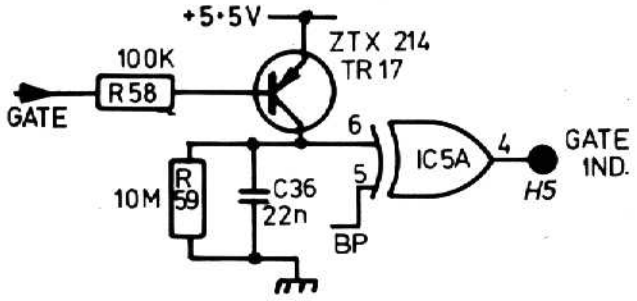

fig. g

**Reset Switch:** When the Reset switch is pressed both RCY and GATE are preset, stopping the measurement cycle in progress and initiating a complete Recycle. C32 ensures that the Reset signal is held HIGH long enough to generate two Recycle operations, even if the switch is closed only momentarily. This is necessary to ensure that both the latches and counters in IC1, IC2 are reset to zero, the second Recycle loading the latches with the zeroed count, to avoid a meaningless count being shown in the display for one measurement cycle. C32 also provides power-on reset.

**TOTAL Signal:** In the Totalise mode, the TOTAL signal is HIGH because S8, S9, S10 are all in the 'OUT' position. $\overline{\text{TOTAL}}$ (TR18 output) is therefore LOW, holding the D input of the Recycle bistable IC7A LOW; RCC never therefore initiates a Recycle because RCY remains LOW. $\overline{\text{GATE}}$ therefore remains HIGH and the counters in IC1, IC2 are permanently enabled. At the same time the TOTAL signal on IC5B ensures that $\overline{\text{STO}}$ is held LOW so that the Counter information is passed directly to the display.

**Gate Indicator:** The GATE signal is also fed to the base of TR17 via R58. When GATE is LOW (i.e. IC2 counting because $\overline{\text{GATE}}$ is HIGH) TR17 is on pulling pin 6 of

IC5A HIGH. The output of IC5A is therefore $\overline{BP}$ and the GATE indicator will show. C36 "stretches" the time pin 6 of IC5A is HIGH so that the indicator shows even with very short gate times.

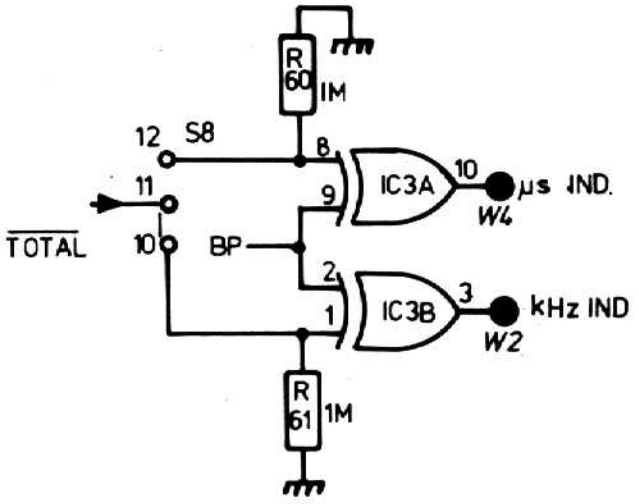


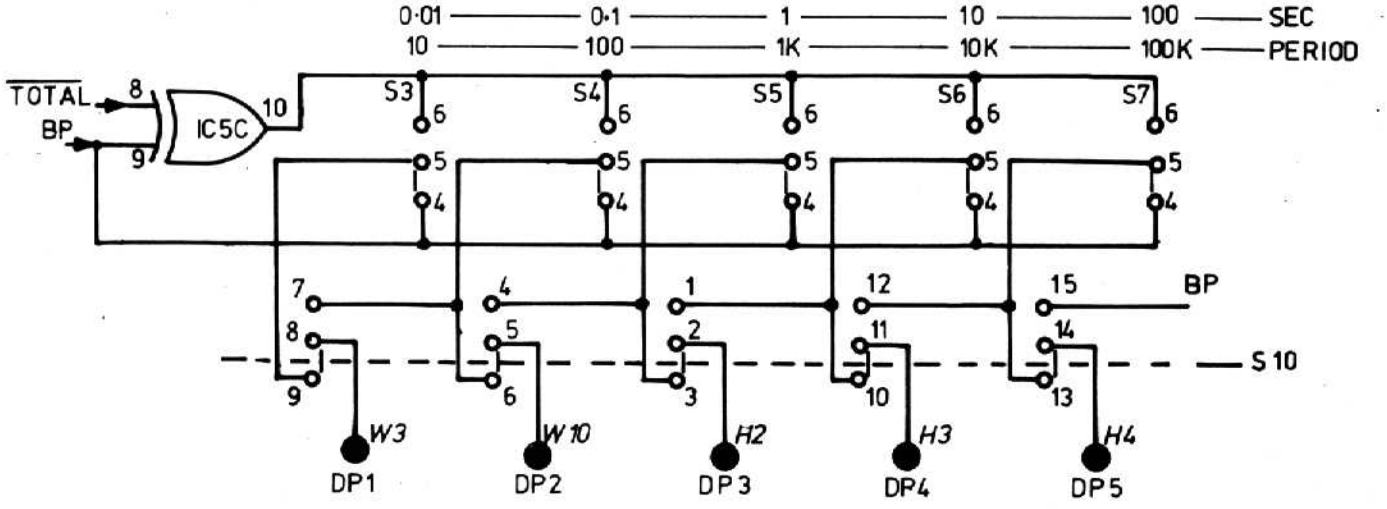

**Decimal Point Selection, µs and kHz indicators**

IC5C generates the $\overline{BP}$ signal required by the LCD to display a character except in Totalise mode. When the range is selected by S3, S4, S5, S6 or S7, this $\overline{BP}$ signal is routed to the appropriate decimal point via S10; BP is routed to decimal points of the unselected ranges. S10 is the High Frequency switch and is used to shift all decimal points one position to the right to enable the prescaled high frequency signal to still read out in kHz.

When Totalise mode is selected, $\overline{TOTAL}$ is LOW and the output of IC5C is BP not $\overline{BP}$; all decimal points are therefore off in totalise mode.

The $\overline{BP}$ signals for the µs and kHz signals are generated by IC3A and IC3B respectively when either pin 8 or pin 1 is pulled HIGH by $\overline{TOTAL}$ being HIGH. The unselected input is pulled LOW by R60 or R61 and that indicator suppressed. In Totalise mode, $\overline{TOTAL}$ is LOW and both indicators are suppressed.



## CALIBRATION

Recalibration of the crystal oscillator may be carried out without dismantling the instrument by peeling off the inspection label to gain access to the multiturn trimmer.

Adjustment can be monitored by either

a) Using a high accuracy frequency counter to measure the internal clock at Socket C (CLOCK IN/CLOCK OUT switch in CLOCK OUT position).

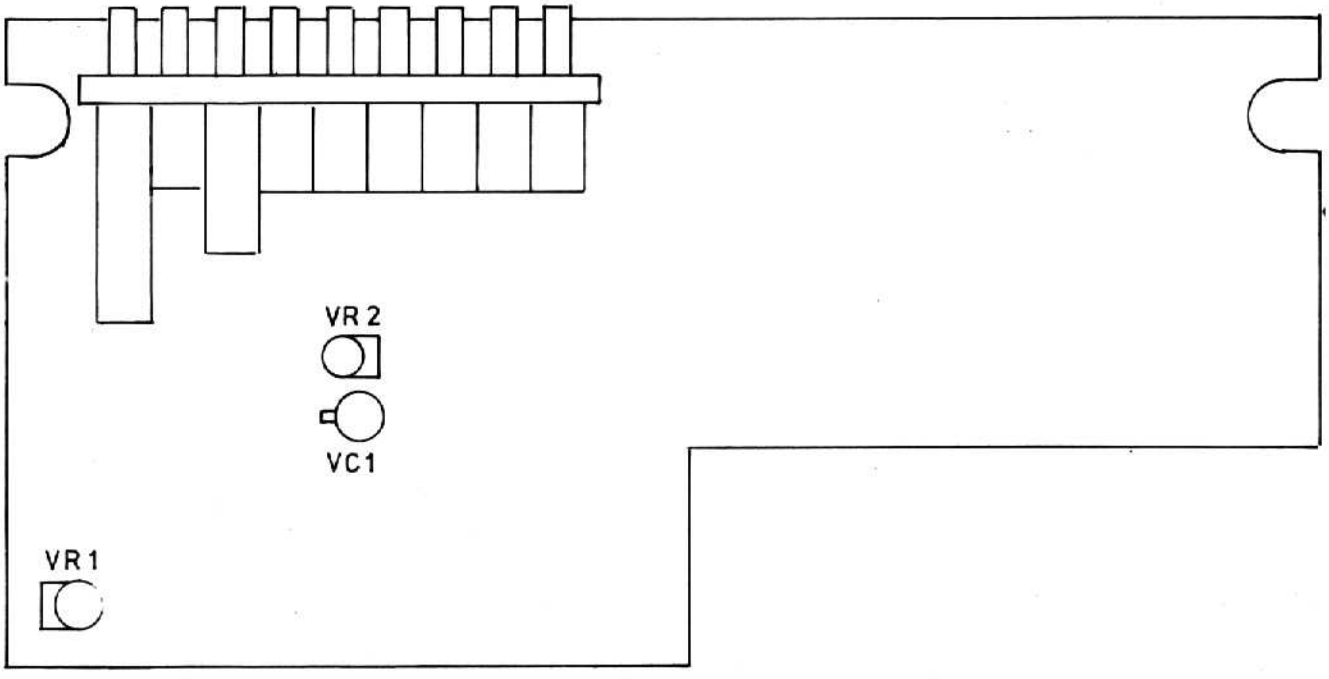
or

b) Using a frequency standard or standard frequency receiver to provide a high accuracy signal at input A.

Use a non-metallic trimming tool when adjusting the oscillator. If only a metal tool is available, allow for the frequency shift that the metal tool introduces whilst making the adjustment so that the meter reads correctly with the trimming tool withdrawn.

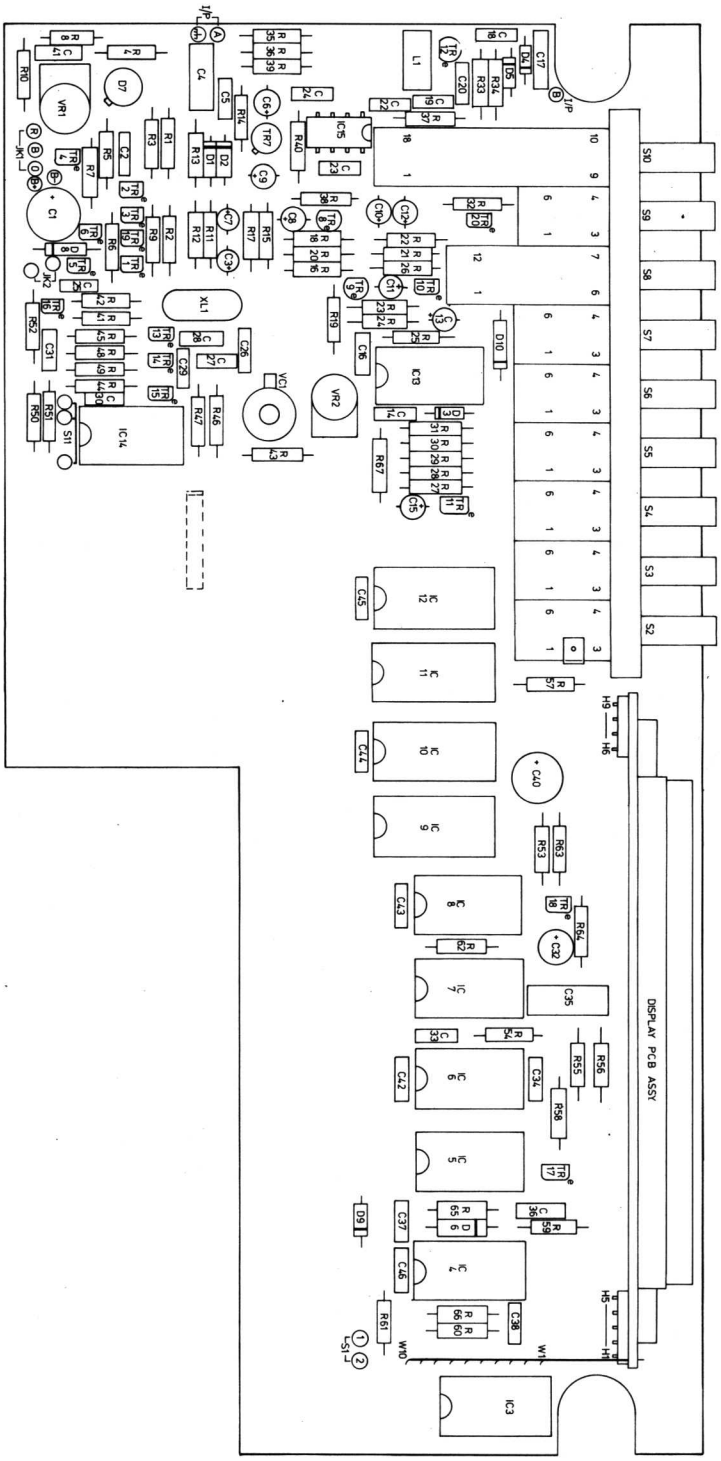
If the internal power supply needs re-setting because components have been replaced, readjust to 5.55V $\pm$ 0.01V using VR1.

If components have been replaced in the A amplifier it may be necessary to re-optimise the Schmitt trigger "window". With an input of 8 to 9mV rms at 20MHz, adjust VR2 to obtain the most stable reading.

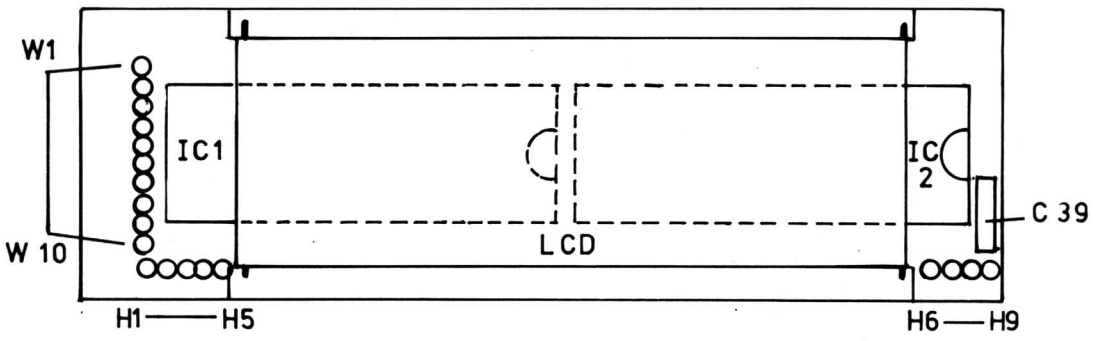


## COMPONENT LAYOUTS

### Main Pcb
### (prior to Issue 10)




### Display Pcb



**PARTS LIST** (refer also to notes on page 18)

**Resistors**

| Ref | Description | Part No |
|---|---|---|
| R1 | 12KJ W25 CF | 23185-3120 |
| R2 | 3R9J W25 CF | 23185-0039 |
| R3 | 2K7J W25 CF | 23185-2270 |
| R4 | 820RJ W25 CF | 23185-1820 |
| R5 | 5K6J W25 CF | 23185-2560 |
| R6 | 100KJ W25 CF | 23185-4100 |
| R7 | 15KJ W25 CF | 23185-3150 |
| R8 | 3K9J W25 CF | 23185-2390 |
| R9 | 100KJ W25 CF | 23185-4100 |
| R10 | 100KJ W25 CF | 23185-4100 |
| R11 | 33KJ W25 CF | 23185-3330 |
| R12 | 10KJ W25 CF | 23185-3100 |
| R13 | 1MOJ W25 CF | 23185-5100 |
| R14 | 1MOJ W25 CF | 23185-5100 |
| R15 | 680RJ W25 CF | 23185-1680 |
| R16 | 560RJ W25 CF | 23185-1560 |
| R17 | 2K2J W25 CF | 23185-2220 |
| R18 | 12KJ W25 CF | 23185-3120 |
| R19 | 680RJ W25 CF | 23185-1680 |
| R20 | 10KJ W25 CF | 23185-3100 |
| R21 | 1KOJ W25 CF | 23185-2100 |
| R22 | 27KJ W25 CF | 23185-3270 |
| R23 | 4K7J W25 CF | 23185-2470 |
| R24 | 1KOJ W25 CF | 23185-2100 |
| R25 | 100KJ W25 CF | 23185-4100 |
| R26 | 10RJ W25 CF | 23185-0100 |
| R27 | 1MOJ W25 CF | 23185-5100 |
| R28 | 1MOJ W25 CF | 23185-5100 |
| R29 | 100KJ W25 CF | 23185-4100 |
| R30 | 100KJ W25 CF | 23185-4100 |
| R31 | 4K7J W25 CF | 23185-2470 |
| R32 | 470RJ W25 CF | 23185-1470 |
| R33 | 2K2J W25 CF | 23185-2220 |
| R34 | 5K6J W25 CF | 23185-2560 |
| R35 | 390RJ W25 CF | 23185-1390 |
| R36 | 10RJ W25 CF | 23185-0100 |
| R37 | 820RJ W25 CF | 23185-1820 |
| R38 | 39KJ W25 CF | 23185-3390 |
| R39 | 12RJ W25 CF | 23185-0120 |
| R40 | 3K3J W25 CF | 23185-2330 |
| R41 | 47KJ W25 CF | 23185-3470 |
| R42 | 56KJ W25 CF | 23185-3560 |
| R43 | 68RJ W25 CF | 23185-0680 |
| R44 | 4K7J W25 CF | 23185-2470 |
| R45 | 120RJ W25 CF | 23185-1120 |
| R46 | 3K3J W25 CF | 23185-2330 |
| R47 | 10KJ W25 CF | 23185-3100 |
| R48 | 3K3J W25 CF | 23185-2330 |
| R49 | 2K2J W25 CF | 23185-2220 |
| R50 | 100RJ W25 CF | 23185-1100 |
| R51 | 2K7J W25 CF | 23185-2270 |
| R52 | 4K7J W25 CF | 23185-2470 |
| R53 | 100KJ W25 CF | 23185-4100 |
| R54 | 10KJ W25 CF | 23185-3100 |
| R55 | 1MOJ W25 CF | 23185-5100 |
| R56 | 680KJ W25 CF | 23185-4680 |
| R57 | 100KJ W25 CF | 23185-4100 |
| R58 | 100KJ W25 CF | 23185-4100 |
| R59 | 10MJ W25 CF | 23185-6100 |
| R60 | 1MOJ W25 CF | 23185-5100 |
| R61 | 1MOJ W25 CF | 23185-5100 |
| R62 | 100KJ W25 CF | 23185-4100 |
| R63 | 100KJ W25 CF | 23185-4100 |
| R64 | 22KJ W25 CF | 23185-3220 |
| R65 | 100KJ W25 CF | 23185-4100 |
| R66 | 10KJ W25 CF | 23185-3100 |
| R67 | 100KJ W25 CF | 23185-4100 |
| VR1 | 1KO PS/H | 23377-2100 |
| VR2 | 10K PS/H | 23377-3100 |

**Capacitors**

| Ref | Description | Part No |
|---|---|---|
| C1 | 47UF 16V Elec | 23557-0631 |
| C2 | 10NZ 63V Cer | 23427-0325 |
| C3 | 47UF 6V3 Tant | 23594-0227 |
| C4 | 100NJ 100V Poly/E | 23620-0207 |
| C5 | 56PK 500V Cer | 23424-0441 |
| C6 | 10UF 16V Tant | 23594-0219 |
| C7 | 22UF 10V Tant | 23594-0225 |
| C8 | 22UF 10V Tant | 23594-0225 |
| C9 | 22OUF 3V Tant | 23594-0223 |
| C10 | 1UOF 35V Tant | 23594-0224 |
| C11 | 22UF 10V Tant | 23594-0225 |
| C12 | 47UF 6V3 Tant | 23594-0227 |
| C13 | 22UF 10V Tant | 23594-0225 |
| C14 | 22NZ 63V Cer | 23427-0326 |
| C15 | 10UF 16V Tant | 23594-0219 |
| C16 | 10NZ 63V Cer | 23427-0325 |
| C17 | 10NS 500V Cer | 23424-0443 |
| C18 | 10NZ 63V Cer | 23427-0325 |
| C19 | 10NZ 63V Cer | 23427-0325 |
| C20 | 10NZ 63V Cer | 23427-0325 |
| C21 | Not Used | |
| C22 | 10NZ 63V Cer | 23427-0325 |
| C23 | 10NZ 63V Cer | 23427-0325 |
| C24 | 10NZ 63V Cer | 23427-0325 |
| C25 | 10NZ 63V Cer | 23427-0325 |
| C26 | 22PG 63V Cer | 23427-0323 |
| C27 | 330PG 63V Cer | 23427-0327 |
| C28 | 330PG 63V Cer | 23427-0327 |
| C29 | 10NZ 63V Cer | 23427-0325 |
| C30 | 10NZ 63V Cer | 23427-0325 |
| C31 | 100PG 63V Cer | 23427-0322 |
| C32 | 10UF 16V Tant | 23594-0219 |
| C33 | 100PG 63V Cer | 23427-0322 |
| C34 | 10NZ 63V Cer | 23427-0325 |
| C35 | 100NJ 100V Poly/E | 23620-0207 |
| C36 | 22NZ 63V Cer | 23427-0326 |
| C37 | 10NZ 63V Cer | 23427-0325 |
| C38 | 100PG 63V Cer | 23427-0322 |
| C39 | 10NZ 63V Cer | 23427-0325 |
| C40 | 47UF 16V Elec | 23557-0631 |
| C41 | 10NZ 63V Cer | 23427-0325 |
| C42 | 10NZ 63V Cer | 23427-0325 |
| C43 | 10NZ 63V Cer | 23427-0325 |
| C44 | 10NZ 63V Cer | 23427-0325 |
| C45 | 10NZ 63V Cer | 23427-0325 |
| C46 | 10NZ 63V Cer | 23427-0325 |
| VC1 | 2 - 20P Trimcap | 23911-0016 |

**Semi-conductors**

| Ref | Description | | Part No |
|---|---|---|---|
| D1 | Dio | 1N4148 | 25021-0901 |
| D2 | Dio | 1N4148 | 25021-0901 |
| D3 | Dio | 1N4148 | 25021-0901 |
| D4 | Dio | BA482 | 25030-0905 |
| D5 | Dio | BA482 | 25030-0905 |
| D6 | Dio | 1N4148 | 25021-0901 |
| D7 | IC | 8069DCZR | 27161-0007 |
| D8 | Dio | 1N4148 | 25021-0901 |
| D9 | Dio | 1N4002 | 25115-0907 |
| D10 | Dio | 1N4148 | 25021-0901 |
| TR1 | Tran PNP | ZTX214-L5 | 25341-0214 |
| TR2 | Tran NPN | ZTX239-L5 | 25380-0229 |
| TR3 | Tran PNP | ZTX214-L5 | 25341-0214 |
| TR4 | Tran NPN | ZTX239-L5 | 25380-0229 |
| TR5 | Tran PNP | ZTX214-L5 | 25341-0214 |
| TR6 | Tran PNP | ZTX214-L5 | 25341-0214 |
| TR7 | Tran FET | 3N201 | 25602-0002 |
| TR8 | Tran NPN | BF199-18-C | 25388-0207 |
| TR9 | Tran NPN | BF199-18-C | 25388-0207 |
| TR10 | Tran NPN | ZTX239-L5 | 25380-0229 |
| TR11 | Tran NPN | ZTX239-L5 | 25380-0229 |
| TR12 | Tran PNP | BF506-18-C | 25341-0315 |
| TR13 | Tran NPN | ZTX239-L5 | 25380-0229 |
| TR14 | Tran PNP | ZTX214-L5 | 25341-0214 |
| TR15 | Tran NPN | ZTX313-L5 | 25380-0230 |
| TR16 | Tran NPN | ZTX239-L5 | 25380-0229 |
| TR17 | Tran PNP | ZTX214-L5 | 25341-0214 |
| TR18 | Tran NPN | ZTX239-L5 | 25380-0229 |
| TR19 | Tran PNP | ZTX550-L5 | 25341-0215 |
| TR20 | Tran NPN | ZTX313-L5 | 25380-0230 |

| Ref | Description | | Part No |
|---|---|---|---|
| IC1 | IC | ICM7224IPL | 27250-0405 |
| IC2 | IC | ICM7224IPL Sel | 27250-0406 |
| IC3 | IC | CD4070BE | 27226-0700 |
| IC4 | IC | CD4011BE | 27226-0110 |
| IC5 | IC | CD4070BE | 27226-0700 |
| IC6 | IC | CD4011BE | 27226-0110 |
| IC7 | IC | CD4013BE | 27226-0130 |
| IC8 | IC | CD4013BE | 27226-0130 |
| IC9 | IC | CD4518BE | 27226-5181 |
| IC10 | IC | CD4518BE | 27226-5181 |
| IC11 | IC | CD4518BE | 27226-5181 |
| IC12 | IC | CD4518BE | 27226-5181 |
| IC13 | IC | SN74LS13N | 27223-0130 |
| IC14 | IC | SN74LS74N | 27223-0740 |
| IC15 | IC | SP8660DP | 27251-0001 |

**Opto, Electro/Mechanical, Mechanical & Packaging Parts**

| Description | | Part No |
|---|---|---|
| Quartz Crystal 4MHz | | 28500-0200 |
| Spacer for TR7 | 1 off | 20661-0800 |
| 5 Way PCB Header | | 22573-0033 |
| 4 Way PCB Header | | 22573-0034 |
| IC Holder 14 Pin | 8 off | 22574-0119 |
| IC Holder 16 Pin | 4 off | 22574-0120 |
| IC Holder 40 pin | 2 off | 22574-0125 |
| 25 Way In Line Skt- | 3 off | 22574-0126 |
| 10 Way Strip connector | | 35171-0290 |
| Threaded stud M3 x 8 | | 20205-0600 |
| Switchbank | | 22225-0517 |
| Vero pin | 2 off | 22469-0200 |
| PCB | | 35555-0270 |
| Pushbutton, Red | | 37113-0120 |
| Pushbutton, Black | 5 off | 37113-0130 |
| Pushbutton, Grey | 3 off | 37113-0140 |
| Washer, s/pf Phono Skt | | 20037-0302 |
| Slide Switch | 2 off | 22218-0205 |
| Phono Socket | | 22580-0301 |
| BNC Socket | 3 off | 22588-0004 |
| Rear Panel | | 33331-0320 |
| Earthing spring to Case Upper | | 35358-0450 |
| Screw for Slide Switches | 4 off | 20234-0026 |
| Display Bezel | | 31711-0010 |
| Front Panel | | 33331-0310 |
| Earthing Strip Front Panel to Main PCB | | 35358-0460 |
| Screened Lead 130mm | cut from | 10143-0106 |
| M3 Washer (Batt holder to Case, Front panel earthing strip to PCB) | 3 off | 20030-0263 |
| Screw 6BA x 3/16" (PCB to Case, Case Upr to Lwr) | 6 off | 20134-0501 |
| M3 Nut (Front Panel earthing strip to PCB) | | 20210-0101 |
| Power Socket 2.5mm | | 22581-0506 |
| Fibre washer | 2 off | 20612-0010 |
| Battery holder | | 20656-0011 |
| LCD | | 26100-0050 |
| Side trim - front | 2 off | 31332-0490 |
| Side trim - rear | 2 off | 31332-0500 |
| Screen - Case lower | | 31346-0050 |
| Screen - Case upper | | 31346-0070 |
| Insulator - Case lower | | 31346-0060 |

| Description | | Part No |
|---|---|---|
| Earthing tag - Sw/bank | | 31511-0040 |
| Case Lower | | 33537-0160 |
| Earthing spring - Case lwr | | 35358-0480 |
| Screw 6BA x 1¼" (Case upper to lower) | | 20134-0503 |
| Screw 6BA x 3/16" c/sunk (Constraint to Case) | 2 off | 20118-0002 |
| Constraint - Battery compartment | | 33145-0310 |
| Foam pad 50 x 20 x 4mm 3 off | cut from | 10300-0304 |
| Pad - battery restraint to Case Upper, cut from | | 10300-0316 |
| Screw M3 x 5mm TR3 (s/tap) (Battery holder to constraint, main pcb to Right Angle Bracket) | 4 off | 20062-0600 |
| Screw M3 x 8mm TR3 (s/tap) (Right Angle Bracket to Display pcb) | 2 off | 20062-0601 |
| Right Angle Support Bracket | 2 off | 33141-0490 |
| Spacer (Right Angle Bracket to Display pcb) | 2 off | 20661-0223 |
| Washer shakeproof M3 (Front panel earthing strip to pcb, and all display bracket screws) | 5 off | 20037-0301 |
| Battery | 6 off | 22010-0405 |
| Handle | | 31336-0200 |
| Feet, black | 4 off | 31748-0190 |
| Battery cover | | 33335-0060 |
| Case Upper | | 33537-0150 |
| Logo label | | 37522-0010 |
| Instruction label | | 37558-0130 |
| Serial No label | | 37522-0020 |
| Guarantee card | | 48581-0230 |
| Instruction book | | 48581-0240 |
| Carton | | 38113-0260 |
| Protective packing piece | | 38161-0010 |
| Calibration Label | | 37541-0480 |
| Aircap Sheet, cut from | | 10612-0202 |
| Printed Sleeve | | 38181-0140 |

## MODELS AND PARTS LIST CHANGES

1) From February 1986 C14 was changed from 10N 63V Ceramic to 100N Ceramic — Part No. 234438-0007 — to improve decoupling of the supply rail to IC15.

2) From May 1987 design changes were incorporated to improve performance. These changes entailed PCB track modifications and component changes on the PCB assembly summarised below:

PCB 35555-0270 revised to Issue 10. Refer to Component Layout opposite and appropriate Circuit Diagram.

### Parts List Deletions

| Ref | Description | | Part No |
|---|---|---|---|
| R31 | 4K7J W25 CF | | 23185-2470 |
| R44 | 4K7J W25 CF | | 23185-2470 |
| TR20 | ZTX313 | | 25380-0230 |
| Vero pin | | 2 off | 22469-0200 |

### Parts List Additions

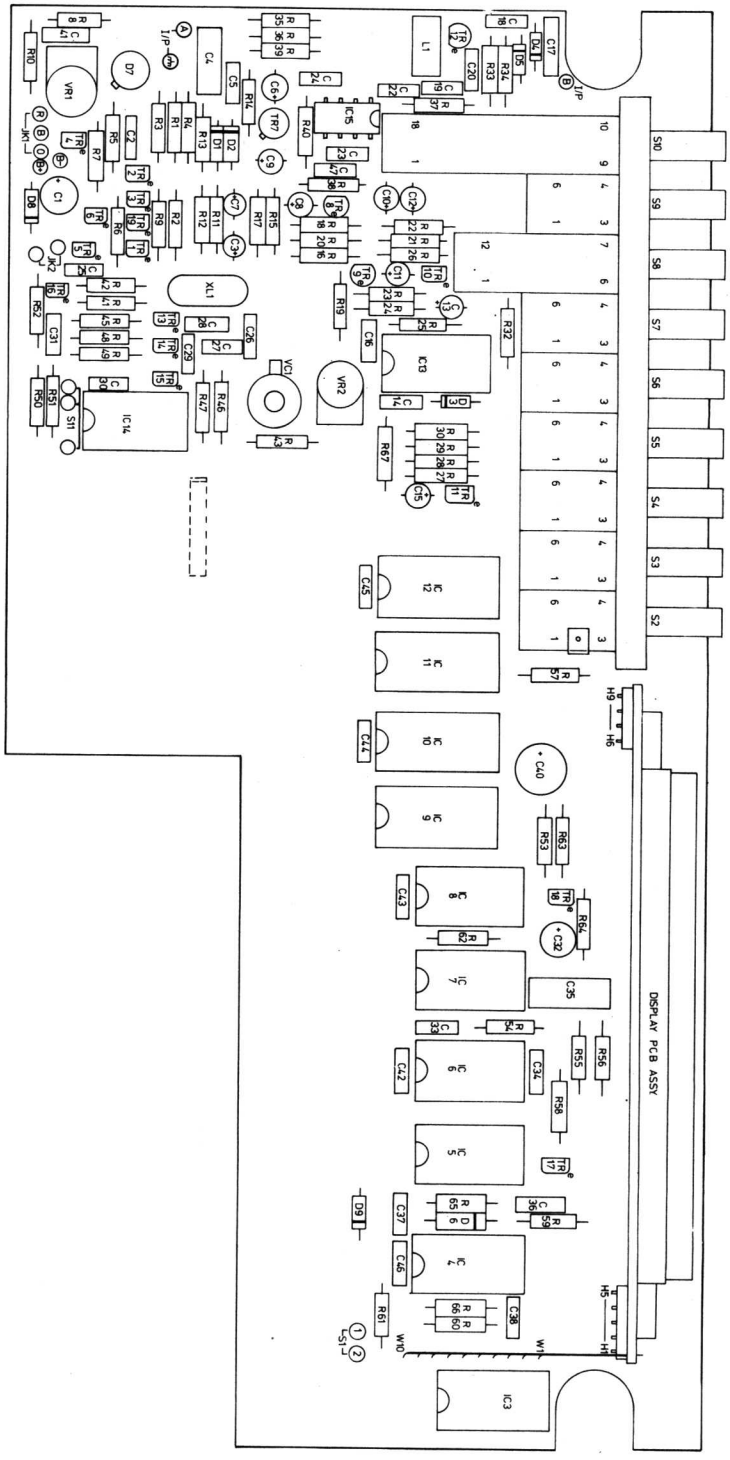
| Ref | Description | Part No |
|---|---|---|
| C47 | 100NM 63V Cer | 23438-0007 |
| D10 | 1N4148 | 25021-0901 |

### Parts List Replacements

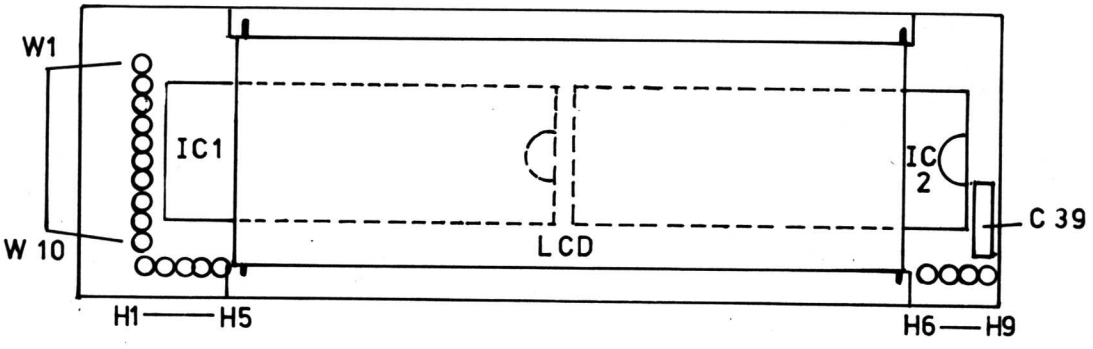
| Ref | Description | | | | Part No |
|---|---|---|---|---|---|
| R11 | Was | 33KJ | now | 39KJ | 23185-3390 |
| R12 | Was | 10KJ | now | 12KJ | 23185-3120 |
| R22 | Was | 27KJ | now | 22KJ | 23185-3220 |
| R23 | Was | 4K7J | now | 12KJ | 23185-3120 |
| R32 | Was | 470RJ | now | 390RJ | 23185-1390 |
| R40 | Was | 3K3J | now | 820RJ | 23185-1820 |
| R45 | Was | 120RJ | now | 100RJ | 23185-1100 |
| R52 | Was | 4K7J | now | 3K9J | 23185-2390 |
| VR2 | Was | 10K | now | 100K | 23377-4100 |
| IC2 | Was | ICM7224IPL Selected | | | |
| Now | | ICM7224IPL | | | 27250-0406 |
| IC13 | Was | 74LS13 | | | |
| | Now | 74HC132 | | | 27231-1320 |

## COMPONENT LAYOUTS

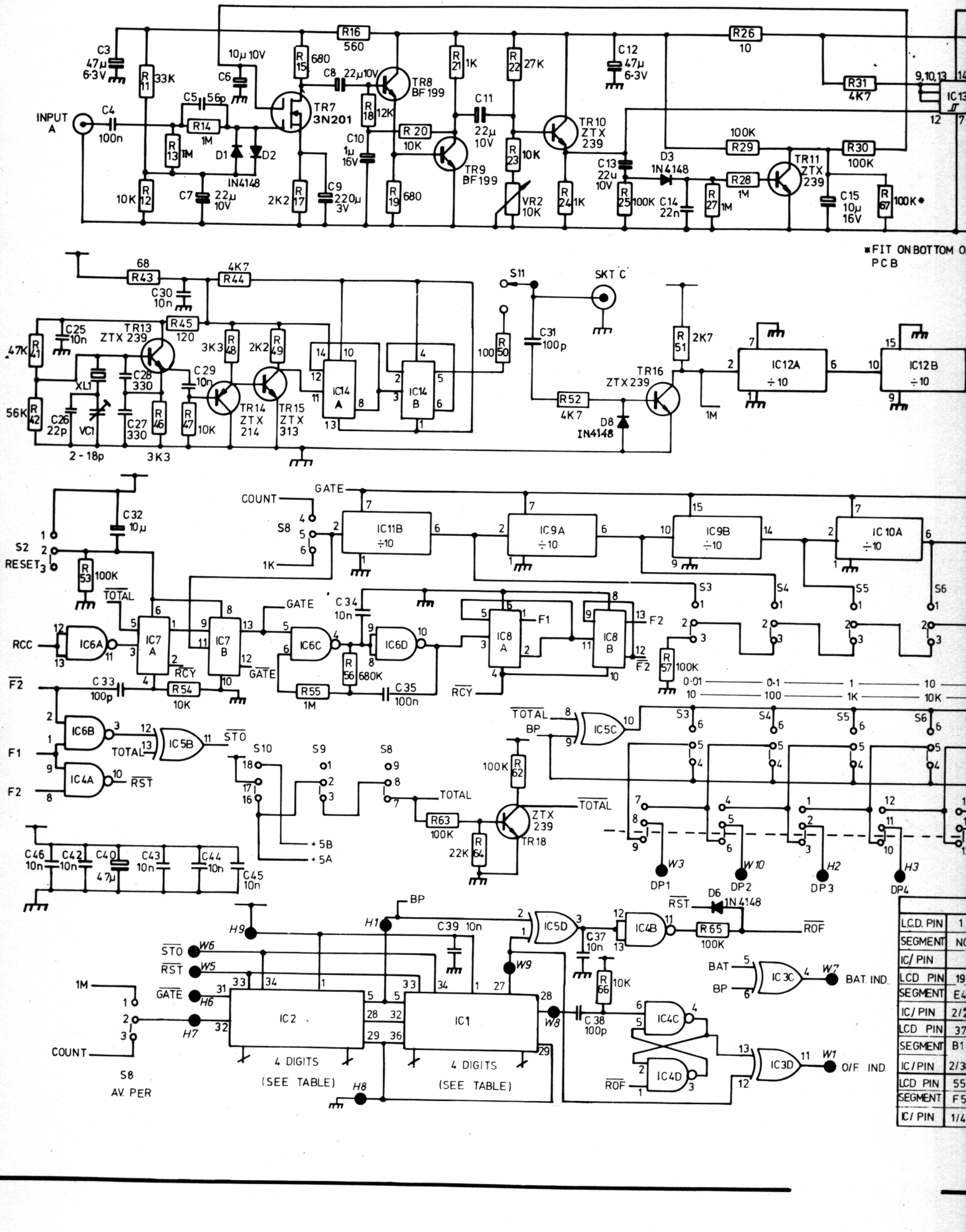
### Main Pcb
### (Issue 10 onwards)



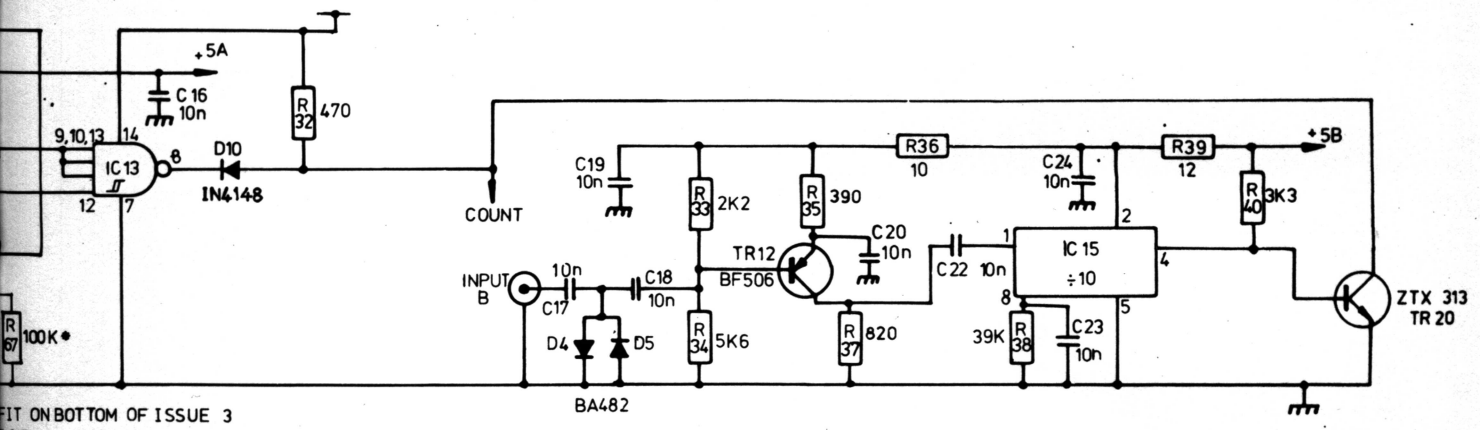

### Display Pcb



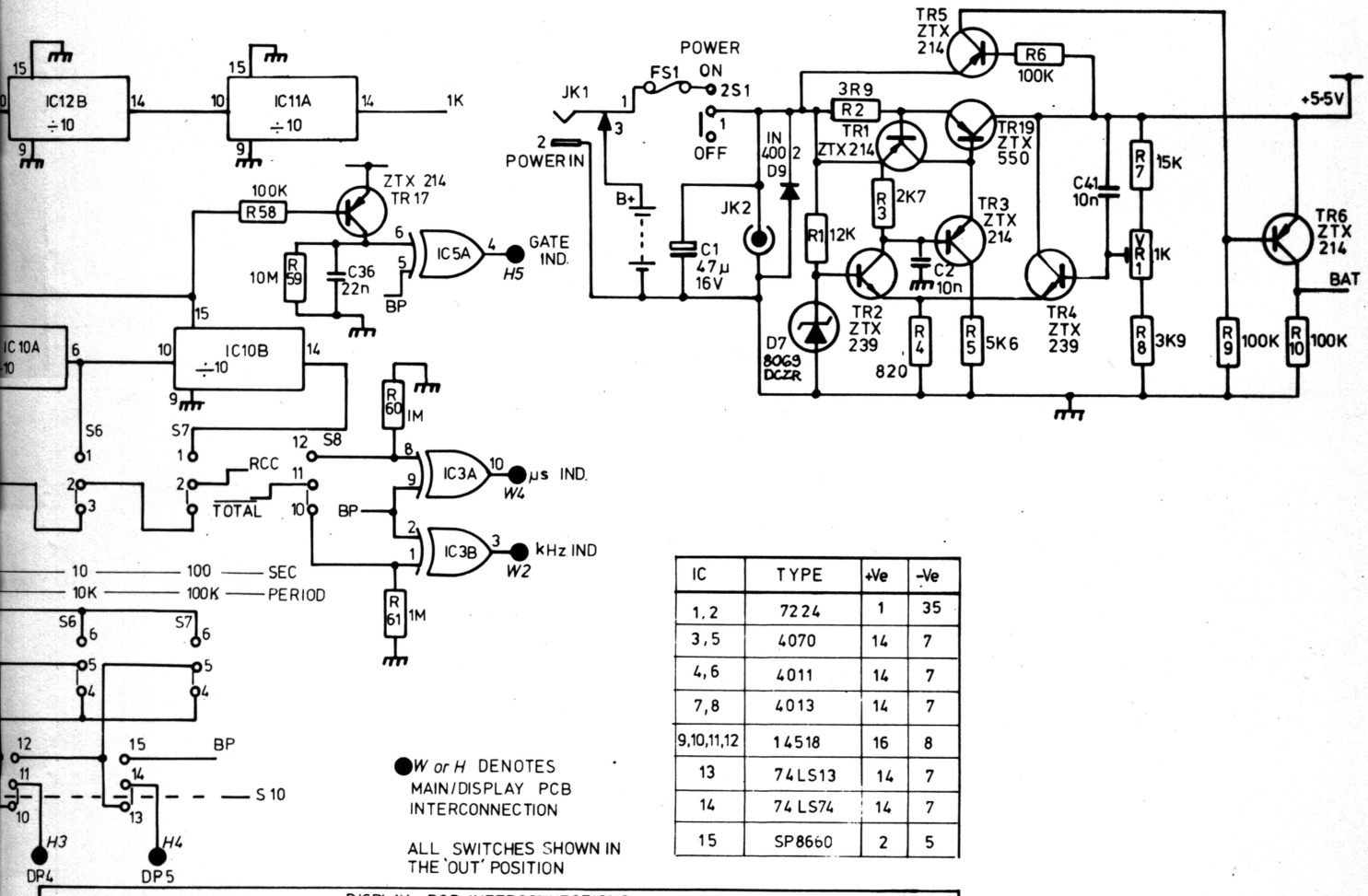
## CIRCUIT DIAGRAM
(Prior to Issue 10)




| | |
|---|---|
| LCD. PIN | 1 |
| SEGMENT | NC |
| IC/ PIN | |
| LCD PIN | 19 |
| SEGMENT | E4 |
| IC/ PIN | 2/2 |
| LCD PIN | 37 |
| SEGMENT | B1 |
| IC/ PIN | 2/3 |
| LCD PIN | 55 |
| SEGMENT | F5 |
| IC/ PIN | 1/4 |




FIT ON BOTTOM OF ISSUE 3
PCB




| IC | TYPE | +Ve | -Ve |
|---|---|---|---|
| 1,2 | 7224 | 1 | 35 |
| 3,5 | 4070 | 14 | 7 |
| 4,6 | 4011 | 14 | 7 |
| 7,8 | 4013 | 14 | 7 |
| 9,10,11,12 | 14518 | 16 | 8 |
| 13 | 74LS13 | 14 | 7 |
| 14 | 74 LS74 | 14 | 7 |
| 15 | SP8660 | 2 | 5 |

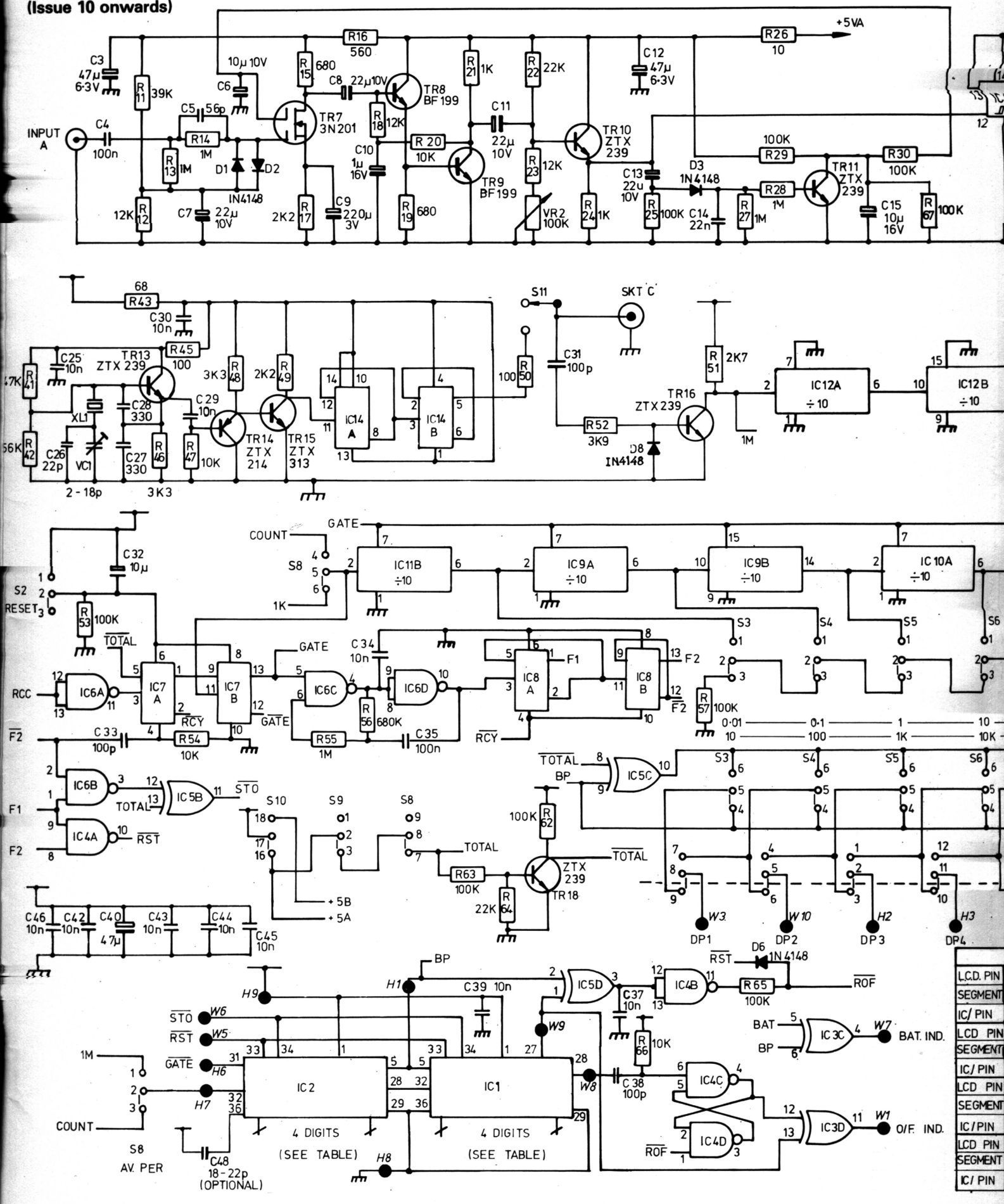
●*W or H* DENOTES MAIN/DISPLAY PCB INTERCONNECTION

ALL SWITCHES SHOWN IN THE 'OUT' POSITION

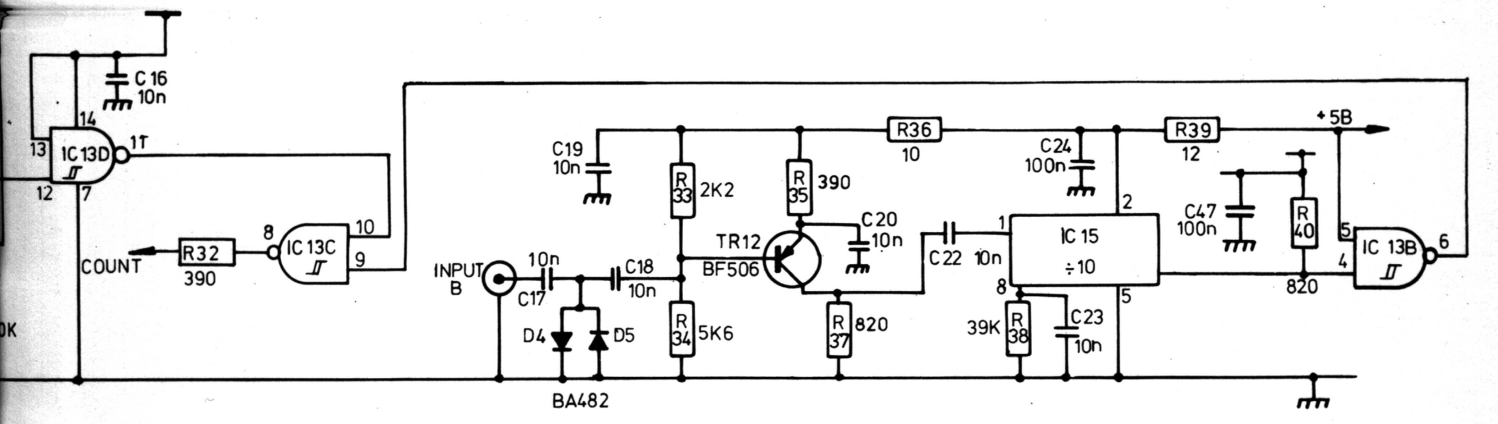
DISPLAY PCB INTERCONNECTIONS

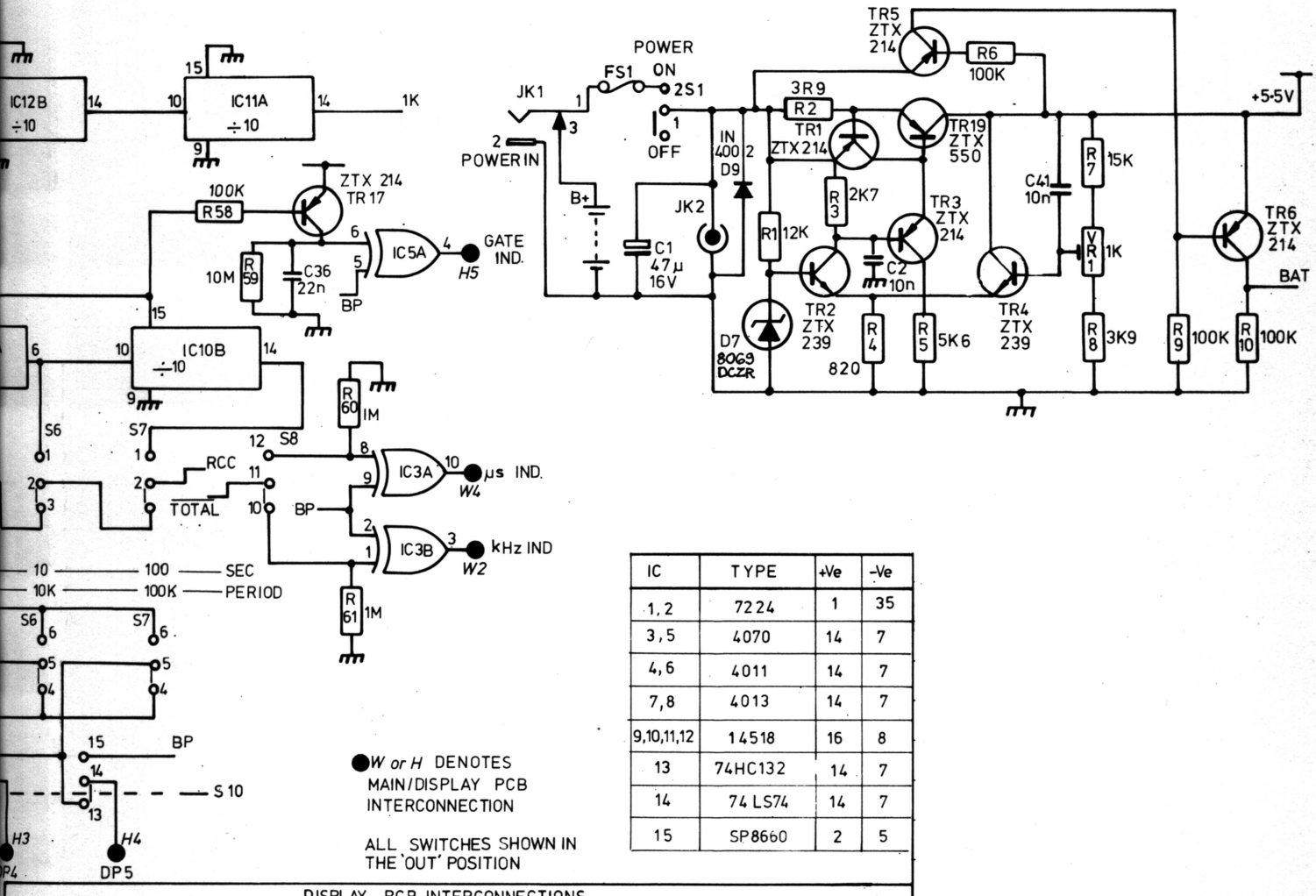
| LCD. PIN | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SEGMENT | NC | BP | BP | GATE IND | E8 | D8 | C8 | E7 | D7 | C7 | E6 | D6 | C6 | DP5 | E5 | D5 | C5 | DP4 |
| IC/ PIN | | 1,2/5 | 1,2/5 | – | 1/24 | 1/23 | 1/22 | 1/17 | 1/16 | 1/15 | 1/10 | 1/9 | 1/8 | – | 1/2 | 1/40 | 1/39 | – |
| LCD PIN | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 |
| SEGMENT | E4 | D4 | C4 | DP3 | E3 | D3 | C3 | DP2 | E2 | D2 | C2 | DP1 | E1 | D1 | C1 | KHz IND | BAT IND | µS IND |
| IC/ PIN | 2/24 | 2/23 | 2/22 | – | 2/17 | 2/16 | 2/15 | – | 2/10 | 2/9 | 2/8 | – | 2/2 | 2/40 | 2/39 | – | – | – |
| LCD PIN | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 |
| SEGMENT | B1 | A1 | F1 | G1 | B2 | A2 | F2 | G2 | B3 | A3 | F3 | G3 | B4 | A4 | F4 | G4 | B5 | A5 |
| IC/PIN | 2/38 | 2/37 | 2/4 | 2/3 | 2/7 | 2/6 | 2/12 | 2/11 | 2/14 | 2/13 | 2/19 | 2/18 | 2/21 | 2/ | 2/20 | 2/25 | 1/38 | 1/37 |
| LCD PIN | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | | |
| SEGMENT | F5 | G5 | B6 | A6 | F6 | G6 | B7 | A7 | F7 | G7 | B8 | A8 | F8 | G8 | O/F IND | NC | | |
| IC/ PIN | 1/4 | 1/3 | 1/7 | 1/6 | 1/12 | 1/11 | 1/14 | 1/13 | 1/19 | 1/18 | 1/21 | 1/20 | 1/26 | 1/25 | – | – | | |

## CIRCUIT DIAGRAM
**(Issue 10 onwards)**




| | |
|---|---|
| L.C.D. PIN | |
| SEGMENT | |
| IC/ PIN | |
| LCD PIN | |
| SEGMENT | |
| IC/ PIN | |
| LCD PIN | |
| SEGMENT | |
| IC/ PIN | |
| LCD PIN | |
| SEGMENT | |
| IC/ PIN | |




| IC | TYPE | +Ve | -Ve |
|---|---|---|---|
| 1,2 | 7224 | 1 | 35 |
| 3,5 | 4070 | 14 | 7 |
| 4,6 | 4011 | 14 | 7 |
| 7,8 | 4013 | 14 | 7 |
| 9,10,11,12 | 14518 | 16 | 8 |
| 13 | 74HC132 | 14 | 7 |
| 14 | 74 LS74 | 14 | 7 |
| 15 | SP8660 | 2 | 5 |

●*W or H* DENOTES MAIN/DISPLAY PCB INTERCONNECTION

ALL SWITCHES SHOWN IN THE 'OUT' POSITION

DISPLAY PCB INTERCONNECTIONS

| L.C.D. PIN | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SEGMENT | NC. | BP | BP | GATE IND | E8 | D8 | C8 | E7 | D7 | C7 | E6 | D6 | C6 | DP5 | E5 | D5 | C5 | DP4 |
| IC/ PIN | | 1,2/5 | 1,2/5 | – | 1/24 | 1/23 | 1/22 | 1/17 | 1/16 | 1/15 | 1/10 | 1/9 | 1/8 | – | 1/2 | 1/40 | 1/39 | – |
| LCD PIN | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 |
| SEGMENT | E4. | D4 | C4 | DP3 | E3 | D3 | C3 | DP2 | E2 | D2 | C2 | DP1 | E1 | D1 | C1 | KHz IND | BAT IND | µS IND |
| IC/ PIN | 2/24 | 2/23 | 2/22 | – | 2/17 | 2/16 | 2/15 | – | 2/10 | 2/9 | 2/8 | – | 2/2 | 2/40 | 2/39 | – | – | – |
| LCD PIN | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 |
| SEGMENT | B1 | A1 | F1 | G1 | B2 | A2 | F2 | G2 | B3 | A3 | F3 | G3 | B4 | A4 | F4 | G4 | B5 | A5 |
| IC/PIN | 2/38 | 2/37 | 2/4 | 2/3 | 2/7 | 2/6 | 2/12 | 2/11 | 2/14 | 2/13 | 2/19 | 2/18 | 2/21 | 2/ | 2/20 | 2/25 | 1/38 | 1/37 |
| LCD PIN | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | | |
| SEGMENT | F5 | G5 | B6 | A6 | F6 | G6 | B7 | A7 | F7 | G7 | B8 | A8 | F8 | G8 | O/F IND | NC | | |
| IC/ PIN | 1/4 | 1/3 | 1/7 | 1/6 | 1/12 | 1/11 | 1/14 | 1/13 | 1/19 | 1/18 | 1/21 | 1/20 | 1/26 | 1/25 | – | – | | |